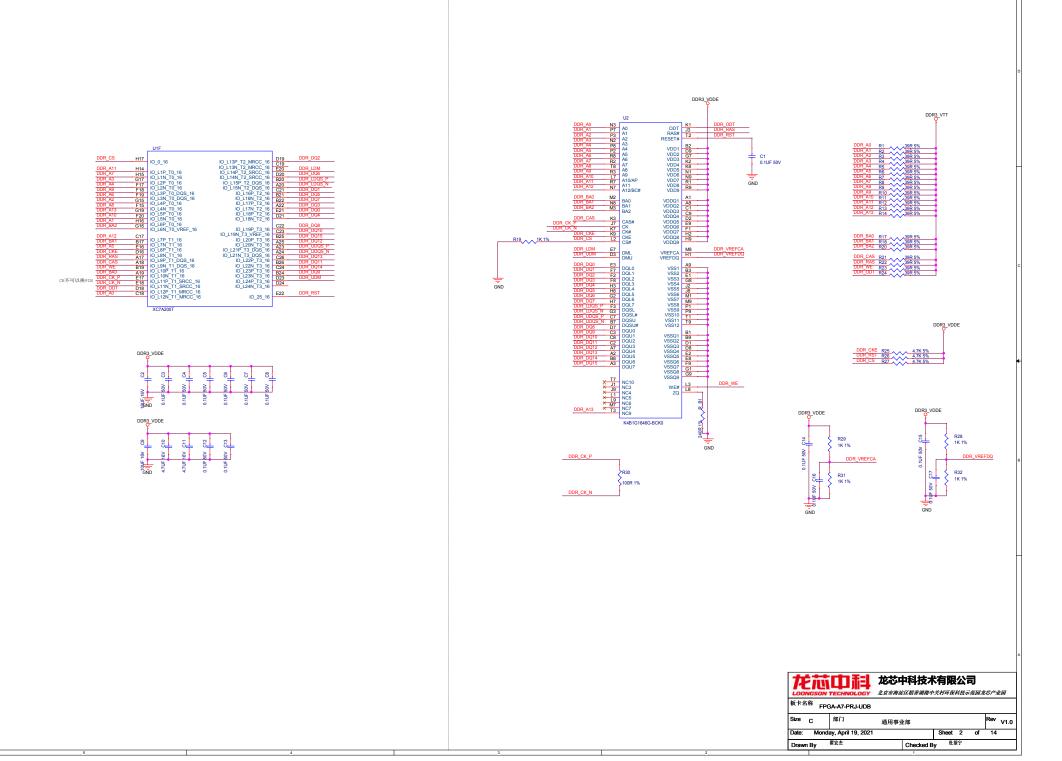
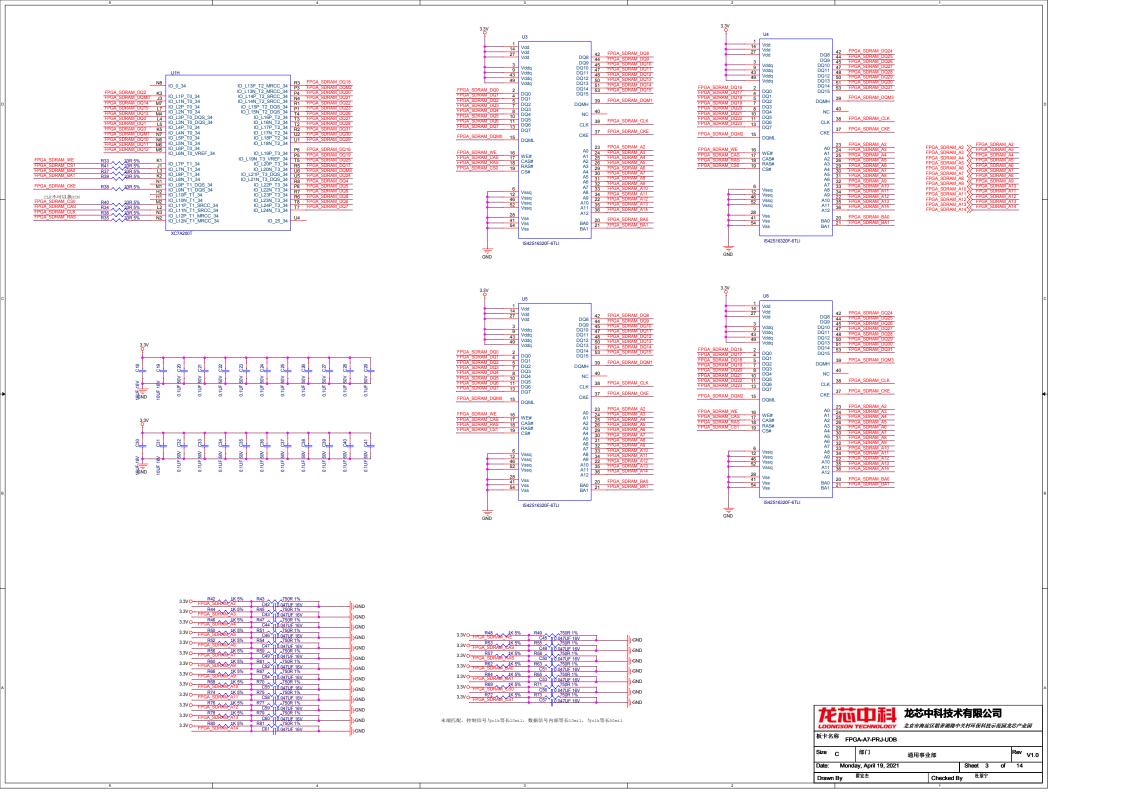


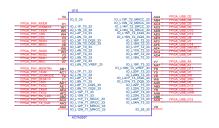
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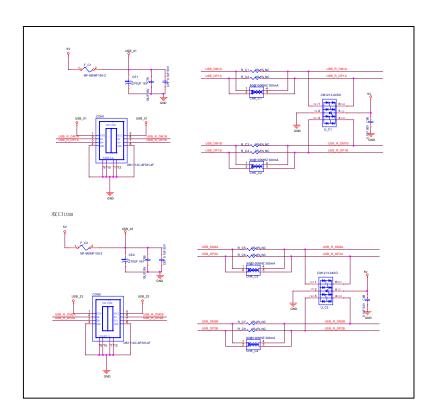
Checked By

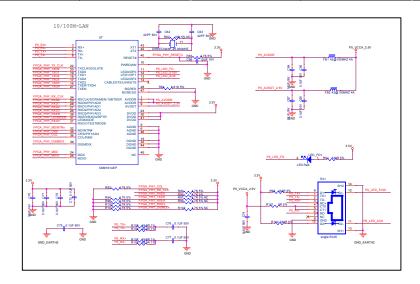
Drawn By

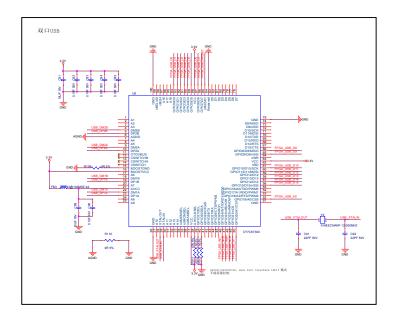




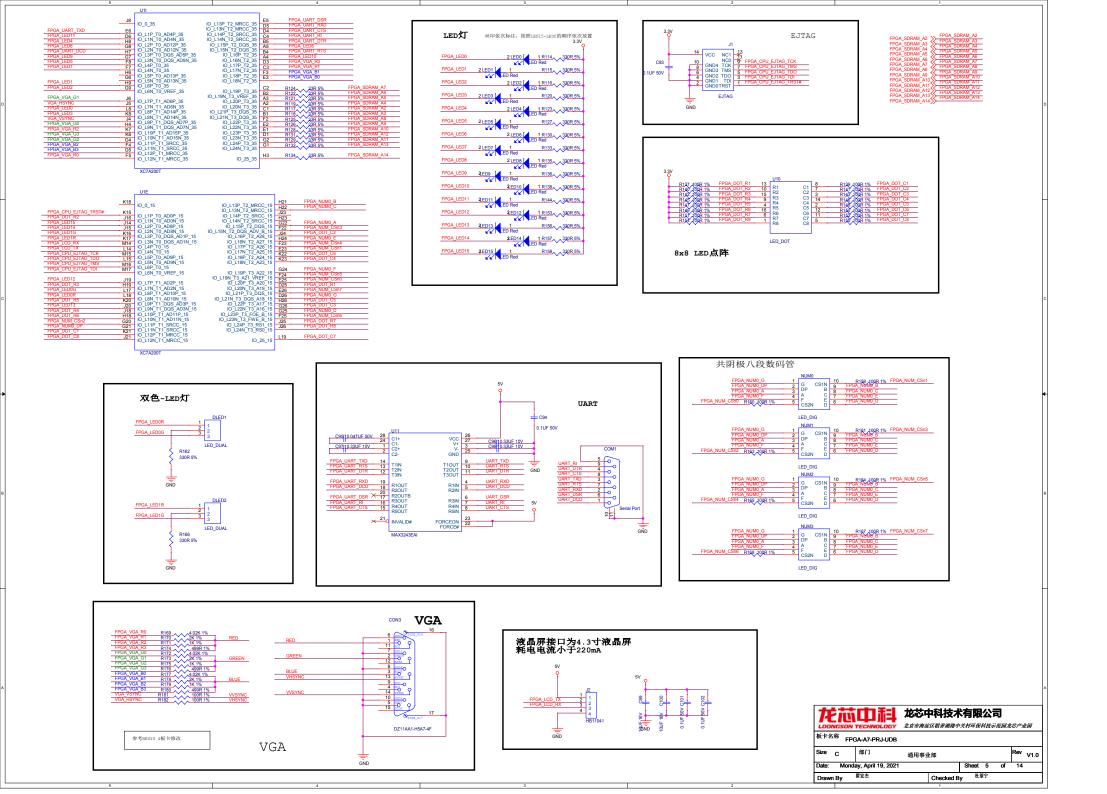


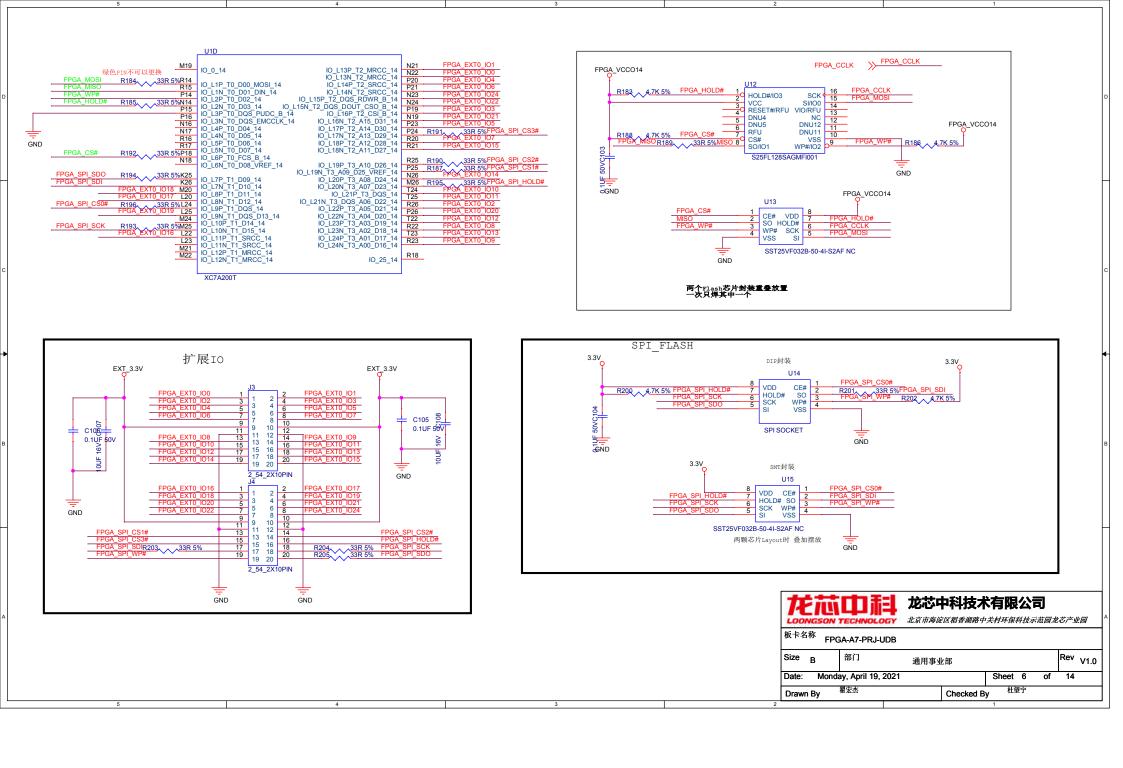


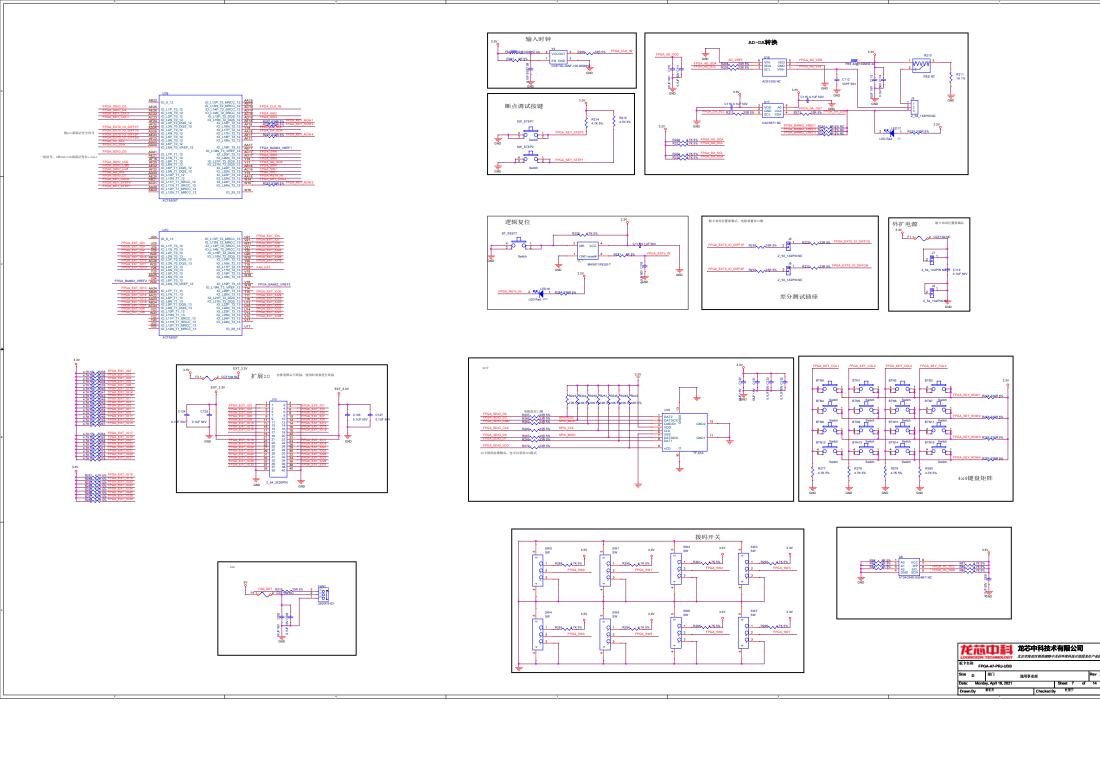


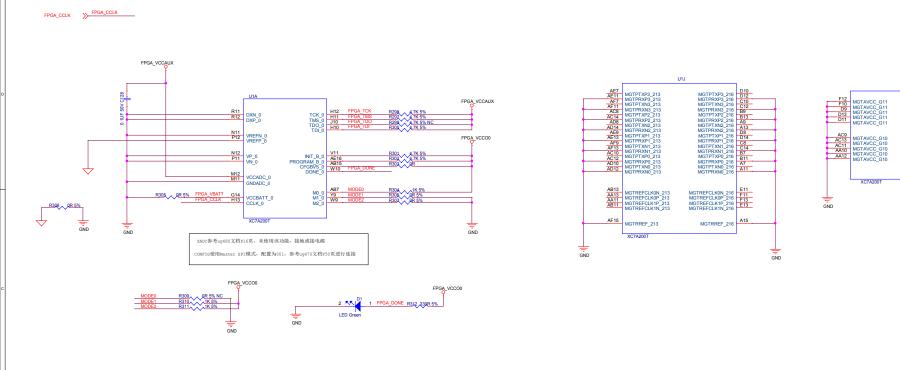




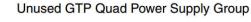








FPGA VCCAUX



If none of the GTP Quads in a power supply group are used in the application, the GTP Quad device pins can be connected as shown in Table 5-4.

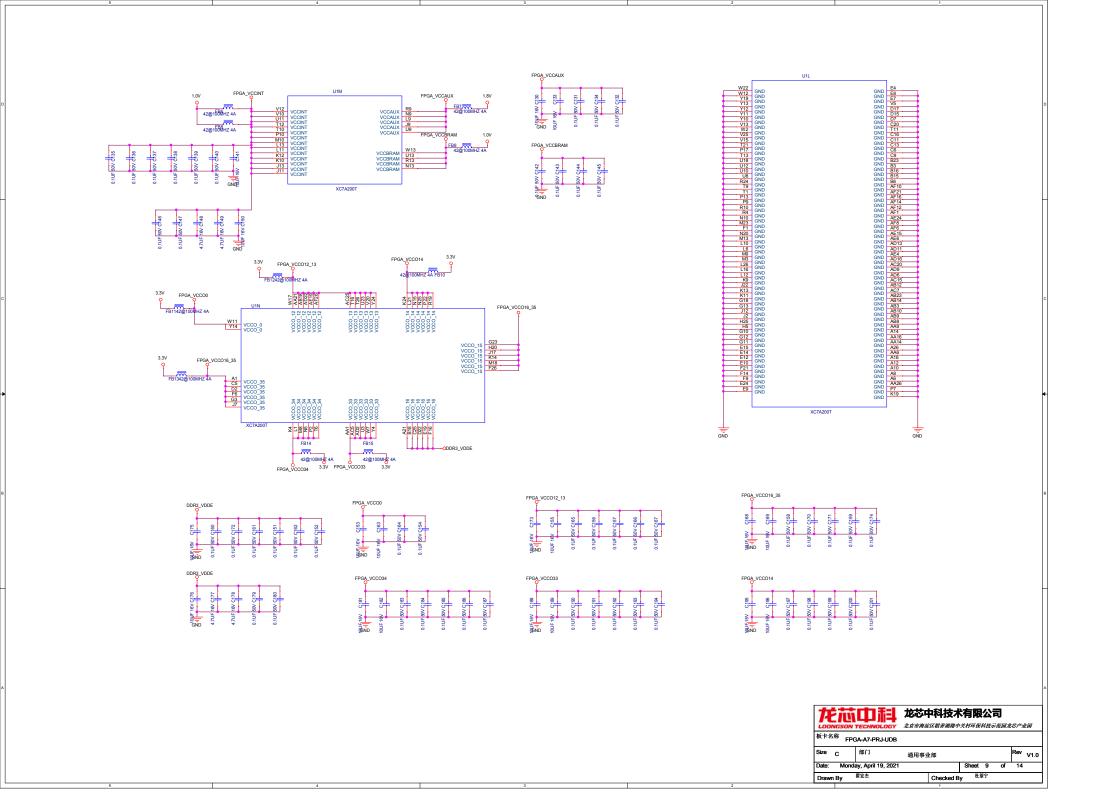
Table 5-4: Unused GTP Quad Column Connections

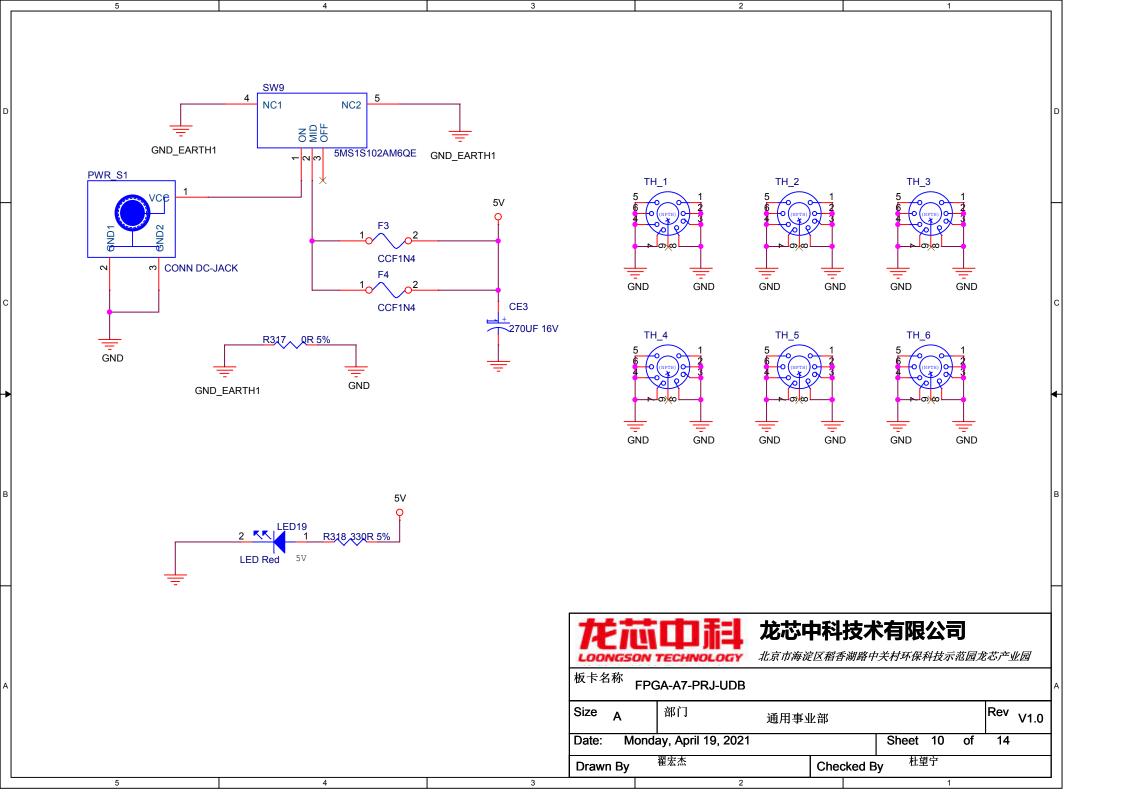
Pin or Pin Pair of the Unused GTP Quad	Connection	
MGTAVCC	GND	
MGTAVTT	GND	
MGTREFCLKP/MGTREFCLKN	Float	
MGTRXP/MGTRXN	GND	
MGTTXP/MGTTXN	Float	
MGTRREF <sup>(1)</sup>	GND	

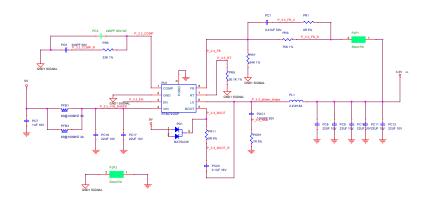
## Notes:

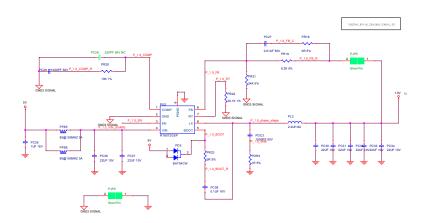
 This is the only scenario when the MGTRREF pins can be connected to ground. In all other scenarios, these pins must be connected for normal operation.

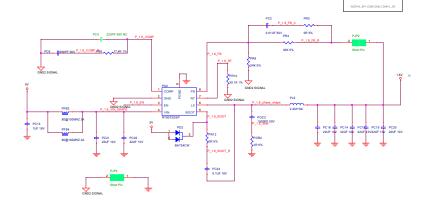


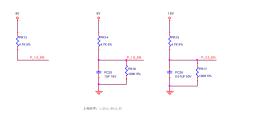












V <sub>OUT</sub> (V)	R <sub>FB1</sub> (kΩ)	R <sub>FB2</sub> (kΩ)	R <sub>C</sub> (kΩ)	C <sub>C</sub> (nF)	L (µH)	C <sub>OUT</sub>
3.3	75	24	33	0.33	0.47	Cer. 20µF + E-Cap 100µF
2.5	51	24	24	0.47	0.47	Cer. 20µF + E-Cap 100µF
1.8	30	24	18	0.56	0.47	Cer. 20µF + E-Cap 100µF
1.5	21	24	15	0.68	0.33	Cer. 20µF + E-Cap 100µF
1.2	12	24	12	1	0.33	Cer. 20μF + E-Cap 100μF
1	6	24	10	1	0.33	Cer. 20µF + E-Cap 100µF



