The Design and Usage of a Operational Amplifier

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***Abstract*—This document details the design of an operational amplifier and using it to design a non-inverting amplifier. The design process of the amplifier will involve a DC analysis for purposes of biasing, an AC analysis for the purposes of gain, and an AC sweep for the purposes of frequency response.**

***Index Terms*—Operational Amplifier, Circuits, Feedback, Frequency Response**

I. Introduction

THE Operational Amplifier, otherwise referred to as an Op-Amp, operates on a differential input with an "open-loop" gain of typically at or exceeding 60 dB, input resistance of typically at or exceeding 10 MΩ, and output resistance typically at or exceeding 100 Ω. As such, the current that enters the Op-Amp is typically in the range of μA. As such, the ideal Op-Amp is considered to have infinite open-loop gain, infinite input resistance, and zero output resistance. Given this description, an Op-Amp may be implemented in many different ways. The Op-Amp considered here will consist of three stages using BJT transistors: the Q2N3904 and the Q2N3906.

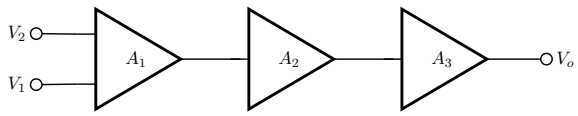

Fig. 1. Multi-Stage Amplifier Representation

Fig. 2 shows the implementation of the Op-Amp without frequency compensation.

Ideally, the open-loop gain of the Op-Amp is given by the product of the stage gains, however, each stage will have an input and output resistance. Thus, the product of all of the gains will also be multipled by ratios derived from voltage division.

$$A = A_1A_2A_3 \cdot \left(\frac{Z_{i_2}}{Z_{o_1} + Z_{i_2}} \cdot \frac{Z_{i_3}}{Z_{o_2} + Z_{i_3}} \cdot \frac{Z_L}{Z_{o_3} + Z_L} \right) \quad (1)$$

We can call the product of these ratios the "transmission" of the Op-Amp and denote it as σ, where the transmission of each stage will be denoted as σ_1, σ_2, and σ_3 respectively.

$$\sigma = \sigma_1\sigma_2\sigma_3 = \frac{Z_{i_2}}{Z_{o_1} + Z_{i_2}} \cdot \frac{Z_{i_3}}{Z_{o_2} + Z_{i_3}} \cdot \frac{Z_L}{Z_{o_3} + Z_L} \quad (2)$$

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Ideally, we don't want to lose any output, thus, we want each ratio to be one and this σ to be ideally one. Practically, σ should be close to one if each amplifier stage is designed well. Before the gain of each stage is calculated, we must first consider the biasing of the transistors within the Op-Amp.

II. The Resistances and Stage Gains of the Op-Amp

A. Finding the Resistor Values

1) Current Mirror Load and Finding Resistor R_1: The first stage of the Op-Amp, which we will denote S_1, will receive the inputs V_2 and V_1. It will also be supplied directly with a current source; where this current source is constructed using a current mirror.

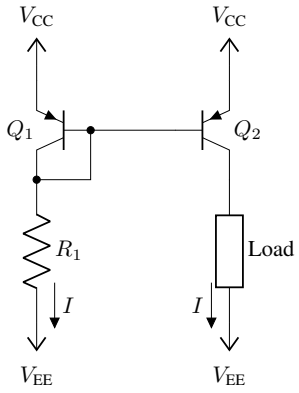

Fig. 3. The Current Mirror Load

With the short from base to collector for Q_1, the collector voltage of Q_1 is now ideally the base voltage of Q_1. Since the bases of Q_1 and Q_2 are shorted together, the base voltages of Q_1 and Q_2 are made ideally equivalent. Since the emitters Q_1 and Q_2 are both wired to V_{CC}, they also have equal emitter voltages. Thus, the base to emitter voltage for Q_1 and Q_2 are equal. As a result, the current through Q_1 will be ideally the same as the current through Q_2, and so the current is "mirrored". With a nodal analysis, we see that I depends on the potential difference across R_1, and with the short from collector to base, we see that this potential difference is $V_{CC} - (V_{EE} + V_{BE})$, thus we have an equation for I.

$$I = \frac{V_{CC} - V_{EE} - V_{BE}}{R_1} \quad (3)$$

I will be the current needed to bias the amplifier, and as such, we can derive an equation for R_1 as a function of I using equation 3.

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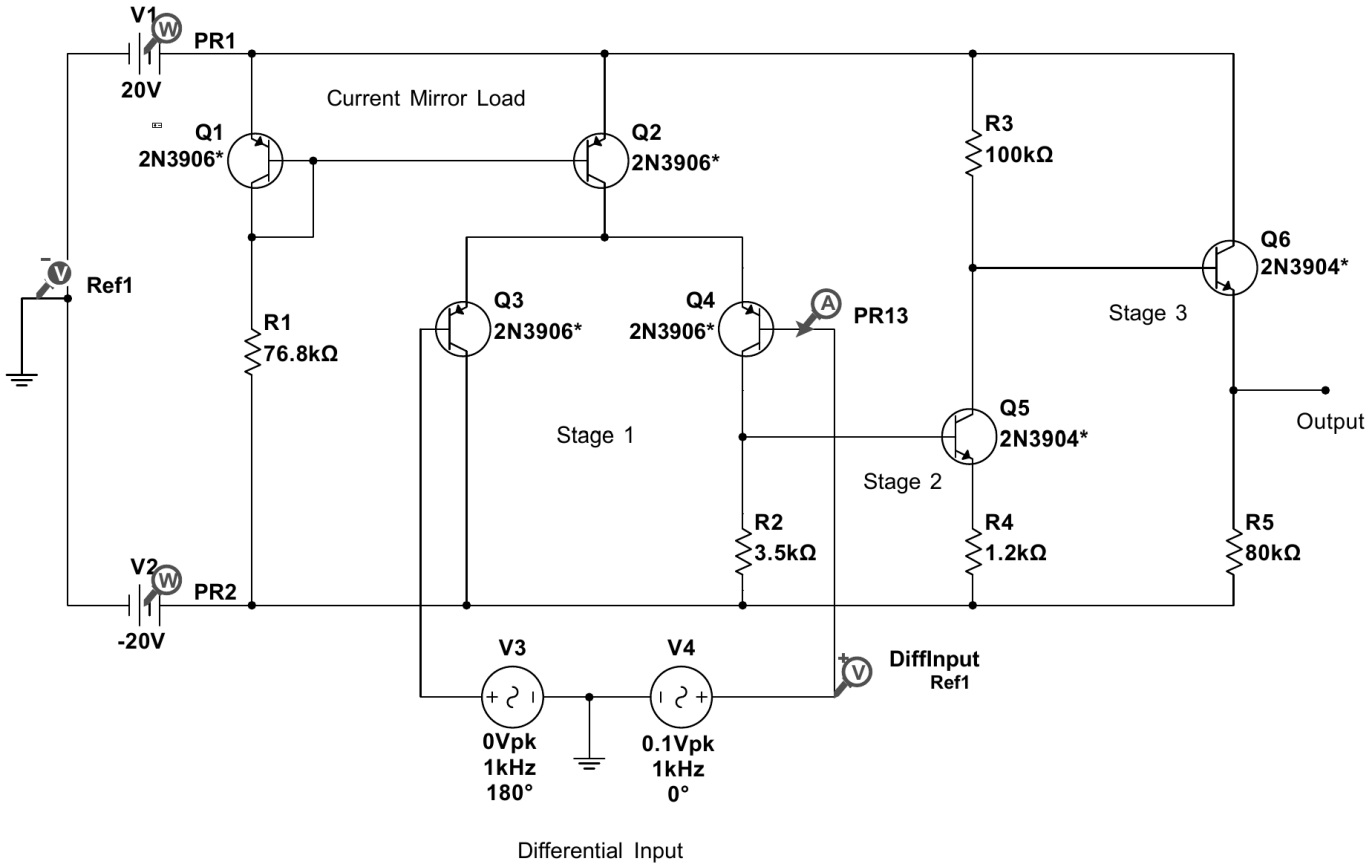


Fig. 2. Op-Amp Schematic Without Frequency Compensation

$$R_1 = \frac{V_{\text{CC}} - V_{\text{EE}} - V_{\text{BE}}}{I} \tag{4}$$

Thus, R_1 will change the biasing of the Op-Amp, but it will not directly affect the gain of the circuit. This will not be the case for the other resistors.

2) The Differential Stage and the First Stage Gain A_1: The first stage of the Op-Amp is a differential bipolar amplifier; in which PNP transistors are used and the output is single-sided.

Since the output of this differential amplifier is fed into another amplifier (the second stage of the Op-Amp), there will be some finite load at the output. The impedance of this load will then be the input impedance of the second stage, Z_{i_2}. The small signal equivalent of the differential amplifier can be used to determine the gain A_1, but due to the single-sided output, only the half-circuit is needed. However, note that the input is differential, thus the input of the amplifier will be half of the actual input; in which the DC offset goes to AC ground.

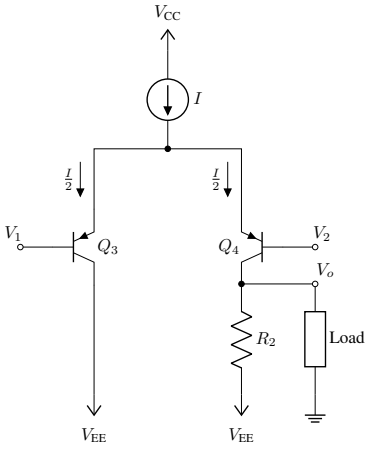


Fig. 4. The Differential Amplifier

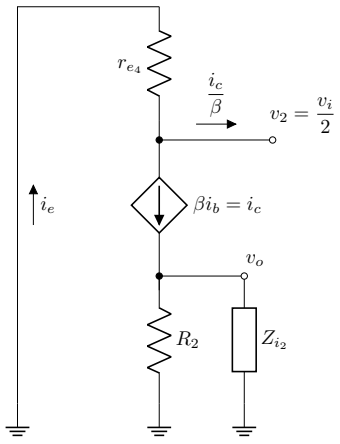


Fig. 5. The Differential Amplifier Small Signal Equivalent

From the small signal half circuit, nodal analysis suggests

$$i_e = -\frac{v_2}{r_{e_4}} \implies i_e = -\frac{1}{2} g_{m_4} v_i \tag{5}$$

as well as

$$i_c = \frac{v_o}{R_2 \parallel Z_{i_2}} \tag{6}$$

Using the current relationship between i_e and i_c for a bipolar junction transistor, we also find

$$i_c = \frac{\beta}{\beta + 1} i_e \implies \frac{v_o}{R_2 \parallel Z_{i_2}} = -\frac{\beta}{2(\beta + 1)} g_{m_4} v_i \tag{7}$$

From equation (7), the gain can be derived as so.

$$\frac{v_o}{v_i} = A_1 = -\frac{\beta}{2(\beta + 1)} g_{m_4} (R_2 \parallel Z_{i_2}) \tag{8}$$

However, it's not yet clear what resistor values A_1 depends on until an expression for Z_{i_2} is found. This impedance will be derived after all of the stage gains are found.

3) The Common Emitter Amplifier and the Second Stage Gain A_2: The second stage of the Op-Amp is a common emitter amplifier; in which a NPN transistor is used.

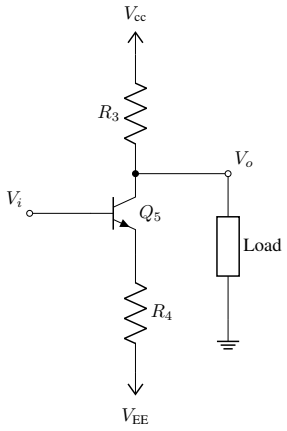


Fig. 6. The Common Emitter Amplifier

Similar to the first stage, the output of the common emitter amplifier will be fed into the third stage, and the impedance of the load will then be the input impedance of the third stage, Z_{i_3}. The gain can be determined by using the small signal equivalent model.

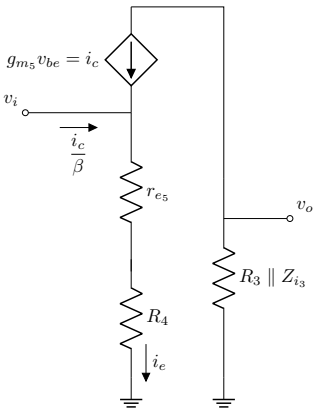


Fig. 7. The Common Emitter Amplifier Small Signal Equivalent

From the small signal equivalent model, i_e and i_e can be expressed using Ohm's Law.

$$i_c = -\frac{v_o}{R_3 \parallel Z_{i_3}} \tag{9}$$

$$i_e = \frac{v_i}{r_{e_5} + R_4} \tag{10}$$

Thus, the gain A_2 can be derived.

$$\frac{v_o}{v_i} = A_2 = -\frac{R_3 \parallel Z_{i_3}}{r_{e_5} + R_4} \tag{11}$$

As with the first stage gain, Z_{i_3} must be derived before determing which resistors the second stage gain will depend on.

4) The Common Collector Amplifier and the Third Stage Gain A_3: The third stage of the Op-Amp is a common collector amplifier; which is also known as a emitter-follower, and is implemented using a NPN transistor.

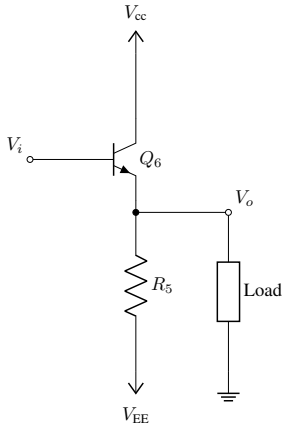


Fig. 8. The Emitter-Follower

While the output of this amplifier will not be fed into another stage, it will be connected to some load, such as a feedback system. That said, this is simply a buffer amplifier; in which there is no amplification nor, ideally speaking, attenuation. By using the small signal model, this can be proven.

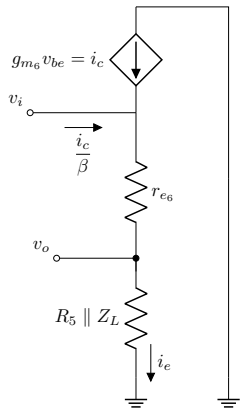


Fig. 9. The Emitter-Follower Small Signal Equivalent

From the small signal model, v_o can be expressed using voltage division, in which r_{e_6} and $R_5 \parallel Z_L$ form the voltage divider.

$$v_o = \frac{R_5 \parallel Z_L}{r_{e_6} + R_5 \parallel Z_L} v_i \tag{12}$$

Thus, the gain of the third stage can be derived.

$$\frac{v_o}{v_i} = A_3 = \frac{R_5 \parallel Z_L}{r_{e_6} + R_5 \parallel Z_L} \tag{13}$$

Note that for $Z_L = \infty$, the equation is simplified.

$$\frac{v_o}{v_i} = A_3 = \frac{R_5}{r_{e_6} + R_5} \tag{14}$$

Practically, r_{e_6} is usually magnitudes smaller than $R_5 \parallel Z_L$; in which both Z_L and R_5 are usually magnitudes above r_{e_6}. Thus, there are two limit conditions we can consider for A_3 to verify that the third stage is indeed a buffer amp.

$$\lim_{r_{e_6} \to 0} \frac{R_5 \parallel Z_L}{r_{e_6} + R_5 \parallel Z_L} = \frac{R_5 \parallel Z_L}{R_5 \parallel Z_L} = 1 \tag{15}$$

$$\lim_{R_5 \parallel Z_L \to \infty} \frac{R_5 \parallel Z_L}{r_{e_6} + R_5 \parallel Z_L} = \lim_{R_5 \parallel Z_L \to \infty} \frac{R_5 \parallel Z_L}{R_5 \parallel Z_L} = 1 \tag{16}$$

However, if Z_L is magnitudes smaller than R_5 and not magnitudes larger than r_{e_6}, then there will be a notable attenuation. The same applies if R_5 is magnitudes smaller than Z_L and not magnitudes larger than r_{e_6}. Practically speaking, the gain of this stage will never be 1 V/V, but it should be within 5% of 1 V/V. A fair assumption of A_3 would be 0.99 V/V, but this all depends on R_5 and Z_L. Note that while we are solving for stage gains here, R_5 will affect the biasing of the the third stage, so it will affect r_{e_6} as well.

B. Finding the Input and Output Resistances

1) The Input and Output Resistance of the First Stage: This resistance, seeing as the first stage is essentially the input stage, is also the input resistance of the Op-Amp. Thus, the resistance is expected to be in or above the mega-ohm range. In order to find this resistance, turn off all independent sources and apply a test source where the resistance is met. For the first stage, recall Fig. 5 and replace the differential input with test source v_x.

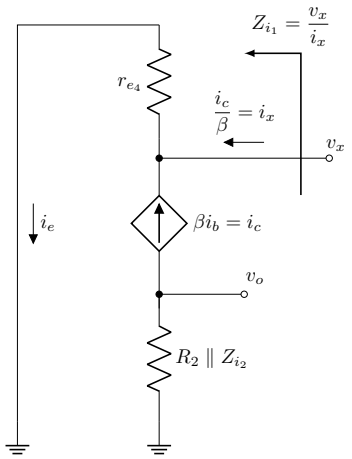


Fig. 10. Testing the Differential Amplifier for Input Resistance

Either by reflecting the emitter resistance r_{e_4} to the base or by using nodal analysis with the current relation between i_e and i_b, the input resistance is easily derived. We will use nodal analysis to find Z_{i_1}.

$$i_e = \frac{v_x}{r_{e_4}} \tag{17}$$

$$i_x = i_b \tag{18}$$

$$i_e = (1 + \beta) i_b \tag{19}$$

$$\implies \frac{v_x}{r_{e_4}} = (1 + \beta) i_x \tag{20}$$

$$\implies \frac{v_x}{i_x} = \boxed{Z_{i_1} = (1 + \beta) r_{e_4}} \tag{21}$$

Starting with the same small signal model, we can ground the input terminal and place a test source at the output terminal to find the output impedance of the first stage, Z_{o_1}. However, since we are inputting a source at the output, we will not consider the load is Z_{i_3}. Instead, this load will be disconnected.

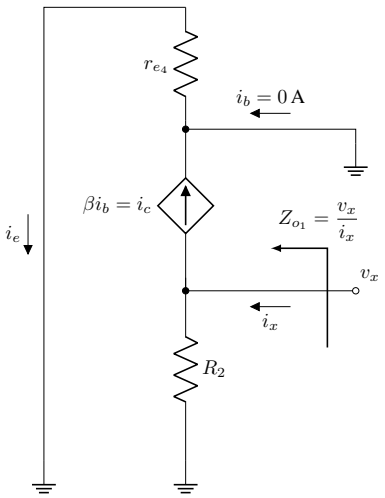


Fig. 11. Testing the Differential Amplifier for Output Resistance

Since the input is grounded, this means there is no voltage applied at the base of the transistor. Thus, there is no current

flowing into the terminal, making $i_e = i_c = 0\,\text{A}$ as they directly depend on i_b. As such, the dependent current source supplies no current, and so the current i_x is not split.

$$i_x = \frac{v_x}{R_2} \tag{22}$$

$$\implies \frac{v_x}{i_x} = Z_{o_1} = R_2 \tag{23}$$

2) The Input and Output Resistance of the Second Stage: The same process applied to the first stage is used here, however, now recall Fig. 7 as the circuit to analyze.

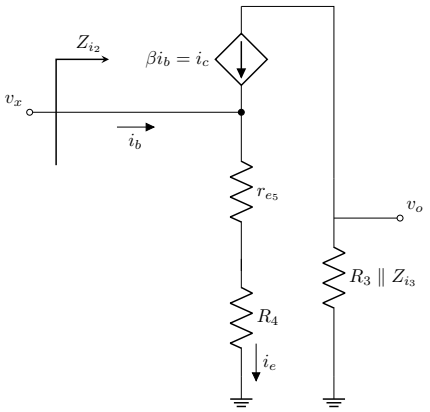


Fig. 12. Testing the Common Emitter Amplifier for Input Resistance

Using nodal analysis, finding the input impedance is a simple process.

$$i_b = i_x \tag{24}$$

$$i_e = (1+\beta)i_b \tag{25}$$

$$i_e = \frac{v_x}{r_{e_5} + R_4} \tag{26}$$

$$\implies (1+\beta)i_x = \frac{v_x}{r_{e_5} + R_4} \tag{27}$$

$$\implies \frac{v_x}{i_x} = Z_{i_2} = (\beta+1)(r_{e_5} + R_4) \tag{28}$$

Looking at Fig. 12, if the input terminal is grounded and v_x is placed at the output terminal, it's clear to see that the output resistance is simply R_3.

$$Z_{o_2} = R_3 \tag{29}$$

3) The Input and Output Resistance of the Third Stage: Recall the small signal model of the third stage (Fig. 9). The same process used for the previous two stages can be used here.

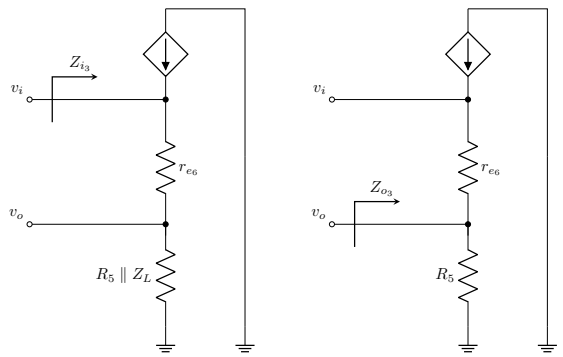


Fig. 13. Testing the Emitter-Follower for Input and Output Impedance

From this circuit, the input and output impedances are easy to see. For the input resistance, r_{e_6} and $R_5 \parallel Z_L$ are in series, thus they can be reflected to the base as a sum.

$$Z_{i_3} = (\beta+1)(r_{e_6} + R_5 \parallel Z_L) \tag{30}$$

For the output resistance, r_{e_6} and R_5 are in parallel.

$$Z_{o_3} = r_{e_6} \parallel R_5 \tag{31}$$

C. The Resistor Dependent Gain Equation

With all of the resistances and gains found, it's now possible to write an equation for A.

$$A_1 = -\frac{\beta(R_2 \parallel (\beta+1)(r_{e_5} + R_4))}{2(\beta+1)r_{e_4}} \tag{32}$$

$$A_2 = -\frac{R_3 \parallel (\beta+1)(r_{e_6} + R_5 \parallel Z_L)}{r_{e_5} + R_4} \tag{33}$$

$$\sigma_1 = \frac{(\beta+1)(r_{e_5} + R_4)}{R_2 + (\beta+1)(r_{e_5} + R_4)} \tag{34}$$

$$\sigma_2 = \frac{(\beta+1)(r_{e_6} + R_5 \parallel Z_L)}{R_3 + (\beta+1)(r_{e_6} + R_5 \parallel Z_L)} \tag{35}$$

$$\sigma_3 = \frac{Z_L}{(r_{e_6} \parallel R_5) + Z_L} \tag{36}$$

$$A = A_1 A_2 A_3 \cdot \sigma_1\sigma_2\sigma_3 = A' \cdot \sigma \tag{37}$$

See Eq. (38) for the full equation for A' and Eq. 39 for the full equation of σ. Since $\sigma \approx 1$, A' is the primary concern for determing A. Since A depends on the value of the emitter resistances, recall that the emitter resistances depend on the collector current flowing through the transistors, and those currents depend on the resistor values chosen for the Op-Amp. Thus, the resistor values must be chosen with consideration for gain A and proper biasing.

III. The DC Biasing of the Op-Amp

Recall that the emitter resistance of a BJT is given by the ratio of the thermal voltage V_T to the collector current I_c.

$$r_e = \frac{V_T}{I_c} \tag{40}$$

Looking back to the current mirror (Fig. 3) and Eq. (4), this is where the main part of the biasing comes into play. With the

$$A' = \frac{\beta(R_2 \parallel (\beta+1)(r_{e_5}+R_4))}{2(\beta+1)r_{e_4}} \cdot \frac{R_3 \parallel (\beta+1)(r_{e_6}+R_5 \parallel Z_L)}{r_{e_5}+R_4} \cdot \frac{R_5}{r_{e_6}+R_5} \tag{38}$$

$$\sigma = \frac{(\beta+1)(r_{e_5}+R_4)}{R_2+(\beta+1)(r_{e_5}+R_4)} \cdot \frac{(\beta+1)(r_{e_6}+R_5 \parallel Z_L)}{R_3+(\beta+1)(r_{e_6}+R_5 \parallel Z_L)} \cdot \frac{Z_L}{(r_{e_6} \parallel R_5)+Z_L} \tag{39}$$

equation, I can be anything. As such, we can already control r_{e_4} in regards to current.

$$I_{c_4} = \frac{\beta}{\beta+1} I_{e_4} \tag{41}$$

$$I_{e_4} = \frac{I}{2} \tag{42}$$

$$r_{e_4} = \frac{V_T}{I_{c_4}} = \frac{2\,(\beta+1)\,V_T}{\beta I} \tag{43}$$

In regards to r_{e_5}, the base current of Q_5 will be given by current division.

$$I_{b_5} = \frac{R_2}{R_2+Z_{i_2}} I_{c_4} \tag{44}$$

$$\implies I_{b_5} = \frac{R_2}{R_2+Z_{i_2}} \left(\frac{\beta}{\beta+1}\right) \frac{I}{2} \tag{45}$$

$$\implies I_{c_5} = \frac{R_2}{R_2+Z_{i_2}} \left(\frac{\beta^2}{\beta+1}\right) \frac{I}{2} \tag{46}$$

$$I_{c_5} = \frac{V_T}{r_{e_5}} \tag{47}$$

$$\implies \frac{(\beta+1)r_{e_5}+(\beta+1)R_4+R_2}{r_{e_5}} = \frac{R_2}{V_T}\left(\frac{\beta^2}{2(\beta+1)}\right) I \tag{48}$$

$$\implies r_{e_5} = \frac{R_2+(\beta+1)R_4}{\frac{\beta^2 I R_2}{2(\beta+1)V_T} - (\beta+1)} \tag{49}$$

Then for r_{e_6}, the base current of Q_6 will be given by another current division; in which the collector current of Q_5 will be divided between R_3 and Z_{i_3}.

$$I_{b_6} = \frac{R_3}{R_3+Z_{i_3}} I_{c_5} \tag{50}$$

$$\implies I_{b_6} = \frac{R_3}{R_3+Z_{i_3}} \cdot \frac{R_2}{R_2+Z_{i_2}} \left(\frac{\beta^2}{\beta+1}\right) \frac{I}{2} \tag{51}$$

$$\implies I_{c_6} = \frac{R_3}{R_3+Z_{i_3}} \cdot \frac{R_2}{R_2+Z_{i_2}} \left(\frac{\beta^3}{\beta+1}\right) \frac{I}{2} \tag{52}$$

$$I_{c_6} = \frac{V_T}{r_{e_6}} \tag{53}$$

$$\implies r_{e_6} = \frac{R_3+(\beta+1)(R_5 \parallel Z_L)}{\frac{\beta^3 I R_3}{2(\beta+1)V_T}\left(\frac{R_2}{R_2+Z_{i_2}}\right) - (\beta+1)} \tag{54}$$

However, despite deriving these equations, tweaking the resistor values based off of these equations will not always match the measured gain. This is because the equations always assume the transistors are always operating in active mode, and if a change in a resistor value pushes a transistor into saturation, these equations are no longer applicable.

IV. Experimenting with Resistor Values

While calculating the resistor values would be both difficult and likely inefficient, the equation derived for the open-loop gain without considering transmission loss, see Eq. (38), provides some incentive on how to tweak the resistor values.

A. Current Mirror Load

For the current mirror, R_1 set to $76.8\,\text{k}\Omega$ was found to properly bias the amplifier; in which the current supplied using this resistance can be calculated using Eq. (3), and when calculated, provides $I \approx 0.512\,\text{mA}$.

B. First Stage

For the first stage, since R_2 is in parallel with Z_{i_2}, increasing R_2 will not increase the gain. Instead, the parallel combination will approach the lesser resistance. So in order to increase the gain of the first stage, setting R_2 to $3.5\,\text{k}\Omega$ and tweaking R_4 would be a decent method.

C. Second Stage

Note that the second stage gain is inversely proportional to R_4, so while setting R_4 to a very high value would seem like a good idea as to increase the first stage gain, we instead want to limit R_4. Since R_4 is scaled by $\beta+1$ for the previous stage, this means R_4 will already be far larger from the perspective of the first stage than for the second stage. In this case, setting R_4 to $1.2\,\text{k}\Omega$ provides satisfactory results.

As for R_3, we have the same situation as with the first stage. Thus, we should pick a value for R_3 and then tweak R_5. As such, setting R_3 to $100\,\text{k}\Omega$ provides good results.

D. Third Stage

With the third stage, setting R_5 to a very large value, such as in the megaohms, would work unlike the first stage since, as Eq. (13) suggests, $R_5 \gg r_{e_6}$ provides gain close to $0\,\text{dB}$, which is ideal. However, this is only the case when the Op-Amp is not supplying a finite load. When a finite load Z_L is attached to the output terminal of the Op-Amp, R_5 will be parallel to this impedance, and as shown in Eq. (13), this effects the gain of the buffer stage. The effect can be shown by limits in which Z_L is kept constant while R_5 is taken to infinity.

$$\lim_{R_5 \to \infty} \frac{R_5 \parallel Z_L}{r_{e_6}+R_5 \parallel Z_L} = \frac{Z_L}{r_{e_6}+Z_L} \tag{55}$$

With this simplification, it is clear to see that R_5 is eventually disregarded as it is increased. This behavior is non-ideal because this means that the gain now depends largely on

Z_L. Specifically, the measure of how large Z_L is to r_{e_6}. For example, if R_5 was chosen to be $1000r_{e_6}$, then the buffer gain without a load would be $\frac{1000}{1001}$ V/V (see Eq. (14)). However, if we connect a load of $Z_L = 100r_{e_6}$, then firstly, the parallel combination can be computed. From there, we can compute the gain.

$$Z_L \parallel R_5 = 100r_{e_6} \parallel 1000r_{e_6} \tag{56}$$

$$= \frac{100r_{e_6} \cdot 1000r_{e_6}}{100r_{e_6} + 1000r_{e_6}} \tag{57}$$

$$= \frac{10^5}{1100} \cdot r_{e_6} \tag{58}$$

$$\implies A_3 = \frac{\frac{10^5}{1100} r_{e_6}}{r_{e_6} + \frac{10^5}{1100} r_{e_6}} \tag{59}$$

$$= \frac{\left(\frac{10^5}{1100}\right)}{\left(\frac{10^5+1100}{1100}\right)} \tag{60}$$

$$= \frac{10^5}{10^5 + 1100} = \frac{1000}{1011}\,\text{V/V} \tag{61}$$

$$\implies \Delta A_3 = \frac{1000}{1001} - \frac{1000}{1011} \approx 10^{-2}\,\text{V/V} \tag{62}$$

$$\approx 0.0863\,\text{dB} \tag{63}$$

While R_5 and Z_L only differed by a factor of ten, it's clear to see that this loss in gain can be increased if this factor increases, and that would be very likely if R_5 is in the range of megaohms. Thus, R_5 was chosen to be 80 kΩ.

V. Op-Amp Specifications With Regards to Resistor Values

A. Power Dissipation

With the resistor values chosen, the power dissipated by the Op-Amp is easily calculated. For currents that flow to V_{EE}, the sum of those currents multiplied by V_{EE} provides the power dissipated as a result of those currents.

$$P_{\text{EE}} = |V_{\text{EE}}| \sum_{i=1}^{N} I_i \tag{64}$$

Then for currents flowing to V_{CC}, replace V_{EE} with V_{CC}.

$$P_{\text{CC}} = V_{\text{CC}} \sum_{i=1}^{M} I_i \tag{65}$$

Thus, the total power dissipation is given by the following equation.

$$P_{\text{net}} = V_{\text{CC}} \sum_{i=1}^{M} I_i + |V_{\text{EE}}| \sum_{i=1}^{N} I_i \tag{66}$$

With this equation, the total power dissipation was found to be 58 mW. The simulation reported a total power dissipation of 58.4 mW.

B. Input Bias Current

Due to the nature of BJTs, there is some current introduced by the input terminal into our Op-Amp design. As such, this current is called the input current or input bias current. This current was found to be approximately 1 microamp.

C. Measured Open-Loop Gain

When performing an AC Sweep, the open-loop gain was found to be 61.84 dB. When applying equations (2), (38), (43), (49), and (54); the open-loop gain was calculated to be 62.6109 dB. Thus, the difference relative to the calculation was approximately 1.2%.

$$E\% = \frac{A_{\text{calculated}} - A_{\text{measured}}}{A_{\text{calculated}}} \approx 1.23\% \tag{67}$$

The value of σ was about 0.987.

D. Open-Loop Bandwidth and Dominant Pole

Bode plots for the open-loop gain and phase were created in Matlab. See Fig. 14 for open-loop gain and 15 for open-loop phase. The plots suggests that a pole exists at 258.73 kHz, thus a bandwidth of 0 Hz to 258.73 kHz.

E. Common-Mode Input Range

For the common-mode input range, the circuit analysis is only concerned with the first stage of the Op-Amp since it acts as the input stage. As such, referring back to Fig. 4, $V_{\text{CM}_{\text{min}}}$ and $V_{\text{CM}_{\text{max}}}$ can be calculated by assuming the saturation conditions $V_{CB} = 0.4\,\text{V}$, $V_{CE} = 0.3\,\text{V}$, and $V_{EB} = 0.7\,\text{V}$.

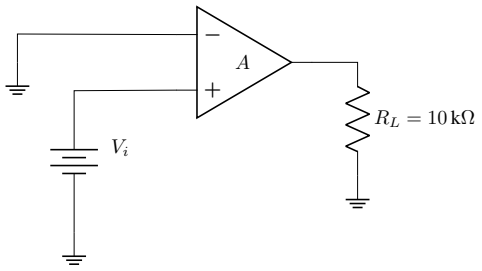
$$V_{\text{CM}_{\text{min}}} = I_c R_2 + V_{CB} - V_{\text{CC}} \tag{68}$$

$$\approx \frac{I}{2} R_2 + V_{CE} - V_{\text{CC}} = -18.7045\,\text{V} \tag{69}$$

$$V_{\text{CM}_{\text{max}}} = V_{\text{CC}} - V_{CE} - V_{EB} = 19\,\text{V} \tag{70}$$

VI. DC Transfer Characteristics

Now with the Op-Amp designed, we can now perform various tests on the Op-Amp. For the DC transfer characteristics of the Op-Amp, we will consider that the inverting terminal is grounded, the non-inverting terminal is connected to a DC supply, and there is a 10 kΩ load.



We will sweep V_i from -100 mV to 100 mV in steps of 0.1 mV, and the slope of the linear aspect of the DC Transfer characteristics will yield the gain. This gain be compared to the calculation of $A'\sigma$. The data collected from the DC sweep was processed in Matlab (see Fig. 16).

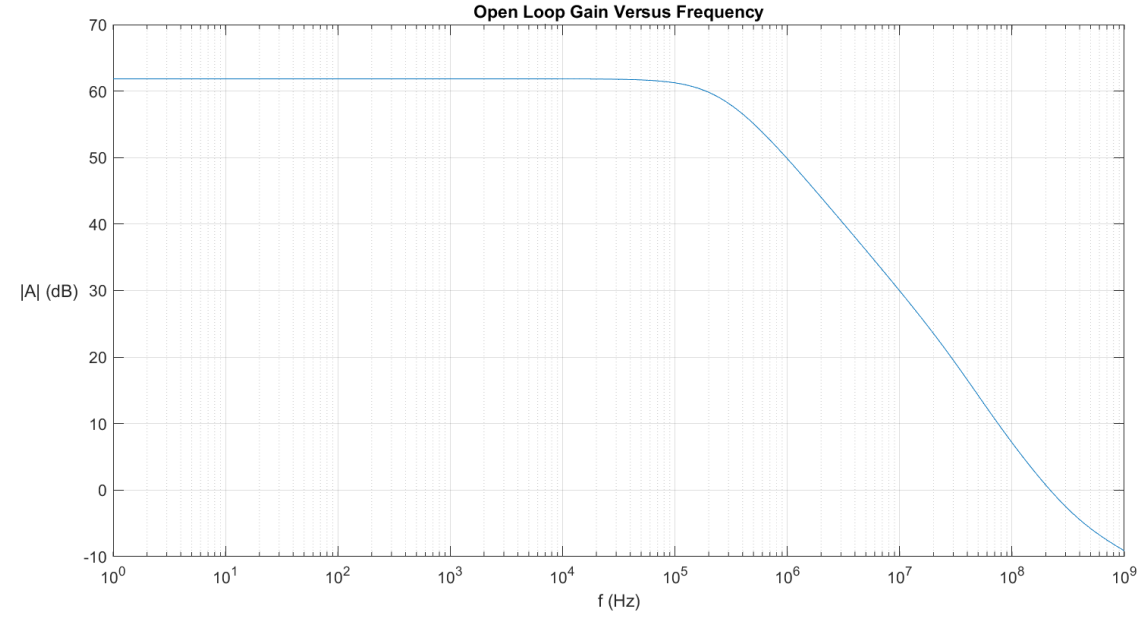


Fig. 14. Bode Plot of Open-Loop Gain

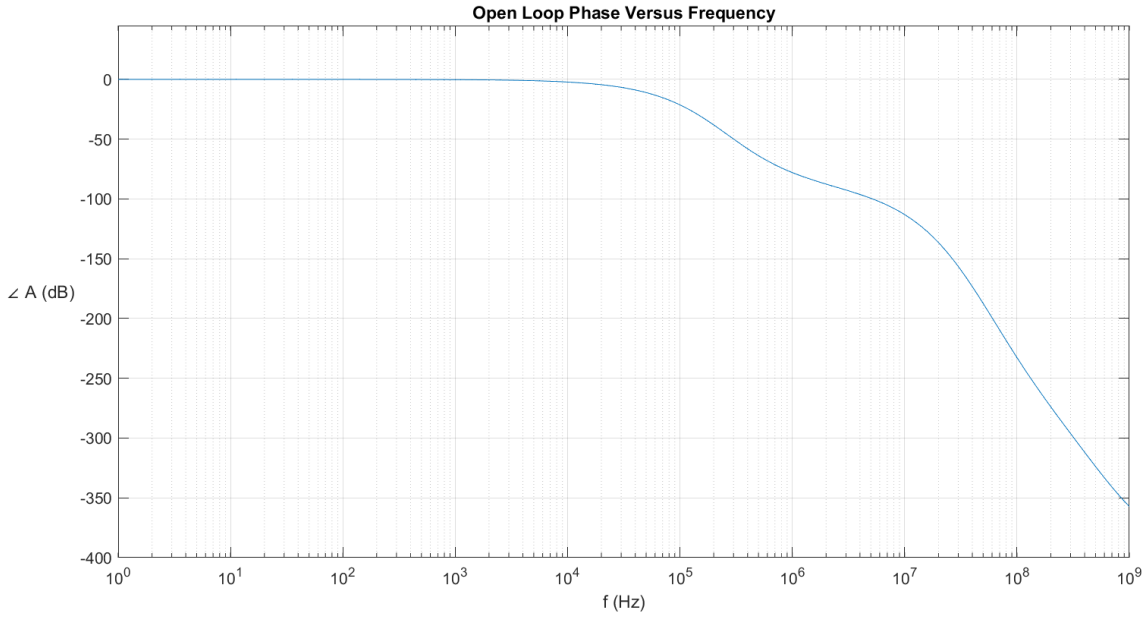


Fig. 15. Bode Plot of Open-Loop Phase

From the plot, the closest eyeball approximation to linear behavior between V_i and V_o is between 1 mV and 6 mV, in which the slope was calculated to be 1105.5 V/V, or in units of decibels, 60.871 dB. With the formula derived for the open-loop gain, the calculation provided 62.02 dB, thus presenting an error of approximately 2% relative to the calculation.

$$E\% = \frac{A_{\text{calculated}} - A_{\text{measured}}}{A_{\text{calculated}}} \approx 1.94\% \tag{71}$$

Compared to the gain with no attached load, which is equivalent to saying $Z_L = \infty$, there is an approximate loss of 0.969 dB, and this makes sense as $Z_L = 10\,\text{k}\Omega$ while $R_5 = 80\,\text{k}\Omega$.

VII. Frequency Compensation

Reviewing the bode plots (see Fig. 14 and Fig. 15), we see that at 0 dB, the phase shift is past -180°. As such, the system is unstable, or rather, if we were to introduce feedback, the system would undergo positive feedback. In order to implement the various Op-Amp circuits we are familiar with,

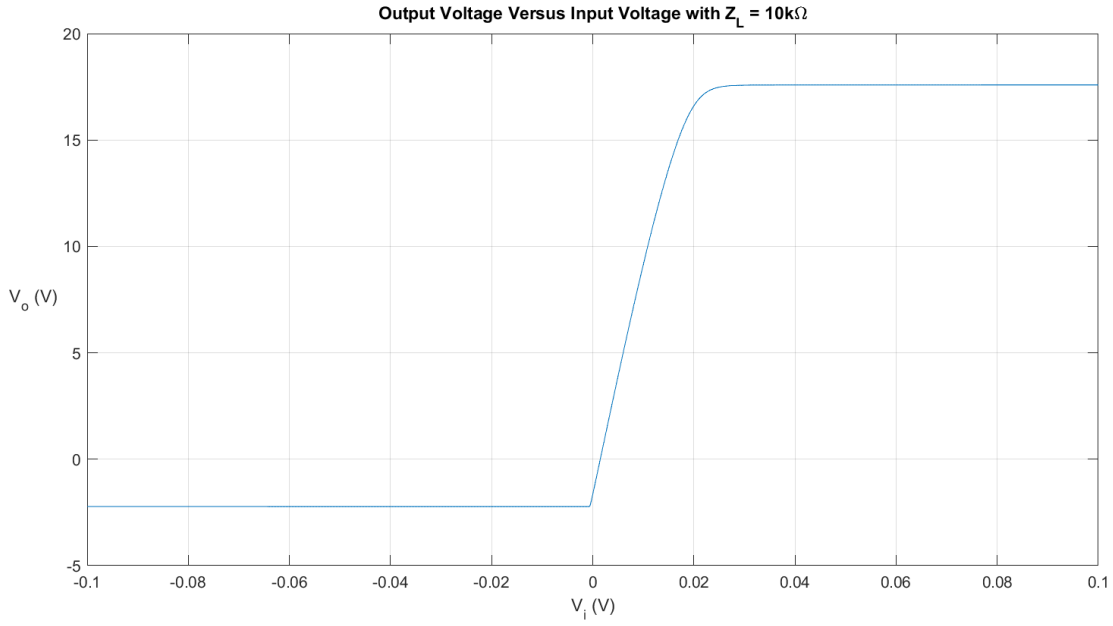


Fig. 16. DC Transfer Characteristics

such as a non-inverting amplifier or a weighted summer, we need to alter the design such that the phase shift is within -180° to 180° when the gain is 0 dB. While there are a few different methods of so-called frequency compensation, we will apply "Miller's compensation".

A. Miller's Compensation Capacitor

After experimenting with different feedback capacitor placements, the best placement was found to be a 200 pF capacitor at the third stage.

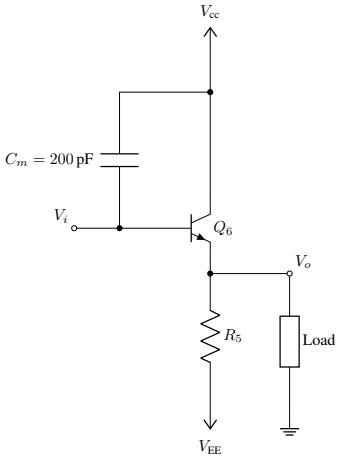


Fig. 17. The Frequency Compensated Emitter-Follower

Essentially, the capacitor will provide a pole, and due to Miller's effect, the compensation capacitor will be amplified. Thus, a smaller capacitor can be used, such as the chosen 200 pF capacitor. However, this new pole becomes the new dominant pole, resulting in a loss of bandwidth. However, at unity gain (0 dB), we now have a phase of approximately $-130°$, thus we are now stable and have a phase margin of approximately $50°$, which is greater than $45°$. See Fig. 18 and 19 for this drawback.

VIII. Implementing Feedback and Building a Non-Inverting Amplifier

With the frequency-compensated Op-Amp, we can now introduce feedback.

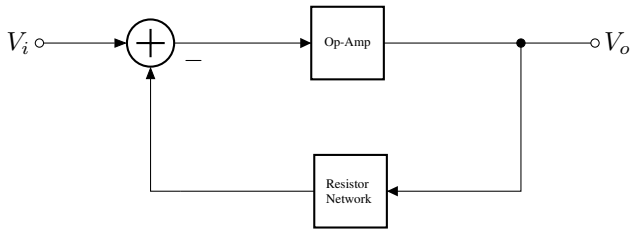


Fig. 20. Block Diagram for a Negative Feedback System

For a non-inverting amplifier, we expect the system to amplify the signal, but not invert it. Thus, for any input V_i, we expect the output to be $|A_f|\,V_i$, where A_f is the gain of the feedback system. As Fig. 20 suggests, the feedback gain A_f is given by the following equation.

$$A_f = \frac{A}{1 + A(s) \cdot B} = \frac{1}{\frac{1}{A(s)} + B} \tag{72}$$

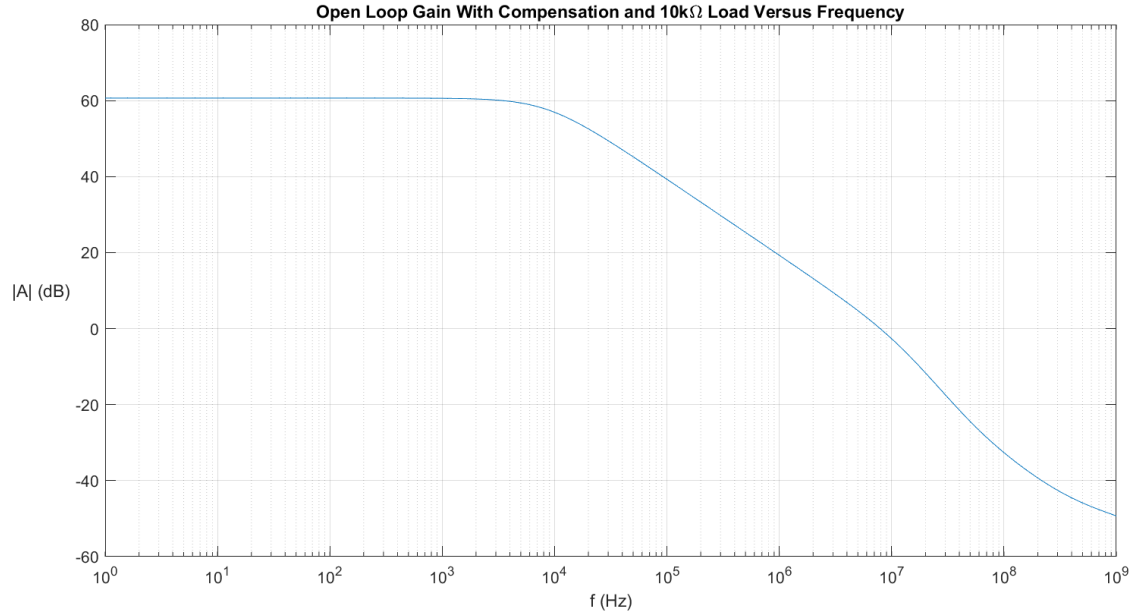


Fig. 18. Bode Plot of Open-Loop Gain After Frequency Compensation

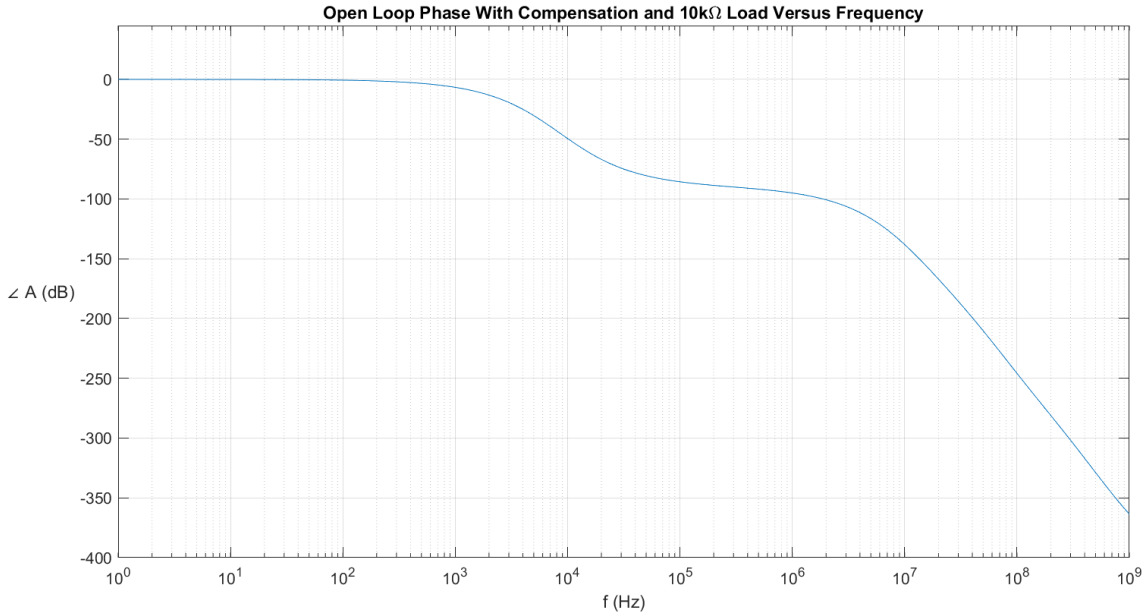


Fig. 19. Bode Plot of Open-Loop Phase After Frequency Compensation

Where $A(s)$ is the open-loop gain of the Op-Amp and B is the gain from feedback: the "loop gain". We have already designed $A(s)$, and for a desired A_f, we can solve for B.

$$B = \frac{1}{A_f} - \frac{1}{A(s)} = \frac{A(s) - A_f}{A_f A(s)} \tag{73}$$

While this suggests that B will or should be frequency-dependent, we can assume that $A(s)$ is constant if s is in the bandwidth found earlier. Thus, B can be implemented as a non-frequency dependent system when we consider this bandwidth.

$$B = \frac{1}{A_f} - \frac{1}{A} = \frac{A - A_f}{A_f A} \tag{74}$$

A. *Designing the Non-Inverting Amplifier*

The goal is to design a non-inverting amplifier with $A_f = 20\,\text{dB} = 10\,\text{V/V}$. Recall that A is already experimentally found

to be approximately $61.84\,\text{dB} = 1235.95\,\text{V/V}$. As such, B can be calculated.

$$A_f = 10 \tag{75}$$

$$A \approx 1235.95 \tag{76}$$

$$\implies B \approx \frac{1}{10} + \frac{1}{1235.95} \approx 0.10081\,\text{V/V} \tag{77}$$

This is the gain we expect from our resistor-network. Since the gain is less than one, we can consider using a *Voltage-Divider* network.

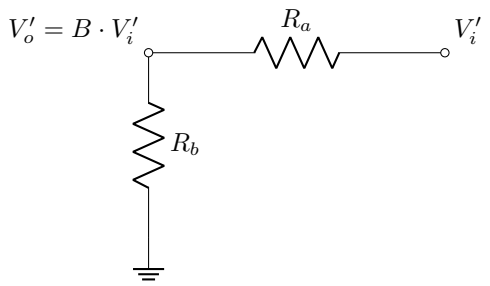


Fig. 21. Voltage-Divider Network

As the analysis suggests, B will simply be the ratio of R_b to the sum of R_a and R_b.

$$B = \frac{V_o'}{V_i'} = \frac{R_b}{R_a + R_b} \tag{78}$$

When we implement this as feedback into your system, $V_i' = V_o$ and $V_o' = B * V_o$. When we introduce the open-loop gain as our Op-Amp, we can use the idea that the Op-Amp sees a differential input; in which the input is the potential difference from the non-inverting terminal to the inverting terminal. As such, if we wire the output of our voltage-divider network to the inverting terminal of the Op-Amp, we essentially achieve the same functionality as the adder seen in Fig. 20; in which the adder acts as a subtracter.

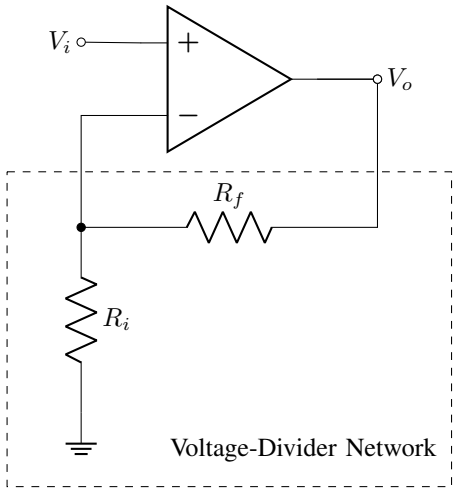


Fig. 22. Non-Inverting Amplifier

For the amplifier, we will let $R_a = R_f$ and $R_i = R_b$.

Seeing as we already calculated B, we can now select values for R_a and R_b. An easy way to do this is to solve for one resistor in terms of the other given that our network is relatively simple.

$$\text{Eq. (78)} \implies BR_a + BR_b = R_b \tag{79}$$

$$\implies R_b = \left(\frac{B}{1-B}\right) R_a \tag{80}$$

We can now select R_a and then simply calculate R_b. Alternatively, we can select R_b and then calculate R_a.

$$R_a = \left(\frac{1-B}{B}\right) R_b \tag{81}$$

Ideally, we should not lose any of our output. However, with a circuit, the feedback and resistor-network will force some of the output current to flow through the feedback loop, thus reducing the output. In order to remedy this, R_b can be chosen to be some resistance in the kilo-ohm range, thus reducing the amount of current that flows through the feedback loop as per current division. As such, we will choose R_a to be $15\,\text{k}\Omega$.

$$R_a = 15\,\text{k}\Omega \implies R_b \approx 1681.68\,\Omega \tag{82}$$

However, this is not an ideal number to work with, and in practice, is inefficient due to resistor tolerance. Thus we will select $1.65\,\text{k}\Omega$ for R_b. See Fig. 27 for the schematic of the non-inverting Op-Amp.

1) Input Impedance of the Non-Inverting Amp: With the feedback added, the input impedance of the entire system has changed. Without feedback, the input impedance would just be the input impedance of the first stage Z_{i_1}, but now, the input impedance is Z_i.

$$Z_i = Z_{i_1}(1 + AB) \approx 3.85\,\text{M}\Omega \tag{83}$$

To experimentally find the input impedance, we can apply a test source V_x to the terminal and measure the current entering the amplifier. From here, calculate the ratio of the test source voltage to input current, and this ratio should theoretically be the input impedance.

B. Results

With the non-inverting amplifier designed, we can now simulate it and verify that it works to our specifications. An AC Sweep was performed without a load attached to the output of the non-inverting amplifier. With that in mind, the bode plots of the gain and phase with feedback are provided (see Fig. 25 and 26).

When we apply a sinusoidal input $v_i = 2\sin(\omega t)$ with $f = 1\,\text{kHz}$, we observe the following. While we expect an output of approximately $v_o = 20\sin(\omega t)$, we instead get some kind of distortion (see Fig. 23). This is due to the results of the DC transfer as seen in Fig. 16, in which the linear operating range is only in the millivolts. With the feedback, this range failed to include up to 2 volts as shown in Fig. 24; in which our range of inputs that produce linear outputs is only between approximately -0.4 V and 1.8 V.

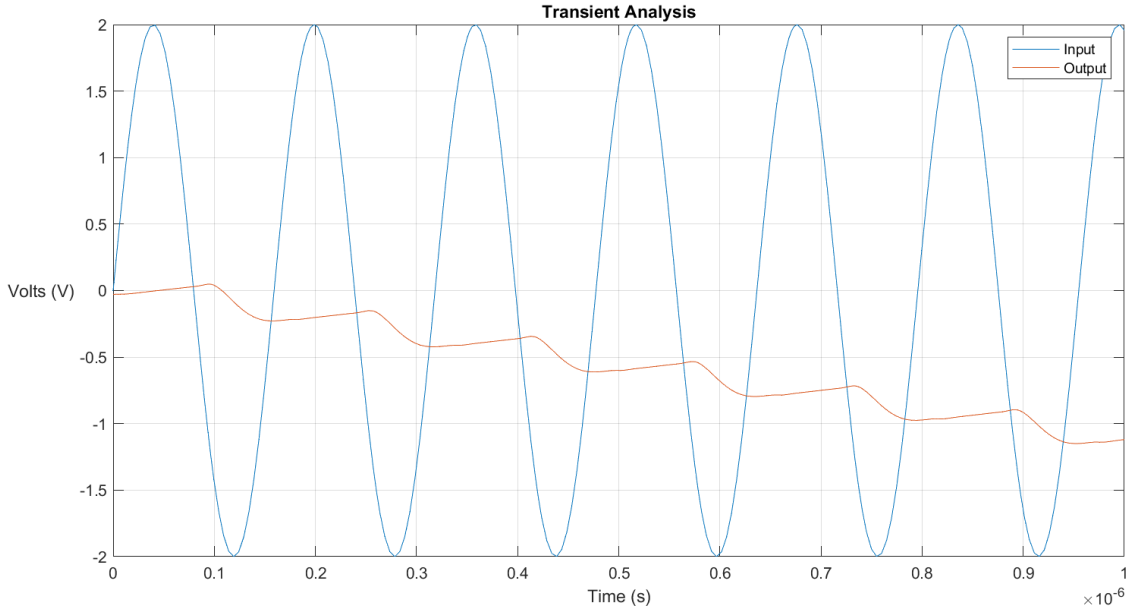


Fig. 23. Transient Analysis

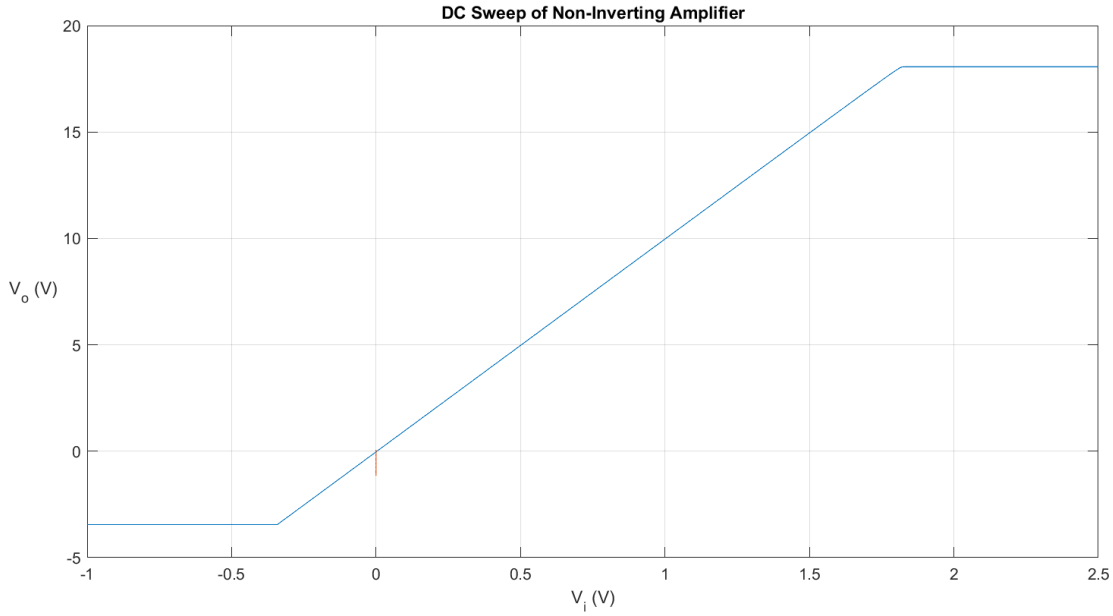


Fig. 24. DC Sweep for Non-Inverting Amplifier

IX. Conclusion

We can summarize the final design with a table of specifications (see Table I) In short, the Op-Amp is itself a complicated and sensitive device. However, when combined with feedback, it can produce powerful results. Furthermore, optimizations to the Op-Amp itself help with these feedback implementations. As a drawback, the gain of the Op-Amp is not used to amplify signals directly, but to ensure that feedback is stable. Alternative designs of this Op-Amp may involve using additional stages to further increase open-loop gain, but that comes at the cost of using more transistors as well as a higher power dissipation. As for the types of transistors used, using MOSFETs instead of BJTs would allow for the Op-Amp to have infinite input impedance and lower power dissipation. Overall, there are many different designs for an Op-Amp; in which the design process of an Op-Amp will involve a theoretical analysis followed by experimental optimizations.

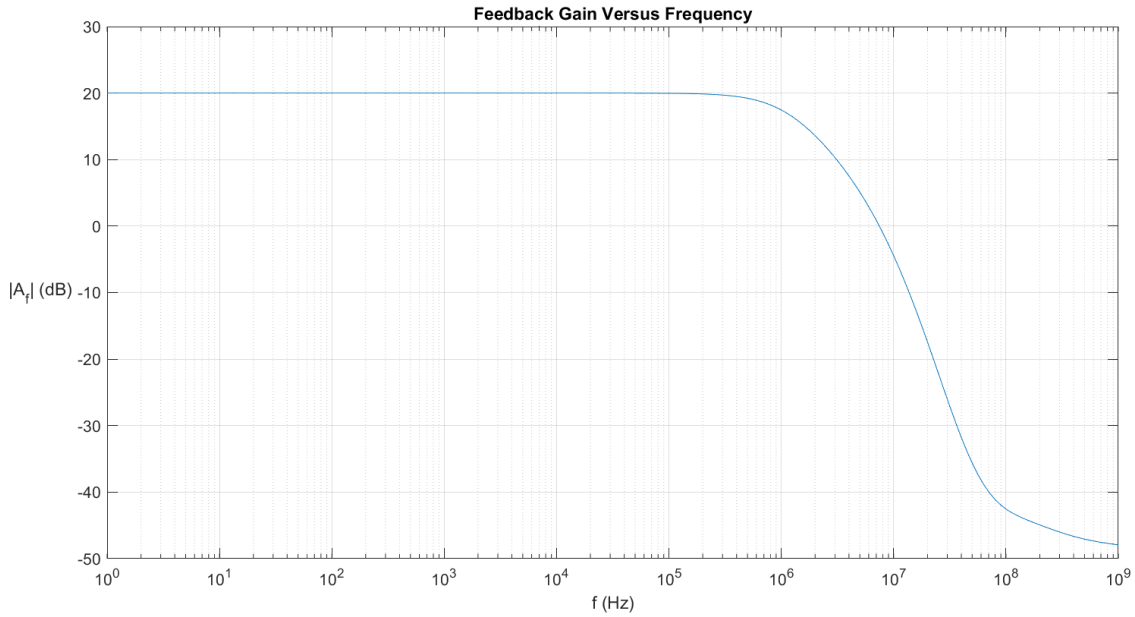


Fig. 25. Bode Plot of Non-Inverting Amplifier Gain

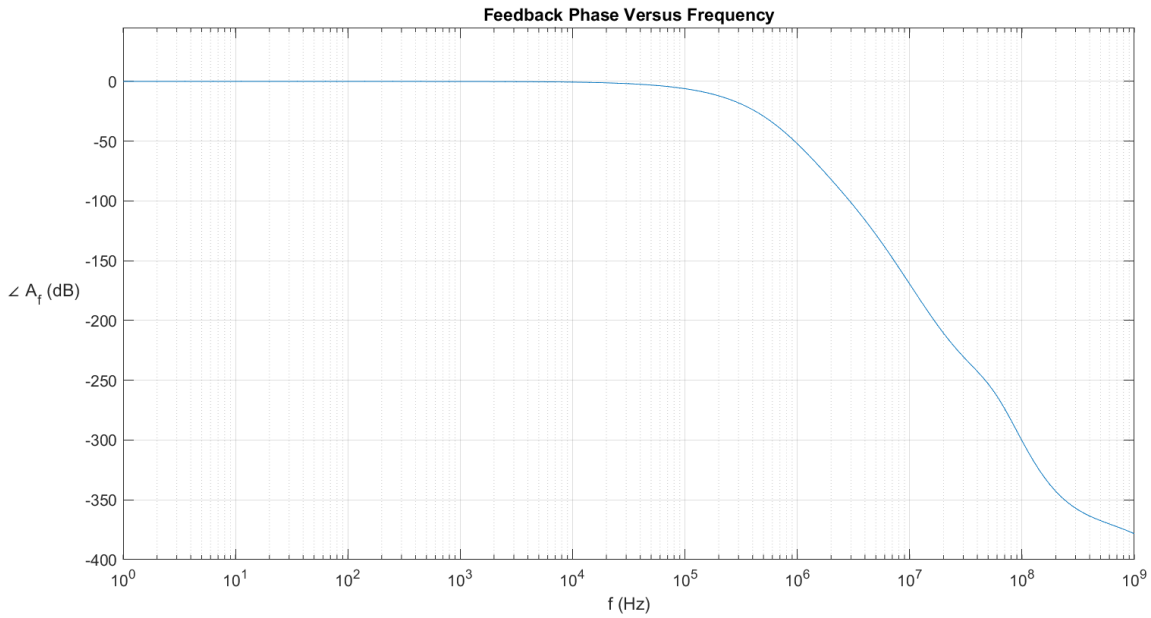


Fig. 26. Bode Plot of Non-Inverting Amplifier Phase

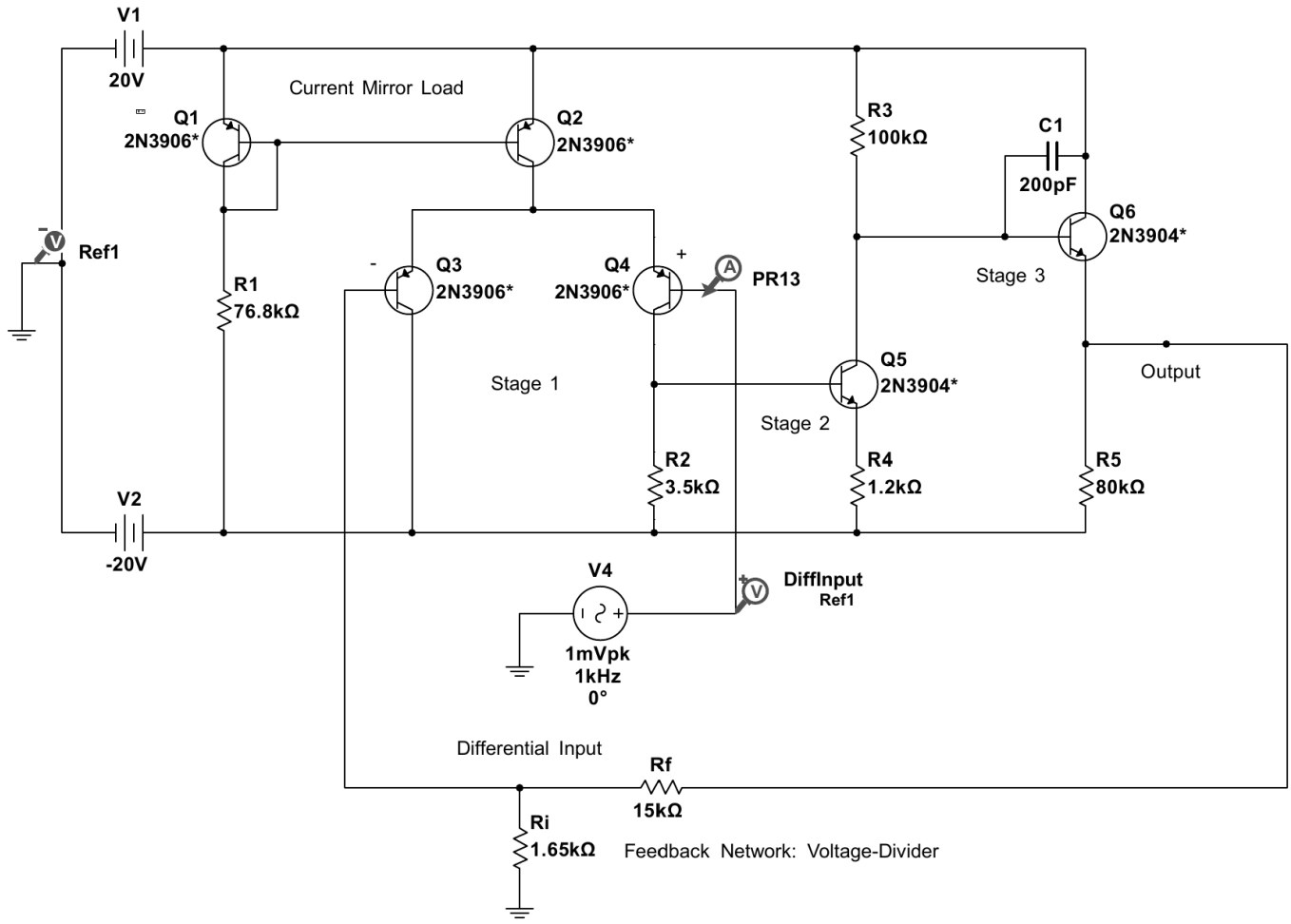


Fig. 27. Non-Inverting Op-Amp Schematic

TABLE I
OP-AMP SPECIFICATIONS

Parameter	Target	Achieved
Open-Loop Gain A	60 dB	61.84 dB
Power Dissipation P_{diss}	$\leq$600 mW	58.4 mW
Min Common-Mode Input Range $V_{\text{CM}_{\text{min}}}$	N/A	-18.7 V
Max Common-Mode Input Range $V_{\text{CM}_{\text{max}}}$	N/A	19 V
Input Current I_{in}	N/A	0.8 μA
Open-Loop Bandwidth	N/A	0 Hz to 8.54 kHz
Closed-Loop Phase Margin	$\geq 45°$	123.45°
Closed-Loop Bandwidth	N/A	0 Hz to 1.115 MHz
Closed-Loop Gain A_f	20 dB	20.0014 dB
Closed-Loop Unity Gain	0 dB	0 dB
Voltage Overshoot	0 V	-1.93 V