राष्ट्रीय प्रौद्योगिकी संस्थान पटना National Institute of Technology Patna

End-Semester Examination (Online mode) Session: 2020-21 Spring'21 Semester

Department: Computer Science and Engineering

Programme: B.Tech.(CS) Semester: 4th (Jan-Jun-2021)

Course: **Computer Architecture (CS4401) (for UG-CS-4) / Computer Organization & Architecture (4CS107) (Backlog)**

Full Marks: 40 Duration: 2 hours

[Attempt all questions; Answer concisely; Use pencil for artwork; Assume missing data]

[Every page must contain **Roll No.**, **Course Code** and **Page No.** on top margin]

1. A computer system has a three-level memory hierarchy, with access time and hit ratios as shown in the figure below:

Level 1 (Cache memory)
Access time $= 50nsec/byte$

Size	Hit ratio
$8M$ bytes	0.80
$16M$ bytes	0.90
$64M$ bytes	0.95

Level 2 (Main memory)
Access time $= 200nsec/byte$

Size	Hit ratio
$4M$ bytes	0.98
$16M$ bytes	0.99
$64M$ bytes	0.995

Level 3
Access time $= 5\mu sec/byte$

Size	Hit ratio
$260M$ bytes	1.0

   a. What should be the minimum sizes of level 1 and 2 memories to achieve an average access time of less than 100 nsec? (5)
   [Course outcome(s) evaluated: CO-(Application/Solve)]

   b. What is the average access time achieved using the chosen sizes of level 1 and level 2 memories? (5)
   [Course outcome(s) evaluated: CO-(Application/Solve)]

2. a. In case of speculative Tomasulo's algorithm in superscalar processor, explain the steps to resolve the following:

$$I_i \xrightarrow{\text{WAW/WAR}} I_j,$$

   where I_i and I_j are any pair of instructions in any instruction sequence. (4)
   [Course outcome(s) evaluated: CO-(Knowledge/Recall)]

   b. Consider the following instruction sequence:

```
        BNEZ    R1    lbl
        ADD     R2    R3    R0
        ADD     R4    R5    R0
        J       lbl1
lbl:    ADD     R6    R7    R0
        ADD     R8    R9    R0
lbl1:   …
```

For this instruction sequence, find the predication instruction sequence to remove control dependencies. (6)
[Hint: Use "CMOVZ [DstReg.] [SrcReg.] [CondReg.]" as the only predication instruction to generate the above instruction sequence.]
[Course outcome(s) evaluated: CO-(Analysis/Determine)]

3. a. Explain with illustration how a unified Graphics architecture can be mapped from a Graphics pipeline in any array processor. (4)
[Course outcome(s) evaluated: CO-(Comprehension/Explain)]

b. Mention the 10-stage graphics pipeline components in Direct3D interface, with illustration. (6)
[Course outcome(s) evaluated: CO-(Knowledge/Recall)]

4. Consider a 96-core future generation multicore system A, but on average only 54 cores of A can be busy. Assume that in A, the cores can be turned off when not in use and such cores draw no power. Also assume that the use of a different number of cores is distributed so as to consider only about average power consumption. Suppose that in A, 90% of time maximum usable cores are used; 9% of time exactly 50 cores are used; and 1% of time is strictly sequential.

a. What is the maximum count of usable cores in the multicore system A? (2)
[Course outcome(s) evaluated: CO-(Application/Solve)]

b. How much speedup can be expected by A in comparison to any uniprocessor system? (3)
[Course outcome(s) evaluated: CO-(Application/Solve)]

c. How would the speedup of A be compared to a 24-processor system that can use all its processors 99% of time? (5)
[Course outcome(s) evaluated: CO-(Application/Solve)]

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