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Assignment-2

Solution-1

Sequence of actions are given as:-

1) P0: Read 120
2) P0: write 120 ← 80
3) P3: write 120 ← 80
4) P1: Read 110
5) P0: write 108 ← 48
6) P0: Write 130 ← 78
7) P3: Write 130 ← 78

1) P0: Read 120

CPU Read - a read miss: I → S

P0.B0: (S, 120, 00, 20)

Read returns 00 20.

2) P0: Write 120 ← 80:

CPU write - I → M

P0.B0: (M, 120, 00, 80)

Invalidate other caches containing 120

P 3.B0: (1, 120, 00, 20)

3) P3: write 120 ← 80

CPU Write - S → M

P3 .B0 : (M, 120, 00, 80)

iv) P1: read 110.

CPU Read – Read miss – I → S

P1.B2: (S, 110, 00, 30) because P0 was the owner, it carries valid content

M → S

P0.B2: (S, 110, 00, 30)

Also update memory now:

M[110] = (00, 30)

Result of read is 00 303

v) P0: write 108 ← 48

CPU write MiSS-S → M

P0.B1: (M, 108, 00, 48)

Invalidate other caches – S → I

P3.B1: (I, 108, 00, 08)

vi) P0: write 130 ← 78

CPU write miss – I → M

P0.B2: (M, 130, 00, 78)

vii) P3: write 130 ← 78

CPU writes – I → M

P3.B2: (M, 130, 00, 78)

Tabular Form:-

P0: Read 120	→ P0.B0: (S, 120, 00, 20)	Read Returns 00 20
P0: Write 120 ← 80	→ P0.B0: (M, 120, 00, 80) P3.B0: (I, 120, 00, 90)	
P3: Write 120 ← 80	→ P3.B0: (M, 120, 00, 80)	
P1: Read 110	→ P1.B2: (S, 110, 00, 30) P0.B2: (S, 110, 00, 30)	Read Returns 00 30
P0: Write 108 ← 48	→ P0.B1: (M, 108, 00, 48) P3.B1: (I, 108, 00, 08)	
P0: Write 130 ← 78	→ P0.B2: (M, 130, 00, 78)	
P3: Write 130 ← 78	→ P3.B2: (M, 130, 00, 78)	

Solution 2:

a) P1 : read 110
P3 : read 110

⇒ P1 : read 110 read miss , satisfied by P0's Cache.
P3 : read 110 read miss, is satisfied by memory

Implementation 1: {N Cache(P1) + N write back(P0)} + {N memory}
= 150 Stall Cycles.

Implementation 2: {N Cache(P1) + N write back(P0)} + {N memory}
= 240 Stall Cycles

b) P0 : read 120 , Read Miss , satisfied by memory.
P0 : read 128 , Read miss, Satisfied by P1's Cache, P1 writes back 128
P0 : read 130 , Read miss satisfied by memory, P0 writes back 140.

Implement 1: 100 + 40 + 10 + 100 + 10 = 260 StallCycles
Implement 2: 100 + 130 + 10 + 100 + 10 = 350 Stall cycles

c) P0 : read 100 Read miss, Satisfied by memory.
P0 : write 108 ← 48 write hit , sends invalidate
P0 : write 130 ← 78 write miss, satisfied by memory write back 110

Implementation 1: 100 + 15 + 10 + 100 = 225 Stall Cycles
Implementation 2: 100 + 15 + 210 + 100 = 225 Stall Cycles.

d) P1: Read 120: Read Miss, Satisfied by Memory.

P1: Read 128, Read + hit

P1: Read 130, Read miss, Satisfied by memory.

Implementation 1: 100+0+100 = 200 Stall Cycles.

Implementation 2: 100+0+100 = 200 Stall Cycles

e). P1: Read 100, Read miss, Satisfied by memory.

P1: Write 108 ← 48, Write miss, write back 128, Satisfied by memory and Send invalidate.

P1: Write 130 ← 78, Write miss, Satisfied by memory.

Implementation 1: 100+10+100+15+100 = 325 Stall Cycles

Implementation 2: 100+10+100+15+100 = 325 Stall Cycles