NPTEL Digital Circuits Workshop
Wadhwani Electronics Laboratory
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Problem set: 3 HW | Date: June 5, 2024

Universal Shifter

Instructions:

1. Use structural modelling for this experiment; means instantiate components and use port map to connect those components.
2. In pen paper design use proper labeling for each wire. And use same labels for the VHDL code.
3. Perform RTL simulation using the given testbench and tracefile.
4. Evaluate your design on Krypton board.

Problem Statement:

1. **Design**

   Design a universal shifter circuit, which can perform logical right shift or left shift on 8-bit input by the specified number of bits.

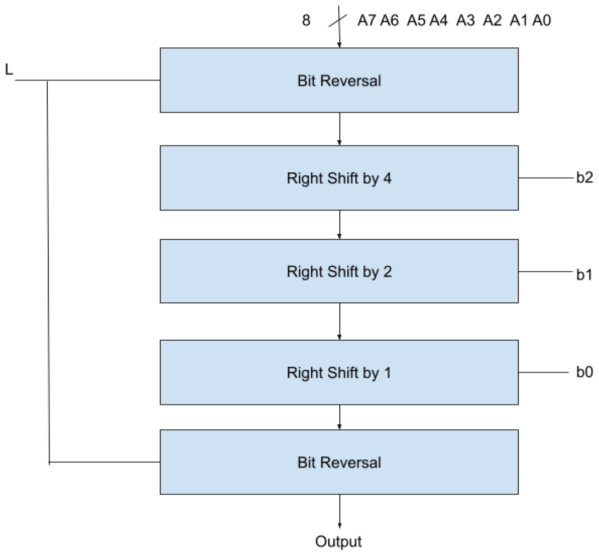

Figure 1: Block diagram

For L = 0, output will be right shifted version of input.
For L = 1, output will be left shifted version of input.

Figure(2) is the design of right shift by 4 block.

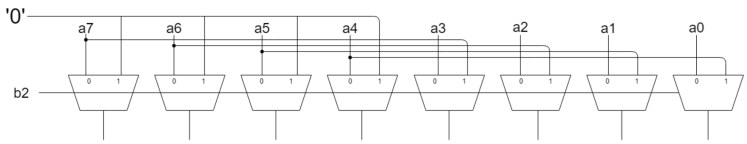

Figure 2: Right shift by 4 bits

The output of shift block in figure(2) will be a7 a6 a5 a4 a3 a2 a1 a0 for b2 = 0.
For b2 = 1 its output will be 0 0 0 0 a7 a6 a5 a4.

2. **VHDL description**

   Describe your designed circuit in VHDL. Block in figure(2) can be described in VHDL as follows

```
n4_bit : for i in 0 to 7 generate
lsb: if i < 4 generate
b2: mux port map(I(0) => a(i), I(1) => a(i+4), S => b(2), Y => s(i));
end generate lsb;
msb: if i > 3 generate
b2: mux port map(I(0) => a(i), I(1) => '0', S => b(2), Y => s(i));
end generate msb;
end generate ;
```

   You need to design the mux used in the above code using logic gates from Gates.vhdl.
   Similarly you can describe Right shift by 2 bit/1 bit and Bit reversal block.

3. **Simulation**

   Simulate your design using the generic testbench to confirm the correctness of your description.
   To do this, use the tracefile given below and modify the testbench given to you appropriately.

   Tracefile format: ($< L\ B2\ B1\ B0\ A7\ A6\ A5\ A4\ A3\ A2\ A1\ A0 >$ $< S7\ S6\ S5\ S4\ S3\ S2\ S1\ S0 >$ 11111111)
   Tracefile

4. **Testing of Board**

   Test the correctness of your design on the Krypton board.
   Perform the pin mapping as follows:

$$L \implies UP; \quad A7\text{-}A0 \implies SW8 - SW1;$$
$$B2 \implies DOWN \quad B1 \implies RIGHT \quad B0 \implies LEFT$$
$$S7 - S0 \implies LED8 - LED1$$