PRINCY JOICE

SUMMARY OF SKILLS

- Overall 5 years of industrial experience with 3.2years in ASIC Verification.
- Knowledge in V**erilog**, **System Verilog, UVM**
- Hands on experience in Bus protocols like SPI, APB, AHB etc.
- Hands on experience in writing verification plans.
- Hands on experience in formal verification (Connectivity check).
- Experience in **LINT** using Verilator
- Basic exposure to Synopsys **Spyglass** Lint tool
- Hands on experience with **EDA** tools.

PROFESSIONAL EXPERIENCE

- Working as Design Verification Engineer in **VERIFWORKS** since May 2019 till present
- Previous Experience
  - Company Name: - SKAP Technologies.
  - Duration: - December 2015 - December 2017.
  - Designation: - Design Engineer

SKILLS

- Methodology : UVM
- HDL/HDVL : Verilog, System Verilog
- Protocol : I2C, AHB, APB
- Scripting Language : Perl and TCL

PROJECTS

Title : **5G base station chip verification**
Client : **Nokia**
Roles and Responsibilities :

- Own UVM based TB and Test development for this chip
- Work with architects to identify appropriate DV strategy.
- UVM based SPI & GPIO pin config verification with Xcelium
- Handled Liberty models in simulation.
- Used black-boxes in simulation to work-around hard macros
- Reusing UVCs available to shift-left timelines for this project

Title : **MSIE flow implementation for T0 spin**
Client : **Nokia**
Roles and Responsibilities :

- T0 tapeout – 28nm (exploring 5nm too)
- Customer netlist – PG netlist + RTL top, glue logic
- Added support to handle GZIPPED netlist files
- Updated flow to handle MBIST generated files (.mbv extension)
- Traditional XLM flow takes 20-25 minutes to compile-elab-sim
- Worked with DV architect to explore advanced XLM features to provide shift-left
    - Created primary partition (XCOM flow)
    - Split the flow to 2 steps – dut_comp and run_xlm, added relevant TCL scripts.
    - Brought down the time per UVM test to 20-seconds against 20-mins

Title : **SimCompat DEV**
Client : **Confidential**
Roles and Responsibilities :

- Work on SV testcases development for known SV compatibility issues
- Provided with 100+ scenarios with LRM pointers
- Analyze LRM sections, understand the issue
- Develop SV tests – PASS and FAIL
- Run using Cloud based platform
- Document findings, present to team

Title : **NXS_GNR_D**

Client : **Intel**

Description :

Multi core are connected to a central compute die. Mutli-core connected to form a single processor in order to increase the processing power.

Responsibilities :

Worked on the Cheetah IP conversion. Cheetah is the environment which is very fast. So, converting HDK environment to cheetah environment.

Title : **VirtIO_MKS_DMA**

Client : **Intel**

Description :

Virtio specification is that virtual environments and guests should have a straightforward, efficient, standard and extensible mechanism for virtual devices, rather than boutique per-environment or per-OS mechanisms.

Responsibilities :

Ran Regression and verifying the changes

Title : **Verification of APB<->SPI Using RAL**

Software platform / tools : **NCSim**

Language / Methodology : **UVM**

The Registers in SPI were verified using Register Abstraction Layer with various number of test cases to ensure the working of registers as per the protocol. SPI has Full duplex communication, higher throughput, not limited to 8-bit words and slave don't need a unique address. The SPI bus specifies four

logic signals SCLK, MOSI, MISO, SS. It supports master slave communication. Each device can operate as either a transmitter or receiver, depending on the function of the device. It is a fully static synchronous design with one clock domain.

Responsibilities:

- Used virtual sequences and virtual sequencer to verify the VIP
- Used Register model to verify the registers

Title : Connectivity verification using Formal & Go2UVM

Client : STek

Tool Used : VC Formal, VCS

Tasks :

- Understand connectivity verification challenges
- Implement Python app to generate Connectivity framework for various Formal tools
- Develop manual tests using Go2UVM to verify connectivity

Automate Go2UVM tests for connectivity

Title : IMA Audio Codec – Lint clean-up

Client : SaberTK

Language/Methodology : Verilog

Tools : JasperGold Superlint

Description :

ADPCM codec involves encoder and decoder. RTL design was provided, goal is to make it lint clean

Responsibilities :

Understand the RTL Design. Analyze Jaspergold Superlint analyzed log files. Fix violations, review with client

Title : Serial data acquisition module – Lint clean-up

Client : SaberTK

Language/Methodology : Verilog

Tools : Spyglass

Description :

- SPI based serial data acquisition design at client side. System side has an AHB interface. New feature was to add increase the address space/memory size. Client ran Spyglass and provided log files for analysis.

Responsibilities :

Understand the RTL Design. Analyze Spyglass analyzed log files. Fix violations, review with client. Issues found:

- Multiple drivers
- Latch on AHB unused legacy code
- Sensitivity list incomplete

Title : I2C Protocol

Client : Confidential

Language/Methodology : System Verilog

Tools : Modelsim

Description :

I2C stands for Inter-Integrated Circuit. It is a bus interface connection protocol incorporated into devices for serial communication. It is a widely used protocol for short distance communication. It is also known as Two Wired Interface (TWI). I was involved in development in function coverage

development.

Responsibilities :

Understand the Design specification and Created Test Plan Verify the IP using System Verilog verification methods.

Title : Verification of AHB Lite (Advanced High-Speed Bus)

Client : Confidential

Language/Methodology : System Verilog

Tools : Modelsim

Description :

AMBA AHB-Lite Protocol addresses the requirements of high-performance and high frequencies system designs. It is a bus interface that supports a single bus master includes a number of features that make it suitable for high bandwidth operation. I was involved in development of Generator, BFM and Monitor component for single point-to point AHB bus. I was also involved in functional coverage development.

Responsibilities :

Understand the Design specification and Created Test Plan Verify the IP using System Verilog verification methods.

Title : Design of APB 3.0 (Advanced Peripheral Bus)

Client : Confidential

Language/Methodology : Verilog

Tools : Modelsim

Description :

APB (Advanced Peripheral Bus) is one of the components of the AMBA bus architecture. APB is low bandwidth and low performance bus used to connect the peripherals like UART, keypad, timer and other peripherals devices to the bus architecture.

Responsibilities :

Understand the Design specification. Implement design using Verilog RTL

Title : Packet Splitter

Client : Confidential

Language/Methodology : Verilog

Tools : Modelsim

Description :

Packet Splitter module allows duplication of data flow to more targets (up to 7 different connections). It is suitable for applications where duplication of data flow is needed.

Responsibilities :

Understand the Design Specification and implement in RTL design

EDUCATIONAL QUALIFICATION

Master of Technology (VLSI Design) Graduated, April 2015, Sathyabama University.

Bachelor of Engineering (Electronics & Communication Engineering) Graduated, April 2013, M.A.M College of Engineering *(*Anna University, Chennai*)* Trichy, Tamil Nadu