PRATIBHA

WORK EXPERIENCE:

- Total 6.4 years of Industry experience in Electronics and 4+ years of experience in Design Verification
- Currently working as Verification Engineer at VerifWorks Pvt Ltd, Sep 2020- Present
- Experience with 3ST Technologies Pvt. Ltd. as a Verification Engineer, March 2017 – Feb 2019
- Experience with Dixon Technologies Pvt. Ltd. as a Production Engg, Aug-2011 – Aug-2014

SKILLS:

- Language : VHDL, Verilog, SystemVerilog
- Methodology : UVM
- Tools : Questa-Sim, Model-Sim, Xilinx-ISE, Quartus, Cadence NC Sim
- Scripting Language: PERL
- Version Control : Git

Projects:

Title : COMET
Client : Confidential
Methodology : UVM
Tool Used : Xcelium

Description :

- Comet IC Supports 9 independent RX and 9 independent TX channels.

Responsibilities :

- Contributed towards preparation of compliance matrix for DV peripheral IP's
- Compiled and simulate UART and APB C based test.
- Implementation the UVM env of UART and APB.
- Write the read/write test for APB
- Develop AHB CIP and integrate

Title : Checker IP Development – AHB & APB
Client : Latch-UP
Methodology : UVM
Tool Used : Verilator
Responsibilities :

- Develop Assertions, Covers for AHB & APB protocols.
- Develop Tests and TB for verifying CIP
- Run on Verilator, fix any compatibility issues
- Develop AHB CIP and integrate

Title : **5G base station chip verification**
Client : **Nokia**
Roles and Responsibilities :

- Team Lead for SoC level verification.
- Track team for timely updates to management and customer stakeholders
- Collating all bug reports – present to management
- Contribute to verification strategy, document, present it to team.

Title: Functional verification of Link Park HIF
Description
LKP HIF is the Host Interface IP of LKV project. HIF block has PFs and VFs. HIF block is responsible for AER, PME, any other blocks which needs to talk to PCIe it has to go through HIF. Some PCIE errors are handled by HIF.
Responsibility

- Modifying environment to the specification required in this project
- Updating both non configuration space csr's and configuration space csr's
- Updating existing testcases to suite latest specification
- Verifying legacy features of this project
- Regression and coverage reporting
- Modified error reporting according to the specification

Title : **SoC_SS VALIDATION**
TB Methodology : **OVM**
EDA : **Synopsys VCS**
Responsibilities :

- Validation of RAS subsystems
- Understood the spec and behavior from the previous gen
- Ported seq to the current gen
- Verified the behavior by running regression test list
- Verified across different variants of the project
- Validation of PCIe subsystems
- RAL Sweep test
- Specified with the proprietary format
- Random writes and reads to the reg
- 3000+ reg
- Scoreboard for PCIe bifurcation
- 8 bifurcations
- 90+tests
- Came up with the post processing scoreboard in PERL
- PCIe Mixer test
- Ported few sequences from previous gen to the current
- Ran and verified the behavior with different config
- Fixed the failures

Title : **Avalon Memory Mapped Interfaces(Verification)**
TB Methodology : **UVM**
EDA : **Mentor Questa 2020.1**

Responsibilities :

- Avalon ST an interface that supports the unidirectional flow of data, including multiplexed streams, packets, and data.
    - Created Test Cases for Avalon ST Protocol.
    - Created Test bench for Sink.

Title : Avalon Memory Mapped Interfaces(Verification)
TB Methodology : UVM
EDA : Mentor Questa 2020.1
Responsibilities :

- Avalon MM an interface that supports the unidirectional flow of data, including multiplexedstreams packets, and data.
    - Created Test Cases for Avalon MM Protocol.
    - Created Test bench for Slave and Contribution of created UVM Env for Avalon MM protocol

Title : AMBA-AHB BUS PROTOCOL VERIICATION (2.0)
TB Methodology : UVM
EDA : Cadence NC Sim
Responsibilities :

- The AMBA APB protocol is targeted at high-performance, low-frequency system designs and includes a number of features that make it suitable for a high-speed submicron interconnect.
    - Understand specifications and devised a test plan. o Created Driver logic for the RTL Verification. o To contribution Master bus function model, and test bench generation.

Title : AMBA-AHB BUS PROTOCOL VERIICATION (2.0)
TB Methodology : UVM
EDA : Cadence NC Sim
Responsibilities :

- The AMBA APB protocol is targeted at high-performance, low-frequency system designs and includes a number of features that make it suitable for a high-speed submicron interconnect.
    - Understand specifications and devised a test plan.
    - Made class-based Verification environment in UVM.
    - Created Driver logic for the RTL Verification

Title : Inter Integrated Circuits(I2C)
HDL : Verilog
EDA : Xilinx-ISE
Responsibilities :

- I2C is a serial communication protocol that only requires two signal lines.
- I2C has half duplex communication and used for low power requirements.
- One or more than one master configuration and slave configuration is possible. o Understanding the spec
    - Came up with testplan
    - Implemented the test bench in Verilog for single master single slave o Wrote test cases

- Verified with waveform

Title : Universal Asynchronous Receiver Transmitter
HDL : Verilog
EDA Tool : Xilinx-ISE
Responsibilities :

- UART is a widely used device for data communication. It has 4 control bits like start bit, data bit, parity bit and stop bit. Contains parallel-to-serial converter for data transmitted and serial-to-parallel converter for data receiver.
  - Understanding the spec o Came up with testplan
  - Implemented the test bench in Verilog o Wrote test cases o Verified with waveform

RESEARCH WORK:

Title : Design of Hybrid 1-Bit Full Adder with Low Power
Team size : 1
Platform : Tanner 14.0
Technology : 90 nm & 180 nm CMOS technology
Responsibilities:

- This project procedure the hybrid full adder with low power and stimulated in TSMC 90nm and 180- nm technologies by using TANNER tool.
- The motive of hybrid full adder design is to provide high speed and low power consumption.
- Less no. of transistors are used in this project.

PROFESSIONAL QUALIFICATION:

- Master of Technology (VLSI Design) from JSS, Noida 2016.
- Bachelor of Technology (Electronics & Communication) from KITE, Jaipur 2011.