UNIVERSITY OF COLOMBO, SRI LANKA

UNIVERSITY OF COLOMBO SCHOOL OF COMPUTING

BACHELOR OF SCIENCE IN COMPUTER SCIENCE
BACHELOR OF SCIENCE HONOURS IN COMPUTER SCIENCE
BACHELOR OF SCIENCE HONOURS IN SOFTWARE ENGINEERING
BACHELOR OF SCIENCE IN INFORMATION SYSTEMS
BACHELOR OF SCIENCE HONOURS IN INFORMATION SYSTEMS

First Year Examination – Semester I – 2018

SCS 1105 – Computer Systems (R1)

TWO (2) HOURS

No of Pages: 16

To be completed by the candidate

Examination Index No: ----------

1.

Important Instructions to candidates:

1. The medium of instruction and questions is **English**.
2. Note that questions appear on both sides of the paper. If a page or a part of a question is not printed, please inform the supervisor immediately.
3. Write your index number in the space provided above.
4. The question paper consists of 04 questions and requested to answer all questions in 02 hours.
5. Any electronic device capable of storing and retrieving text including electronic dictionaries and mobile phones are **not allowed**.

For Examiner's use only	
Question No	**Marks**
1	
2	
3	
4	
Total	

1. **(a)** What is the decimal number equivalent of the 16-bit floating point number **0 11000 0101010101**? Assume that 16-bit floating point representation is with a sign bit, 5-bit exponent and 10-bit mantissa.

[5 Marks]

(b) What is the 16 bit floating point representation of the decimal value **+1365.3125?** Assume that 16 bit floating point representation contains a sign bit, a 5-bit exponent and a 10-bit mantissa.

[5 Marks]

(c) What is the loss of accuracy (round-off-error) when converting the decimal value **+1365.3125** to its 16 bit floating point representation containing a sign bit, a 5-bit exponent and a 10-bit mantissa?

[5 Marks]

(d) What is the IEEE standard 32-bit floating point representation of the decimal number **+1365.328125**?

[5 Marks]

(e) What is the equivalent decimal number to the IEEE standard 32-bit floating point representation of **0 10001000 11111111110000000000000** ?

[5 Marks]

2. (a) Simplify the following Boolean functions using Boolean algebraic laws:

(i). $R.(P.Q + P.\overline{Q}) + \overline{R}.(\overline{P}.\overline{Q} + \overline{P}.Q)$

[3 Marks]

(ii). $\bar{R}.(\bar{P}.\bar{Q} + P.Q + P.\bar{Q}) + P.(Q.R + \bar{Q}.R)$

[3 Marks]

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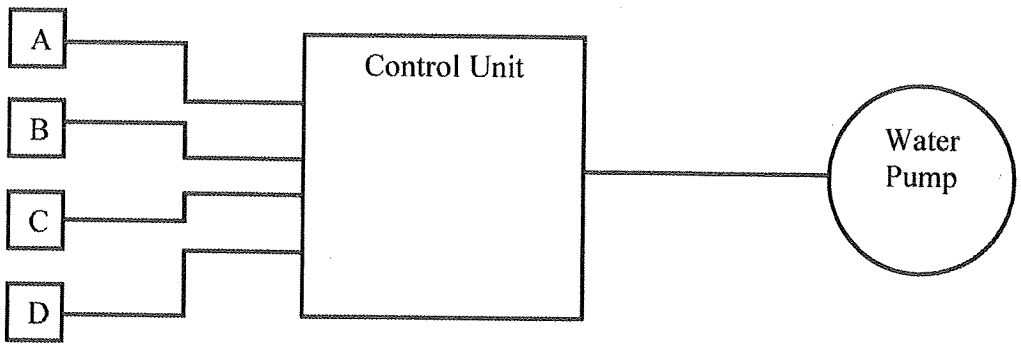
(b). Authorities of a football club has implemented an automatic ground watering system to eliminate the manual watering procedure which was not efficient. Newly implemented system takes input readings from four sensor units, namely A, B, C and D, and based on their values the water pump is activated through a control unit. All four sensor units are capable of producing only two states that are ***active*** and ***inactive***. It is said that water pump's activation X, is given in the following Boolean algebraic statement:

$$X = \bar{A}.\bar{B}.\bar{C}.D + \bar{A}.\bar{B}.C.D + \bar{A}.B.\bar{C}.\bar{D} + \bar{A}.B.\bar{C}.D + \bar{A}.B.C.\bar{D} + A.\bar{B}.C.D + A.B.\bar{C}.\bar{D} + A.B.C.\bar{D}$$



(i). Complete the truth table given below for the above Boolean logic expression:

[4 Marks]

A	B	C	D	X
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

(ii). In order to design the **most simplified** circuit with minimum number of logic gates, draw the **Karnaugh-Map** for the above truth table and by **clearly showing** your grouping, derive the simplified Boolean expression in both **Sum of Product** and **Product of Sum** forms.

[8 Marks]

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(iii). Design the logic circuits for the **Sum of Product** and **Product of Sum** expressions in above (ii) using only **NAND** and **NOR** gates. Clearly indicate the method and steps.

[4 Marks]

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(iv). Club authorities have informed that they want to have a switch that enables them to activate the water pump even when the control unit decides to deactivate it. However, when the control unit decides to activate the pump, the switch should not prevent it. Based on this requirement, the circuit vendors have devised a switch that produces ***state active*** (Boolean one) when it is on and ***state inactive*** (Boolean zero) when it is off. Draw a block diagram clearly and show how you would integrate this switch to the existing circuit?

[3 Marks]

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3. (a) Briefly explain each of the following components of the computer. Clearly state the task(s) they perform.

[5 Marks]

(i). Program Counter (PC)

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(ii). Memory Address Register (MAR)

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(iii). Control Bus

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(iv). Data Segment in Memory

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(v). Heap Segment in Memory

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(b). Briefly explain why the **Clock Speed** is **not** equal to the **CPU Performance**. Use the **General Performance Equation** to explain your answer and mention how the CPU throughput (performance) can be improved.

[5 Marks]

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(c) Consider a machine with an instruction format of the form **opcode R M** where **R** is a register address and **M** is a memory address. Instructions are 16 bits long and one of the instruction formats provides 4 bits for the op-code, 4 bits for the register and other 8 bits for the memory address of the operand. Assume that the word size of this machine is 8 bits (byte addressable).

Some of the op-codes of the above (a) processor is given below:

0001 – L R, A	**LOAD** the register **R** with the content of memory cell **A**
0010 – LI R, I	**LOAD** the register **R** with the value **I**
0011 – ST R, A	**STORE** the content of the register **R** to the memory cell whose address is **A**
0101 – ADD R0, R1, R2	**ADD** the numbers in registers **R1** and **R2** and place the result in register **R0**
1001 - XOR R0, R1, R2	**XOR** the bit patterns in **R1** and **R2** and place the result in **R0**
1000 - AND R0, R1, R2	**AND** the bit patterns in **R1** and **R2** and place the result in **R0**

1110 – JMP R, A	**JUMP** to the instruction located in the memory cell **A** if the bit pattern in **R** is equal to the one in **R0**
1111 - HALT	**HALT** the execution

Write down the machine code instruction sequence to execute the pseudo code given below.

[15 Marks]

*Initialize **A** to 25*
*Initialize **B** to 3*
*Initialize **Counter** to ten*
*While **Counter** is Greater Than or Equal To 0*
    X is equal to the subtraction of B from A
    *Set **A** to the value of **X***
    *Decrement **Counter** by one*
Store A in memory
Halt programme

(Assume that the variables **A**, **B**, **Counter**, **X** are stored in the memory addresses 80_{hex}, 81_{hex}, 82_{hex}, 83_{hex} respectively and the initial program counter (PC) is 30_{hex})

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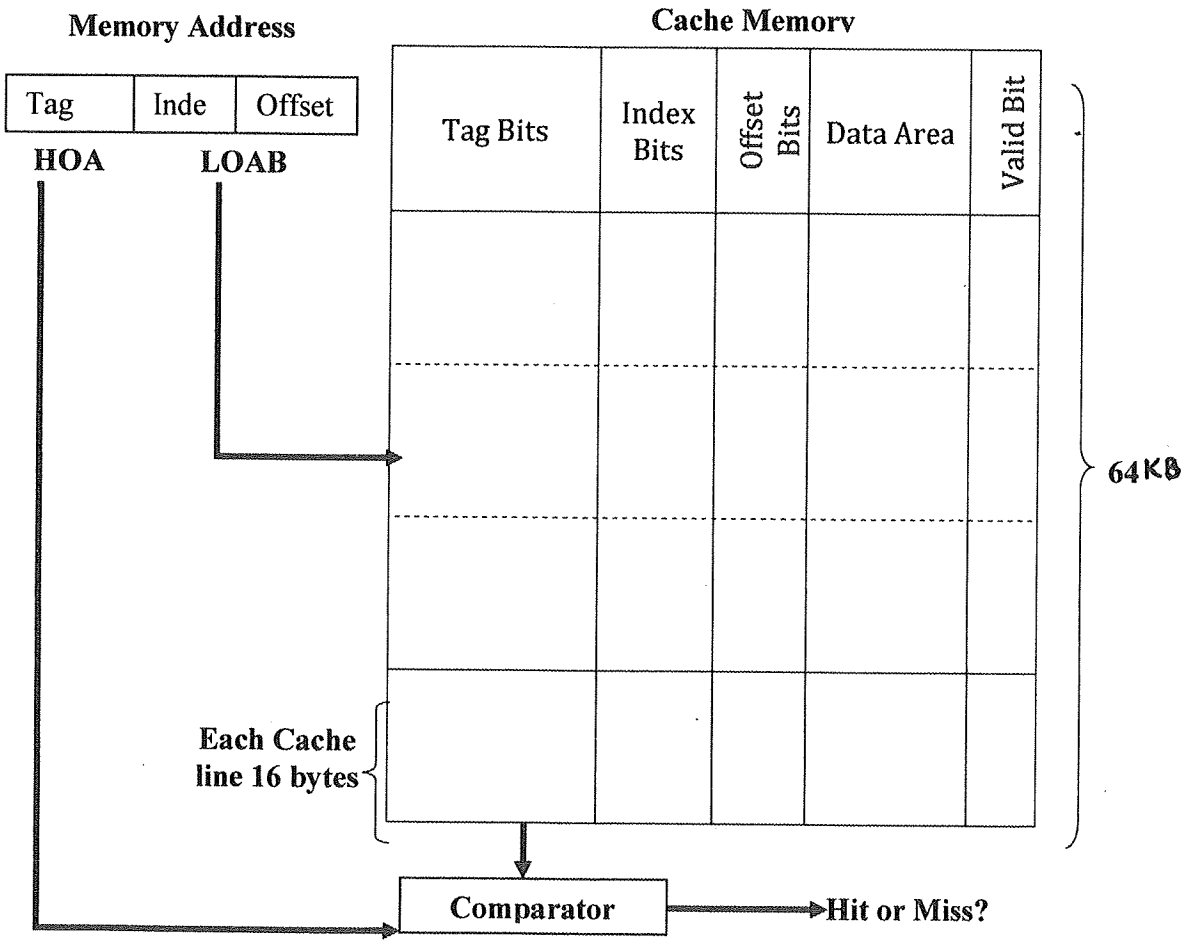
4. (a) Consider a computer system with the following characteristics:

- Total of 1 MB of main memory
- Byte addressable
- Cache block size of 16 bytes
- Cache size of 64 KB



(i). If the cache is designed as a direct-mapped cache, give the corresponding tag, cache line index and offsets for the following main memory addresses of

[6 Marks]

Physical Address	Tag	Cache Line Index	Offset
• 0x66AF0010			
• 0x39D01234			
• 0xC3D5ABBE			

(ii). Give two main memory addresses that map to the same cache slot of each of following addresses by considering the cache architecture described in above (i).

[2 Marks]

0x66AF0010:
0x39D01234:

(iii). If the cache is designed as ***fully associative***, give the corresponding tag and offset values for the following main memory addresses:

[4 Marks]

Address	Tag	Offset
• 0x66AF0010		
• 0xC3D5ABBE		

(iv). If the cache is designed ***two-way set associative***, give the corresponding tag, cache set index and offset values for the following main memory addresses:

[6 Marks]

Address	Tag	Cache Set Index	Offset
• 0x66AF0010			
• 0xC3D5ABBE			

(b). In a paged memory management system, total size of the physical memory is 128MB and the virtual memory is 2GB. The page size is 4KB.

(i). How many bits will be allocated as the Higher Order Address Bits (HOAB) and Lower Order Address Bits (LOAB) to identify page numbers and corresponding words respectively? (Clearly show your calculation steps)

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(ii). How many page frames are there in the system?

[2 Marks]

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(iii). Determine the maximum number of entries that the page table could have.

[2 Marks]

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