8 Point FFT

July 17, 2025

[ ]:
```
# The following is the module, Overlap and IP initialisation
```

[28]:
```
from pynq import Overlay, MMIO
import ctypes
```

[3]:
```
overlay = Overlay('fft_lakshay_zybo.xsa')
```

[4]:
```
overlay?
```

[5]:
```
ip = overlay.Eight_Point_FFT_IP_0
```

[6]:
```
overlay.ip_dict
```

[6]:
```
{'Eight_Point_FFT_IP_0': {'type': 'user.org:user:Eight_Point_FFT_IP:1.0',
  'mem_id': 'S00_AXI',
  'memtype': 'REGISTER',
  'gpio': {},
  'interrupts': {},
  'parameters': {'C_S00_AXI_DATA_WIDTH': '32',
   'C_S00_AXI_ADDR_WIDTH': '7',
   'Component_Name': 'design_1_Eight_Point_FFT_IP_0_0',
   'EDK_IPTYPE': 'PERIPHERAL',
   'C_S00_AXI_BASEADDR': '0x43C00000',
   'C_S00_AXI_HIGHADDR': '0x43C0FFFF',
   'WIZ_DATA_WIDTH': '32',
   'WIZ_NUM_REG': '26',
   'SUPPORTS_NARROW_BURST': '0',
   'DATA_WIDTH': '32',
   'PROTOCOL': 'AXI4LITE',
   'FREQ_HZ': '50000000',
   'ID_WIDTH': '0',
   'ADDR_WIDTH': '7',
   'AWUSER_WIDTH': '0',
   'ARUSER_WIDTH': '0',
   'WUSER_WIDTH': '0',
   'RUSER_WIDTH': '0',
   'BUSER_WIDTH': '0',
   'READ_WRITE_MODE': 'READ_WRITE',
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  'HAS_BURST': '0',
  'HAS_LOCK': '0',
  'HAS_PROT': '1',
  'HAS_CACHE': '0',
  'HAS_QOS': '0',
  'HAS_REGION': '0',
  'HAS_WSTRB': '1',
  'HAS_BRESP': '1',
  'HAS_RRESP': '1',
  'NUM_READ_OUTSTANDING': '8',
  'NUM_WRITE_OUTSTANDING': '8',
  'MAX_BURST_LENGTH': '1',
  'PHASE': '0.0',
  'CLK_DOMAIN': 'design_1_processing_system7_0_0_FCLK_CLK0',
  'NUM_READ_THREADS': '4',
  'NUM_WRITE_THREADS': '4',
  'RUSER_BITS_PER_BYTE': '0',
  'WUSER_BITS_PER_BYTE': '0',
  'INSERT_VIP': '0'},
 'registers': {},
 'driver': pynq.overlay.DefaultIP,
 'device': <pynq.pl_server.embedded_device.EmbeddedDevice at 0xb385f2e0>,
 'state': None,
 'bdtype': None,
 'phys_addr': 1136656384,
 'addr_range': 65536,
 'fullpath': 'Eight_Point_FFT_IP_0'},
'processing_system7_0': {'type': 'xilinx.com:ip:processing_system7:5.5',
 'gpio': {},
 'interrupts': {},
 'parameters': {'C_EN_EMIO_PJTAG': '0',
  'C_EN_EMIO_ENET0': '0',
  'C_EN_EMIO_ENET1': '0',
  'C_EN_EMIO_TRACE': '0',
  'C_INCLUDE_TRACE_BUFFER': '0',
  'C_TRACE_BUFFER_FIFO_SIZE': '128',
  'USE_TRACE_DATA_EDGE_DETECTOR': '0',
  'C_TRACE_PIPELINE_WIDTH': '8',
  'C_TRACE_BUFFER_CLOCK_DELAY': '12',
  'C_EMIO_GPIO_WIDTH': '64',
  'C_INCLUDE_ACP_TRANS_CHECK': '0',
  'C_USE_DEFAULT_ACP_USER_VAL': '0',
  'C_S_AXI_ACP_ARUSER_VAL': '31',
  'C_S_AXI_ACP_AWUSER_VAL': '31',
  'C_M_AXI_GP0_ID_WIDTH': '12',
  'C_M_AXI_GP0_ENABLE_STATIC_REMAP': '0',
  'C_M_AXI_GP1_ID_WIDTH': '12',
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'C_M_AXI_GP1_ENABLE_STATIC_REMAP': '0',
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'C_S_AXI_ACP_ID_WIDTH': '3',
'C_S_AXI_HP0_ID_WIDTH': '6',
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'C_S_AXI_HP1_ID_WIDTH': '6',
'C_S_AXI_HP1_DATA_WIDTH': '64',
'C_S_AXI_HP2_ID_WIDTH': '6',
'C_S_AXI_HP2_DATA_WIDTH': '64',
'C_S_AXI_HP3_ID_WIDTH': '6',
'C_S_AXI_HP3_DATA_WIDTH': '64',
'C_M_AXI_GP0_THREAD_ID_WIDTH': '12',
'C_M_AXI_GP1_THREAD_ID_WIDTH': '12',
'C_NUM_F2P_INTR_INPUTS': '1',
'C_IRQ_F2P_MODE': 'DIRECT',
'C_DQ_WIDTH': '32',
'C_DQS_WIDTH': '4',
'C_DM_WIDTH': '4',
'C_MIO_PRIMITIVE': '54',
'C_TRACE_INTERNAL_WIDTH': '2',
'C_USE_AXI_NONSECURE': '0',
'C_USE_M_AXI_GP0': '1',
'C_USE_M_AXI_GP1': '0',
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'C_USE_S_AXI_ACP': '0',
'C_PS7_SI_REV': 'PRODUCTION',
'C_FCLK_CLK0_BUF': 'TRUE',
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'C_FCLK_CLK2_BUF': 'FALSE',
'C_FCLK_CLK3_BUF': 'FALSE',
'C_PACKAGE_NAME': 'clg400',
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'C_GP1_EN_MODIFIABLE_TXN': '1',
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'PCW_DDR_RAM_HIGHADDR': '0x1FFFFFFF',
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'PCW_UART0_HIGHADDR': '0xE0000FFF',
'PCW_UART1_BASEADDR': '0xE0001000',
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'PCW_USB0_HIGHADDR': '0xE0102fff',
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'PCW_TTC1_BASEADDR': '0xE0105000',
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'PCW_FCLK_CLK2_BUF': 'FALSE',
'PCW_FCLK_CLK3_BUF': 'FALSE',
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'PCW_UIPARAM_DDR_COL_ADDR_COUNT': '10',
'PCW_UIPARAM_DDR_CL': '7',
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'PCW_UIPARAM_DDR_T_RCD': '7',
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'PCW_UIPARAM_DDR_DQS_TO_CLK_DELAY_0': '0.0',
'PCW_UIPARAM_DDR_DQS_TO_CLK_DELAY_1': '0.0',
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'PCW_UIPARAM_DDR_CLOCK_3_PROPOGATION_DELAY': '160',
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'PCW_PACKAGE_DDR_DQS_TO_CLK_DELAY_2': '-0.009',
'PCW_PACKAGE_DDR_DQS_TO_CLK_DELAY_3': '-0.033',
'PCW_PACKAGE_DDR_BOARD_DELAY0': '0.089',
'PCW_PACKAGE_DDR_BOARD_DELAY1': '0.075',
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'PCW_PACKAGE_DDR_BOARD_DELAY2': '0.085',
'PCW_PACKAGE_DDR_BOARD_DELAY3': '0.092',
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'PCW_CRYSTAL_PERIPHERAL_FREQMHZ': '33.333333',
'PCW_APU_PERIPHERAL_FREQMHZ': '666.666666',
'PCW_DCI_PERIPHERAL_FREQMHZ': '10.159',
'PCW_QSPI_PERIPHERAL_FREQMHZ': '200',
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'PCW_USB0_PERIPHERAL_FREQMHZ': '60',
'PCW_USB1_PERIPHERAL_FREQMHZ': '60',
'PCW_SDIO_PERIPHERAL_FREQMHZ': '100',
'PCW_UART_PERIPHERAL_FREQMHZ': '100',
'PCW_SPI_PERIPHERAL_FREQMHZ': '166.666666',
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'PCW_USE_S_AXI_GP1': '0',
'PCW_USE_S_AXI_ACP': '0',
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'PCW_S_AXI_GP1_FREQMHZ': '10',
'PCW_S_AXI_ACP_FREQMHZ': '10',
'PCW_S_AXI_HP0_FREQMHZ': '10',
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'PCW_USE_DMA2': '0',
'PCW_USE_DMA3': '0',
'PCW_USE_TRACE': '0',
'PCW_TRACE_PIPELINE_WIDTH': '8',
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'PCW_USE_TRACE_DATA_EDGE_DETECTOR': '0',
'PCW_TRACE_BUFFER_CLOCK_DELAY': '12',
'PCW_USE_CROSS_TRIGGER': '0',
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'PCW_M_AXI_GP0_SUPPORT_NARROW_BURST': '0',
'PCW_M_AXI_GP0_THREAD_ID_WIDTH': '12',
'PCW_M_AXI_GP1_ID_WIDTH': '12',
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'PCW_PRESET_BANK1_VOLTAGE': 'LVCMOS 3.3V',
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'PCW_DDR_PORT3_HPR_ENABLE': '0',
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'PCW_SD1_SD1_IO': '<Select>',
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'PCW_MIO_20_IOTYPE': '<Select>',
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'PCW_MIO_20_SLEW': '<Select>',
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'PCW_MIO_21_IOTYPE': '<Select>',
'PCW_MIO_21_DIRECTION': '<Select>',
'PCW_MIO_21_SLEW': '<Select>',
'PCW_MIO_22_PULLUP': '<Select>',
'PCW_MIO_22_IOTYPE': '<Select>',
'PCW_MIO_22_DIRECTION': '<Select>',
'PCW_MIO_22_SLEW': '<Select>',
'PCW_MIO_23_PULLUP': '<Select>',
'PCW_MIO_23_IOTYPE': '<Select>',
'PCW_MIO_23_DIRECTION': '<Select>',
'PCW_MIO_23_SLEW': '<Select>',
'PCW_MIO_24_PULLUP': '<Select>',
'PCW_MIO_24_IOTYPE': '<Select>',
'PCW_MIO_24_DIRECTION': '<Select>',
'PCW_MIO_24_SLEW': '<Select>',
'PCW_MIO_25_PULLUP': '<Select>',
'PCW_MIO_25_IOTYPE': '<Select>',
'PCW_MIO_25_DIRECTION': '<Select>',
'PCW_MIO_25_SLEW': '<Select>',
'PCW_MIO_26_PULLUP': '<Select>',
```

```
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'PCW_MIO_26_DIRECTION': '<Select>',
'PCW_MIO_26_SLEW': '<Select>',
'PCW_MIO_27_PULLUP': '<Select>',
'PCW_MIO_27_IOTYPE': '<Select>',
'PCW_MIO_27_DIRECTION': '<Select>',
'PCW_MIO_27_SLEW': '<Select>',
'PCW_MIO_28_PULLUP': '<Select>',
'PCW_MIO_28_IOTYPE': '<Select>',
'PCW_MIO_28_DIRECTION': '<Select>',
'PCW_MIO_28_SLEW': '<Select>',
'PCW_MIO_29_PULLUP': '<Select>',
'PCW_MIO_29_IOTYPE': '<Select>',
'PCW_MIO_29_DIRECTION': '<Select>',
'PCW_MIO_29_SLEW': '<Select>',
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'PCW_MIO_30_IOTYPE': '<Select>',
'PCW_MIO_30_DIRECTION': '<Select>',
'PCW_MIO_30_SLEW': '<Select>',
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'PCW_MIO_32_IOTYPE': '<Select>',
'PCW_MIO_32_DIRECTION': '<Select>',
'PCW_MIO_32_SLEW': '<Select>',
'PCW_MIO_33_PULLUP': '<Select>',
'PCW_MIO_33_IOTYPE': '<Select>',
'PCW_MIO_33_DIRECTION': '<Select>',
'PCW_MIO_33_SLEW': '<Select>',
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'PCW_MIO_34_DIRECTION': '<Select>',
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'PCW_MIO_35_IOTYPE': '<Select>',
'PCW_MIO_35_DIRECTION': '<Select>',
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'PCW_MIO_36_IOTYPE': '<Select>',
'PCW_MIO_36_DIRECTION': '<Select>',
'PCW_MIO_36_SLEW': '<Select>',
'PCW_MIO_37_PULLUP': '<Select>',
'PCW_MIO_37_IOTYPE': '<Select>',
'PCW_MIO_37_DIRECTION': '<Select>',
'PCW_MIO_37_SLEW': '<Select>',
```

```
'PCW_MIO_38_PULLUP': '<Select>',
'PCW_MIO_38_IOTYPE': '<Select>',
'PCW_MIO_38_DIRECTION': '<Select>',
'PCW_MIO_38_SLEW': '<Select>',
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'PCW_MIO_40_DIRECTION': '<Select>',
'PCW_MIO_40_SLEW': '<Select>',
'PCW_MIO_41_PULLUP': '<Select>',
'PCW_MIO_41_IOTYPE': '<Select>',
'PCW_MIO_41_DIRECTION': '<Select>',
'PCW_MIO_41_SLEW': '<Select>',
'PCW_MIO_42_PULLUP': '<Select>',
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'PCW_MIO_42_DIRECTION': '<Select>',
'PCW_MIO_42_SLEW': '<Select>',
'PCW_MIO_43_PULLUP': '<Select>',
'PCW_MIO_43_IOTYPE': '<Select>',
'PCW_MIO_43_DIRECTION': '<Select>',
'PCW_MIO_43_SLEW': '<Select>',
'PCW_MIO_44_PULLUP': '<Select>',
'PCW_MIO_44_IOTYPE': '<Select>',
'PCW_MIO_44_DIRECTION': '<Select>',
'PCW_MIO_44_SLEW': '<Select>',
'PCW_MIO_45_PULLUP': '<Select>',
'PCW_MIO_45_IOTYPE': '<Select>',
'PCW_MIO_45_DIRECTION': '<Select>',
'PCW_MIO_45_SLEW': '<Select>',
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'PCW_MIO_46_IOTYPE': '<Select>',
'PCW_MIO_46_DIRECTION': '<Select>',
'PCW_MIO_46_SLEW': '<Select>',
'PCW_MIO_47_PULLUP': '<Select>',
'PCW_MIO_47_IOTYPE': '<Select>',
'PCW_MIO_47_DIRECTION': '<Select>',
'PCW_MIO_47_SLEW': '<Select>',
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'PCW_MIO_48_DIRECTION': 'out',
'PCW_MIO_48_SLEW': 'slow',
'PCW_MIO_49_PULLUP': 'enabled',
'PCW_MIO_49_IOTYPE': 'LVCMOS 3.3V',
'PCW_MIO_49_DIRECTION': 'in',
```

```
   'PCW_MIO_49_SLEW': 'slow',
   'PCW_MIO_50_PULLUP': '<Select>',
   'PCW_MIO_50_IOTYPE': '<Select>',
   'PCW_MIO_50_DIRECTION': '<Select>',
   'PCW_MIO_50_SLEW': '<Select>',
   'PCW_MIO_51_PULLUP': '<Select>',
   'PCW_MIO_51_IOTYPE': '<Select>',
   'PCW_MIO_51_DIRECTION': '<Select>',
   'PCW_MIO_51_SLEW': '<Select>',
   'PCW_MIO_52_PULLUP': '<Select>',
   'PCW_MIO_52_IOTYPE': '<Select>',
   'PCW_MIO_52_DIRECTION': '<Select>',
   'PCW_MIO_52_SLEW': '<Select>',
   'PCW_MIO_53_PULLUP': '<Select>',
   'PCW_MIO_53_IOTYPE': '<Select>',
   'PCW_MIO_53_DIRECTION': '<Select>',
   'PCW_MIO_53_SLEW': '<Select>',
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ned#unassigned#unassigned#unassigned#unassigned#unassigned#unassigned#unassigned
#unassigned#unassigned#unassigned#unassigned#unassigned#unassigned#unassigned#un
assigned#unassigned#unassigned#unassigned#unassigned#unassigned#unassigned#unass
igned#unassigned#unassigned#unassigned#unassigned#unassigned#unassigned#unassign
ed#unassigned#unassigned#unassigned#unassigned#unassigned#unassigned#unassigned#
UART 1#UART 1#unassigned#unassigned#unassigned#unassigned',
   'PCW_MIO_TREE_SIGNALS': 'unassigned#unassigned#unassigned#unassigned#unassign
ed#unassigned#unassigned#unassigned#unassigned#unassigned#unassigned#unassigned#
unassigned#unassigned#unassigned#unassigned#unassigned#unassigned#unassigned#una
ssigned#unassigned#unassigned#unassigned#unassigned#unassigned#unassigned#unassi
gned#unassigned#unassigned#unassigned#unassigned#unassigned#unassigned#unassigne
d#unassigned#unassigned#unassigned#unassigned#unassigned#unassigned#unassigned#u
nassigned#unassigned#unassigned#unassigned#unassigned#unassigned#unassigned#tx#r
x#unassigned#unassigned#unassigned#unassigned',
   'PCW_PS7_SI_REV': 'PRODUCTION',
   'PCW_FPGA_FCLK0_ENABLE': '1',
   'PCW_FPGA_FCLK1_ENABLE': '0',
   'PCW_FPGA_FCLK2_ENABLE': '0',
   'PCW_FPGA_FCLK3_ENABLE': '0',
   'PCW_NOR_SRAM_CS0_T_TR': '1',
   'PCW_NOR_SRAM_CS0_T_PC': '1',
   'PCW_NOR_SRAM_CS0_T_WP': '1',
   'PCW_NOR_SRAM_CS0_T_CEOE': '1',
   'PCW_NOR_SRAM_CS0_T_WC': '11',
   'PCW_NOR_SRAM_CS0_T_RC': '11',
   'PCW_NOR_SRAM_CS0_WE_TIME': '0',
```

```
'PCW_NOR_SRAM_CS1_T_TR': '1',
'PCW_NOR_SRAM_CS1_T_PC': '1',
'PCW_NOR_SRAM_CS1_T_WP': '1',
'PCW_NOR_SRAM_CS1_T_CEOE': '1',
'PCW_NOR_SRAM_CS1_T_WC': '11',
'PCW_NOR_SRAM_CS1_T_RC': '11',
'PCW_NOR_SRAM_CS1_WE_TIME': '0',
'PCW_NOR_CS0_T_TR': '1',
'PCW_NOR_CS0_T_PC': '1',
'PCW_NOR_CS0_T_WP': '1',
'PCW_NOR_CS0_T_CEOE': '1',
'PCW_NOR_CS0_T_WC': '11',
'PCW_NOR_CS0_T_RC': '11',
'PCW_NOR_CS0_WE_TIME': '0',
'PCW_NOR_CS1_T_TR': '1',
'PCW_NOR_CS1_T_PC': '1',
'PCW_NOR_CS1_T_WP': '1',
'PCW_NOR_CS1_T_CEOE': '1',
'PCW_NOR_CS1_T_WC': '11',
'PCW_NOR_CS1_T_RC': '11',
'PCW_NOR_CS1_WE_TIME': '0',
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'PCW_NAND_CYCLES_T_AR': '1',
'PCW_NAND_CYCLES_T_CLR': '1',
'PCW_NAND_CYCLES_T_WP': '1',
'PCW_NAND_CYCLES_T_REA': '1',
'PCW_NAND_CYCLES_T_WC': '11',
'PCW_NAND_CYCLES_T_RC': '11',
'PCW_SMC_CYCLE_T0': 'NA',
'PCW_SMC_CYCLE_T1': 'NA',
'PCW_SMC_CYCLE_T2': 'NA',
'PCW_SMC_CYCLE_T3': 'NA',
'PCW_SMC_CYCLE_T4': 'NA',
'PCW_SMC_CYCLE_T5': 'NA',
'PCW_SMC_CYCLE_T6': 'NA',
'PCW_PACKAGE_NAME': 'clg400',
'PCW_PLL_BYPASSMODE_ENABLE': '0',
'Component_Name': 'design_1_processing_system7_0_0',
'EDK_IPTYPE': 'PERIPHERAL',
'CAN_DEBUG': 'false',
'TIMEPERIOD_PS': '1250',
'MEMORY_TYPE': 'COMPONENTS',
'MEMORY_PART': None,
'DATA_WIDTH': '8',
'CS_ENABLED': 'true',
'DATA_MASK_ENABLED': 'true',
'SLOT': 'Single',
```

```
  'CUSTOM_PARTS': None,
  'MEM_ADDR_MAP': 'ROW_COLUMN_BANK',
  'BURST_LENGTH': '8',
  'AXI_ARBITRATION_SCHEME': 'TDM',
  'CAS_LATENCY': '11',
  'CAS_WRITE_LATENCY': '11',
  'SUPPORTS_NARROW_BURST': '0',
  'NUM_WRITE_OUTSTANDING': '8',
  'NUM_READ_OUTSTANDING': '8',
  'PROTOCOL': 'AXI3',
  'FREQ_HZ': '50000000',
  'ID_WIDTH': '12',
  'ADDR_WIDTH': '32',
  'AWUSER_WIDTH': '0',
  'ARUSER_WIDTH': '0',
  'WUSER_WIDTH': '0',
  'RUSER_WIDTH': '0',
  'BUSER_WIDTH': '0',
  'READ_WRITE_MODE': 'READ_WRITE',
  'HAS_BURST': '1',
  'HAS_LOCK': '1',
  'HAS_PROT': '1',
  'HAS_CACHE': '1',
  'HAS_QOS': '1',
  'HAS_REGION': '0',
  'HAS_WSTRB': '1',
  'HAS_BRESP': '1',
  'HAS_RRESP': '1',
  'MAX_BURST_LENGTH': '16',
  'PHASE': '0.0',
  'CLK_DOMAIN': 'design_1_processing_system7_0_0_FCLK_CLK0',
  'NUM_READ_THREADS': '4',
  'NUM_WRITE_THREADS': '4',
  'RUSER_BITS_PER_BYTE': '0',
  'WUSER_BITS_PER_BYTE': '0',
  'INSERT_VIP': '0'},
 'driver': pynq.overlay.DefaultIP,
 'device': <pynq.pl_server.embedded_device.EmbeddedDevice at 0xb385f2e0>}}
```

[ ]:
```
# This will work only when the .bit file is loaded
ip.register_map
```

[ ]:
```
# The following are the cells for writing the values at the Slave register␣
 ↪Addresses.
# The slave register addresses can be obtained from the register map, it will␣
 ↪work only
# when the bit file is uploaded
```

[11]:
```
ip.write(0x0, 56)
ip.write(0x4, 154)
ip.write(0x8, 170)
ip.write(0xC, 184)
ip.write(0x10, 190)
ip.write(0x14, 201)
ip.write(0x18, 10)
ip.write(0x1c, 9)
```

[13]:
```
print(ip.read(0x0))
print(ip.read(0x4))
print(ip.read(0x8))
print(ip.read(0xC))
print(ip.read(0x10))
print(ip.read(0x14))
print(ip.read(0x18))
print(ip.read(0x1c))
```

```
56
154
170
184
190
201
10
9
```

[14]:
```
#Start signal
ip.write(0x60, 1)
```

[15]:
```
print(ip.read(0x60))
```

```
1
```

[18]:
```
#Done signal
print(ip.read(0x64))
```

```
1
```

[30]:
```
print(ctypes.c_int32(ip.read(0x20)).value)
print(ctypes.c_int32(ip.read(0x24)).value) #-291
print(ctypes.c_int32(ip.read(0x28)).value)
print(ctypes.c_int32(ip.read(0x2c)).value)
print(ctypes.c_int32(ip.read(0x30)).value) #-121
print(ctypes.c_int32(ip.read(0x34)).value)
print(ctypes.c_int32(ip.read(0x38)).value)
print(ctypes.c_int32(ip.read(0x3c)).value) #-290
```

```
971
```

```
-291
67
22
-121
23
67
-290
```

[31]:
```
print(ctypes.c_int32(ip.read(0x40)).value)
print(ctypes.c_int32(ip.read(0x44)).value) #-251
print(ctypes.c_int32(ip.read(0x48)).value) #-163
print(ctypes.c_int32(ip.read(0x4c)).value)
print(ctypes.c_int32(ip.read(0x50)).value)
print(ctypes.c_int32(ip.read(0x54)).value) #-69
print(ctypes.c_int32(ip.read(0x58)).value)
print(ctypes.c_int32(ip.read(0x5c)).value)
```

```
0
-251
-163
69
0
-69
163
251
```

[ ]:
```
# The following is the automated process for taking input and returning output␣
↪of the 8 point FFT
```

[38]:
```
BASE_ADDRESS = 0x00
```

[46]:
```
address_input = BASE_ADDRESS
```

[47]:
```
print("Enter the real values of the FFT")
for i in range(8):
    ip.write(address_input, int(input()))
    address_input += 4
```

```
Enter the real values of the FFT
1
0
1
0
1
0
1
0
```

[48]:
```
print("Enter the imaginary values of the FFT")
for i in range(8):
    ip.write(address_input, int(input()))
    address_input += 4
```

```
Enter the imaginary values of the FFT
1
0
0
0
0
0
0
0
```

[ ]:
```
#Start signal
ip.write(0x60, 1)
```

[ ]:
```
# Use for debugging only
# print(ip.read(0x60))
```

[ ]:
```
while(not ip.read(0x64) #Done signal):
   continue
print("The output is ready")
```

[49]:
```
address = BASE_ADDRESS + 0x20
```

[50]:
```
print("The real values are \n")
for i in range(8):
    print(ctypes.c_int32(ip.read(address)).value)
    address += 4
```

```
The real values are

971
-291
67
22
-121
23
67
-290
```

[43]:
```
print("The imaginary values are \n")
for i in range(8):
    print(ctypes.c_int32(ip.read(address)).value)
    address += 4
```

```
The imaginary values are
```

```
0
-251
-163
69
0
-69
163
251
```

[ ]: