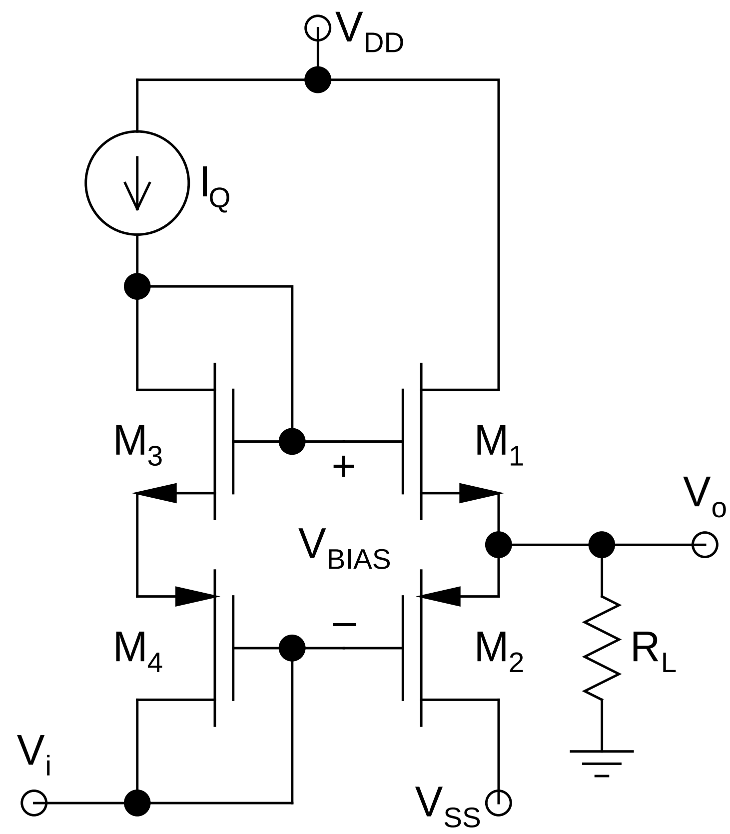
- ***Summary***:
  - ***Quite small standby power***
  - ***Large current driving capability***
  - ***Almost linear VTC***
  - ***Very low distortion at the output***
  - $A_v \sim 1$
  - ***No phase shift between input and output***
  - ***Very low output resistance***

  Thus, this stage is a superb one and is highly popular!

- ***MOS Implementation***:
  - *Biased using dual symmetric power supplies V_{DD}/V_{SS}*
  - *M_1-M_2 in push-pull configuration*
    - *M_1 supplying current to load (R_L) during the positive half cycle*
    - *M_2 pulling current away from load during the negative half cycle*



Circuit Schematic

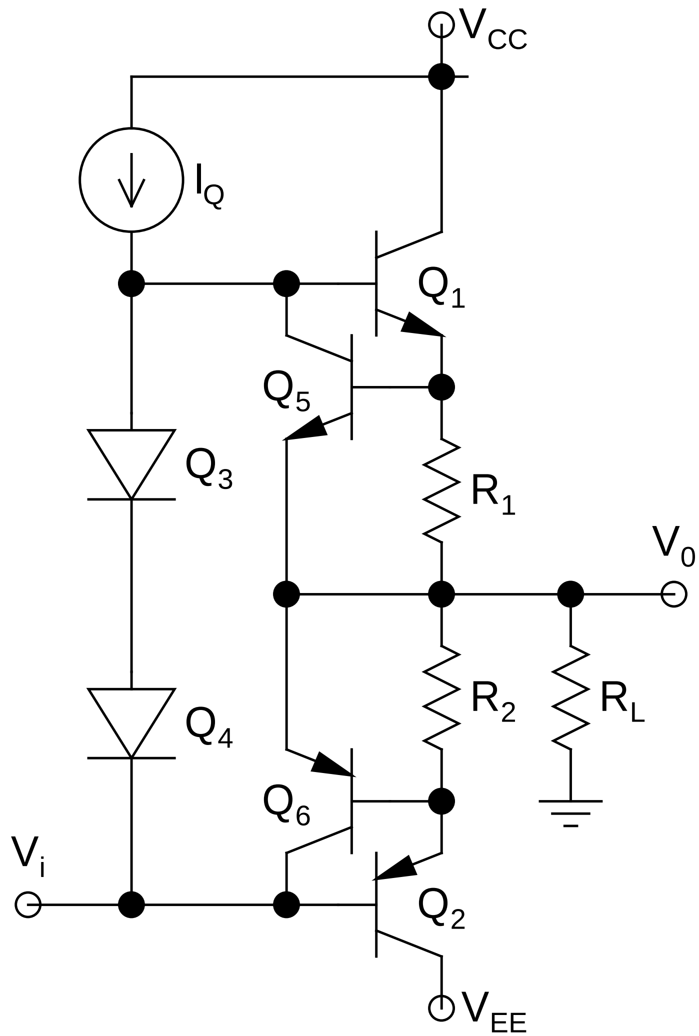
- M_1-M_2 ***prebiased*** by the ***series combination*** of M_3-M_4 (***both diode-connected***) ***biased with*** I_Q
- ***Develops*** V_{BIAS} ***across the gates of*** M_3-M_4, which is ***same as that between the gates of*** M_1-M_2
- V_{BIAS} ***chosen to be slightly less than*** $(V_{TN} + |V_{TP}|)$
- ***Crossover Distortion eliminated completely***, at the cost of ***introducing standby power*** into the system
- ***Rest of the operation of the circuit exactly similar to that of a BJT Class AB Push-Pull Output Stage***

- ***All transistors suffer from body effect problem***

  $\Rightarrow$ ***More distortion at the output***
- ***The linearity of the VTC is not that good***
- ***Low current drive capability***
- ***Biasing itself becomes tricky***, due to the ***body effect of M_3-M_4***
- The ***output resistance not that low***, since ***MOSFETs have lower g_m than BJTs***
- Overall, the stage ***suffers from quite a few problems*** and is ***not used much***
- We will explore this through an assignment

- ***Overload Protection***:
  - ***Protects the output stage from accidental short-circuits***
  - ***Needs 4 more components***:
    - ***2 BJTs*** (Q_5,Q_6)
    - ***2 Resistors*** (R_1,R_2)

    R_1,R_2 ~ 25-50 Ω



Circuit Schematic

- During ***normal operation***, these ***extra circuits*** play absolutely ***no role***, and come ***into picture*** only under ***accidental short-circuit*** of the ***output terminal to ground***
- ***Numerical Example***:
  - Assume V_i at its ***positive peak***, the ***maximum drive current*** to the base of Q_1 = 1 mA, and $\beta_1 = 100$
  - Now output gets ***accidentally shorted to ground*** ($V_o = 0$)

    $\Rightarrow$ $I_{c1} = 100\ mA$ and $V_{ce1} = 5\ V$

    $\Rightarrow$ $P_1 = 500\ mW$
  - This may be ***way above*** the ***maximum power rating*** of the transistor (~ ***100-150 mW***) and the transistor would ***burn out*** $\Rightarrow$ ***potentially dangerous situation***!

➢ ***Principle of Operation of the Protection Circuit***:

- Assume ***positive V_i*** with Q_1 ***supplying current to load***
- ***Q_2 is off during this time***
- As $R_L\downarrow$, $I_{c1}\uparrow$ (since $I_{c1} = V_o/R_L$)

  $\Rightarrow$ ***V_{be5} ($= I_{c1}R_1$) also*** $\uparrow$
- As $V_{be5} \rightarrow V_\gamma$ of Q_5, it starts to ***turn on***

  $\Rightarrow$ A ***part of base drive current*** of Q_1 starts to get ***shunted away*** by Q_5, and ***appears at the output*** almost ***without any gain*** ($1/\alpha_5$)
- This acts as a ***limit of the rate*** at which the ***output current can increase***, and thus, ***protects the circuit***

- Thus, the ***current can't increase indefinitely***
- Assume $R_1 = 30\ \Omega$ and $V_\gamma = 0.6\ V$

  $\Rightarrow$ As soon as ***I_{c1} reaches about 20 mA***, ***Q_5 cuts in***, ***shunts current away from the base of Q_1***, and ***protects the circuit***
- Due to the ***exponential dependence*** of this ***shunted current*** on V_{be5}, the ***maximum output current*** will ***saturate near around 20 mA itself***
- Thus, under this case, if the output is ***accidentally shorted to ground***, then ***$P_1(max)$ will be around 100 mW***, which is ***well within limit***, and ***protection will be achieved***