- ***Solving Eqs.(1) and (2)***:

$$I_{c1} = I_{EE}/[1 + \exp(-V_{id}/V_T)]$$

$$I_{c2} = I_{EE}/[1 + \exp(V_{id}/V_T)]$$

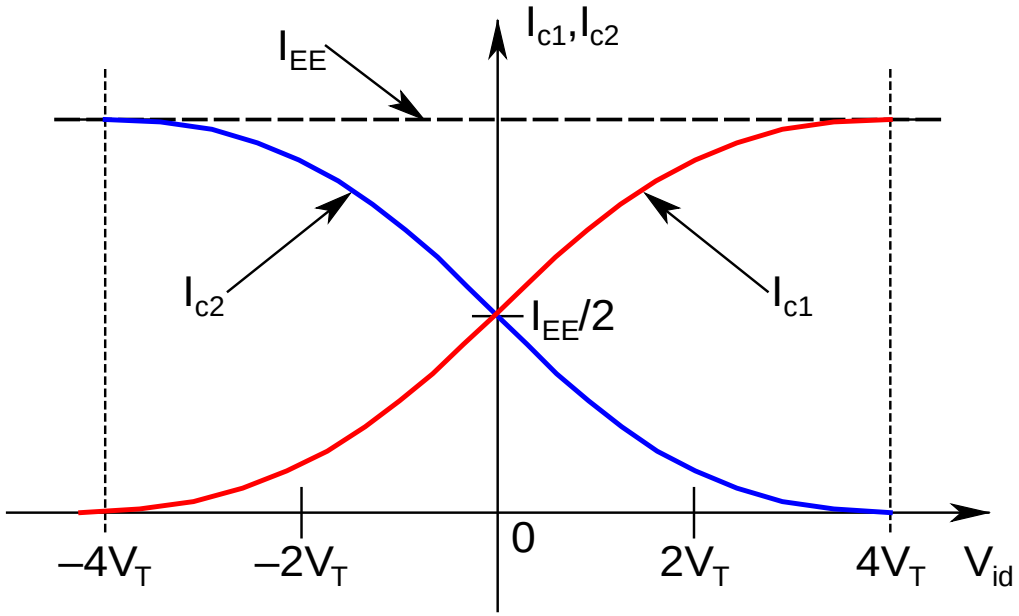
- ***Extremely interesting results***:
  - ***For $V_{id} = 0$, $I_{c1} = I_{c2} = I_{EE}/2$***

    I_{EE} shared equally between Q_1 and Q_2
  - ***For positive V_{id}, $I_{c1}\uparrow$ and $I_{c2}\downarrow$***

    For negative V_{id}, $I_{c1}\downarrow$ and $I_{c2}\uparrow$

    But for both cases, their sum is constant and equal to I_{EE}
  - ***For $V_{id} > 4V_T$, $I_{c1} \rightarrow I_{EE}$*** and ***$I_{c2} \rightarrow 0$***

    For –ve V_{id}, with $\lvert V_{id}\rvert > 4V_T$, $I_{c2} \rightarrow I_{EE}$ and ***$I_{c1} \rightarrow 0$***



The Current Transfer Characteristics of an npn DA

- ***Linear Range*** of the circuit ~ $\pm 4V_T$ (~ ***±100 mV at room temperature***)
- This range is known as the ***analog domain***

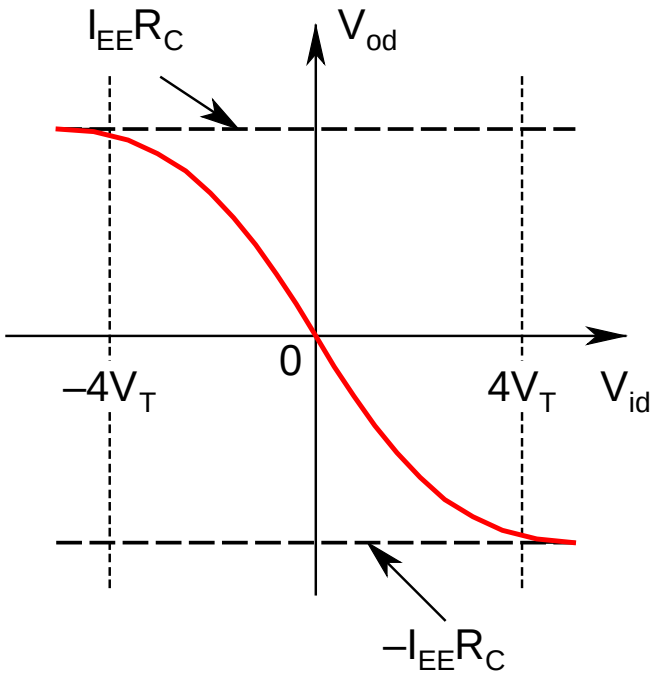
- ***For V_{id} out of this range, either Q_1 or Q_2 carries the entire I_{EE}, with the other remaining off*** $\Rightarrow$ acts as a ***Current Switch***
  - This is the ***digital domain***
- ***For analog applications, both devices must be on and in the linear range of the I_c-V_{id} characteristic***
- ***The highest linearity, which is also the region of the highest g_m ($= \partial I_c/\partial V_{id}$), occurs around $V_{id} = 0$ ($V_{i1} = V_{i2}$)***
- ***This is the most preferred DC bias point***

- ***At this point, $I_{C1} = I_{C2} = I_{EE}/2$, and all small-signal parameters of Q_1 and Q_2 are identical to each other***
- ***This particular biasing scheme leads to a Balanced DA, having properties:***
  - ***Q_1-Q_2 completely matched***
  - ***R_Cs identically equal to each other***
  - ***Both inputs connected to DC ground or to the same DC potential (ground is the best choice, obviously)***
  - ***Both Q_1 and Q_2 biased at $I_{EE}/2$***
- ***We will consider only Balanced DAs***

- ***Unbalanced DAs create anomalies in circuit operation***
- Now, the ***output voltages***:

  $V_{o1} = V_{CC} - I_{c1}R_C$ and $V_{o2} = V_{CC} - I_{c2}R_C$
- Define ***Differential-Mode Output Voltage***:

  $V_{od} = V_{o1} - V_{o2} = I_{EE}R_C\tanh[-V_{id}/(2V_T)]$
  - V_{od} (***positive maximum***) $= I_{EE}R_C$
  - V_{od} (***negative minimum***) $= -I_{EE}R_C$
  - At $V_{id} = 0$, $V_{od} = 0$
    - ***Permits direct coupling of stages without the need of any coupling capacitor***



Linear Range = $\pm 4V_T$ (~ $\pm$100 mV at room temperature)

The Voltage Transfer Characteristics of an npn DA

- ***DC Biasing***:
  - $V_i = V_I + v_i$ (V_I: ***DC bias voltage***, v_i: ***ac small-signal voltage***)
  - $I_c = I_C + i_c$ (I_C: ***DC bias current***, i_c: ***ac small-signal current***)
  - ***The ideal DC bias point should be $V_{I1} = V_{I2}$***

    $\Rightarrow$ ***$I_{C1} = I_{C2} = I_{EE}/2$***
  - ***Thus, any arbitrary DC voltage can be applied at the bases of Q_1-Q_2, provided they are same***

    $\Rightarrow$ ***Ideal choice***: ***ground***

    $\Rightarrow$ ***Necessitates a negative power supply for proper biasing***