Current-Voltage Relation

• For $V_{GS} > V_{TN}$ and *small* V_{DS} :

$$I_{D} = k_{N} \left(V_{GT} V_{DS} - V_{DS}^{2} / 2 \right)$$

$$V_{GT} = V_{GS} - V_{TN} = Gate overdrive$$

$$k_{N} = (W/L)k_{N}'$$

= Device transconductance parameter

$$W/L = Aspect ratio$$

$$k'_{N} = \mu_{n}C'_{ox}$$

- = Process transconductance parameter
- $\mu_n = Channel \ electron \ mobility$
- For *small* V_{DS} , the V_{DS}^2 term can be *neglected*
 - \triangleright I_D changes *linearly* with V_{DS}
 - Linear (or Non-Saturation) Region
- As V_{DS}^{\uparrow} , the *restraining* effect of V_{DS}^{2} term \uparrow
 - \triangleright Rate of increase of I_D with V_{DS} slows down

- For inversion channel to exist at the D end, V_{GD} must $be > V_{TN}$
 - $\gt V_{DS}$ must be $\lt V_{GT}$
- When $V_{DS} = V_{GT}$, the *channel* is said to be *pinched-off* at the *D end*, and I_D *does not increase any more*
- This value of V_{DS} is known as the *drain-to-source saturation voltage* $V_{DS,sat}$

$$\triangleright V_{DS,sat} = V_{GT}$$

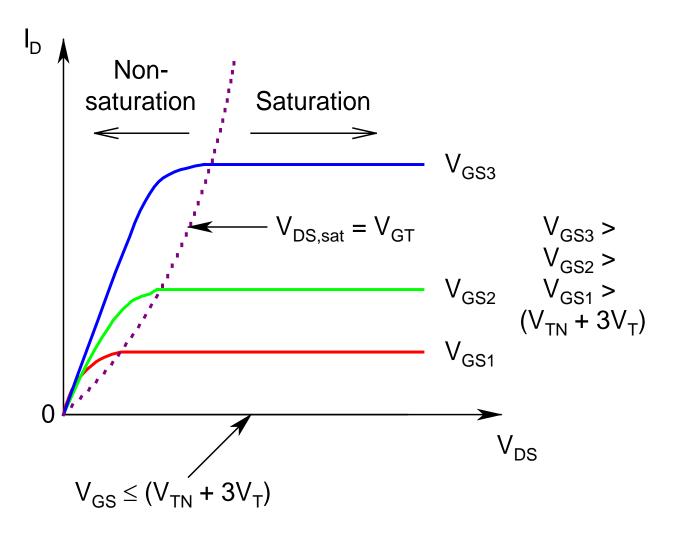
- For $V_{DS} > V_{DS,sat}$, the *mode of operation* is known as *saturation*
- Drain current in saturation:

$$I_{D} = \frac{k_{N}}{2} V_{GT}^{2}$$

- ightharpoonup Obtained from the non-saturation I_D expression by substituting $V_{DS} = V_{GT}$
- \triangleright Note that I_D is independent of V_{DS}
- Above equations are valid for $V_{GT} > 3V_T$
 - (~ 80 mV at room temperature)

The Complete LEVEL 0 Model

$$\begin{split} I_{D} &= k_{N} \left(V_{GT} V_{DS} - V_{DS}^{2} / 2 \right) \\ & \left(\textit{linear region} - V_{GT} > 3 V_{T}, V_{DS} < V_{GT} \right) \\ &= \left(k_{N} / 2 \right) V_{GT}^{2} \\ & \left(\textit{saturation region} - V_{GT} > 3 V_{T}, V_{DS} \ge V_{GT} \right) \\ &= 0 \\ & \left(\textit{cutoff region} - V_{GT} \le 3 V_{T}, \textit{any } V_{DS} \right) \end{split}$$



I_D-V_{DS} Characteristics