- Noting that $V_{B17} = V_{E16}$:

  $V_{EB23B} = V_{B16} - V_{E16} - V_{CB17} = V_{BE16} - V_{CB17}$
- Under ***normal operating condition***, $V_{BE16} \sim 0.7$ V
- If Q_{17} also is in the ***FA mode***, which is the ***desired mode of operation***, then the ***CB junction*** of Q_{17} will be ***reverse biased***

  $\Rightarrow V_{CB17}$ is ***positive***

  $\Rightarrow V_{EB23B} < V_{BE16}$, and Q_{23B} would ***remain off***
- Now, if ***for any reason whatsoever***, Q_{17} ***moves towards saturation***, then V_{CB17} would ***decrease***

- As soon as V_{CB17} ***equals zero*** (corresponding to ***onset of saturation*** of Q_{17}):
  - $\Rightarrow$ Q_{23B} would ***turn on*** and ***rob*** the ***base drive away from the base*** of Q_{16}
  - $\Rightarrow$ Q_{17} ***pushed back*** to the ***FA mode of operation***
- This ***chain of events*** is ***pretty complicated indeed***
- Thus, Q_{23B} ***prevents*** Q_{17} from ***saturating***, and thus, ***ensures optimum performance*** of the circuit

- ***Anomalies and Limitations***:
  - ***Common-Mode Rejection***
  - ***Input Offset Voltage/Input Offset Current***
  - ***Saturation Voltages***
  - ***Minimum Allowed Supply Voltage***
  - ***Slew Rate and Full-Power Bandwidth***

➢ *Common-Mode Rejection*:

- An *extremely important parameter* (*CMRR*)
- *Depends on*:
  - ❖ The *output resistance* r_{08} of Q_8
  - ❖ *Matching of the input transistors* (Q_1-Q_2 and Q_3-Q_4)
- *Higher* $r_{08} \Rightarrow$ *Better CMRR*
- *More mismatch in the input transistors* $\Rightarrow$ *Worse CMRR*
- *Exact calculation of* A_{cm} *is pretty tedious*
- A *rough estimate* of A_{cm} can be *obtained* by noting that:
  - ❖ For *common-mode input*, the *common collector point* of Q_1-Q_2 is *not at ac ground*, but *connected to the collector* of Q_8
  - ❖ $r_{o8} = V_{AP}/I_{C8} = 2.6\ M\Omega$

- Now, refer to the ***2-port equivalent*** of the ***differential-input stage***, having the ***input resistance*** R_{i2} of the ***gain stage*** as its ***load***
- Noting that the stage is basically ***CE(D)***:

$$\Rightarrow A_{cm} \simeq \frac{-\left(R_{01} \parallel R_{i2}\right)}{1/G_{m1} + 2r_{08}} = -0.48$$

- Thus:

  CMRR = $|A_{dm}/A_{cm}| = 4.85 \times 10^5$ (113.76 dB)

  which is ***phenomenal***
- This figure is ***much higher*** than that ***computed earlier***
- Of course, the ***analysis*** is ***highly simplistic***
- Even then, the ***actual value*** may be ***well above 100 dB***

- ***Input Offset Voltage/Input Offset Current***:
  - Created due to a ***mismatch*** between the ***input transistors***
  - For an ***op-amp*** with $A_{vOL} = 10^5$, operated with a ***power supply*** of ±10 V, V_{id} ***needed*** to cause V_0 to ***reach either of these two extremes*** = ±100 μV
  - The ***mismatch*** between the ***input transistors*** typically create a ***voltage difference*** between the ***inputs***, known as the ***Input Offset Voltage*** (V_{OS})
  - ***Typical value*** of V_{OS} for ***741 op-amp*** ~ 5-10 mV
  - This would ***cause*** V_0 to ***saturate*** at either $+V_{CC}$ or $-V_{CC}$
  - This is known as ***saturation*** or ***latch-up*** problem

- In ***741***, there is a ***provision*** to ***eliminate*** this ***problem***, known as ***offset nulling***
- Refer to the ***circuit*** of 741, and note ***pin numbers*** 1 and 5 ***connected*** to the ***emitters*** of Q_5 and Q_6
- Between these ***two pins***, a ***potentiometer*** is connected, with its ***wiper*** connected to $-V_{CC}$
- This ***potentiometer*** is known as the ***offset null resistor***
- It ***eliminates*** the ***effect*** of V_{OS} by ***creating*** an ***unequal division*** of ***bias currents*** in the ***two branches*** of the ***input circuit***, just enough to ***balance*** the ***difference*** caused due to ***device mismatch***

- ***Procedure***:
  - ***Tie both inputs to ground***: V_0 would most likely ***saturate*** at either $+V_{CC}$ or $-V_{CC}$
  - Next, ***move the wiper*** of the ***potentiometer*** in the ***direction*** that creates a ***magnitude reduction*** of V_0
  - Towards the ***end***, it will become ***very sensitive***, and a ***perfect nulling***, i.e., V_0 becoming ***exactly zero***, ***may not be possible***
  - The ***typically expected minimum value*** of V_0 may be ~ 5-10 mV
  - Leave the ***potentiometer setting*** at the ***best possible*** achieved result
  - ***Done***!