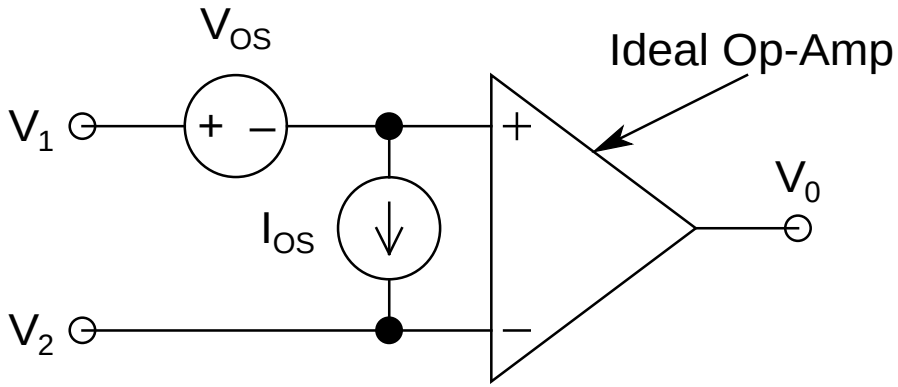
- ***The Input Offset Current (I_{OS})***:
  - ***Difference*** between the ***base currents*** (known as ***Input Bias Currents*** I_1 and I_2) of Q_1 and Q_2
  - ***Extremely small*** (~ ***tens to hundreds of nA***)
- I_{OS} and V_{OS} are actually ***interrelated***, since both of them are created due to ***device mismatch***, and have almost ***identical manifestations***



Both V_{OS} and I_{OS} are not used
V_{OS} (I_{OS}) is used when the input is voltage (current)

Modeling of the Anomalies With Regard to V_{OS} and I_{OS}

➢ *Saturation Voltages*:

- An *ideal op-amp* should have *rail-to-rail swing* at the *output*
- The *actual output swing* of a *real op-amp* is *never between rail-to-rail*
- Refer to the *op-amp schematic*, in conjunction with the *schematics* of the *gain stage* and the *output stage*
- As V_{i2} of the *gain stage* becomes *positive*, V_{02} (= V_{i3}) goes *negative* with a *large gain*

  $\Rightarrow$ V_2 and V_0 *follow* V_{i3} due to *emitter follower* (CC) action
- With V_0 *negative*, Q_{14} *turns off*, and Q_{20} *draws current from the load*

- Assuming that Q_{17} can ***soft saturate***, and neglecting the ***voltage drop*** across R_8, the ***minimum possible value*** of V_0:

  $V_0^- = -V_{CC} + V_{CE17}(SS) + V_{EB23A} + V_{EB20} = -13.4$ V

- Note that it is about ***two diode drops above*** $-V_{CC}$
- Now, for ***negative*** V_{i2}, V_{02} ***swings*** to a ***large positive value***, ***followed by*** V_2 and V_0
- With V_0 ***positive***, Q_{20} ***turns off***, and Q_{14} ***supplies current to load***
- ***Maximum positive limit*** of V_0 is ***reached*** when Q_{13A} ***soft saturates***:

  $V_0^+ = V_{CC} - V_{EC13A}(SS) - V_{BE14} = 14.1$ V

- Note again that it is ***lower*** than V_{CC} by ***little more than one diode drop***
- Also, interesting to note is that the ***positive*** and ***negative*** peaks of V_0 are ***not same***

  $\Rightarrow$ ***Maximum possible output swing is asymmetric***
- These ***two limits*** of V_0 are known as ***positive and negative saturation voltages*** (V_{SAT}^{+} and V_{SAT}^{-} respectively)
- If the ***input drive*** to the ***op-amp*** and the ***gain*** are such that the ***magnitude*** of V_0 becomes ***greater*** than either V_{SAT}^{+} or $|V_{SAT}^{-}|$, then V_0 would get ***clipped*** at either of these ***two values***

➢ *Minimum Allowed Supply Voltage*:

- Circuit for 741 is ***extremely robust***, and can be ***operated*** with a ***very wide range*** of ***supply voltage***
- However, there is a ***lower limit*** of the ***supply voltage***, below which it ***can't be ensured*** that ***all transistors*** operate in the ***FA region***
- To find this, look for the ***branch*** containing the ***most number of transistors***, since ***that branch*** would obviously ***need the largest voltage*** across it to ***ensure*** that all its ***constituent transistors operate in the FA region***
- From the ***circuit schematic*** of 741, ***this branch*** can be very easily identified to be ***either of the two sections of the input stage***

- Considering the ***left branch***, neglecting the ***potential dropped*** across R_1, and not letting ***CE voltage*** of any of the ***transistors*** to ***drop below*** 0.7 V (***onset of saturation***), there would ***four diode drops*** (~ 2.8 V) ***along this branch***

  $\Rightarrow$ ***741 should work satisfactorily for power supply all the way down to about ±3 V***

  $\Rightarrow$ ***Under this power supply***, ***V_0^+ and V_0^- will be 2.1 V and –1.4 V respectively***

- Thus, there is a ***wide range*** of ***power supply***, ***starting from ±3 V***, for which ***741 should work satisfactorily***

  $\Rightarrow$ ***Shows the robustness of the circuit***

➢ *Slew Rate and Full-Power Bandwidth*:

- This *limitation* is *observed* under *large-signal operation*, when the *input signal swing* is *greater* than the *linear range* of the *input differential pair*
- *Recall*: The *linear range* of a *bipolar differential pair* is ~ $\pm 4V_T$
- *Beyond this*, it basically *acts like a switch*, *transferring the bias current between the two branches*, *depending on the sign of the input voltage*
- Under such cases, the *compensation capacitor* C_C *limits* the *maximum possible rate of change* of V_0
- This is known as the *Slew Rate* (SR) of the op-amp:

  $SR = (dV_0/dt)_{max}$

- ***Two*** SRs are defined: SR^+ (***positive SR***) and SR^- (***negative SR***) for ***positive*** and ***negative*** excursions of V_0 respectively, generally expressed in ***V/μsec***
- A ***rough estimate*** of these quantities can be obtained by referring to the ***schematic*** of the op-amp
- Assume that a ***large negative signal*** is applied at the ***base*** of Q_1 (w.r.t. the base of Q_2)
- This will instantly turn the Q_1-Q_3 branch ***off***

  $\Rightarrow$ Q_5, and thus, Q_6, ***turn off***

  $\Rightarrow$ ***Entire bias current*** I_{C8} would ***flow through*** the Q_2-Q_4 branch, and ***start to charge*** C_C

- Note that the ***rate of this charging*** would be ***constant*** (***constant current charging***)

  $\Rightarrow$ ***Collector potential*** of Q_{17} would ***increase linearly with time***

- Due to ***emitter follower*** action of Q_{23A} and Q_{14}, V_0 would also start to ***increase linearly with time***

  - Q_{20} ***remains off***, since V_0 is in its ***positive excursion***

- Thus:

  $SR^+ = I_{C8}/C_C = (19\ \mu A)/12.5\ pF) = 1.52\ V/\mu sec$

- If the ***frequency*** of the ***input signal*** is such that the ***required time rate of change*** of V_0 is ***more*** than this, then V_0 ***won't be able to follow*** the input – rather, it will be ***dictated*** by the SR^+, and will ***change linearly with time***