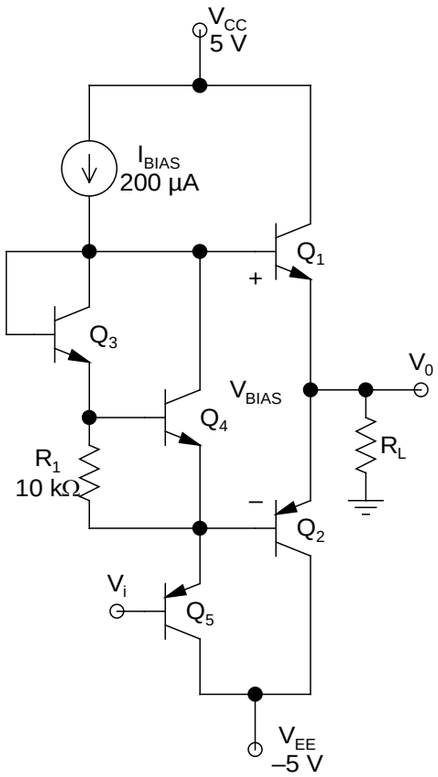
Department of Electrical Engineering
Indian Institute of Technology, Kanpur

EE 210 **END-SEM P3** **6.5.21**

$I_{S3} = I_{S4} = 2$ fA, $I_{S1} = I_{S2} = 10$ fA. I_{BIAS} is ideal. All transistors have $\beta = 200$ (neglect any drop in the value of β at low current levels).



With R_L removed:

a) Perform a self-consistent analysis, and find the split of I_{BIAS} in Q_3 and Q_4. **3**

b) Evaluate V_{BIAS}. **2**

c) What should be the DC offset of V_i to ensure that the DC offset of V_0 is zero? **1**

d) If V_i is a ±4 V sinuosid superimposed on the DC offset calculated in part c), what's the peak-to-peak swing of V_0? Justify your answer. **2**

e) What is the *total* standby power dissipation? **1**

With $R_L = 1$ kΩ:

f) Determine the power conversion efficiency. **3**