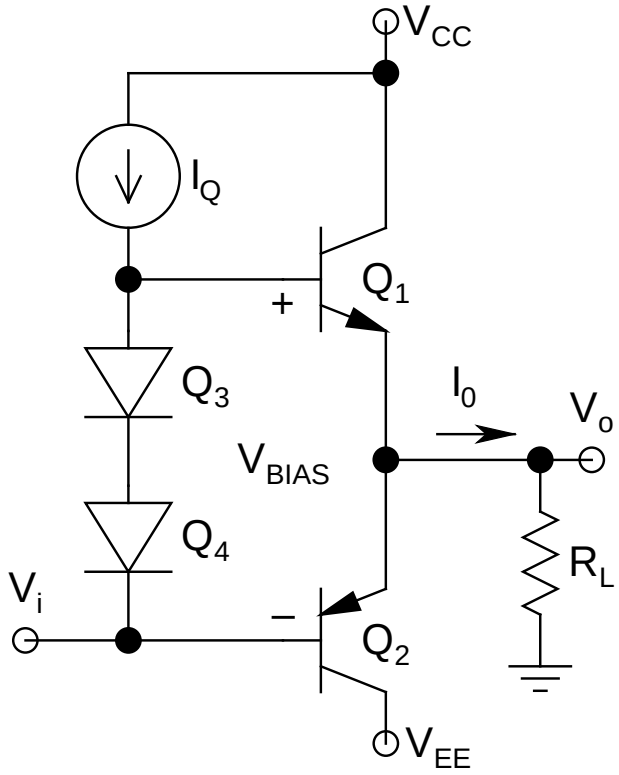
- ***BJT Implementation***:
  - ***Needs additional circuitry*** (I_Q-Q_3-Q_4)
  - Q_3-Q_4 ***diode-connected*** transistors and both are ***biased by the same current*** I_Q
  - This produces a ***DC bias*** V_{BIAS} between the ***bases*** of Q_1-Q_2



Circuit Schematic

- Consider ***idling condition*** with ***R_L open-circuited*** (***$I_0 = 0$***)
- ***Neglecting base currents*** of Q_1-Q_2, ***I_Q flows through Q_3-Q_4*** and ***develops a voltage drop***:

$$V_{BIAS} = V_{BE3} + V_{BE4} = V_T \ln\left(\frac{I_Q^2}{I_{S3} I_{S4}}\right)$$

- ***I_Q, I_{S3}, and I_{S4} chosen such that $V_{BIAS} \approx 2V_\gamma$***
- ***Note***: ***V_{BIAS} is also equal to (V_{BE1} + V_{EB2})***

  $\Rightarrow$ ***Q_1-Q_2 remain at the verge of conduction***, ***carrying a standby (or idling) current $I_{Standby}$***

- This ***extra current*** of ($I_Q + I_{standby}$) causes ***standby*** (or ***idling***) power dissipation
- Noting that:

$$V_{BIAS} = V_{BE1} + V_{EB2} = V_T \ln\left(\frac{I_{Standby}^2}{I_{S1}I_{S2}}\right)$$

$$\Rightarrow I_{Standby} = I_Q\sqrt{\frac{I_{S1}I_{S2}}{I_{S3}I_{S4}}}$$

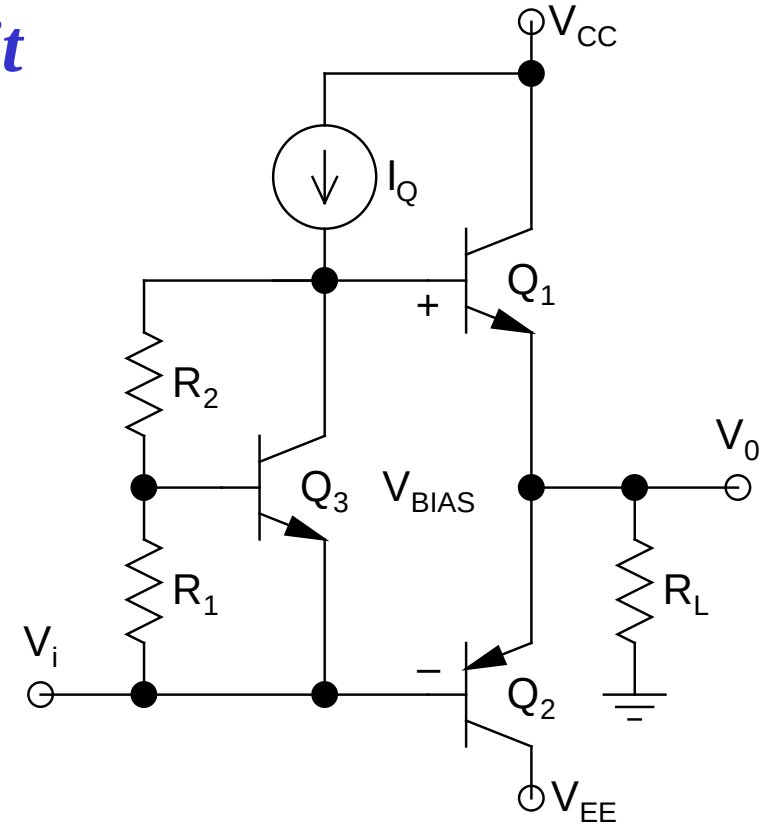
- Now, ***Q_1-Q_2 has to supply/sink large amount of current to/from load*** $\Rightarrow$ ***Their BE junction areas are made large*** $\Rightarrow$ ***Large I_{S1}-I_{S2}***

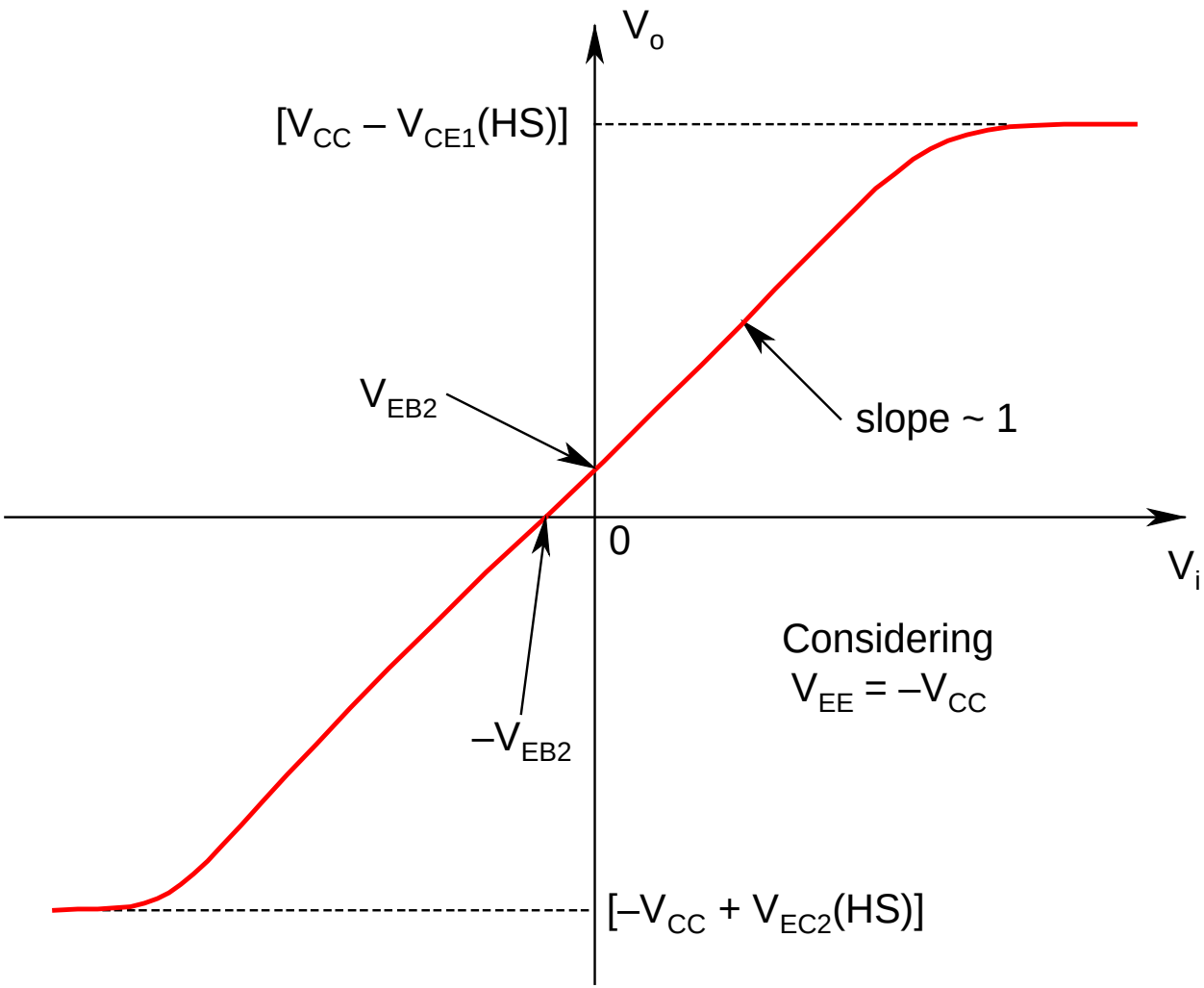
- I_{S1}-I_{S2} typically 10 times or more than I_{S3}-I_{S4}

  $\Rightarrow I_{standby} \geq 10 I_Q$

  $\Rightarrow$ Adds to the power overhead of the circuit

- Another option of prebias circuit:
  - V_{BE}-Multiplier
  - $V_{BIAS} = V_{BE3}(1 + R_2/R_1)$
  - Values of R_1 and R_2 chosen to give $V_{BIAS} = 2V_\gamma$





The Voltage Transfer Characteristic (VTC)

- ***The VTC does not pass through origin***
- ***Intercepts*** (known as ***input-output offset***):
  - $V_i = 0$, $V_o = +V_{EB2}$
  - $V_o = 0$, $V_i = -V_{EB2}$
- ***For $V_i > -V_{EB2}$, $V_{be1}\uparrow$ and $V_{eb2}\downarrow$, with their sum remaining constant at V_{BIAS}***

  $\Rightarrow$ ***Q_1 starts to conduct and supply current to the load*** (R_L), while ***Q_2 starts to go deeper into cutoff***

  $\Rightarrow$ ***V_o starts to follow V_i with a slope ~1*** (***CC stage***)

- ***V_o can rise all the way up to $[V_{CC} - V_{CE1}(HS)]$, provided that V_i can drive it that far***
- Similarly, ***for $V_i < -V_{EB2}$, $V_{eb2} \uparrow$ and $V_{be1} \downarrow$, with their sum again remaining constant at V_{BIAS}***

  $\Rightarrow$ ***Q_2 starts to conduct and pull current away from the load*** (R_L), while ***Q_1 starts to go deeper into cutoff***

  $\Rightarrow$ ***V_o again starts to follow V_i with a slope ~1***, and ***can go down all the way to $[V_{EE} + V_{EC2}(HS)]$***