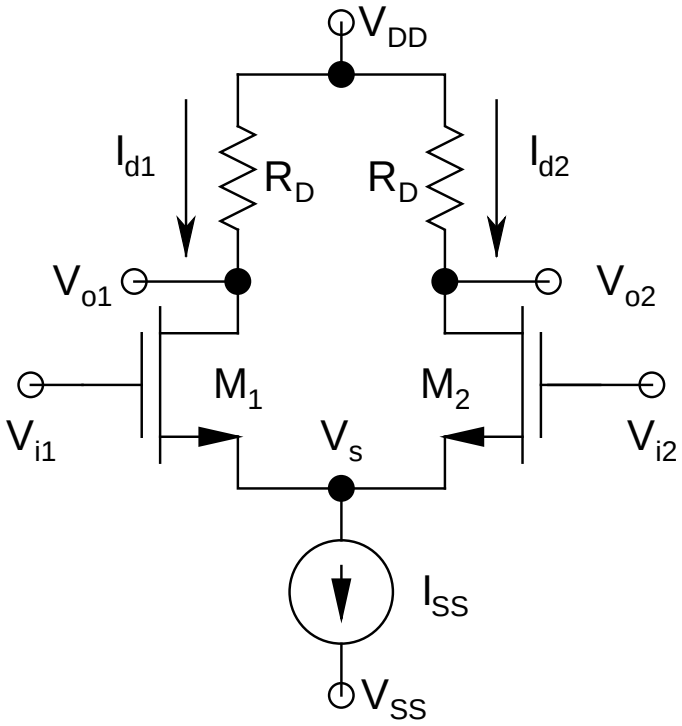
- ***NMOS DA (SCP)***:
  - M_1-M_2 constitute a ***perfectly matched pair***, and have their ***sources connected together***, hence, the name
  - I_{SS}: ***DC bias current source***
  - ***All voltages and currents are instantaneous***



NMOS DA Topology

- $V_{gs1} = V_{i1} - V_s$, and $V_{gs2} = V_{i2} - V_s$
- ***KVL around M_1-M_2 GS loop***:

$$V_{i1} - V_{gs1} + V_{gs2} - V_{i2} = 0$$

$$\Rightarrow V_{gs1} - V_{gs2} = V_{i1} - V_{i2} = V_{id}$$

- ***Neglecting CLM Effect***:

$$I_{d1} = \frac{k'_N}{2}\left(\frac{W}{L}\right)\left(V_{gs1} - V_{TN1}\right)^2 \quad \text{and}$$

$$I_{d2} = \frac{k'_N}{2}\left(\frac{W}{L}\right)\left(V_{gs2} - V_{TN2}\right)^2$$

- Ran into a problem, since ***both M_1 and M_2 would have body effect present***
  - ***Both bodies connected to V_{SS}***, but the ***common source node is at a floating potential V_s***

    $\Rightarrow$ ***Analytical evaluation of I_{d1} and I_{d2} becomes pretty tedious***
- ***If the CLM effect is also included***, then ***the problem would need numerical solution***!
- To get a ***first-order estimate***, ***neglect body effect***

  $\Rightarrow V_{TN1} = V_{TN2} = V_{TN0}$

- Thus:

$$V_{id} = \frac{\sqrt{I_{d1}} - \sqrt{I_{d2}}}{\sqrt{\frac{k'_N}{2}\left(\frac{W}{L}\right)}} \qquad (1)$$

- Also:

$$I_{d1} + I_{d2} = I_{SS} \qquad (2)$$

- ***Solving Eqs.(1) and (2)***:

$$I_{d1} = I_{SS}/2 + \xi \quad \text{and}$$

$$I_{d2} = I_{SS}/2 - \xi$$

$$\xi = \frac{k'_N}{4}\left(\frac{W}{L}\right)V_{id}\sqrt{\frac{4I_{SS}}{k'_N(W/L)} - V_{id}^2}$$

- For $V_{id} = 0$, $\xi = 0$, and $I_{d1} = I_{d2} = I_{SS}/2$
  - *Most preferred DC bias point of the circuit*
- *For $V_{id} > 0$, $I_{d1}\uparrow$ and $I_{d2}\downarrow$*
- *For $V_{id} < 0$, $I_{d1}\downarrow$ and $I_{d2}\uparrow$*
- But *for both cases*, the *sum of I_{d1} and I_{d2} remains constant at I_{SS}*
- *Linear Range* of this circuit is *defined by the values of V_{id}*, which *turns either M_1 or M_2 off*

- To find the ***Linear Range***, ***use Eq.(1)*** and ***put either I_{d1} or I_{d2} equal to I_{SS}***:

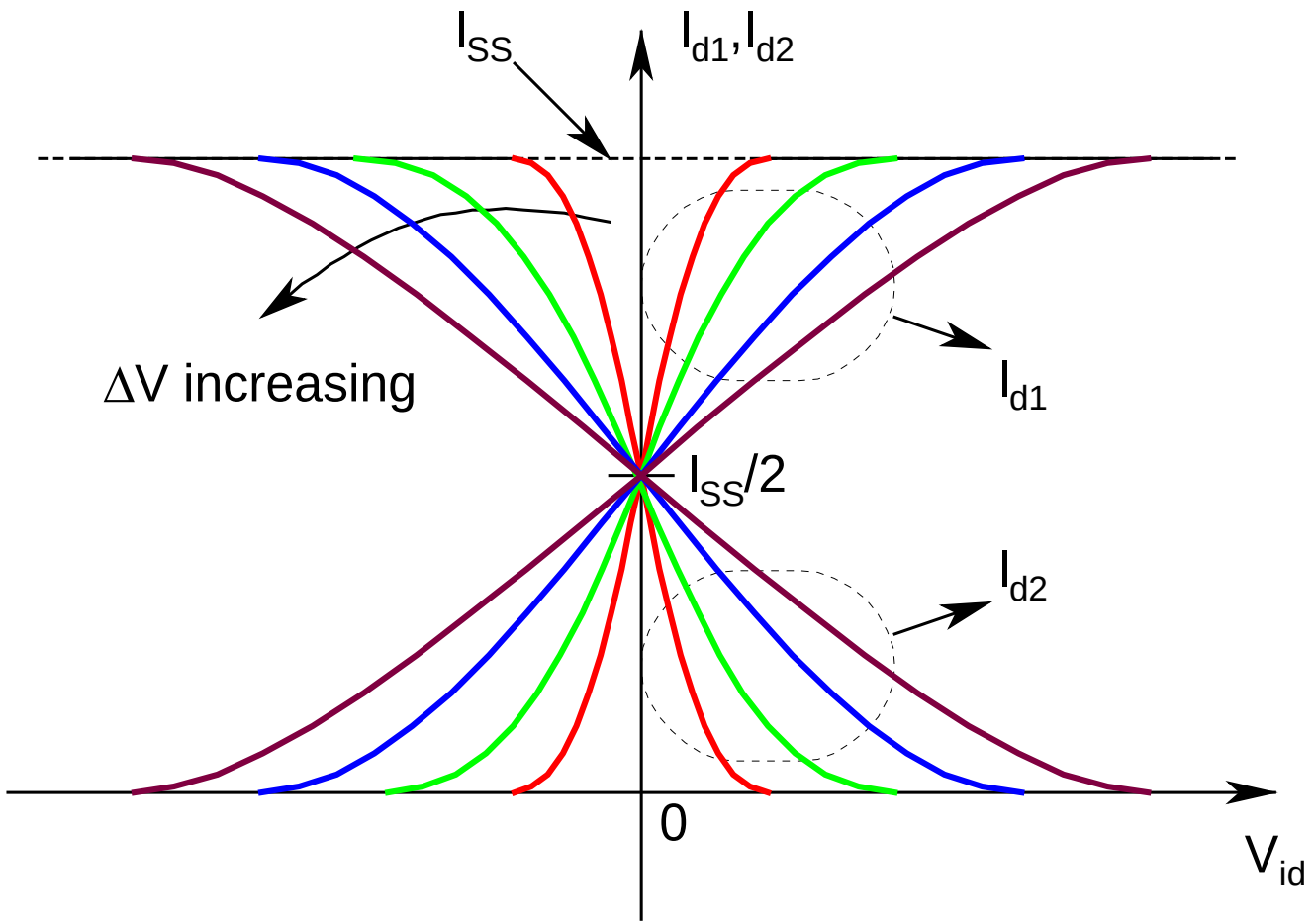
$$\Rightarrow V_{id} = \pm\sqrt{\frac{2I_{SS}}{k'_N(W/L)}} = \pm\sqrt{2}\left(\sqrt{\frac{2I_{d1}}{k'_N(W/L)}}\right)\Bigg|_{V_{id}=0}$$

$$= \pm\sqrt{2}\,(\Delta V)\Big|_{V_{id}=0}$$

since for $V_{id} = 0$, $I_{SS} = 2I_{d1} = 2I_{d2}$

ΔV = ***Gate Overdrive for M_1/M_2 for $V_{id} = 0$***

- ***Thus, the Linear Range is a function of I_{SS} and (W/L)*** $\Rightarrow$ ***Tremendous flexibility***!
- ***Recall***: In ***npn DA***, this ***Linear Range*** was ***$\pm 4V_T$***, and ***depended only on temperature***



The Current Transfer Characteristics of an NMOS DA