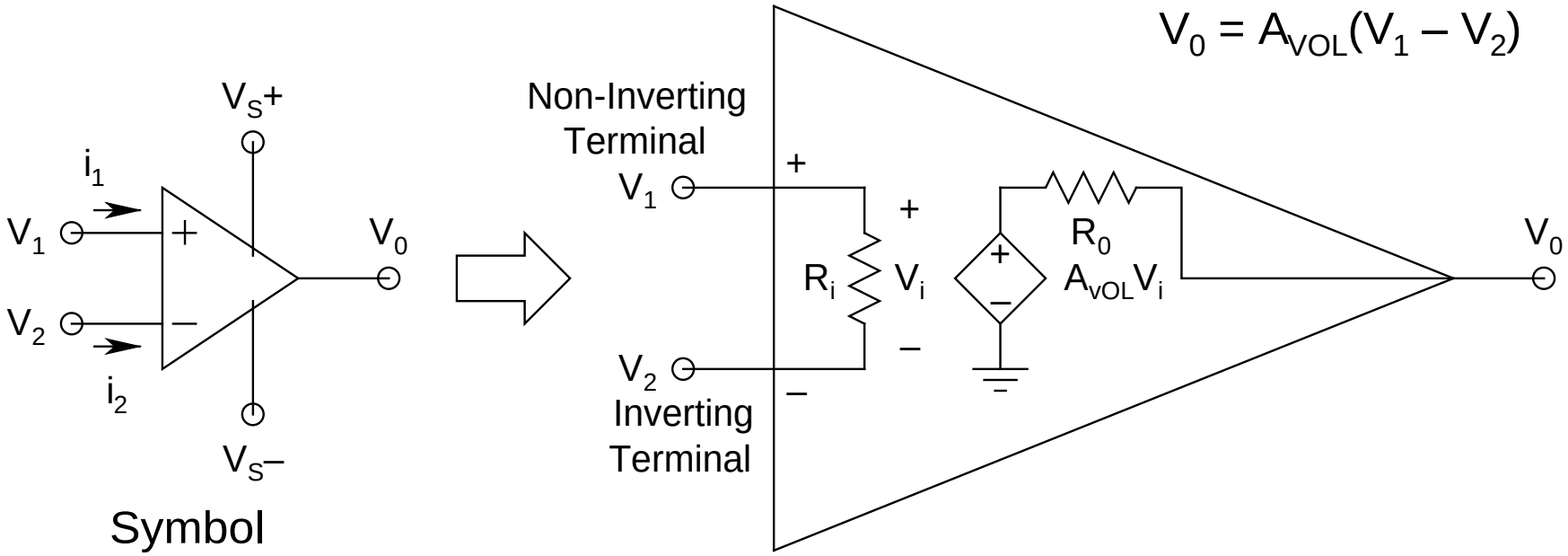
Operational Amplifier [Op-Amp (OA)]

- Gem of analog circuits: extremely versatile and has multitude of applications
- ***Two inputs***, ***one output***, and ***biased with dual symmetric power supplies***
- ***Extremely large open-loop gain and input resistance***, and ***very small output resistance***
- Has ***very high bandwidth*** too $\Rightarrow$ ***prone to oscillations*** $\Rightarrow$ needs to be ***compensated*** $\Rightarrow$ **reduces available bandwidth to ~5-10 Hz**

- **Most important property**:
  - ***Rejects signals common to both inputs***
  - Denoted by a parameter known as the ***Common-Mode Rejection Ratio*** (**CMRR**)
  - Has ***very high CMRR*** $\Rightarrow$ **suppresses noise**
- **Limitations/Anomalies**:
  - ***Offset Voltage and Offset Current***
  - ***Saturation Voltages***
  - ***Slew Rate***
  - ***Minimum Allowed Supply Voltage***

Op-Amp Symbol & Schematic:



V_1, V_2: Input Voltage, V_0: Output Voltage, i_1, i_2: Input Current
V_S+, V_S-: Dual Symmetric Power Supplies, R_i: Input Resistance
R_0: Output Resistance, A_{VOL}: Open-Loop Gain

* OAs are essentially ***voltage amplifiers***
  - Note the ***VCVS*** configuration at the output
* Note that the ***difference signal*** $V_i \ (= V_1 - V_2)$ is a ***floating signal*** (i.e., a signal that is measured between two points, ***none of which may be ground***)
  - However, ***the output V_0 is always measured with respect to ground***
* ***Typical values***: $\mathbf{A_{VOL} \geq 10^5}$, $\mathbf{R_i \geq 1\,M\Omega}$, $\mathbf{R_0 \leq 100\,\Omega}$, $\mathbf{V_{S^+}}$ **and** $\mathbf{V_{S^-}} = \mathbf{\pm 3\,V\ (minimum) - \pm 15\,V}$, $\mathbf{CMRR \geq 80\,dB\ (10^4)}$, **Uncompensated Bandwidth** $\mathbf{\geq 1\,MHz}$, **Compensated Bandwidth** $\mathbf{\leq 10\,Hz}$

* Basically a ***voltage amplifier*** (**amplifies ac as well as DC, subject to power supply limits**)
* For $V_1 > V_2$, V_0 ***is positive*** $\Rightarrow$ terminal for V_1 is termed as **non-inverting**
* For $V_2 > V_1$, V_0 ***is negative*** $\Rightarrow$ terminal for V_2 is termed as **inverting**
* R_i ***is extremely large*** $\Rightarrow$ for all practical purposes, the input currents to the op-amp can be neglected

  $\Rightarrow i_1 = i_2 = 0$
* ***Famous OA paradox***: **The input terminals are open and short at the same time**

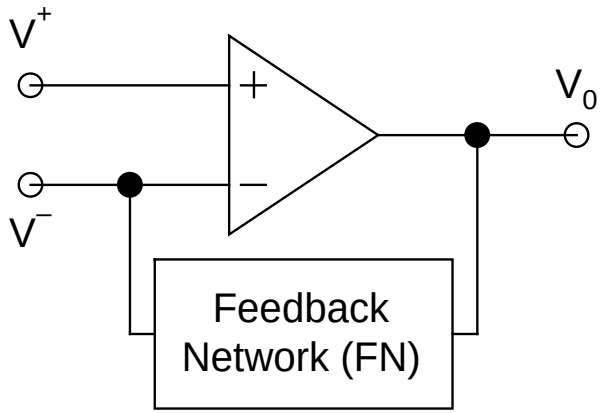
Brief Background History:

* In 1965, ***Bob Widlar*** of ***Fairchild Semiconductors*** (bought by ***ON Semiconductors*** in 2016) designed the first ***monolithic*** (**single substrate**) OA
* Named it ***μA 709*** (μA was a prefix used for Fairchild products)
* A number of improvements were carried out almost immediately, and the next generation OA was marketed as ***μA 741***
* Became a huge hit, and 741 became synonymous with OAs (***uses bipolar technology***)

Applications:

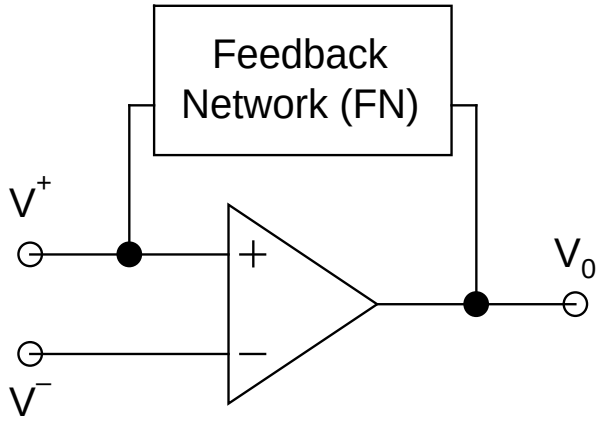
* **Open-loop**: No input-output connection, i.e., ***no feedback***
* **Closed - loop**:
  - ***Negative*** (***degenerative***) ***feedback***: the output fed back to the input in such a way that it ***opposes*** the very cause producing it $\Rightarrow$ **stable system**
  - ***Positive*** (***regenerative***) feedback: the output fed back to the input in such a way that it ***adds*** to the input and produces more output and the process repeats $\Rightarrow$ **highly unstable system**

Negative Feedback:



* Output fed back to the ***inverting*** terminal of the OA through the FN
* $V_0 = A_v\left(V^+ - V^-\right)$
* If due to some reason, V_0 ***increases***, then V^- would ***increase***, which would pull V_0 ***down***
* Thus, the effect is ***opposing*** the cause that produced it
  - $\Rightarrow$ **Negative Feedback**
  - $\Rightarrow$ **Stable System**: All disturbances die down automatically

Positive Feedback:



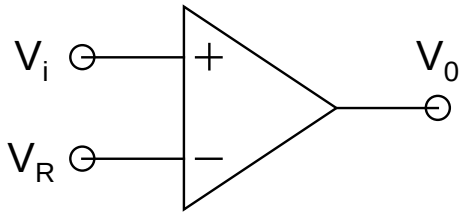
* Output fed back to the ***non-inverting*** terminal of the OA through the FN
* $V_0 = A_v\left(V^+ - V^-\right)$
* If due to some reason, V_0 ***increases***, then V^+ would ***increase***, which would ***increase*** V_0 further, and the process would repeat
* Thus, the effect is ***aiding*** the cause that produced it
  - $\Rightarrow$ **Positive Feedback**
  - $\Rightarrow$ **Highly Unstable System**: All disturbances build up, eventually leading to ***oscillations*** at the output

Open-Loop:

*** Comparator**

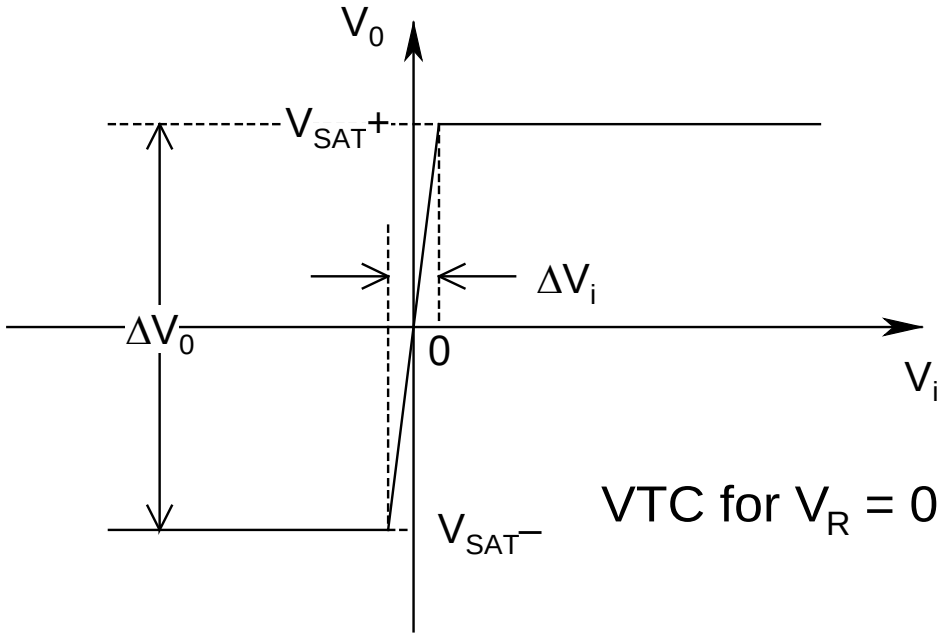
*** Zero-Crossing Detector (Square-Wave Generator)**

Comparator:



V_R: Reference Voltage

Compares V_i with V_R
and produces output



VTC for $V_R = 0$

Diagram not to scale

* Generally, the power supply connections to the OA are not shown for brevity, though they are of course very much there
* We will follow this practice hence onward
* With $V_R = 0,$ and due to very large A_{VOL}:
  - For positive V_i, V_0 saturates at V_{SAT^+} (***positive saturation voltage***, which is very close to the ***positive power supply***)
  - For negative V_i, V_0 saturates at V_{SAT^-} (***negative saturation voltage***, which is very close to the ***negative power supply***)

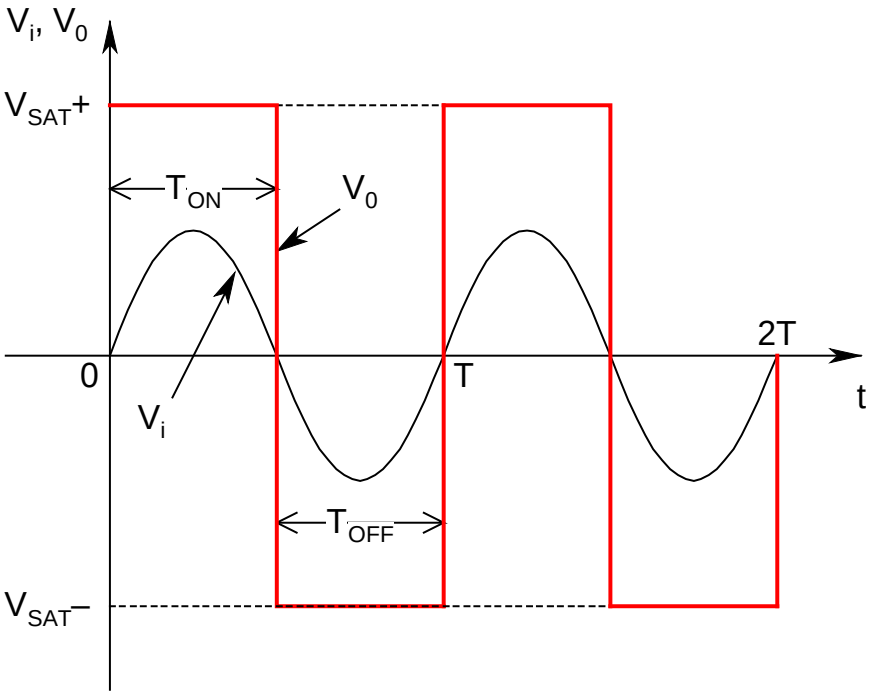
* The ***finite slope*** of the VTC is caused by ***finite*** A_{VOL}
* If A_{VOL} ***were infinite***, then the change of V_0 would have been ***instantaneous*** (i.e., $\Delta V_i \to 0$)
* ***Estimate of*** ΔV_i:
  - Let $V_{SAT} = \pm 15$ V and $A_{VOL} = 10^5$:

$$\Rightarrow \Delta V_i = \left(V_{SAT^+} - V_{SAT^-}\right) \Big/ A_{VOL} = \left(30\ \text{V}\right) \Big/ 10^5$$

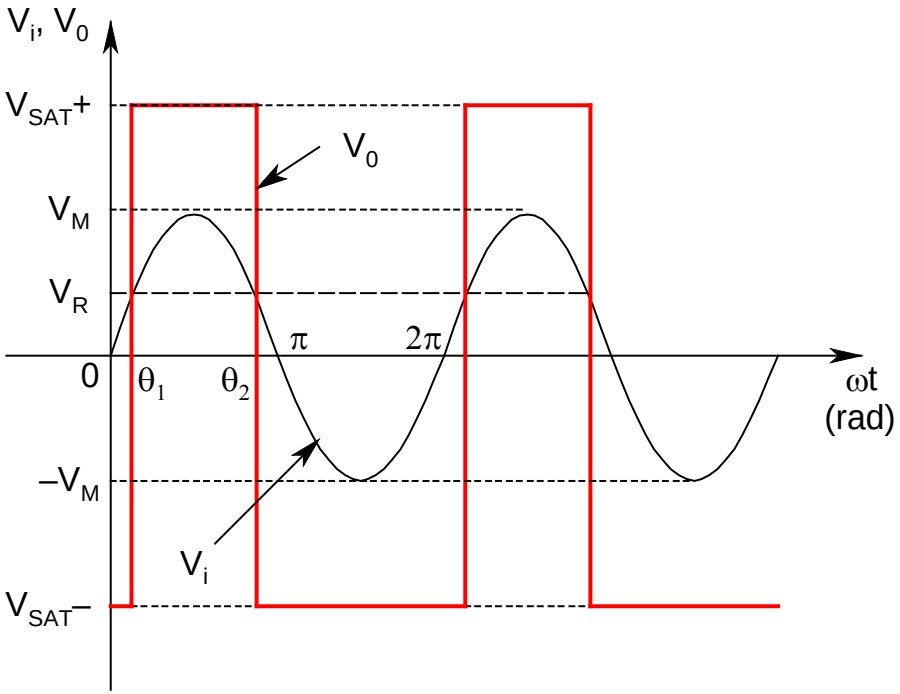
$$= 0.3\ \text{mV} = 300\ \mu\text{V (really small!)}$$

* If $V_R \neq 0$, then the change would take place around V_R
  $\Rightarrow$ Known as **Comparator with Threshold**
* Can be used in ***digital circuits*** too
  $\Rightarrow$ Known as **Digital Comparator**

Zero-Crossing Detector (Square-Wave Generator):



$V_R = 0$



$V_R > 0$

* Simple ***comparator*** with ***sinusoidal input*** (V_i) and with a ***reference voltage*** V_R

* Output changes state when input ***crosses zero*** (for $V_R = 0$) or ***crosses*** V_R $\left(V_R \neq 0\right)$
* ***Duty Cycle*** (δ) of a square wave: $\delta = T_{ON}/T$, where T $\left(= T_{ON} + T_{OFF}\right)$ is the ***Time Period***
* ***Note***:
  - For $V_R = 0$, $\delta = 50\%$
  - For positive V_R, $\delta < 50\%$
  - For negative V_R, $\delta > 50\%$
* By adjusting the ***sign and magnitude*** of V_R, we can achieve ***any value*** of δ
* ***Note that amplitude of V_i is immaterial***

Example: $V_i = V_M \sin(\omega t)$, with $V_M = 5$ V, and $V_R = 1$ V. Find δ.

First, we find $\theta_1 = \sin^{-1}\left(\frac{V_R}{V_M}\right) = 11.54°$, and

$$\theta_2 = 180° - \theta_1 = 168.46°$$

Thus, the angle over which the output is high

$= (\theta_2 - \theta_1) = 156.92°$

$\Rightarrow$ Duty Cycle $\delta = \frac{156.92°}{360°} = 0.436$ or 43.6%

Exercise: Evaluate δ for $V_R = -1$ V

Anomaly : Offset Voltage and Current:

* The previous two analyses assume that when $V_i = 0$, $V_0 = 0$, i.e., the ***VTC passes through origin***
* This is ***true for ideal OAs***
* However, ***real OAs*** have an ***inherently built-in voltage difference*** between its two inputs, which would ***always make the output saturated***, ***even with zero input***

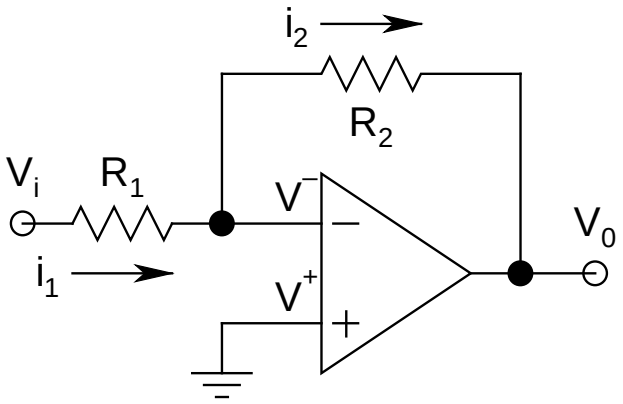
* Happens due to ***component mismatch*** in the OA circuit
* Known as the **Offset Voltage** (V_{OS})
* Typical values of V_{OS} ~ **1-10 mV**
* Also, for a ***real OA***, the input currents i_1 and i_2 are ***not zero***, ***but finite and unequal***

  $\Rightarrow$ The difference between these two currents is known as the **Offset Current** (I_{OS})
* Typical values of I_{OS} ~ **10 nA or so**

- **Closed-Loop**: ***Negative Feedback***:
  - Plethora of applications
    - **Inverting and Non-Inverting Amplifiers**
    - **Summing Amplifier**
    - **Voltage Follower**
    - **Differential** or **Difference Amplifier** (**DA**)
    - **Instrumentation Amplifier**
    - **Level Shifter**
    - **Active Filter** (***Low-Pass***, ***High-Pass***, ***Band-Pass***)
    - **Integrator** and **Differentiator**
    - **Logarithmic** and **Exponential Amplifier**

Inverting Amplifier:

* R_2 provides ***negative feedback***
  - Note that it is connected between the output and the inverting (–) terminal $\Rightarrow$ ***negative feedback***



* V^+ and V^- are the voltages at the non-inverting and inverting terminals of the op-amp, respectively
  - Note that $V^+ = 0,$ since that terminal is ***grounded***
* One very important ***assumption*** in op-amp circuit analysis: $R_i \to \infty \Rightarrow$ input current to the op-amp = 0

$$\Rightarrow i_1 = i_2 \Rightarrow \left(V_i - V^-\right)/R_1 = \left(V^- - V_0\right)/R_2$$

* Also, $V_0 = A_{vOL}\left(V^+ - V^-\right) = -A_{vOL}V^-$

* Thus, the ***closed-loop gain*** (A_{vCL}) can be expressed as:

$$A_{vCL} = \left.\frac{V_0}{V_i}\right|_{closed-loop} = -\left[\frac{R_1}{R_2} + \frac{1}{A_{vOL}}\left(1 + \frac{R_1}{R_2}\right)\right]^{-1} \quad (\textbf{\textit{show}})$$

* The negative sign in front implies that the output voltage is ***exactly out-of-phase*** with the input voltage (i.e., they are ***180° apart***) $\Rightarrow$ **Inverting Amplifier**

* ***Note***: If $A_{vOL} \to \infty,$ then $A_{vCL} \simeq -R_2/R_1$

  $\Rightarrow$ An extremely simple expression results

* Note that the ***closed-loop gain*** is just equal to the ***resistor ratio*** (feedback resistor/input resistor)
* ***Caution***: For this simplification to hold, A_{vOL} should be at least ***100 times*** R_2/R_1 (will produce ***1% error***)
* Lower values of A_{vOL} will correspondingly produce more error in the result
* Thus, blindly using the simplified result without any regard to A_{vOL} is perilous!
* Note also that the resistance ***seen*** by the input V_i is simply equal to R_1 (to be discussed next)

Concept of Virtual Ground & Summing Point Constraint:

* **Valid only when the OA is under negative feedback**
* Due to the ***large open-loop gain*** (A_{vOL}) of the OA, the ***difference*** between the voltages at the inverting and non-inverting terminals is ***vanishingly small***
* Thus, if the non-inverting terminal is grounded (i.e., ***Real Ground***), then the inverting terminal is also assumed to be at ***ground potential***, even though actually it may not be so

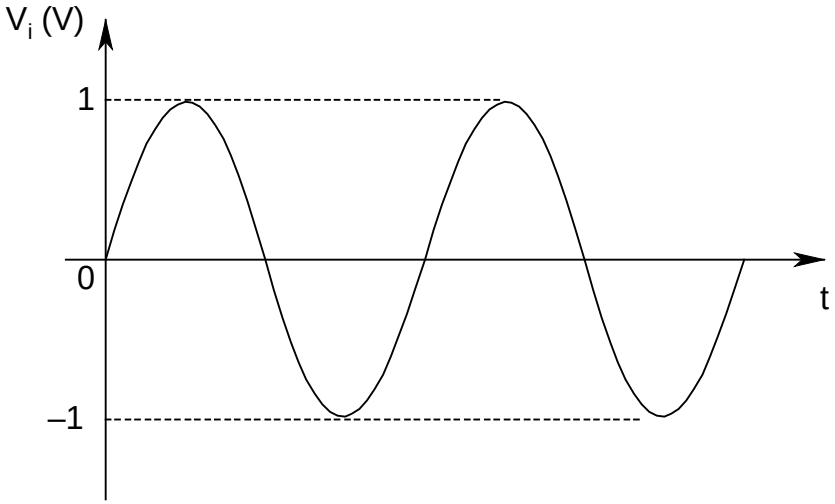
  $\Rightarrow$ Known as ***Virtual Ground*** (to distinguish it from actual ground)

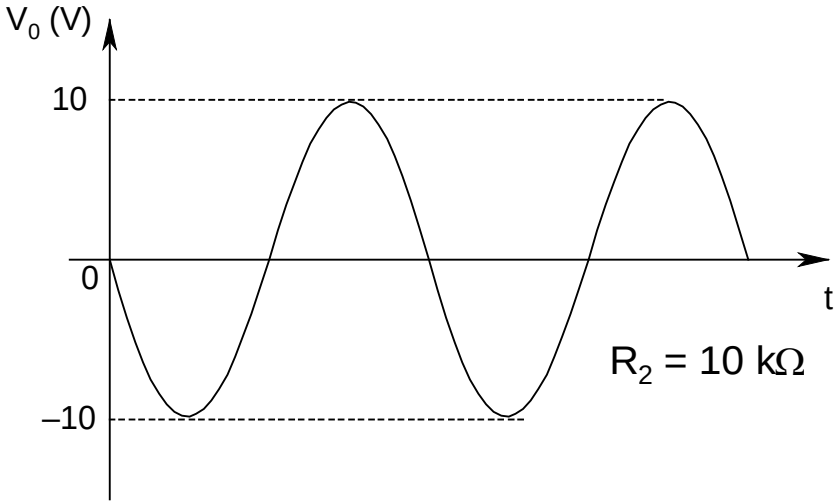
* The assumption that $V^+ = V^-$ as well as $i_1 = i_2 = 0$ is known as the ***Summing Point Constraint***
* These two assumptions make the analysis of OA circuits absolutely trivial
* Extending this argument, we can say that for OAs under negative feedback, the voltages at the inverting and non-inverting terminals always ***track*** each other, such that their difference is zero (almost!)
* ***Caution***: These assumptions are applicable only for OAs under negative feedback, **never apply these assumptions when the OA is under positive feedback**

Important Assumptions for OA Circuit Analysis:

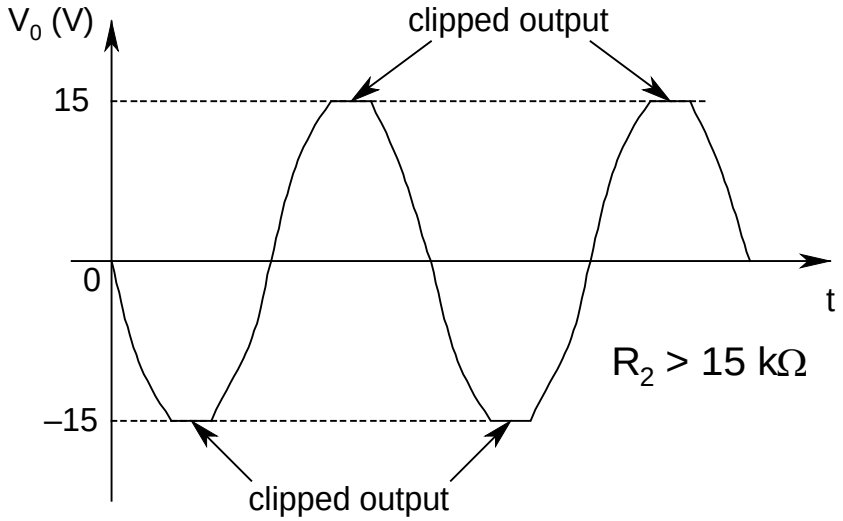
* $R_i \rightarrow \infty \Rightarrow$ Zero input currents to the OA
* $A_{vOL} \rightarrow \infty \Rightarrow$ Summing Point Constraint can be applied at the input terminals under negative feedback
* $R_0 \rightarrow 0 \Rightarrow$ The output behaves like an ***ideal voltage source***
* The OA can source and sink any current, up to the ***maximum permissible limit***, at its output
* **Be very careful while applying KCL at the output terminal of an OA, since the OA may be sourcing or sinking current (which would have opposite signs)**

Limitations : Saturation Voltages :



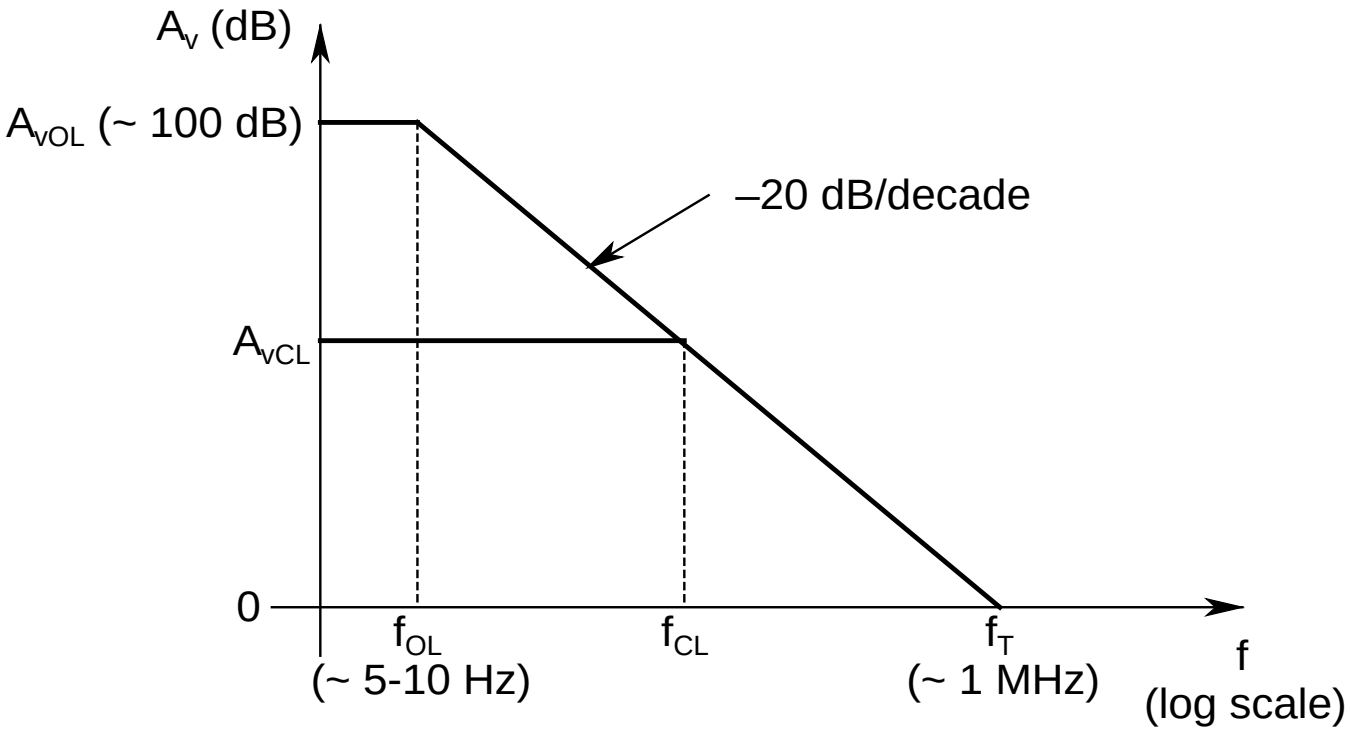


R_1 = 1 kΩ
V_{SAT}+ = 15 V
V_{SAT}– = –15 V



Limitations : Bandwidth (Unity-Gain Cutoff) :

* OAs are ***compensated for stability*** with regard to unwanted oscillations
* Compensation creates a ***pole*** in the frequency response characteristic, typically at about ***5-10 Hz***
* After that, the gain rolls off at ***– 20 dB/decade***
* The frequency at which the magnitude of this gain becomes ***unity*** (i.e., ***0 dB***) is known as the ***unity-gain cutoff frequency*** (f_T)
* ***Relation***: $A_{vOL} \times f_{OL} = A_{vCL} \times f_{CL} = f_T$, where f_{OL} and f_{CL} are the ***open-loop*** and ***closed-loop*** cutoff frequencies



As $A_{vCL}\uparrow$, $f_{CL}\downarrow$, and vice-versa

Limitations : Slew Rate :

* ***Slew Rate*** (SR) is the ***maxuimum*** possible rate of change of the output with respect to time (in V/μsec), which is constant for a given OA, and is typically about ***0.5-2 V/μsec***

* ***Given by***: $SR = \omega_M V_{SAT} = \omega_0 V_0 = \omega_0 |A| V_i$

  where ω_M: ***Full-power bandwidth***: **Maximum possible bandwidth when the output is swinging between $\pm V_{SAT}$**

  ω_0: **Bandwidth when the output is swinging between $\pm V_0$ ($< \pm V_{SAT}$)**

Example :

Let $R_1 = 1\ \text{k}\Omega$, $R_2 = 10\ \text{k}\Omega$, $V_{SAT} = \pm 15$ V, and SR = 1 V/μsec. Find ω_0 for $V_i = 10$ mV, 100 mV, and 1 V.

$$|A| = 10, \quad \therefore \ \omega_0 = \frac{SR}{|A| V_i} = \frac{(1\ \text{V}/\mu\text{sec})}{10 \times V_i}$$

Thus, for V_i = 10 mV, $\omega_0 = 10$ Mrad/sec

= 100 mV, = 1 Mrad/sec

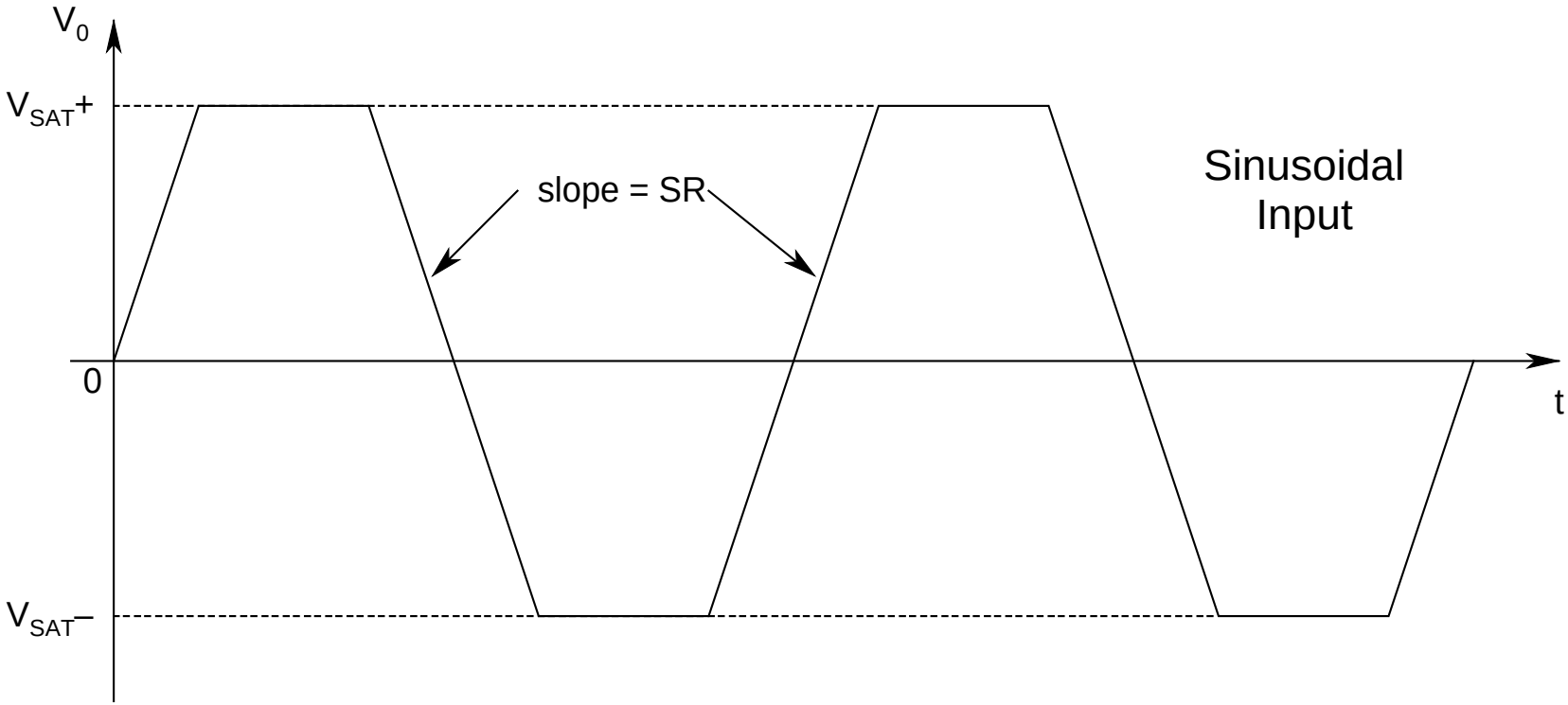
= 1 V, = 100 krad/sec

Note: ω_0 is an inverse function of both gain $(|A|)$ and the input signal amplitude (V_i)

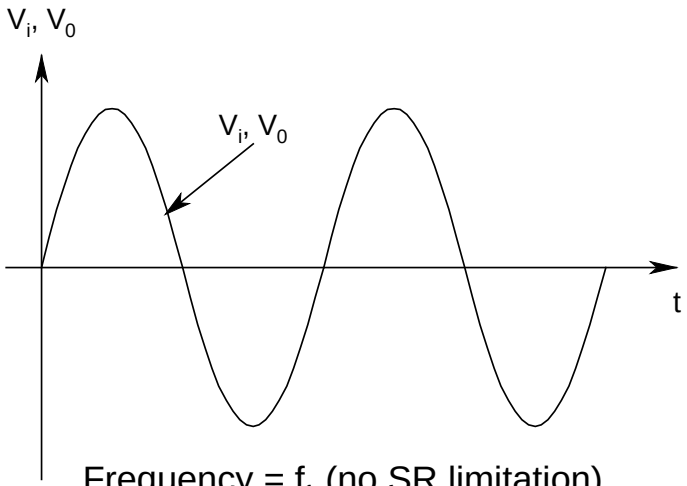
Thus, as $|A|$ and $V_i \uparrow$, $\omega_0 \downarrow$

An Interesting Scenario :

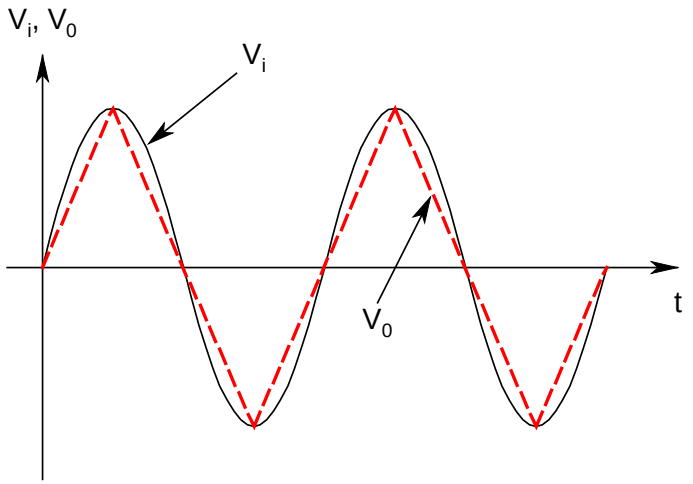
The amplitude and frequency of the sinusoidal input signal is such that the output becomes both saturation voltage and slew rate limited



Dramatic Effect of SR Limitation :

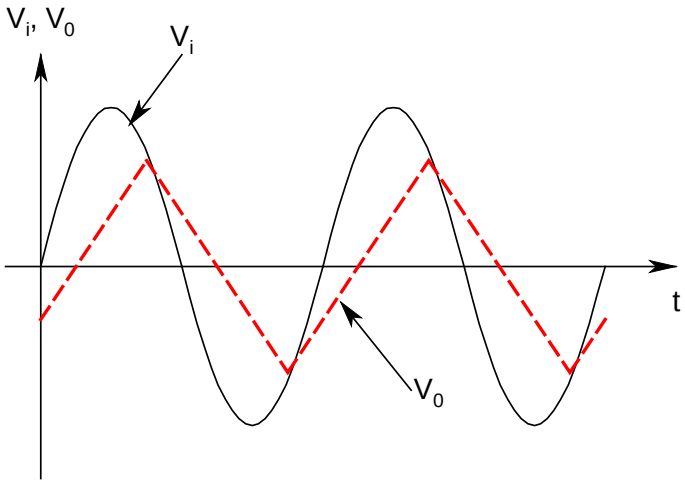


Frequency = f_1 (no SR limitation)



Frequency = f_2 (> f_1) (moderate SR limitation)

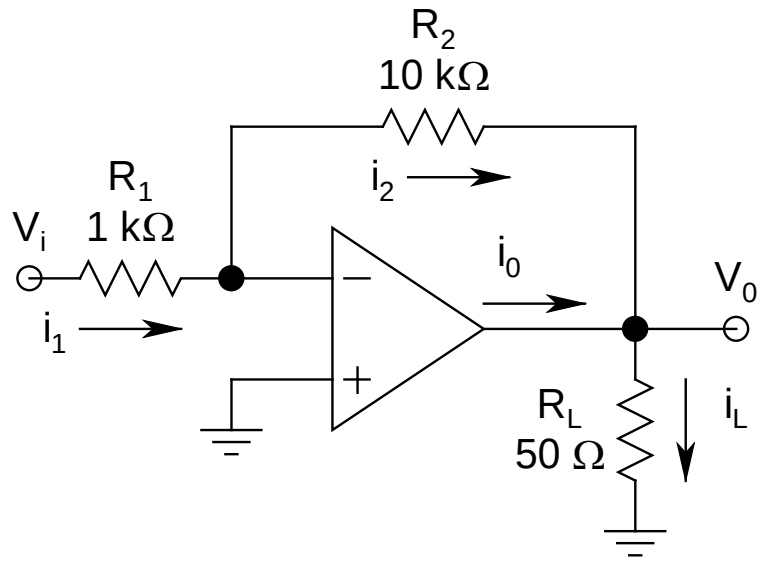
Under unity feedback configuration ((to be discussed later)



Frequency = f_3 (> f_2) (severe SR limitation)

Limitation : Output Current Source/Sink Capability :

* OAs have a limit on the ***maximum current*** $(i_{0,max})$ that they can source or sink
* This puts a ***lower limit*** on the value of the load resistance that it can drive



* Let $V_i = -1\ V \Rightarrow V_0 = +10\ V$ (without R_L)
* ***With R_L***: KCL at the output (***note that V_0 is positive***)

$$-\frac{V_0}{R_2} + i_0(\max) = \frac{V_0}{R_L} \quad (\textbf{\textit{OA has to source current}})$$

* For $i_{0,max} = 25$ mA, $V_0 = 1.24$ V (***note that the nominal value is 10 V***)
* This severe attenuation in the output voltage is caused by the ***limited current drive capability*** of the OA coupled with the small value of R_L
* Thus, there is a minimum value of R_L, beyond which the output will start to attenuate $\Rightarrow$ find this minimum value of R_L for this example (***Ex***.)
* ***Caution***: While using KCL at the output node of an OA: **Always check if the current being sourced/ sunk by the OA is below $i_{0,max}$**

Summing Amplifier (or simply Summer) :

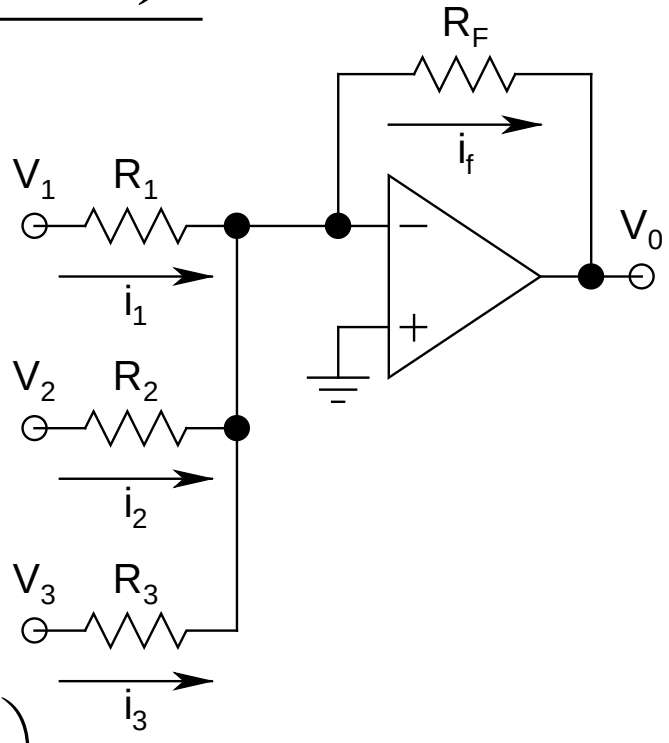
* $i_1 + i_2 + i_3 = i_f$ (***no input current to the OA***)

$$\Rightarrow \frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} = -\frac{V_0}{R_F}$$

(***virtual ground at the inverting terminal***)

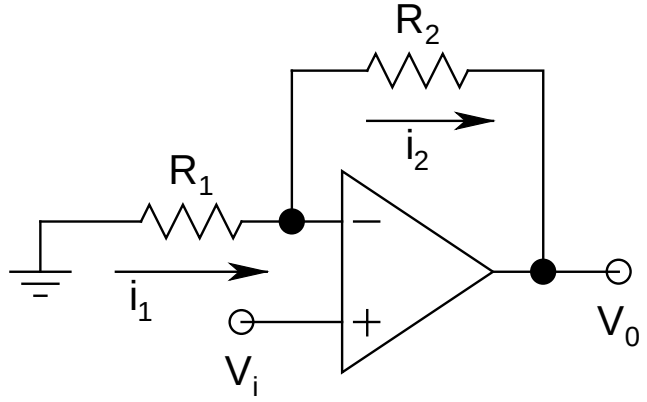
$$\Rightarrow V_0 = -\left(\frac{R_F}{R_1} V_1 + \frac{R_F}{R_2} V_2 + \frac{R_F}{R_3} V_3 \right)$$

$$= -\sum_{i=1}^{n} \left(\frac{R_F}{R_i} V_i \right)$$



* Note that the circuit produces an ***weighted sum*** of the input voltages, with the weighting factor given by R_F/R_i for the i^{th} input
* ***Ex***: If $R_1 = 1\ k\Omega,\ R_2 = 2\ k\Omega,\ R_3 = 5\ k\Omega,$ and $R_F = 10\ k\Omega,$ then $V_0 = -\left(10V_1 + 5V_2 + 2V_3\right)$
* Immensely popular in earlier days of ***analog computers***
* With the advent of ***digital computers***, has lost favor
* All the limitations discussed for inverting amplifier hold for all OA circuits to be discussed, including this one

Non-Inverting Amplifier :



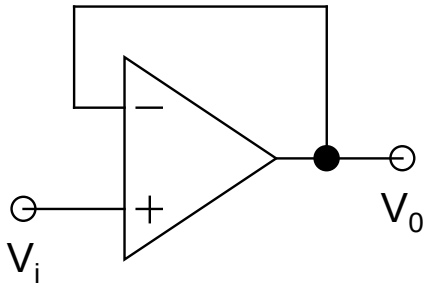
* Note that the feedback is still ***negative*** (output fed back to the ***inverting*** terminal of the OA)
* Input V_i applied to the ***non-inverting*** terminal
* Applying ***summing point constraint***:

$$i_1 = i_2 \Rightarrow -\frac{V_i}{R_1} = \frac{V_i - V_0}{R_2} \Rightarrow A_{vCL} = \frac{V_0}{V_i} = 1 + \frac{R_2}{R_1}$$

* Thus, input and output are ***in phase***, and the magnitude of the voltage gain $\geq 1 \Rightarrow$ ***Non-Inverting Amplifier***
* The input signal source V_i is not ***loaded*** at all by the OA, since the input resistance is ***infinite***

Voltage Follower :

* An interesting application of the ***non-inverting amplifier***
* Put $R_2 = 0$ (***short-circuit***), i.e., connect the output directly to the inverting terminal of the OA
* Then, $A_{vCL} = 1$, irrespective of the value of R_1
* Thus, R_1 can as well be removed (***open-circuit***)
* Resulting circuit is known as ***voltage follower***, since the output follows the input with ***unity gain*** and ***no phase shift***
* This configuration is also known as ***buffer***, with $R_i \to \infty$, $R_0 \to 0$, and $A_v = 1$



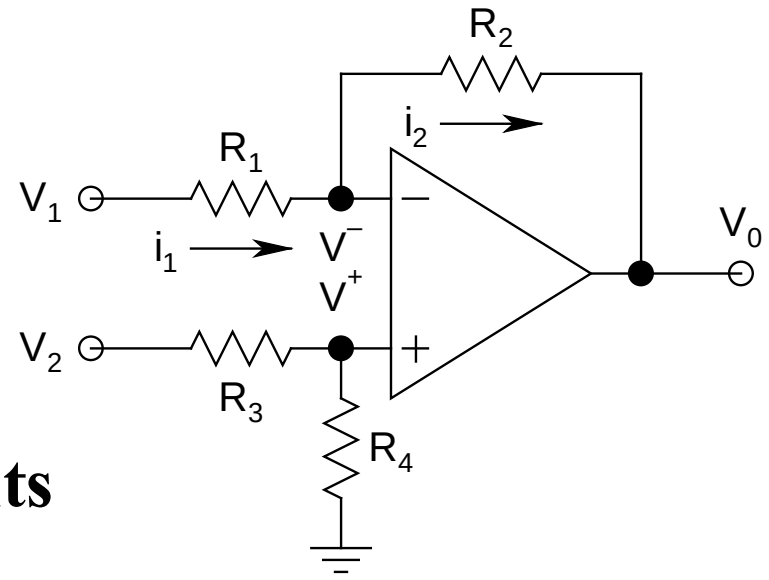
* Frequently used for ***isolation*** between stages
* Another name for this configuration is ***unity feedback configuration***, since the entire output is fed back to the input
* Also, since the ***closed-loop gain is unity***, the ***bandwidth*** of the circuit is equal to f_T (**maximum**)
* Used also for ***impedance matching***, when a ***driver*** circuit having ***high output resistance*** drives a ***load*** having ***low input resistance***

Differential (or Difference) Amplifier (DA) :

* Extremely useful circuit:

  Amplifies the difference between the two input signals, while rejecting signals common to both inputs

  $\Rightarrow$ An excellent ***noise suppressor***



* To analyze this circuit, we apply ***summing point constraint***, which yields $V^+ = V^-$, and input current to the OA = 0

* ***Note***: The circuit has only ***negative feedback***

* $i_1 = i_2 \Rightarrow \dfrac{V_1 - V^-}{R_1} = \dfrac{V^- - V_0}{R_2}$ and $V^+ = \dfrac{R_4}{R_4 + R_3} V_2$

* Thus, $V_0 = -\dfrac{R_2}{R_1} V_1 + \left(1 + \dfrac{R_2}{R_1}\right)\left(\dfrac{R_4/R_3}{1 + R_4/R_3}\right) V_2$

* ***Exercise***: Show that the same result could also have been obtained by applying ***Superposition Principle***

* ***An interesting outcome***: Make $R_2/R_1 = R_4/R_3$

  $\Rightarrow V_0 = \dfrac{R_2}{R_1}(V_2 - V_1) \quad \cdots \quad (1)$

  $\Rightarrow$ A ***perfect differential output***, with ***no common-mode signal present*** there! $\Rightarrow$ **CMRR** $\rightarrow \infty$

* For a ***DA***, the output voltage V_0 is expressed as:

$$V_0 = A_{dm} V_{id} + A_{cm} V_{ic}$$

where

V_{id} = ***differential-mode input voltage*** $= V_2 - V_1$

V_{ic} = ***common-mode input voltage*** $= \left(V_1 + V_2\right)/2$

A_{dm} = ***differential-mode gain***

A_{cm} = ***common-mode gain***

Common-Mode Rejection Ratio:

$$\text{CMRR} \triangleq 20 \log_{10} \left| A_{dm} / A_{cm} \right| \quad (\textbf{\textit{expressed in dB}})$$

* Compare with (1): $A_{dm} = R_2 / R_1$, $A_{cm} = 0$, and

$$\text{CMRR} \rightarrow \infty$$

* It is obvious that if $R_2/R_1 \neq R_4/R_3$, then $A_{cm} \neq 0$, and would result in a ***finite CMRR***
* ***Exercise***: Find A_{dm}, A_{cm}, and CMRR, if $R_2/R_1 = 10$ and $R_4/R_3 = 11$
* Immensely useful circuit, particularly for ***telemetry*** applications
* Differential Amplifier is the heart of another extremely useful block, namely ***Instrumentation Amplifier***

Instrumentation Amplifier :

* Bread-and-Butter Circuit for ***Instrumentation Engineers***
* Used for ***field telemetry applications***, where the points of measurements and processings are far away

  $\Rightarrow$ The signal may get thoroughly ***corrupted by noise*** during transmission, and it becomes extremely ***difficult to extract*** using conventional circuits
* ***Requirements*** of such a circuit:
  - Should have ***extremely high input resistance***, so that the ***measuring instrument does not load the signal***
  - Should have ***perfect impedance matching***

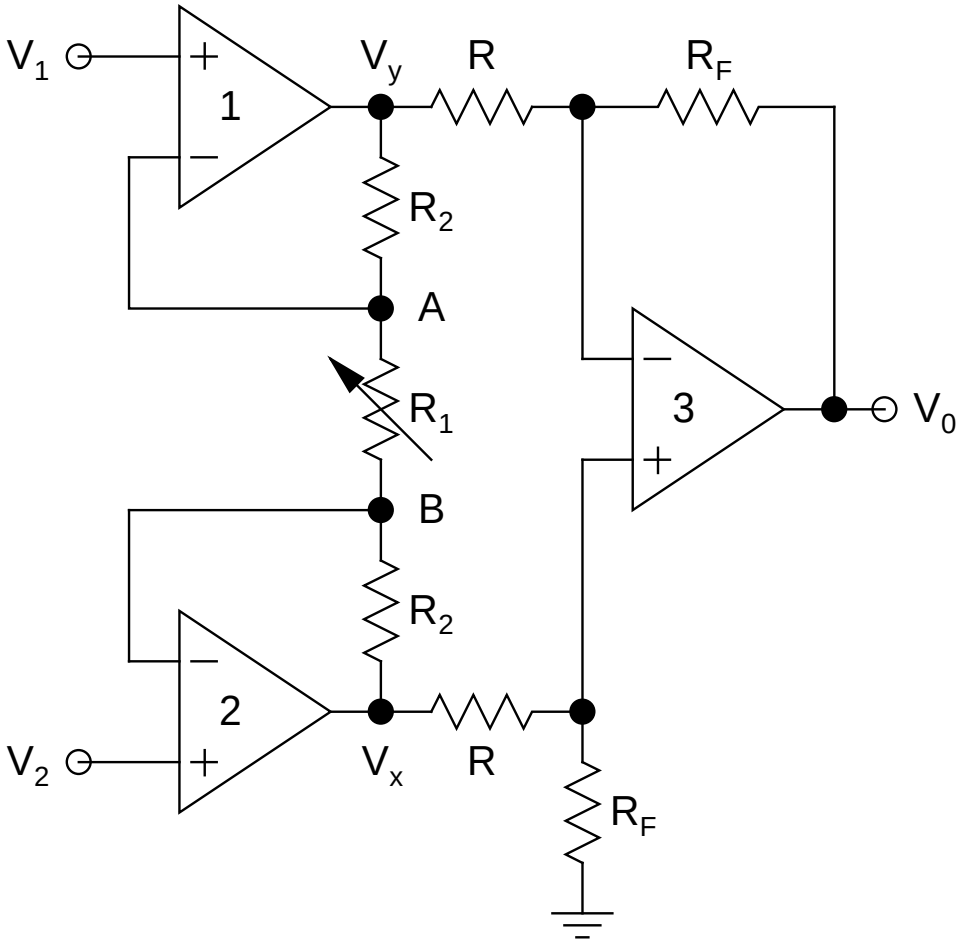
- Should have ***extremely high*** A_{dm} and ***very small*** A_{cm} **(ideally zero)**

  $\Rightarrow$ An ***extremely large CMRR*** is a necessity to ***suppress noise***

* ***Simplest circuit solution***:

- Precede a ***DA*** (having ***high*** A_{dm} ***and CMRR***) by a ***buffer*** (having ***high*** R_i providing ***perfect impedance matching***)

* Resulted in the ***Instrumentation Amplifier***



Instrumentation Amplifier

* ***Note***: OAs 1 and 2 are ***buffers***, while OA 3 is a ***DA***
* Both 1 and 2 have ***negative feedback***, thus we can apply the ***summing point constraint*** for both of them
* Thus, **voltages at nodes A and B are equal to the input voltages V_1 and V_2**, respectively
* Also, since OAs 1 and 2 do not draw any input current,
  $\therefore$ the current through the branch R_2-R_1-R_2 is the same
* Thus, V_x and V_y can be immediately expressed in terms of V_1 and V_2

* Note that the input resistance seen by the inputs V_1 and V_2 is ***infinitely large***, thus the circuit does not cause any ***loading*** of the input signal

* OA3 being a simple ***DA***, the output voltage V_0 can be easily expressed as:

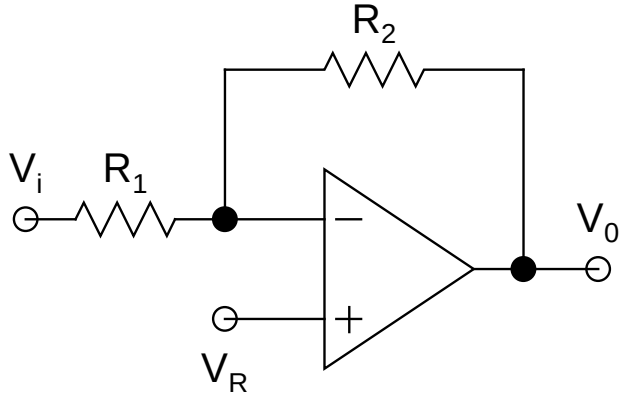
$$V_0 = \frac{R_F}{R}\left(V_x - V_y\right) = \frac{R_F}{R}\left(1 + \frac{2R_2}{R_1}\right)\left(V_2 - V_1\right)$$

where V_x and V_y have been expressed in terms of V_1 and V_2 (***Exercise***: Prove this expression for V_0)

* Note that the ***voltage gain*** of the first stage (i.e., the buffer stage) is $\left(1+2R_2/R_1\right)$
* Generally, R_1 is kept ***variable***, so that the gain of the circuit can be ***adjusted***

  $\Rightarrow$ R_1 is known as the ***gain resistor***
* Extremely useful circuit, and instrumentation engineers can't live without it!
* Note that resistors have ***tolerance***, thus, even though the ideal expression for V_0 indicates ***infinite CMRR***, in actual situations, the ***CMRR would be finite, but large***

Level Shifter:



* ***Adds DC offset to a time-varying signal***
* Circuit resembles an ***inverting amplifier***, with a ***reference voltage*** V_R applied at the ***non-inverting terminal***
* ***Negative feedback*** present in the circuit can be easily identified $\Rightarrow$ ***summing point constraint*** can be applied $\Rightarrow$ the voltage at the inverting terminal is also V_R

* Thus, $V_0 = -\frac{R_2}{R_1} V_i + \left(1 + \frac{R_2}{R_1}\right) V_R$ (***by superposition***)

* The magnitude of the ***DC offset***, amounting to $\left(1 + R_2/R_1\right) V_R$, can be easily identified from the above expression

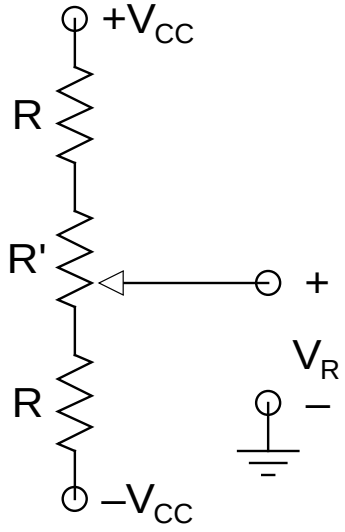
* Note also that the ***sign*** of the DC offset can be changed by changing the ***sign*** of V_R

* For a specific requirement of the ***DC offset***, either the ***resistor ratio*** $\left(R_2/R_1\right)$ or the ***reference voltage*** $\left(V_R\right)$ or ***both*** can be changed

For Continuously Varying V_R:

* Uses two fixed value resistors (R) and a ***potentiometer*** (R')
* Biased using dual power supply $\pm V_{CC}$: the same supply that powers the OA
* The range of V_R (***Exercise***: Prove it):

$$-\frac{V_{CC}R'}{2R+R'} \le V_R \le +\frac{V_{CC}R'}{2R+R'}$$

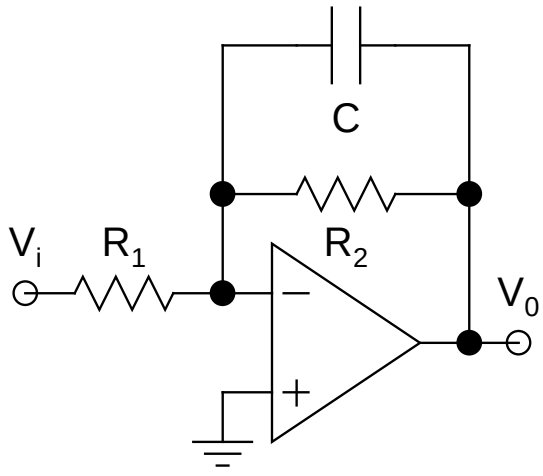


* For ***higher resolution***, use potentiometer with ***higher number of turns*** $\Rightarrow$ ***CROs*** use this technique to add ***DC offset*** to a signal

Active Filters:

* We have already seen ***passive filters*** using resistors, inductors, and capacitors
* ***Passive filters*** are **incapable of producing voltage gain** (the gain is always ≤ 1)
* Filters can also be constructed using OAs, which **can provide for voltage gain**
  - $\Rightarrow$ Known as ***Active Filters***
  - $\Rightarrow$ Can design ***LPF***, ***HPF***, and ***BPF*** using OAs

LPF:



* First note that the OA is under ***negative feedback***, ∴ ***virtual ground concept*** can be applied
* Thus, the circuit is simply an ***inverting amplifier***, with a **capacitor C in parallel with a resistor R_2** in **the feedback branch**
* ***Resistor R_2 is necessary***, ∵ without it, the OA won't have any **DC feedback path**, and will go under ***open-loop***, with output ***saturating to*** $\pm V_{SAT}$

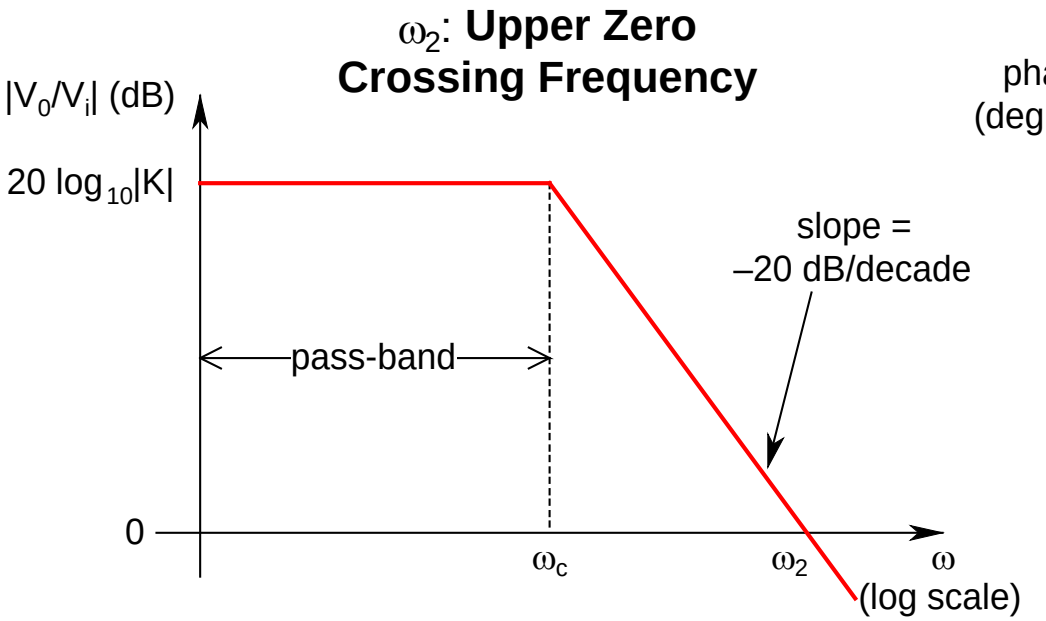
* Impedance of parallel combination of R_2 and C:

$$Z = R_2 \| \left(\frac{1}{j\omega C} \right) = \frac{R_2}{1 + j\omega R_2 C}$$

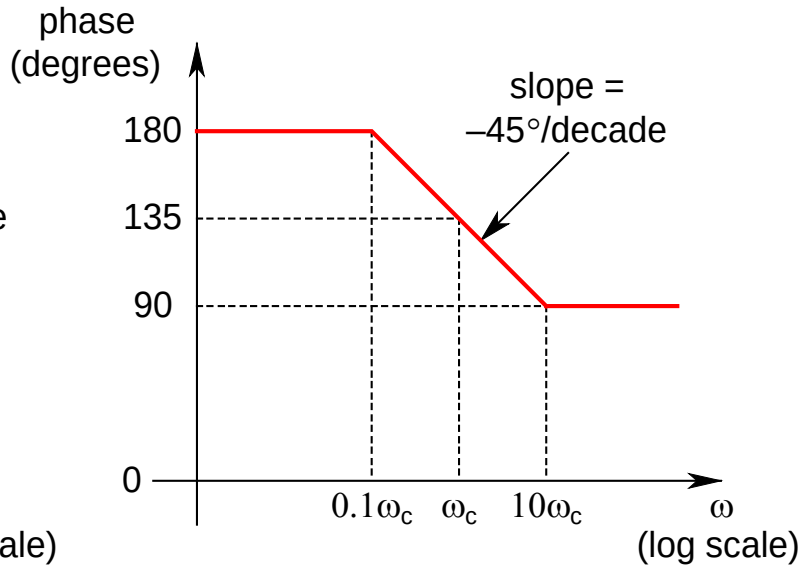
* Thus, $\frac{V_0}{V_i} = -\frac{Z}{R_1} = -\frac{R_2/R_1}{1 + j\omega R_2 C} = \frac{K}{1 + j\omega/\omega_c}$

  - $K \left(= -R_2/R_1\right)$ is the ***low-frequency*** (or ***pass-band***) ***gain***, with the negative sign implying ***180° phase shift*** between input and output
  - $\omega_c \left[= 1/\left(R_2 C\right)\right]$ is the ***upper cutoff frequency***

* From the transfer function, ***LPF*** behavior is obvious



Asymptotic Gain Plot



Asymptotic Phase Plot

* ***Note***: Gain controlled by R_1 and R_2, while cutoff frequency controlled by C $\Rightarrow$ tremendous flexibility
* Also known as a ***first-order filter***, since the transfer function has only a ***single pole***

* Note that the transfer function has a ***single pole*** at ω_c

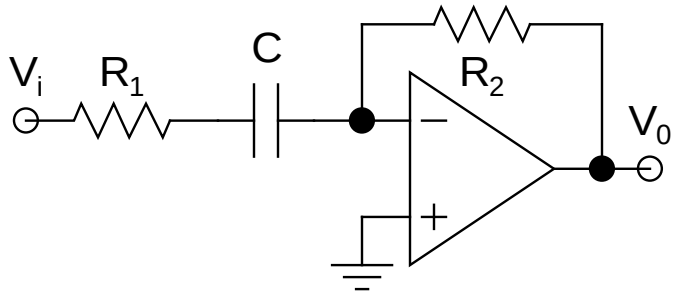
  $\Rightarrow$ The gain stays ***constant*** at $20\log_{10}|K|$ till ω_c,

  and then ***drops*** @ 20 dB/decade

* For ***very low frequency*** $(\omega \to 0)$, the phase angle of the output is $180°$ (or, equivalently, $-180°$) (due to the presence of the ***negative sign*** in front of the transfer function) till $0.1\omega_c$, and then starts to ***drop*** @$45°$/decade till $10\omega_c$, resulting in a ***final*** phase of $90°$ (or, equivalently, $-270°$) as $\omega \to \infty$

HPF:

* Only difference from LPF is that C is taken off from the feedback branch and put in the input branch



* Impedance of the series combination of R_1 and C:

$$Z_1 = R_1 + \frac{1}{j\omega C} = \frac{1 + j\omega R_1 C}{j\omega C}$$

* Thus, $\dfrac{V_0}{V_i} = -\dfrac{R_2}{Z_1} = -\dfrac{j\omega R_2 C}{1 + j\omega R_1 C} = -\dfrac{j\omega/\omega_1}{1 + j\omega/\omega_c}$

$\omega_1 \left[= 1/\left(R_2 C\right)\right]$ is the ***lower zero crossing frequency***

$\omega_c \left[= 1/\left(R_1 C\right)\right]$ is the ***lower cutoff frequency***

* ***Note***: As $\omega \to 0$, $\left|V_0/V_i\right| \to 0$; and as $\omega \to \infty$,

  $\left|V_0/V_i\right| \to \omega_c/\omega_1 = R_2/R_1$ (constant)

  $\Rightarrow$ ***HPF*** behavior established

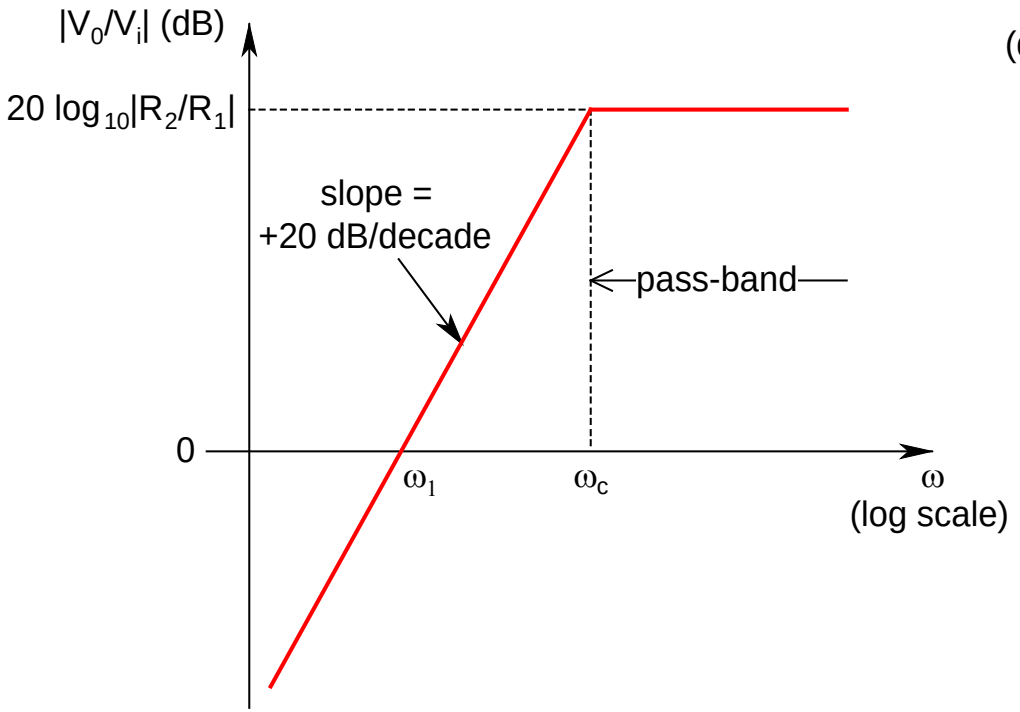
* $\left|\textbf{\textit{Pass-Band Gain}}\right| = \omega_c/\omega_1 = R_2/R_1$

  $\Rightarrow$ For large pass-band gain, R_2/R_1 should be large

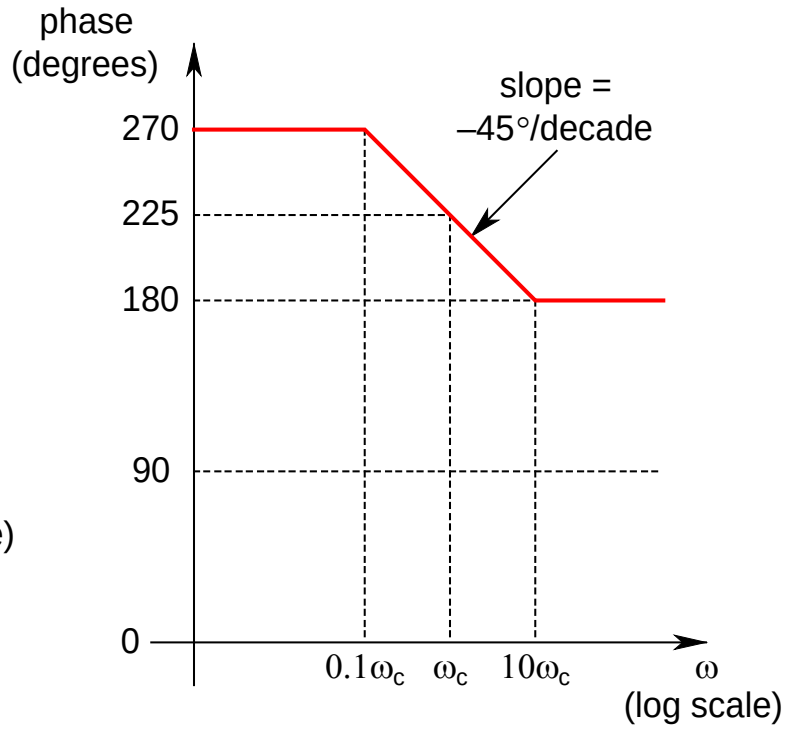
  $\Rightarrow$ R_2 should be much larger than R_1

  $\Rightarrow$ $\boldsymbol{\omega_1 \ll \omega_c}$

* ω_1 is known as ***lower zero crossing frequency***, since at this frequency $\left|V_0/V_i\right|$ = 1 (0 dB), and then ***increases*** @ 20 dB/decade till ω_c, after which it becomes ***constant***



Asymptotic Gain Plot



Asymptotic Phase Plot

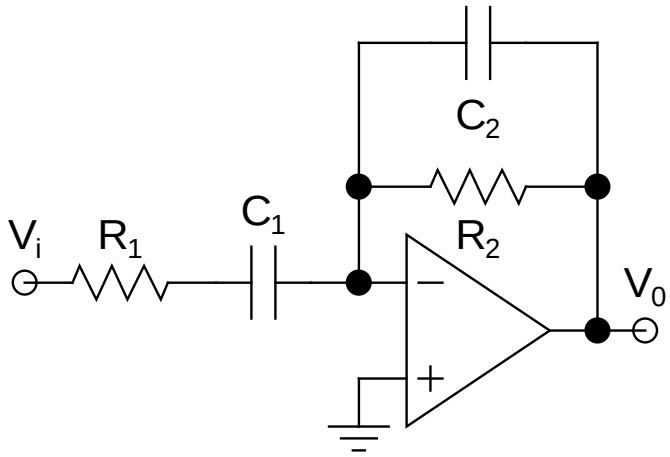
* ***Note***: As $\omega \rightarrow 0$, phase = 180° (due to the negative sign in front of the transfer function) + 90° (constant phase contributed by ω_1) = 270°

BPF:

* **Combination of LPF and HPF**: ***R_1-C_1 creates lower cutoff*** (for ***HPF***), and ***R_2-C_2 creates upper cutoff*** (for ***LPF***)

* Impedance of series combination of R_1 and C_1:

$$Z_1 = R_1 + \frac{1}{j\omega C_1} = \frac{1 + j\omega R_1 C_1}{j\omega C_1}$$



* Impedance of parallel combination of R_2 and C_2:

$$Z_2 = R_2 \,||\left(\frac{1}{j\omega C_2}\right) = \frac{R_2}{1 + j\omega R_2 C_2}$$

* Thus, $\dfrac{V_0}{V_i} = -\dfrac{Z_2}{Z_1} = -\dfrac{j\omega R_2 C_1}{\left(1+j\omega R_1 C_1\right)\left(1+j\omega R_2 C_2\right)}$

$$= -\frac{j\omega/\omega_1}{\left(1+j\omega/\omega_L\right)\left(1+j\omega/\omega_H\right)}$$

$\omega_1\left[=\ 1/\left(R_2C_1\right)\right]$ is the ***lower zero crossing frequency***

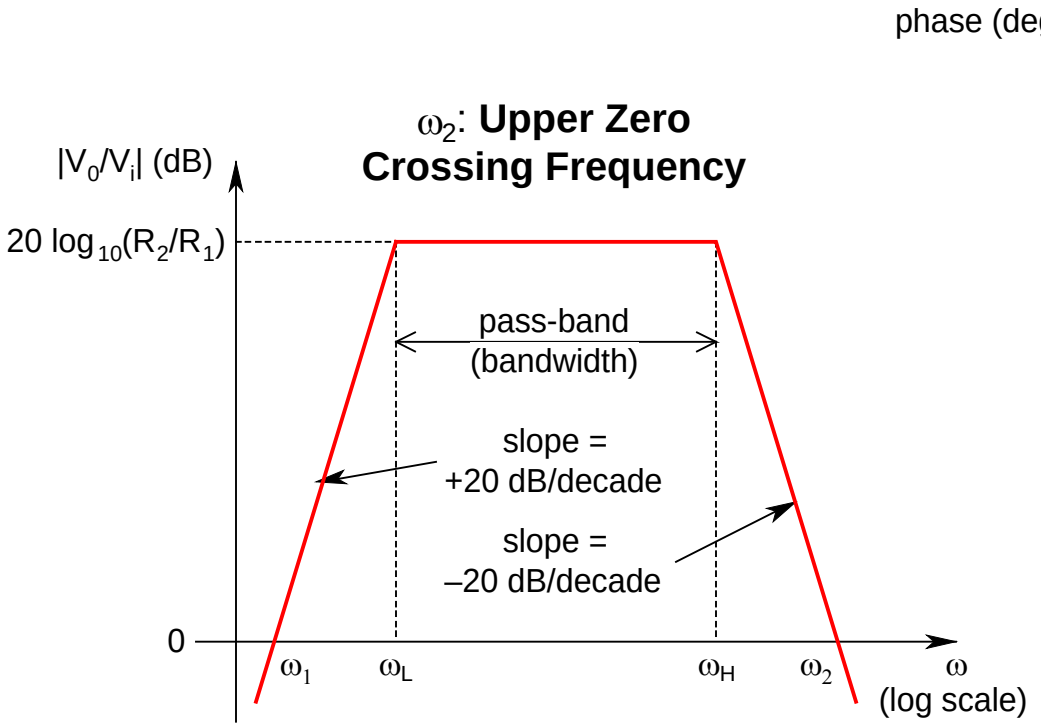
$\omega_L\left[=\ 1/\left(R_1C_1\right)\right]$ is the ***lower cutoff frequency*** **(for HPF)**

$\omega_H\left[=\ 1/\left(R_2C_2\right)\right]$ is the ***upper cutoff frequency*** **(for LPF)**

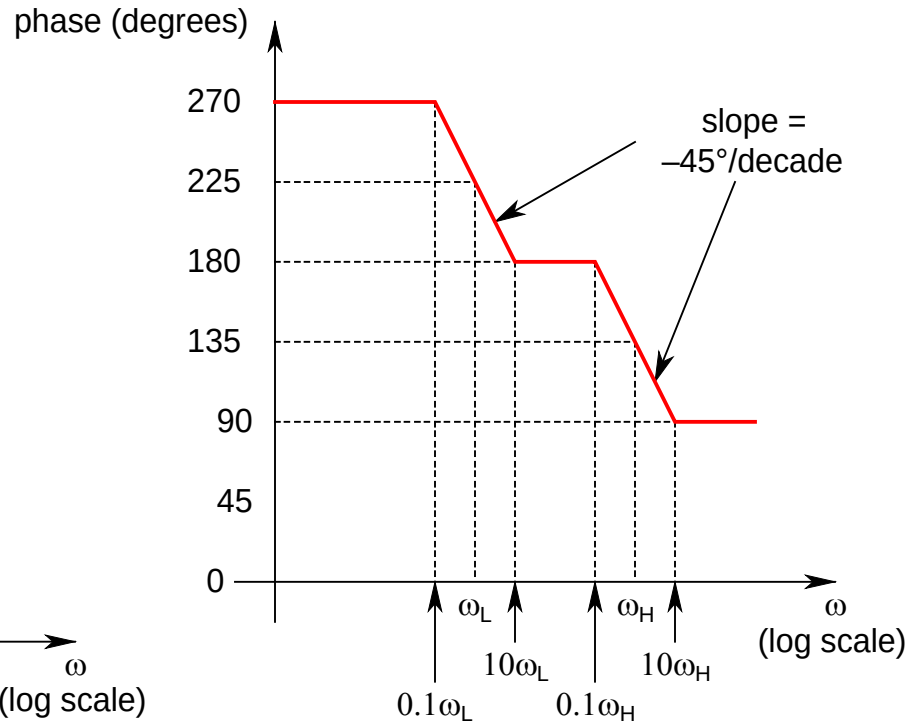
* ***Pass-Band*** $= \omega_H - \omega_L$

* $\left|\textbf{\textit{Pass-Band Gain}}\right| = R_2/R_1,$ thus for large pass-band gain,

$R_2 \gg R_1 \Rightarrow C_2 \ll C_1$ ($\because\ \omega_H > \omega_L$ and $\omega_1 \ll \omega_L$)



Asymptotic Gain Plot



Asymptotic Phase Plot

* In plotting the phase, it is assumed that $\omega_H > 100\omega_L$
* Note that the phase ranges between $\pm 90°$, **characteristic of a BPF**

Design Problem: Pass-band gain = 40 dB, lower cutoff frequency = 200 Hz, bandwidth = 800 Hz.

Choose $R_1 = 1\ k\Omega$, pass-band gain = 40 dB = 100

$\Rightarrow\ R_2 = 100\ k\Omega$

$f_L = 200\ Hz = 1/(2\pi R_1 C_1) \Rightarrow C_1 = 0.8\ \mu F$

Bandwidth = 800 Hz $\Rightarrow\ f_H = f_L + BW = 1\ kHz$

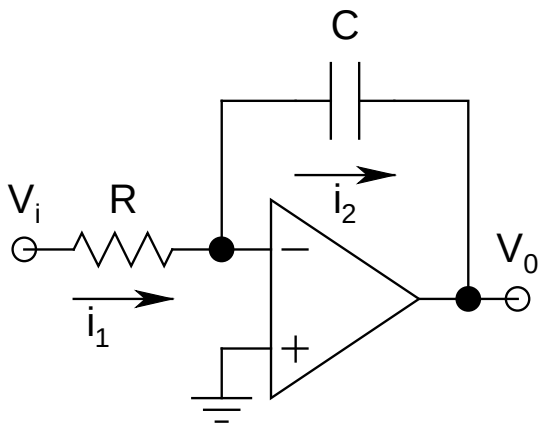
$= 1/(2\pi R_2 C_2) \Rightarrow C_2 = 1.6\ nF$ (***Note***: $\ll C_1$)

$f_1 = 2$ decades below $f_L = 2\ Hz$

$f_2 = 2$ decades above $f_H = 100\ kHz$

Check: $f_1 = 1/(2\pi R_2 C_1) = 2\ Hz$ (checked!)

Integrator:



* ***Time-domain application***: output an ***integrated*** version of input
* Looks exactly similar to an ***LPF***: note that **the function performed by an LPF in frequency- domain is exactly the same as that done by an integrator in time- domain**
* Identifying ***negative feedback*** and applying ***virtual ground*** concept:

$$i_1 = i_2 \Rightarrow \frac{V_i}{R} = -C\frac{dV_0}{dt}$$

$$\Rightarrow\ V_0 = -\frac{1}{RC}\int V_i dt = -\frac{1}{\tau}\int_0^t V_i dt + V_0(0)$$

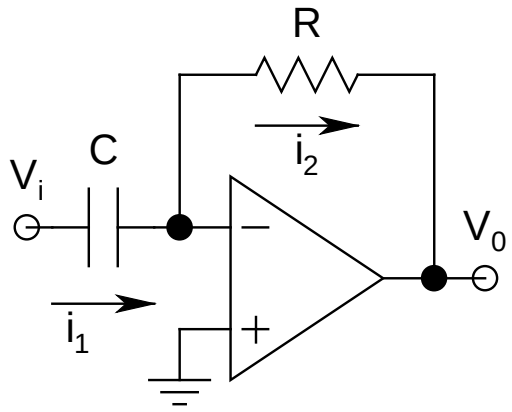
- τ (= RC) is the ***time constant of integration***
- $V_0(0)$ is the initial value of V_0 at t = 0

* Thus, if V_i is a ***square pulse***, V_0 will be ***triangular***; and for ***triangular*** V_i, V_0 will be ***parabolic***, etc.

* Practical integrators would have a resistor R_2 shunting the capacitor C in the feedback path to prevent any ***open-loop*** condition of the OA, which would ***saturate*** the output at $\pm V_{SAT}$

* ***Caution***: The time constant R_2C created by this additional resistor should in no way ***affect*** the integration time constant τ (= RC)
* This makes the design of a practical integrator little ***tricky***
* Also, the capacitor needs to be ***discharged*** periodically to prevent any undesirable accumulation of charges in it
* Used sparingly

Differentiator:



* Another ***time-domain application***: output a ***differentiated*** version of input
* Looks exactly similar to an ***HPF***: **note that the function performed by an HPF in frequency- domain is exactly the same as that done by a differentiator in time- domain**
* Identifying ***negative feedback*** and applying ***virtual ground*** concept:

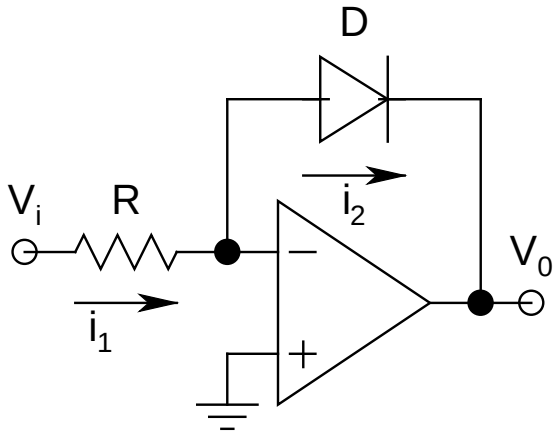
$$i_1 = i_2 \Rightarrow C\frac{dV_i}{dt} = -\frac{V_0}{R}$$

$$\Rightarrow\ V_0 = -RC\frac{dV_i}{dt} = -\tau\frac{dV_i}{dt}$$

τ (= RC) is the ***time constant of differentiation***

* Thus, a ***triangular*** input will produce a ***square wave*** output, etc.
* This circuit also is rarely used since it tends to ***amplify*** the noise present at the input (note that the ***derivative of a noise spike can be dangerously large***!)
* Occasionally used for ***waveshaping***

Logarithmic Amplifier:



* Output ***logarithmic*** function of input
* ***Non-linear*** application due to the presence of a ***non-linear*** element (diode D) in the feedback path
* This circuit is a little complicated, since the feedback path gets ***broken*** when the diode becomes ***reverse biased*** and the output saturates to V_{SAT^+}
* However, when the diode is ***forward biased***, then the feedback path is ***maintained***, with the diode voltage equal to $-V_0$ (due to ***virtual ground***)

* Note that under this condition, ***negative feedback*** is maintained and ***virtual ground*** concept can be applied

$$\Rightarrow i_2 = I_S\left[\exp\left(-\frac{V_0}{V_T}\right)-1\right]$$

I_S: ***Reverse Saturation Current*** of diode

V_T: ***Thermal Voltage*** (26 mV at T = 300 K)

$$\Rightarrow i_1 = i_2 \Rightarrow \frac{V_i}{R} = I_S\left[\exp\left(-\frac{V_0}{V_T}\right)-1\right]$$

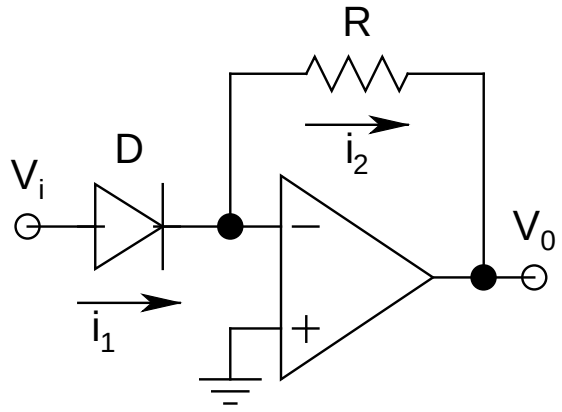
$$\Rightarrow V_0 = -V_T \ln\left[\left(\frac{V_i}{I_S R}\right)+1\right] \qquad \cdots \qquad (1)$$

Observations:

* For $V_i = 0$, $V_0 = 0$, i.e., the VTC passes through ***origin***
* For ***positive*** V_i, a current equal to V_i / R will flow through R, and the same current would flow through D as well, thus developing an output voltage V_0, given by (1)
* For $V_i \gg I_S R$, then the -1 term in (1) can be neglected, and V_0 becomes a ***true logarithmic function*** of V_i

* Note that the ***maximum*** output voltage can only be equal to the ***negative of diode voltage***, which typically ranges between ***0 to about 1V*** (for Si diodes)
* Note that due to the logarithmic dependence of V_0 on V_i, a ***large change in V_i can be compressed to a small change in V_0***
* For ***negative*** V_i, the diode becomes ***reverse biased***, the feedback path gets ***broken***, the OA becomes ***open-loop***, the inverting terminal acquires a ***finite*** negative voltage, and ***V_0 swings to V_{SAT^+}***

Exponential Amplifier:



* **Dual of Logarithmic Amplifier**
* Note that the ***negative*** feedback path is always maintained through the resistor R (***virtual ground applicable***)
* Note also that so long as the diode remains ***reverse biased***, the input signal V_i can't reach the OA terminal, and V_0 ***would be zero***
* Thus, for all ***negative*** V_i, $V_0 = 0$
* For ***positive*** V_i, the diode becomes ***forward biased***
* **Note the limited positive range of V_i**

* Thus,

$$i_1 = i_2 \Rightarrow I_S\left[\exp\left(\frac{V_i}{V_T}\right)-1\right] = -\frac{V_0}{R}$$

which gives:

$$V_0 = -I_S R\left[\exp\left(\frac{V_i}{V_T}\right)-1\right]$$

* For $V_i > 4V_T$, which is about 100 mV at room temperature, the -1 term can be neglected, and the output becomes a ***true exponential function*** of the input

* Note that the role of this circuit is exactly ***opposite*** to that of the logarithmic amplifier:
  - While the **logarithmic amplifier** ***compresses*** a ***large change*** in the input voltage into a ***small variation*** of the output voltage, the **exponential amplifier**, on the other hand, ***expands*** a ***very small range*** of the input voltage into a ***very large range*** of the output voltage

* ***Caution***: Due to the ***exponential*** dependence of V_0 on V_i, with an increase in V_i, V_0 would increase ***rapidly***, and the output may get ***saturated*** at V_{SAT^-} pretty quickly

  $\Rightarrow$ Puts an ***upper limit*** on V_i for fidelity in operation