

Crossover Distortion

➤ **Crossover Distortion:**

- **Quantified by ϕ** (refer to the diagram)
- **Expressed as:**

$$\phi = \sin^{-1}(V_\gamma / V_M)$$

V_M : **Amplitude of the input signal**

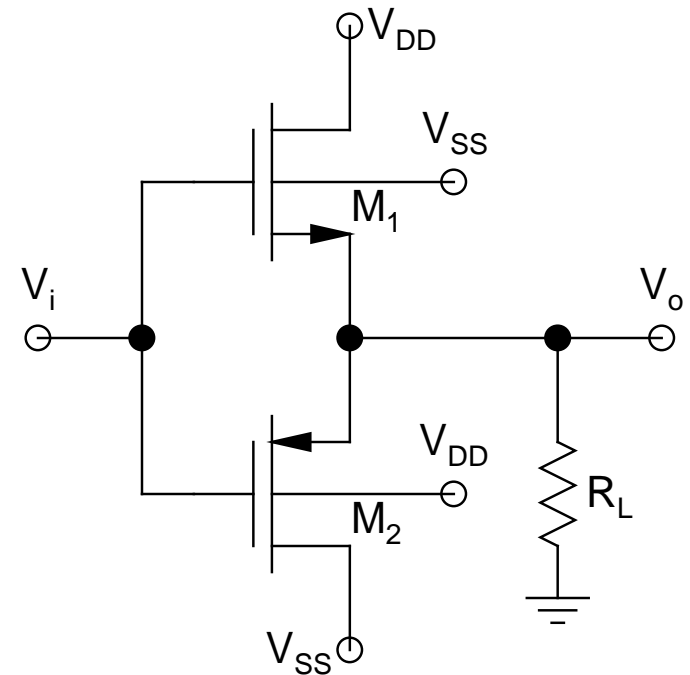
- **Appears four times over a complete cycle**
- **Parameterized** by a term known as the **Total Crossover Distortion (TCD)**, **expressed in percent:**

$$TCD = (2\phi / \pi) \times 100\%$$

- **This distortion becomes more acute as $V_M \downarrow$**
- **For $V_M \leq V_\gamma$, no output** ($V_o = 0$ always)

- ***MOS Implementation:***

- *Working principle absolutely similar to BJT implementation*
- *Only exception that V_γ replaced by V_{TN} and V_{TP}*
- ***Q-point:*** $V_i = V_o = 0$
- *Both devices suffer from body effect issue*



Circuit Schematic

- V_{TN} and V_{TP} function of V_o
 - ⇒ VTC significantly nonlinear
 - ⇒ Output shows more distortion
- V_i can't be more than V_{DD} or less than V_{SS}
 - ⇒ V_o can't have rail-to-rail swing
- Also, MOS devices are *inherently much poorer* than their BJT counterparts in terms of *current carrying capability*
 - ⇒ *Makes this stage quite a poor choice*
(needs extremely large W/L ratios)

- *Class AB Push-Pull Output Stage:*

- In a *Class B* stage, *Crossover Distortion* arises because the transistors are *absolutely cold* in the *standby state*, i.e., *dead off*
- If instead, these are *prebiased* at the *verge of conduction*, *but not quite turned on*, then a *slight swing* of the *input either way* can make *one of these transistors turn on* and *either supply current to the load* or *pull current away from the load*
- *This is the whole idea behind a Class AB stage*

- *Either of the output transistors remain on for complete half cycles*
- Thus, it's a *mixture of Class A and Class B operation*
- Hence, it's called *Class AB Push-Pull Stage*
- *Eliminates Crossover Distortion completely*
- *Obvious fallout:*
 - *Dissipation of standby power*
- *Extremely popular topology and widely used*
- *Efficiency drops slightly as compared to a pure Class B stage*

- **BJT Implementation:**

- *Needs additional circuitry*

(I_Q - Q_3 - Q_4)

- Q_3 - Q_4 *diode-connected*

transistors and both

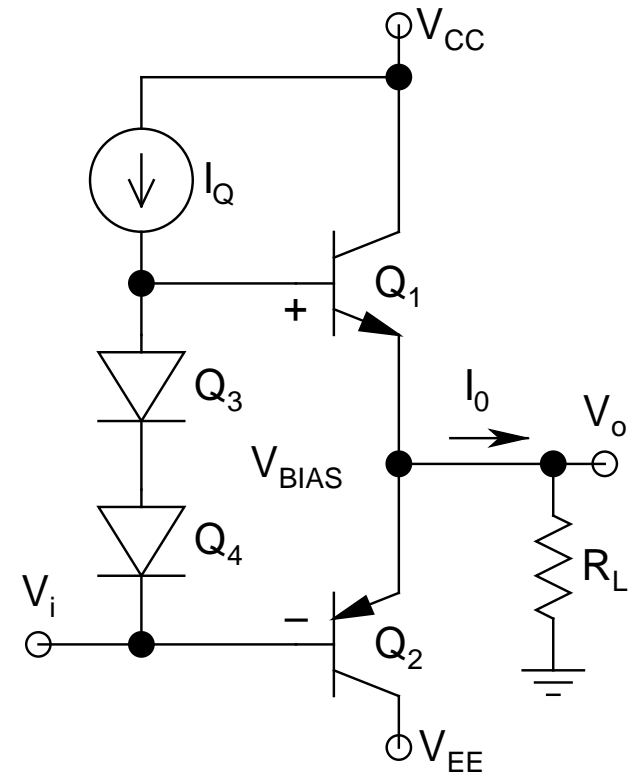
are *biased by the same*

current I_Q

- This produces a *DC bias*

V_{BIAS} between the *bases*

of Q_1 - Q_2



Circuit Schematic