OUTPUT STAGES

- ***Main Purpose***:
  - ***To drive load with sufficient current***
- Both ***BJT*** and ***MOS*** output stages available
- ***BJT*** output stages preferred due to their ***large current handling capability***
- ***BiMOS*** circuits use ***MOS*** devices in the ***core*** of the circuit, while using ***BJT*** devices in the ***output*** stage
  - ***Best of both worlds***!

- ***Requirements***:
  - ***Sufficient drive current/power transfer to load***
  - ***Low output distortion***
  - ***Ideal voltage source***:
    - ***Thevenin equivalent***: V_0 ***with*** $R_0 \rightarrow 0$
  - ***Voltage gain*** A_v ***independent of load***
    - ***Ideally unity with no phase shift***
  - ***Low Standby*** (or ***Idling***) ***Power***
    - ***While not driving any load***
  - ***Should not degrade frequency response***

- ***High power conversion efficiency η***
  - η = (*average power delivered to load*)/(*average power drawn from supply*)

- ***Classification***:
  - ***Depends on the conduction angle*** (θ)
    - θ: ***Angle over the complete cycle (360°) for which either both or one of the output transistors are/is on***
  - ***Class A***:
    - $\theta = 360°$ and $\eta_{max} = 25\%$ (***large standby power***)
  - ***Class B***:
    - θ ***slightly less than*** $180°$ and $\eta_{max} = 78.5\%$ (***zero standby power***)

- ***Class AB***:
  - $\theta = 180°$ and $\eta_{max} \approx 78.5\%$ (***very small standby power***)
- ***Class C***:
  - $\theta << 180°$ (***used in RF applications***)
- There are ***other classes*** also, namely ***D***, ***E***, ***F***, ***G***, and ***H***
  - Used only in ***special cases***, e.g., ***pulse width modulated input***, ***lowering of distortion***, etc.
- In this course, we shall be discussing only about ***Class B*** and ***Class AB*** output stages

- ***Class B***:
  - Uses ***complementary*** set of output transistors (***npn and pnp***, ***NMOS and PMOS***)
  - One takes care of the ***positive half cycle***, while the other takes care of the ***negative half cycle***
  - ***θ slightly less than 180° for each***
  - ***Both output devices never ON simultaneously***
    - ***Zero standby power*** (***significant advantage***)
  - Also known as ***Push-Pull Stage***

- During ***positive half cycle***, the stage ***pushes current through load***
- During ***negative half cycle***, the stage ***pulls current away from load***
- ***Very high η_{max} of 78.5%***
- However, there is a ***very big limitation***, known as ***Crossover Distortion***
  - Also known as ***Deadband Distortion***
  - ***Occurs during zero crossings of the signal***
  - ***For BJT/MOS Class B stage***, the ***input voltage must at least equal V_γ (~ 0.6 V)/V_{TN}($|V_{TP}|$) (~ 0.7-1 V)*** for the ***output stage transistors to turn on***

- ***Class AB***:
  - ***Eliminates Crossover Distortion*** by ***prebiasing the output transistors***
    - ***They remain at the verge of conduction in the standby stage***
  - ***θ exactly equal to 180°***
  - ***η_{max} slightly less than 78.5%*** due to a ***small amount of standby power***
  - ***Extremely popular and most widely used***

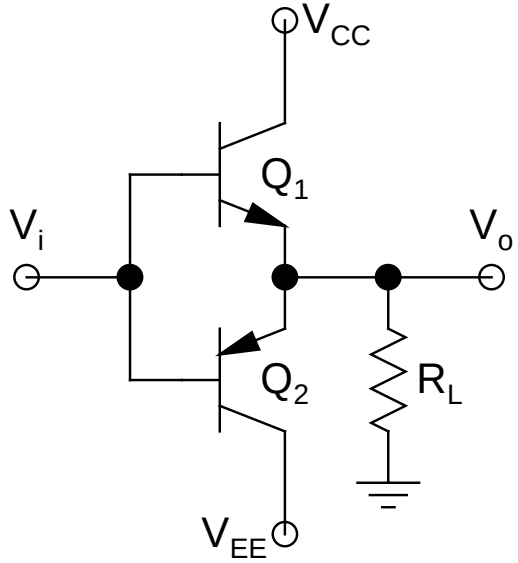
- ***Class B Push-Pull Output Stage***:

  BJT Implementation:

  - Also known as ***Comple-mentary Output Stage***
  - ***Uses dual symmetric power supplies***
  - ***Typical values used***:

    ±3 V, ±5 V, ±12 V, ±15 V
  - ***Q-point***: $V_i = V_o = 0$

    $\Rightarrow V_{be1} = V_{eb2} = 0$



Circuit Schematic

- ***Both Q_1 and Q_2 cutoff***

  $\Rightarrow$ ***Zero standby power***

- ***Note***: $V_{be1} + V_{eb2} = 0$ (***always***)

- ***As $V_i \uparrow$ beyond zero***, $V_{be1} \uparrow$ ***and*** $V_{eb2} \downarrow$

  $\Rightarrow$ ***Q_1 moves towards turning on*** and ***Q_2 is pushed deeper into cutoff***

- ***V_i has to be at least equal to V_γ for Q_1 to conduct*** - till then, ***V_o remains zero***

- ***Once V_i becomes greater than V_γ, Q_1 turns on***, ***supplies current to the load*** (R_L), and ***V_o starts to increase***

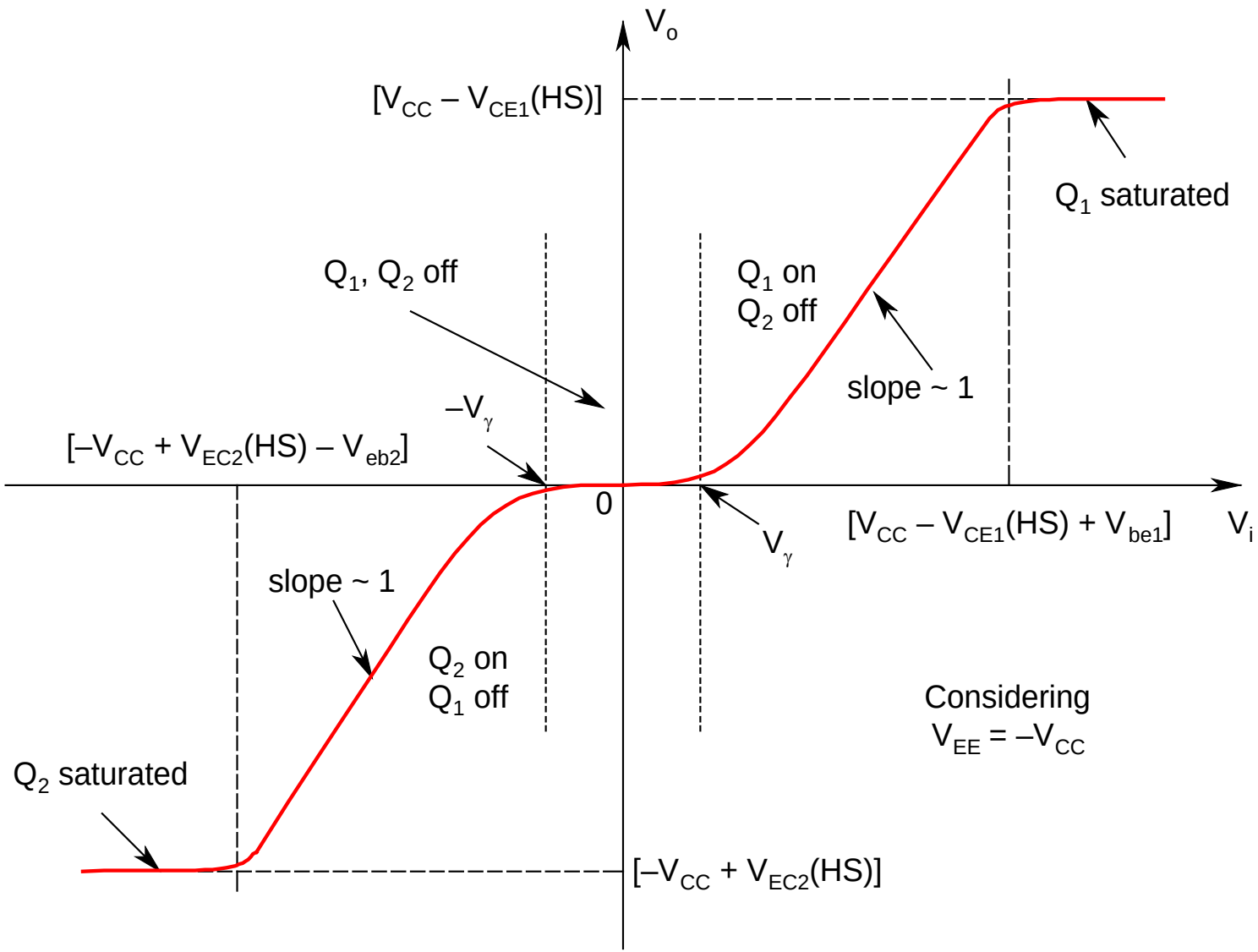
- Similarly, ***as V_i↓ below zero***, ***V_{be1}↓ and V_{eb2}↑***

  $\Rightarrow$ ***Q_2 moves towards turning on*** and ***Q_1 is pushed deeper into cutoff***

- Again, ***V_i has to be at least equal to $-V_\gamma$ for Q_2 to conduct*** - till then, ***V_o remains zero***

- ***Once V_i becomes less than $-V_\gamma$, Q_2 turns on***, ***pulls current away from the load*** (R_L), and ***V_o starts to decrease*** (***remains negative***)

- Thus, the name ***Push-Pull***
  - ***Each transistor remains on for little less than half a cycle***

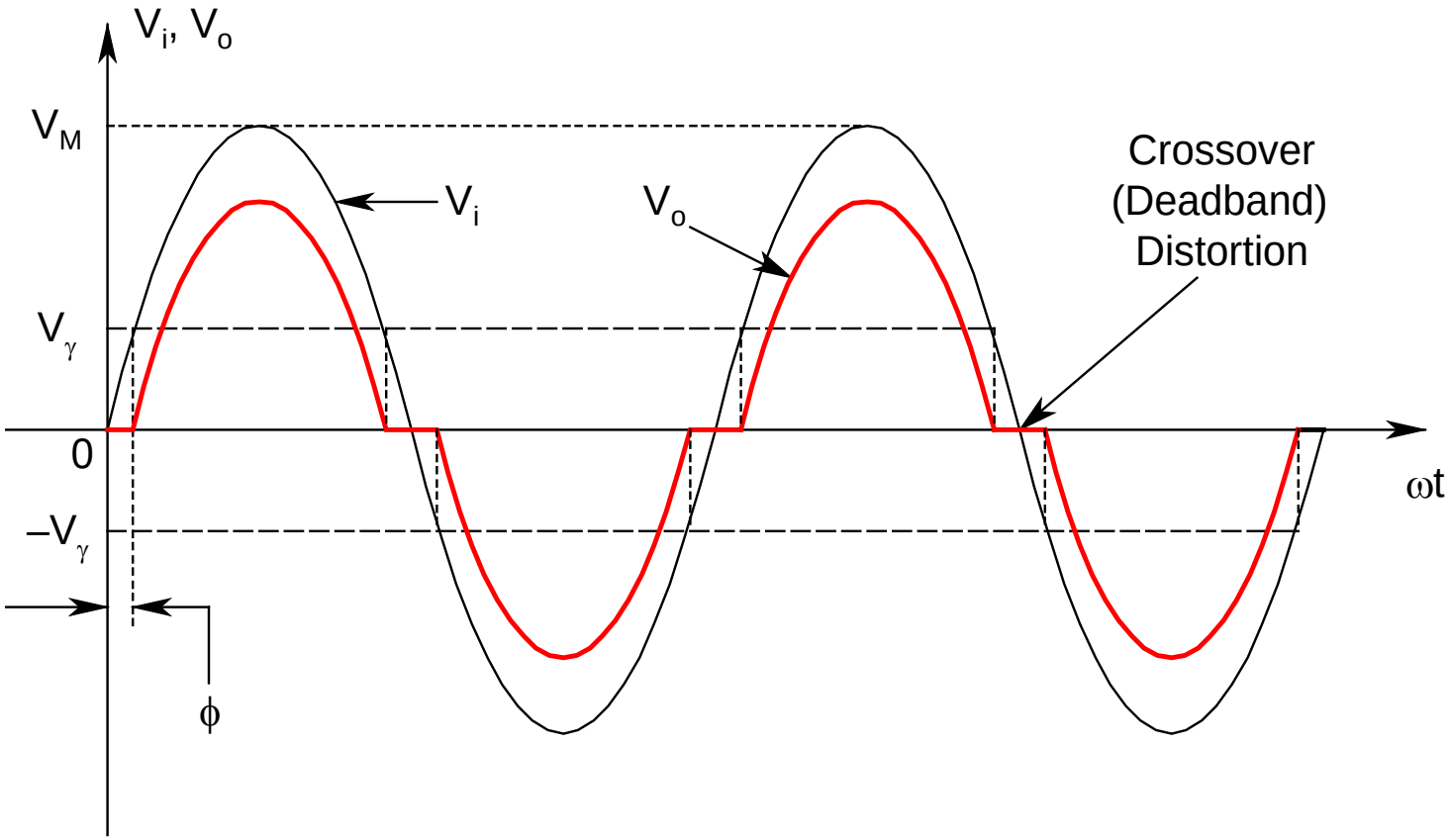


The Voltage Transfer Characteristic (VTC)

- Note the ***deadband*** (***$V_o = 0$***) ***between*** $\pm V_\gamma$
- Consider ***positive*** V_i:
  - ***For*** $V_i > V_\gamma$, V_o ***follows*** V_i with a ***slope of almost unity*** and ***without any phase shift*** (***CC stage***)
  - ***As*** $V_o \uparrow$, $V_{ce1} \downarrow$, and Q_1 ***starts to move towards saturation***

    $\Rightarrow$ ***Positive*** $V_{o,max} = V_{CC} - V_{CE1}(HS)$
  - However, for this to happen, V_i ***has to be greater than*** V_{CC} (since there is an ***extra drop of*** V_{be1})

    $\Rightarrow$ ***This point can never be reached***
- ***The characteristic for negative*** V_i ***can be similarly understood***



Crossover Distortion

➢ *Crossover Distortion*:

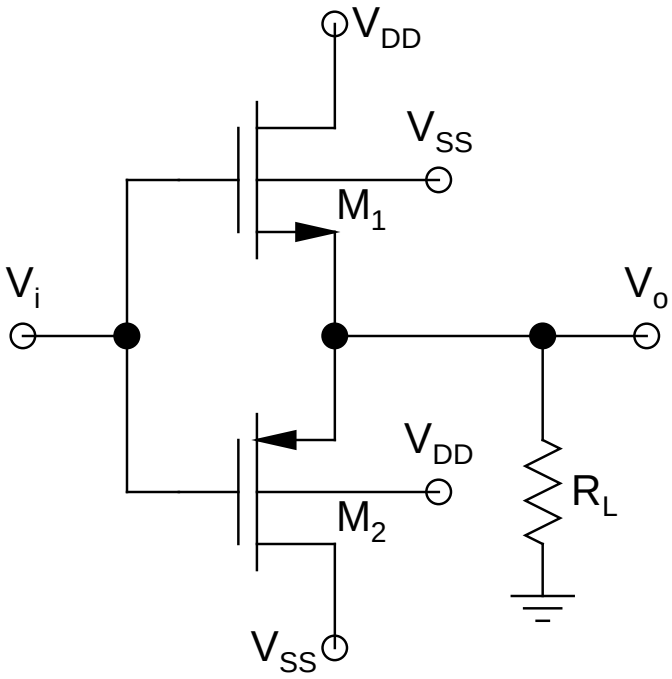
- *Quantified by* ϕ (refer to the diagram)
- *Expressed as*:

  $\phi = \sin^{-1}(V_\gamma / V_M)$

  V_M: *Amplitude of the input signal*
- *Appears four times over a complete cycle*
- *Parameterized* by a term known as the *Total Crossover Distortion* (*TCD*), *expressed in percent*:

  $TCD = (2\phi/\pi)\times 100\%$
- *This distortion becomes more acute as* $V_M \downarrow$
- *For* $V_M \leq V_\gamma$, *no output* ($V_o = 0$ *always*)

- ***MOS Implementation*:**
  - ***Working principle absolutely similar to BJT implementation***
  - ***Only exception that V_γ replaced by V_{TN} and V_{TP}***
  - ***Q-point*: $V_i = V_o = 0$**
  - ***Both devices suffer from body effect issue***



Circuit Schematic

- ***V_{TN} and V_{TP} function of V_o***

  $\Rightarrow$ ***VTC significantly nonlinear***

  $\Rightarrow$ ***Output shows more distortion***

- ***V_i can't be more than V_{DD} or less than V_{SS}***

  $\Rightarrow$ ***V_o can't have rail-to-rail swing***

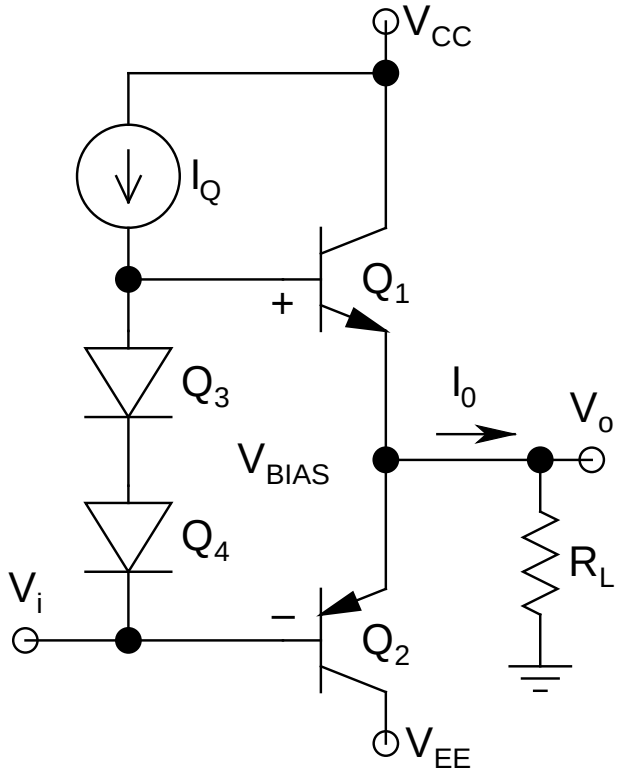
- Also, ***MOS devices*** are ***inherently much poorer*** than their ***BJT counterparts*** in terms of ***current carrying capability***

  $\Rightarrow$ ***Makes this stage quite a poor choice***
  (***needs extremely large W/L ratios***)

- ***Class AB Push-Pull Output Stage***:
  - In a ***Class B*** stage, ***Crossover Distortion*** arises because the transistors are ***absolutely cold*** in the ***standby state***, i.e., ***dead off***
  - If instead, these are ***prebiased*** at the ***verge of conduction***, ***but not quite turned on***, then a ***slight swing*** of the ***input either way*** can make ***one of these transistors turn on*** and ***either supply current to the load*** or ***pull current away from the load***
  - ***This is the whole idea behind a Class AB stage***

- ***Either of the output transistors remain on for complete half cycles***
- Thus, it's a ***mixture of Class A and Class B operation***
- Hence, it's called ***Class AB Push-Pull Stage***
- ***Eliminates Crossover Distortion completely***
- ***Obvious fallout***:
  - ***Dissipation of standby power***
- ***Extremely popular topology and widely used***
- ***Efficiency drops slightly as compared to a pure Class B stage***

- ***BJT Implementation***:
  - ***Needs additional circuitry*** (I_Q-Q_3-Q_4)
  - Q_3-Q_4 ***diode-connected*** transistors and both are ***biased by the same current*** I_Q
  - This produces a ***DC bias*** V_{BIAS} between the ***bases*** of Q_1-Q_2



Circuit Schematic

- Consider ***idling condition*** with ***R_L open-circuited*** (***$I_0 = 0$***)
- ***Neglecting base currents*** of Q_1-Q_2, ***I_Q flows through Q_3-Q_4*** and ***develops a voltage drop***:

$$V_{BIAS} = V_{BE3} + V_{BE4} = V_T \ln\left(\frac{I_Q^2}{I_{S3} I_{S4}}\right)$$

- ***I_Q, I_{S3}, and I_{S4} chosen such that $V_{BIAS} \approx 2V_\gamma$***
- ***Note***: ***V_{BIAS} is also equal to (V_{BE1} + V_{EB2})***

  $\Rightarrow$ ***Q_1-Q_2 remain at the verge of conduction***, ***carrying a standby (or idling) current $I_{Standby}$***

- This ***extra current*** of ($I_Q + I_{standby}$) causes ***standby*** (or ***idling***) power dissipation
- Noting that:

$$V_{BIAS} = V_{BE1} + V_{EB2} = V_T \ln\left(\frac{I_{Standby}^2}{I_{S1}I_{S2}}\right)$$

$$\Rightarrow I_{Standby} = I_Q\sqrt{\frac{I_{S1}I_{S2}}{I_{S3}I_{S4}}}$$

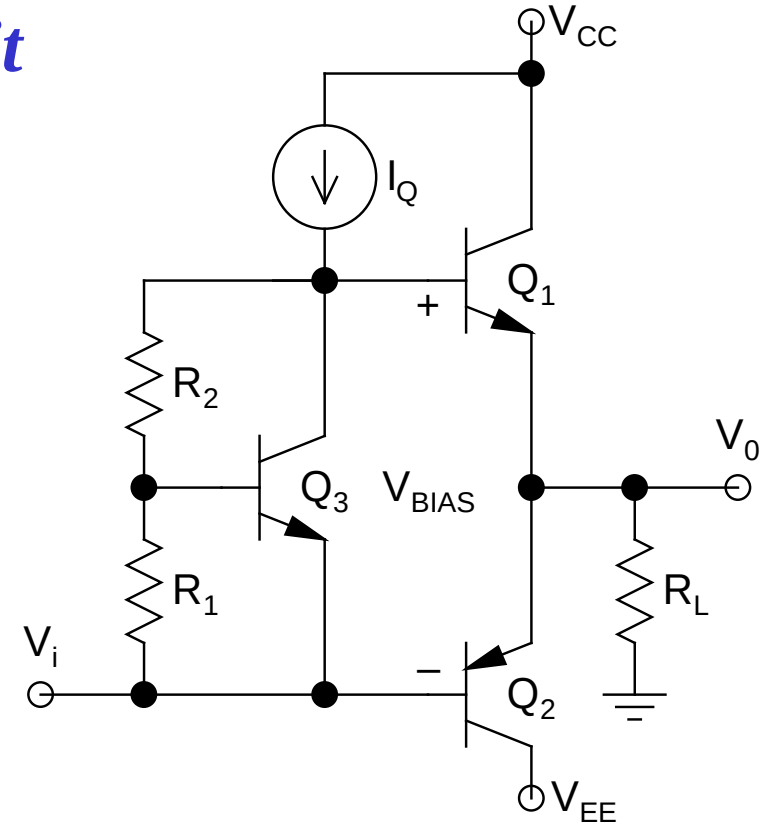
- Now, ***Q_1-Q_2 has to supply/sink large amount of current to/from load*** $\Rightarrow$ ***Their BE junction areas are made large*** $\Rightarrow$ ***Large I_{S1}-I_{S2}***

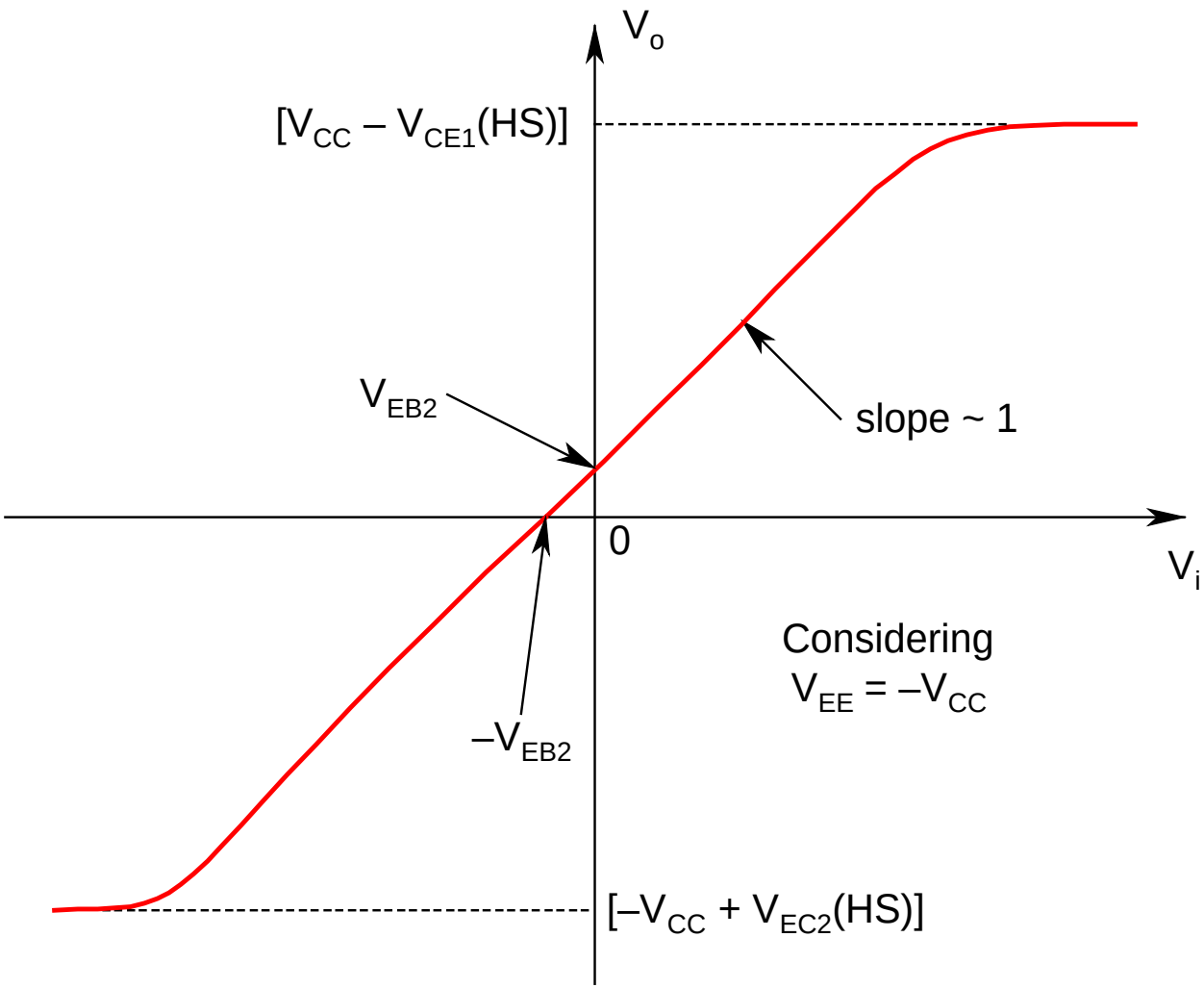
- I_{S1}-I_{S2} typically 10 times or more than I_{S3}-I_{S4}

  $\Rightarrow I_{standby} \geq 10 I_Q$

  $\Rightarrow$ Adds to the power overhead of the circuit

- Another option of prebias circuit:
  - V_{BE}-Multiplier
  - $V_{BIAS} = V_{BE3}(1 + R_2/R_1)$
  - Values of R_1 and R_2 chosen to give $V_{BIAS} = 2V_\gamma$





The Voltage Transfer Characteristic (VTC)

- ***The VTC does not pass through origin***
- ***Intercepts*** (known as ***input-output offset***):
  - $V_i = 0$, $V_o = +V_{EB2}$
  - $V_o = 0$, $V_i = -V_{EB2}$
- ***For $V_i > -V_{EB2}$, $V_{be1}\uparrow$ and $V_{eb2}\downarrow$, with their sum remaining constant at V_{BIAS}***

  $\Rightarrow$ ***Q_1 starts to conduct and supply current to the load*** (R_L), while ***Q_2 starts to go deeper into cutoff***

  $\Rightarrow$ ***V_o starts to follow V_i with a slope ~1*** (***CC stage***)

- ***V_o can rise all the way up to $[V_{CC} - V_{CE1}(HS)]$, provided that V_i can drive it that far***
- Similarly, ***for $V_i < -V_{EB2}$, $V_{eb2} \uparrow$ and $V_{be1} \downarrow$, with their sum again remaining constant at V_{BIAS}***

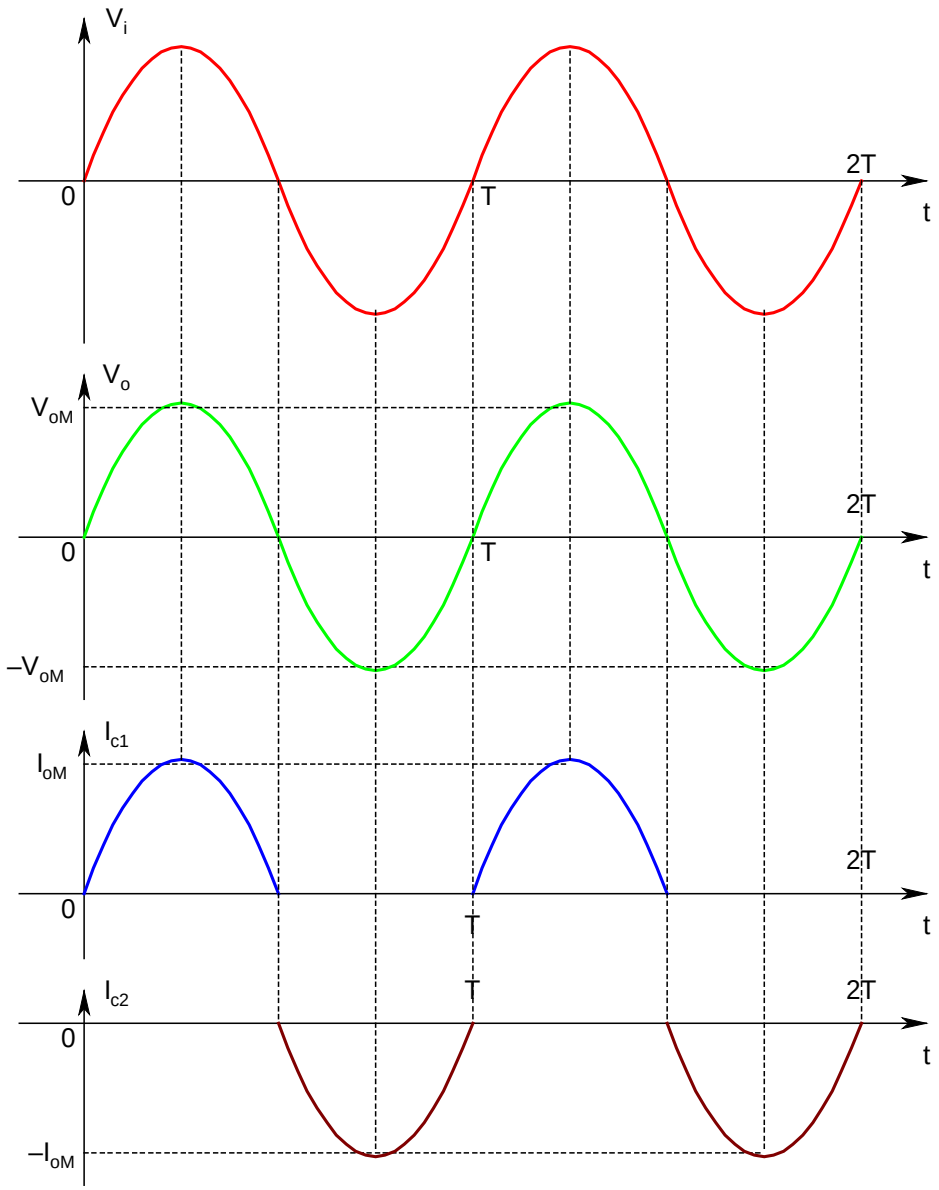
  $\Rightarrow$ ***Q_2 starts to conduct and pull current away from the load*** (R_L), while ***Q_1 starts to go deeper into cutoff***

  $\Rightarrow$ ***V_o again starts to follow V_i with a slope ~1***, and ***can go down all the way to $[V_{EE} + V_{EC2}(HS)]$***

➢ *Power Output and Efficiency*:

- Refer to the figure in the next slide
  - ❖ *The constant offset of $|V_{EB2}|$ is neglected*
- ***Both transistors are not ON over the entire cycle***
  - ❖ ***Q_1 takes care of the positive half cycle***
  - ❖ ***Q_2 takes care of the negative half cycle***
- V_{oM}: ***Maximum value of V_o***
  - ❖ ***Maximum possible swing between $[V_{CC} - V_{CE1}(HS)]$ and $[V_{EE} + V_{EC2}(HS)]$***
- I_{oM}: ***Maximum value of load current*** $(= V_{oM}/R_L)$
- ***Average rms power P_L delivered to load***:

$$P_L = \frac{V_{oM}}{\sqrt{2}} \times \frac{I_{oM}}{\sqrt{2}} = \frac{V_{oM}^2}{2R_L}$$


V_i
0
T
2T
t
V_o
V_{oM}
0
T
2T
t
$-V_{oM}$
I_{c1}
I_{oM}
0
T
2T
t
I_{c2}
T
2T
0
t
$-I_{oM}$

- Now, we need to calculate the ***power supplied to the stage by the power supplies***
- The ***average current I_{supply} drawn by Q_1 from V_{CC}*** (***happens only during the positive half cycle***):

$$I_{supply} = \frac{1}{T}\int_0^T I_{c1}(t)dt = \frac{1}{2\pi}\int_0^{\pi} I_{oM}\sin\theta d\theta = \frac{I_{oM}}{\pi} = \frac{V_{oM}}{\pi R_L}$$

- ***The same current will also be pushed by Q_2 to V_{EE} ($= -V_{CC}$) during the negative half cycle***
- ***Thus, over a complete cycle, the average supply power P_{supply} drawn from the power supplies***:

$$P_{supply} = 2V_{CC}I_{supply} = 2V_{CC}V_{oM}/(\pi R_L)$$

- Thus, the ***power conversion efficiency*** (η):

$$\eta = \frac{P_L}{P_{supply}} = \frac{V_{oM}^2 / (2R_L)}{2V_{CC}V_{oM} / (\pi R_L)} = \frac{\pi V_{oM}}{4V_{CC}}$$

- ***η directly proportional to V_{oM}***, and ***independent of R_L***

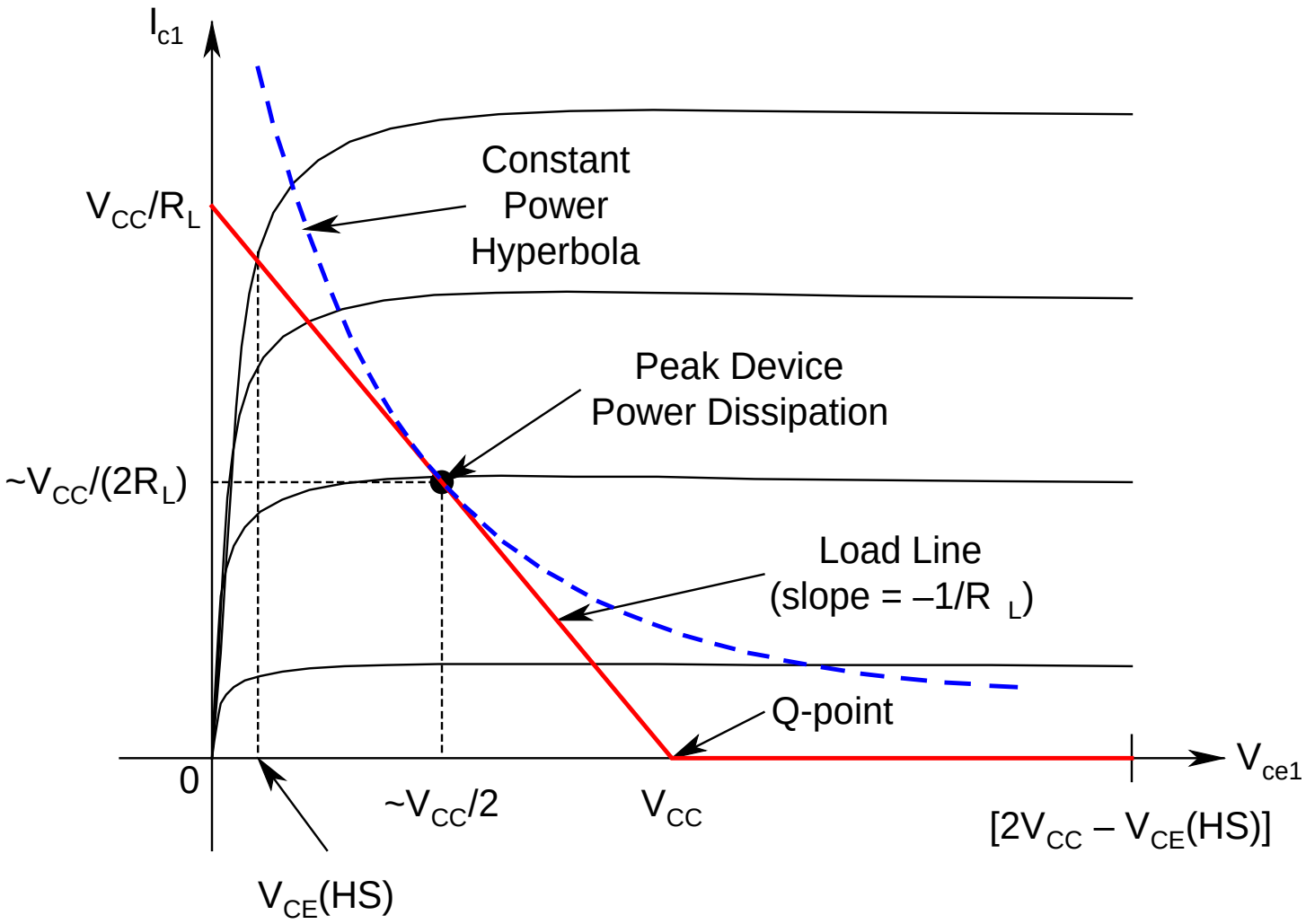
  $\Rightarrow$ ***Significant advantage***

- Also, ***$V_{oM}(max) \approx V_{CC}$***

  $\Rightarrow$ ***$\eta_{max} = \pi/4 = 0.785$ (or 78.5%)***

- ***This value may not be attainable in practice***
  - ***For $V_{oM} = -V_{CC}$, V_i has to be less than $-V_{CC}$***, which ***may not be practically achievable***
  - This analysis ***neglects the standby power*** (***quite small though***) $\Rightarrow$ ***Inclusion of this term will reduce η_{max}***

- ***Transistor Ratings***:
  - Specified by ***two parameters***:
    - ***Breakdown Voltage***
    - ***Maximum Power Rating***
  - ***Breakdown Voltage***:
    - ***Maximum positive/negative V_{CE} that can be applied to an npn/pnp BJT***
      - Known as the ***Collector-to-Emitter Breakdown Voltage with Base Open*** (BV_{CE0})
    - ***Focus on Q_1*** (***Q_2 will be similar***)
    - Refer to the diagram in the next slide (***Output characteristic of Q_1 along with the load line***)
    - In the analysis, the ***offset in the VTC***, the ***small standby current***, and ***V_{CE1}(HS)*** are ***neglected***



The Output Characteristic of Q_1 along with the Load Line

- ***At Q-point***: $V_o = 0 \Rightarrow V_{ce1} = V_{CC}$
- ***During positive half cycle***:

  $V_o(max) \approx V_{CC} \Rightarrow V_{ce1} \approx 0$

  $\Rightarrow$ ***V_{ce1} ranges between 0 and V_{CC} during the positive half cycle***
- The ***slope of the load line*** in this part of the characteristic = $-1/R_L$
- ***For negative half cycle***, ***Q_1 cuts off*** (***Q_2 conducts during this period***)

  $\Rightarrow$ ***$I_{c1} = 0$ for V_o ranging between 0 and $-V_{CC}$***

  $\Rightarrow$ ***$V_{ce1}(max) = 2V_{CC}$***

  $\Rightarrow$ ***$BV_{CE0} = 4V_{CC}$*** [using a ***Safety Factor*** (or ***Factor of Safety***) of 2]

- ***Maximum Power Rating***:
  - ***Same for both Q_1 and Q_2***
  - ***Average power P_L delivered by Q_1 to R_L during the positive half cycle*** = ***area covered under the load line***

$$\Rightarrow P_L = \frac{1}{2} \times V_{CC} \times \frac{V_{CC}}{R_L} = \frac{V_{CC}^2}{2R_L}$$

  - Refer to the ***constant power hyperbola*** ($V_{ce1} \times I_{c1}$) shown in the figure
  - ***Maximum power dissipation of Q_1 happens when this hyperbola becomes tangent to the load line***, ***which is right at the middle of the load line***
  - ***Proof***:

Constant power hyperbola (P_1):

$$P_1 = V_{ce1} \times I_{c1} = \left(V_{CC} - I_{c1}R_L\right) \times I_{c1} = V_{CC}I_{c1} - I_{c1}^2 R_L$$

Plug $dP_1/dI_{c1} = 0$ to get $I_{c1} = V_{CC}/(2R_L)$

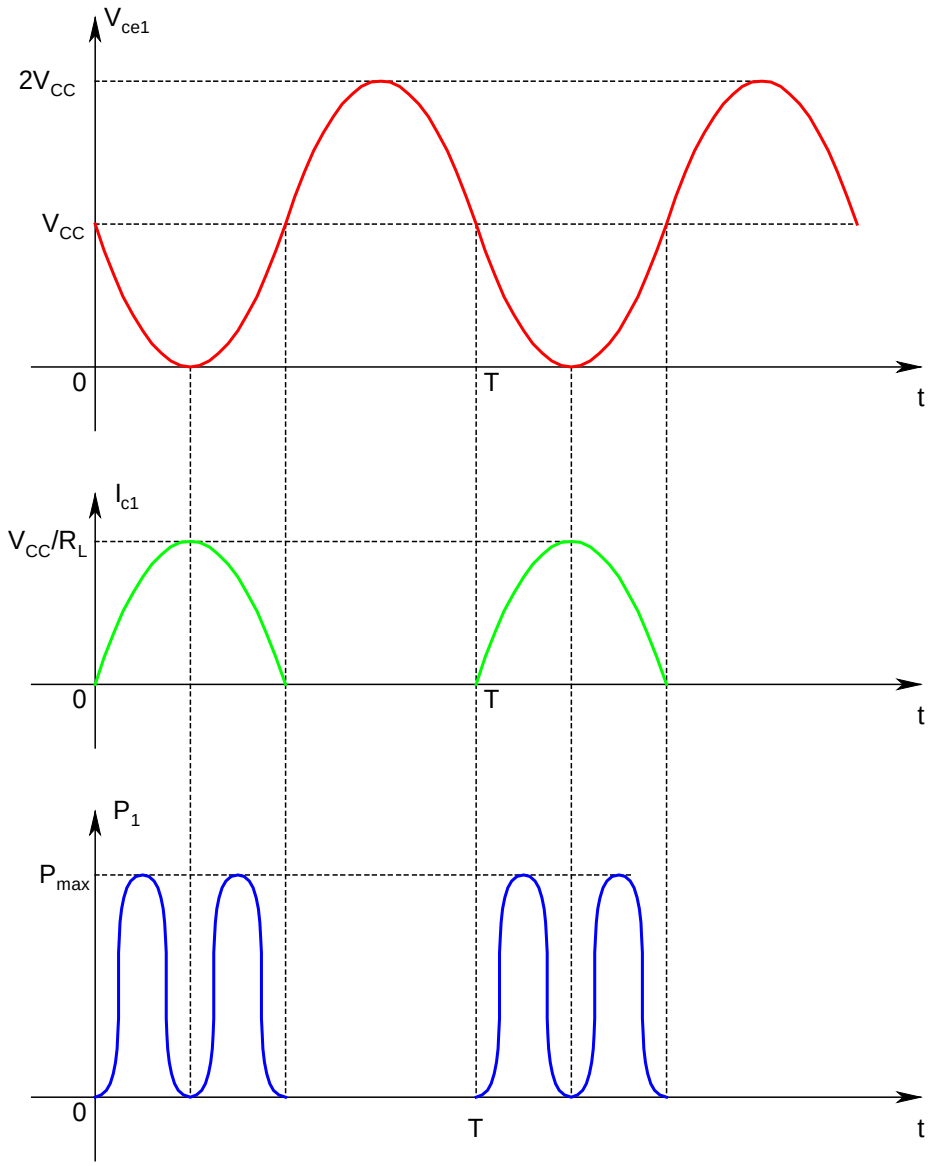
This is the ***mid-point of the load line***, with ***coordinates*** $[V_{CC}/2, V_{CC}/(2R_L)]$

$$\Rightarrow P_{max} = \frac{V_{CC}^2}{2R_L} \quad (\textbf{\textit{using a Safety Factor of 2}})$$

- There is also ***standby power***:

  $P_{Standby} = V_{CC} \times I_{Standby}$

- In general, $P_{max} >> P_{Standby}$
- Refer to the figure in the next slide
  - V_{ce1} ***oscillates between 0 and*** $2V_{CC}$
  - I_{c1} ***appears only during the positive half cycle***, ***with peak value of*** V_{CC}/R_L (***when*** $V_{ce1} = 0$)
  - P_1 $(= V_{ce1} \times I_{c1})$ ***oscillates*** between 0 and $V_{CC}^2/(4R_L)$ at ***twice the frequency*** only during the ***positive half cycle***


V_{ce1}
$2V_{CC}$
V_{CC}
0
T
t
I_{c1}
V_{CC}/R_L
0
T
t
P_1
P_{max}
0
T
t

- ***Two Special Cases***:
  - $R_L \rightarrow \infty$ (***open-circuit***):

    Load line becomes horizontal with $I_{c1} = 0$

    $\Rightarrow P_1 = 0 \Rightarrow$ ***no issue***
  - $R_L = 0$ (***short-circuit***):

    Load line becomes vertical with $I_{c1} \rightarrow \infty$

    Potentially dangerous situation

    Resulting power dissipation and consequent heat generation can completely damage the device
- ***In actual situation***, I_{c1} ***won't reach infinite value due to***:
  - ***Limited current driving capability of the driver stage***
  - ***Fall of*** β ***at high current levels*** due to ***High-Level Injection*** or ***Kirk Effect***
- These two are ***in-built self-protection mechanisms***
- Nevertheless, ***practical output stages need short-circuit protection***

➢ *Linearity and Output Resistance*:

- *While supplying/sinking current to/from load*, Q_1/Q_2 *operate in CC mode*

  $\Rightarrow A_v = R_L/(R_L + r_{Ei})$ $(i = 1,2)$ $(r_{Ei} = V_T/I_{ci})$

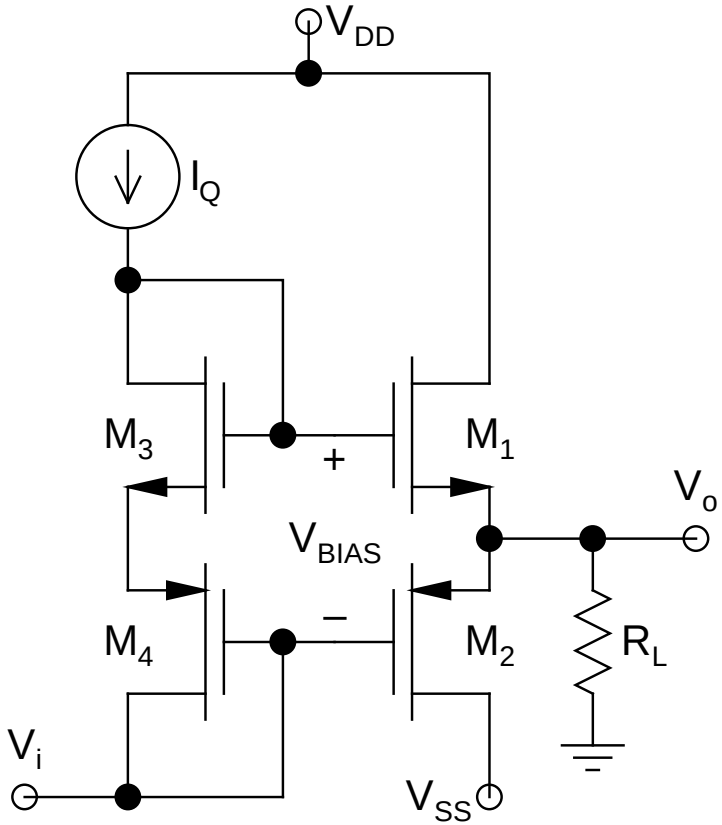
- Thus, if $R_L >> r_{Ei}$, then $A_v \rightarrow 1$, and *very high linearity in the VTC can be achieved*
- However, r_{Ei} *is not constant* - rather *it changes with the load current*
- Thus, A_v *can depart significantly from unity*, when the *load current is very small* (*large* r_{Ei})
- Referring to the *VTC*, the *slope of the characteristic near* $\pm V_\gamma$ will be *significantly less than unity* (*Class B*)

- However, ***as $V_o \uparrow$, load current $\uparrow$, $r_{Ei} \downarrow$***, and the ***VTC starts to attain its maximum slope of unity***
- Thus, ***for major part***, the ***VTC is highly linear*** and ***produces an almost distortionless output***
- ***Output Resistance***:
  - ***Open R_L*** and ***look back from the output***
  - ***$R_0 = r_{Ei}$*** (***by inpsection***), since ***bases of Q_1-Q_2*** can be considered to be at ***ac ground***
  - ***R_0 is variable***, but ***for major part***, ***extremely small***
- Generally, the ***linearity and output resistance*** are ***calculated*** at the ***region of maximum slope*** of the ***VTC***

- ***Summary***:
  - *Quite small standby power*
  - *Large current driving capability*
  - *Almost linear VTC*
  - *Very low distortion at the output*
  - $A_v \sim 1$
  - *No phase shift between input and output*
  - *Very low output resistance*

  Thus, this stage is a superb one and is highly popular!

- ***MOS Implementation***:
  - ***Biased using dual symmetric power supplies V_{DD}/V_{SS}***
  - ***M_1-M_2 in push-pull configuration***
    - ***M_1 supplying current to load (R_L) during the positive half cycle***
    - ***M_2 pulling current away from load during the negative half cycle***



Circuit Schematic

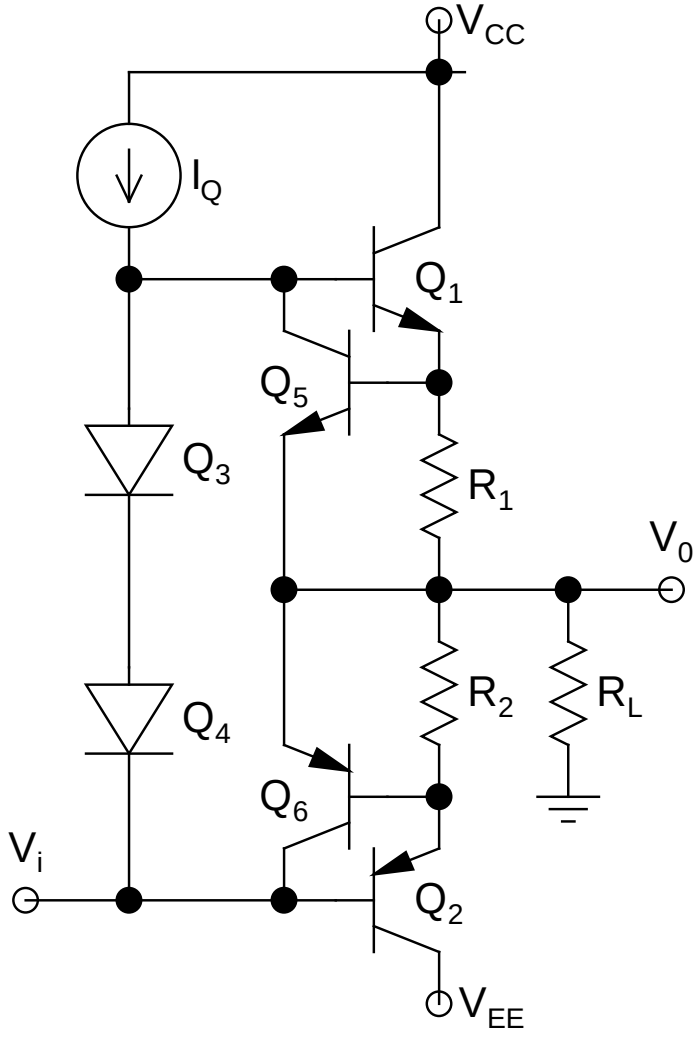
- M_1-M_2 ***prebiased*** by the ***series combination*** of M_3-M_4 (***both diode-connected***) ***biased with*** I_Q
- ***Develops*** V_{BIAS} ***across the gates of*** M_3-M_4, which is ***same as that between the gates of*** M_1-M_2
- V_{BIAS} ***chosen to be slightly less than*** $(V_{TN} + |V_{TP}|)$
- ***Crossover Distortion eliminated completely***, at the cost of ***introducing standby power*** into the system
- ***Rest of the operation of the circuit exactly similar to that of a BJT Class AB Push-Pull Output Stage***

- ***All transistors suffer from body effect problem***

  $\Rightarrow$ ***More distortion at the output***
- ***The linearity of the VTC is not that good***
- ***Low current drive capability***
- ***Biasing itself becomes tricky***, due to the ***body effect of M_3-M_4***
- The ***output resistance not that low***, since ***MOSFETs have lower g_m than BJTs***
- Overall, the stage ***suffers from quite a few problems*** and is ***not used much***
- We will explore this through an assignment

- ***Overload Protection***:
  - ***Protects the output stage from accidental short-circuits***
  - ***Needs 4 more components***:
    - ***2 BJTs*** (Q_5,Q_6)
    - ***2 Resistors*** (R_1,R_2)

      R_1,R_2 ~ 25-50 Ω



Circuit Schematic

- During ***normal operation***, these ***extra circuits*** play absolutely ***no role***, and come ***into picture*** only under ***accidental short-circuit*** of the ***output terminal to ground***
- ***Numerical Example***:
  - Assume V_i at its ***positive peak***, the ***maximum drive current*** to the base of Q_1 = 1 mA, and $\beta_1 = 100$
  - Now output gets ***accidentally shorted to ground*** ($V_o = 0$)

    $\Rightarrow$ $I_{c1} = 100\ mA$ and $V_{ce1} = 5\ V$

    $\Rightarrow$ $P_1 = 500\ mW$
  - This may be ***way above*** the ***maximum power rating*** of the transistor (~ ***100-150 mW***) and the transistor would ***burn out*** $\Rightarrow$ ***potentially dangerous situation***!

➢ *Principle of Operation of the Protection Circuit*:

- Assume *positive* V_i with Q_1 *supplying current to load*
- Q_2 *is off during this time*
- As $R_L \downarrow$, $I_{c1} \uparrow$ (since $I_{c1} = V_o/R_L$)

  $\Rightarrow V_{be5}\ (= I_{c1}R_1)$ *also* $\uparrow$
- As $V_{be5} \rightarrow V_\gamma$ of Q_5, it starts to *turn on*

  $\Rightarrow$ A *part of base drive current* of Q_1 starts to get *shunted away* by Q_5, and *appears at the output* almost *without any gain* $(1/\alpha_5)$
- This acts as a *limit of the rate* at which the *output current can increase*, and thus, *protects the circuit*

- Thus, the ***current can't increase indefinitely***
- Assume $R_1 = 30\ \Omega$ and $V_\gamma = 0.6\ V$

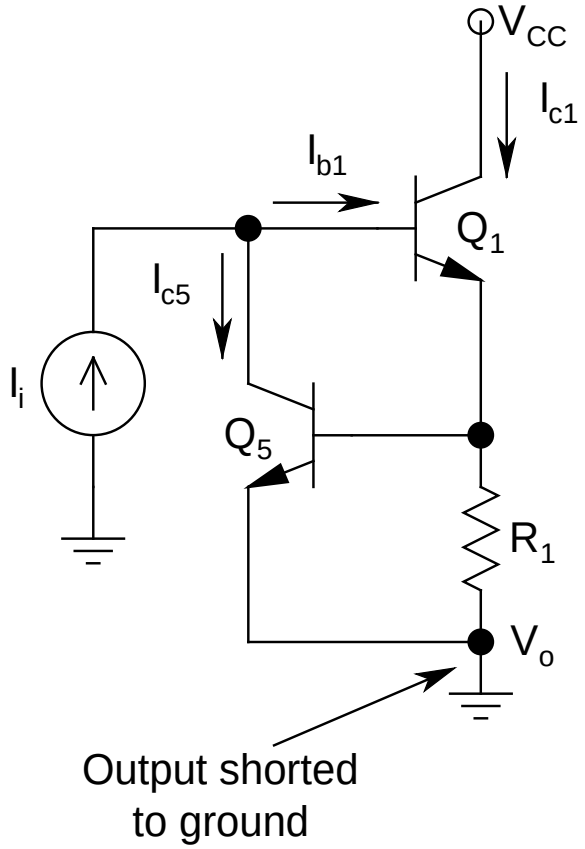
  $\Rightarrow$ As soon as I_{c1} ***reaches about 20 mA***, Q_5 ***cuts in***, ***shunts current away from the base of*** Q_1, and ***protects the circuit***
- Due to the ***exponential dependence*** of this ***shunted current*** on V_{be5}, the ***maximum output current*** will ***saturate near around 20 mA itself***
- Thus, under this case, if the output is ***accidentally shorted to ground***, then P_1***(max) will be around 100 mW***, which is ***well within limit***, and ***protection will be achieved***

- Similarly, for the ***negative half cycle***, this job of ***protection will be achieved by the Q_6-R_2 combination***
- The ***drop across R_2*** will depend on the ***amount of current*** being ***sunk by Q_2***
- Once this drop ***reaches the cut-in voltage*** of Q_6, it will ***turn on***, and ***bypass the drive current of Q_2***, thus ***protecting the circuit***
- This ***protection circuit*** is ***widely used*** due to its ***efficacy***, and the ***most popular analog building block***, the ***op-amp***, ***uses this protection scheme***

➢ *Quantitative Estimate of the Protection Mechanism*:

- Assume ***V_i positive*** and ***supplying drive current*** I_i to Q_1
- ***Output shorted to ground*** $\Rightarrow V_o = 0$
- $I_i = I_{b1} + I_{c5}$

  $I_{c5} = I_{S5}\exp(V_{be5}/V_T)$
- $V_{be5} = I_{c1}R_1$ (***assuming $\alpha_1 = 1$*** and ***neglecting I_{b5}***)



Protection Scheme

- For ***small values*** of I_{c1}, V_{be5} will be ***small***, and I_{c5} will be ***negligible***
- Also, $I_{c1} = \beta_1 I_{b1} = \beta_1(I_i - I_{c5})$

  $\Rightarrow \beta_1 I_i = I_{c1} + \beta_1 I_{S5} \exp(I_{c1} R_1 / V_T)$
- This is the ***final protection expression***
- For ***small*** I_{c1}, the ***second term*** on the ***RHS*** will be ***negligible***

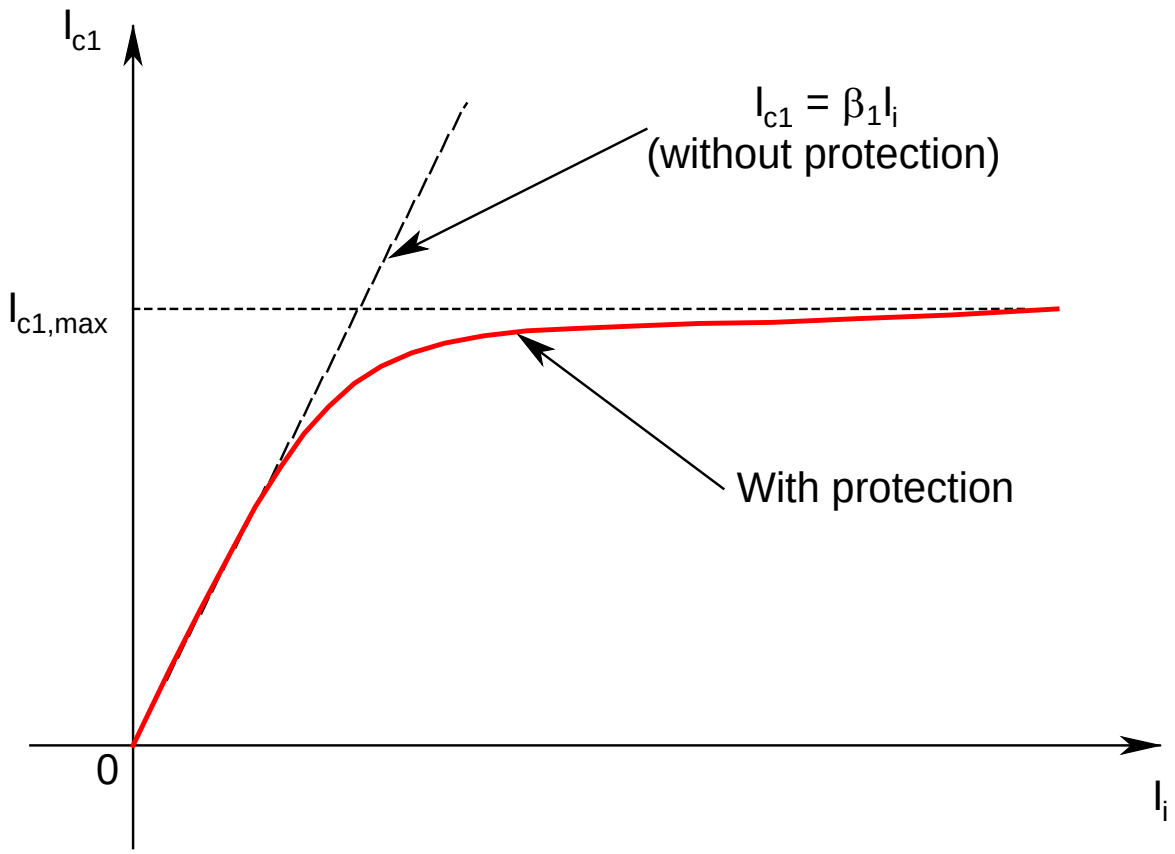
  $\Rightarrow$ ***I_{c1} would follow I_i linearly with proportionality constant β_1***
- As ***I_{c1}*** $\uparrow$, the ***second term*** on the RHS ***increases at a much more rapid rate*** than the ***first term***

- Once it starts to become ***comparable*** to the first term, a ***very little change*** in I_{c1} can ***counter a large change*** in I_i

  $\Rightarrow$ ***I_{c1} gets clamped to almost a constant value of $I_{c1,max}$***

- Note that the ***protection equation*** is ***transcendental***

  $\Rightarrow$ ***Needs numerical or iterative solution***



Protection Characteristic