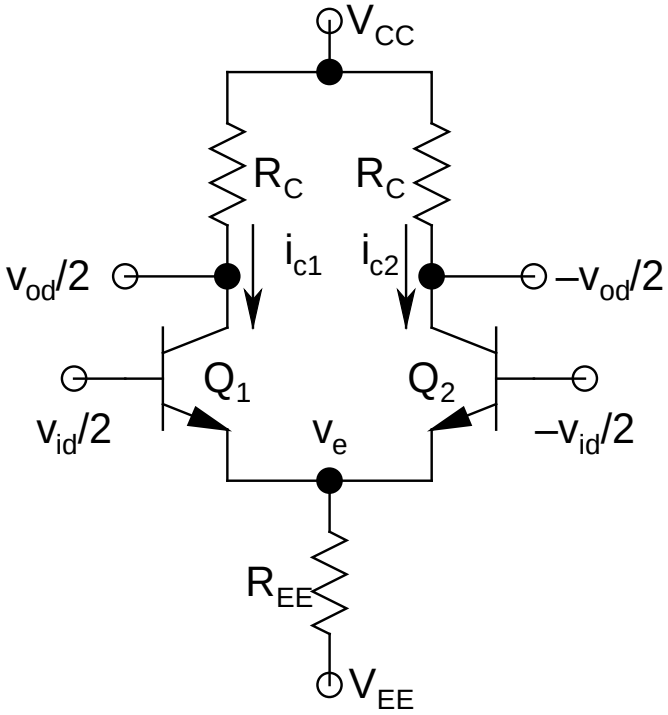
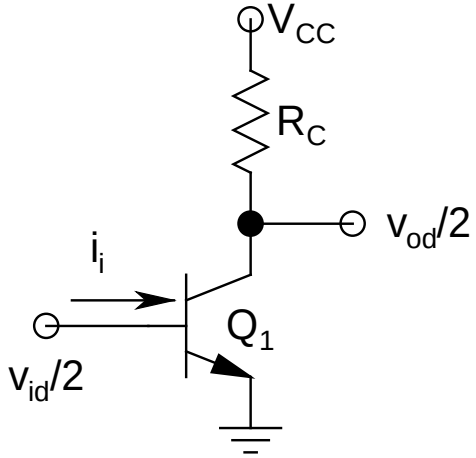
➢ *Differential-Mode Half Circuit*: *Calculation of A_{dm}*:



npn DA Under Pure Differential-Mode Input



Differential-Mode Half-Circuit

- ***Thus, the left and right parts of the circuit become absolutely symmetrical***

  $\Rightarrow$ ***Either of the parts can be used***

  $\Rightarrow$ ***Leads to the differential-mode half-circuit***

- $g_{m1} = g_{m2} = g_m = I_{EE}/(2V_T)$, $r_{E1} = r_{E2} = r_E = 2V_T/I_{EE}$, and $r_{\pi 1} = r_{\pi 2} = r_\pi = \beta r_E$

- ***Can be easily identified to be a CE stage***

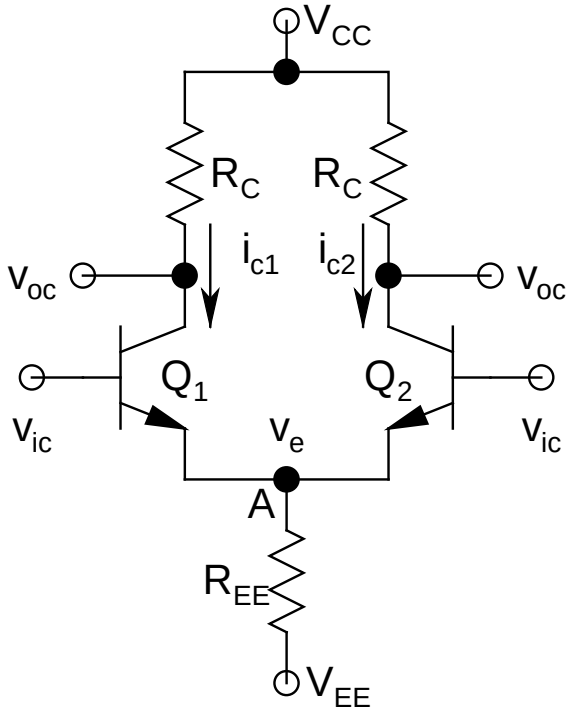
  $\Rightarrow A_{dm} = v_{od}/v_{id} = (v_{od}/2)/(v_{id}/2) = -R_C/r_E$

- ***Differential-mode input resistance***:

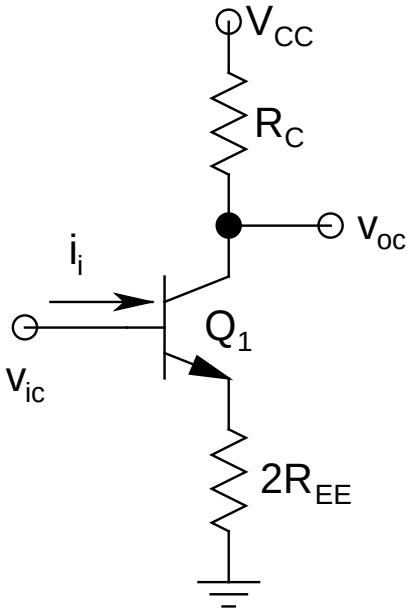
  $R_{id} = v_{id}/i_i = 2(v_{id}/2)/i_i = 2r_\pi$

- ***The simplicity of the analysis is simply mind-boggling***!

➢ *Common-Mode Half-Circuit*: *Calculation of* A_{cm}:



npn DA Under Pure Common-Mode Input



Common-Mode Half-Circuit

- $i_{c1} = i_{c2} = i_c = g_m(v_{ic} - v_e)$
- These two currents ***sum up at node A*** and ***flow through R_{EE}***, ***creating a voltage drop of $2i_cR_{EE}$ across it***
- Thus, ***R_{EE} can be split into two parts***, ***$2R_{EE}$ each***, and ***each part put in the emitter leads of Q_1 and Q_2***
- ***The lead connecting the two parts of R_{EE} would not carry any current, and can be removed***
- ***Thus, the circuit becomes perfectly symmetric along a vertical cut-line going through the middle of the circuit***, and we can ***consider either of them***

  $\Rightarrow$ ***Leads to the common-mode half-circuit***

- ***Can be easily identified to be a CE(D) stage***

  $\Rightarrow A_{cm} = v_{oc}/v_{ic} = -R_C/(r_E + 2R_{EE}) \approx -R_C/(2R_{EE})$

  (since, in general, $R_{EE} >> r_E$)

- ***Common-mode input resistance***:

  $R_{ic} = v_{ic}/i_i = r_\pi + (\beta + 1)2R_{EE} \approx 2\beta R_{EE}$

  (since, in general, $R_{EE} >> r_\pi$)

- ***Input resistance of the npn DA***:

  $R_i = R_{id} \| R_{ic} \approx R_{id} = 2r_\pi$ (***from superposition***)

  (since, in general, $R_{ic} >> R_{id}$)

- ***CMRR*** $= 20\log_{10}(|A_{dm}/A_{cm}|) \approx 20\log_{10}(2R_{EE}/r_E)$

- ***Some insights***:
  - A_{dm} *is independent of* R_{EE}, however, A_{cm} *is a strong function of* R_{EE}
  - *Goal is to make* A_{cm} *as close to zero as possible*

    $\Rightarrow$ *Make* R_{EE} *as large as possible*
  - *High value of* R_{EE} *will automatically ensure high value of CMRR* (*Highly desirable*!)
  - *High CMRR can also be achieved by reducing* r_E

    $\Rightarrow$ *Can be obtained by increasing the DC bias current*

    $\Rightarrow$ *DC power dissipation of the circuit goes up*

    $\Rightarrow$ Also, *DC biasing may become suspect*!

- ***Increasing the Linear Range***:
  - ***Linear Range***: $\pm 4V_T$ (~ ***± 100 mV at room temperature***)
  - ***For some applications, this may not be enough***
  - ***Linear Range can be increased by attaching two identical resistors (R_E) in the emitter branches of Q_1 and Q_2***
  - ***Increases Linear Range by $I_{EE}R_E$*** (***Show***!)
  - ***This method decreases A_{dm}*** (***differential-mode half-circuit becomes CE(D) topology***)
  - ***Has minimal effect on A_{cm}***
  - ***CMRR suffers***! $\Rightarrow$ ***Not an optimal choice***!