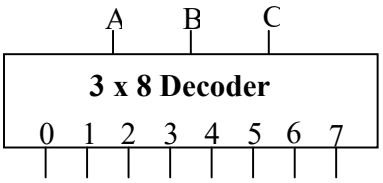
ESc201A Home Assignment 9 (last) Nov. 04, 2019.

Solutions of the HA#9 will be on Brihaspati on 11/11/19.

1. Four switches operate a lamp as follows: the lamp lights up if switches 1,3 and 4 are closed (bit '1') and switch 2 is open (bit '0'), or if 2, 4 are closed and 3 is open, or if all the switches are kept closed. Express this as a boolean function in a standard sum of product form and solve it using k- map.

2. Assume you have been asked to design a flight takeoff signal for the pilot and the conditions given are:
   i) Flights can takeoff in fair weather.
   ii) In bad weather flights can takeoff only with instrument capability.
   iii) No flights can takeoff if the flight controllers are on strike.
   Design the logic circuit with minimum number of gates.

3. A 3x8 decoder, as shown, is provided to perform the following operations:



   a) $X=A\,\bar{B}C + B\,\bar{C}$.
   b) $Y= \bar{B}C + A\,\bar{C}$
   c) $Z=AB\,\bar{C} + \bar{A}B$
   Use this decoder and implement all of X, Y, and Z functions using only 3-input OR gates.

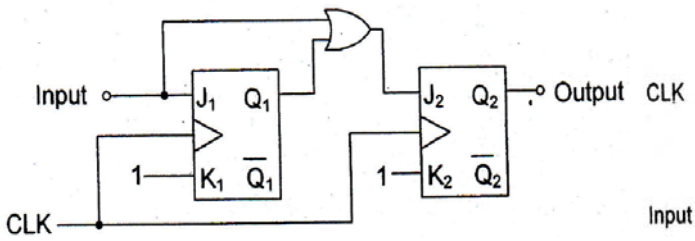
4. Design a circuit that will give the 2's complement of a 3-bit number using SR Flip-Flop and a register with other gates, as required.

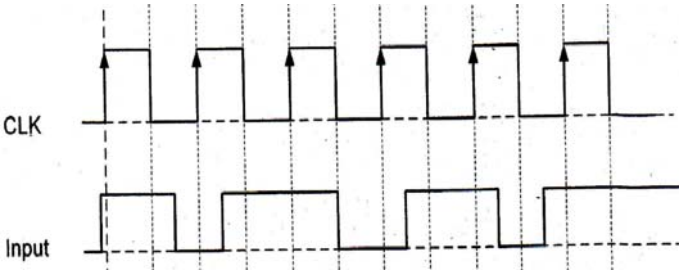
5. Using OR, AND and XOR gates for the logic circuit:

(a) The gated S-R latch has unpredictable behaviour if the S and R inputs are both equal to 1. One way to solve this problem is to modify the inputs in such a way that the state holds (does not change) when S=1, R=1 appears at the input. Achieve this by using a minimum number of gates outside the SR-latch.

(b) Verify that the JK Truth Table is satisfied by the equation $Q_{n+1}= J_n\,\bar{Q}_n + \bar{K}_nQ_n$.

6. Reproduce the characteristic table of a JK-Flip-Flop. The input waveform to the given circuit of the left is as shown below on the right. Assume that all the devices in the circuit have no delay. Sketch the output waveform with proper timing with respect to the clock.





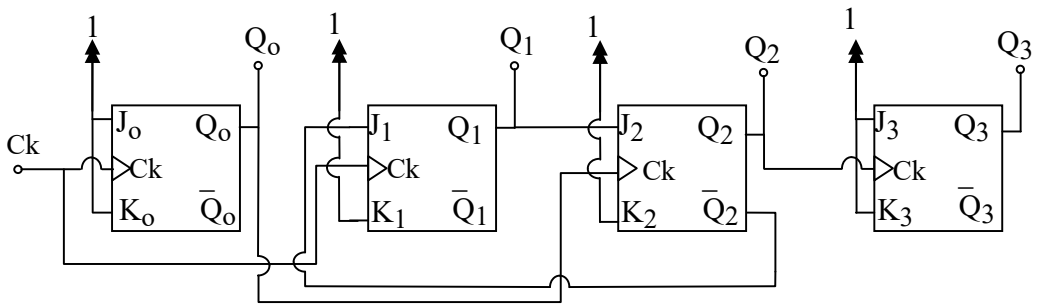
7. Design a synchronous counter using D-flip-flop such that it generates the following sequences of state $Q_AQ_BQ_C$ (010; 110; 001; 011; 010). Consider all unused states as "Don't care". Give the simplified expressions for the D inputs of the flip-flops. Use 2-input AND and OR gates for the logic circuit.

8. A sequential circuit with two flip-flops A and B, two inputs X, Y and an output Z has the behaviour:
   $A(t + 1) = \bar{X}{:}Y + X{:}B; B(t + 1) = \bar{X}{:}A + X{:}B; Z = A$
   Draw the logic diagram of the circuit, list the state table and draw the state transition graph.

9. A Flip-Flop is required which has the truth table give here. Realize it using JK Flip-Flop and any minimum additional gates required.

X	Y	Q_{n+1}
0	0	$\bar{Q}_n$
1	0	Q_n
0	1	1
1	1	0

10. For the block diagram shown below, show that it is a 4:1 counter, which starts from the outputs at (0000).



11. Design a synchronous counter using T flip-flops that goes through the following repeating sequence 0, 1, 3,7,6,4. Take the unused states as don't care states.
12. Design a 3- bit synchronous counter using JK-flipflops showing the implemented circuit using AND and OR gates only, which counts 0, 2, 4, 6, 7, 5, 3, 1, 0,.....
13. Design a Modulo-6 ripple up-counter using J-K Flip-Flops, returning to the 000 state at the last required count.
14. From a frequency of 10KHz, generate a signal of frequency 1KHz having the following waveform.