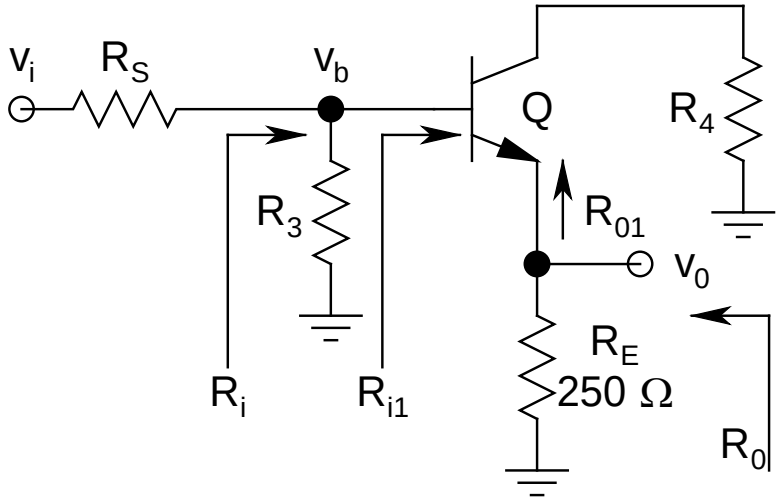
- ***What if the output is taken from emitter***?
- Redraw the ***ac schematic***:



ac Midband Schematic for Output Taken from Emitter

- ***First, short v_i to ground***

  $\Rightarrow$ ***R_3 comes in parallel with R_S (call this combination R_5)***

  $\Rightarrow R_5 = R_3 \| R_S = 900\ \Omega$

- ***R_5 comes in series with r_π (call this combination R_6)***

  $\Rightarrow R_6 = R_5 + r_\pi = 2.2\ k\Omega$

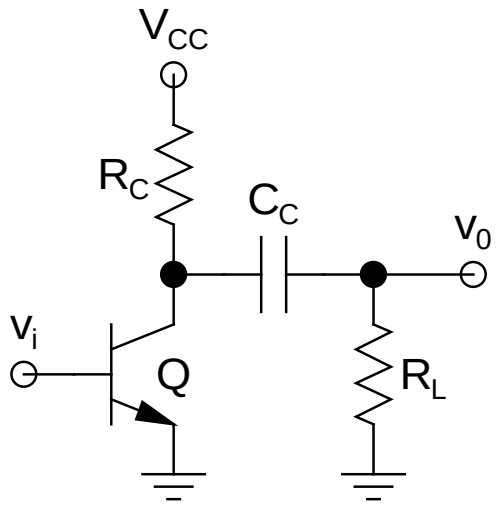
- ***Transform R_6 to emitter by dividing it by (β +1)***

  $\Rightarrow R_{01} = R_6/(\beta + 1) = 21.8\ \Omega$

- Thus, $R_0 = 20\ \Omega$ (***Easy***?)
- ***Summary***:
  - $A_v = 0.827$
  - $R_i = 6.72\ k\Omega$
  - Resistance ***seen*** by $v_i = 7.72\ k\Omega$
  - $R_0 = 20\ \Omega$
- Thus, this circuit has ***voltage gain close to unity***, ***ok input resistance***, and ***very small output resistance***
  - ***Ideal characteristics*** needed for a ***Buffer***/***Isolator***/ ***Impedance Matcher***

- ***Loading Effect***:
  - ***Neglecting r_0***:

    $A_v = -g_m(R_C \| R_L)$
  - ***R_L has no role in DC biasing, but comes into picture in ac calculations***
  - As $R_L \downarrow \Rightarrow |A_v| \downarrow$
    - Known as ***Loading Effect***
  - Similar situation happens when a ***high output resistance driver*** drives a ***low input resistance load*** (e.g., ***CE stage driving a CB stage***)



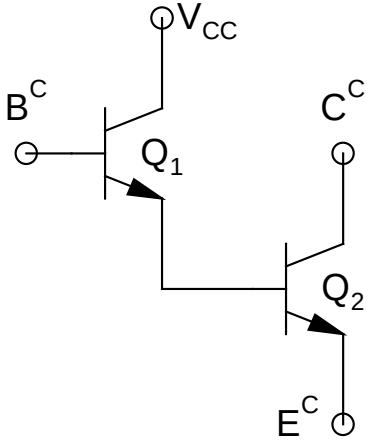
- The ***gain of the CE stage*** will be ***severely compromised*** due to ***low input resistance*** of the ***CB stage***
  - Known as ***Impedance Mismatch*** between ***Driver and Load***
- Under such a situation, need an ***Isolator***/***Buffer***/ ***Impedance Matcher*** between the two stages
- A ***CC stage perfectly fits the bill*** due to its ***high input resistance*** and ***low output resistance***, and ***can be used to couple the CE stage to CB stage***
- ***MOS circuits generally don't have this problem***

Compound Connections

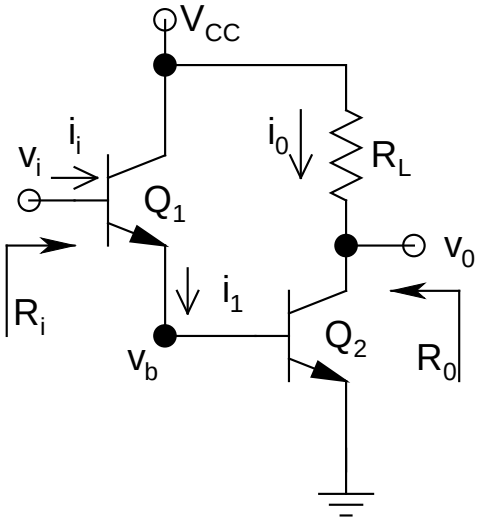
- ***Multi-Stage***
- Have some ***special properties***
- ***Popular Topologies***:
  - ***Darlington***
  - ***Cascode***
  - ***DP*** (or ***DA***)
- ***Modules by themselves***

- ***Darlington***:
  - Cascade of a ***CC*** stage, followed by either a ***CE*** or a ***CC*** stage
  - ***Two biggest advantages***:
    - ***Extremely large R_i***
    - ***Extremely large A_i***
  - ***These two advantages are automatic for MOS stages***

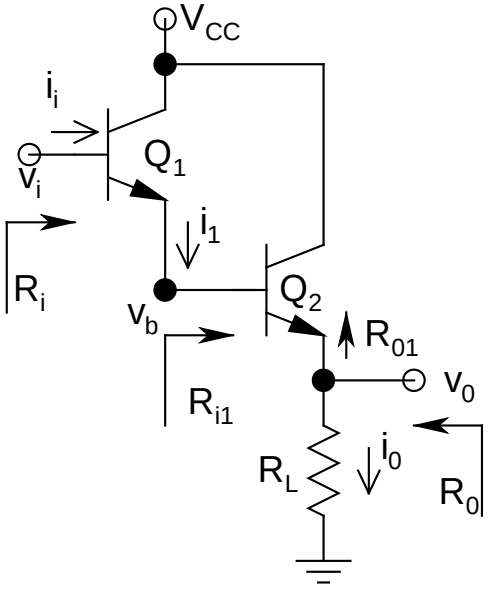
    $\Rightarrow$ ***MOS Darlington has no special use***



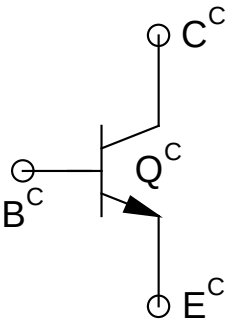
Generic Circuit



CC-CE Stage



CC-CC Stage



Compact Representation

- For ***DC biasing***:

$$I_{C2} = \beta_2 I_{B2} = \beta_2 I_{E1} \approx \beta_2 I_{C1}$$

$$\Rightarrow r_{\pi 2} = \beta_2 r_{E2} = \beta_2 V_T / I_{C2} = V_T / I_{C1} = r_{E1}$$