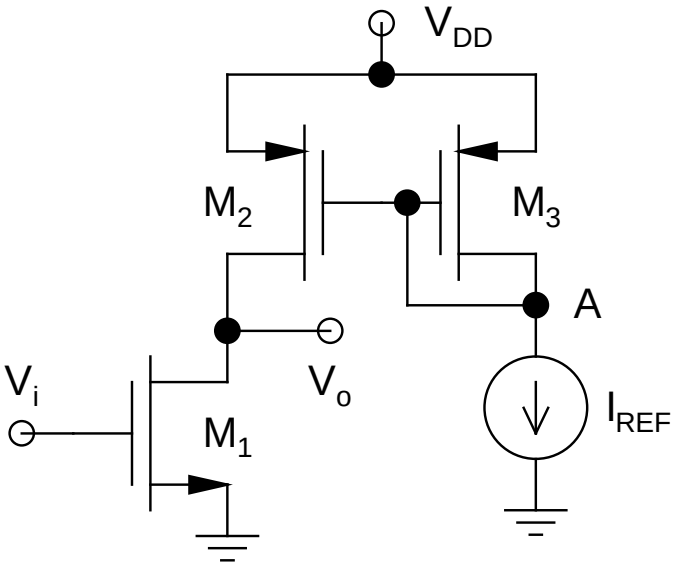
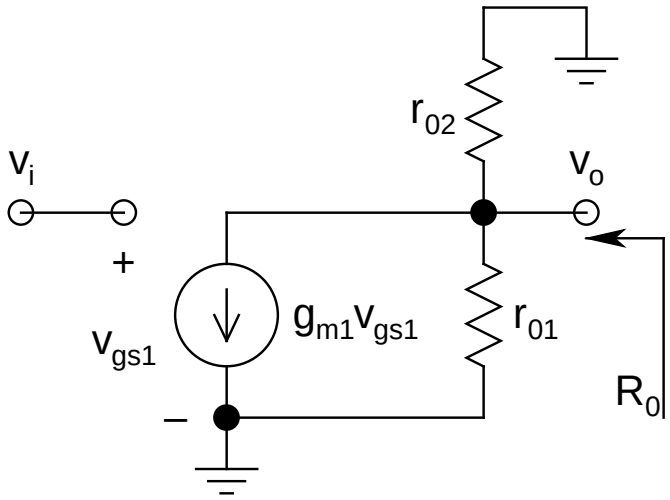




Circuit Schematic **ac Midband Equivalent**

- ***M_1 body connected to ground, M_2-M_3 bodies connected to V_{DD}***
  - *No body effect problem for any of the devices* (*biggest advantage of this circuit*)

- Identify M_2-M_3 as a ***PMOS current mirror*** (***perfectly matched***)

  $\Rightarrow I_{D1} = I_{D2} = I_{D3} = I_{REF}$

- This gives the ***required value*** of V_I

  $\Rightarrow$ ***DC biasing*** of the circuit is ***pretty straightforward***

- For ***ac analysis***, we note that ***node A*** is ***both open and short*** at the same time (similar to ***npn gain stage*** with ***pnp active load***)

  $\Rightarrow A_v = v_o/v_i = -g_{m1}R_0$

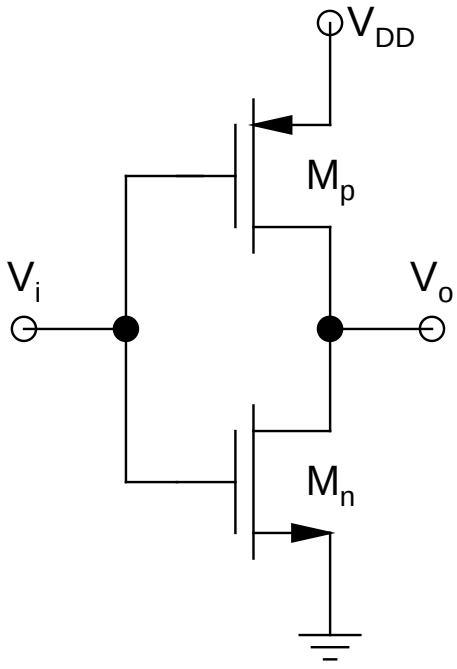
  R_0 $(= r_{01} \| r_{02})$: ***Output resistance*** of the circuit

- ***Caution***: $r_{01} \neq r_{02}$, even though M_1 and M_2 carry the same ***DC bias current***, since $\lambda_n \neq \lambda_p$ (in general)
- This circuit is ***immensely useful*** since it gives ***extremely large voltage gain and output resistance***
- Only ***problem*** is that it needs a ***PMOS current mirror***, thus necessitating use of an ***extra PMOS***
- An ***even better design*** exists, which ***eliminates*** the need for this ***extra PMOS***

- ***A Better CMOS Gain Stage***:
  - ***No body effect issue***
  - However, there are ***some design issues***
  - M_n-M_p have ***same magnitude*** of the ***threshold voltage***:

    $V_{TN0} = |V_{TP0}|$
  - ***Process transconductance parameters***:

    $k'_N = \mu_n C'_{ox}$ and $k'_P = \mu_p C'_{ox}$



Circuit Schematic

- ***Oxide capacitance per unit area*** $\left(C'_{ox} = \varepsilon_{ox} / t_{ox}\right)$ ***same for both devices***, since they have ***same*** t_{ox}
- However, $\mu_n \sim 2\mu_p$ (***for Si***)
- Thus, $k'_N = 2k'_P$
- ***Ideal DC bias point*** of the circuit is $V_I = V_0 = V_{DD}/2$ (yields $V_{GSn} = |V_{GSp}|$ and $V_{DSn} = |V_{DSp}|$)
- Can be achieved only if the stage is ***completely balanced*** (***same threshold voltage magnitude*** and ***same device transconductance parameter***)
- Thus, k_N ***and*** k_P ***need to be matched***

- ***Can be achieved by making $(W/L)_p = 2(W/L)_n$***
- If ***CLM effect*** is ***not that important***, or if $\lambda_n = \lambda_p$, then this procedure works out ***just fine***
- However, if $\lambda_n \neq \lambda_p$, then for ***balancing the circuit***, the following relation ***must hold*** (***show***!):

  $k_P(1 + \lambda_p V_{DD}/2) = k_N(1 + \lambda_n V_{DD}/2)$
- Under this condition, $k_N \neq k_P$, but the circuit will be ***perfectly matched and balanced***
- Known as: ***Stage unmatched by nature, but matched by performance***