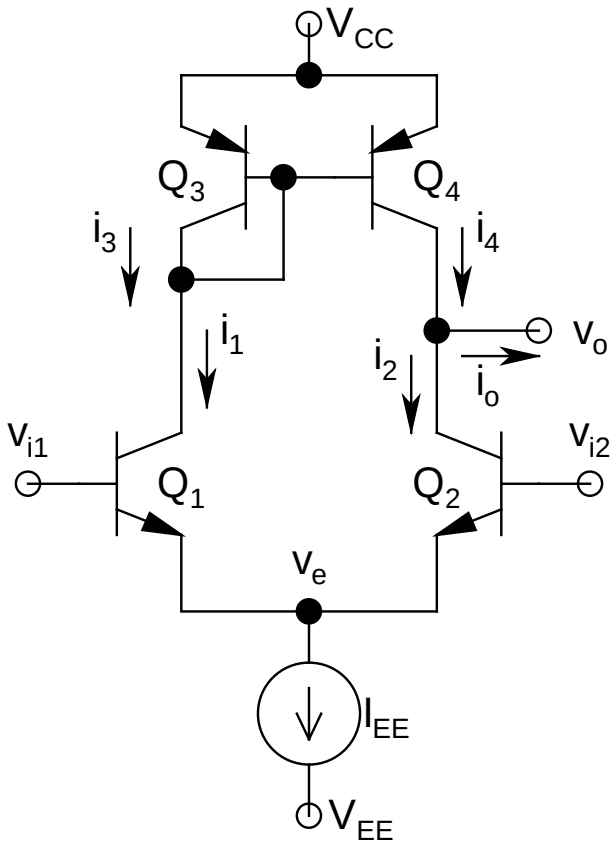
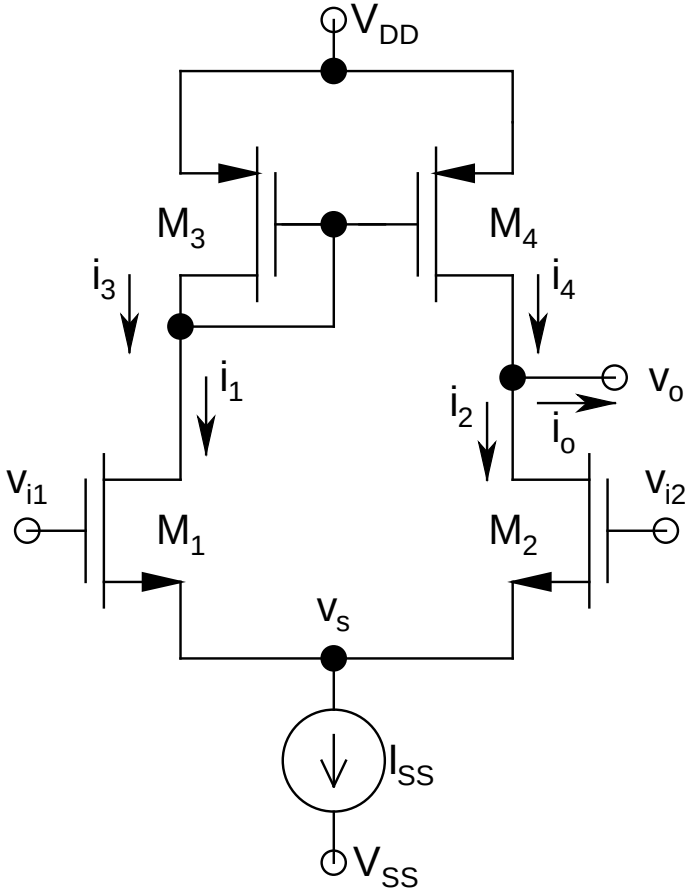
- ***Actively Loaded DA***:



BJT Implementation



MOS Implementation

- Absolutely ***similar topologies*** for ***both BJT and MOS implementations***
- ***Produces double-ended to single-ended conversion***, i.e., ***from two inputs to a single output***
- Q_1-Q_2/M_1-M_2/Q_3-Q_4/M_3-M_4 ***perfectly matched***
- ***Output should never be taken from collector/drain of*** Q_1/M_1 (***Why***?)
- ***DC biasing*** is ***absolutely straightforward*** with ***all branch currents equal to*** $I_{EE}/2$ ***or*** $I_{SS}/2$

- ***Caution***: ***Half-circuit technique can't be used for this circuit***, since ***collector/drain circuits of the two sides are coupled***, i.e., $i_3 = i_4$ (***always***)
- This circuit can be ***analyzed by inspection***
- ***Define*** $v_{id} = v_{i1} - v_{i2}$
- ***Apply*** $+v_{id}/2$ ***at the base of*** Q_1***/gate of*** M_1
- ***Apply*** $-v_{id}/2$ ***at the base of*** Q_2***/gate of*** M_2
- From ***symmetry*** of the circuit ***around the BE/GS loops***, the ***common emitter/source node*** is at ***ac ground*** (i.e., $v_e = v_s = 0$)

- Since $v_s = 0$, M_1-M_2 *won't have any body effect issue*
- Now, $i_3 = i_4$ (*mirror*), $i_3 = i_1$ (*same branch*), and $i_2 = -i_1$ (*symmetry*)
- Also, $i_1 = g_m v_{id}/2$ and $i_2 = -g_m v_{id}/2$

  $g_m = I_{EE}/(2V_T)$ (*BJT Implementation*)

  $= (k_N I_{SS})^{1/2}$ (*MOS Implementation*)
- Hence, the *short-circuit output current* (with the *output terminal shorted to ground*):

  $i_o = i_4 - i_2 = i_1 - i_2 = 2i_1 = g_m v_{id}$

- To find the ***output voltage***, we need to use the ***Thevenin technique***:
  - ***Open-Circuit Voltage*** = ***Short-Circuit Current*** × ***Thevenin Resistance***
- ***Thevenin Resistance*** (***looking from the output***):

  $R_0 = r_{02} \| r_{04}$
- Thus, the ***output voltage***:

  $v_o = i_o R_0 = g_m (r_{02} \| r_{04}) v_{id}$
- Hence, the ***differential-mode gain***:

  $A_{dm} = v_o / v_{id} = +g_m (r_{02} \| r_{04})$
- $R_i = 2r_\pi$ (***BJT Implementation***)

- ***Ex.***: ***Prove the expressions for A_{dm} and R_i from the hybrid-π model***
- ***A_{cm} for this circuit is a little difficult to evaluate***
- However, the ***CMRR can be safely approximated as***:

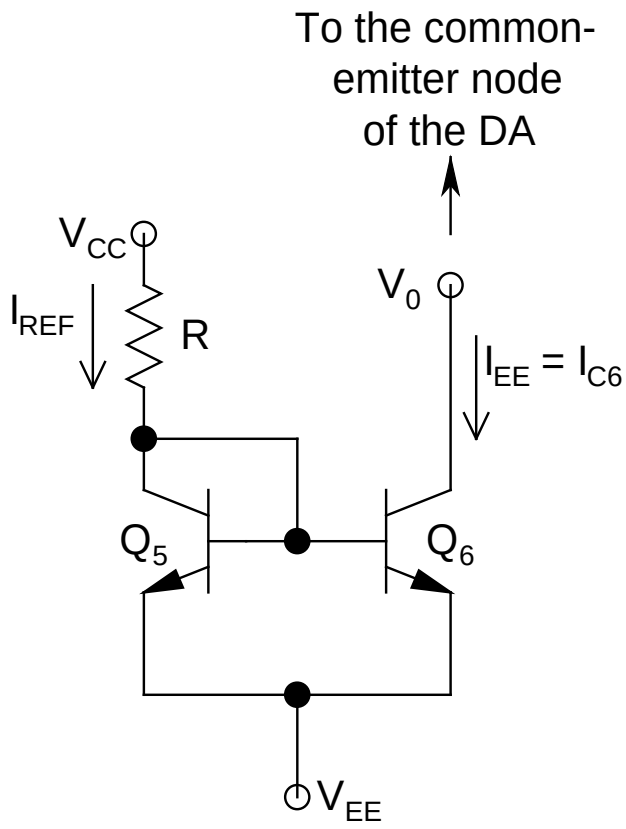
  $$CMRR \approx 20\log_{10}(2g_m R_{EE})$$

  R_{EE}: ***Output resistance of the bias current source I_{EE}/I_{SS}***
- In order to ***improve CMRR***, various ***current source topologies*** can be used

- ***Example***: ***Simple npn CM***
  - ***One of the simpler choices***
  - ***Q_5-Q_6 perfectly matched***
  - ***Neglecting base currents***:

    $I_{REF} = I_{EE} = I_{C6}$

    $= (V_{CC} - V_{BE} - V_{EE})/R$
  - $R_{EE} = r_{06} = V_A/I_{EE}$
  - Acts as a ***current source*** of ***magnitude I_{EE}*** with a shunt ***resistance R_{EE}***



- ***Insights***:
  - ***Recall***: A_{dm} ***independent of*** R_{EE}, but A_{cm} ***and CMRR strongly depend on*** R_{EE}
  - ***To maximize CMRR***, R_{EE} ***should be increased as much as possible***
  - ***To increase*** R_{EE}, other ***current sources*** discussed in class, e.g., ***ratioed mirror***, ***cascode***, ***Widlar***, etc., can be used
  - Note that with ***more advanced architectures***, V_0***(min) increases***, and may become a ***limiting factor***!