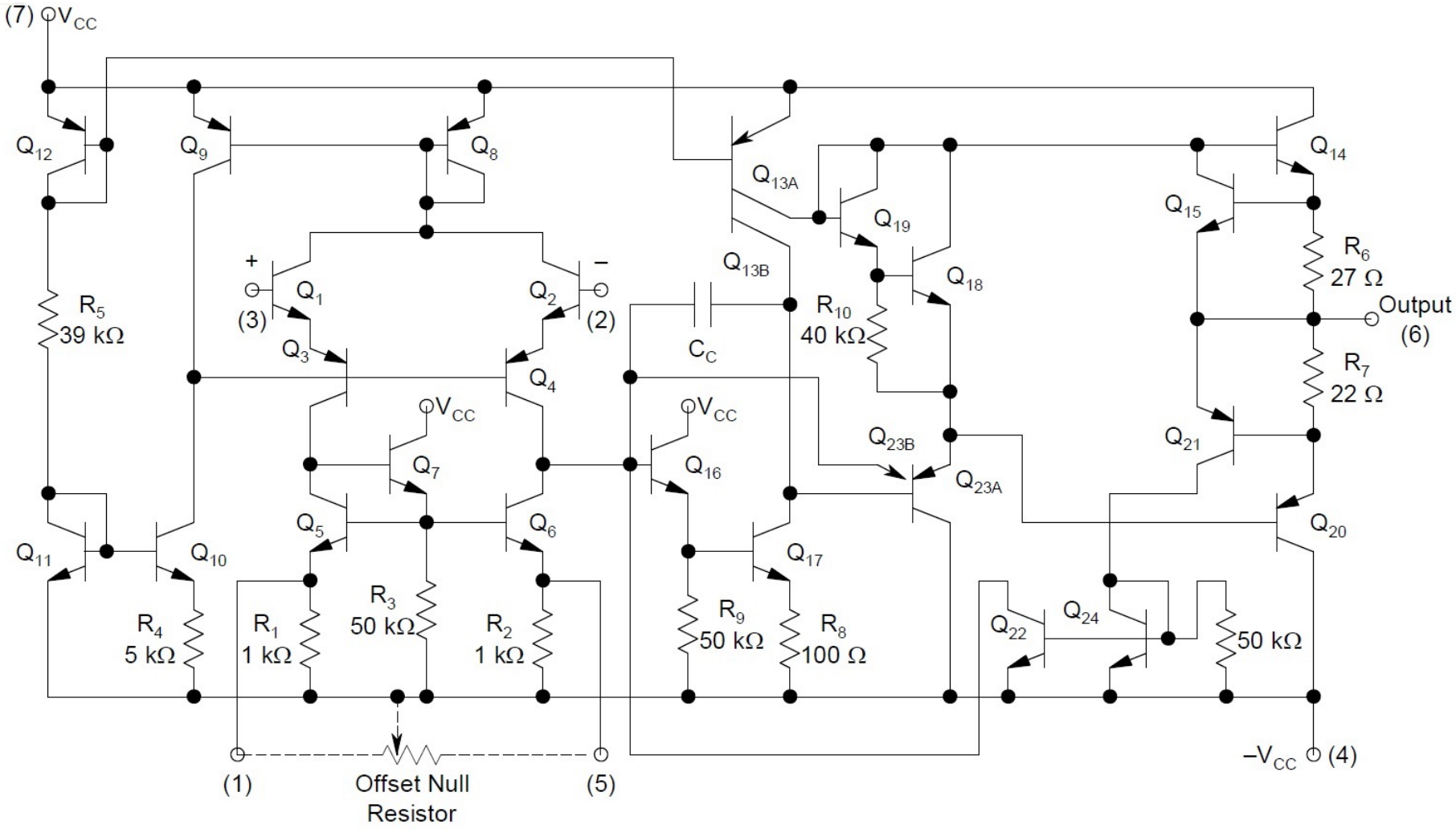
- V_1, V_2, and V_0 are measured ***w.r.t. ground***, but V_i is a ***floating signal*** (***difference*** between V_1 and V_2)
- The ***controlled source*** in the ***MacroModel*** is ***VCVS***
- For $V_1 > (<) V_2$, V_0 is ***positive*** (***negative***)
- ***Typical values for 741 op-amp***:
  - $A_{vOL} \sim 10^5$ (***100 dB***), $R_i >$ ***1 MΩ***, $R_0 <$ ***100 Ω***, CMRR ~ ***80-100 dB***, V_S+ and V_S–: ***±3 V to ±15 V***

- ***Uncompensated bandwidth*** typically ***larger than 1 MHz***
- Such a ***large gain*** and ***high bandwidth*** system will be prone to ***oscillations*** (***instability***)
- Need adequate ***compensation***
  - ***Compensated bandwidth*** drops to about ***5-10 Hz***

- ***History of 741 Op-Amp***:
  - In ***1965***, ***Bob Widlar*** (remember ***Widlar current source***?) of ***Fairchild Semiconductors*** (now defunct) first came up with the design of a ***monolithic*** (***single substrate IC***) ***op-amp***

- Named it ***μA 709*** (***μA*** was the ***trademark*** of ***Fairchild Semiconductors***)
- Almost immediately thereafter, ***a number of improvements*** were made on the ***original architecture***, and ***μA 741*** evolved
- It became so ***popular*** that ***the term 741*** became a ***legend***
- ***All subsequent op-amp designs continued to be called 741***!
- ***Initial design*** of course was based on ***bipolar technology***, since at that time, ***MOSFETs were not even there***!

- In ***late 70s***, ***JFET version*** of op-amps came into existence, followed by the ***MOSFET version*** in the ***80s***
- The ***design pedagogy*** of the ***original version*** is a ***real beauty***
- So many ***brilliant innovations*** were ***incorporated*** in the ***design***, that it is a ***learner's paradise***!
- In this chapter, we will do a ***detailed analysis*** of the ***bipolar version*** of the ***741 op-amp***
- So, sit tight and enjoy! :)



The schematic of the 741 bipolar op-amp (the pin numbers of the 741 chip is shown in parantheses).

- ***Steps of the Analysis***:
  - First, we need to do the ***DC analysis***
  - For this, we need to find the ***reference branch***
  - This branch should be from ***rail-to-rail*** (i.e., ***between the two power supplies***)
  - It should encounter only ***base-emitter junctions*** and ***resistors***

    $\Rightarrow$ The branch Q_{11}-Q_{12}-R_5 is our ***reference branch***
  - ***The DC current flowing through this branch fixes the DC bias current of all other branches***