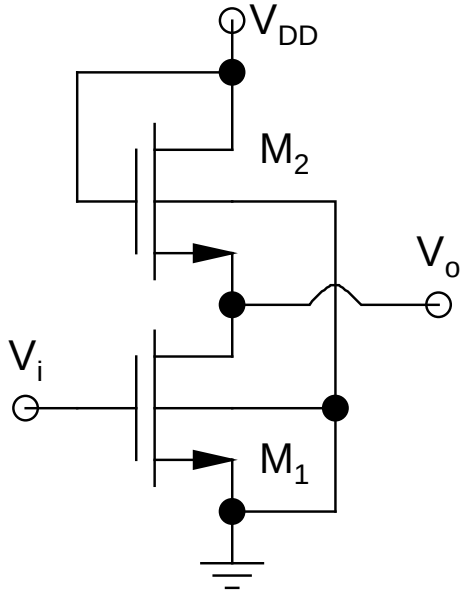
- ***Variants of Actively Loaded CS Stage***:
  - ***Saturated Enhancement Load***
  - ***Depletion Load***
  - ***Complementary PMOS Load***
    - Also known as ***CMOS Gain Stage***
- ***The last one is the most popular***

- ***Saturated Enhancement Load***:
  - ***Both bodies tied to ground***
    - ***For M_1: $V_{SB1} = 0$***
    - ***For M_2: $V_{SB2} = V_o$***
  - ***M_2 is enhancement mode***
    - ***V_{TN02} positive***
  - ***M_2 is also diode-connected***
    - ***Always operates in saturation***
  - ***M_2 has a floating body effect***



Circuit Schematic

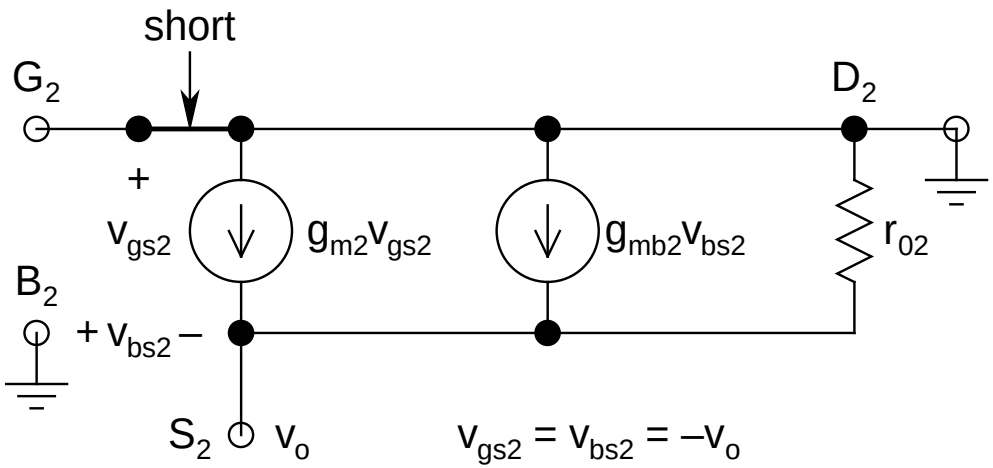
problem: ***V_o is a variable*** and ***V_{TN2} will continuously change with a change in V_o***

- ***For M_2 to remain on, its V_{GS2} ($= V_{DD} - V_o$) must be $> V_{TN2}$***
- Thus, there is a ***maximum possible V_o***, beyond which ***it cannot rise*** (***M_2 would cut off***)
- To estimate this ***maximum V_o***, for the time being, ***neglect that $3V_T$ cushion***
- Then:

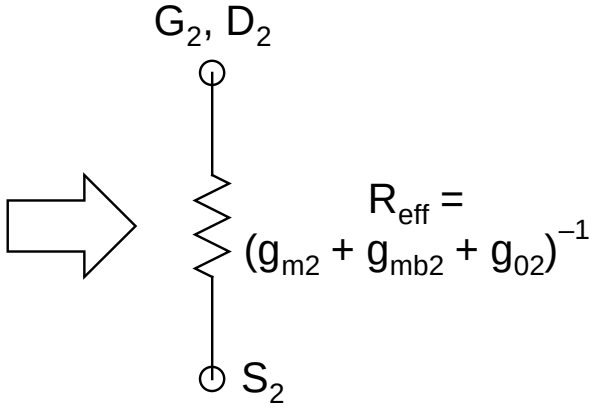
$$V_{DD} - V_{o,max} > V_{TN2} \text{ (}\textit{with } V_{SB2} = V_{o,max}\text{)}$$

$$V_{TN2} = V_{TN02} + \gamma\left(\sqrt{2\phi_F + V_{o,max}} - \sqrt{2\phi_F}\right)$$

- ***Solution of this equation would give $V_{o,max}$***
- ***Once $V_{o,max}$ is obtained***, the ***best bias point would be at $V_0 = V_{o,max}/2$***
- Before doing ***ac analysis***, ***let's investigate M_2***:



ac Midband Equivalent of M_2



Simplified Equivalent