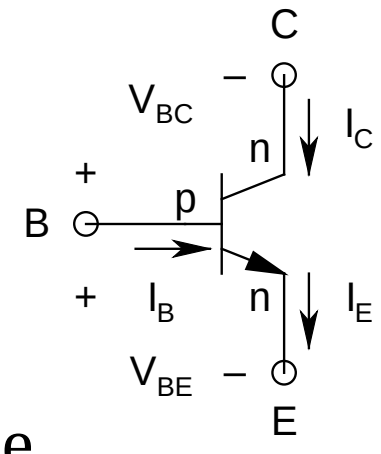
Bipolar Junction Transistors (BJTs)

- Basically two ***back-to-back diodes***
- Immensely important device
- Name originates from ***Transfer of Resistor***
- ***Three-Layer/Terminal*** [***Emitter*** (E), ***Base*** (B), ***Collector*** (C)] ***Two-Junction*** [***Base-Emitter*** (BE), ***Base-Collector*** (BC)] device
- Current through two terminals (E and C) can be ***controlled*** by the current through the third terminal (B)

- ***Active device*** $\Rightarrow$ capable of producing ***voltage/current/power gain***
- ***Two basic usage***:
  - **Amplification** (***Analog Circuits***)
  - **Switching** (***Digital Circuits***)
- ***Two types***: **npn** and **pnp**
- We will be discussing only npn BJTs
- ***Bipolar***: both ***electrons*** and ***holes*** contribute to ***current transport*** through the device
- ***Current controlled device***

Symbol and Current/Voltage Convention:

* For an ***npn*** transistor, the ***collector and base currents*** (I_C and I_B respectively) ***flow in*** and the ***emitter current*** (I_E) ***flows out*** of the transistor



  $\Rightarrow$ Applying KCL, treating the whole of the transistor as a ***big node***:

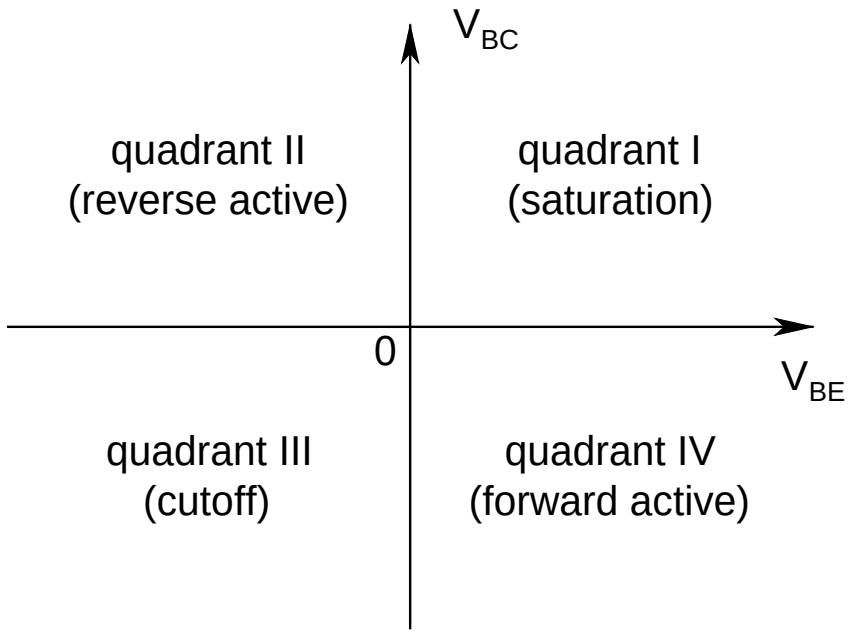
  $I_E = I_C + I_B$

* E and C are ***n-type***, while B is ***p-type***

* Note the ***notational convention*** of the applied voltages (V_{BE} and V_{BC}) – ***p-side first***

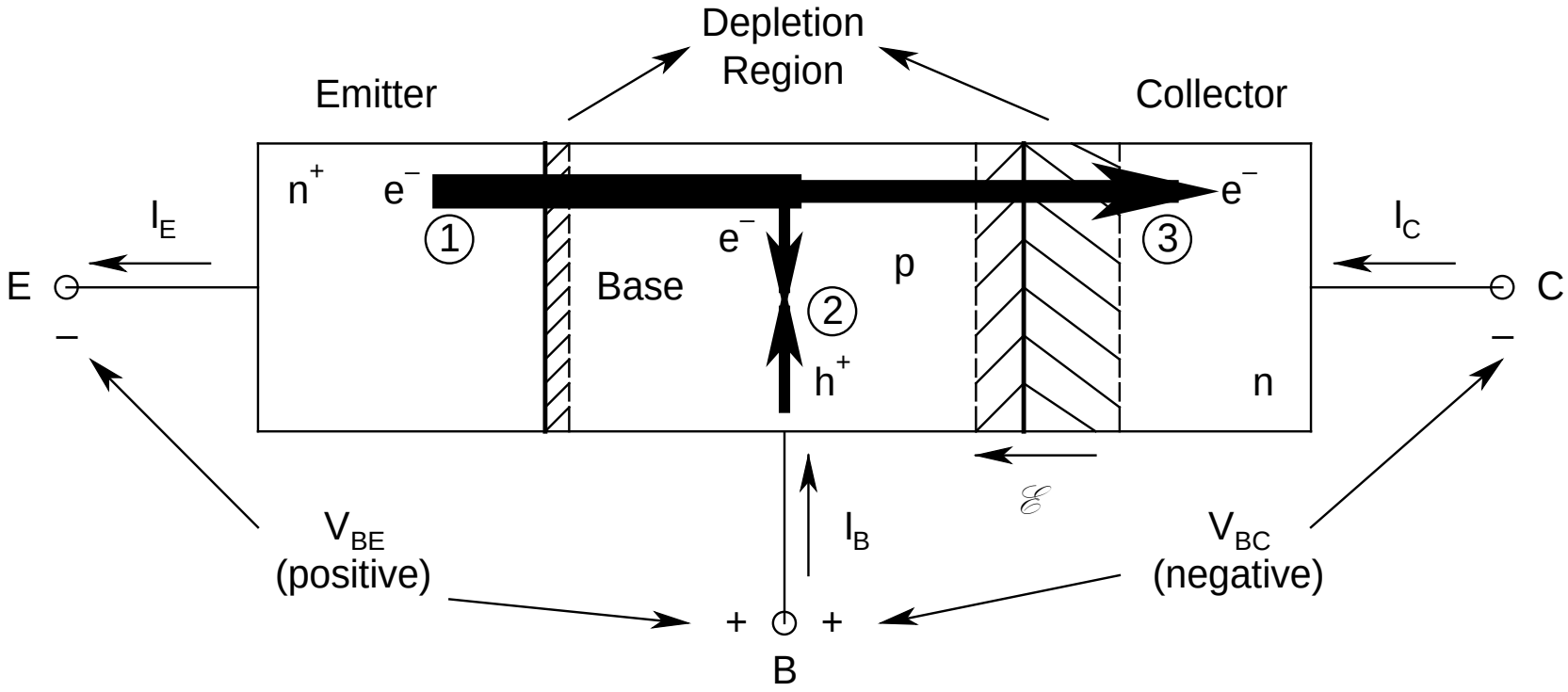
Modes of Operation:

* ***BE*** and ***BC*** junctions can either be ***forward*** or ***reverse*** biased $\Rightarrow$ ***4 possible modes of operation***
  - **Forward Active**: ***BE junction forward biased***
    BC junction reverse biased
  - **Reverse Active**: ***BE junction reverse biased***
    BC junction forward biased
  - **Saturation**: ***Both junctions forward biased***
  - **Cutoff**: ***Both junctions reverse biased***



Quadrants III and IV: Analog Domain
Quadrants I and III: Digital Domain
Quadrant II: Finds use only in TTL circuits

Operation in the Forward Active (FA) Mode:



① Injection Component

② Recombination Component

③ Collection Component

* **BE junction forward biased**: ***electrons injected from E to B***, thus ***emitter current (I_E) flows out of the emitter terminal***
* In B, electrons ***diffuse*** towards the ***BC junction*** due to the presence of ***diffusion gradient***
  Note: ***electrons*** are ***minority carriers*** in ***p-base***
* In this process, some electrons will ***recombine*** with the ***majority carriers*** (***holes***) present in B
* The holes ***lost*** due to this ***recombination process*** will be ***supplied*** by the ***external circuit***, thus, ***base current (I_B) flows into the base terminal***

* Electrons, which did not recombine, will reach the edge of the BC depletion region, and will get swept to C by the ***junction electric field***
* Thus, ***collector current (I_C) flows into the C terminal***
* ***A small change in I_B can cause a large change in I_C to I_E ratio***, due to a phenomenon known as **base control**
* For a ***good*** transistor, ***I_B should be as small as possible $\Rightarrow$ the base region should be as thin as possible***

Current Gain:

* Note that the ***sum of the collection component and the recombination component must always equal the injection component*** (**charge conservation**)

  $\Rightarrow I_E = I_C + I_B$

* ***Common-Emitter Current Gain*** $(\beta) = I_C / I_B$

* ***Common-Base Current Gain*** $(\alpha) = I_C / I_E$

* Thus, $\boldsymbol{\beta = \alpha / (1 - \alpha)}$ and $\boldsymbol{\alpha = \beta / (\beta + 1)}$

* For a ***good*** transistor, $\boldsymbol{I_B}$ ***should be as small as possible*** $\Rightarrow$ $\boldsymbol{\alpha \to 1}$, and **β is quite large** (~***100-500***)

* ***Closer is the value of α to 1, better is the BJT***!

Current-Voltage Characteristic:

* Note that ***BE junction basically is a diode***

$$\Rightarrow I_E = I_{ES}\left[\exp\left(V_{BE}/V_T\right)-1\right] \simeq I_{ES}\exp\left(V_{BE}/V_T\right)$$

$\because$ ***BE junction is sufficiently forward biased***

$\therefore$ The ***-1 term can be neglected***

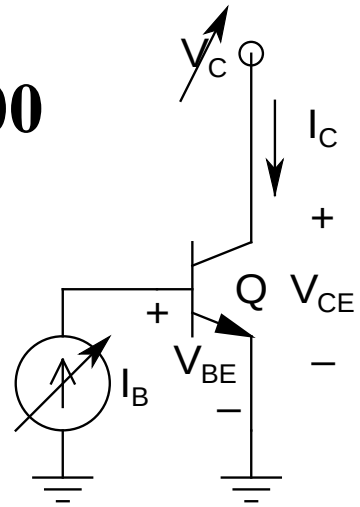
- I_{ES}: Reverse saturation current of the BE junction
- V_T: ***Thermal Voltage*** $(= kT/q) =$ ***26 mV at room temperature*** $(\mathbf{T = 300\ K})$

* Thus, $I_C = \alpha I_E = I_S \exp\left(V_{BE}/V_T\right)$

- $I_S = \alpha I_{ES} =$ ***saturation current of the BJT***
- $I_B = I_E - I_C$

Output Characteristic:

* ***Note***: $V_C = V_{CE}$ (variable), also I_B is variable
* When BJT is in the ***forward active*** mode, ***V_{BE} is assumed to get clamped at 0.7 V*** **(about 100 mV above V_γ)** $\Rightarrow$ ***Thumb rule***
* Now, $V_{CE} = V_{BE} - V_{BC}$
* Thus, for all values of ***$V_{CE} > 0.7\,V$***, ***V_{BC} is negative***, implying the ***BC junction remains reverse biased***, and ***forward active operation is maintained***



* *For* $V_{CE} = 0.7\,V, V_{BC} = 0$

  $\Rightarrow$ *BC junction is neither forward nor reverse biased* – **it is actually under zero bias**

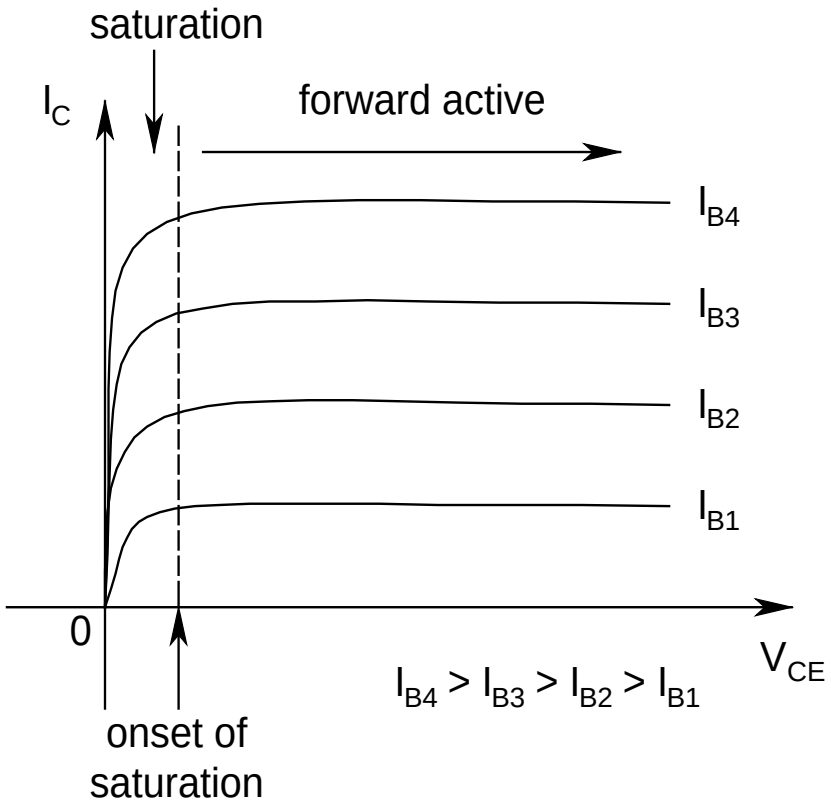
* *As soon as* V_{CE} *drops below* $0.7\,V$, V_{BC} *changes sign and becomes positive*

  $\Rightarrow$ **BC junction is now forward biased, and forward active mode of operation is lost**

  $\Rightarrow$ **BJT enters saturation mode of operation, with both junctions forward biased**

  $\Rightarrow$ $V_{CE} = 0.7\,V$ *is known as* **onset of saturation**

* ***Once V_{CE} drops below 0.7 V, the BJT enters the saturation mode of operation***
* ***With further reduction in V_{CE}, the BJT moves deeper into saturation***
  - $\Rightarrow$ This is the ***mode of operation of BJTs for digital circuits***, however, ***BJTs used in analog circuits should never ever enter this mode of operation***
  - $\Rightarrow$ $\therefore$ ***A quick check is needed to ensure that V_{CE} is greater than 0.7 V in analog circuits***



npn BJT Output Characteristic

Why V_{BE} = 0.7 V?:

* ***Note***: **I_E (and thus I_C) varies exponentially with respect to V_{BE}**

  $\Rightarrow$ ***A small change in V_{BE} can cause a very large change in I_C***

* ***As a rule of thumb, V_{BE} under the forward active mode is assumed to get*** **pinned** ***at 0.7 V***

  $\Rightarrow$ **This is a heuristic used for quick estimate**

  $\Rightarrow$ The answer may not be accurate, however, good enough!

Degree of Saturation (DoS):

* *In saturation, BC junction also becomes forward biased and collector starts injecting electrons to base*
* *The base gets flooded with minority carriers (electrons), with a corresponding increase in recombination, and thus, the base current ($I_{B,sat}$)*
* *Note that at the same time, the collector current ($I_{C,sat}$) starts to drop due to this reverse injection process*
* **The net effect is a drop in β** $\Rightarrow$ *in the saturation region, β is denoted by* β_{sat} $(= I_{C,sat} / I_{B,sat})$, *and has a value smaller than that in the FA region*

* $DoS \triangleq \frac{\beta}{\beta_{sat}}$, and ***has a value*** ≥ 1

* ***Note***: **At onset of saturation, DoS = 1, and as the BJT is driven deeper and deeper into saturation, the value of DoS keeps on increasing**

* ***The value of DoS is a tell-tale sign of judging how deeply the transistor is driven into saturation***

* ***Commonly used values***: $V_{BE(FA)} = 0.7\ V$, $V_{CE(FA)} > 0.7\ V$, $V_{CE(OS)} = 0.7\ V$, $V_{CE(HS)} = 0.1\ V$, $V_{BE(HS)} = 0.8\ V$

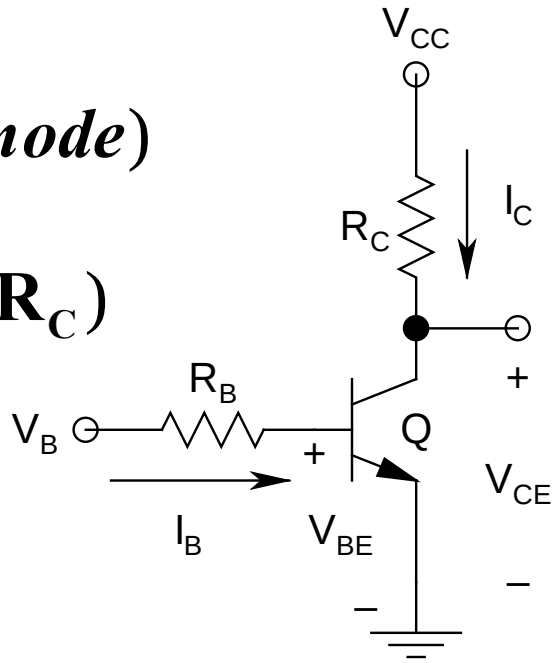
  OS **:** ***Onset of Saturation***, ***HS*** **:** ***Hard Saturation***

Load Line Analysis:

* $I_B = \dfrac{V_B - V_{BE}}{R_B}$, with $V_{BE} = 0.7$ V (***FA mode***)

* Also, $I_C = \beta I_B$ (***Note***: **Independent of R_C**)

* Thus, for different values of V_B, we would get different values of I_B, and correspondingly different values of I_C



$\Rightarrow$ A series of ***output characteristics*** (i.e., I_C versus V_{CE}) can be drawn

* The ***DC operating point*** or the ***Q-point*** can lie ***anywhere*** on any of these curves

* Also, by varying V_B ***smoothly***, almost a ***continuous*** variation of I_B can be obtained, which would yield almost ***continuous*** values of I_C
* ***Thus, the output characteristics, in effect, completely fill up quadrant I***
* Now, to fix a ***unique bias point***, we need to draw the ***load line***, and the ***intersection point*** of this load line with the particular characteristic for a given V_B and I_B would give us the information about the ***Q-point***
* ***Load line equation***: $I_C = \dfrac{V_{CC} - V_{CE}}{R_C}$

* ***2 boundary points***:
  - $I_C = 0,\ V_{CE} = V_{CC}$
  - $V_{CE} = 0,\ I_C = V_{CC} / R_C$
* Joining these two points by a ***straight line*** gives the ***load line***
* This line will ***intersect*** with the output characteristics at ***infinite*** number of points
* **Each of these points is a possible operating point**
* **The best choice for the operating point (or Q-point) is right at the center of the load line**:

$$\Rightarrow V_{CEQ(best)} = V_{CC}/2 \text{ and } I_{CQ(best)} = V_{CC}/(2R_C)$$

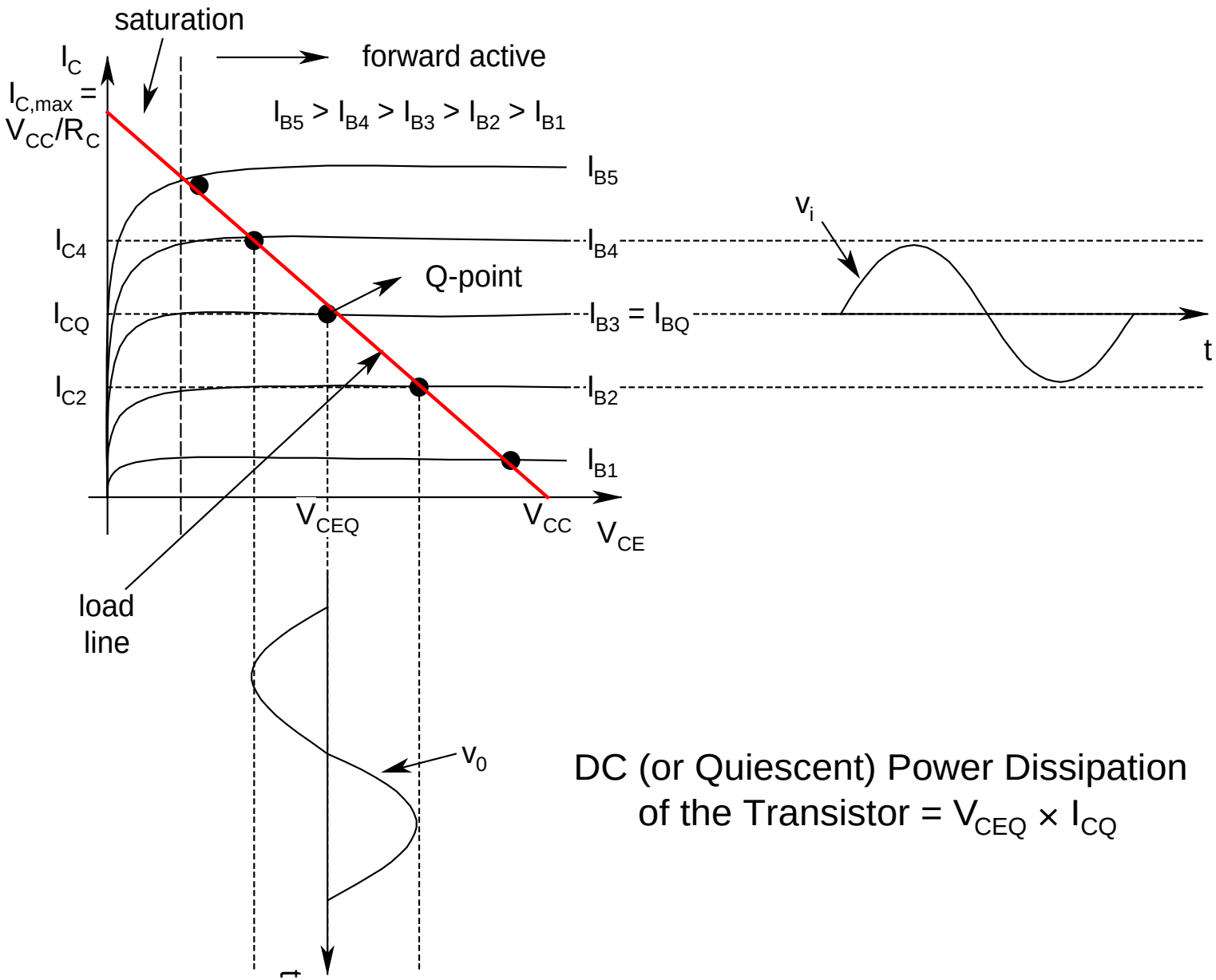
* ***Justification***:

- When this circuit is to be used as an ***amplifier***, then an ***ac small-signal*** v_i will be ***superimposed*** on the ***DC bias voltage*** V_B
- This would cause the ***dynamic operating point*** to ***move along the load line in either direction***
- **As it shifts towards the V_{CE} axis, Q moves towards cutoff $\left(\text{since } I_C \text{ decreases}\right)$, and as it moves towards the I_C axis, Q moves towards saturation $\left(\text{since } V_{CE} \text{ decreases}\right)$**

- **If Q enters either cutoff or saturation region, then it would produce clipping (or distortion) in the output voltage v_0**

$\Rightarrow$ ***If the Q-point is located exactly at the center of the load line, then the maximum possible undistorted peak-to-peak swing of the output voltage v_0 will be achieved***

$\Rightarrow$ **Golden Rule of Thumb for BJT biasing**



DC (or Quiescent) Power Dissipation of the Transistor = $V_{CEQ} \times I_{CQ}$

What is the Role of R_C?:

* For fixed V_B (and thus, I_B):
  - As R_C decreases, $I_{C,max}$ will increase

    $\Rightarrow$ Q moves towards ***cutoff***

    $\Rightarrow$ v_0 will get ***clipped*** during ***positive half cycle***
  - As R_C increases, $I_{C,max}$ will decrease

    $\Rightarrow$ Q moves towards ***saturation***

    $\Rightarrow$ v_0 will get ***clipped*** during ***negative half cycle***
  - In either of these two cases, the range of the ***maximum undistorted peak-to-peak output voltage swing*** will be correspondingly reduced

Observations:

* If R_C is ***very high***, then the load line may not have any intersection point at all with the output characteristics under the FA region, and the Q-point will move to the ***saturation region***

  $\Rightarrow$ ***Disastrous way to bias a transistor for analog circuit applications***

* A transistor biased in the ***FA region*** behaves like an ***ideal current source*** with ***infinite output resistance***

* However, if a transistor is biased in the saturation region, it ceases to behave like a constant current source

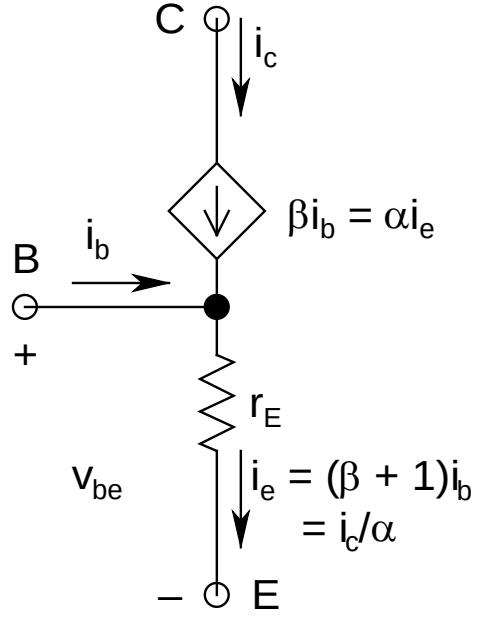
* In the saturation region, I_C becomes a strong function of V_{CE}, showing ***very small output resistance***
* Transistors used in analog circuit applications like ***amplifiers***, should always be biased in the ***FA region***, where I_C does not show any dependence on V_{CE}

  $\Rightarrow$ ***I_{CQ} would not change with any variation of V_{CE}***
* This is important to maintain ***constant*** values of all the ***ac small-signal model parameters*** (to be discussed)
* If I_{CQ} varied with V_{CE}, then the behavior of the circuit would become ***erratic***

AC Small-Signal Model:

* Representation of the transistor as a ***linear network***
* Actual model is quite tedious and complicated
* Here, we will present the ***simplest one***, known as the **low-frequency T-model**
* It consists of ***only 2 parameters***:
  - β (or α): ***Common-Emitter*** (or ***Common-Base***) ***Current Gain***
  - r_E: ***Incremental Emitter Resistance***

$$\triangleq dV_{BE}/dI_E = V_T/I_{EQ} \simeq V_T/I_{CQ} \ (\because \alpha \to 1)$$



* ***Note***: r_E is expressed in terms of I_{CQ} (or I_{EQ})

  $\Rightarrow$ ***The linearization is done around the DC bias point*** (**Q-point**)

  $\Rightarrow$ $\therefore$ ***DC analysis must precede ac analysis*** in order to obtain the ***bias point information***, and thus, ***the value of*** r_E

* Also, note the $v_{be} = i_e r_E$, which can also be written as: $v_{be} = (\beta+1) i_b r_E \simeq \beta i_b r_E = i_b r_\pi$, with $r_\pi = \beta r_E$

  $\Rightarrow$ r_π is another ***small-signal parameter***, defined as ***incremental base-emitter resistance***

  $\Rightarrow$ ***Note that this resistance appears in the base lead***

Analysis of Amplifiers Using Transistors:

* The analysis proceeds as follows:

  - First, ***DC biasing analysis*** is done, which yields the ***DC bias point*** (**Q-point**)

    $\Rightarrow$ Gives I_{CQ} and V_{CEQ}

  - I_{CQ} is needed to obain the values of the ***small-signal parameters***

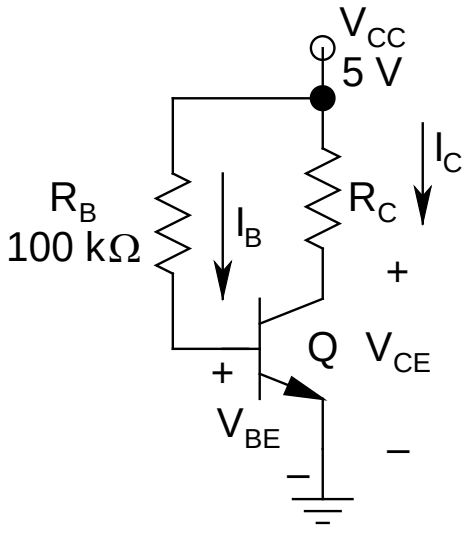
  - V_{CEQ} is needed to ensure that the transistor is biased in the ***FA region*** ($V_{CEQ} > 0.7$ V, and ideally $V_{CC}/2$, known as the **best bias point**)

* Then, the transistor is replaced by its ***ac small-signal model***
* Subsequently, ***usual network analysis*** is done to obtain:
  - ***Voltage Gain*** (A_v)
  - ***Current Gain*** (A_i)
  - ***Power Gain*** $(A_p = |A_v \times A_i|)$
  - ***Input Resistance*** (R_i)
  - ***Output Resistance*** (R_0)

Biasing:

* Fixing the ***DC operating point*** (known as the ***Q-point*** or ***Quiescent Operating Point***)
* Defined by two parameters: I_{CQ} and V_{CEQ}, with the subscript Q denoting the ***Q-point values***
* If the transistor is to be used as an ***amplifier*** (**analog application**), then it must be biased in the ***FA region***
* On the other hand, if the transistor is to be used as a ***switch*** (**digital application**), then it must ***toggle between cutoff and saturation modes of operation***

***Example*: Fixed Resistor Bias:**



To start the DC bias analysis, assume that Q is in the FA region, with $V_{BE} = 0.7$ V, and $V_{CE} > 0.7$ V

$$\Rightarrow I_{BQ} = \frac{V_{CC} - V_{BE}}{R_B} = \frac{5 - 0.7}{100\text{ k}} = 43\ \mu\text{A}$$

Now, to find I_{CQ}, we need the value of β

Let's assume $\beta = 100 \Rightarrow I_{CQ} = \beta I_{BQ} = 4.3$ mA

Note that to find I_{CQ}, we did not need the value of R_C

***This is true only if Q is in the FA region, where I_C is independent of R_C $\Rightarrow$* Extremely important observation**

Now, $V_{CEQ} = V_{CC} - I_{CQ}R_C$

Thus, ***R_C controls the value of V_{CE}***

Recall that $V_{CEQ(best)} = V_{CC}/2 = 2.5\ \text{V}$

$\Rightarrow$ Best value of $R_C = (2.5\ \text{V})/(4.3\ \text{mA}) = 581.4\ \Omega$

Note: For $R_C < 581.4\ \Omega$, V_{CEQ} would ***increase*** and Q would move towards ***cutoff***

On the other hand, if $R_C > 581.4\ \Omega$, V_{CEQ} would ***decrease*** and Q would move towards ***saturation***

The value of R_C to operate Q at ***onset of saturation***

$= (5 - 0.7)/(4.3\ \text{mA}) = 1\ \text{k}\Omega$

If the value of R_C is more than 1 kΩ, then Q will be driven into ***saturation***

As R_C increases, Q will go into ***deep*** (or ***hard***) ***saturation*** with $V_{CE(HS)} = 0.1$ V and $V_{BE(HS)} = 0.8$ V

The value of β will change to $\boldsymbol{\beta_{sat}}$, with ***DoS > 1***

Example: Let's visit the scene for $R_C = 10$ kΩ

Obviously, Q will be under ***hard saturation***

$$\Rightarrow I_{B,sat} = \left(V_{CC} - V_{BE(HS)}\right)/R_B = \left(5 - 0.8\right)/\left(100\text{ k}\right) = 42\ \mu\text{A}$$

$$I_{C,sat} = \left(V_{CC} - V_{CE(HS)}\right)/R_C = \left(5 - 0.1\right)/\left(10\text{ k}\right) = 490\ \mu\text{A}$$

$$\Rightarrow \beta_{sat} = I_{C,sat}/I_{B,sat} = 11.7 \text{ and } \boldsymbol{DoS} = \beta/\beta_{sat} = 8.6$$

How to Check the Mode of Operation?:

* Let's consider the same circuit with $R_C = 10\ k\Omega$, but now we assume that Q is in the FA region

  $\Rightarrow I_B$ and I_C remain at 43 μA and 4.3 mA respectively

* But, $V_{CEQ} = V_{CC} - I_{CQ}R_C = 5 - \left(4.3\ mA\right) \times (10\ k\Omega)$

  $= -38\ V!$

* Now, in a circuit with bias voltages ranging from ground (0 V) to V_{CC} (5 V), it is impossible to have a ***negative voltage*** at any node of the circuit

* Thus, the analysis is ***wrong***, and Q is ***NOT*** in the FA region, it's actually in ***hard saturation***!

Useful Information for Transistor Circuit Analysis:

* All ***pure*** ac voltages (i.e., without any DC offset) are ***DC short***, since their average value is zero
* All ***pure*** DC voltages are ***ac short***, since they don't have any time variation
* ***In DC analysis, open up all capacitors***
* ***In ac analysis, short all capacitors***
* ***In ac analysis, null all independent sources,*** **but don't touch dependent sources**

Amplifier Topologies:

* **4 basic topologies**:
  - CE (***Common-Emitter***)
  - CB (***Common-Base***)
  - CC (***Common-Collector***)
  - CE(D) [***Common-Emitter (Degeneration)***]
* **CE**:
  - ***Input at B, output from C, E grounded***
  - A_i ***large*** $(= \beta)$, $|A_v|$ ***moderate to large,*** A_p ***huge***
  - ***180° phase shift between input and output***

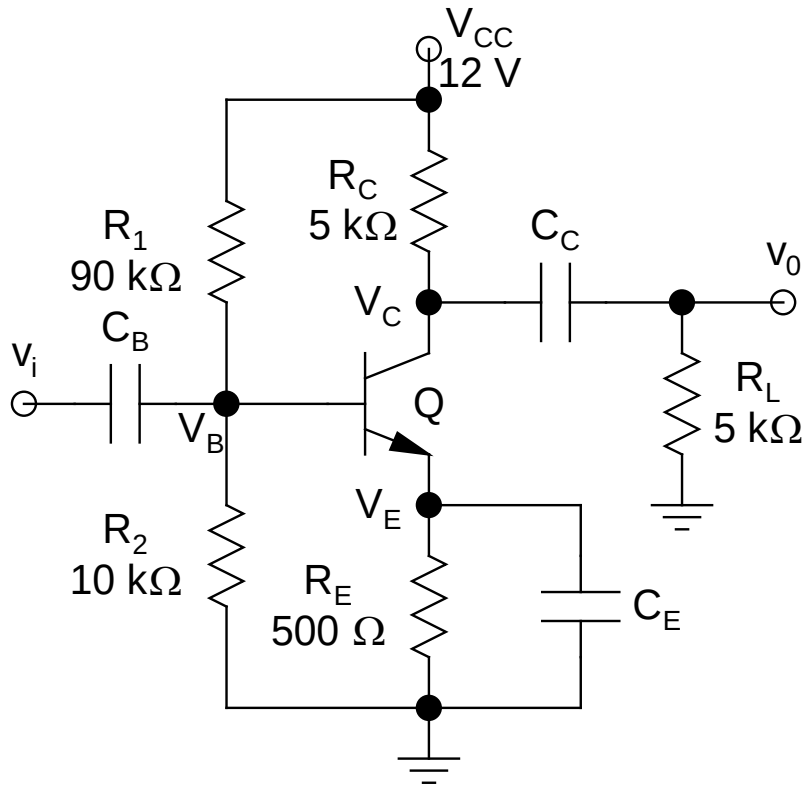
* **CB**:
  - ***Input at E, output from C, B grounded with or without a resistor***
  - $A_i \leq 1$ $(= \alpha)$, $|A_v|$ ***moderate***, A_p ***moderate***
  - ***Input and output in phase***
* **CC**:
  - ***Input at B, output from E, C connected either to ground (for negative supply circuits) or to the positive power supply with or without a resistor***
  - A_i ***large*** $(= \beta + 1)$, $|A_v| \leq 1$, A_p ***moderate***
  - ***Input and output in phase***

* **CE(D)**:
  - ***Input at B, output from C, E grounded through a resistor***
  - A_i ***large*** (= β), $|A_v|$ ***small***, A_p ***moderate***
  - ***180° phase shift between input and output***
  - This topology has an advantage in that it provides for an ***excellent frequency response***
* As an example, we will discuss a very important circuit block, known as ***RC-Coupled Amplifer***, which provides both current as well as voltage gain, and thus, ***large power gain***

RC-Coupled Amplifier:

* Extremely powerful analog circuit amplifier module

* Core circuit for ***audio amplifiers***



C_B: Base Blocking Capacitor
C_E: Emitter Bypass Capacitor
C_C: Collector Coupling Capacitor
All are high-value capacitors (> μF)
For DC Analysis: Treated as Open
For ac Analysis: Treated as Short

Purpose of the Capacitors:

* C_B: ***Base Blocking Capacitor***
  - Isolates the ac signal source from the circuit core
  - The DC level of the ac signal (i.e., the ***offset***) cannot affect the DC bias point of the circuit

* C_E: ***Emitter Bypass Capacitor***
  - Plays no role in DC analysis, since it opens up
  - For ac analysis, it shorts out R_E, putting the emitter of Q to ac ground

* C_C: ***Collector Coupling Capacitor***
  - Isolates the load resistance R_L from the circuit core such that it cannot alter the DC bias point

DC Analysis:

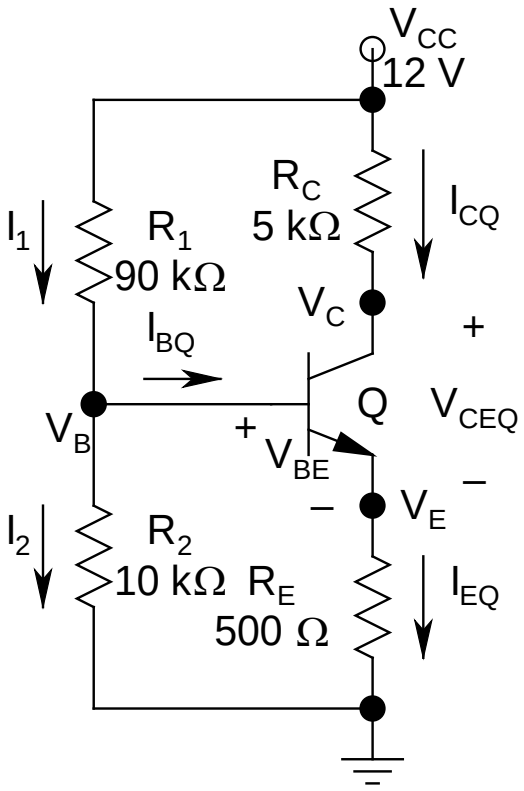
* ***All capacitors open up***

* Note that typical value of β is $\geq$ 100, thus, I_B is a miniscule fraction of I_C

  $\Rightarrow \boldsymbol{I_E \simeq I_C}$

* Also, $I_2 = I_1 - I_{BQ}$

* R_1 and R_2 are chosen in such a way that $I_1 \gg I_{BQ} \Rightarrow I_2 \simeq I_1$



* Thus, $V_B = R_2 V_{CC} / (R_1 + R_2) = 1.2$ V

  $\Rightarrow V_E = V_B - V_{BE} = 0.5$ V and $I_{EQ} \simeq I_{CQ} = V_E / R_E = 1$ mA

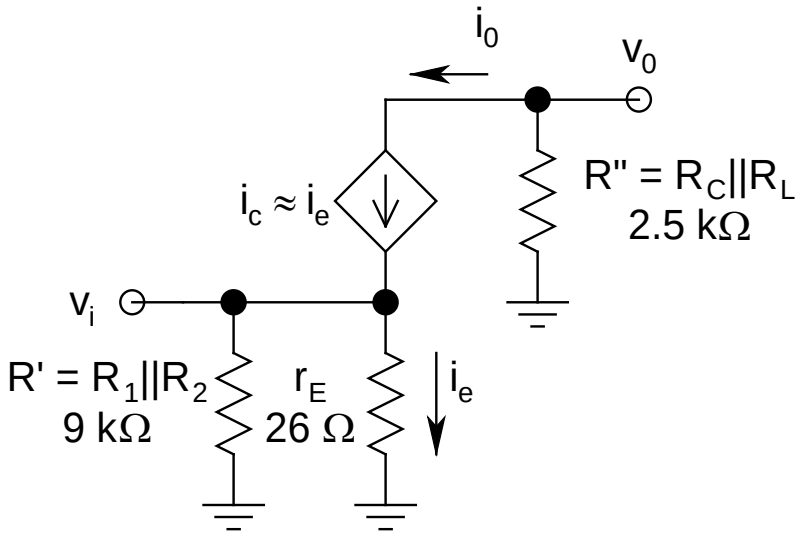
  and $V_{CEQ} = V_{CC} - I_{CQ}(R_C + R_E) = 6.5$ V (close to $V_{CC}/2$)

ac Analysis:

* ***All capacitors shorted***

  $\Rightarrow$ R_E gets bypassed

* ***V_{CC} nulled*** $\Rightarrow$ R_1 comes in parallel to R_2 (R'), and R_C comes in parallel with R_L (R'')



* ***Replace Q by its low-frequency T-model***

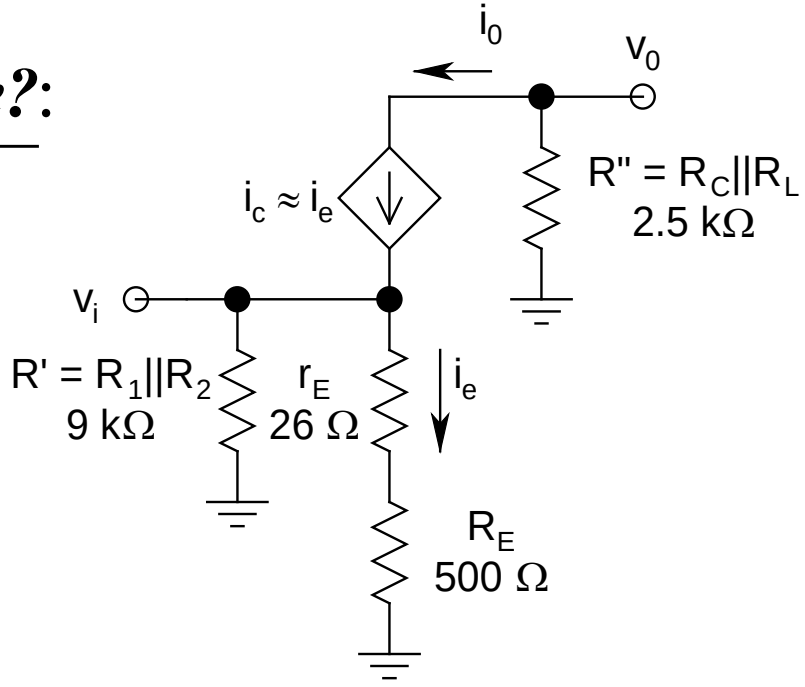
  • ***Note***: $i_0 = i_c \simeq i_e$, $\because$ base current neglected

* Voltage gain: $A_v = \dfrac{v_0}{v_i} = \dfrac{-i_0 R''}{i_e r_E} = -\dfrac{2.5\ \text{k}\Omega}{26\ \Omega} = -96.2$

  • ***Note***: $r_E = V_T / I_{CQ} = (26\ \text{mV})/(1\ \text{mA}) = 26\ \Omega$

* The ***negative*** sign for A_v implies that v_0 is ***exactly out-of-phase*** with v_i (i.e., they are ***180° apart***)
* Note that the input v_i appears at the ***base***, while the output v_0 is taken from ***collector***, with emitter grounded
  $\Rightarrow$ ***Common-Emitter (CE) Amplifier***
* For a ***CE amplifier***, there is a ***phase shift of 180°*** between the input and output
* To ***increase*** A_v, either ***decrease*** r_E, ***increase*** R'', or ***both***
* r_E ***can be decreased by increasing*** I_C (***by a change in bias***)
* R'' ***can be increased by making*** $R_L \gg R_C$ ($max.\ R'' = R_C$)
* ***Note***: **Power gain** = $\left|A_v \times A_i\right| > 9620$ (for $\beta > 100$)

What Happens if C_E is not there?:



* ***DC bias point unchanged***
* ***Due to the absence of C_E, R_E unbypassed***
* Input is still at ***base***, and output is still from the ***collector***, but now ***emitter is grounded through a resistor***

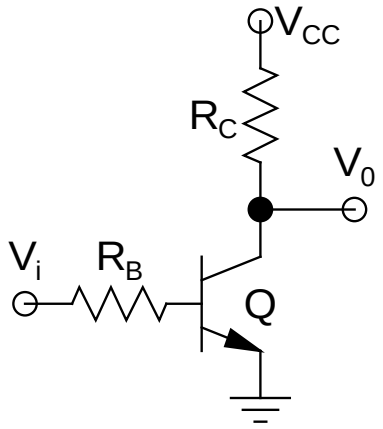
  $\Rightarrow$ ***Common-Emitter (Degeneration)*** [***CE(D)***]

* Voltage gain: $A_v = \dfrac{v_0}{v_i} = \dfrac{-i_0 R''}{i_e\left(r_E + R_E\right)} = -\dfrac{2.5\ \text{k}\Omega}{526\ \Omega} = -4.75$

* ***Note the drastic reduction in A_v (gain degeneration!)***

Simple BJT Inverter:

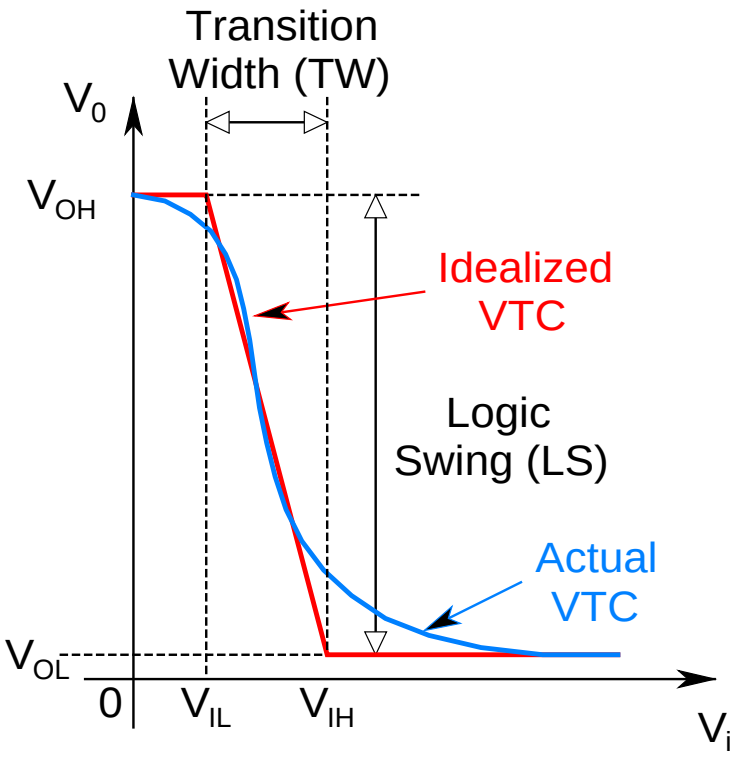
* Basic digital building block
* Known as ***Inverter*** (or ***NOT Gate***)
* Digital circuits have ***two levels***:
  - ***High*** (or ***Hi***) – close or equal to V_{CC}
  - ***Low*** (or ***Lo***) – close or equal to 0



* ***Operation***:
  - $V_i = 0$ (***Lo***), Q is ***off***, $V_0 = V_{CC}$ (***Hi***)
  - $V_i = V_{CC}$ (***Hi***), Q is driven to ***hard saturation***,

    $V_0 = V_{CE(HS)} = 0.1$ V (***Lo***)

    $\Rightarrow$ ***Inverter***



Voltage Transfer Characteristic (VTC)

V_{OH}: Output Hi
V_{OL}: Output Lo
V_{IL}: Input Lo
V_{IH}: Input Hi

NM_H: Noise Margin (High) = $V_{OH} - V_{IH}$
NM_L: Noise Margin (Low) = $V_{IL} - V_{OL}$

TW: Transistion Width = $V_{IH} - V_{IL}$
LS: Logic Swing = $V_{OH} - V_{OL}$

Design Example:

Choose $V_{CC} = 5$ V, $R_C = 2$ kΩ, and $R_B = 20$ kΩ

$V_i = 0\,V$, *Q off* $\Rightarrow$ $\mathbf{V_{OH} = V_{CC} = 5\,V}$

$V_i = 5\,V$, *Q in hard saturation* $\Rightarrow$ $\mathbf{V_{OL} = V_{CE(HS)} = 0.1\,V}$

$\mathbf{V_{IL}}$: **Maximum** ***value of the input that would still ensure that V_0 remains at V_{OH}***

Taken to be equal to $\mathbf{V_{BE} = V_\gamma = 0.6\,V}$

Note that Q just starts to conduct at this point

$\mathbf{V_{IH}}$: **Minimum** ***value of the input that would still ensure that V_0 remains at V_{OL}***

Actual computation is quite tedious

Analysis of V_{IH}:

It is assumed that when $V_i = V_{IH}$, Q is at the onset of saturation with $V_{BE} = 0.7$ V, but with $V_{CE} = 0.1$ V

This is a **clear contradiction**, however, it gives a sufficiently close estimate of V_{IH}

$$\Rightarrow I_C = \frac{V_{CC} - V_{CE}}{R_C} = \frac{5 - 0.1}{2\ \text{k}} = 2.45\ \text{mA}$$

BJTs used in inverters typically have ***$\beta \sim$ 50-100***

Also, β is assumed to have its ***nominal value*** (i.e., ***the value in the FA region***) at this point

Choosing $\beta = 80 \Rightarrow I_B = I_C/\beta = 30.6\ \mu\text{A}$

$$\Rightarrow V_{IH} = V_{BE} + I_B R_B = 0.7 + (30.6\ \mu A) \times (20\ k\Omega)$$

$$= 1.3\ V$$

Thus, $\boldsymbol{LS = V_{OH} - V_{OL} = 4.9\,V}$

$\boldsymbol{TW = V_{IH} - V_{IL} = 0.7\,V}$

$\boldsymbol{NM_H = V_{OH} - V_{IH} = 3.7\,V}$

$\boldsymbol{NM_L = V_{IL} - V_{OL} = 0.5\,V}$

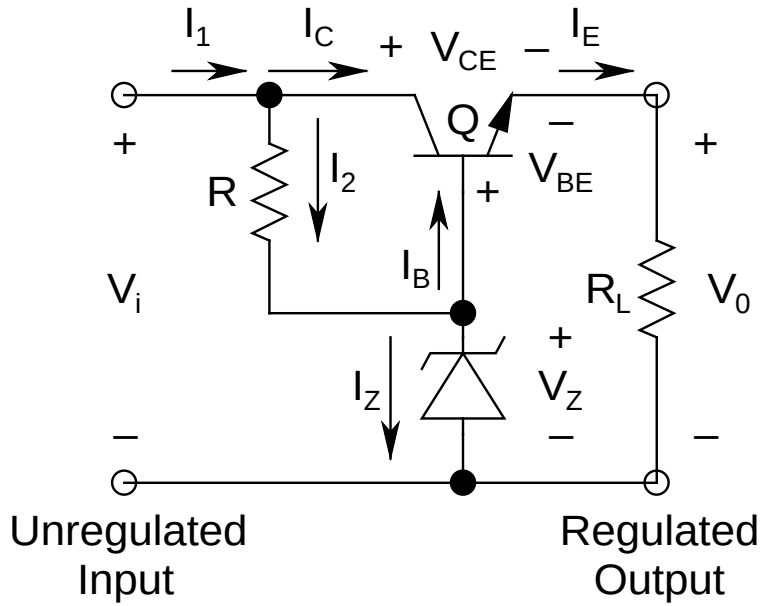
$$\textbf{\textit{Transition Region Gain}} \triangleq \frac{dV_0}{dV_i} = \frac{V_{OH} - V_{OL}}{V_{IL} - V_{IH}}$$

$$= -\frac{LS}{TW} = -7$$

* ***Note***: **Higher the magnitude of the gain, sharper is the response**
* The inverter is the heart of digital circuits, and can be configured in various topologies to produce a variety of digital gates, e.g., ***AND***, ***OR***, ***NAND***, ***NOR***, etc.
* One of the simplest digital blocks to design, and works very well $\Rightarrow$ pretty robust circuit
* ***Note***: Q acts as a **switch** $\Rightarrow$ either ***cutoff*** (with output in the ***Hi*** state) or in ***hard saturation*** (with output in the ***Lo*** state) $\Rightarrow$ that's why it's a **Gate**!

Simple BJT Series Voltage Regulator:

* Extremely simple and powerful circuit
* Operates under the principle of ***negative feedback***
* $V_0 = V_Z - V_{BE} = I_E R_L$
* ***Recall***: I_E depends on V_{BE} exponentially



$\Rightarrow$ Large change in I_E can be accommodated by a very small change in V_{BE}, which can be assumed to be clamped at ~ 0.7 V

* If for any reason, V_0 tends to ***increase***, then V_{BE} ***drops***, which ***reduces*** I_E, and thus, V_0 ***reduces***
* Similarly, if for any reason, V_0 tends to ***decrease***, then V_{BE} ***increases***, which ***increases*** I_E, and thus, V_0 ***increases***
* ***Note that the cause and effect are opposite***

  $\Rightarrow$ **Negative Feedback**
* Extremely robust circuit, with the output having almost ***no ripple***
* ***Note that Q should never saturate*** $\Rightarrow$ $\mathbf{V_{CE,min} = 0.7\ V}$

Design Issues & Constraints:

* $\because$ V_Z has a constant value, let's say 5 V

  $\therefore$ V_0 will have a fixed and constant value of 4.3 V

  Note: **This is independent of the value of R_L**

* ***Minimum value of V_i should be*** $\geq V_0 + V_{CE(min)}$

* Q is known as ***series pass transistor***, since it passes V_i to output with a drop of V_{CE}

* ***Current Relations***: $I_1 = I_C + I_2$, $I_2 = I_Z + I_B$, $I_C = \beta I_B$, and $I_E = (\beta + 1) I_B$

* ***The role of R is very critical***: **it should be chosen extremely carefully**

* The output should never be ***short-circuited***, i.e., R_L should never be made ***zero***, since in that case, ***huge current*** will flow at the output, which will completely ***destroy*** the regulator due to ***over-heating***

  $\Rightarrow$ Actual regulators have ***short-circuit protection***

* If the minimum allowed value of R_L is $\boldsymbol{R_{L,min}}$, which leads to the maximum value of I_E ($\boldsymbol{I_{E,max}} = V_0 / R_{L,min}$) and V_i is at its minimum value $\boldsymbol{V_{i,min}}$, then the current supplied by V_i should not only supply $\boldsymbol{I_{B,max}}$ $\left[= I_{E,max} / (\beta + 1)\right]$, but also the minimum required Zener current $\boldsymbol{I_{Z,min}}$ to sustain breakdown

$$\Rightarrow \text{This gives } \boldsymbol{R_{max}} = \frac{V_{i,min} - V_Z}{I_{B,max} + I_{Z,min}}$$

* With load removed, i.e., R_L open-circuited,

  $I_E = I_C = I_B = 0$

* Under this situation, with V_i at its maximum value $\boldsymbol{V_{i,max}}$, the Zener current should not exceed its maximum limit of $\boldsymbol{I_{Z,max}}$

$$\Rightarrow \text{ This gives } \boldsymbol{R_{min}} = \frac{V_{i,max} - V_Z}{I_{Z,max}}$$

* ***Exercise***: Verify that any value of R falling outside this range will be detrimental for the circuit