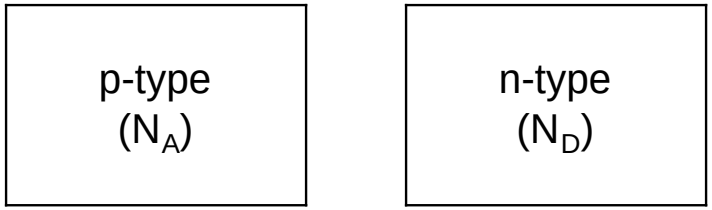
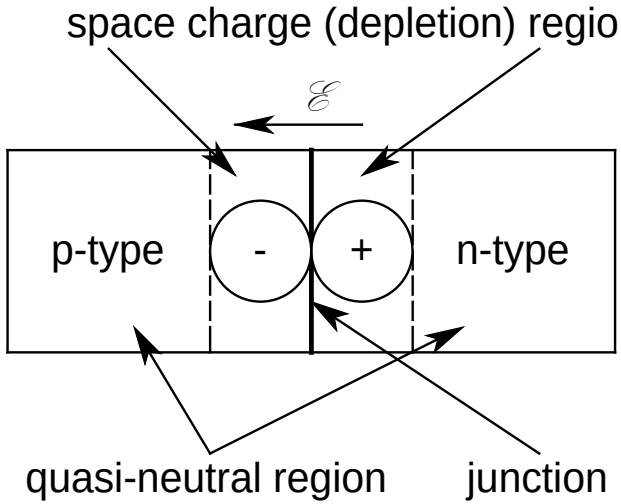
Diodes & Associated Circuits



Before joining



After joining

p-side: holes ***majority carriers***

electrons ***minority carriers***

n-side: electrons ***majority carriers***

holes ***minority carriers***

Treat holes as ***antiparticle*** of electrons

$$N_A \leftrightarrow N_A^- + \text{hole}$$

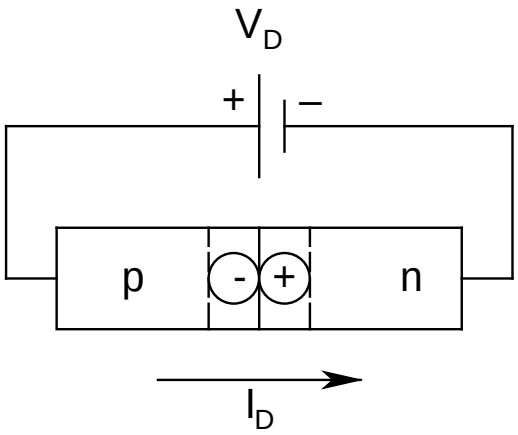
$$N_D \leftrightarrow N_D^+ + \text{electron}$$

* Upon joining, holes move from p-side to n-side, leaving ***ionized acceptors*** N_A^- there, and electrons move from n-side to p-side, leaving ***ionized donors*** N_D^+ there
* This motion is purely due to ***diffusion***, caused due to huge ***concentration gradients*** of carriers
* Thus, a ***charge dipole*** starts to build up around the junction, with n-side ***positive*** with respect to the p-side $\Rightarrow$ known as ***depletion region***
* An ***electric field*** is created across the junction, which tends to ***oppose*** the diffusive motion

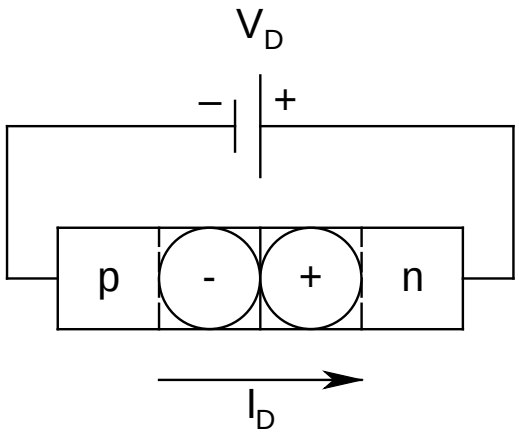
* This ***electric field*** causes an opposite carrier motion due to ***drift***
* Thus, a point will be reached when the ***drift*** flow will exactly ***balance*** the ***diffusive*** flow for ***each type of carrier***
* Under such a condition, the ***net*** holes and electrons (***individually***) crossing the junction will be ***zero***, resulting in ***zero net current***

  $\Rightarrow$ Known as ***equilibrium***
* ***Note***: Under ***equilibrium***, the device does ***not*** carry any ***net*** current

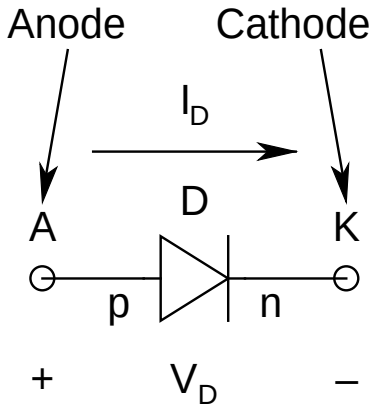
Forward & Reverse Bias:



Forward Bias:
p-side positive
w.r.t. n-side



Reverse Bias:
n-side positive
w.r.t. p-side



Symbol and
current-voltage
convention

* By definition:

- V_D is measured as the voltage ***at the p-side with respect to that at the n-side***, with V_D ***positive*** implying that the diode is under ***forward bias***, and V_D ***negative*** implying that the diode is under ***reverse bias***
- I_D is ***positive*** when it flows from ***p-side to n-side***, and ***negative*** when it flows from ***n-side to p-side***

Forward Bias:

* V_D ***positive*** – p-side more ***positive*** than n-side
* Holes get ***repelled*** from the p-side to the n-side
* Electrons get ***repelled*** from the n-side to the p-side
* Known as the ***carrier injection process***
* Note that this process creates ***flow of charge carriers***, and thus, ***current***
* Note also that both ***hole and electron currents*** are ***in the same direction*** (***p-side to n-side***) $\Rightarrow$ ***positive***
* The ***total current*** I_D is the ***sum*** of these two currents
* The ***magnitude*** of this current increases ***exponentially*** with the magnitude of the applied forward bias (V_D)

Reverse Bias:

* V_D ***negative*** – n-side more ***positive*** than p-side
* Holes get ***pulled*** from the p-side to the battery
* Electrons get ***pulled*** from the n-side to the battery
* Known as the ***carrier extraction process***
* Note that both ***holes and electrons*** again ***flow in the same direction***, thus causing ***currents also in the same direction*** (***n-side to p-side***) $\Rightarrow$ ***negative***
* The ***total current*** I_D is the ***sum*** of these two currents
* The ***magnitude*** of this current is ***independent*** of the ***magnitude*** of the applied reverse bias (V_D)

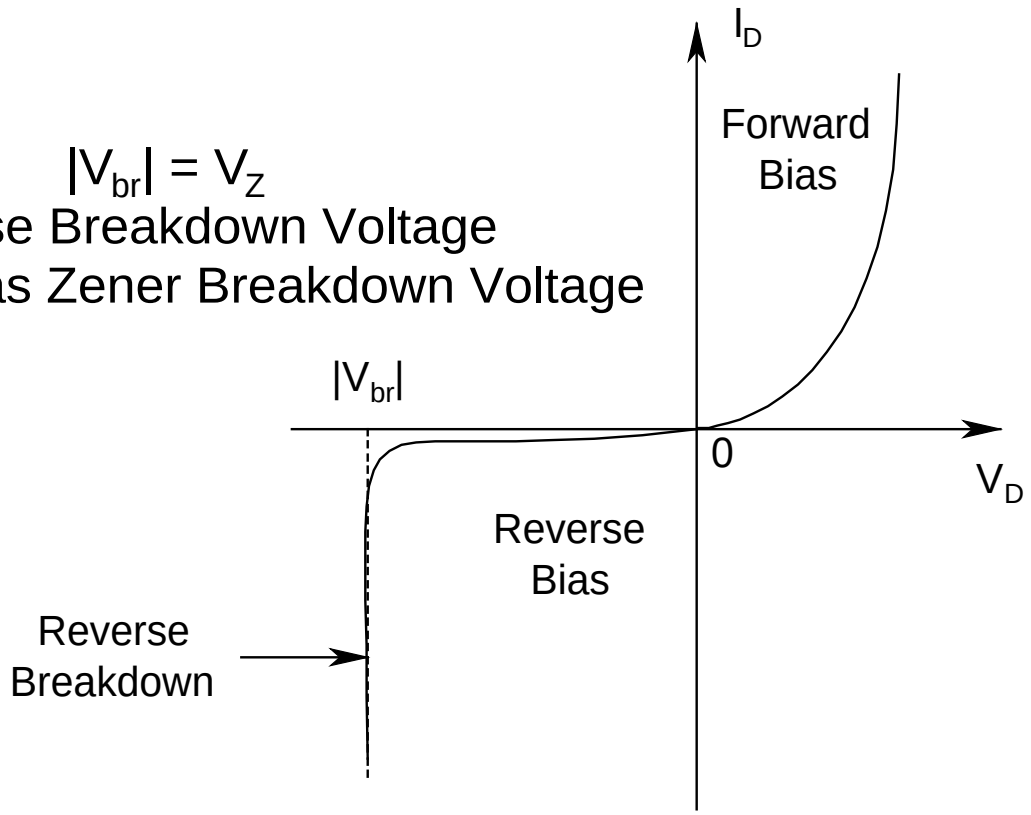
I-V Relation:

* $I_D = I_0\left[\exp\left(V_D/V_T\right)-1\right]$
  - I_0: ***Reverse Saturation Current*** (typically of the order of ***nA-fA***)
  - V_T: ***Thermal Voltage*** $\left(=kT/q\right)$ (***26 mV at 300 K***)
* ***Note***: For $V_D \geq 4V_T$ $\left(\sim 100\text{ mV at room temperature}\right)$:
  - $I_D \simeq I_0 \exp\left(V_D/V_T\right)$ (***a true exponent***) (typically ~mA)
  - ***Flows from p to n***
* For ***negative*** V_D and $\left|V_D\right| \geq 4V_T$:
  - $I_D \simeq -I_0$ ($I_0 \sim$ ***nA-fA – extremely small***)
  - ***Flows from n to p*** (note the ***negative sign***)

* From the ***I-V characteristic***, ***rectification*** property is clearly visible:
  - For ***positive*** V_D, ***significant*** current flows from ***p-side to n-side***, which is an ***exponential*** function of the applied voltage
  - For ***negative*** V_D, ***negligible*** current flows from ***n-side to p-side***, which is ***independent*** of the applied voltage
* This property can be exploited in a variety of circuit applications

Complete I-V Characteristic:

$|V_{br}| = V_Z$
Reverse Breakdown Voltage
Also known as Zener Breakdown Voltage



Note that the forward and reverse current scales are not same

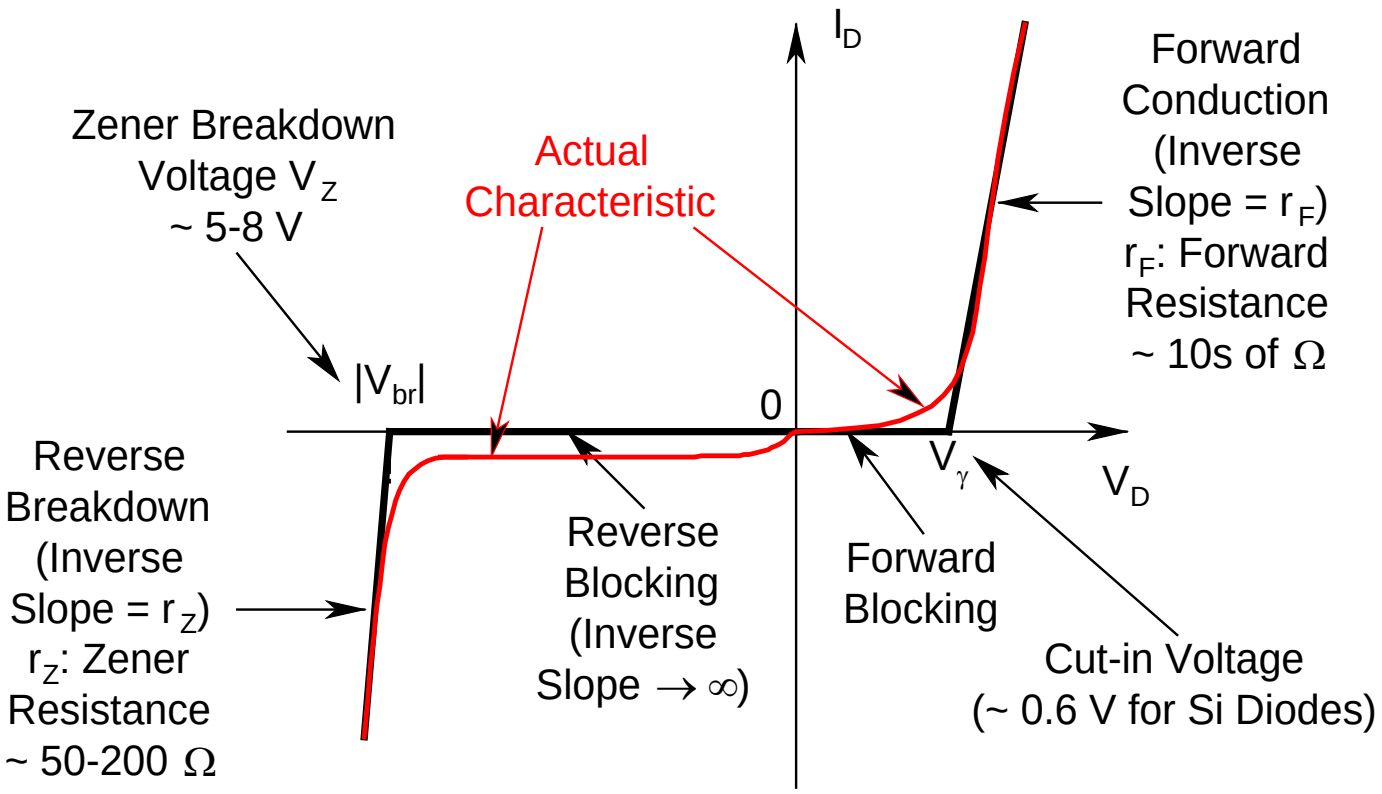
Reverse Breakdown:

* As the ***reverse bias*** voltage across the diode ***increases***, the ***depletion region*** also starts to ***widen***, thus ***accommodating more charges***
* The ***dipole strength*** starts to ***increase*** along with the ***electric field*** across the junction, which is directed from ***n to p***
* When this field ***increases*** beyond a ***critical field***, then ***electrons*** start to get ***detached*** from ***atoms*** (***field ionization***), which may ***knock*** other electrons off from other atoms (***impact ionization***)

  $\Rightarrow$ ***avalanche breakdown***

* There is another ***breakdown process***, known as ***Zener breakdown***, which occurs for diodes having ***both sides very heavily doped***
* This results in a ***very thin depletion region*** across the junction, and electrons can ***tunnel*** through this barrier (***quantum mechanically***)
* ***Zener breakdown voltage*** $\leq$ 3 V
* ***Avalanche breakdown voltage*** $\geq$ 5 V
* Diodes having breakdown voltage ***in the range of 3 V to 5 V***, break down by a ***combination*** of both these mechanisms

Piecewise Linear Model:



Note: The forward and reverse current scales are not same

Regions:

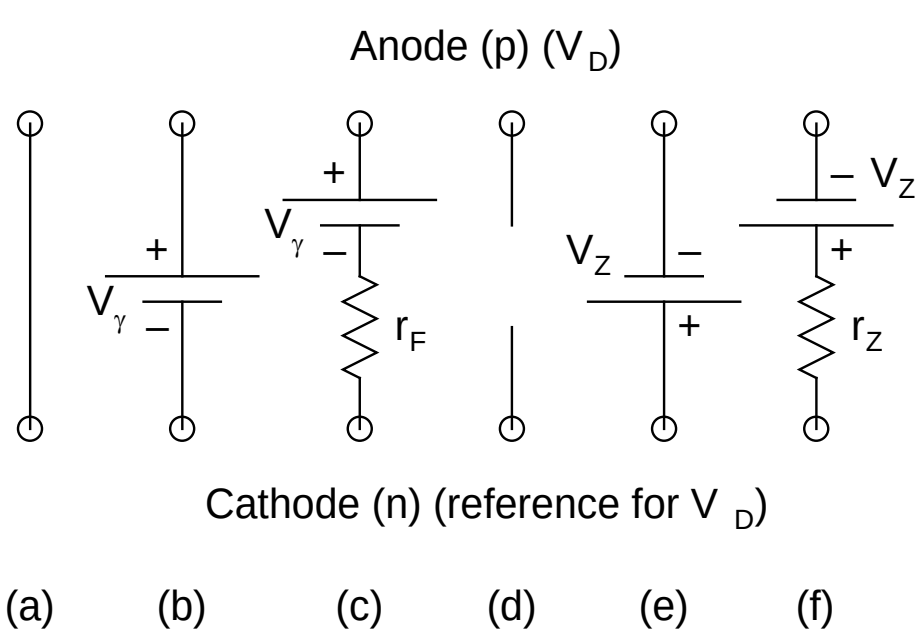
* $0 \leq V_D \leq V_\gamma$: ***Forward Blocking***
  - V_γ: ***Cut-in Voltage*** (~ ***0.6 V*** for ***Si diodes***)
  - $I_D = 0$
* $V_D \geq V_\gamma$: ***Forward Conduction***
  - I_D increases ***linearly*** with V_D with an ***inverse slope*** of r_F
  - r_F: ***Diode Forward Resistance*** (~ 10s of Ω)

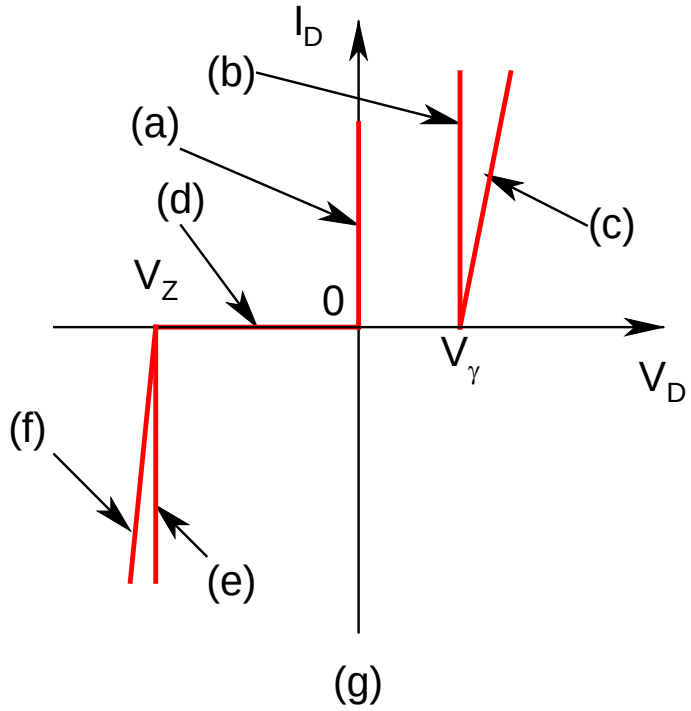
    $= \left[dI_D/dV_D\right]^{-1}$

* Diodes under ***forward bias*** and for V_D ***beyond*** V_γ, offers ***small resistance*** (results from the ***exponential*** I-V characteristic)

* V_D ***negative*** and $0 \leq |V_D| \leq |V_{br}|$: ***Reverse Blocking***
  - $I_D = 0$
* V_D negative and $|V_D| \geq |V_{br}|$: ***Reverse Breakdown***
  - $|I_D|$ increases ***linearly*** with $|V_D|$ with an ***inverse slope*** of r_Z
  - r_Z: ***Zener Resistance*** (~ 50-200 Ω) = $\left[d|I_D| / d|V_D| \right]^{-1}$
* Diodes under ***reverse bias***, with $|V_D| > |V_{br}|$, offers ***small resistance***
* Thus, if current is ***not*** controlled by some ***external means***, then it may ***damage*** the device

Circuit Models:





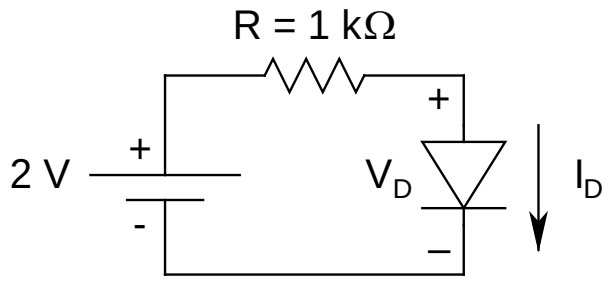
Forward Bias: *V_D positive*: (a) 0th order model,
(b) 1st order model, (c) 2nd order model,
Reverse Bias: *V_D negative*: (d) 0th order model,
(e) 1st order model, (f) 2nd order model.
(g) Corresponding piecewise linear models

Example: Find I_D and V_D, using i) 0th order, ii) 1st order, and iii) 2nd order diode models. [$V_\gamma = 0.6$ V, $r_F = 50\ \Omega$]

i) ***0th order model***:

$$I_D = 2/(1\text{ k}) = 2\text{ mA}$$

$$V_D = 0\text{ V}$$



ii) ***1st order model***:

$$I_D = (2-0.6)/(1\text{ k}) = 1.4\text{ mA and } V_D = 0.6\text{ V}$$

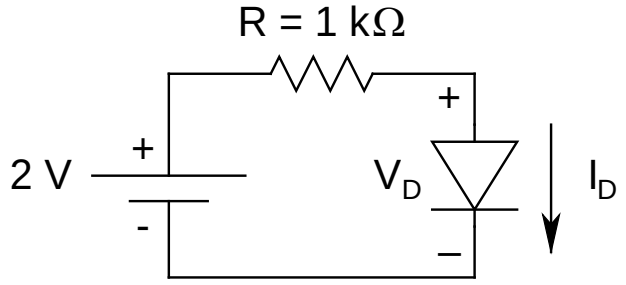
iii) ***2nd order model***:

$$I_D = (2-0.6)/(1\text{ k} + 50) = 1.33\text{ mA}$$

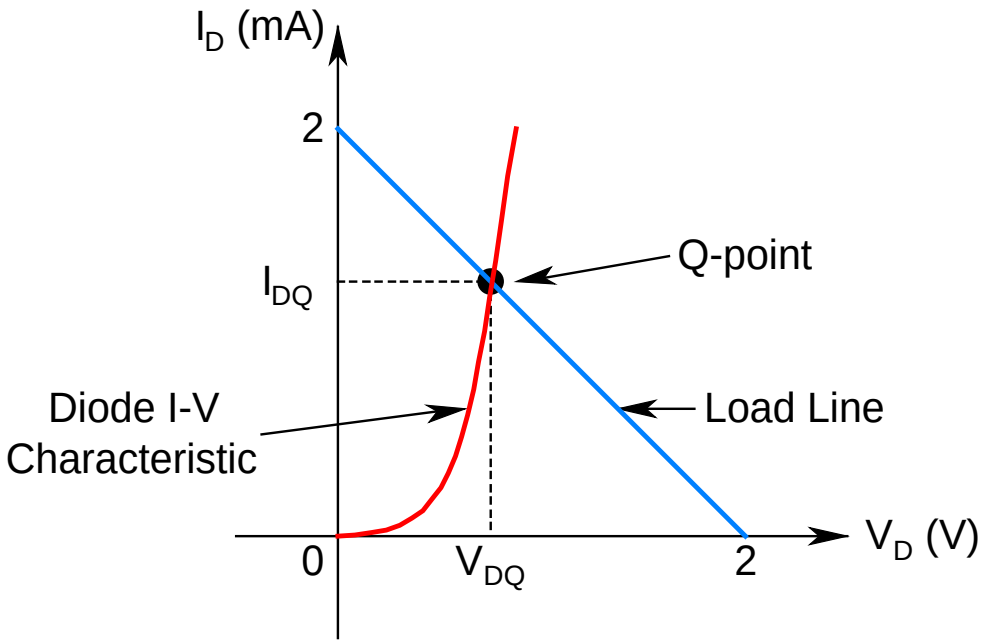
$$V_D = V_\gamma + I_D r_F = 0.667\text{ V}$$

Exact Analysis: *Concept of Load Line*:

* To find the ***exact*** values of I_D and V_D (***need I_0***)
* ***Diode I-V Relation***: $I_D = I_0 \exp\left(V_D / V_T\right)$
  - Neglected the -1 term, since $V_D \gg V_T$
* ***Load Line Equation***: $I_D = \left(2 - V_D\right)/(1\ \mathrm{k})$
* The ***intersection point*** of these two characteristics is known as the ***quiescent operating point***, or the ***Q-point***
* **Two solution techniques**:
  - ***Graphical Method***
  - ***Iterative Method***



Graphical Method:



V_{DQ}, I_{DQ}: Quiescent values of V_D, I_D = 0.7 V, 1.3 mA (obtained from iterative method using I_0 = 3 fA)

DC Quiescent Power Dissipation = $V_{DQ} \times I_{DQ}$ = 0.9 mW

The two ***end points*** of the ***load line***:

1. $V_D = 0$: $I_D = 2/(1\text{ k}) = 2$ mA

2. $I_D = 0$: $V_D = 2$ V

Iterative Method:

* Note that ***simultaneous analytical solution*** of the two equations is ***impossible***, since they form a set of ***transcendental*** equations
* Hence, ***numerical*** or ***iterative*** solution is needed
* **Procedure**:
  - Start with an ***initial guess*** of V_D (~ 0.6 V)
  - Find I_D from the ***load line equation***
  - Use this I_D to find corresponding V_D from the ***diode I-V relation***
  - Repeat till ***convergence*** is attained

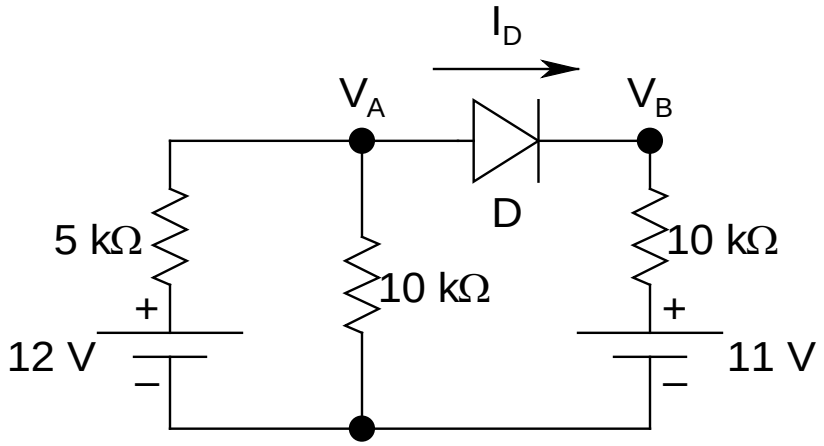
Analysis of Circuits Having Diodes:

*** Procedure**:

- Assume that the diode is ***on*** and choose ***model order***
- Perform ***circuit analysis*** and find the ***current*** flowing through the diode
- If the current is in the ***forward direction*** through the diode, then the assumption was ***correct***
- However, if the current is in the ***reverse direction*** and ***significant***, then the initial assumption that the diode is on was ***wrong***
- Then, ***rework*** the problem, with the diode being ***off***

Example:

Assume that D is ***on***, and use the ***0th order*** diode model



Thus, $V_A = V_B$

Node equation at V_A:

$$\frac{12 - V_A}{5\text{ k}} = \frac{V_A}{10\text{ k}} + \frac{V_A - 11}{10\text{ k}}$$

$$\Rightarrow V_A = 8.75\text{ V} = V_B$$

Thus, the 11 V battery would supply $(11 - 8.75)/10\text{ k} = 0.225$ mA through the diode in the ***reverse*** direction, which is ***impossible***

Thus, our initial assumption that the diode was ***on*** is ***wrong***, since it cannot carry such a ***large*** current in the ***reverse*** direction

Hence, the diode is actually ***off***, and $V_A \neq V_B$

Thus, ***disconnecting*** the diode from the circuit (since it is ***open-circuit*** under the ***0th order*** model)

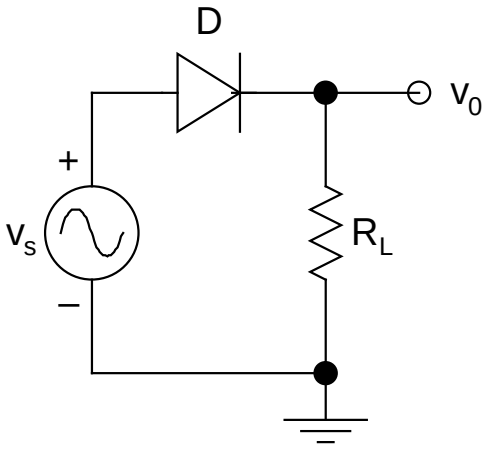
$$V_A = \frac{10}{10+5} \times 12 = 8 \text{ V, and } V_B = 11 \text{ V}$$

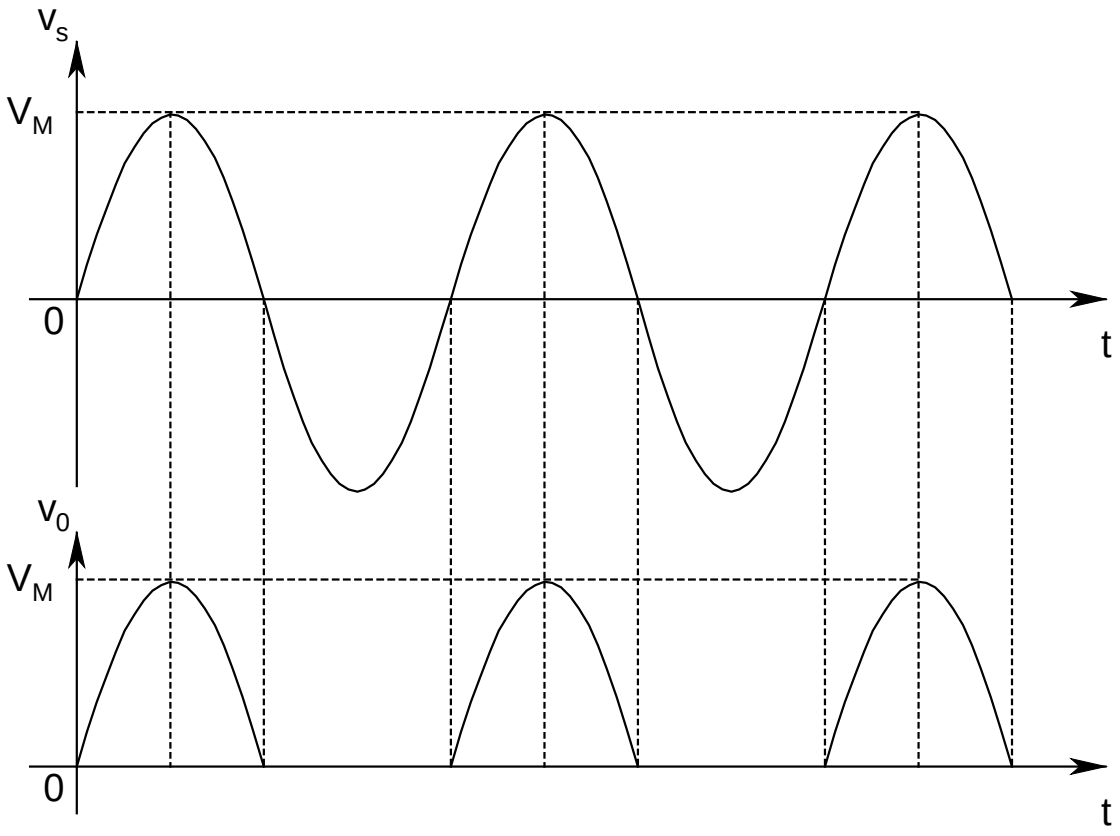
Hence, the diode is under a ***reverse bias*** of 3 V, or under a ***bias of -3 V***

Ex: Rework the problem using 2nd order diode model

- ***Diode Applications***:
  - **Rectification (*conversion of AC to DC*)**
    - ***Half-wave***
    - ***Full-Wave***
    - ***Bridge***
  - **Clamping**
  - **Clipping**
  - **Wave-shaping**
  - **Peak Detection**
  - **Peak-to-Peak Detection**

Half -Wave Rectifier (HWR):





Using 0th Order Diode Model

* ***Note***: The diode D acts as a ***gate*** and ***passes*** signal through it only when it is ***forward biased***, while ***blocking*** it completely when it is ***reverse biased***
* For ***ideal*** diodes, $v_0 = v_s$ for ***positive*** v_s, and $v_0 = 0$ for ***negative*** v_s
* Thus, only the ***positive*** half-cycle of the input signal is ***passed*** on to the output, while the ***negative*** half-cycle is completely ***blocked***

  $\Rightarrow$ ***Half-Wave Rectification***
* The circuit is known as ***Half-Wave Rectifier (HWR)***

* Actual scenario is little ***different***

* Using ***2nd order*** diode model, having V_γ and r_F :

$$\bullet\ v_0 = \frac{R_L\left(v_s - V_\gamma\right)}{R_L + r_F} \qquad v_s \geq V_\gamma$$

$$= 0 \qquad \text{otherwise}$$

* Thus, v_0 remains zero till v_s becomes equal to V_γ, which is $\sim$ ***0.6 V*** for Si diodes

* Also, the ***peak*** value of v_0 will be ***less*** than V_M

* The result is a ***distorted sinusoid*** at the output

* For $V_M \gg V_\gamma$, the distortion would be ***less***

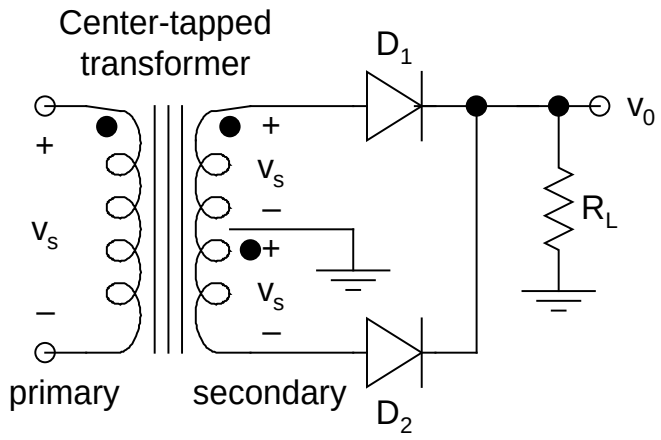
* Note that for ***negative*** cycle of v_s, D is under ***reverse bias***
* It has to be ensured that even for the ***maximum*** reverse bias, it does not undergo ***reverse breakdown***
* Defined by a ***parameter*** known as ***peak inverse voltage*** (***PIV***)
* For the circuit considered, PIV is obviously ***equal*** to V_M
* The ***breakdown voltage*** of D should be chosen to be at least equal to $2V_M$, where 2 is known as the ***safety factor*** (or ***factor of safety***)

Full-Wave Rectifier (FWR):

* The ***disadvantage*** of HWR is obvious, since it ***passes*** **only** the ***positive*** half cycle, while ***blocking*** the ***negative*** half cycle
* Thus, the output ***appears*** **only** during the ***positive*** half cycle, while it is ***zero*** during the ***negative*** half cycle
* It would be much more useful if ***both*** positive and negative half cycles of the input signal can be ***rectified*** to produce a ***unidirectional*** (or ***DC***) ***output***
* 2 ways: ***Center-Tapped Transformer*** & ***Bridge Rectifier***

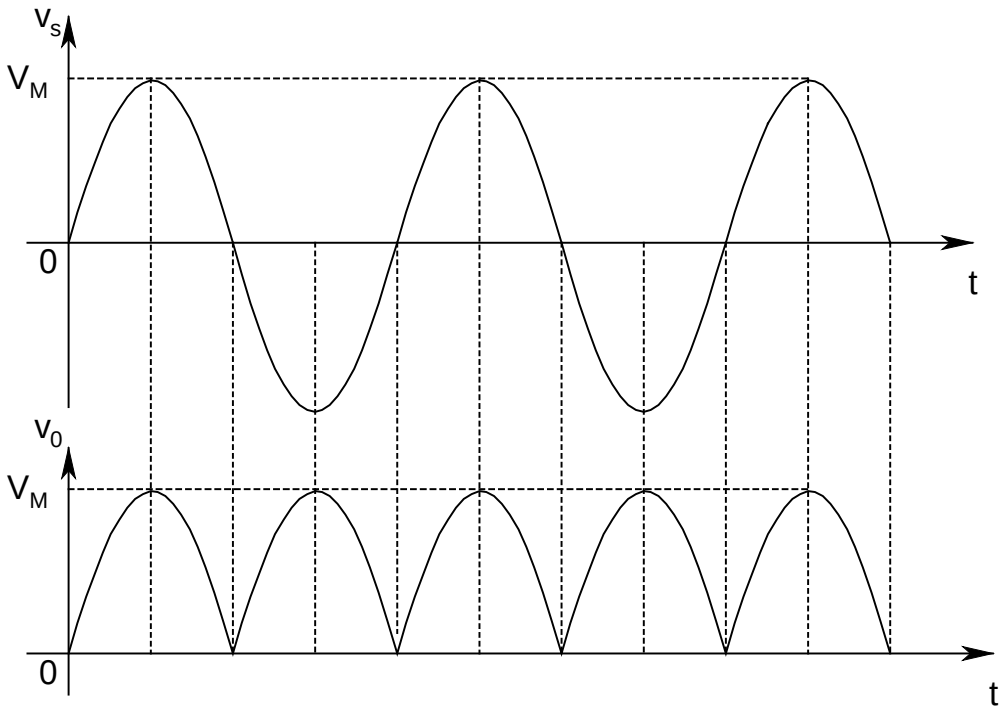
FWR Using Center-Tapped Transformer:

Transformer Secondary
Center Point Grounded



Turns Ratio 1:2

- Convention: The potentials at these ends are either all positive or all negative with respect to the other end at any given instant of time



Using 0th Order Diode Model

* For ***positive*** v_s, D_1 gets ***forward*** biased and v_0 ***follows*** v_s
* Note under this condition, D_2 remains ***reverse*** biased, since its anode is at a ***lower*** voltage than its cathode
* Similarly, for ***negative*** v_s, D_2 becomes ***forward*** biased and D_1 becomes ***reverse*** biased, and again v_0 ***follows*** v_s
* Note that under ***both*** these conditions, the ***current*** flowing through R_L is ***unidirectional***

  $\Rightarrow$ ***Full-wave rectification***

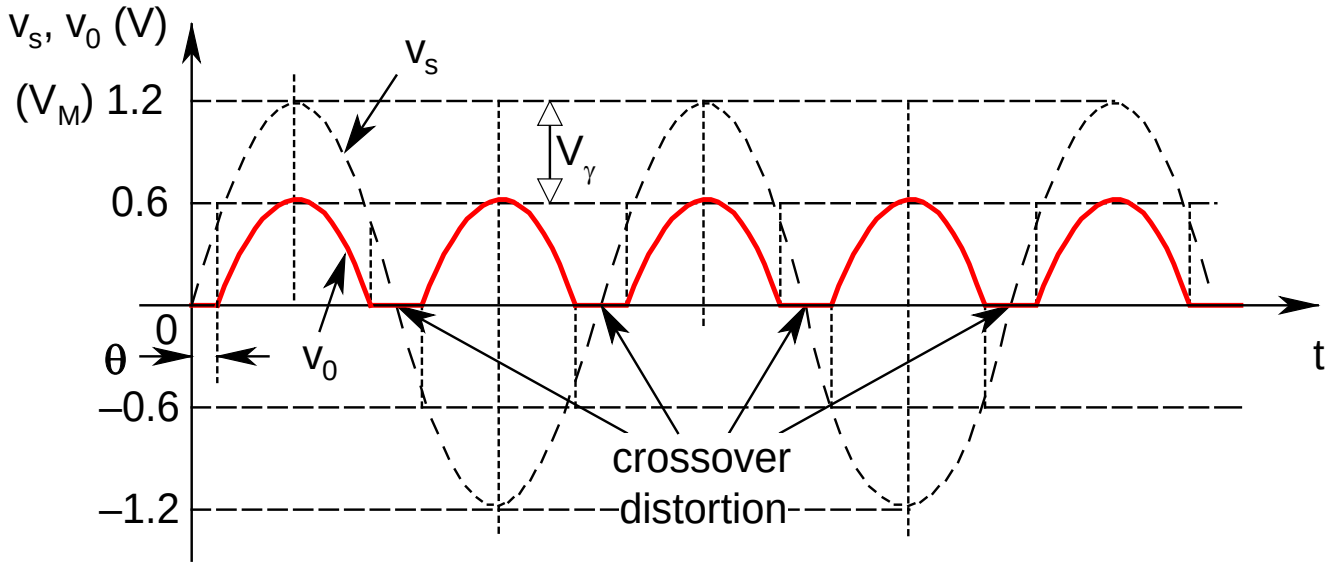
Crossover Distortion:

* Note that for actual diodes, even if the 1st order model is used, then they ***cannot conduct*** until the forward bias across them is ***at least equal to*** V_γ
* This creates a ***deadband*** of around $2V_\gamma$ around all the ***crossover points*** (i.e., points where the input signal ***crosses zero*** in the time axis)
* This problem becomes ***more acute*** if V_M is ***not much larger*** than V_γ
* For $V_M \sim V_\gamma$, this ***crossover distortion*** may completely overwhelm the output

$\theta = \sin^{-1}(V_\gamma/V_M)$ = Angle of Crossover Distortion

Appears 4 times in a complete cycle

Total Crossover Distortion (TCD) = $(2\theta/\pi)\times 100\%$



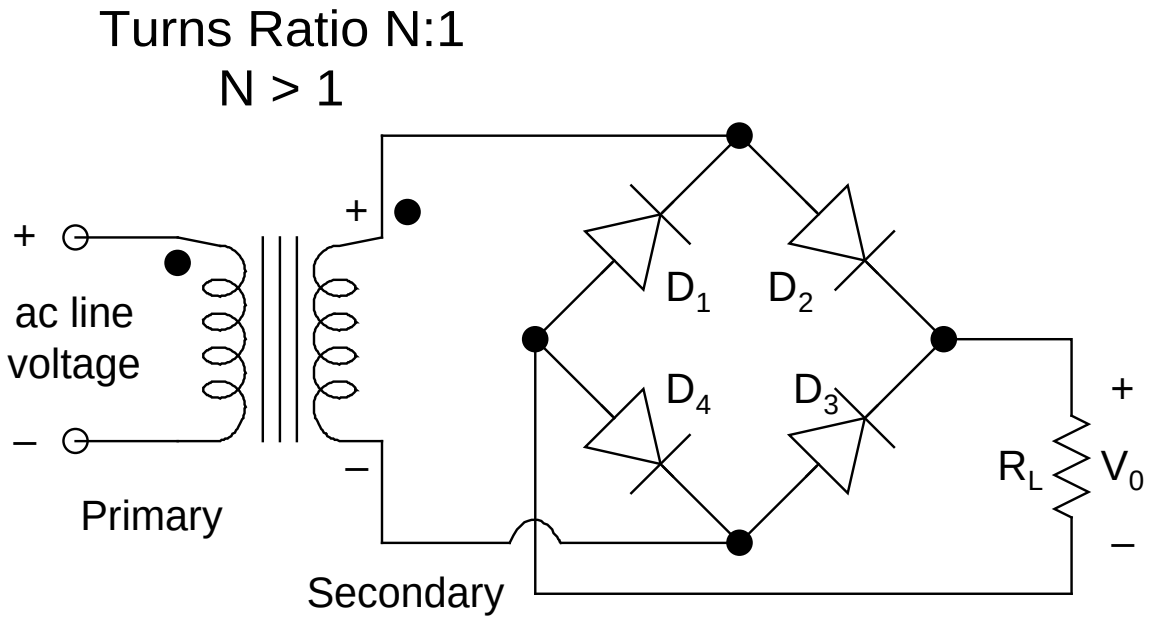
Using 1st Order Diode Model

Regarding PIV:

* Consider ***positive*** half cycle, with D_1 ***forward*** biased and D_2 ***reverse*** biased
* When $v_0 = V_M$, the cathode of D_2 is at V_M
* The center point of the transformer is grounded
* Hence, the lowest point of the transformer secondary is at $-V_M$, which is also the anode voltage of D_2
* Thus, $PIV = 2V_M$, and ***rated breakdown voltage*** $= 4V_M$ (taking ***2 as the safety factor***)

Bridge Rectifier (BR):

* Widely used and highly popular
* All small electrical appliances that work using ***line voltage*** has this circuit built-in within PCB
* Does not need center-tapped transformer, and ***normal*** transformer can be used
* The transformer is ***step-down***, having a ***turns ratio*** of N:1, which typically steps down the line voltage (***230 V rms***) to about ***3-12 V*** (***DC***)
* ***Uses 4 diodes $\Rightarrow$ slightly more expensive***



Positive Half Cycle: Path: D_2-R_L-D_4 (D_1 and D_3 Reverse Biased)
Negative Half Cycle: Path: D_3-R_L-D_1 (D_2 and D_4 Reverse Biased)
Current through R_L : Unidirectional for both cycles (V_0 always positive)

Regarding Crossover Distortion:

* Note that for positive (as well as negative half cycles), ***two*** diodes come in ***series***, each having a cut-in voltage of V_γ, producing a total drop of $2V_\gamma$

  $\Rightarrow$ ***Higher crossover distortion*** and ***lower peak value of the output***

Regarding PIV:

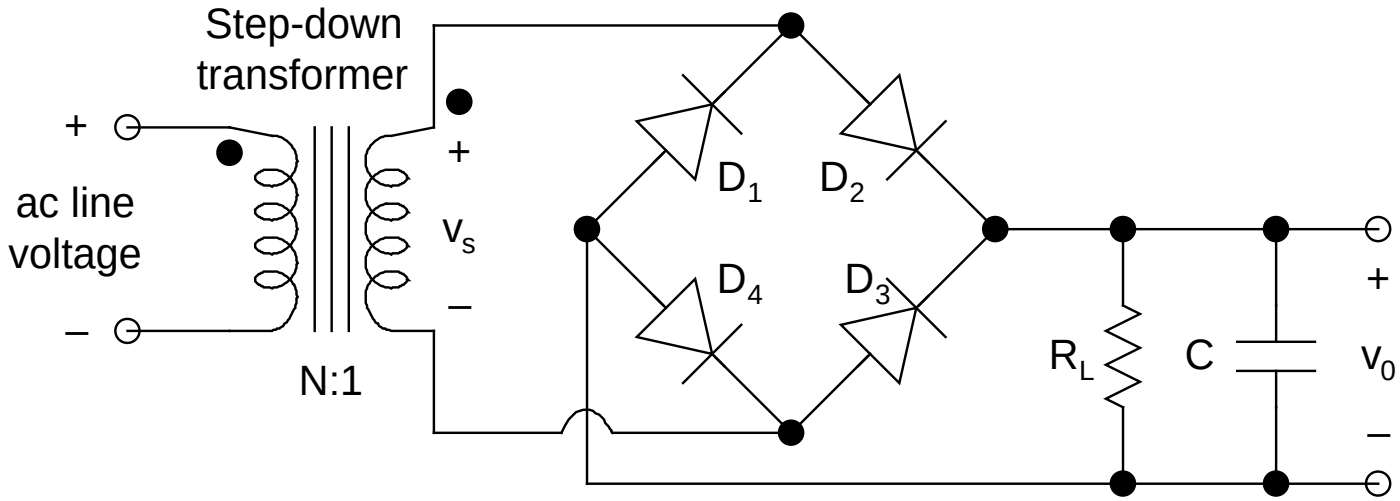
* Note that when $v_0 = V_M$, the cathode of D_3 is at V_M, however, its anode is at ground
* Thus, $PIV = V_M$ and ***rated breakdown voltage*** = $2V_M$ (***using a safety factor of 2***)

Observation:

* Note that even though both FWR and BR produce ***unidirectional*** output, by no stretch of imagination, they can be treated as ***DC*** signals, since they are function of time, and vary widely from 0 to V_M
* Thus, it is not of much use, unless it can be made more or less ***constant***, i.e., ***independent of time***
* Gave rise to another very important analog building block: ***Unregulated DC Power Supply***

- ***DC Unregulated Power Supply***
  - Main goal is to obtain a more or less ***constant*** output, which can be treated as close to ***DC***
  - The simplest way to achieve this is to connect a ***capacitor*** C in ***parallel*** to the ***load resistance*** R_L in both implementations of the FWR (using ***center-tapped transformer*** or ***bridge rectifier***)
  - For a ***bridge rectifier***, during both positive and negative half cycles, a set of ***two diodes*** will conduct and C will charge up to the ***maximum*** voltage V_M (using 0th order diode model)

$v_s = V_M \sin(\omega t)$

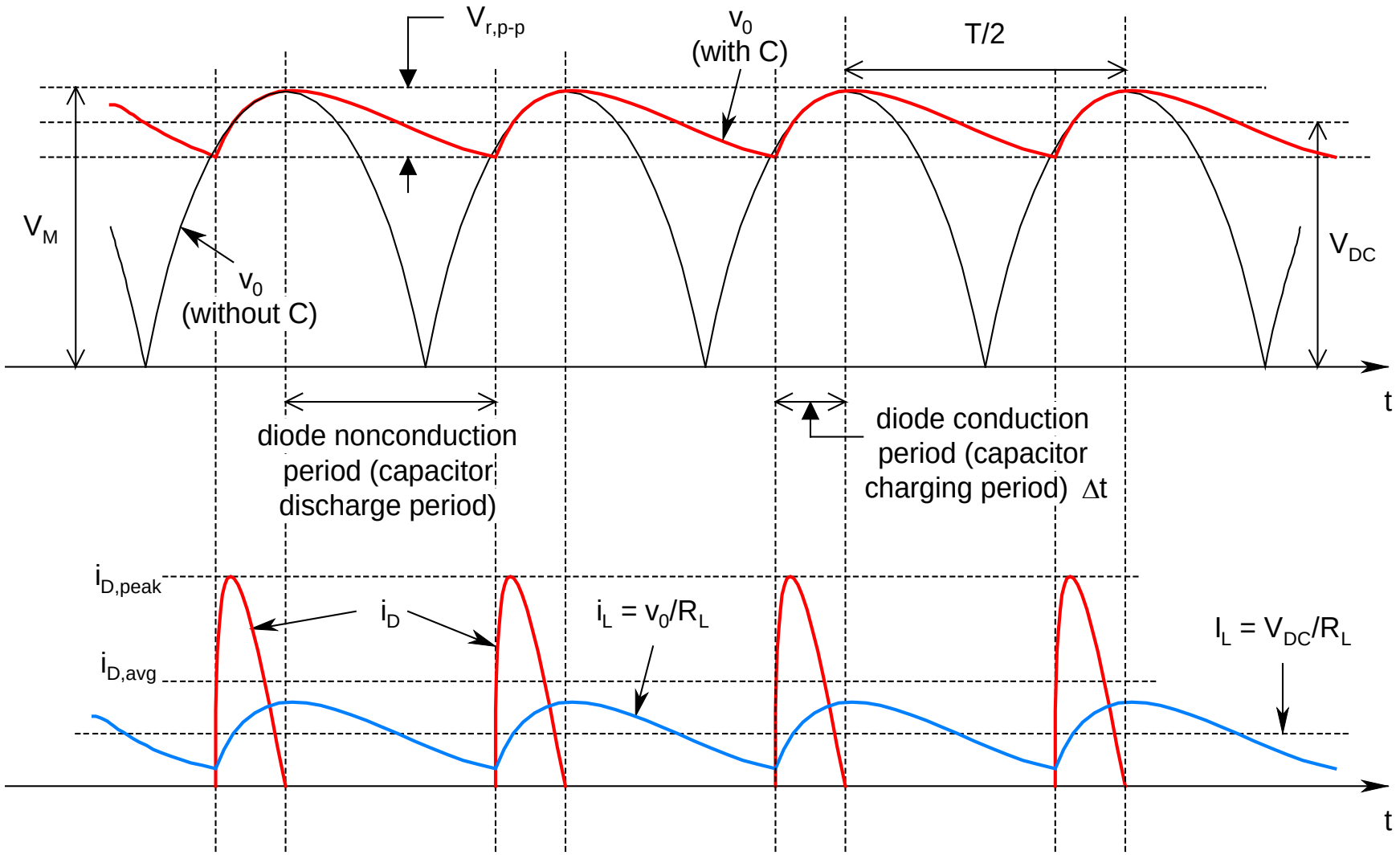


DC Unregulated Power Supply

- As soon as the input starts to fall, the diode will get ***reverse*** biased, and C will start to ***discharge*** through R_L with a ***time constant*** τ (= $R_L C$)
- If this time constant is made ***much larger*** as compared to the ***half period*** of the input signal, then there will be ***very little drop*** of the output voltage (***almost linearly***) during this time
- This process would ***repeat*** for each cycle, and an almost ***constant*** output will be produced
- This is, in essence, the working principle of an ***unregulated DC voltage regulator***

Using 0th order diode model

percent ripple = $(V_{r,p\text{-}p}/V_{DC})\times 100$



$V_{r,p\text{-}p}$: peak-to-peak ripple voltage; i_D: diode current; i_L: load current; V_{DC}: DC output voltage

* ***Note***: v_0 oscillates between V_M and $(V_M - V_{r,p\text{-}p})$

  $\Rightarrow$ For a proper DC output, $V_{r,p\text{-}p}$ should be as small as possible (***ideally zero***)

  $\Rightarrow V_{DC} \simeq V_M$

* To achieve this, the discharge time constant τ $(= R_L C)$ should be ***much larger*** than T/2 (T = ***time period*** of the input signal)

  $\Rightarrow$ C should be ***as large as possible***

  $\Rightarrow$ Discharge profile would almost be a ***straight line***, and $V_{DC} \simeq V_M - V_{r,p\text{-}p}/2$

* Diode ***conducts*** only for a brief period, known as the ***diode conduction period*** (Δt) , during which the ***charge lost*** by C during the ***discharge period*** gets ***replenished***

  $\Rightarrow$ Known as ***capacitor charging period*** (Δt)

* The diode remains ***off*** for the rest of the time

  $\Rightarrow$ Known as the ***non-conduction period*** (or ***capacitor discharge period***)

* Load current $i_L = v_0 / R_L$, thus, it follows the v_0 waveform ***exactly***

* Diode current $i_D = i_L + i_C$, where

  $$i_C = C\frac{dv_0}{dt}$$

  is the ***capacitor charging current***

  Note that this current flows ***only*** during Δt

* The profile of i_D is like a ***skewed hillock***, with the skew towards the ***left*** (almost a ***triangle***)

* The ***peak*** and ***average*** diode currents are denoted by $i_{D,peak}$ and $i_{D,avg}$, respectively

* The average or ***DC load current*** is given by

  $$I_L = V_{DC}/R_L$$

Analysis:

* During ***capacitor discharge period*** [which actually extends for a time interval $\left(T/2-\Delta t\right)$]:

$$v_0 = V_M \exp\left(-t/\tau\right)$$

* Now, in general, $\boldsymbol{\Delta t \ll T/2}$

$\Rightarrow$ At the ***end*** of discharge period:

$$v_0 = V_M - V_{r,p-p} \simeq V_M \exp\left[-T/\left(2\tau\right)\right]$$

* Also, $\boldsymbol{T/\left(2\tau\right) \ll 1}$

$$\Rightarrow \exp[-T/(2\tau)] \simeq [1-T/(2\tau)]$$

$$\Rightarrow V_{r,p-p} = V_M \frac{T}{2\tau} = V_M \frac{T}{2R_L C}$$

Observations:

* For ***small*** $V_{r,p\text{-}p}$:
  - ***C should be large*** – has a negative effect
  - ***R_L should be large*** – lesser load current
  - ***T should be small*** – less time to discharge
* For very small $V_{r,p\text{-}p}$, $V_{DC} \simeq V_M$, and $I_L \simeq V_M / R_L$
* ***Note***: Under this condition: $V_{r,p-p} \simeq I_L / (2fC)$

  f = ***cycle frequency*** = 1/T
* ***Caution***: **This expression is valid only if $V_{r,p\text{-}p} \ll V_{DC}$, however, can be used with acceptable error for less than 10% ripple**

Diode Conduction Period:

* Starts as soon as it gets ***forward*** biased, and continues till v_s reaches V_M

$$\Rightarrow V_M \cos\left[\omega(\Delta t)\right] = V_M - V_{r,p-p}$$

Time t = 0 at the instant when $v_s = V_M$

$\omega = 2\pi f$ (with $f = 1/T$)

* Note: $\Delta t \ll T/2$, and using the identity $\cos(2\theta) \simeq 1 - 2\theta^2$ (***for small θ***):

$$V_M\left[1 - 2\left\{\omega(\Delta t)/2\right\}^2\right] \simeq V_M - V_{r,p-p}$$

$$\Rightarrow \Delta t \simeq \frac{1}{\omega}\sqrt{\frac{2V_{r,p-p}}{V_M}}$$

* ***Caution***: This expression is only valid for $\boldsymbol{\Delta t \ll T/2}$
* For large $V_{r,p\text{-}p}$ (particularly for ***more than 10% ripple***), this expression ***should not be used***
* The ***inverse*** dependence of Δt on ω is ***misleading*** (actually the product $\omega(\Delta t)$ should be ***small***)
* Therefore, this expression just gives an ***estimate*** and is by no means accurate

Average and Peak Diode Currents:

* Can be found by ***equating*** the charges that are ***supplied*** to the capacitor during the ***charging period***, with the one that is ***lost*** during the ***discharge period***
* Charge ***lost*** by the capacitor during the ***discharge period*** = $CV_{r,p\text{-}p}$
* Charge ***supplied*** to it during the ***charging period*** = $i_{C,avg}\Delta t$, where $i_{C,avg}$ is an ***average charging current*** of the capacitor during the time interval Δt

* $i_{C,avg} = i_{D,avg} - i_{L,avg}$, where $i_{D,avg}$ is the ***average diode current*** during the ***charging period*** and $i_{L,avg}$ is the ***average load current***

* If $V_{r,p\text{-}p}$ is ***small***, then $i_{L,avg} \simeq I_L \simeq V_M / R_L$

* Thus, the ***charge balance equation***:

$$\left(i_{D,avg} - I_L\right)\Delta t = CV_{r,p\text{-}p}$$

$$\Rightarrow i_{D,avg} = I_L\left(1 + \pi\sqrt{\frac{V_M}{2V_{r,p-p}}}\right)$$

Recall: $V_{r,p-p} \simeq \dfrac{I_L}{2fC}$ and $\Delta t \simeq \dfrac{1}{\omega}\sqrt{\dfrac{2V_{r,p-p}}{V_M}}$

* The ***peak*** value of the ***diode current*** occurs as soon as the diode gets ***forward biased***, i.e., at $t = -\Delta t$

* Using KCL at the output node at $t = -\Delta t$:

$$i_{D,peak} = C\left.\frac{dv_s}{dt}\right|_{t=-\Delta t} + i_L$$

* ***Recall***: $v_s = V_M\cos(\omega t)$, with t measured from the peak of the signal, and $i_L \simeq I_L$

$$\Rightarrow i_{D,peak} = I_L\left(1+\pi\sqrt{\frac{2V_M}{V_{r,p-p}}}\right)$$

Observations:

* ***Note***: $i_{D,avg} \simeq i_{D,peak}/2$, since $V_{r,p-p} \ll V_M$

  $\Rightarrow$ the ***diode current*** waveform is close to being a ***right-angled triangle***

  $\Rightarrow$ ***Both*** $i_{D,avg}$ ***and*** $i_{D,peak}$ ***are*** $\gg I_L$

* Should be intuitively obvious, since C ***discharges*** for a ***much longer time*** interval with an ***almost constant*** DC current I_L, whereas it is ***charged*** for a ***very short duration*** (Δt)

  $\Rightarrow$ Thus, from ***charge balance***, the ***charging current should be much larger than the DC load current***

* Both $i_{D,avg}$ and $i_{D,peak}$ are ***inverse*** function of $V_{r,p\text{-}p}$
* ***Recall***: $V_{r,p\text{-}p}$ is an ***inverse*** function of C
* Thus, ***high value of C reduces $V_{r,p\text{-}p}$ but increases $i_{D,avg}$ and $i_{D,peak}$***
* Diodes have ***peak and impulse current ratings***
* ***Peak Current Rating***: The ***maximum*** current that the diode can ***safely carry*** under ***normal operating condition*** (i.e., the current is ***sustained***)
* ***Impulse Current Rating***: The ***maximum*** current that the diode can ***safely carry*** for a ***very short period of time***

* The ***impulse current rating*** along with the ***permissible time*** are specified in the ***data sheet*** of the diode
* If the current flowing through the diode ***exceeds*** these current ratings, then it would cause ***destructive breakdown*** of the diode due to ***excessive heating*** caused by ***large power dissipation***
* Thus, ***indiscriminately increasing the value of the filter capacitor C to smooth out the output voltage waveform is, in general, not a good practice***

Example: Transformer secondary output = 15 V (rms), 50 Hz. Maximum permissible drop in v_0 from no load (i.e., $R_L \to \infty$, open-circuit) to full load (corresponding to $R_L = 100\ \Omega$) not to exceed 1 V.

To find C; and $i_{D,avg}$, $i_{D,peak}$, and Δt at full load.

Solution: $V_M = 15 \times \sqrt{2} = 21.2$ V

With no load, $I_L = 0$ and $V_{DC} = V_M$

Under full load, $V_{DC} = V_M - V_{r,p\text{-}p}/2$

$\because$ Maximum drop allowed is 1 V,

$\therefore\ V_{r,p\text{-}p} = 2$ V

$$\Rightarrow C = V_M \Big/ \left(2 f R_L V_{r,p\text{-}p} \right) \; = \; 1006 \; \mu F$$

Note how large the required value of C is!

Note: The analysis done so far is pretty accurate if $V_{r,p\text{-}p}$ is less than 10% of V_{DC}

The analysis results can still be used even if $V_{r,p\text{-}p}$ is more than 10% of V_{DC}, however, obviously, the result will be less accurate

Average DC Output Voltage $V_{DC} = V_M - V_{r,p\text{-}p} \big/ 2$

$= 20.2$ V

Note that $V_{r,p\text{-}p}$ is just less than 10% of V_{DC}

$\Rightarrow$ Average full load current $I_L = V_{DC}/R_L = 202$ mA

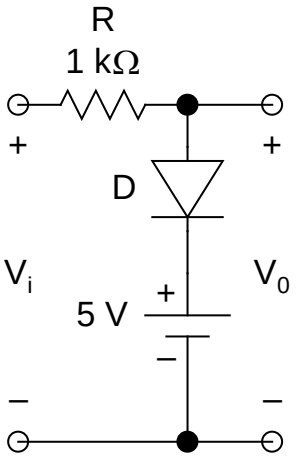
$$i_{D,avg} = I_L\left(1+\pi\sqrt{\frac{V_M}{2V_{r,p-p}}}\right) = 1.66 \text{ A}$$

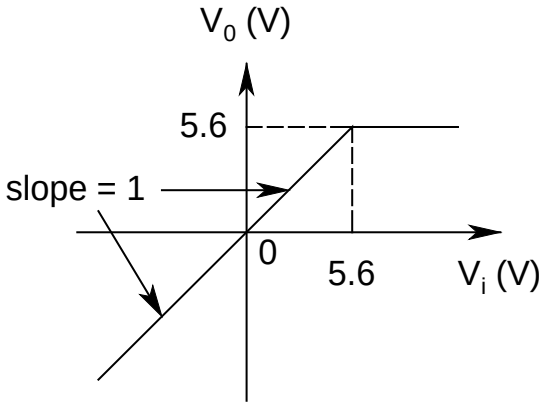
$$i_{D,peak} = I_L\left(1+\pi\sqrt{\frac{2V_M}{V_{r,p-p}}}\right) = 3.12 \text{ A}$$

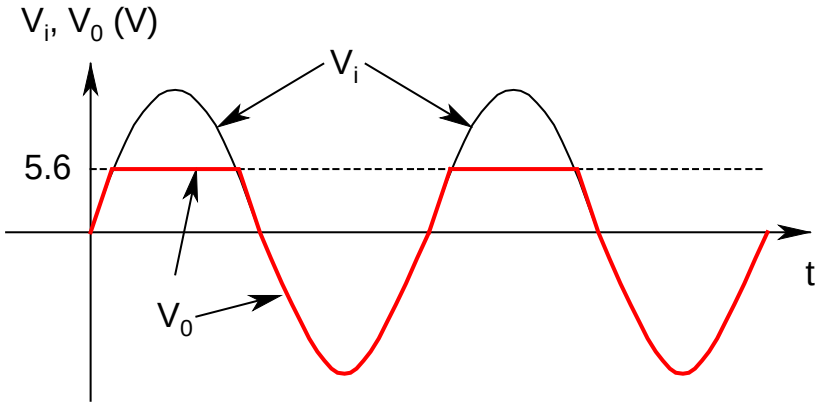
Note: $i_{D,peak}$ is about twice that of $i_{D,avg}$, and both are much larger than I_L (15 and 8 times, respectively)

$$\Delta t \simeq \frac{1}{\omega}\sqrt{\frac{2V_{r,p-p}}{V_M}} = 1.4 \text{ ms} \quad \begin{pmatrix} \text{note}: T/2 = 10 \text{ ms} \\ \Delta t \text{ is more than } 10\% \end{pmatrix}$$

Diode Clamping Circuit:







Voltage Transfer Characteristic (VTC) using 1st order diode model with V_γ = 0.6 V

* Cathode of D at constant 5 V DC

  $\Rightarrow$ It cannot conduct until its anode reaches 5.6 V

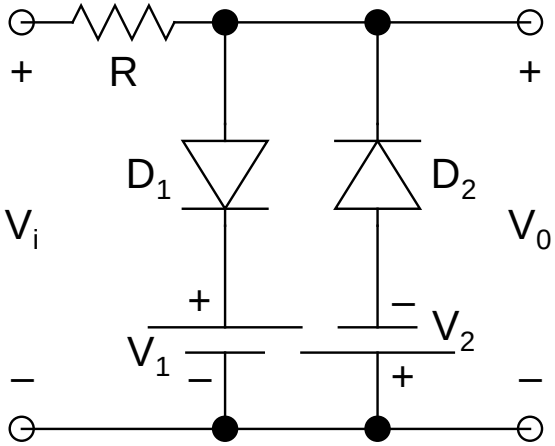
  $\Rightarrow$ For all negative values of V_i, as well as for positive values less than 5.6 V, D remains ***off***, and $\boldsymbol{V_0}$ ***follows*** $\boldsymbol{V_i}$

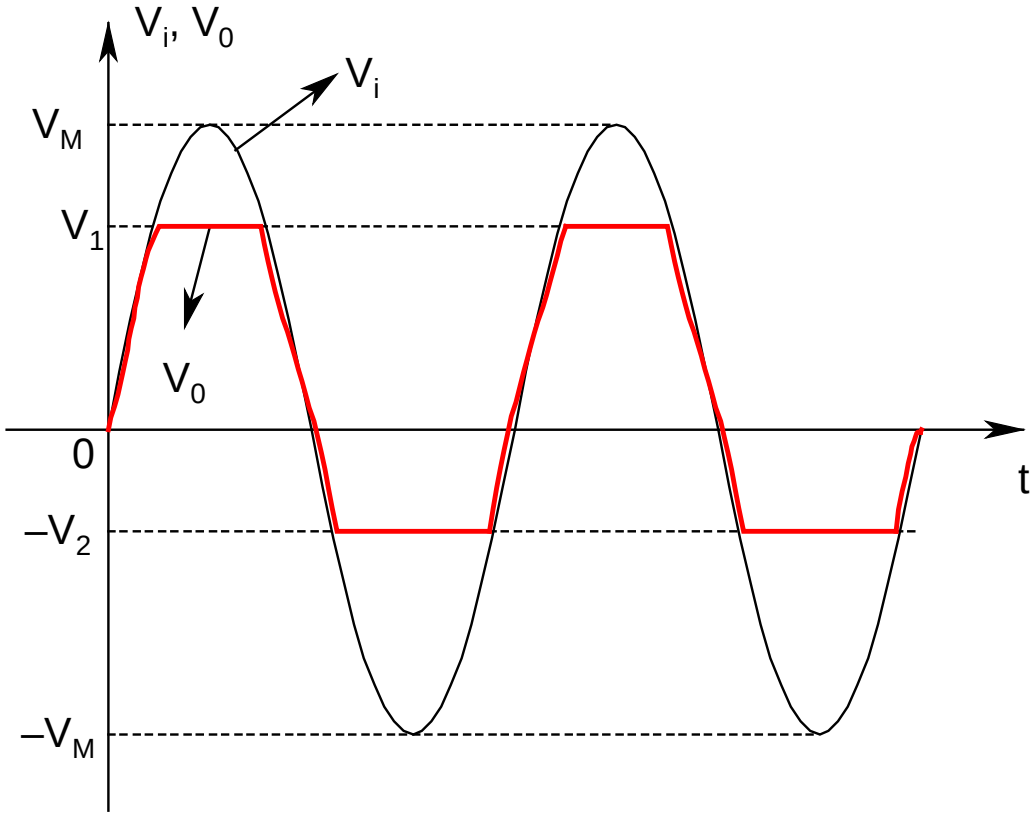
  $\Rightarrow$ For $V_i \geq 5.6$ V, the diode branch turns ***on*** and V_0 gets ***clamped/clipped*** at 5.6 V

  $\Rightarrow$ ***Diode clamping/clipping circuit***

* ***Exercise***: Use 2nd order diode model with $V_\gamma = 0.6$ V and $r_F = 50\ \Omega$, and rework the problem

Dual Clipper:





Using 0th order diode model

* Provides for ***clipping*** of input waveforms in both ***positive*** and ***negative*** half cycles
* Cathode of D_1 sitting at $+V_1$ and anode of D_2 sitting at $-V_2$

  $\Rightarrow$ Using 0th order diode model, for all values of V_i from $-V_2$ to $+V_1$, both diodes would be ***off***, and ***V_0 would follow V_i***
* For D_1 to conduct, its anode voltage must be $\geq V_1$, and for D_2 to conduct its cathode voltage must be $\leq -V_2$

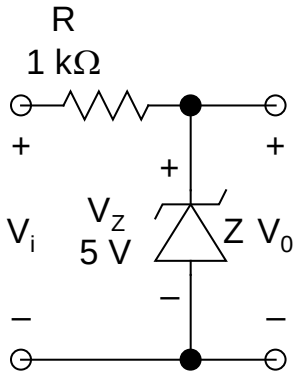
* Thus, for $V_i \geq V_1$, D_1 ***conducts***, D_2 remains ***off***, and V_0 gets ***clamped/clipped*** at V_1
* Similarly, for $V_i \leq -V_2$, D_2 ***conducts***, D_1 remains ***off***, and V_0 gets ***clamped/clipped*** at $-V_2$
* Note: If $V_1 = |V_2|$, then the clipping will be ***perfectly symmetric*** for both positive and negative half cycles
* ***Exercise***: Rework the problem using 2nd order diode model with $V_\gamma = 0.6$ V and $r_F = 50\ \Omega$

Zener Diode:

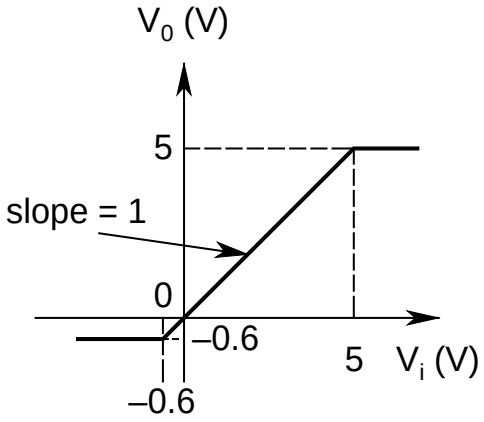
* **Normal diodes** have ***breakdown voltage in excess of 50 V*** (in general)
* **Zener diodes**, on the other hand, have ***breakdown voltage*** typically in the range of ***3-8 V***
* Under ***forward bias***, there is absolutely ***no difference*** between a normal diode and a Zener diode
* Zener diodes, under breakdown, ***clamps*** the voltage across it at the ***breakdown voltage***
* Zener diodes, operated in the breakdown mode, have some important circuit applications

Zener Diode Clamping Circuit:

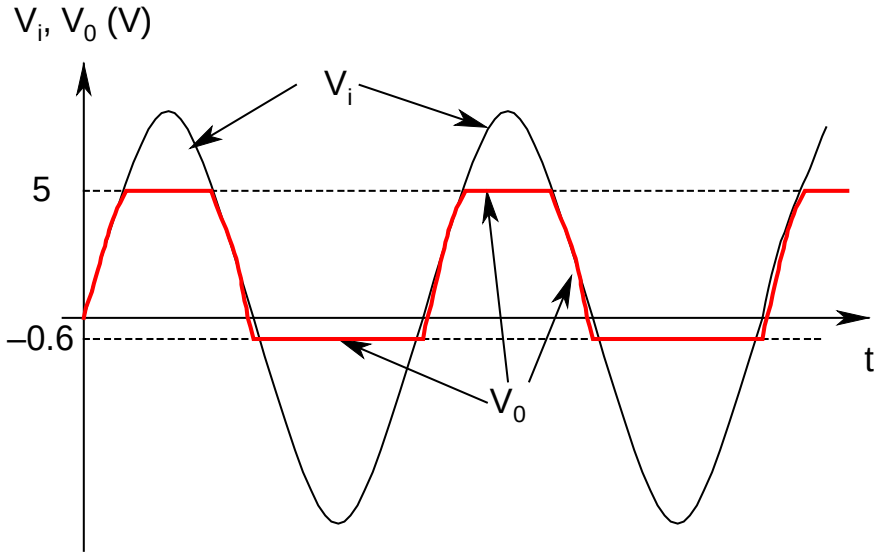
Note the symbol of a Zener diode



V_Z: Zener Breakdown Voltage (actually negative, but defined as a positive number)



Voltage Transfer Characteristic (VTC) using 1st order diode model with V_γ = 0.6 V and V_Z = 5 V

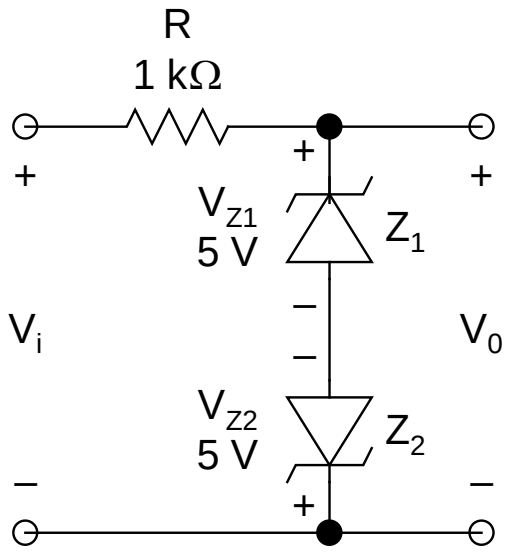


Using 1st order diode model

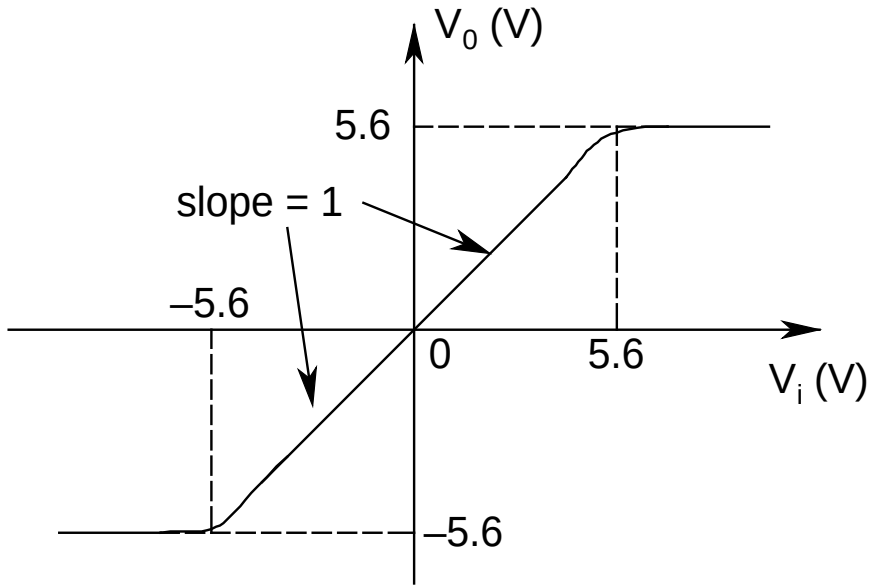
* For ***negative*** V_i, Z will be ***forward biased***, and would ***clamp*** V_0 at $-V_\gamma$ (= -0.6 V) for all values of $V_i \leq -0.6$ V
* For $V_i \geq V_Z$ (= 5 V), Z will ***break down*** and ***clamp*** the voltage across it at V_Z
* For V_i ranging between $-0.6\,V$ ***and*** $5\,V$, Z will be ***off***, and V_0 would ***follow*** V_i
* ***Exercise***: Rework the problem using 2nd order Zener diode model with $r_Z = 100\ \Omega$

  r_Z: Zener resistance under breakdown mode

Dual Clipper Using Zener Diodes:



We have chosen $V_{Z1} = V_{Z2}$, however, it need not be so.
But $V_{\gamma 1} = V_{\gamma 2} = V_{\gamma} = 0.6$ V.



VTC using 1st order diode model

* Note the ***back-to-back*** connection of Z_1 and Z_2

  $\Rightarrow$ Known as ***double-anode Zener***

* For $V_i > (V_{Z1} + V_\gamma)$, Z_1 will operate under ***breakdown mode*** and Z_2 will operate under ***forward bias***

  $\Rightarrow V_0$ will get ***clamped*** at $\left(V_{Z1} + V_\gamma\right)$

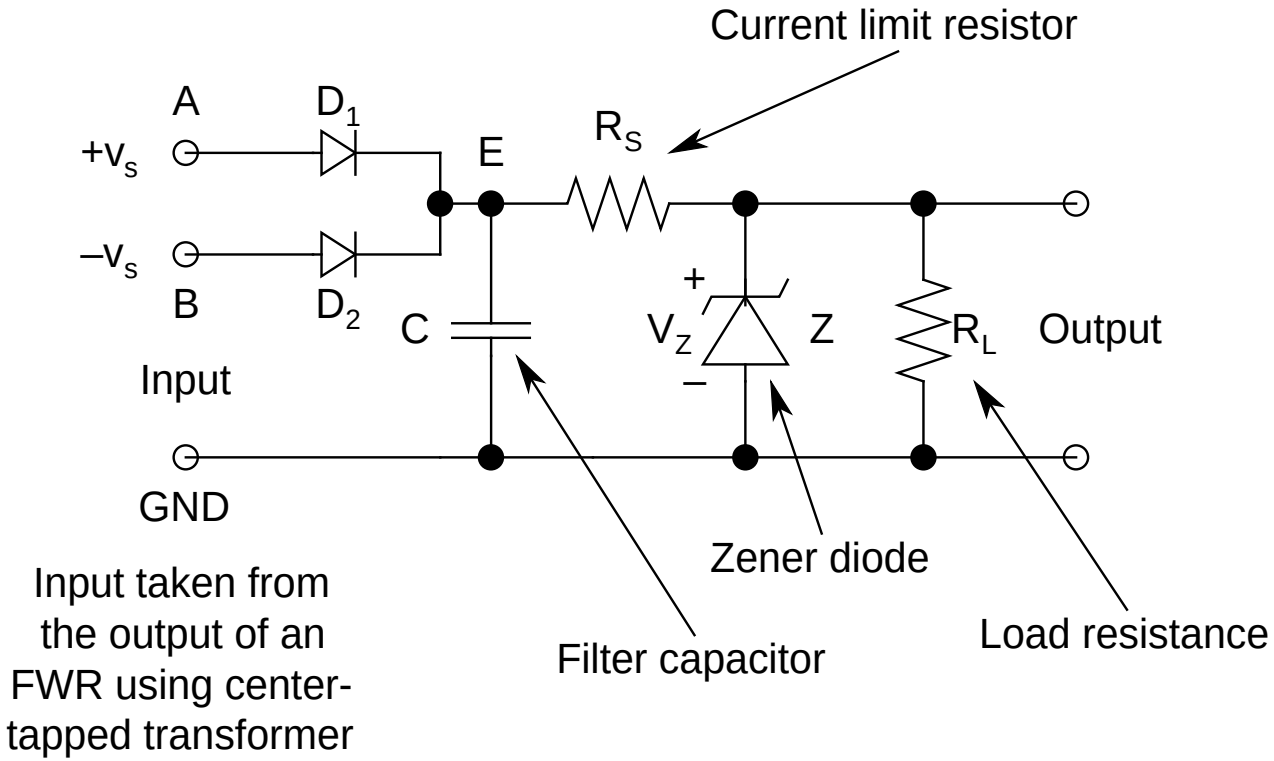
* For $V_i < -(V_{Z2} + V_\gamma)$, Z_2 will operate under ***breakdown mode*** and Z_1 will operate under ***forward bias***

  $\Rightarrow V_0$ will get ***clamped*** at $\left[-(V_{Z2} + V_\gamma)\right]$

* In between these two values of V_i, either of Z_1 or Z_2 will be ***off*** and ***V_0 would follow V_i***

Regulated DC Power Supply:

* Immensely useful module to convert ***ac input*** to ***DC output***, with almost ***no ripple*** present at the output, as well as the output being ***independent*** of the value of the ***load resistance***
* It's a ***series*** combination of an ***FWR*** circuit (either using a ***center-tapped transformer*** or a ***bridge rectifier***), a ***capacitive filter*** circuit, and a ***Zener diode clamping*** circuit



Regulated DC Power Supply
(*Zener Voltage Regulator*)

* The voltage at point E is almost a ***sawtooth*** waveform, varying between V_M and $(V_M - V_{r,p\text{-}p})$

  V_M: peak value of input, $V_{r,p\text{-}p}$: peak-to-peak ripple

* If these values lie ***below*** the breakdown voltage V_Z of the Zener diode, then the latter would have ***no role*** to play in the operation of the circuit, and the output will simply be given by the ***voltage division*** between R_L and R_S

* However, if these voltages are ***greater*** than V_Z, then the Zener diode would operate in the ***breakdown mode***, and the output would get ***clamped*** at V_Z

* Thus, the output would have ***no ripple*** present in it, and would be completely ***independent*** of the value of the ***load resistance*** R_L
* However, the actual picture is not that perfect!

Actual Scenario:

* A practical Zener diode, operating in the ***breakdown mode***, need a ***minimum current*** ($I_{Z,min}$) to flow through it to ***sustain*** the breakdown mode
* Also, a practical Zener diode has a limit on the ***maximum current*** ($I_{Z,max}$) that it can safely ***sink***

* $I_{Z,max}$ is dictated by the ***maximum allowed power dissipation*** in a Zener diode, $P_{Z,max}$, given by

  $P_{Z,max} = V_z \times I_{z,max}$

* Added to that is the ***Zener resistance*** r_Z in the breakdown mode, typically ranging about 50-100 Ω
* In the presence of this r_Z, the actual output across the Zener diode ***will not be constant***, but would keep on ***changing with changing input voltage***

  $\Rightarrow$ ***ripples would start to show up at the output***, depending on the variations present in the voltage at point E

* r_Z also dictates the ***maximum current*** that the Zener can safely carry for a given $P_{Z,max}$
* In presence of r_Z :

$$P_{Z,max} = \left(V_Z + I_{Z,max} r_z\right) \times I_{Z,max} = V_Z I_{Z,max} + I_{Z,max}^2 r_Z$$

* For a given V_Z, $P_{Z,max}$, and r_Z, the maximum allowable Zener current $I_{Z,max}$ is obtained from the solution of this ***quadratic equation***
* Generally, in actual operation, the ***maximum*** current through the Zener diode is ***not allowed to exceed*** $I_{Z,max} / 2$ $\left(\text{using } \textbf{\textit{factor of safety}} = 2\right)$

Role of R_S:

* It is a ***current limit resistor***, and its role is immense
* It ***limits the maximum current*** that can flow through the Zener diode
  - $\Rightarrow$ Protects it from ***excessive power dissipation*** and consequent ***overheating***
  - $\Rightarrow$ Also, acts as a ***current limit*** for ***accidental short-circuit*** situation $\left(\text{i.e., } R_L = 0\right)$
* There are ***lower and upper limits*** of the values of R_S, denoted by $\boldsymbol{R_{S,min}}$ and $\boldsymbol{R_{S,max}}$, respectively

* $\boldsymbol{R_{S,min}}$ is dictated by the ***open-circuit condition*** (i.e., $R_L \rightarrow \infty$) under the ***maximum possible voltage*** at point E, since under such a condition, the Zener diode would carry the ***maximum amount of current***
* $\boldsymbol{R_{S,max}}$ is governed by the condition that the circuit should be able to deliver the ***required load current*** as well as the ***minimum Zener current*** (thus, sustaining its breakdown mode) for the ***lowest possible voltage*** at point E
* ***Note***: $\boldsymbol{R_{S,max}}$ ***is a function of*** $\boldsymbol{R_L}$

* For a given value of R_S, there is a corresponding ***range*** of values of R_L, beyond which the circuit operation is ***unsafe***
* Also, a practical Zener Voltage Regulator would have s***hort-circuit protection***, to safeguard it from ***accidental short-circuits***

Example: V_E varies between 10 V and 15 V, $V_Z = 5$ V, $I_{Z,min} = 1$ mA, $P_{Z,max} = 1$ W, $R_L = 100\ \Omega$, neglect r_Z, and factor of safety = 2. Find $R_{S,min}$ and $R_{S,max}$.

$$I_{Z,max} = P_{Z,max} / V_Z = (1\text{ W})/(5\text{ V}) = 200\text{ mA}$$

Using factor of safety 2, permissible $I_{Z,max} = 100$ mA

Load current $I_L = V_Z / R_L = (5\text{ V}/100\ \Omega) = 50$ mA

$I_L + I_{Z,min} = 51$ mA, and $V_{E,min} = 10$ V

$$\Rightarrow R_{S,max} = (V_{E,min} - V_Z)/(51\text{ mA}) = 98\ \Omega$$

Note: If R_S is greater than this value, then the Zener will starve for current, and proper circuit operation will be lost

$I_L + I_{Z,max} = 150\ \text{mA}$, and $V_{E,max} = 15\ \text{V}$

$\Rightarrow R_{S,min} = (V_{E,max} - V_Z)/(150\ \text{mA}) = 67\ \Omega$

Note: If R_S is lower than this value, then the Zener current will exceed the maximum permitted value

Thus, the allowed value of R_S ranges between $67\ \Omega$ and $98\ \Omega$

Exercise: Use any value of R_S outside this range, and show that either the Zener would starve for current or the current through the Zener would exceed its maximum permissible limit

Example: All data same as previous example, but now $R_S = 80\ \Omega$ (fixed). Find the allowed range of R_L.

The minimum value of current that can flow through $R_S = (V_{E,min} - V_Z) / R_S = 62.5$ mA

This current should be able to supply at least $I_{Z,min}$, as well as $I_{L,max}$

$\Rightarrow R_{L,min} = V_Z / (62.5\ \text{mA} - I_{Z,min}) = 81\ \Omega$

Similarly, the maximum current that can flow through $R_S = (V_{E,max} - V_Z) / R_S = 125$ mA

This current should supply $I_{L,min}$, as well as $I_{Z,max}$

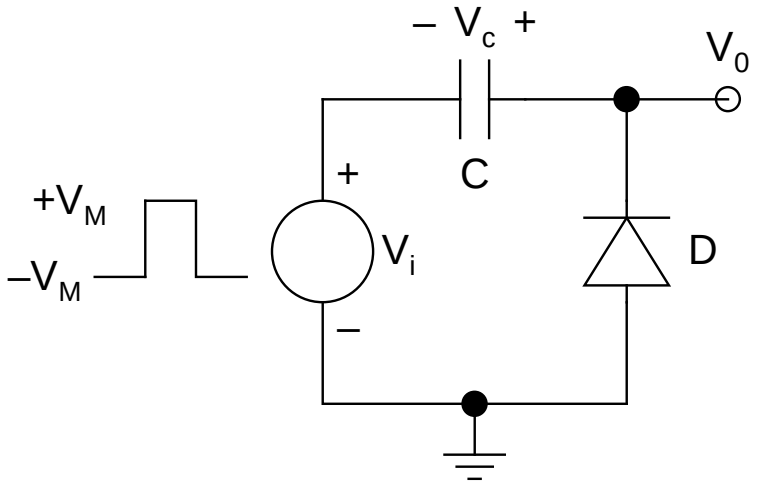
$\Rightarrow R_{L,max} = V_Z / (125\ mA - I_{Z,max}) = 200\ \Omega$

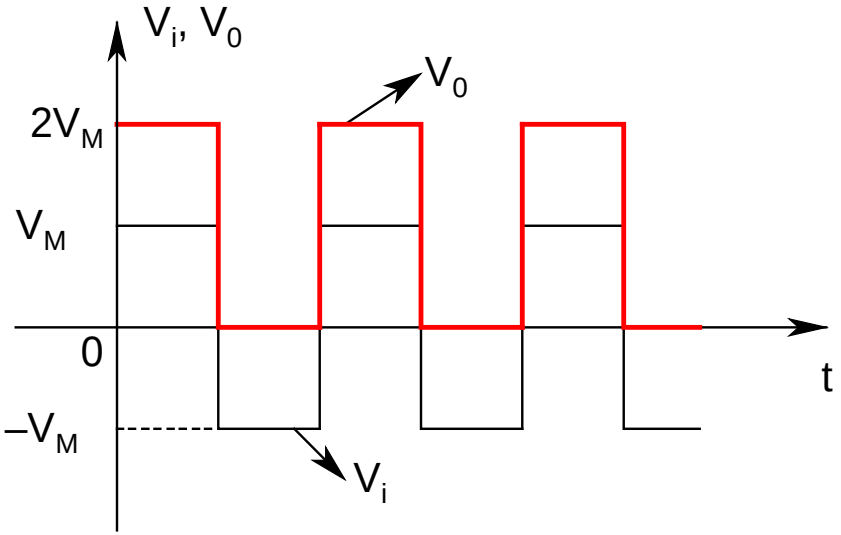
Thus, the allowed range of values of R_L should be between $81\ \Omega$ and $200\ \Omega$

Exercise: Use any value of R_L outside this range, and show that either the Zener would starve for current or the current through the Zener would exceed its maximum permissible limit

DC Restorator:

* This circuit is also known as ***DC Level Shifter*** or ***Diode Clamp***
* Used to add a certain amount of ***DC offset*** (either ***positive*** or ***negative***) to the input signal





Using 0th order model

* Assume ***ideal*** diode, and intially capacitor C was completely ***discharged*** (i.e., $V_c = 0$)
* V_i is a ***square wave*** having amplitude $\pm V_M$ and ***zero DC offset***
* For $V_i = -V_M$, D becomes ***forward biased*** and ***clamps*** V_0 to zero volts (using ***0th order model***)
* ***Note***: Under this condition, $\boldsymbol{V_c = +V_M}$
* For $V_i = +V_M$, D ***cuts off*** and $\boldsymbol{V_c}$ ***adds to*** $\boldsymbol{V_i}$ to produce $\boldsymbol{V_0 = 2V_M}$
* The circuit effectively ***doubles*** the input voltage amplitude $\Rightarrow$ also known as ***Voltage Doubler***

Observations:

* ***Note***: The circuit actually ***does not*** double the input voltage, rather it adds a ***DC offset*** equal to the ***amplitude*** of the input signal

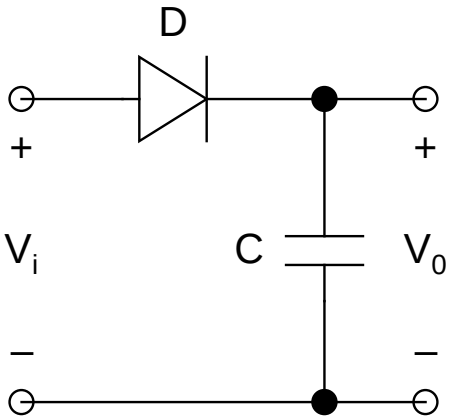
  $\Rightarrow$ The ***peak-to-peak*** value of V_0 remains the ***same*** as that of V_i

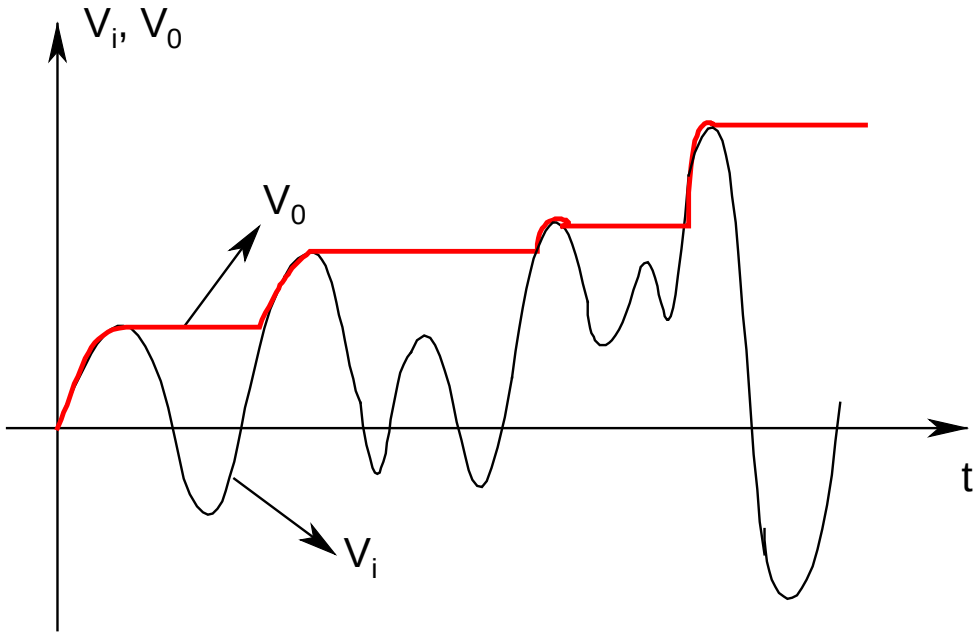
* V_i ***need not be symmetric***

* ***D can be reversed***

  $\Rightarrow$ V_0 would have ***positive peak*** clamped at ***0***, while the ***negative peak*** would be at $-2V_M$ with a ***DC offset of*** $-V_M$

Peak (or Envelope) Detector:



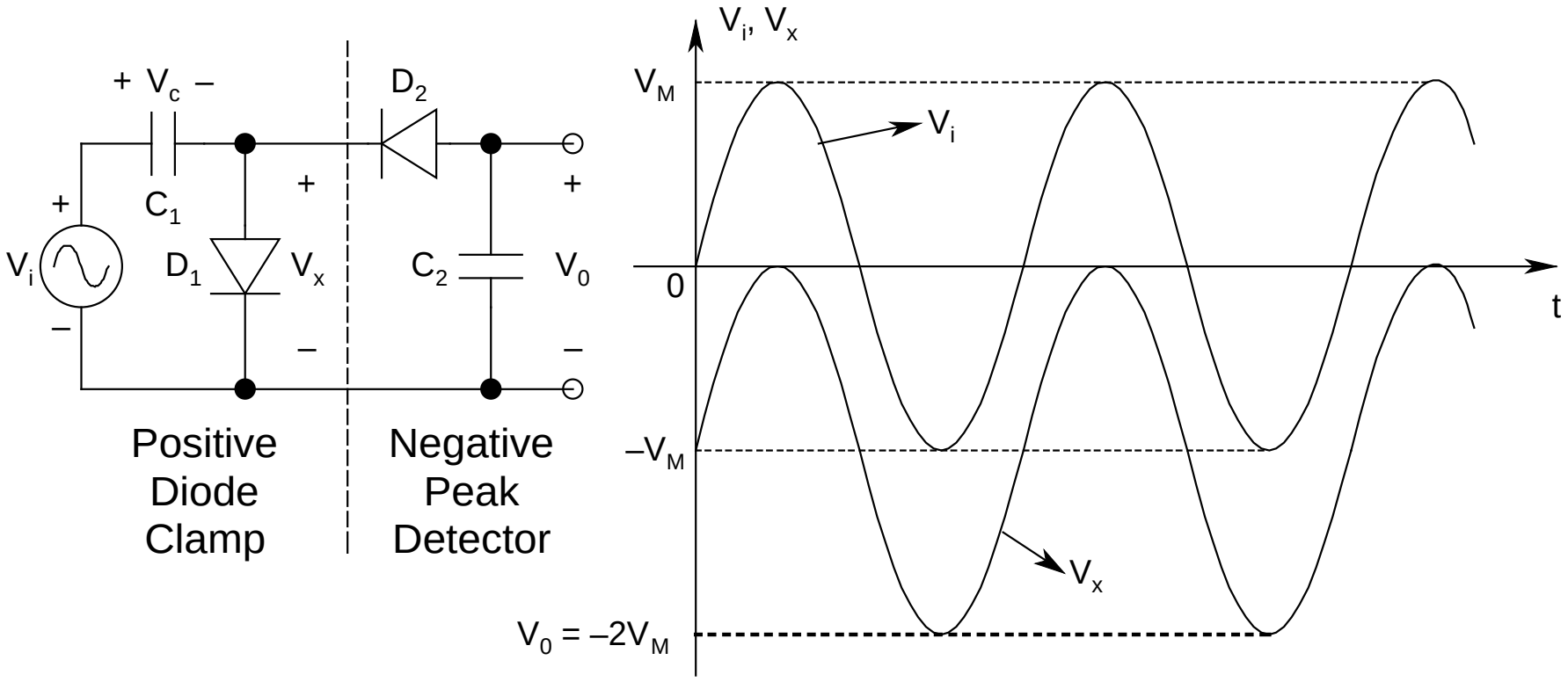


Using 0th order diode model

Also known as ***Sample and Hold Circuit***

* Similar to an ***HWR with a filter capacitor*** (C)
* Assuming that C is initially completely ***discharged***, V_0 will ***follow*** V_i whenever D is ***forward biased*** (assuming ***ideal*** diode)
* However, as soon as V_i starts to ***decrease*** beyond its ***maximum*** value, D immediately gets ***reverse biased***, and C ***stores*** the charge corresponding to the ***last peak value*** of V_i
* Very popular circuit earlier, however, is rarely used nowadays due to the availability of much better options

Peak-to-Peak Detector:



* Measures the ***peak-to-peak*** value of the input signal and ***holds*** (or ***clamps***) that value at the output
* Consists of ***two*** blocks:
  - A ***positive diode clamp*** (C_1-D_1), and
  - A ***negative peak detector*** (C_2-D_2)
* For ***positive*** V_i, D_1 gets ***forward biased***, ***clamps*** V_x at ***0 V***, and C_1 gets ***charged to*** V_M (i.e., $V_c = V_M$, ***carefully note the polarity***)
* Note that $V_x = -(V_c - V_i)$

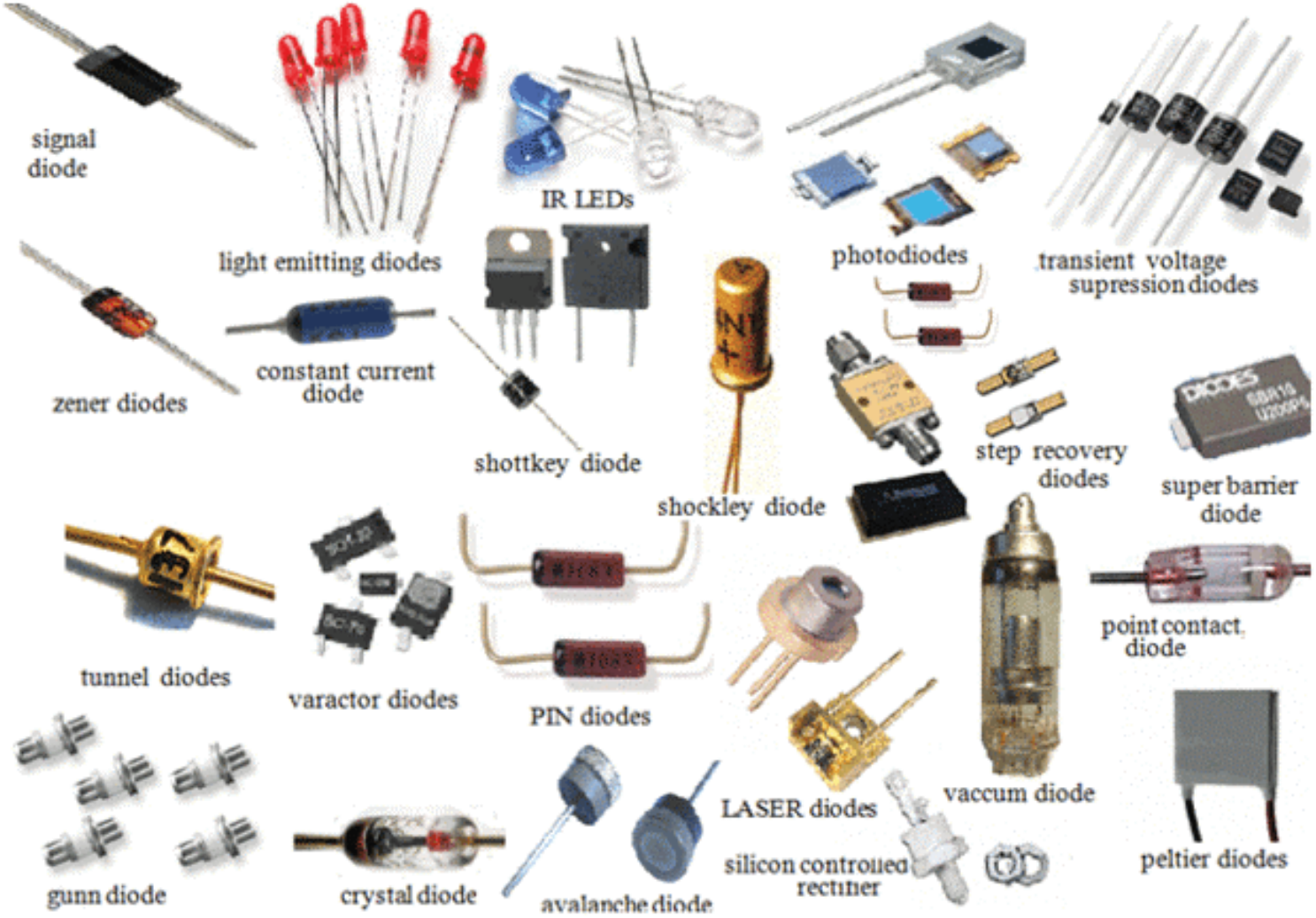
* ***V_c remains clamped at V_M,*** whereas the ***maximum*** and ***minimum*** values of V_i are $+V_M$ and $-V_M$ respectively

  $\Rightarrow$ ***V_x swings between 0 and $-2V_M$***

  $\Rightarrow$ ***V_0 gets clamped at $-2V_M$***

* Quite useful circuit to detect the ***peak-to-peak*** value of any input waveform

* ***Note that the input need not be symmetric***

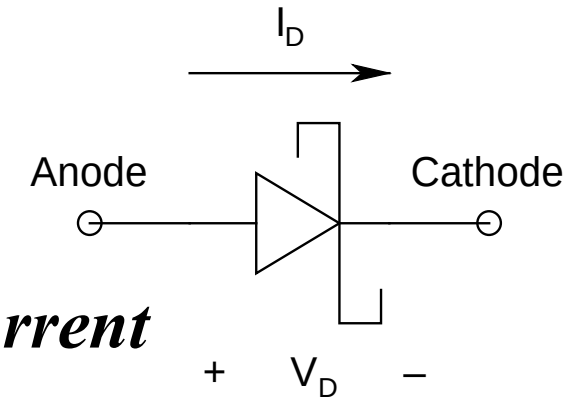


Types of Diode

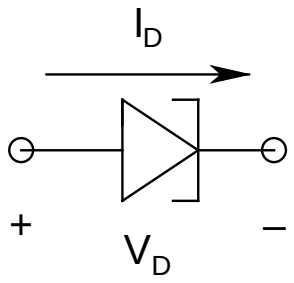
- ***Some Special Diodes***:
  - **Schottky Diode**
  - **Tunnel Diode**
  - **Varactor Diode**
  - **Light Emitting Diode (*LED*)**
  - **LASER Diode**
  - **Photodetector [*Photodiode* (*PD*)]**
  - **Solar Cell**

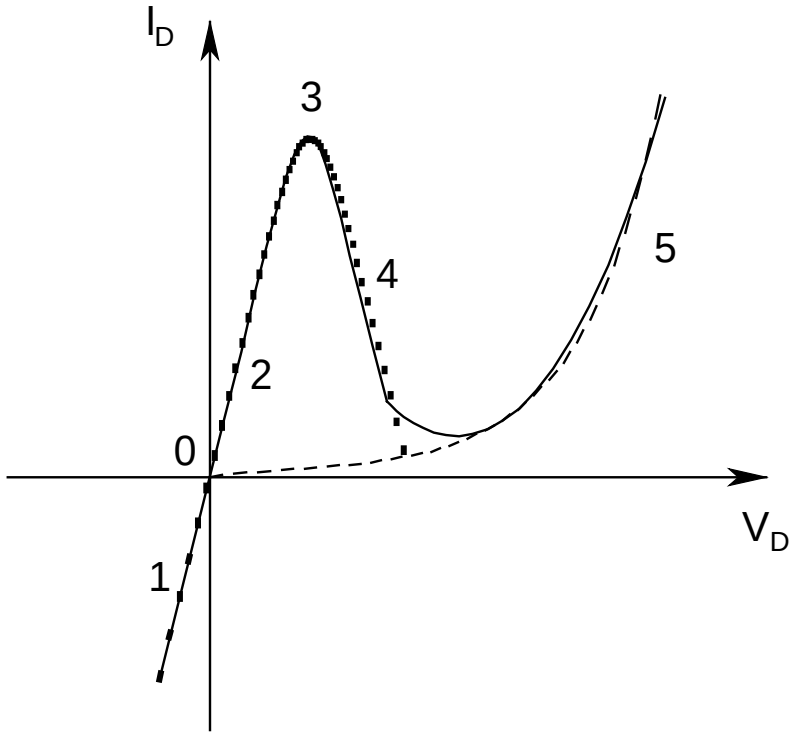
Schottky Diode:

* ***Metal-semiconductor junction***
* ***Low cut-in voltage*** ($V_\gamma \simeq$ 0.1-0.2 V)
* ***High reverse leakage current***
* Can carry ***large amount of forward current***
* ***Low reverse breakdown voltage***
* Exhibits ***low capacitance*** (***majority carrier device***)
* ***Excellent frequency response*** characteristic with ***very high cutoff frequency***
* Used in ***RF applications***



Tunnel Diode:



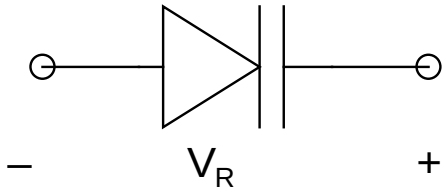


Note the negative resistance region (4),
as well as the reverse characteristic (1)

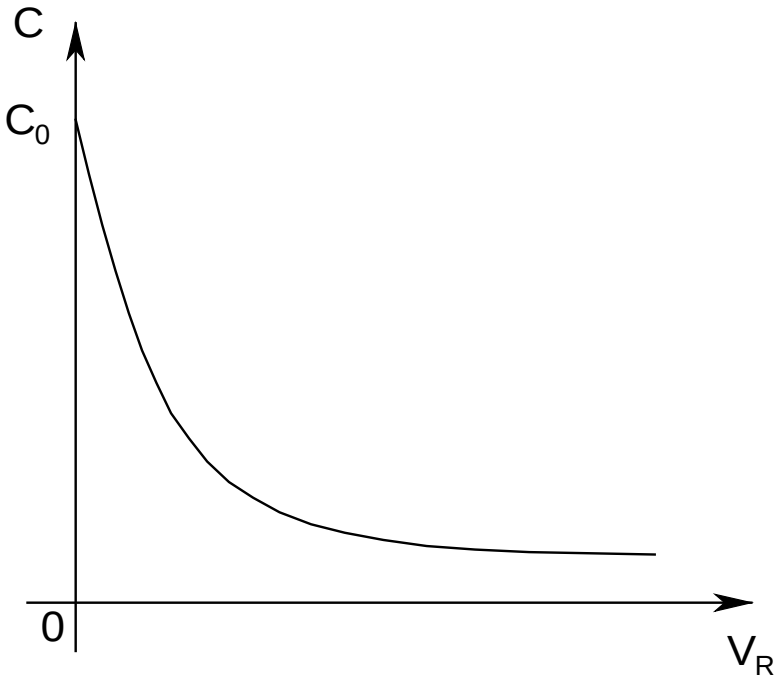
* Also known as ***Esaki diode***, named after its inventor Leo Esaki in 1957
* pn junction diode, with both sides ***very heavily doped,*** with a ***very thin junction depletion region***
* Shows peculiar ***negative resistance*** region in the current-voltage characteristic
* For both forward and reverse bias near zero, carriers ***tunnel*** freely across the junction, thus producing an almost ***linear*** (***resistive***) characteristic (1 and 2)

* Eventually, the current reaches a ***peak*** (3) and then starts to ***drop*** (4), yielding a ***negative resistance*** region!
* In the background, normal ***injection*** current of the diode flows, and finally takes over the characteristic (5)
* The ***reverse current never saturates***! (Thought to have ***zero reverse breakdown voltage***)
* Extremely ***fast*** device, with ***cutoff frequency*** as high as ***300 GHz***
* ***Usage***: **High-speed switching circuits**, **RF oscillators**

Varactor Diode:



Note the polarity
of the applied voltage



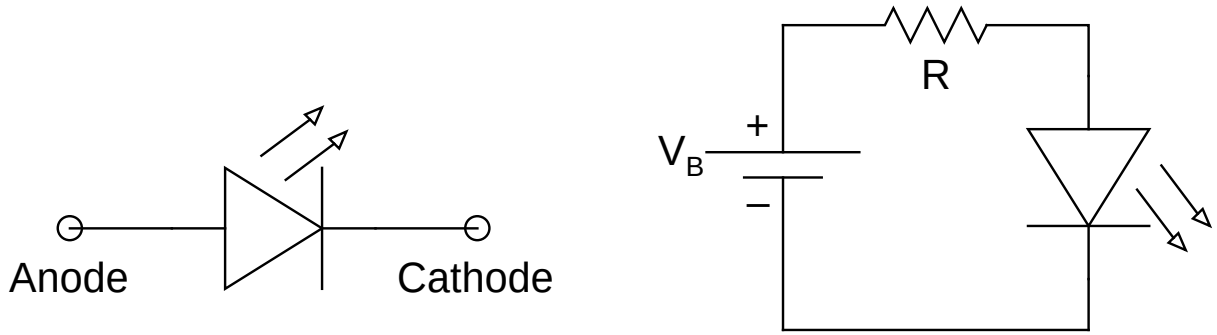
* Varactor $\rightarrow$ ***Variable Reactor***
* Also known as ***varicap diode***, ***varible capacitance diode***, ***variable reactance diode***, and ***tuning diode***

* Operated in ***reverse bias*** mode, with ***negligible current*** flowing through the device
* There is a ***capacitance*** around the junction, which ***decreases*** with an ***increase*** in the applied ***reverse bias***, following the relation $C \propto V_R^{-n}$, where n is either 1/2 or 1/3, depending on the ***type of junction***
* ***Usage***: **Tuning circuits**, **Voltage-Controlled Oscillators**
* Using special technology, $n = 2$ can be achieved

  $\Rightarrow$ ***Resonance frequency*** $\omega_0 = 1/\sqrt{LC} \propto V_R$

  $\Rightarrow$ A highly ***linear*** response can be obtained

Light Emitting Diode (LED):



* ***pn junction diode***, operated under ***forward bias***

  $\Rightarrow$ Significant amount of ***carrier injection***/***recombination***

* Energy lost due to recombination = ***Bandgap Energy*** (E_g)

  $\Rightarrow$ Carried away by ***photons*** (***quanta of light***)

* Known as ***electroluminescence***

* $E_g = h\nu = hc/\lambda \Rightarrow \lambda = hc/E_g = \boldsymbol{1.24/E_g}$

  λ in ***μm***, E_g in ***eV***

* λ for ***visible range ~ 400 nm to 760 nm***

  $\Rightarrow$ Corresponds to $\boldsymbol{E_g}$ ***of 1.63 to 3.1 eV***

* ***Color*** (λ in nm, material): ***Violet*** (***400-450***, ***InGaN***), ***Blue*** (***450-500***, ***ZnSe***), ***Green*** (***500-570***, ***GaP***), ***Yellow*** (***570-590***, ***GaAsP***), ***Orange*** (***590-610***, ***AlGaInP***), ***Red*** (***610-760***, ***AlGaAs***)

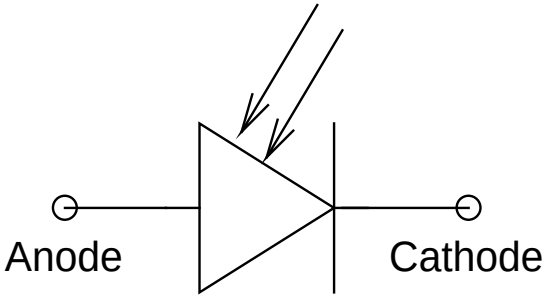
* Active device is coated with a ***transparent material*** (typically ***glass***) with ***anti-reflection coating***

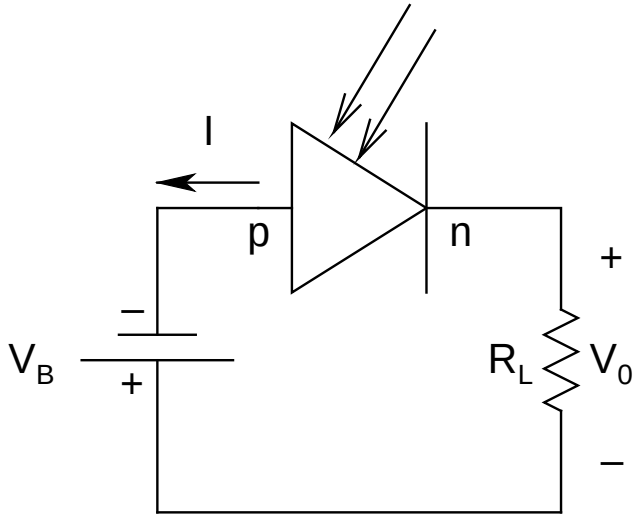
LASER Diode:

* **LASER**: ***Light Amplification by Stimulated Emission of Radiation***
* Symbol same as that of an LED
* The light emitted by LEDs is ***noncoherent*** (i.e., ***not in phase***) and ***nonmonochormatic*** (i.e., ***not having a single wavelength***)
* ***Usage***: **Fiber Optic Communication**, **laser printer**, **laser pointer**, **barcode reader**, **CD/DVD reader**, etc.

* In LASERs, the light emitted by the active device is made to go through ***repeated reflections*** through the use of ***two mirrors*** (called ***Bragg reflectors***) at the two ends of the ***optical cavity*** (creates a ***standing wave*** for the light), and eventually taken out through a ***Brewster mirror*** (a mirror tilted at ***Brewster angle***, which passes light only of a ***particular polarization***)
  $\Rightarrow$ ***intense coherent monochromatic light***
* ***Laser Power***: **10s of mW to 100s of mW**

Photodetector:



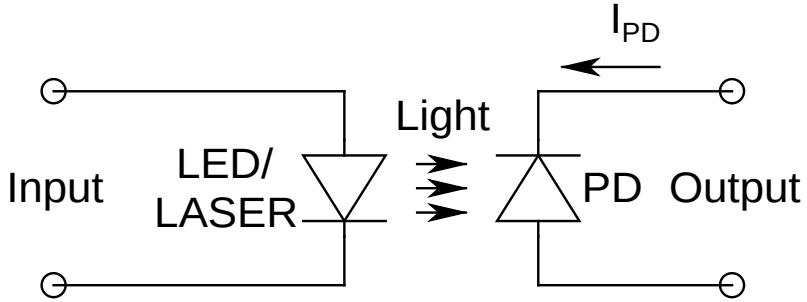


* Also known as ***photodiode*** (***PD***)
* Operation just ***opposite*** of LED: while ***LED*** produces ***light*** under ***forward bias***, ***PD*** (under ***reverse bias***) produces ***current*** when ***illuminated*** (***photovoltaic effect***)

* ***Magnitude*** of this current ***proportional*** to the ***intensity*** of the incident light
* Light breaks ***covalent bonds*** and create ***electron-hole pairs*** (***EHPs***), with ***electrons*** moving from ***p to n***, and ***holes*** moving from ***n to p***, due to the ***large electric field*** (created by ***reverse bias***) across the junction (recall that it points from ***n to p***)
* ***Usage***: **Burglar alarm**, **moving object counter**, **automatic street lights**, **fire and smoke detector,** etc.

An Interesting Application : Opto-Isolator:

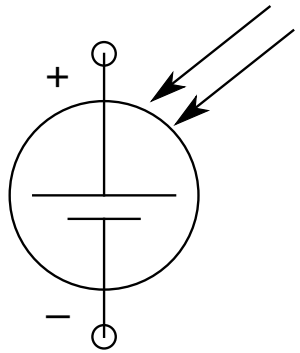
* Also known as ***opto-coupler***
* ***No*** electrical connection between input and output
  $\Rightarrow$ ***Total electrical isolation***



* The LED/LASER emits light, which is detected by the PD, and current (I_{PD}) ***proportional*** to the input light flows in the output circuit
* If due to some ***obstruction*** in the light path, the light gets ***blocked***, then I_{PD} ***dips***, and activates a ***relay***
  $\Rightarrow$ ***Perfect security system*** (**Burglar Alarm**)

Solar Cell:

* Normal Si ***pn*** junction diode
* Operates under the principle of ***photovoltaic effect*** $\Rightarrow$ converts ***optical energy*** to ***electrical energy***



* Very similar to PD, however, while PDs are ***reverse biased***, the solar cell act as a ***source of power***
* Incident light breaks ***covalent bonds*** and create ***EHPs***, which are ***separated*** by the ***junction electric field***, and gets ***collected*** by external contacts, creating a ***current***

* The current can either be made to ***flow through a load***, or be used to ***charge a battery***
* ***Open-circuit voltage*** of an individual cell is small ~ ***0.65-0.7 V***
* A large number of them are arranged in a ***series-parallel combination $\Rightarrow$ solar panel***
* ***Low efficiency*** (best reported so far ***~ 30%***)
* ***High cost***, but ***coming down exponentially***
* ***An extremely hot thrust area of research and development in renewable energy sources***