- ***Differential Current***:

$$\partial I_d = I_{d1} - I_{d2} = 2\xi$$

- ***Differential-Mode Output Voltage***:

$$V_{od} = V_{o1} - V_{o2} = (V_{DD} - I_{d1}R_D) - (V_{DD} - I_{d2}R_D)$$
$$= -(\partial I_d)R_D = -2\xi R_D$$

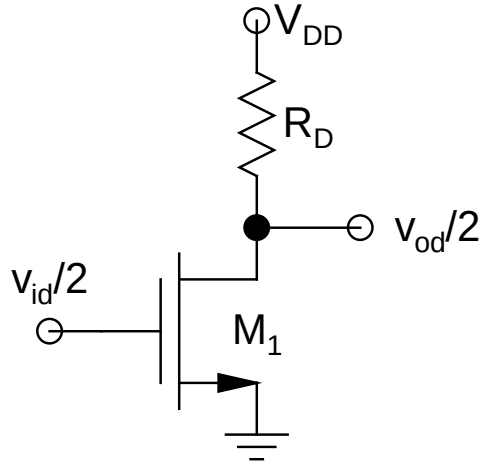
- ***Note***:
  - When $V_{id} = 0$, $\xi = 0$, $\partial I_d = 0$, and $V_{od} = 0$
  - *This is the perfect DC bias point*
  - *No need for interstage coupling capacitor*
  - $I_{D1} = I_{D2} = I_{SS}/2$
  - $V_{Id} = 0 \Rightarrow$ *Tie both gates to ground* and *use a negative power supply*

- ***ac Analysis***:
  - ***The procedure adopted for npn DA can be lifted verbatim***
- ***Differential-Mode Half-Circuit***: ***Calculation of A_{dm}***:
  - ***The common-source node is at ac ground*** (***from symmetry***)
  - ***Body is also at ac ground***

    $\Rightarrow v_{bs} = 0 \Rightarrow g_{mb} v_{bs} = 0$
  - ***Simple CS stage***:

    $\Rightarrow A_{dm} = v_{od}/v_{id} = -g_m R_D$

    $g_m = k_N \Delta V$

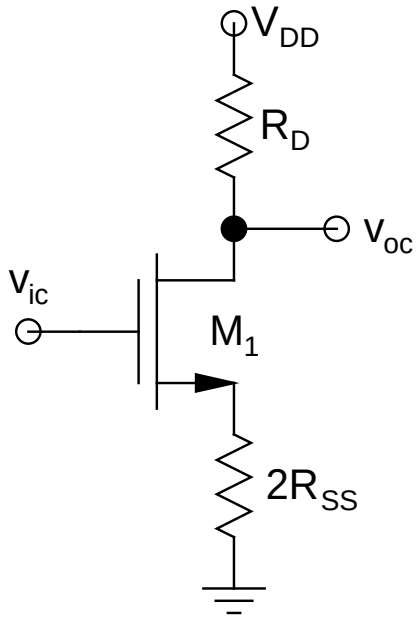


Differential-Mode Half-Circuit

- ***Common-Mode Half-Circuit***: ***Calculation of Acm***:
  - ***CS(D) stage***, but now ***with body effect present***

    $\Rightarrow A_{cm} = v_{oc}/v_{ic}$

    $= -g_m R_D/[1 + (g_m + g_{mb})2R_{SS}]$



Common-Mode Half-Circuit

- Thus:

  $CMRR = 20\log_{10}(|A_{dm}/A_{cm}|)$

  $\approx 20\log_{10}[2(g_m + g_{mb})R_{SS}]$

- Again, ***R_{SS} plays no role in A_{dm}***, but ***determines A_{cm} and CMRR***

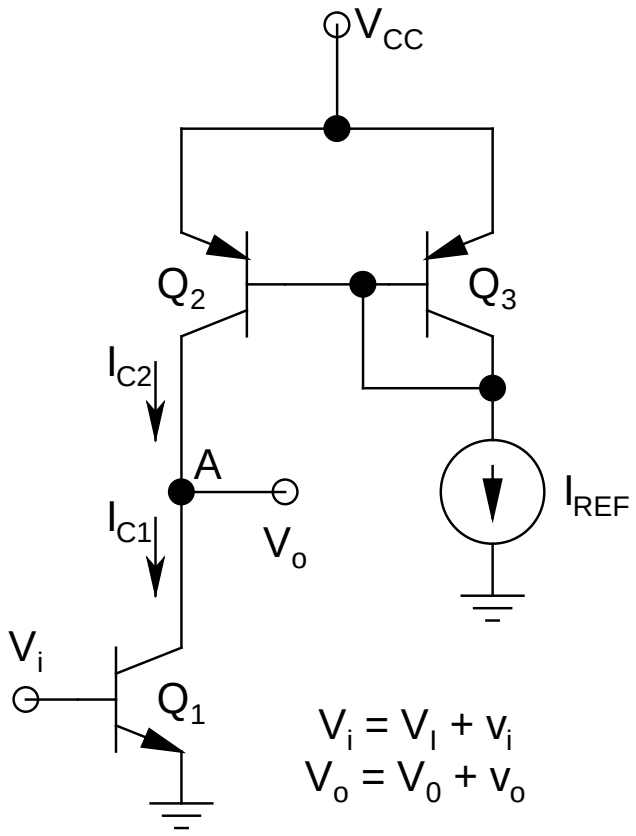
  $\Rightarrow$ ***A high value of R_{SS} highly desirable***

- ***Actual situation is not so rosy and hunky-dory***
- ***The DA can become unbalanced if there is a mismatch between the devices and/or the resistors, and our analysis would fail***!
- Gives rise to ***offset voltage*** (***for both npn and NMOS DA***) and ***offset current*** (***only for npn DA***)
- ***This mismatch is caused by technology and is totally random***
- ***Fortunately, the effect is not that severe, since there are technological innovations to match devices and/or resistors***

Actively Loaded Amplifier Stages

- ***Main Goal***: ***To reduce usage of resistors as much as possible*** and ***use transistors instead as active load***
- Interesting to note that ***transistors offer much higher resistance than physical resistors***, while ***occupying much smaller chip area***

- ***npn CE Stage With pnp Active Load***:
  - Q_1: ***Driver***, Q_2: ***Load***
  - Identify Q_2-Q_3 as a ***pnp current mirror***
  - Q_2-Q_3 constitute a ***matched pair***
  - ***Neglecting base currents***: $I_{C2} = I_{REF}$
  - ***Biasing of the circuit is tricky***



Circuit Diagram