Department of Electrical Engineering
Indian Institute of Technology, Kanpur

EE 210 **Home Assignment #11** **Assigned: 24.3.21**

1. For the NMOS source-coupled pair discussed in class, derive the expressions for I_{d1}, I_{d2}, and the linear range V_{id}, and compare them with those given in class.

2. Determine the required bias current (I_{SS}) and the device widths (i.e., W_1 and W_2) of an NMOS source coupled pair, as discussed in class, to have the following properties: i) g_m with $V_{id} = 0$ should be 1 mA/V, and ii) V_{id} of 200 mV should result in ΔI_d of 85% of the maximum value. Assume L = 1 μm, and $k'_N = 194\ \mu A/V^2$. Neglect body effect and channel length modulation effect.

3. Consider the bipolar active load CE amplifier circuit, as discussed in class. Neglecting base currents and assuming Q_2-Q_3 to be identical, find the required value of the dc bias voltage V_I to be applied at the base of Q_1 to satisfy the current relations and also to bias the transistors to give the best operating point. What is the corresponding base-emitter voltage of Q_2/Q_3? Find the ac small-signal midband voltage gain, and the output resistance. Assume $V_{CC} = 5$ V, $I_{REF} = 1$ mA, $I_{SN} = 10^{-16}$ A, $I_{SP} = 5 \times 10^{-16}$ A, $V_{AN} = 130$ V, and $V_{AP} = 52$ V.

4. Consider the NMOS CS amplifier stage with saturated enhancement load, as discussed in class. Find the required dc bias voltage to be applied at the gate of M_1 to satisfy the current relations and also to bias the transistors to give the best operating point. Find the ac small-signal midband voltage gain, and the output resistance. Assume $V_{DD} = 5$ V, $V_{TN0} = 0.6$ V, $k'_N = 40\ \mu A/V^2$, $\lambda_n = 0.2\ V^{-1}$, $(W/L)_1 = 25$, $(W/L)_2 = 1$, $2\phi_F = 0.6$ V, and $\gamma = 0.2\ V^{1/2}$.

5. Consider the NMOS CS amplifier stage with depletion load, as discussed in class. Choose the threshold voltage of the depletion load (i.e., M_2) such that even when the output is at its maximum value, the device should remain on with a cushion of 78 mV in its threshold voltage. Take other data from Prob.4, and repeat Prob.4.

6. Consider the MOS complementary active load CS amplifier circuit, as discussed in class. Assuming M_2-M_3 to be identical, find the required dc bias voltage to be applied at the gate of M_1 to satisfy the current relations and also to bias the transistors to give the best operating point. What is the corresponding gate-source voltage of M_2/M_3? Find the ac small-signal midband voltage gain, and the output resistance. Assume $I_{REF} = 100\ \mu A$, $(W/L)_N = 10$, $(W/L)_P = 20$, $V_{TP0} = -0.7$ V, $k'_P = 20\ \mu A/V^2$, and $\lambda_P = 0.15\ V^{-1}$. Take other required data from Prob. 4.

7. Consider the CMOS gain stage, as discussed in class. Assume that the dc value of the input voltage applied to the gate of the NMOS transistor is 2 V. Determine the amount of level shift required between the input and the gate of the PMOS transistor to yield dc quiescent value of the output voltage to be 2.5 V. Determine the ac small-signal midband voltage gain, and the output resistance. Take the required data from Probs. 4 and 6.