OUTPUT STAGES

- ***Main Purpose***:
  - ***To drive load with sufficient current***
- Both ***BJT*** and ***MOS*** output stages available
- ***BJT*** output stages preferred due to their ***large current handling capability***
- ***BiMOS*** circuits use ***MOS*** devices in the ***core*** of the circuit, while using ***BJT*** devices in the ***output*** stage
  - ***Best of both worlds***!

- ***Requirements***:
  - ***Sufficient drive current/power transfer to load***
  - ***Low output distortion***
  - ***Ideal voltage source***:
    - ***Thevenin equivalent***: V_0 ***with*** $R_0 \rightarrow 0$
  - ***Voltage gain*** A_v ***independent of load***
    - ***Ideally unity with no phase shift***
  - ***Low Standby*** (or ***Idling***) ***Power***
    - ***While not driving any load***
  - ***Should not degrade frequency response***

- ***High power conversion efficiency η***
  - η = (*average power delivered to load*)/(*average power drawn from supply*)

- ***Classification***:
  - ***Depends on the conduction angle*** (θ)
    - θ: ***Angle over the complete cycle (360°) for which either both or one of the output transistors are/is on***
  - ***Class A***:
    - $\theta = 360°$ and $\eta_{max} = 25\%$ (***large standby power***)
  - ***Class B***:
    - θ ***slightly less than*** $180°$ and $\eta_{max} = 78.5\%$ (***zero standby power***)

- ***Class AB***:
  - $\theta = 180°$ and $\eta_{max} \approx 78.5\%$ (***very small standby power***)
- ***Class C***:
  - $\theta << 180°$ (***used in RF applications***)
- There are ***other classes*** also, namely ***D***, ***E***, ***F***, ***G***, and ***H***
  - Used only in ***special cases***, e.g., ***pulse width modulated input***, ***lowering of distortion***, etc.
- In this course, we shall be discussing only about ***Class B*** and ***Class AB*** output stages

- ***Class B***:
  - Uses ***complementary*** set of output transistors (***npn and pnp***, ***NMOS and PMOS***)
  - One takes care of the ***positive half cycle***, while the other takes care of the ***negative half cycle***
  - ***θ slightly less than 180° for each***
  - ***Both output devices never ON simultaneously***
    - ***Zero standby power*** (***significant advantage***)
  - Also known as ***Push-Pull Stage***

- During ***positive half cycle***, the stage ***pushes current through load***
- During ***negative half cycle***, the stage ***pulls current away from load***
- ***Very high η_{max} of 78.5%***
- However, there is a ***very big limitation***, known as ***Crossover Distortion***
  - Also known as ***Deadband Distortion***
  - ***Occurs during zero crossings of the signal***
  - ***For BJT/MOS Class B stage***, the ***input voltage must at least equal V_γ (~ 0.6 V)/V_{TN}($|V_{TP}|$) (~ 0.7-1 V)*** for the ***output stage transistors to turn on***

- ***Class AB***:
  - ***Eliminates Crossover Distortion*** by ***prebiasing the output transistors***
    - ***They remain at the verge of conduction in the standby stage***
  - ***θ exactly equal to 180°***
  - ***η_{max} slightly less than 78.5%*** due to a ***small amount of standby power***
  - ***Extremely popular and most widely used***