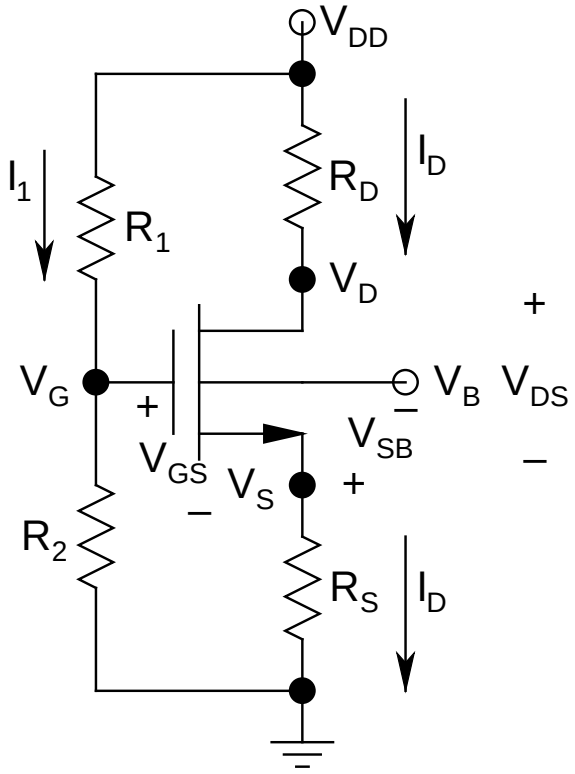
Discrete Stage Biasing: MOSFET

- ***Almost universally biased using 4-Resistor Bias***
- ***Significantly more complicated than BJT biasing, since there is no quick estimate***
- ***Also, body effect and CLM complicate matters***



- ***No I_G $\Rightarrow$ R_1-R_2 combination provides a perfect voltage division***

$$\Rightarrow V_G = \frac{R_2}{R_1 + R_2} V_{DD}$$

- $V_S = I_D R_S$ and $V_D = V_{DD} - I_D R_D$

$$\Rightarrow I_D = \frac{k_N}{2}\left(V_G - I_D R_S - V_{TN}\right)^2 \times \left(1 + \lambda\left[V_{DD} - I_D\left(R_S + R_D\right)\right]\right)$$

- Also:

$$V_{TN} = V_{TN0} + \gamma\left(\sqrt{2\phi_F + I_D R_S - V_B} - \sqrt{2\phi_F}\right)$$

- ***Extremely intimidating***!
- ***I_D equation becomes cubic***!
- ***Thus, bias calculation including all higher order effects is pretty tedious, and almost impossible for hand analysis***
- ***Need to make approximations***!

- Assume $\lambda V_{DS} < 0.1$:

$$\Rightarrow I_D = \frac{k_N}{2}\left(V_G - I_D R_S - V_{TN}\right)^2$$

- ***Even then it's quite complicated, since V_{TN} has a square root dependence on I_D***
- ***Tie B and S together*** $\Rightarrow V_{SB} = 0$ and $V_{TN} = V_{TN0}$
  - ***Note that it can't be done always***!

$$\Rightarrow I_D = \frac{k_N}{2}\left(V_G - I_D R_S - V_{TN0}\right)^2$$

- ***Even now, it's a quadratic equation in I_D***
- ***However, much easier to solve than earlier cases***
- ***No further simplification possible***!
- ***Solving, we will get 2 values of I_D: one will be the correct one***, while ***the other one will be unphysical***
- ***2 values of I_D will give 2 different values of V_{GS}: one > V_{TN0}*** and the ***other < V_{TN0}***

- ***Obviously, I_D for $V_{GS} < V_{TN0}$ is completely meaningless, since the device is off under that condition***
- Compute V_{DS} [= $V_{DD} - I_D(R_S + R_D)$]
  - ***Should be > V_{GT} (saturation mode)***
  - ***For BB, $V_{DS} = V_{DD}/3$***
- $P_D = V_{DD} \times (I_D + I_1)$ [$I_1 = V_{DD}/(R_1 + R_2)$]
- ***Here, no constraints on R_1 and R_2, and they can be made as large as physically possible to reduce I_1, and thus P_D***

IC Stage Biasing

- ***Avoids resistors as much as possible***
  - ***Resistors take up very large area on IC chips, which is at a premium***
- ***Uses transistors as biasing elements***
  - ***Much more compact than resistors***, and ***area consumption is almost negligible as compared to resistors***
- Also known as ***active biasing***

- ***Parameters***:
  - ***Output Current I_0***
    - ***As per specification***
  - ***Output Resistance R_0***
    - $R_0 = \Delta V_0/\Delta I_0 = dV_0/dI_0 = v_0/i_0$ (***ac***)
    - ***As large as possible*** - ***ideally infinite***
  - ***Minimum Allowed Output Voltage $V_{0,min}$***
    - ***As small as possible*** - ***ideally zero***
    - ***Dictated by***:
      - ***For BJT***: $V_{CE}(\text{min}) = V_{CE}(\text{SS}) = 0.2$ V
      - ***For MOSFET***: $V_{DS}(\text{min}) = V_{GT}(\text{min}) = 80$ mV