- ***DC Biasing***:
  - $V_i = V_I + v_i$ (V_I: ***DC bias voltage***, v_i: ***ac small-signal voltage***)
  - $I_c = I_C + i_c$ (I_C: ***DC bias current***, i_c: ***ac small-signal current***)
  - ***The ideal DC bias point should be $V_{I1} = V_{I2}$***

    $\Rightarrow$ $I_{C1} = I_{C2} = I_{EE}/2$
  - ***Thus, any arbitrary DC voltage can be applied at the bases of Q_1-Q_2, provided they are same***

    $\Rightarrow$ ***Ideal choice***: ***ground***

    $\Rightarrow$ ***Necessitates a negative power supply for proper biasing***

- ***Under this condition***:

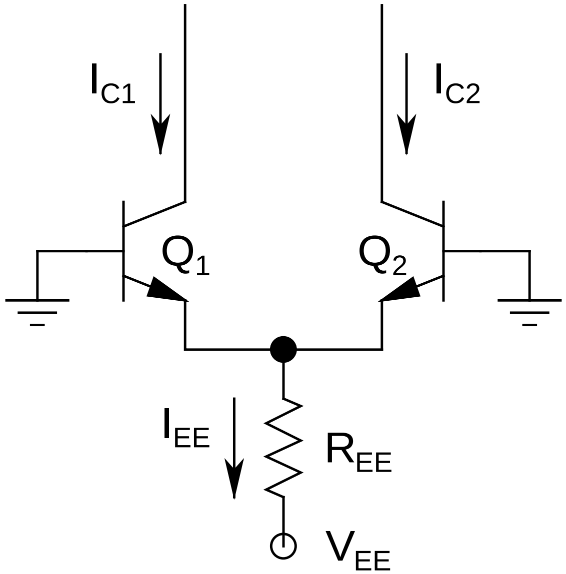
  $V_{01} = V_{02} = V_{CC} - I_{EE}R_C/2$ and $V_{0d} = 0$

- ***The simplest DC biasing scheme is to attach a resistor R_{EE} from the common emitter point to V_{EE}***:

  $\Rightarrow I_{EE} = (-0.7 - V_{EE})/R_{EE}$

  and $I_{C1} = I_{C2} = I_{EE}/2$

  $\Rightarrow$ ***Both Q_1 and Q_2 have same g_m, r_E, r_π, and r_0***



Simplest DC Biasing Scheme for npn DA

- ***To improve performance, any of the current sources discussed earlier could be used in place of R_{EE}***

- ***A check is needed to see that Q_1 and Q_2 are biased in the forward active region***
- For this circuit, for ***best biasing***:

  $V_{CE1} = V_{CE2} = (V_{CC} + |V_{EE}|)/3$ (***3-element o/p branch***)

> ***ac Analysis***:

- ***Balanced DAs have perfect symmetry around the vertical cut-line going through the middle of the circuit***
- ***Can be analyzed using heuristics***
  - Known as the ***Half-Circuit Technique***
- ***This technique is based on an algorithm***

  (***Understand it thoroughly to get a clear grasp***!)

- ***Algorithm for the Half-Circuit Technique***:
  - ***Apply inputs v_{i1} and v_{i2} at the bases of Q_1 and Q_2 respectively***
  - ***Outputs v_{o1} and v_{o2} taken from the collectors of Q_1 and Q_2 respectively***
  - Define $v_{id} = (v_{i1} - v_{i2})$ as the ***pure differential-mode input***
  - Define $v_{ic} = (v_{i1} + v_{i2})/2$ as the ***pure common-mode input***
  - Thus:

    $v_{i1} = v_{id}/2 + v_{ic}$

    $v_{i2} = - v_{id}/2 + v_{ic}$

- Define $v_{od} = (v_{o1} - v_{o2})$ as the ***pure differential-mode output***
- Define $v_{oc} = (v_{o1} + v_{o2})/2$ as the ***pure common-mode output***
- Thus:

  $v_{o1} = v_{od}/2 + v_{oc}$

  $v_{o2} = - v_{od}/2 + v_{oc}$
- ***Now, assuming that pure differential-mode and pure common-mode signals are completely non-interacting***:
  - ***Pure differential-mode output can only be caused by a pure differential-mode input***
  - ***Pure common-mode output can only be caused by a pure common-mode input***

- Based on these, define:
  - ***Differential-Mode Gain***: $A_{dm} = v_{od}/v_{id}$
  - ***Common-Mode Gain***: $A_{cm} = v_{oc}/v_{ic}$
- Thus, from the ***principle of superposition***:
  - $v_{o1} = (A_{dm}/2)v_{id} + A_{cm}v_{ic}$
  - $v_{o2} = -(A_{dm}/2)v_{id} + A_{cm}v_{ic}$
- Thus, ***each output carries both differential- and common-mode signals***, however, the ***differential-mode signals are out of phase***, whereas the ***common-mode ones are in phase***
- ***Hence, the difference between the two outputs carries only the differential-mode signal, with a gain double that of a single output***