Department of Electrical Engineering
Indian Institute of Technology, Kanpur

EE 210 **QUIZ 2B** **16.4.21**
Total Marks: 15 **Total Time: 30 Mins.**

Transistor pairs M_1-M_2, M_3-M_4, and Q_5-Q_6 are perfectly matched. The stage is to be designed to have CMRR of 80 dB, subjected to the following requirements and constraints:

* M_1 and M_2 must operate with g_m of 80 μA/V.
* I_{C6} must be 8 μA (DC).

a) Evaluate the required values of R_1, R_2, and $(W/L)_1$ [= $(W/L)_2$]. **9**

b) For your designed circuit:
   i) Estimate the magnitude of the common-mode gain ($|A_{cm}|$). **4**
   ii) Determine the DC power dissipation. **2**

Negect body effect and DC base current, and assume that $\lambda|V_{DS}| << 1$ (for both NMOS and PMOS).

Other data: *for npn*: $\beta = 100$, $V_A = 130$ V; *for NMOS*: $k'_N = 40$ μA/V^2, $\lambda_n = 0.01$ V^{-1}; *for PMOS*: $\lambda_p = 0.012$ V^{-1}.

No other data required if you attempt the problem correctly. ☺