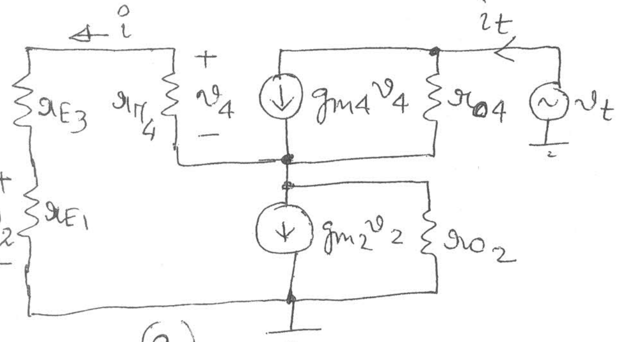
EE 210

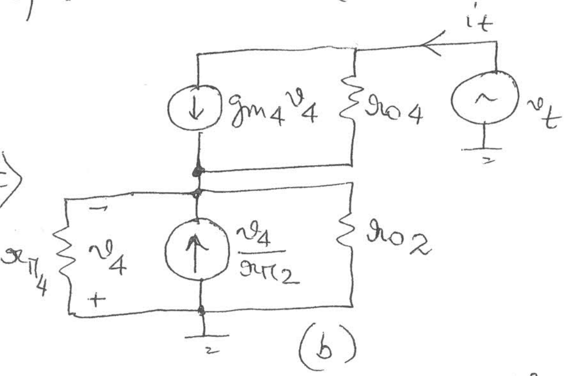
Solⁿ to HA #7

1. Assuming $R \gg (r_{E1}+r_{E2})$, where $r_E = 1/g_m$, & $r_E \| r_\pi \simeq r_E$, the eqv. ckt. is shown in (a) & the simplified eqv. is shown in (b).



(a)

$\Rightarrow$



(b)

From (a): $v_4 = -i\, r_{\pi 4}$, $v_2 = i\, r_{E1} \Rightarrow v_2 = -\frac{r_{E1}}{r_{\pi 4}} v_4 \simeq -\frac{v_4}{\beta}$.

$\therefore g_{m2}v_2 = -g_{m2}\frac{v_4}{\beta} = -\frac{v_4}{r_{\pi 2}}$ ($\because r_{\pi 2} = \beta/g_{m2}$).

$(r_{E1}+r_{E3})$ appears in series with $r_{\pi 4}$, & can be assumed to be much smaller than $r_{\pi 4}$ $\Rightarrow$ we get eqv. (b).

Current source $\frac{v_4}{r_{\pi 2}}$ is proportional to the voltage appearing across itself $\Rightarrow$ simply behaves like a resistor $r_{\pi 2}$. This appears in parallel with $r_{\pi 4}$, producing an eqv. $r_\pi/2$ ($\because r_{\pi 2} = r_{\pi 4} = r_\pi$). Also, $r_{o2} \gg \frac{r_\pi}{2} \Rightarrow$ the eqv. resistance is simply $r_\pi/2$.

The resultant ckt. should be quite familiar to us, & by inspection

$$R_o = \frac{v_t}{i_t} = r_{o4}\left(1+g_{m4}\frac{r_\pi}{2}\right) = r_{o4}\left(1+\frac{\beta}{2}\right) \simeq \frac{\beta r_{o4}}{2} \quad (\text{assuming } \beta/2 \gg 1).$$

This is exactly half of the value given in class (βr_o).

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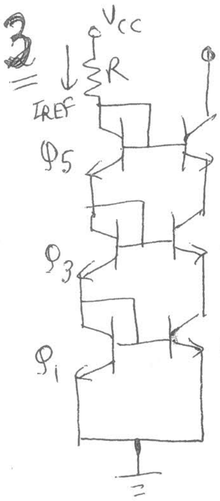
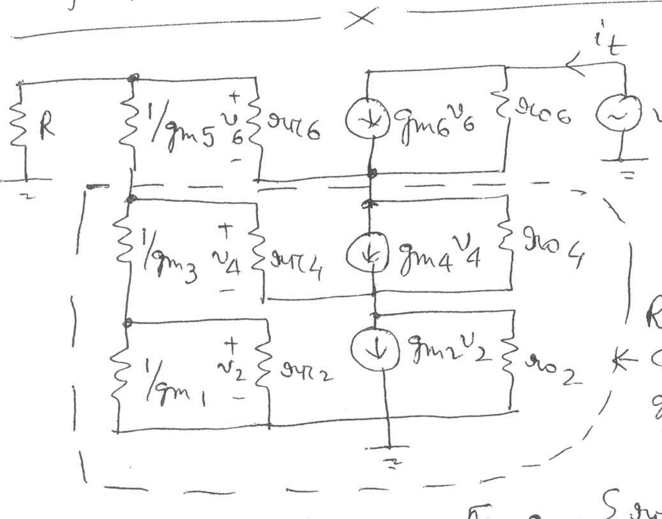
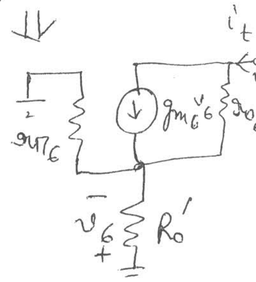


$\Rightarrow$



Neglecting the small resistance $1/g_{m5}$, the base of Q_6 is at ac ground.

$\Downarrow$



By inspection, $R_o = \frac{v_t}{i_t} = r_{o6}\left[1+g_{m6}\{r_{\pi 6} \| R_o'\}\right]$

$r_{\pi 6} \ll R_o' \Rightarrow R_o \simeq r_{o6}(1+g_{m6}r_{\pi 6}) \simeq \beta_0 r_{o6}$ (same as a normal cascode).

Try to figure out physically why R_o does not increase for a BJT double cascode.

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2 All devices have same g_m & r_o, ∵ all devices are identical, & they are carrying the same current. Also, assuming $\lambda V_{DS} \ll 1$ (an extremely prudent assumption, unless V_{DS} is very high), $g_m = \sqrt{2K_n'\left(\frac{W}{L}\right)I_D} = \underline{3.16 \times 10^{-4}\,\mho}$.

$\lambda = \frac{1}{L}\frac{dX_d}{dV_{DS}}$, which gives $\underline{\lambda = 0.0125\ V^{-1}} \Rightarrow r_o = \frac{1}{\lambda I_D} = \underline{800\ k\Omega}$.

The overall output resistance of NMOS Cascode Current Source:

$R_o = g_m r_o^2 = \underline{202.24\ M\Omega}$ (mind-bogglingly high!).

The open-ckt. voltage of a current source, by definition, $V_{OC} = I_o \times R_o = \underline{20.22\ kV}$!!

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4 $I_{REF} = \frac{V_{CC} - V_{BE1}}{R_1} = \frac{V'}{R_1}$, where $V' = V_{CC} - V_{BE1}$. Also, $V_{BE1} = V_{BE2} + I_o R_2$.

$\Rightarrow I_o R_2 = V_{BE1} - V_{BE2} = V_T \ln \frac{I_{REF}}{I_o}$. The total resistance in the ckt $R = R_1 + R_2$

$= R_1 + \frac{V_T}{I_o}\ln\frac{I_{REF}}{I_o} = R_1 + \frac{V_T}{I_o}\ln\frac{V'}{I_o R_1}$. To find min R, take derivative of this

eqn. w.r.t. R_1, & plug it to zero $\Rightarrow$ $\underline{R_1 = \frac{V_T}{I_o}}$ & $\underline{R_2 = \frac{V_T}{I_o}\ln\frac{V'}{V_T}}$.

These are the reqd. expressions of R_1 & R_2 that would give min. total resistance.

Now, for the values given, $\underline{R_1 = 5.2\ k\Omega}$ & $\underline{R_2 = 36.5\ k\Omega}$. These values seem to be practical, however, with this value of R_1 (5.2 kΩ), $I_{REF} = 5.6$ mA, resulting in the total power drawn from the supply $= V_{CC} \times I_{REF} = 169$ mW, which is too high. ∴ In practical applications with high values of V_{CC}, in order to reduce the power dissipation, R_1 is increased, & R_2 is accordingly tailored in order to get the desired output current.

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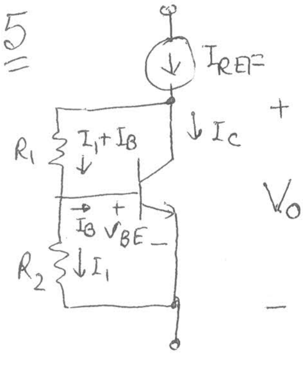

$V_o = (I_1 + I_B)R_1 + V_{BE}$ (refer to the fig.) $= \left(1 + \frac{R_1}{R_2}\right)V_{BE} + I_B R_1$

∵ $I_1 = \frac{V_{BE}}{R_2}$. Also, $I_{REF} = I_1 + I_B + I_C$, with $I_C = \beta I_B$.

$\Rightarrow I_B = \frac{1}{\beta + 1}\left(I_{REF} - \frac{V_{BE}}{R_2}\right)$. Substituting I_B back in V_o,

$$V_o = \left(1 + \frac{R_1}{R_2}\right)V_{BE} + \frac{R_1}{(\beta+1)R_2}\left(I_{REF}R_2 - V_{BE}\right)$$

which is the reqd. expression to prove.

Substituting the given values, $\boxed{V_o = 7 + \frac{2.7}{\beta + 1}}$. Note that the nominal value of V_o (neglecting base current) is $V_o = \left(1 + \frac{R_1}{R_2}\right)V_{BE} = \underline{7V}$.

Considering base current, $V_o = \underline{7.245\ V}$ ($\beta = 10$), $\underline{7.053\ V}$ ($\beta = 50$), $\underline{7.027\ V}$ ($\beta = 100$), $\underline{7.014\ V}$ ($\beta = 200$), & $\underline{7.011\ V}$ ($\beta = 250$).

Thus, as β increases, V_o approaches its nominal value of 7 V.

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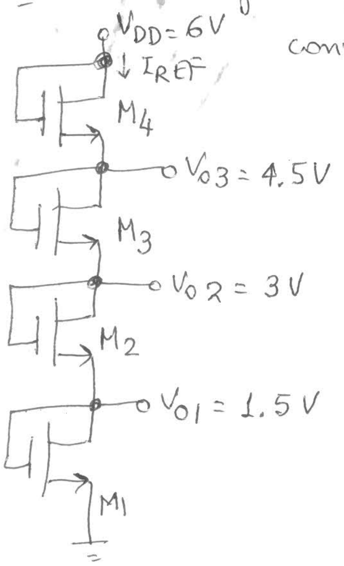
6 $\because$ 3 voltage references are needed, $\therefore$ we need 4 transistors. All bodies are connected to ground. $V_{TN1} = V_{TN0} = \underline{\underline{0.7V}}$. $V_{BS2} = -V_{O1} = -1.5V \Rightarrow$



$V_{TN2} = \underline{\underline{0.97V}}$, $V_{BS3} = -V_{O2} = -3V \Rightarrow V_{TN3} = \underline{\underline{1.15V}}$, $V_{BS4} = -V_{O3} = -4.5V \Rightarrow V_{TN4} = \underline{\underline{1.29V}}$. $V_{GS1} = V_{O1} = \underline{\underline{1.5V}}$, $V_{GS2} = V_{O2} - V_{O1} = \underline{\underline{1.5V}}$, $V_{GS3} = V_{O3} - V_{O2} = \underline{\underline{1.5V}}$, $V_{GS4} = V_{DD} - V_{O3} = \underline{\underline{1.5V}}$. Thus, for this particular case, all transistors operate with same value of V_{GS}. $V_{DS1} = V_{DS2} = V_{DS3} = V_{DS4} = \underline{\underline{1.5V}}$ ($\because V_{GS} = V_{DS}$ for all transistors).

Now, $\Delta V_1 = V_{GS1} - V_{TN1} = \underline{\underline{0.8V}}$, $\Delta V_2 = V_{GS2} - V_{TN2} = \underline{\underline{0.53V}}$, $\Delta V_3 = V_{GS3} - V_{TN3} = \underline{\underline{0.35V}}$, $\Delta V_4 = V_{GS4} - V_{TN4} = \underline{\underline{0.21V}}$.

i) Choose M_1 to be of min. size $\Rightarrow$ $\boxed{W_1 = L_1 = MFS = 1\mu m}$

$I_{REF} = \frac{K_n'}{2}\left(\frac{W}{L}\right)_1 \Delta V_1^2 (1 + \lambda V_{DS1}) = \frac{40}{2} \times 1 \times 0.8^2 \times (1 + 0.1 \times 1.5) = \underline{\underline{14.72\mu A}}$

Thus, $\left(\frac{W}{L}\right)_2 = \frac{14.72 \times 2}{40 \times 0.53^2 \times (1 + 0.1 \times 1.5)} = \underline{\underline{2.28}}$ $\boxed{L_2 = 1\mu m \quad W_2 = 2.28\mu m}$

$\left(\frac{W}{L}\right)_3 = \frac{14.72 \times 2}{40 \times 0.35^2 \times (1 + 0.1 \times 1.5)} = \underline{\underline{5.22}}$ $\boxed{L_3 = 1\mu m \quad W_3 = 5.22\mu m}$

$\left(\frac{W}{L}\right)_4 = \frac{14.72 \times 2}{40 \times 0.21^2 \times (1 + 0.1 \times 1.5)} = \underline{\underline{14.5}}$ $\boxed{L_4 = 1\mu m \quad W_4 = 14.5\mu m}$

Total Power Drawn $= 14.72\mu A \times 6V = \underline{\underline{88.32\mu W}}$ Total area $= \Sigma(WL) = \underline{\underline{23\mu m^2}}$

ii) Choose M_4 to be of min size $\Rightarrow$ $\boxed{W_4 = L_4 = 1\mu m}$

$I_{REF} = \frac{40}{2} \times 1 \times 0.21^2 \times (1 + 0.1 \times 1.5) = \underline{\underline{1\mu A}}$

Thus, $\left(\frac{W}{L}\right)_3 = \frac{1 \times 2}{40 \times 0.35^2 \times (1 + 0.1 \times 1.5)} = 0.35$ $\boxed{W_3 = 1\mu m \quad L_3 = 2.82\mu m}$

$\left(\frac{W}{L}\right)_2 = \frac{1 \times 2}{40 \times 0.53^2 \times (1 + 0.1 \times 1.5)} = 0.15$ $\boxed{W_2 = 1\mu m \quad L_2 = 6.46\mu m}$

$\left(\frac{W}{L}\right)_1 = \frac{1 \times 2}{40 \times 0.8^2 \times (1 + 0.1 \times 1.5)} = 0.068$ $\boxed{W_1 = 1\mu m \quad L_1 = 14.72\mu m}$

Total Power Drawn $= \underline{\underline{6\mu W}}$ (Dramatic saving from case i), $88.32\mu W$)

Total area $= \Sigma(WL) = \underline{\underline{25\mu m^2}}$ (almost identical to case i)

The reason why design ii) is better, because we chose that transistor to be of min. size, which has the least value of ΔV. $\because I_D \propto \left(\frac{W}{L}\right)$ & ΔV^2, $\therefore$ min. values of WL & ΔV can be utilized to produce the least I_{REF}, resulting in least power dissipation. The total area, to a first order, is independent of what transistor is chosen to be min. sized in the one!

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