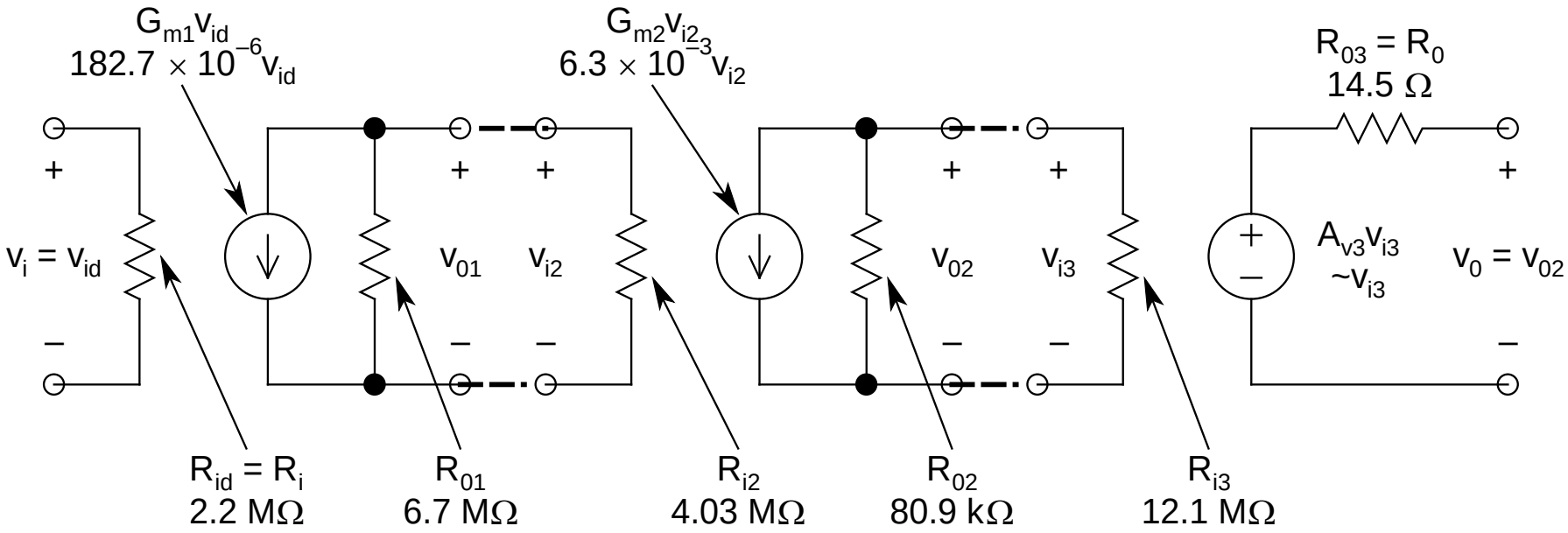
➢ *Overall Performance*:

- Just *cascade* the *2-port equivalents* of the *three stages*



Complete 2-Port Representation of 741 Op-Amp

- ***Voltage gain of the input stage***:

  $A_{v1} = v_{01}/v_{id} = -G_{m1}(R_{01}||R_{i2}) = -459.7$

- ***Voltage gain of the gain stage***:

  $A_{v2} = v_{02}/v_{01} = -G_{m2}(R_{02}||R_{i3}) = -506.3$

- ***Voltage gain of the output stage***:

  $A_{v3} \sim 1$

- Thus, the ***overall voltage gain*** of ***741 op-amp***:

  $A_{vOL} = v_0/v_{id} = (v_0/v_{i3}) \times (v_{i3}/v_{i2}) \times (v_{i2}/v_{id})$

  $= 2.33 \times 10^5$ (107.3 dB)

  Note: $v_{i3} = v_{02}$, and $v_{i2} = v_{01}$

- This is an ***excellent value***, in spite of the ***significant loading effect*** of the ***gain stage*** on the ***input stage***

➢ *Observations*:

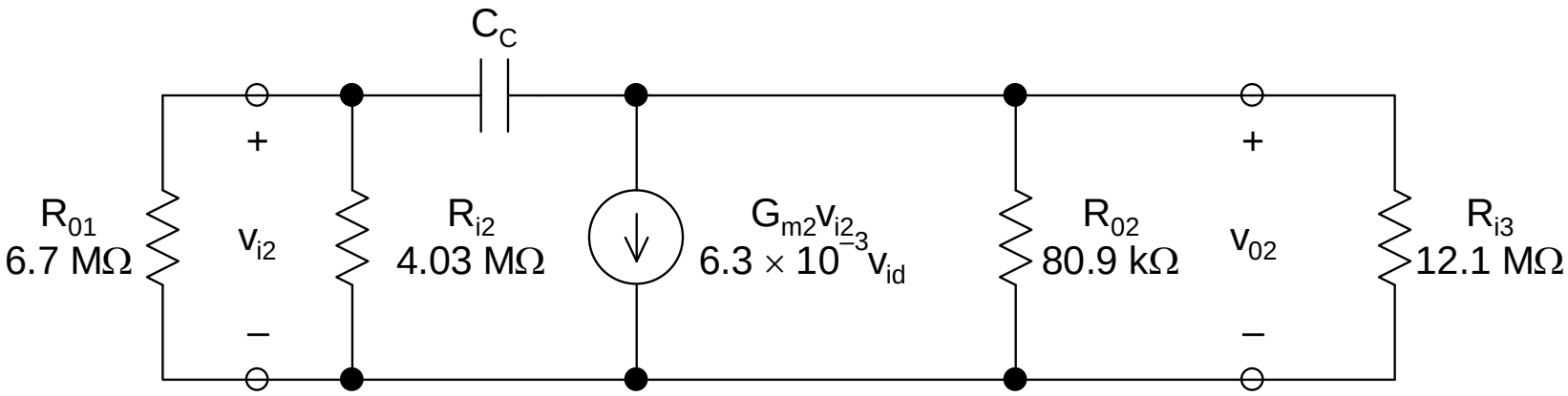
- A_{vOL} is actually the ***differential-mode gain*** (A_{dm})
- It is ***positive***
  - ❖ ***Positive*** v_{id} produces ***positive*** v_0
  - ❖ ***Bases*** of Q_1 and Q_2 are termed as ***non-inverting*** (+) and ***inverting*** (–) terminals respectively
- ***Input and output resistances*** are 2.2 MΩ and 14.5 Ω respectively, both of which are ***excellent values***
- The ***exact value*** of A_{cm} is ***slightly difficult to evaluate***, however, an ***estimate of CMRR can be made***
- Using the ***result*** of our ***simple analysis*** of ***DA***:

  $CMRR \approx 2g_{m1}r_{08} = 1923$ (66 dB)
- This is not too bad!
  - ❖ ***Actual value is much higher than this***

- ***Compensation***:
  - Actual evaluation of the ***frequency response*** characteristic of 741 is a ***huge task***, even with the ***ZVTC technique***
  - There will be ***numerous poles and zeros***, out of which, some will be ***important***, while others will be ***inconsequential***
  - However, there will of course be a ***Dominant Pole*** (DP), and rough calculation shows that it is ~ ***1 MHz***, which is the ***bandwidth*** of the ***uncompensated op-amp***

- Now, ~ ***100 dB open-loop gain*** with ***1 MHz bandwidth*** is a ***ready recipe for disaster*** as far as the ***stability of the system*** is concerned
- Hence, for ***unconditional stability*** under ***unity negative feedback***, e.g., ***voltage follower***, ***compensation is imperative***
- In 741, this task is accomplished by the technique of ***Dominant Pole Compensation*** (DPC) through the use of the ***compensation capacitor*** C_C, ***connected between the input and output of the gain stage***

- To obtain the ***required value*** of C_C, we use the cascade of the ***2-port networks***, as was done earlier to compute the ***overall voltage gain***



- Denote $R' = R_{01} || R_{i2} = 2.5\ M\Omega$ and $R'' = R_{02} || R_{i3} = 80.4\ k\Omega$

- The ***simplified circuit*** can be easily identified as the ***three-legged creature***, and using the ***ZVTC technique***:

$$R_C^0 = R' + R'' + G_{m2} R' R'' = 1.27\ G\Omega$$

- Now, to get an estimate of the ***DPF*** f_d, we assume that the ***open-loop gain*** is exactly 100 dB, and the ***first pole*** of the ***uncompensated op-amp*** is ***exactly 1 MHz***

$$\Rightarrow f_d = 10\ \text{Hz}$$

- Also, $f_d = \omega_d/(2\pi)$, with $\omega_d = 1/\tau$, and

$$\tau = R_C^0 C_C$$