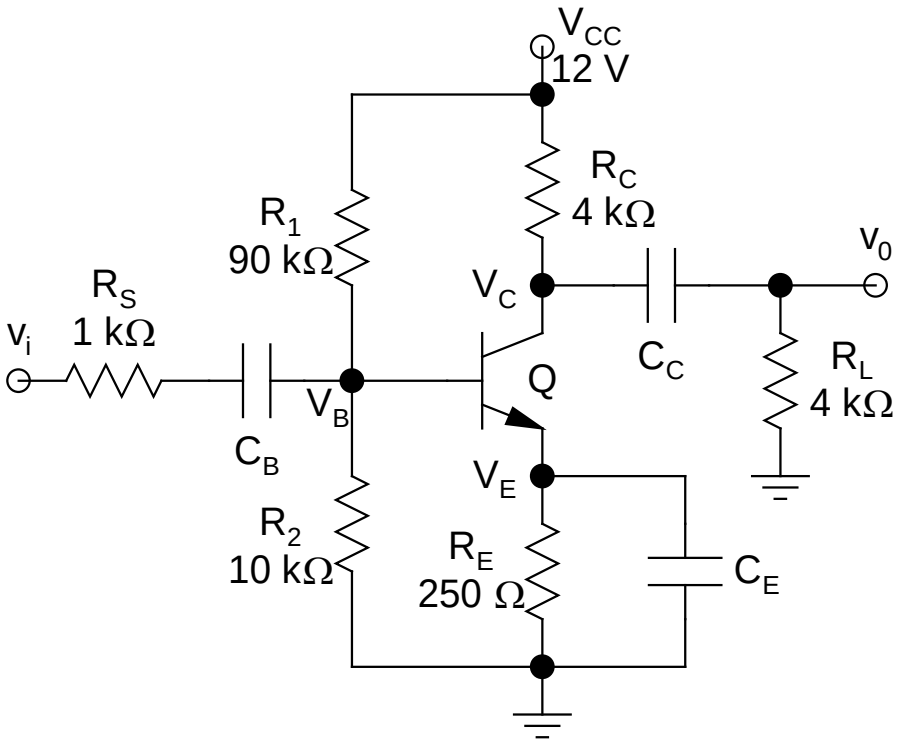
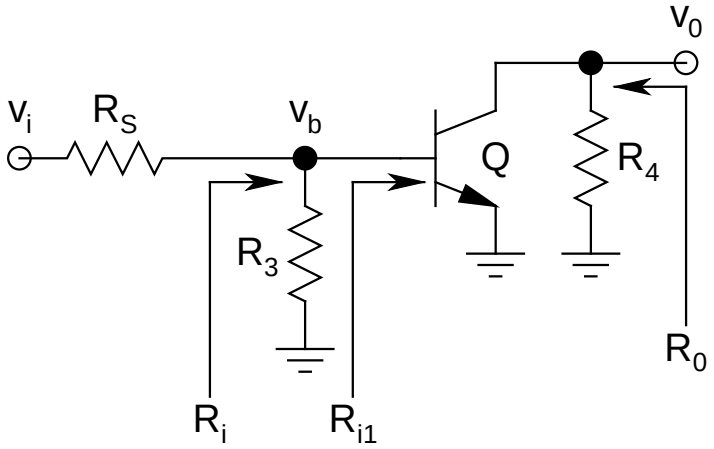




Complete Circuit

ac Midband Schematic

C_B: Base Blocking Capacitor , C_C: Collector Coupling Capacitor
C_E: Emitter Bypass Capacitor , R_S: Source Resistance , R_L: Load Resistance

- C_B,C_C: Used for ***DC isolation*** of the ***bias circuit*** from ***the source and the load***
  - ***DC biasing becomes independent of source and load***
- C_E: ***Plays no role in DC*** (***opens up***), but ***shorts out R_E in ac*** (will see its effects later)
- These 3 capacitors dictate the ***lower cutoff frequency*** (f_L) of the circuit
- Typically have values in the order of ***μF to 100s of μF*** in order to give ***f_L as close to 0*** (***DC***) as possible

- First need to do the ***DC analysis*** to find the ***operating point***
- ***All capacitors open up for DC analysis***
  - ***R_S and R_L play no role***
- ***Neglecting base current***:

$V_B = V_{CC}R_2/(R_1 + R_2) = 1.2$ V

$\Rightarrow V_E = V_B - V_{BE} = 0.5$ V

$\Rightarrow I_E \approx I_C = V_E/R_E = 2$ mA

$V_C = V_{CC} - I_C R_C = 4$ V

$V_{CE} = 3.5$ V (***quite close to $V_{CC}/3$***)

- ***DC bias point analysis done***!

- Now we can move on to the ***ac analysis***
- ***All capacitors get shorted*** due to their ***high values***, assuming ***frequency of operation*** is ***beyond f_L*** and ***less than f_H***, i.e., ***midband range***
- ***C_E bypasses R_E***

  $\Rightarrow$ ***Emitter of Q goes to ground***

  $\Rightarrow$ ***R_E plays no role in ac analysis***
- ***Refer to the ac schematic***
  - $R_3 = R_1 \| R_2 = 9\ k\Omega$
  - $R_4 = R_C \| R_L = 2\ k\Omega$
- ***Need β for ac analysis*** (***choose 100***)

- $r_E = V_T/I_C = 13\ \Omega$, and $r_\pi = \beta r_E = 1.3\ k\Omega$
- $R_{i1} = r_\pi = 1.3\ k\Omega$
- $R_i = R_{i1} \| R_3 = 1.14\ k\Omega$
- Total resistance ***seen*** by $v_i = R_S + R_i = 2.14\ k\Omega$
- For calculation of ***voltage gain*** A_v, apply ***chain rule***:

$A_v = v_0/v_i = (v_0/v_b) \times (v_b/v_i)$

$v_0/v_b = - R_4/r_E = - 153.85$ (***CE stage***)

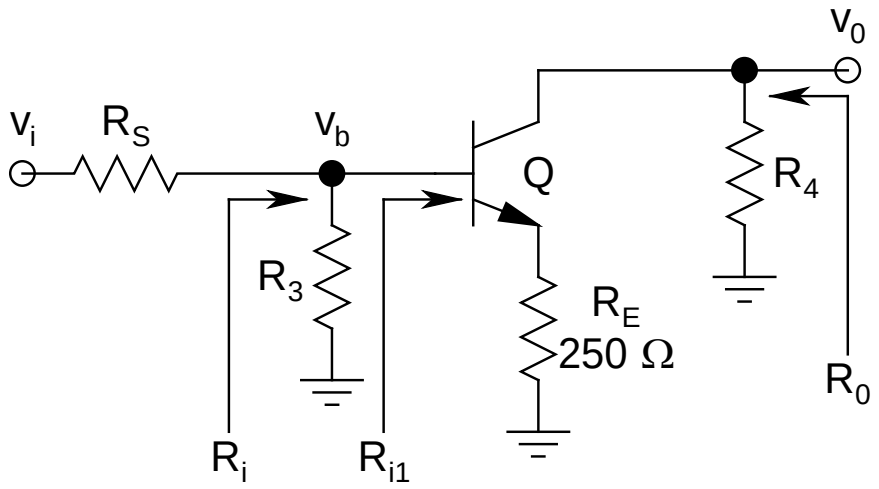
$v_b/v_i = R_i/(R_i + R_S) = 0.533$

$\Rightarrow A_v = - 82$ (***Very Good Gain***!)

- Note that v_i and v_0 are ***exactly out of phase***, which is expected from a ***CE stage***
- $R_0 = r_0 \| R_4 \approx R_4 = 2\ k\Omega$

  (since for ***discrete circuits***, r_0 is generally ***neglected***)
- ***This completes the analysis of the stage***
- ***Summary***:
  - $A_v = -82$
  - $R_i = 1.14\ k\Omega$
  - Resistance ***seen*** by $v_i = 2.14\ k\Omega$
  - $R_0 = 2\ k\Omega$

- Now let's explore what happens if ***C_E were absent***, i.e., ***R_E unbypassed***
- Redraw the ***ac schematic***:



ac Midband Schematic for R_E unbypassed