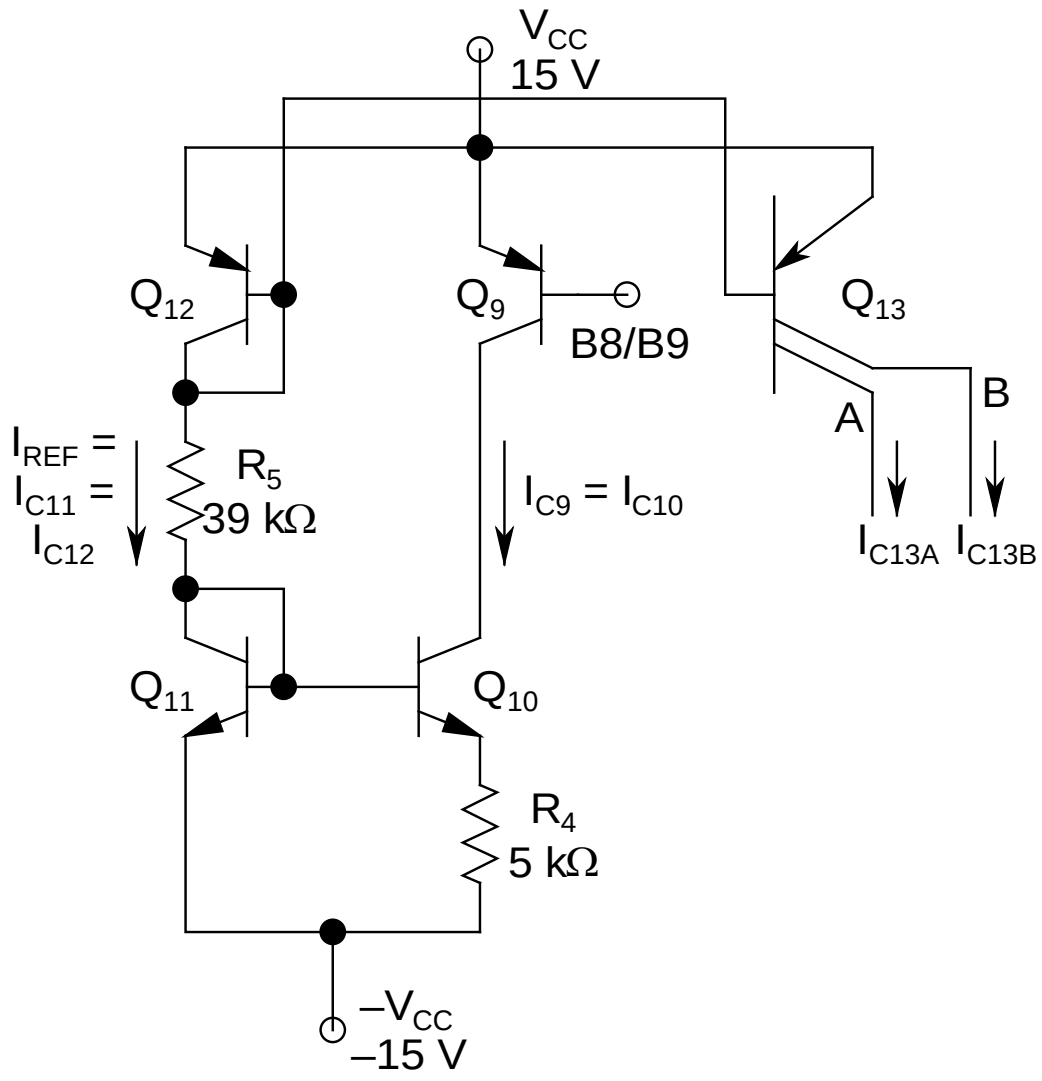
- Next is ***identification of modules***
- Q_{10}-Q_{11}-R_4 can be identified as the ***Widlar current source***
- Current through Q_{10} is ***same*** as that of Q_9, which forms a ***mirror configuration*** with Q_8
- Current through Q_8 ***biases the DA***, which is the ***combination*** of Q_1-Q_4
- Q_5-Q_6-R_1-R_2 ***combination*** can be identified as a ***ratioed mirror*** with the ***keep-alive resistor*** R_3 and the ***base current boost*** provided by Q_7

- ***Output of the DA*** is fed to Q_{16}-Q_{17}-R_8-R_9 combination, which is a ***CC-CE Darlington***, and acts as the ***gain stage***
- The ***output of the gain stage*** is fed to the ***Class-AB output stage***, consisting of:
  - Q_{14} and Q_{20}: ***Complementary output transistors***
  - Q_{18}-Q_{19}-R_{10}: ***Prebias circuit for the output stage***
  - Q_{15}-Q_{21}-R_6-R_7: ***Short-circuit protection circuit***
- Q_{13}, Q_{22}-Q_{24}, and the unnumbered 50 kΩ resistor have ***special roles***, which we will discuss about later

- ***DC Analysis***:
  - ***Assumptions***:
    - ***Neglect base current and Early effect***
    - ***Both + and – input terminals grounded***
      - ***Recall that is is the most preferred DC biasing arrangement for DAs***
    - Q_1-Q_2, Q_3-Q_4, Q_8-Q_9, and Q_{10}-Q_{11} ***perfectly matched***
    - ***±15 V power supply***
  - ***Reference branch*** (Q_{11}-Q_{12}-R_5) ***current***:

$$I_{REF} = I_{C11} = I_{C12} = [V_{CC} - V_{EB12} - V_{BE11} - (-V_{CC})]/R_5 = 733.3\ \mu A$$



DC Biasing of the Main Branches