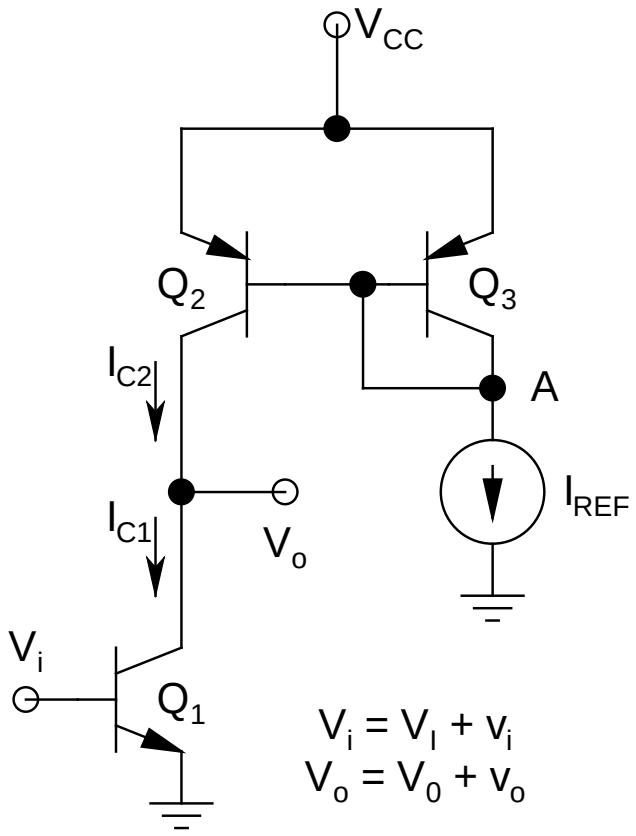
- ***npn CE Stage With pnp Active Load***:
  - Q_1: ***Driver***, Q_2: ***Load***
  - Identify Q_2-Q_3 as a ***pnp current mirror***
  - Q_2-Q_3 constitute a ***matched pair***
  - ***Neglecting base currents***: $I_{C2} = I_{REF}$
  - ***Biasing of the circuit is tricky***



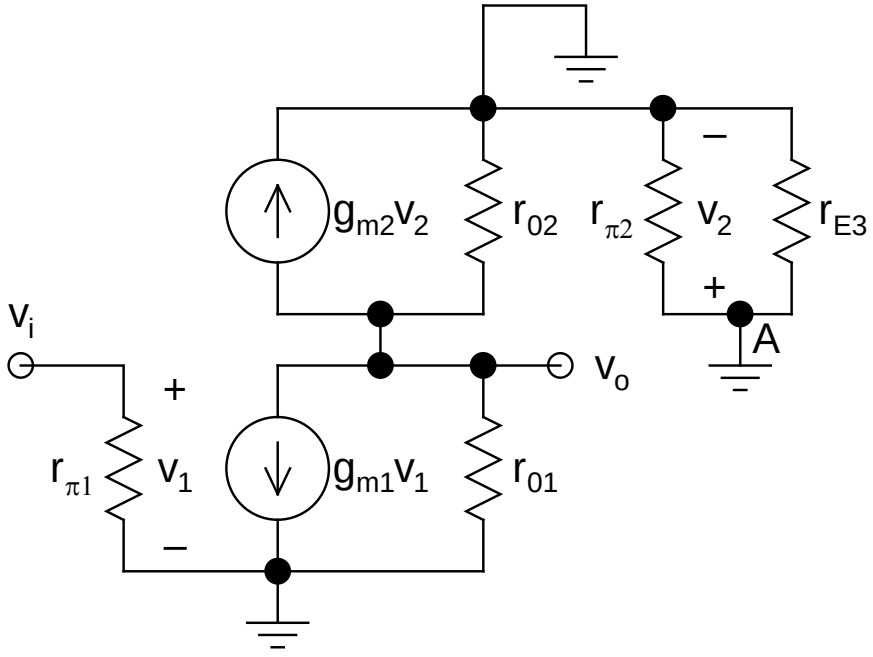
Circuit Diagram

- There is a ***trivial solution*** of $I_{C1} = I_{C2} = 0$, and the ***circuit collapses***
- For ***proper biasing***, I_{C1} ***must equal*** I_{C2} $(= I_{REF})$
- Thus, V_I ***should be properly adjusted***, such that:

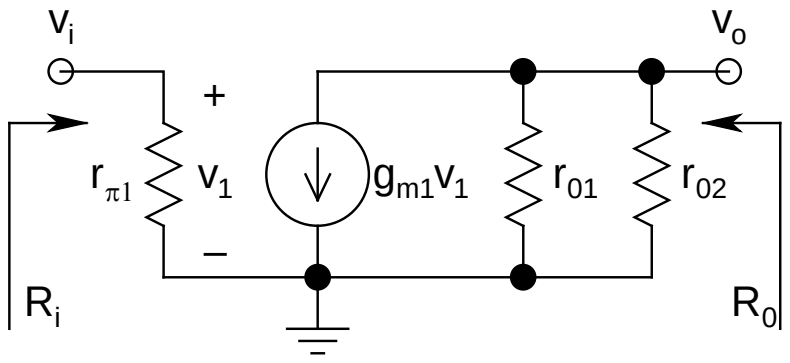
  $V_I = V_T \ln(I_{REF}/I_{S1})$
- ***Such a high precision in*** V_I ***may not be practically achievable***

  $\Rightarrow$ ***Use a resistor in series with*** V_I ***and self-consistently solve for the bias point***

➢ *ac Analysis*:



ac Midband Equivalent



Simplified Equivalent

- First, note that Q_3 is ***diode-connected*** (***BC short***)

  $\Rightarrow$ The ***equivalent*** of Q_3 is simply a ***resistor*** r_{E3}
- ***Node A*** is a peculiar one, and can be considered ***open or short both***!
  - ***Open because the current source I_{REF} is ideal***
  - ***Short because the base of Q_2-Q_3 is at a fixed DC potential, and thus ac ground***
- In either case, ***$v_2 = 0 \Rightarrow g_{m2}v_2$ disappears***!

  $\Rightarrow$ Leads to the ***simplified equivalent***
- ***By inspection***: $R_i = r_{\pi 1}$ and $R_0 = r_{01} \| r_{02}$
- $A_v = v_o/v_i = - g_{m1}R_0 = - 1/(\eta_n + \eta_p)$

  $\eta_n = V_T/V_{AN}$ and $\eta_p = V_T/V_{AP}$
- ***Enormously large gain possible***!

p-channel MOSFET (PMOS)

- Before moving to ***NMOS stages with active load***, it will be prudent to visit some details regarding ***PMOS***
- ***Substrate***: ***n-type*** (N_D)
  - ***Bulk Potential***:

    $\phi_F = V_T \ln(N_D/n_i)$
- ***Source/Drain***: p^+
- ***Channel Carriers***: ***Holes***