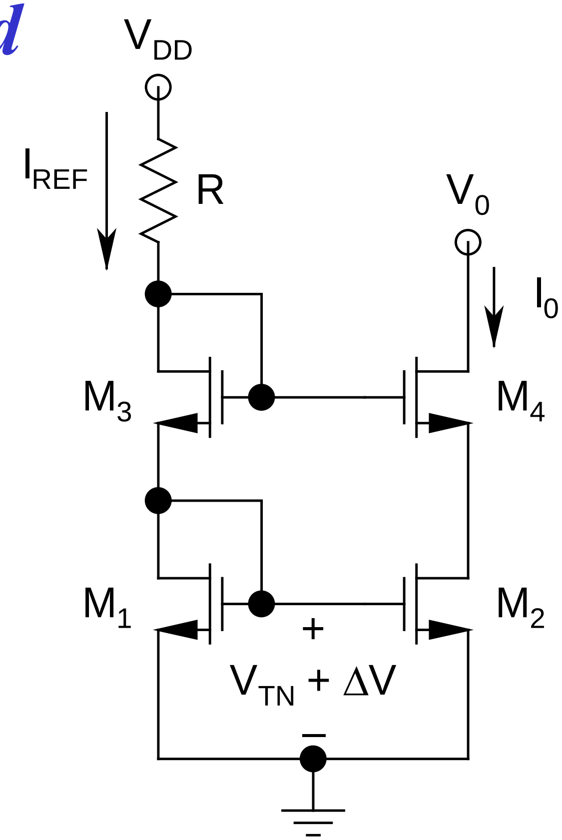
- ***NMOS Cascode***:
  - ***All Ms perfectly matched***
  - ***All bodies connected to ground***
    - ***M_1-M_2 does not have body effect***, ***but M_3-M_4 does***!
    - ***Makes hand analysis quite tedious***

      $\Rightarrow$ ***Neglect body effect***
  - ***All Ms operate with same V_{GS}***
  - Define $\Delta V = V_{GS} - V_{TN} = V_{GT}$
    - ΔV = ***Gate Overdrive***



- ***The reference current***:

$$I_{REF} = \frac{V_{DD} - 2V_{GS}}{R} = \frac{k_N}{2} V_{GT}^2 \quad (\textbf{\textit{neglecting}}\ \boldsymbol{\lambda})$$

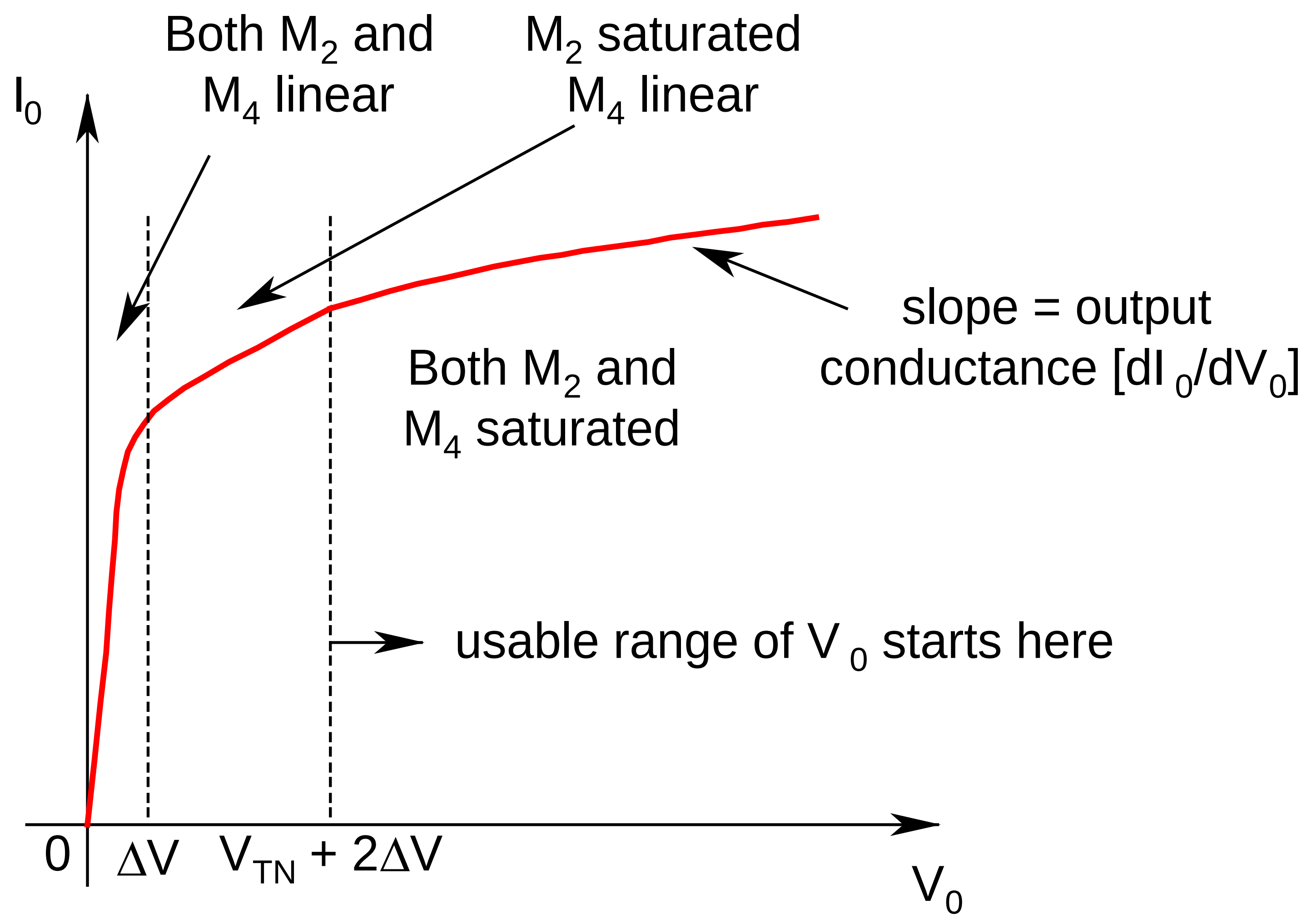
- ***V_{GS} and I_{REF} can be found*** $\Rightarrow I_0 = I_{REF}$
- $V_{G1} = V_{G2} = V_{GS} = V_{TN} + \Delta V$
- $V_{G3} = V_{G4} = 2V_{GS} = 2(V_{TN} + \Delta V)$
- $V_{S4} = V_{D2} = V_{TN} + \Delta V$

$\Rightarrow V_{GS2} = V_{DS2}$

$\Rightarrow$ ***M_2 can never enter linear region***

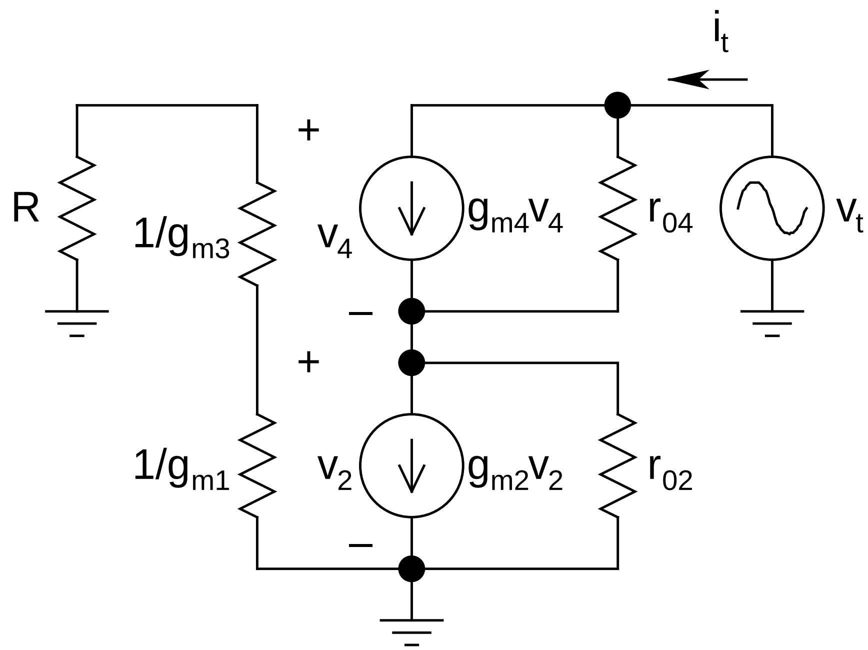
$\Rightarrow V_{0,min} = V_{DS2} + V_{DS4} = V_{TN} + 2\Delta V$

- ***This can be quite significant***, ***since V_{TN} is added to ΔV***
  - ***Assuming $\Delta V \sim 0.1$ V and $V_{TN} \sim 0.7$ V, $V_{0,min} \sim 0.8$ V, which is very large***
  - ***This is one of the drawbacks of this simple cascode circuit*** (***modified cascode doesn't have this problem***)
- ***If V_0 drops below (V_{TN} + 2ΔV), first M_4 enters linear region, and circuit performance starts to get affected***
- ***For further drop in V_0, M_2 also enters linear region, and the current mirror collapses***!



I_0
Both M_2 and M_4 linear
M_2 saturated M_4 linear
slope = output conductance [dI_0/dV_0]
Both M_2 and M_4 saturated
usable range of V_0 starts here
0
ΔV
$V_{TN} + 2\Delta V$
V_0

➢ *Calculation of R_0*:



Exact Equivalent

- *M_1 and M_3 diode-connected* $\Rightarrow 1/g_{m1}$ and $1/g_{m3}$

- ***The left part of the circuit has no source***

  $\Rightarrow v_2 = 0 \Rightarrow g_{m2}v_2 = 0$

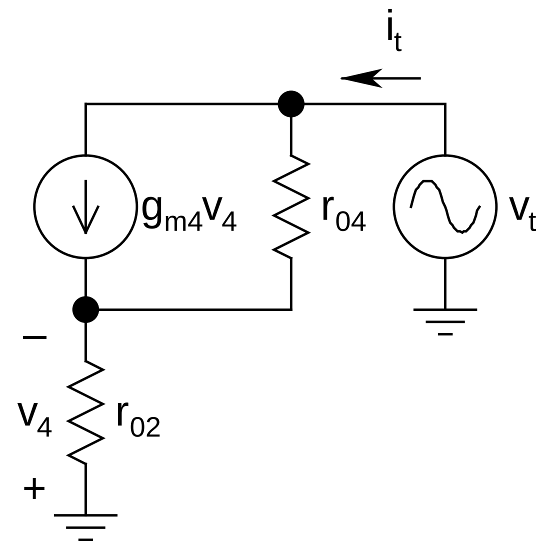
  $\Rightarrow$ ***Leads to the simplified equivalent*** (now should look very familiar!)

- ***By inspection***:

  $R_0 \approx r_{o4}(1 + g_{m4}r_{02})$

  $\approx g_{m4}r_{02}r_{04}$

- ***Can be huge***!



Simplified Equivalent

- ***Double Cascode***:
  - ***Can be implemented in both BJT & MOS***
  - ***In npn Double Cascode***, ***another pair Q_5-Q_6 stacked upon Q_3-Q_4***
    - ***Find $V_{0,min}$ and R_0***
  - ***In NMOS Double Cascode***, ***another pair M_5-M_6 stacked upon M_3-M_4***
    - ***Find $V_{0,min}$***
    - $R_0 \approx g_{m6} r_{06} R_0$ ($R_0 \approx g_{m4} r_{02} r_{04}$)
  - ***Hence, show that double cascode in BJT offers absolutely no advantage in terms of R_0***

- ***Low Value Current Source***:
  - ***Current thrust***: ***Low-power circuits***

    $\Rightarrow$ ***Increase in battery life***
  - ***If bias current can be reduced from mA to μA***, ***for the same power supply voltage***, ***power drawn reduces by three orders of magnitude***!
  - ***Normal CMs can also produce bias current in μA range***, however, ***the required resistance will be huge*** $\Rightarrow$ ***uneconomical for ICs***
  - ***Most common***: ***Widlar Current Source***
    - ***After its inventor Bob Widlar*** (***father of op-amp***)