Department of Electrical Engineering
Indian Institute of Technology, Kanpur

EE 210 **Assignment #9** **Assigned: 10/3/21**

1. Show that for a CS(D) stage, the expressions for the voltage gain A_v and the output resistance R_0 are given by $A_v = -g_mR_D/[1 + (g_m + g_{mb})R_S + (R_S + R_D)/r_0]$, and $R_0 = R_S + r_0[1 + (g_m + g_{mb})R_S]$ respectively. Note that the expression for the output resistance is identical to that of a CG stage biased by a non-ideal current source, having a source resistance R_S. Also, if $R_S \to \infty$ (i.e., the current source tends to become ideal), then $R_0 \to \infty$, as expected.

2. In a CB circuit, assume $I_C = 260\ \mu A$, $\beta = 100$, and $R_C = 10\ k\Omega$. Determine the input resistance, voltage gain, and output resistance. Neglect r_0. Now, assume that the transistor has a base resistance r_b of 101 Ω. How will it affect the input resistance and voltage gain?

3. Show that if a CB circuit is excited by an ideal current source, then the output resistance R_0', looking into the collector of the transistor, is given by $R_0' = \beta r_0$.

4. Show that for a CG stage, if the output resistance r_0 cannot be neglected, but the body effect can be neglected, then the input resistance (R_i) is given by $(r_0 + R_D)/(1 + g_mr_0)$, where R_D is the drain (i.e., load) resistance, and g_m is the transconductance of the MOSFET. Hence, show that the expression for the ac small-signal midband voltage gain (A_v) can be given by $(1 + g_mr_0)R_D/(r_0 + R_D)$. Note that in the limit of very large r_0, R_i and A_v simplify to $1/g_m$ and g_mR_D respectively, as expected.

5. The transistor (Q) used in the circuit shown in Fig.1 has $\beta = 200$. Assume the capacitors C_1-C_3 to have very large values, so that they can be treated as short circuits in midband. Neglect r_0 of the transistor.
   a) Choose R_B to give $I_C = 1$ mA, and choose R_C to give maximum undistorted peak-to-peak output voltage swing.
   b) Compute the ac small-signal midband transresistance (v_0/i_s) of the circuit.

6. The BJT (Q) in the circuit shown in Fig.2 has $\beta = 100$. Assume the capacitors C_1 and C_2 to have very large values, so that they can be treated as short circuits in midband. Neglect r_0 of the transistor.
   a) Determine the dc collector current and the collector-to-emitter voltage.
   b) Calculate the input resistance R_i, the output resistance R_0, and the voltage gain v_0/v_i.

7. In the circuit shown in Fig.3, called a ***boot-strapped follower***, assume the capacitors C_1 and C_2 to have very large values, so that they can be treated as short circuits in midband. Neglect r_0 of the transistor.
   a) Calculate the dc collector current, assuming $\beta = 100$.
   b) Calculate the input resistance R_i and the voltage gain v_0/v_s.

c) Repeat b) for the case when capacitor C_2 is open-circuited. Compare the results with those obtained in b) to find the advantages of bootstrapping.

8. The amplifier shown in Fig.4 consists of two identical CE amplifiers connected in cascade. Assume the capacitors C_1-C_5 to have very large values, so that they can be treated as short circuits in midband. Neglect r_0 of the transistors.
   a) For V_{CC} = 15 V, $R_1 = R_3$ = 100 kΩ, $R_2 = R_4$ = 47 kΩ, $R_{E1} = R_{E2}$ = 3.9 kΩ, $R_{C1} = R_{C2}$ = 6.8 kΩ, and β = 100, determine the dc collector current and the collector-to-emitter voltage of each transistor. Neglect base currents for dc analysis.
   b) Now, perform an ac small-signal midband analysis of the stage, and determine the following:
      i) R_{i1} and v_{b1}/v_s for R_S = 5 kΩ.
      ii) R_{i2} and v_{b2}/v_{b1}.
      iii) v_0/v_{b2} for R_L = 2 kΩ.
      iv) the overall voltage gain v_0/v_s.

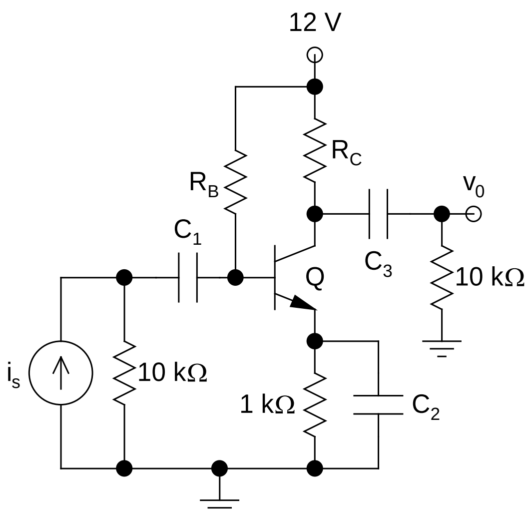

Fig.1

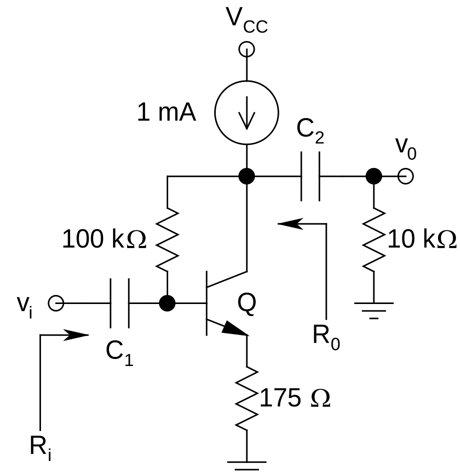

Fig.2

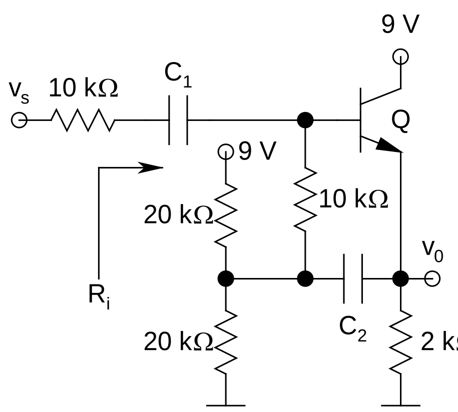

Fig.3

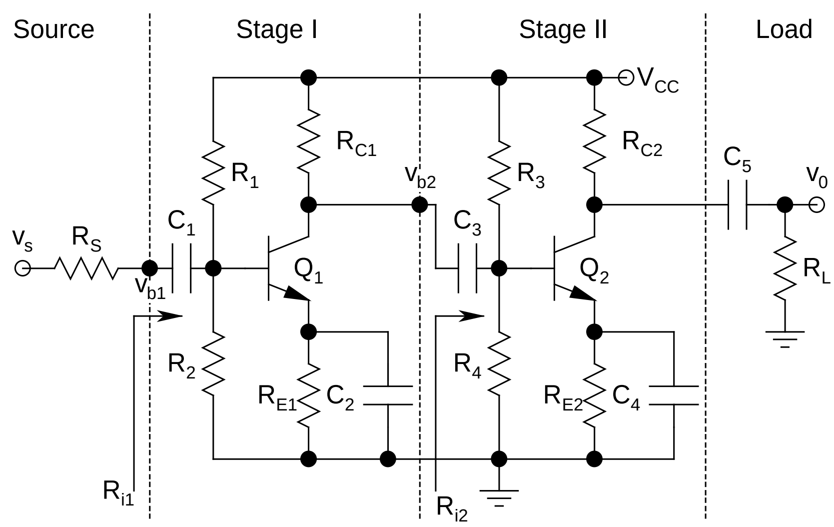

Fig.4