ESc201A Home Assignment 8 Oct. 21, 2019.

Solutions of the HA#7 will be on Brihaspati on 28/10/19.

1. Obtain the truth table for the following function: (x.y+z)(y+x.z) and write it as sum of products (SOP) and product of sums (POS).
2. Use Boolean identities to prove that $(w.x.z+\overline{w}.x+\overline{x}.z+\overline{y}).(y+w.x+x.z)=x.(w+y).(\overline{w}+\overline{y})+z.(x+y)$
3. Minimize the following functions using K-map:

(a) $F(A,B,C,D)= A.B.\overline{C}.\overline{D}+\overline{A}.B.\overline{C}.\overline{D}+A.\overline{B}.\overline{C}.D+\overline{A}.B.C.D+A.B.C.\overline{D}+\overline{A}.B.C.\overline{D}$

(b) $F(X,Y,Z)=\sum m(0,1,2,3,4,5,6)$

(c) $F(X,Y,Z)=\prod M(0,1,2,4)$

(d) $F(A,B,C,D,E)=\sum(2,6,8,10,12,14,18,22,24,26,28,30)$.

4. Express the function $F(A, B, C, D) = \sum(2, 3, 4, 6, 12, 14) + \sum_{Don't\ Care}(7, 9, 10, 11, 15)$ in the minimized Sum of Products form.
5. Express the function $F(A, B, C, D) = \sum(1, 3, 4, 6, 9, 11, 12, 14) + \sum_{Don't\ Care}(5, 7)$ in the minimized Products of Sum form.
6. Find a minimal expression for a Boolean function F(A,B,C,D) where F is true when E is true, except when E takes X states.

A	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
B	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
C	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
D	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
E	1	0	1	1	0	0	0	0	1	X	1	X	0	X	0	X

7. Design a combinational circuit with 3 inputs and 1 output

(a) The output is 1 when the binary value of the inputs is less than 3. The output is 0 otherwise

(b) The output is 1 when the binary value of inputs is an odd number.

8. Carry out the following conversions:

(a) $(111011.10101)_2 = (?)_{10}$

(b) $(361)_{10} = (?)_2$

(c) $(0.90625)_{10} = (?)_2$

(d) $(75.4375)_{10} = (?)_2$

(e) $(B95C.A5)_{16} = (?)_{10}$

(f) $(1101101101001010 1.1110000111)_2 = (?)_{16}$

(g) $(1959)_{10} = (?)BCD$

(h) $(1100001100010)BCD = (?)_{10}$

9. Show that any Boolean expression can be implemented using either NAND or NOR gates only.
10. Perform the following arithmetic operations using 2's complement method: (Use 8-bit representation of number).
    (a) 50 – 21, (b) -50 + 21, (c) -50 - 21
11. a) Show that a 1-bit Half adder can be implemented with an Exclusive-OR (XOR) gate and an AND gate.
    b) Show that a 1-bit Full adder can be implemented with two Half adders and an OR gate.