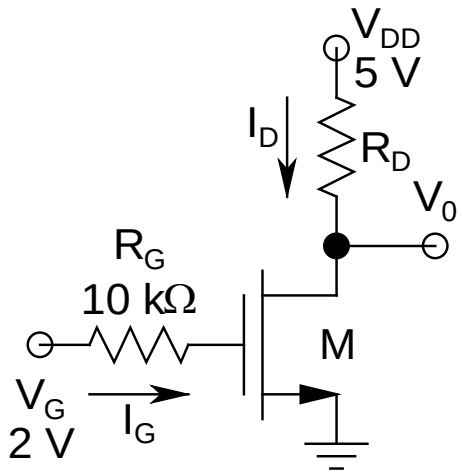
DC Bias Point Calculation

- ***To find R_D for BB***
  - $V_{TN0} = 1$ V, $k'_N = 40\ \mu A/V^2$, $W/L = 10$
- ***Body terminal not shown***
  - ***Implies that it is connected to the most negative potential available in the circuit (ground in this case)***

$\Rightarrow V_{SB} = 0 \Rightarrow V_{TN} = V_{TN0}$

- $I_G = 0 \Rightarrow V_{GS} = V_G = 2$ V



- $V_{GT} = V_{GS} - V_{TN} = 1$ V
- ***Assuming saturation mode of operation and neglecting CLM***:

  $I_D = (k_N/2) V_{GT}^2 = 200$ μA
- ***For BB***, $V_{DS} = V_{DD}/2 = 2.5$ V (***2-element output branch***):

  $R_D = (V_{DD} - V_{DS})/I_D = 12.5$ kΩ
- $V_{DS} > V_{GT} \Rightarrow$ ***Assumption of saturation mode of operation validated***
- $P_D = V_{DS} \times I_D = 0.5$ mW

Small-Signal Model

- The ***electrical equivalent*** of the MOSFET at the ***DC bias point***
- ***Must be biased in saturation***
  - ***Resembles a constant current source***
- ***DC analysis must precede***, since ***need the information regarding the Q-point*** (I_D, V_{DS})
- ***This model for NMOS and PMOS is the same*** (***incremental model***)

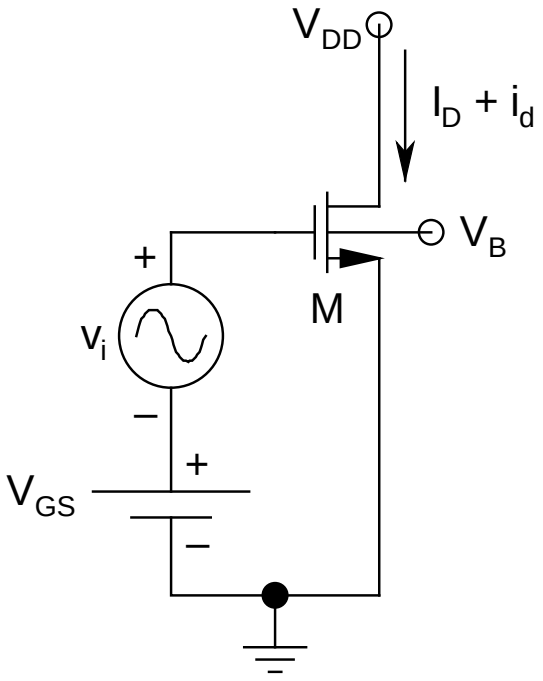
Validity of the Small-Signal Model

- The ***instantaneous current*** (***assuming $\lambda V_{DS} < 0.1$***):

$$I_d = \frac{k_N}{2}\left(V_{GT} + v_i\right)^2$$

$$= I_D + \frac{k_N}{2}\left[2V_{GT}v_i + v_i^2\right]$$

$$\Rightarrow \; i_d = k_N V_{GT} v_i \left[1 + \frac{v_i}{2V_{GT}}\right]$$



- Thus, for ***linear relationship*** between i_d and v_i, ***v_i must be << V_{GT}***
- Note that ***V_{GT} (minimum) = $3V_T$***
- Hence, ***v_i should be at least ten times less than $3V_T$***
- Recall in ***BJT***, for ***linear relationship*** between i_c and v_i, ***v_i has to be << V_T***
  - ***Three times less than that for MOSFET***
  - ***MOSFETs are inherently more linear device than BJTs*** (***compare quadratic with exponential***)