BIASING

- To find the ***DC operating point*** (***bias point***, ***Q-point***)
- Has to ***precede ac analysis***, since ***small-signal parameters depend on the bias point***
- For ***diodes***: (I_D, V_D)
- For ***BJTs***: (I_C, V_{CE})
- For ***MOSFETs***: (I_D, V_{DS})
- Also, $P_D = V_D \times I_D$ (***Diodes***), $V_{CE} \times I_C$ (***BJTs***), and $V_{DS} \times I_D$ (***MOSFETs***)

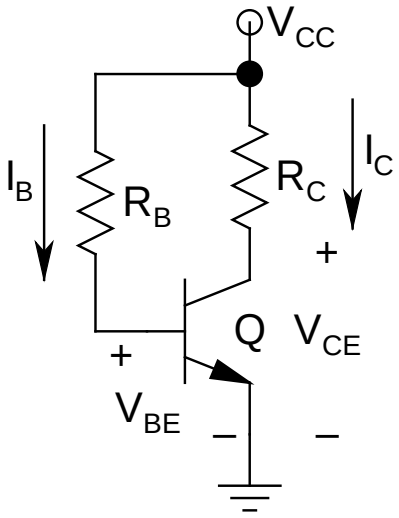
- ***DC power dissipated in a circuit*** = (***Supply Voltage***) × (***Supply Current***)
- Circuits may be ***biased*** by ***single supply*** (***positive/negative and ground***) or ***dual supply*** (***positive and negative***)
- Devices should be ***properly biased*** and ***ideally*** should be under the ***best biasing*** (BB)
- Also, need ***voltage references*** to provide ***fixed DC voltages*** at some ***circuit nodes***

- ***Two types***:
  - ***Discrete Stage Biasing***:
    - Uses ***power supplies*** and ***resistors*** along with the ***active devices***
    - Used for ***discrete circuits*** assembled in ***breadboards***
    - Also known as ***passive biasing***
  - ***IC (Integrated Circuit) Stage Biasing***:
    - ***Avoids resistors*** as much as possible and ***uses transistors*** as ***biasing elements***
    - Used for ***IC stages***
    - Also known as ***active biasing***

Discrete Stage Biasing: BJT

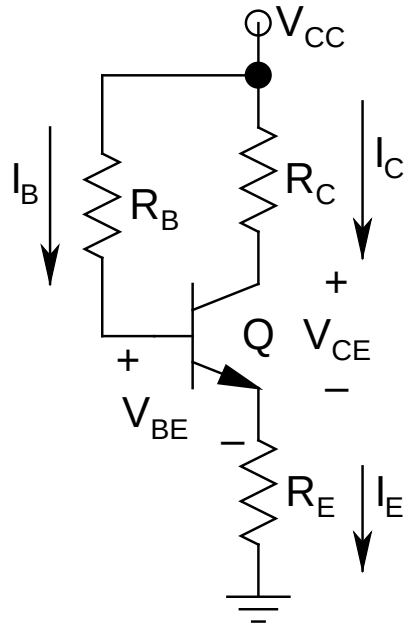
- Will be using ***quick estimate*** (V_{BE} = 0.7 V)
- ***FA mode of operation*** with $V_{CE} \geq 0.2$ V
- ***Error of ±5-10% perfectly acceptable***
- ***Common Schemes***:
  - ***Fixed Resistor Bias***
  - ***Emitter Feedback Bias***
  - ***Collector Feedback Bias***
  - ***Voltage Divider (or 4-Resistor) Bias***

- ***Fixed Resistor Bias***:
  - $I_B = (V_{CC} - V_{BE})/R_B$
  - $I_C = \beta I_B$
  - $I_E = (\beta + 1)I_B \approx I_C$
  - $V_{CE} = V_{CC} - I_C R_C$
    - For BB, $V_{CE} = V_{CC}/2$
  - P_D (***circuit***) $= V_{CC} \times I_E$
  - ***Note***: ***Need β to find the operating point***
  - The ***simplest biasing circuit***, but has ***severe β dependence***



- ***Emitter Feedback Bias***:
  - ***While writing KVL, never take CE or BC loops, since V_{CE} and V_{BC} are not known***
  - ***Consider only BE loops with $V_{BE} = 0.7$ V***
  - $V_{CC} = I_B R_B + V_{BE} + I_E R_E$

$$\Rightarrow I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1) R_E}$$

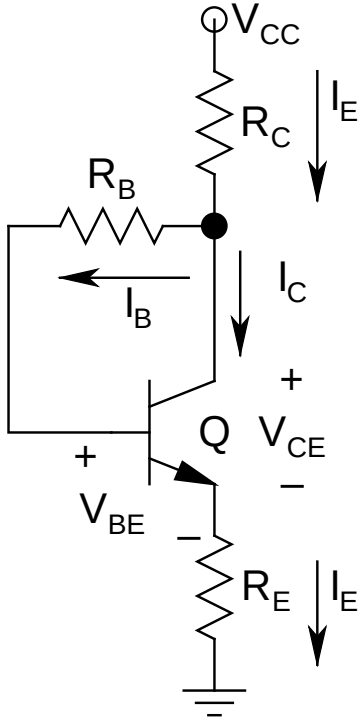


- $I_C = \beta I_B$
- $V_{CE} = V_{CC} - I_C R_C - I_E R_E \approx V_{CC} - I_C(R_C + R_E)$
- $P_D = V_{CC} \times I_E$
- This is a ***3-element output branch***, with ***$V_{CE} = V_{CC}/3$ for BB***
- ***Rest $2V_{CC}/3$ drops across R_C and R_E, with the ratio typically chosen to be 2:1*** (reason later!)
- Circuit is ***very robust*** since R_E provides ***negative feedback***
- Also, has ***better β insensitivity***

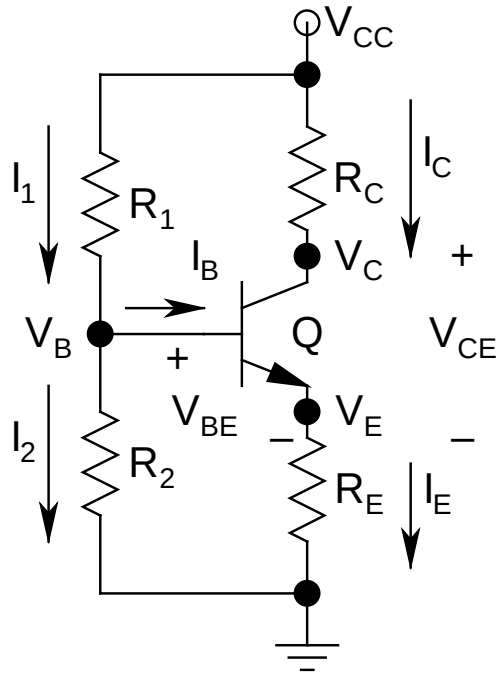
- ***Collector Feedback Bias***:
  - $V_{CC} = I_E(R_C + R_E) + I_B R_B + V_{BE}$

    $$\Rightarrow I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)(R_C + R_E)}$$
  - $I_C = \beta I_B$
  - $V_{CE} = V_{CC} - I_E(R_C + R_E)$
  - $P_D = V_{CC} \times I_E$
  - This circuit also provides

    better β insensitivity



- ***Voltage Divider (or 4-Resistor) Bias***:
  - ***The best***: ***Extremely robust and versatile***
  - If properly designed, ***almost β independent***
  - If $I_1 \geq 10 I_B$, $I_1 \approx I_2$



$$\Rightarrow V_B \simeq \frac{R_2}{R_1 + R_2} V_{CC}$$

$$\Rightarrow V_E = V_B - V_{BE} \text{ and } I_C \simeq I_E = V_E / R_E$$

- ***Example***: Let $V_{CC} = 5$ V, $R_1 = 40$ kΩ, $R_2 = 10$ kΩ, $R_C = 2$ kΩ, and $R_E = 300$ Ω
  - ***Quick estimate***: Assume $\beta \geq 100$

    $\Rightarrow V_B = 1$V, $V_E = 0.3$ V, $I_C \approx I_E = 1$ mA, $V_{CE} = 2.7$ V, and $P_D = 5.5$ mW

    $\Rightarrow$ Done! Piece of cake, isn't it?
  - $I_1 = 100$ μA and $I_B \leq 10$ μA (for $\beta \geq 100$): Assumption of $I_1 \geq 10 I_B$ validated
  - Actually, ***as I_1 and β go down***, this ***analysis becomes more and more inaccurate***!

- ***Exact Analysis***:
  - ***Sufficiently more complicated***
  - ***Open the base lead*** and

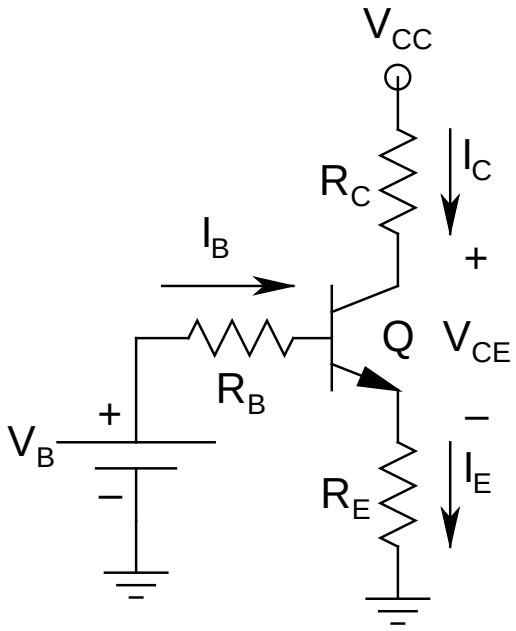
    Thevenize the left branch

$$\Rightarrow V_B = \frac{R_2}{R_1 + R_2} V_{CC} = 1\ \text{V}$$

$$R_B = R_1 \| R_2 = 8\ \text{k}\Omega$$

  - Also, $V_B = I_B R_B + V_{BE} + I_E R_E$

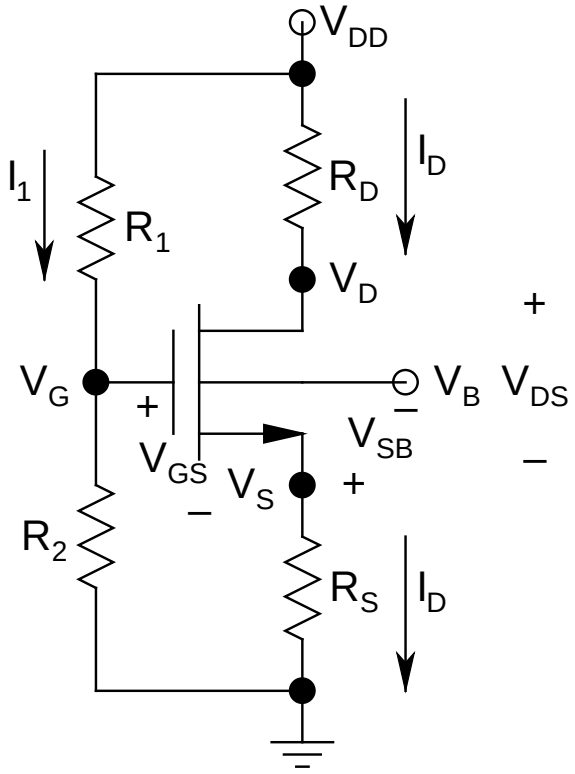
$$\Rightarrow I_B = \frac{V_B - V_{BE}}{R_B + (\beta + 1) R_E}$$



- Gives:
  - I_B = 7.83 μA, I_C = 0.78 mA, and V_{CE} = 3.2 V for β = 100 (***quite off from quick estimate***!)
  - I_B = 3.6 μA, I_C = 0.9 mA, and V_{CE} = 2.93 V for β = 250 (***within ±10% error band***)
- Thus, ***as β↑, accuracy of quick estimate↑***
- Also, ***as R_B↓, accuracy↑***
- ***R_B should not be too small***, ***since P_D↑↑***
- Thus, there are ***various design constraints***

Discrete Stage Biasing: MOSFET

- ***Almost universally biased using 4-Resistor Bias***
- ***Significantly more complicated than BJT biasing, since there is no quick estimate***
- ***Also, body effect and CLM complicate matters***



- ***No I_G $\Rightarrow$ R_1-R_2 combination provides a perfect voltage division***

$$\Rightarrow V_G = \frac{R_2}{R_1 + R_2} V_{DD}$$

- $V_S = I_D R_S$ and $V_D = V_{DD} - I_D R_D$

$$\Rightarrow I_D = \frac{k_N}{2}\left(V_G - I_D R_S - V_{TN}\right)^2 \times \left(1 + \lambda\left[V_{DD} - I_D\left(R_S + R_D\right)\right]\right)$$

- Also:

$$V_{TN} = V_{TN0} + \gamma\left(\sqrt{2\phi_F + I_D R_S - V_B} - \sqrt{2\phi_F}\right)$$

- ***Extremely intimidating***!
- ***I_D equation becomes cubic***!
- ***Thus, bias calculation including all higher order effects is pretty tedious, and almost impossible for hand analysis***
- ***Need to make approximations***!

- Assume $\lambda V_{DS} < 0.1$:

$$\Rightarrow I_D = \frac{k_N}{2}\left(V_G - I_D R_S - V_{TN}\right)^2$$

- ***Even then it's quite complicated, since V_{TN} has a square root dependence on I_D***
- ***Tie B and S together*** $\Rightarrow V_{SB} = 0$ and $V_{TN} = V_{TN0}$
  - ***Note that it can't be done always***!

$$\Rightarrow I_D = \frac{k_N}{2}\left(V_G - I_D R_S - V_{TN0}\right)^2$$

- ***Even now, it's a quadratic equation in I_D***
- ***However, much easier to solve than earlier cases***
- ***No further simplification possible***!
- ***Solving, we will get 2 values of I_D: one will be the correct one***, while ***the other one will be unphysical***
- ***2 values of I_D will give 2 different values of V_{GS}: one > V_{TN0}*** and the ***other < V_{TN0}***

- ***Obviously, I_D for $V_{GS} < V_{TN0}$ is completely meaningless, since the device is off under that condition***
- Compute V_{DS} [= $V_{DD} - I_D(R_S + R_D)$]
  - ***Should be > V_{GT} (saturation mode)***
  - ***For BB, $V_{DS} = V_{DD}/3$***
- $P_D = V_{DD} \times (I_D + I_1)$ [$I_1 = V_{DD}/(R_1 + R_2)$]
- ***Here, no constraints on R_1 and R_2, and they can be made as large as physically possible to reduce I_1, and thus P_D***

IC Stage Biasing

- ***Avoids resistors as much as possible***
  - ***Resistors take up very large area on IC chips, which is at a premium***
- ***Uses transistors as biasing elements***
  - ***Much more compact than resistors***, and ***area consumption is almost negligible as compared to resistors***
- Also known as ***active biasing***

- ***Parameters***:
  - ***Output Current I_0***
    - ***As per specification***
  - ***Output Resistance R_0***
    - $R_0 = \Delta V_0/\Delta I_0 = dV_0/dI_0 = v_0/i_0$ (***ac***)
    - ***As large as possible*** - ***ideally infinite***
  - ***Minimum Allowed Output Voltage $V_{0,min}$***
    - ***As small as possible*** - ***ideally zero***
    - ***Dictated by***:
      - ***For BJT***: $V_{CE}(\text{min}) = V_{CE}(\text{SS}) = 0.2$ V
      - ***For MOSFET***: $V_{DS}(\text{min}) = V_{GT}(\text{min}) = 80$ mV

- ***I_0 should be independent of power supply and temperature***
  - ***Temperature and Supply Independent Biasing***
- ***Should use minimum number of circuit elements***
  - ***Economization of space***
- ***Should not affect frequency response***

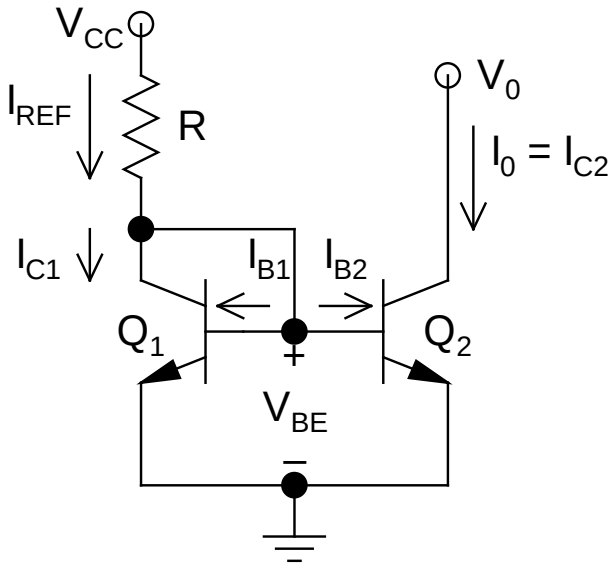
- It is ***almost impossible to satisfy all these constraints simultaneously***
  - ***Look for optimization***

Current Sources/Sinks

- Also known as ***Current Mirrors*** (CM)
- Can be used for ***biasing*** as well as ***load elements*** (known as ***active load***)
- Designed based on ***required specifications***
- ***Two sources of errors***:
  - ***Systematic***: ***Even when devices are matched***
  - ***Random***: ***When there is a random mismatch between devices***

- ***Simple npn CM***:
  - Q_1 has its ***B and C shorted***
    - ***Can never saturate*** ($V_{BC} = 0$)
    - Known as ***diode-connected BJT***
  - Q_1 and Q_2 have ***same V_{BE}***
  - I_{REF} = ***Reference Current***

    $= (V_{CC} - V_{BE})/R$
  - I_0 = ***Output Current*** = I_{C2}
  - V_0 = ***Output Voltage***
    - ***Variable***, ***depends on the load connected to it***



- ***General Analysis***:

$$I_{REF} = I_{C1} + I_{B1} + I_{B2} = I_{C1}\left(1 + \frac{1}{\beta_1}\right) + \frac{I_{C2}}{\beta_2}$$

- Now:

$$V_{BE} = V_T \ln\left(\frac{I_{C2}}{I_{S2}}\right) = V_T \ln\left(\frac{I_{C1}}{I_{S1}}\right)$$

$$\Rightarrow I_{C2} = KI_{C1} \quad \left(K = I_{S2}/I_{S1}\right)$$

- Thus:

$$I_{REF} = I_{C2}\left[\frac{1}{\beta_2} + \frac{1}{K}\left(1 + \frac{1}{\beta_1}\right)\right]$$

- ***Finally***:

$$I_0 = I_{C2} = \frac{I_{REF}}{\frac{1}{\beta_2} + \frac{1}{K}\left(1 + \frac{1}{\beta_1}\right)}$$

- This is the ***exact expression*** of I_0, ***without making any assumptions/approximations whatsoever***
- The ***only assumption*** so far is that we have ***neglected Early effect***, which we would include soon

- Now, we ***make approximations/assumptions***:

1. $\beta_1 = \beta_2 = \beta$:

$$\Rightarrow I_0 = \frac{KI_{REF}}{1 + \frac{1+K}{\beta}}$$

2. $I_{S1} = I_{S2} = I_S$ $(K = 1)$:

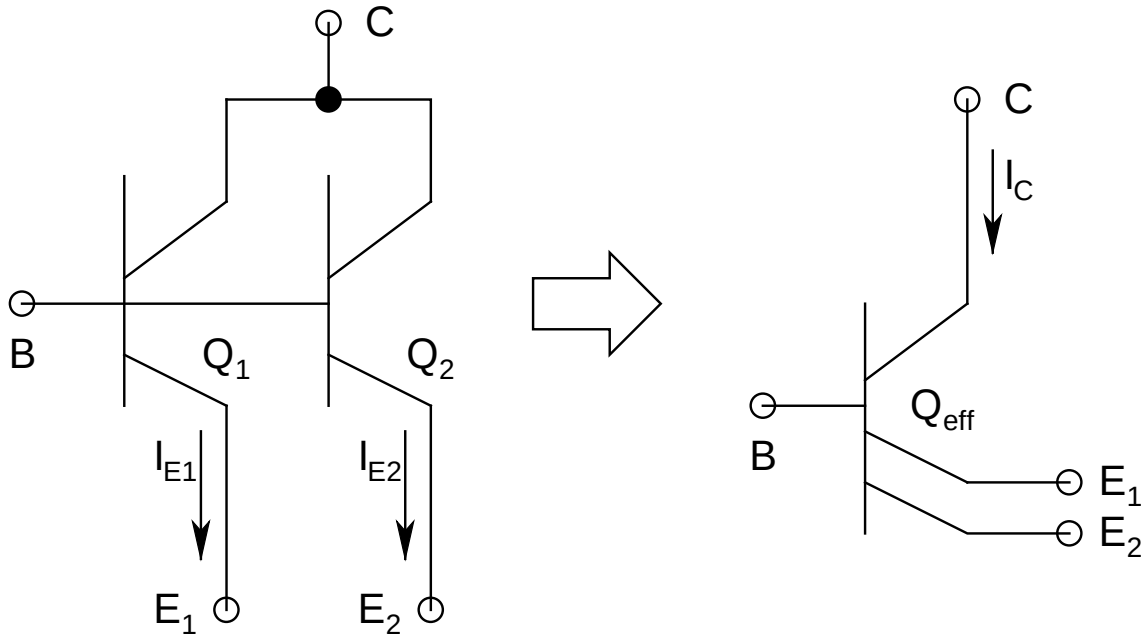
$$\Rightarrow I_0 = \frac{I_{REF}}{1 + 2/\beta}$$

3. And finally $\beta >> 2$:

$\Rightarrow I_0 = I_{REF} \Rightarrow$ ***Current Mirror***!

- For this to happen, Q_1 and Q_2 must have ***same β*** (***>> 2***), and ***same I_S***
- If two BJTs have ***same β, I_S, and V_A***, they are known as a ***matched pair***
- If $I_{S1} \neq I_{S2}$ and/or $\beta_1 \neq \beta_2$, then $I_0 \neq I_{REF}$
  - Leads to ***random error*** (***process induced***)
- If $\beta_1 = \beta_2$, but $I_{S1} \neq I_{S2}$, then $I_0 = KI_{REF}$
  - ***K or 1/K can only be integers***
    - ***I_0 and I_{REF} become integer multiples of each other***

- ***Multi-Emitter BJT***:



➢ $I_{S1} = I_{S2} \Rightarrow I_{E1} = I_{E2} = I_E \Rightarrow I_C \approx 2I_E$

- ***This does not imply that $\alpha = 2$, since there are two emitters***

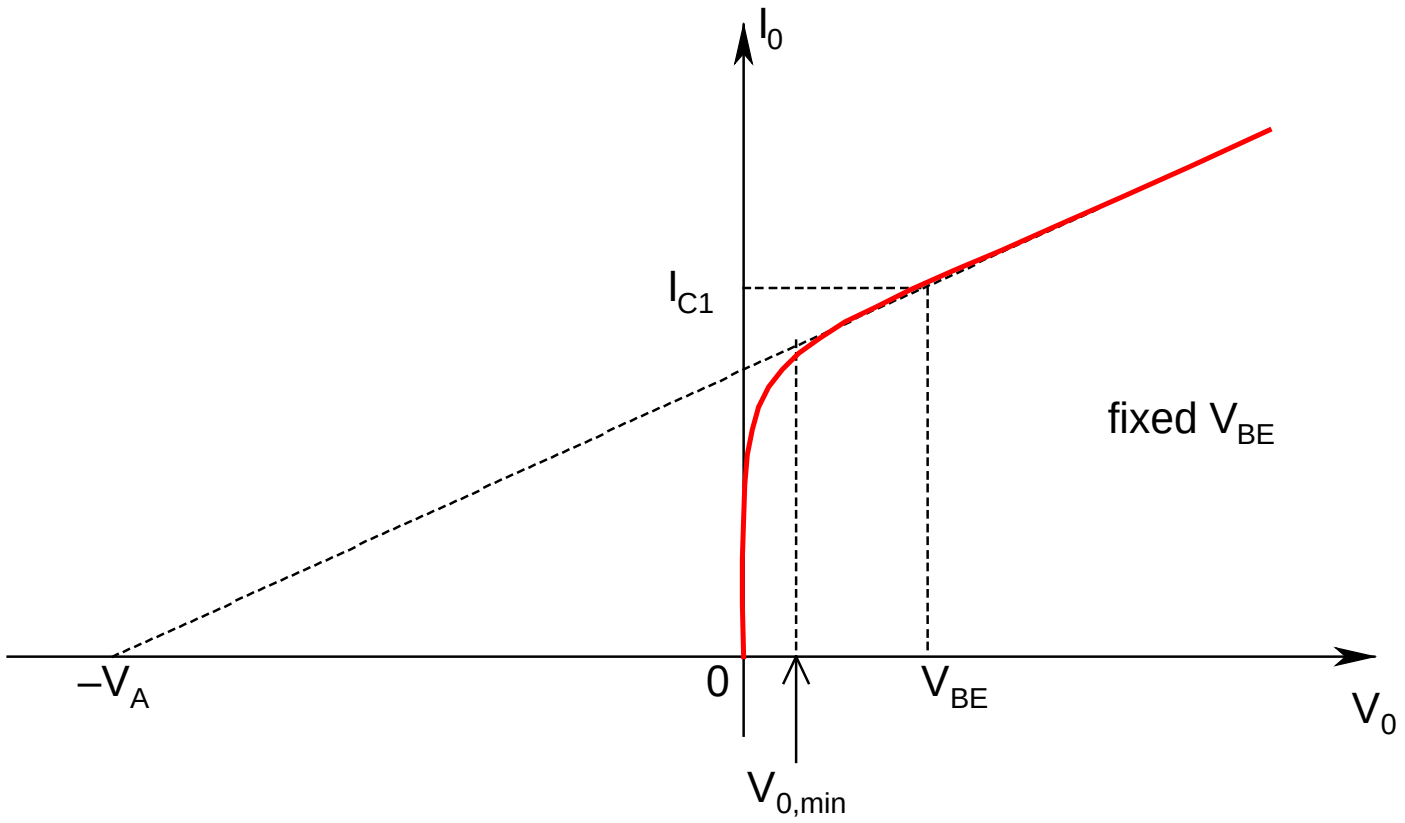
- ***Systematic Error***:
  - ***Even if Q_1 and Q_2 are perfectly matched and $\beta >> 2$, still I_0 may not equal I_{REF}!***
  - ***Recall***:

$$I_C = I_S[\exp(V_{BE}/V_T)](1 + V_{CE}/V_A)$$

  - ***Thus***:

$$\frac{I_{C2}}{I_{C1}} = \frac{I_0}{I_{C1}} = \frac{1+V_{CE2}/V_A}{1+V_{CE1}/V_A} = \frac{1+V_0/V_A}{1+V_{BE}/V_A}$$

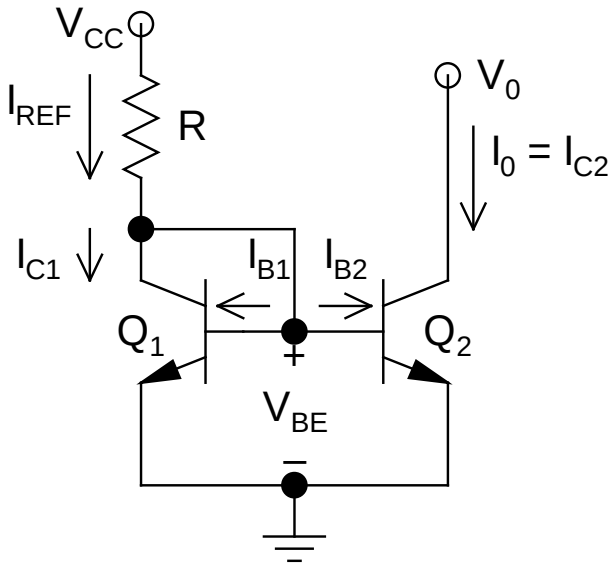
  - Therefore, ***$I_0 = I_{C1}$ only when $V_0 = V_{BE}$***



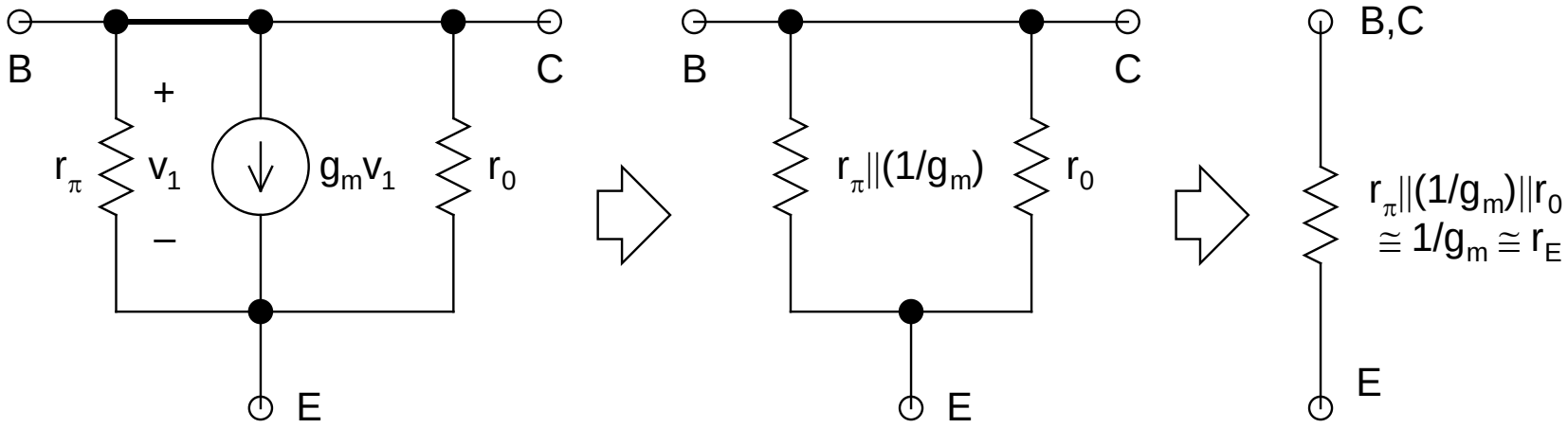
$$V_{0,min} = V_{CE2}(SS) = 0.2\ V$$

- ***Simple npn CM***:
  - Q_1 has its ***B and C shorted***
    - ***Can never saturate*** ($V_{BC} = 0$)
    - Known as ***diode-connected BJT***
  - Q_1 and Q_2 have ***same V_{BE}***
  - I_{REF} = ***Reference Current***

    $= (V_{CC} - V_{BE})/R$
  - I_0 = ***Output Current*** = I_{C2}
  - V_0 = ***Output Voltage***
    - ***Variable***, ***depends on the load connected to it***



- ***Output Resistance R_0***:
  - First, ***investigate Q_1***



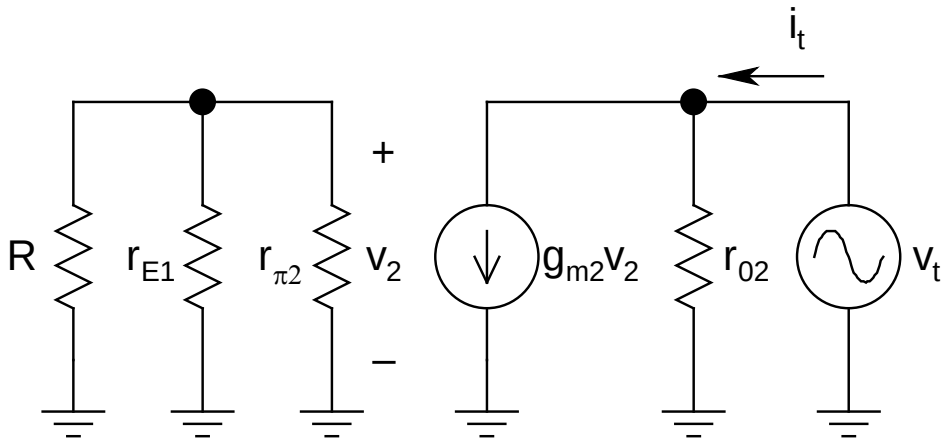
  - The ***small-signal equivalent*** consists simply of r_E, which is the same as that for a ***diode***
    - Hence the name ***diode-connected BJT***

- ***Algorithm to find R_0:***
  - ***Short all independent DC/ac voltage sources***
  - ***Open all independent DC/ac current sources***
  - ***Replace the active device by its low-frequency hybrid-π model***
  - ***Excite the output terminal by a test voltage source (ac) v_t***
  - ***Find the current (ac) i_t drawn from v_t***
  - ***Then, $R_0 = v_t / i_t$***

- ***For the complete circuit***:
  - ***Left part of the circuit has no source***

    $\Rightarrow v_2 = 0$

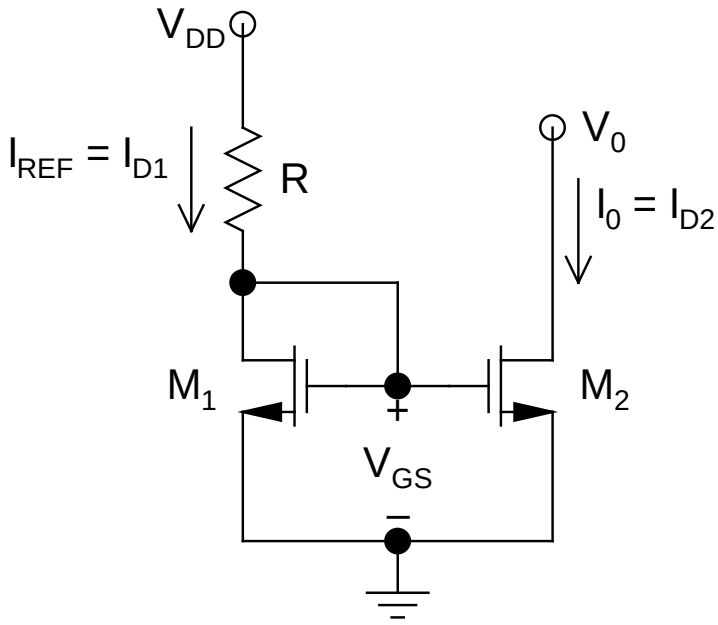
    $\Rightarrow g_{m2}v_2 = 0$



  - Thus, $R_0 = v_t/i_t = r_{02} = V_{A2}/I_0$
  - For a ***good current source***, ***R_0 should be as large as possible*** (***ideally infinite***)

    $\Rightarrow$ ***V_{A2} should be as large as possible*** and/or ***I_0 should be as small as possible***

- ***Simple NMOS CM***:
  - $V_{GS1} = V_{GS2} = V_{GS}$
  - M_1 has its ***D and G shorted*** $\Rightarrow V_{GD1} = 0$
    $\Rightarrow$ ***always in saturation***, since $V_{DS1} > V_{GT1}$
    $\Rightarrow$ Known as ***diode-connected MOSFET***



  - Even though $I_G = 0$, the analysis is slightly more cumbersome than simple BJT CM

- ***In general, for NMOS (PMOS), the B terminal is always connected to the most negative (positive) potential available in the circuit to ensure that SB and DB junctions never get forward biased***
- ***Both M_1 and M_2 have their B terminals grounded*** $\Rightarrow V_{SB1} = V_{SB2} = 0$
  - $V_{TN1} = V_{TN01}$ and $V_{TN2} = V_{TN02}$
- Thus:

$$I_{REF} = I_{D1} = \frac{k'_{N1}}{2}\left(\frac{W}{L}\right)_1 \left(V_{GS} - V_{TN01}\right)^2$$

- For a ***given V_{DD} and R***, the equation has ***2 unknowns***: I_{D1} and V_{GS}
- Need ***another equation*** for ***unique solution***, which is the ***load line equation***:

  $I_{D1} = (V_{DD} - V_{GS})/R$
- ***Simultaneous solution*** of these ***two equations*** would give a ***unique solution*** for I_{D1} and V_{GS}
  - ***Caution***: ***2 roots, out of which, one will be unphysical***
- So far, we have ***neglected CLM***, which we would include soon!

- Now:

$$V_{GS} = V_{TN01} + \sqrt{\frac{2I_{REF}}{k'_{N1}\left(W/L\right)_1}} = V_{TN02} + \sqrt{\frac{2I_0}{k'_{N2}\left(W/L\right)_2}}$$

- Thus:

$$I_0 = \frac{k'_{N2}\left(W/L\right)_2}{2}\left[\left(V_{TN01} - V_{TN02}\right) + \sqrt{\frac{2I_{REF}}{k'_{N1}\left(W/L\right)_1}}\right]^2$$

- This is the ***exact expression*** of I_0, ***without making any assumptions/approximations whatsoever***

- Now, if $V_{TN01} = V_{TN02} = V_{TN0}$, and $k'_{N1} = k'_{N2} = k'_N$:

$$I_0 = \frac{(W/L)_2}{(W/L)_1} I_{REF}$$

- ***Very similar*** to BJT CM, but with a ***big exception***:
  - ***In BJT CM, this ratio could only be an integer***
  - ***In MOS CM, no such restriction exists***: ***$(W/L)_2$ can be >, =, or < $(W/L)_1$ $\Rightarrow$ any arbitrary current ratio can be obtained***

- Finally, if $(W/L)_2 = (W/L)_1$:

  $I_0 = I_{REF} \Rightarrow$ ***Current Mirror***!

- Two MOSFETs are deemed to constitute a ***matched pair***, if they have ***same*** V_{TN0}, γ, ϕ_F, λ, and k'_N
  - Note that all of these are ***process parameters***
  - ***(W/L) is NOT a process parameter***, since it's under ***designer's control***
  - ***If (W/L)s are also same, then the pair is known as perfectly matched***

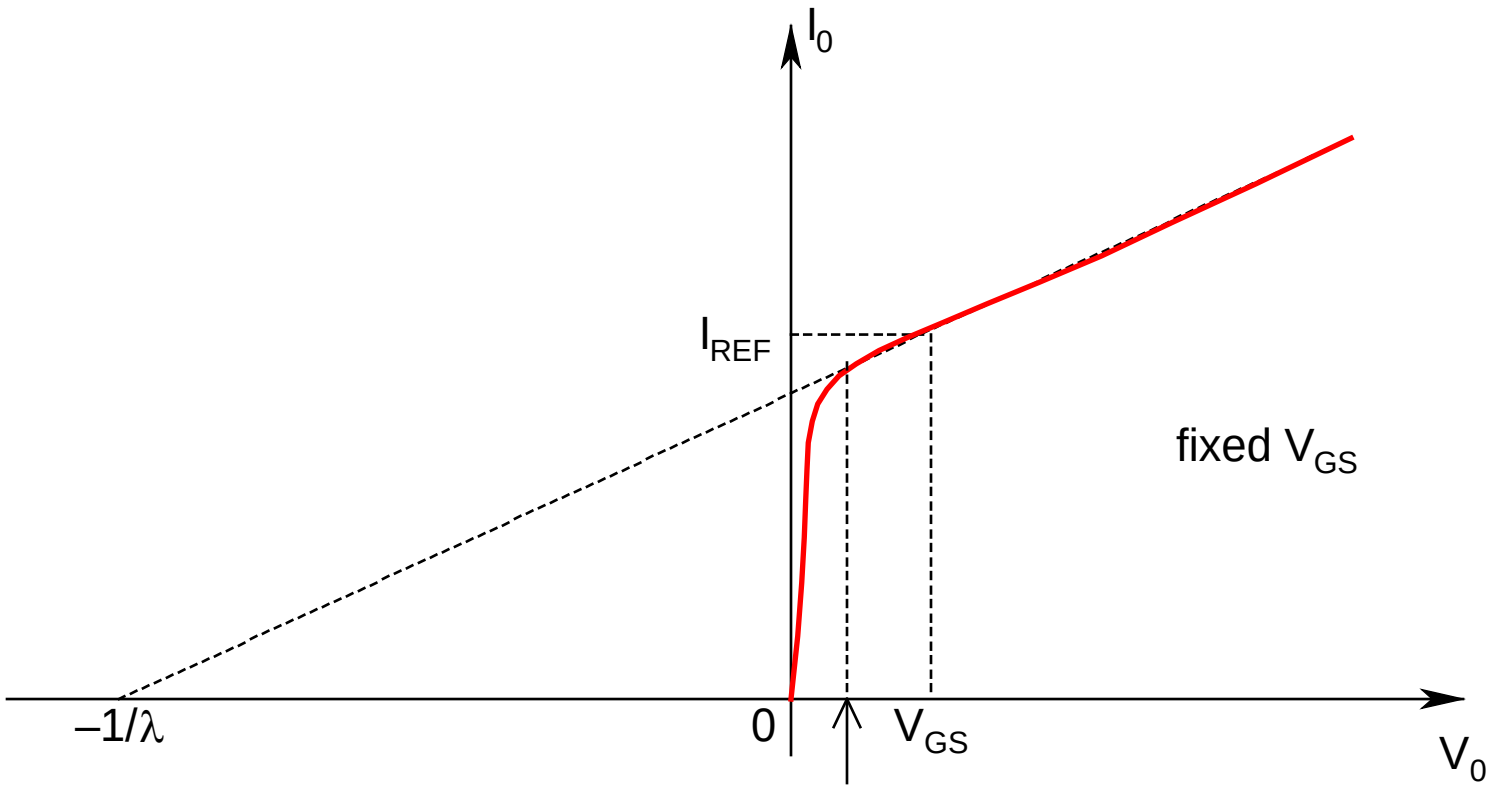
- ***Systematic Error***:
  - Even if M_1 and M_2 are ***perfectly matched***, still I_0 ***may not equal*** I_{REF}!
  - Recall:

$$I_D = \frac{k_N}{2} V_{GT}^2 \left(1 + \lambda V_{DS}\right)$$

  - Thus:

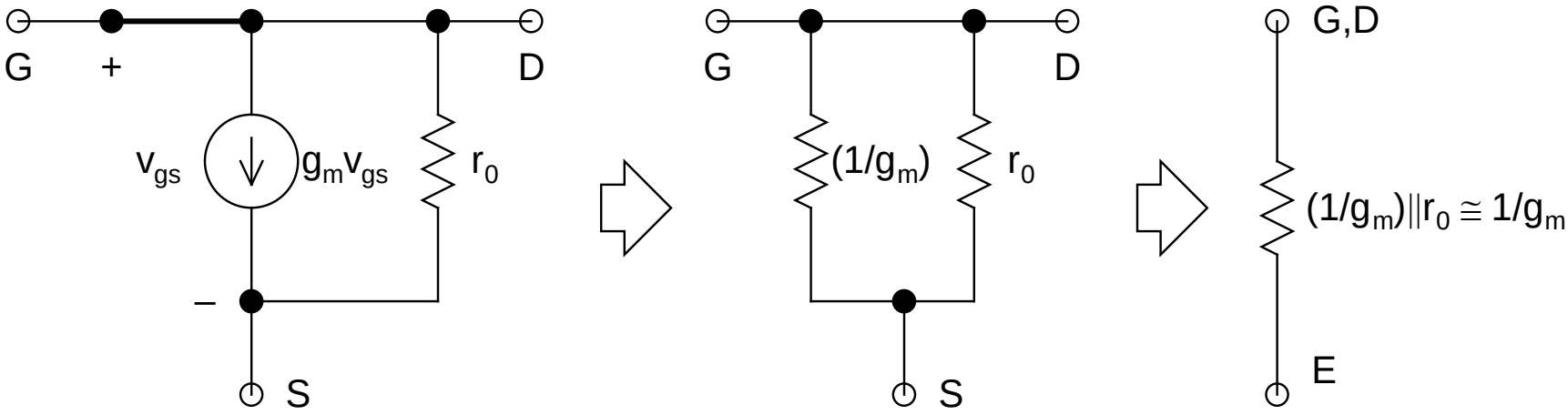
$$\frac{I_0}{I_{REF}} = \frac{1 + \lambda V_{DS2}}{1 + \lambda V_{DS1}} = \frac{1 + \lambda V_0}{1 + \lambda V_{GS}}$$

  - Therefore, ***$I_0 = I_{REF}$ only when $V_0 = V_{GS}$***



$V_{0,min} = V_{DS2}(sat)$ (lowest allowed value $\approx 3V_T$)

- ***Output Resistance R_0***:
  - First, ***investigate M_1***

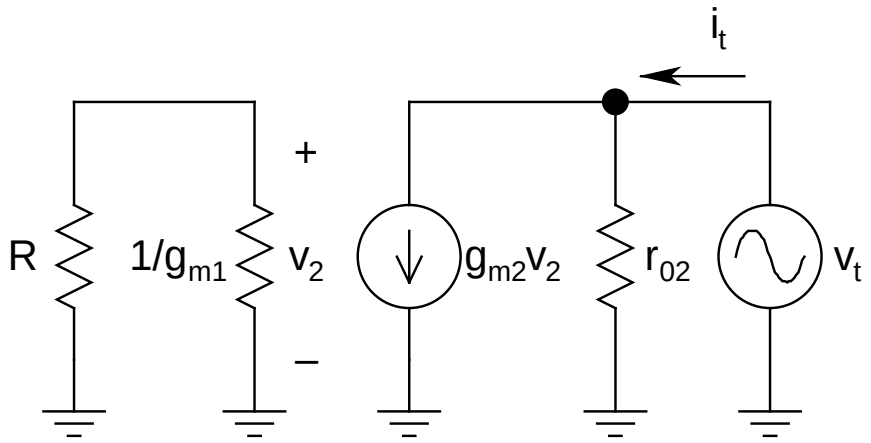


  - The ***small-signal equivalent*** consists simply of $1/g_m$, which is similar to r_D for ***diodes***
    - Hence the name ***diode-connected MOSFET***

- ***For the complete circuit***:
  - ***Left part of the circuit has no source***

    $\Rightarrow v_2 = 0$

    $\Rightarrow g_{m2}v_2 = 0$

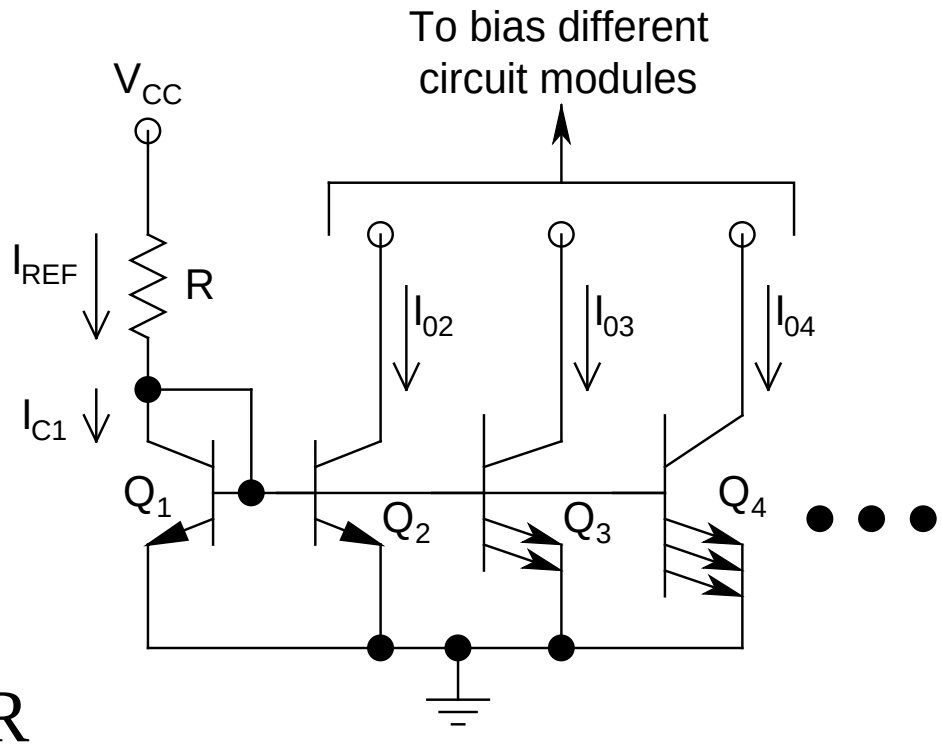


  - Thus, $R_0 = v_t/i_t = r_{02} = 1/(\lambda I_0)$
  - For a ***good current source***, ***R_0 should be as large as possible*** (***ideally infinite***)

    $\Rightarrow$ ***λ should be as small as possible*** and/or ***I_0 should be as small as possible***

- ***Golden Rule for Calculation of R_0***:
  - For a ***BJT*** (or ***MOSFET***):
    - With E (or S) ***grounded***
    - ***No electrical connection*** (***feedback***) between C (or D) and B (or G)
    - ***Looking from*** the C (or D)
      - ***The only resistance seen will be the output resistance of the BJT (or MOSFET)***

- ***npn Current Repeater***:
  - ***Uses multi-emitter BJTs***
  - ***Maximum number of emitters = 4***
  - ***All emitters tied together***
  - ***All Qs have same V_{BE}***
  - $I_{REF} = (V_{CC} - V_{BE})/R$

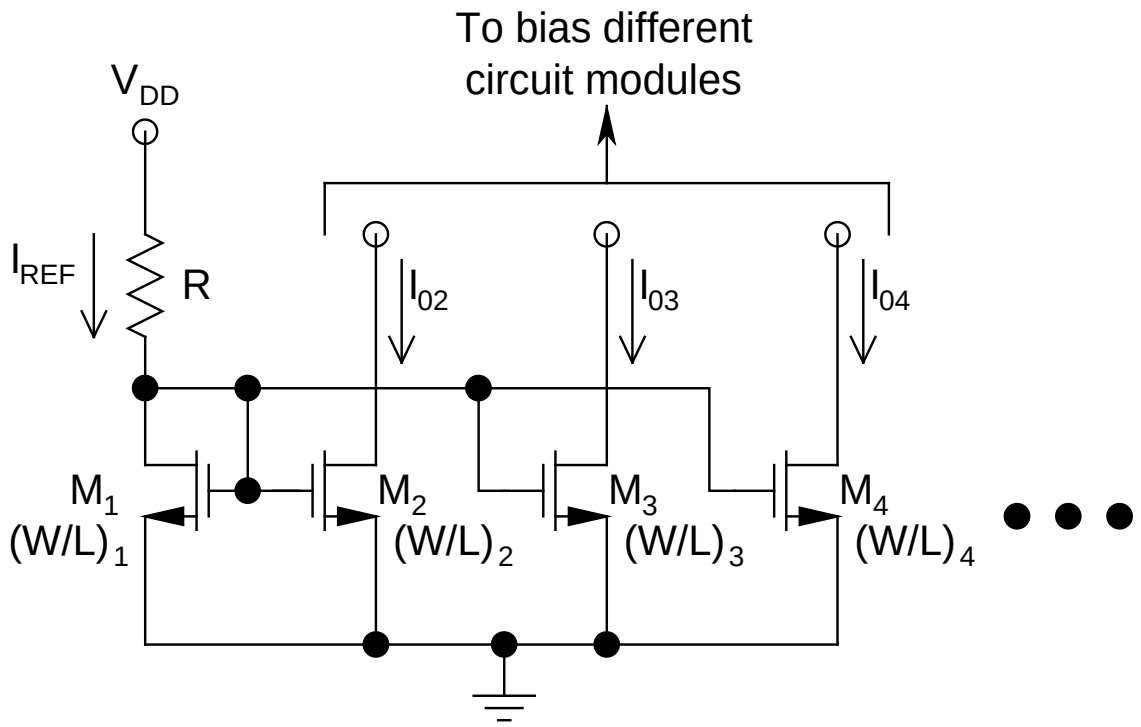


- ***Neglecting I_B***:

  $I_{02} = I_{REF}$, $I_{03} = 2I_{REF}$, $I_{04} = 3I_{REF}$, …

- ***Limitations***:
  - ***Output current can never be a non-integer ratio of I_{REF} $\Rightarrow$ no arbitrary scaling possible***
  - ***Loading Problem***:
    - ***I_{REF} not only supplies I_{C1}, but I_Bs of all the Qs***
    - ***As more Qs are added, I_Bs will keep on increasing***
    - ***I_{C1} starts to depart significantly from I_{REF}***
    - ***It's not I_{REF} that's mirrored, it's I_{C1}***
    - ***A reduction in I_{C1} will affect all output currents***
    - ***Hence, this circuit is not very popular***

- ***NMOS Current Repeater***:



- $I_{REF} = I_{D1} = (V_{DD} - V_{GS})/R$

$$I_{D1} = \frac{k'_N}{2}\left(\frac{W}{L}\right)_1 V_{GT}^2 \quad \left(\textbf{\textit{assuming } } \lambda V_{DS} < 0.1\right)$$

- ***All Ms have same V_{GS} and are matched***

$$\Rightarrow I_{0i} = \frac{(W/L)_i}{(W/L)_1} I_{REF} \quad (i = 2, 3, 4, \ldots)$$

- ***Tremendous flexibility***
  - ***Any arbitrary current ratio can be obtained***
  - ***No loading effect***
  - ***Highly popular and universal choice***

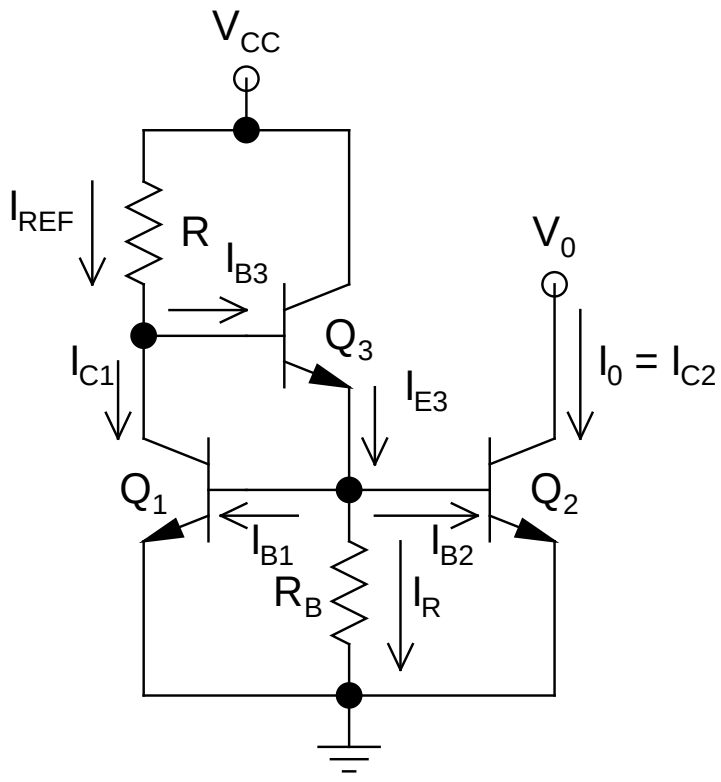
- ***More on W/L Ratio***:
  - ***Generally, in technology, W/L is kept between 0.01 and 100***
  - ***The ideal ratio is between 0.02 and 50***
  - ***Minimum Feature Size*** (MFS):
    - ***Minimum dimension that can be resolved in an IC chip***
      - ***Has gone down from 10s of μm in 80s to a few nm now***!
  - ***For W/L > 1 (or < 1), L (or W) is chosen equal to MFS***
    - ***Yields minimum possible device area*** (W × L)

- ***npn CM With Better β Insensitivity***:
  - $I_{REF} = (V_{CC} - 2V_{BE})/R$
  - Neglecting I_{B3}:

    $I_{C1} = I_{REF}$
  - ***If Q_1 and Q_2 are matched***:

    $I_0 = I_{C2} = I_{C1} = I_{REF}$

    $\Rightarrow$ ***Simple CM***
  - ***The actual advantage of the circuit lies elsewhere***!



- First, assume ***R_B is absent***

$$\Rightarrow I_{E3} = I_{B1} + I_{B2} = I_{C1}/\beta_1 + I_{C2}/\beta_2 = 2I_0/\beta_1$$

(***assuming $\beta_1 = \beta_2$***)

$$\Rightarrow I_{B3} = \frac{I_{E3}}{\beta_3 + 1} = \frac{2I_0}{\beta_1(\beta_3 + 1)}$$

$$I_{REF} = I_{C1} + I_{B3} = I_0\left[1 + \frac{2}{\beta_1(\beta_3 + 1)}\right]$$

$$\Rightarrow I_0 = \frac{I_{REF}}{1 + \dfrac{2}{\beta_1(\beta_3 + 1)}}$$

- Now, if $\beta_1 = \beta_3 = \beta$, and $\beta >> 1$:

  $I_0 \approx I_{REF}(1 - 2/\beta^2)$
- Compare with that of simple CM:

  $I_0 \approx I_{REF}(1 - 2/\beta)$
- ***The advantage is obvious***!
- ***Further Insights***:
  - I_{E3} (= $I_{B1} + I_{B2}$) ~ ***few 10s of μA***
  - ***At such a low current, β drops significantly from its nominal value***
  - ***Thus, full advantage of the circuit can't be exploited***

- ***Here comes the role of R_B***:
  - ***It drains a constant current*** (= V_{BE}/R_B), ***which gets added to*** ($I_{B1} + I_{B2}$), and ***boosts*** I_{E3} (and, thus, I_{C3})
  - ***Thus, β_3 gets pulled up to its nominal value***
  - ***This resistor has a special name***: ***Keep Alive***, ***since it keeps Q_3 alive***!
- ***However, it creates some issues as well***:
  - ***Additional power drain due to the additional current flowing through R_B***
  - ***If $I_{E3} \uparrow$, so would I_{B3}***

    $\Rightarrow$ I_{C1} may depart from I_{REF}
  - ***Design optimization needed***

- ***Now, for R_0***:
  - ***Looking at C_2***
  - ***E_2 grounded***
  - ***No connection between C_2 and B_2*** (***no feedback***)
  - ***Therefore, by inspection***:

    $R_0 = r_{02} = V_{A2}/I_0$

- ***Also, by inspection***:

  $V_{0,min} = V_{CE2}(SS) = 0.2\ V$

- ***There is no MOS counterpart for this circuit for obvious reasons***!

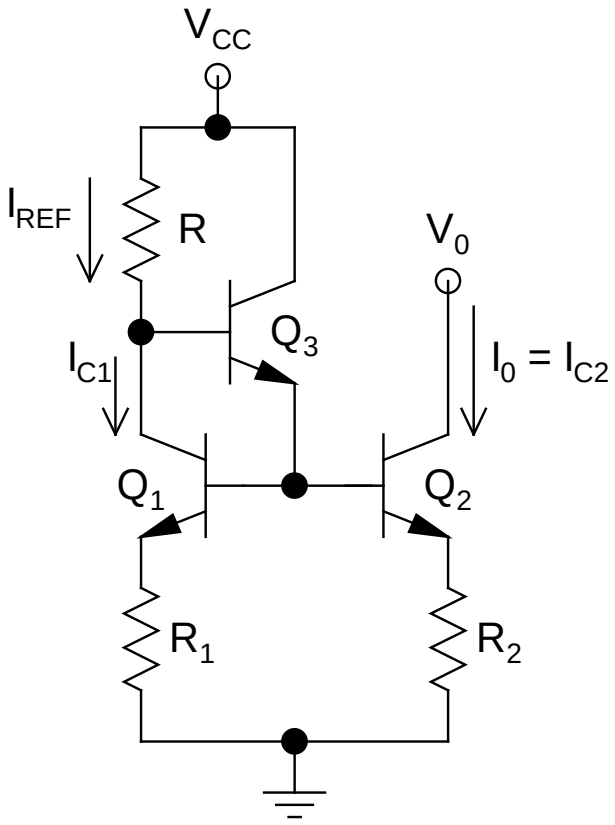
- ***npn Ratioed CM***:
  - ***Q_1-Q_2 matched pair***
  - ***Neglecting all I_B***, $I_{E1} = I_{C1}$ $= I_{REF}$, and $I_{E2} = I_{C2} = I_0$
  - $I_{REF} = (V_{CC} - 2V_{BE})/(R + R_1)$
  - ***KVL around Q_1-Q_2 BE loop***:

    $V_{BE1} + I_{REF}R_1 = V_{BE2} + I_0R_2$

    $\Rightarrow I_0 = (I_{REF}R_1 + \Delta V_{BE})/R_2$

    $\Delta V_{BE} = V_{BE1} - V_{BE2}$

    $= V_T \ln(I_{REF}/I_0)$



- ***Note the ln dependence***:
  - ***For $I_{REF}/I_0 = 2$, $\Delta V_{BE} = 18$ mV***
  - ***For $I_{REF}/I_0 = 10$, $\Delta V_{BE} = 60$ mV***

  $\Rightarrow$ ***ΔV_{BE} can be neglected if $I_{REF}R_1 > 10\Delta V_{BE}$***

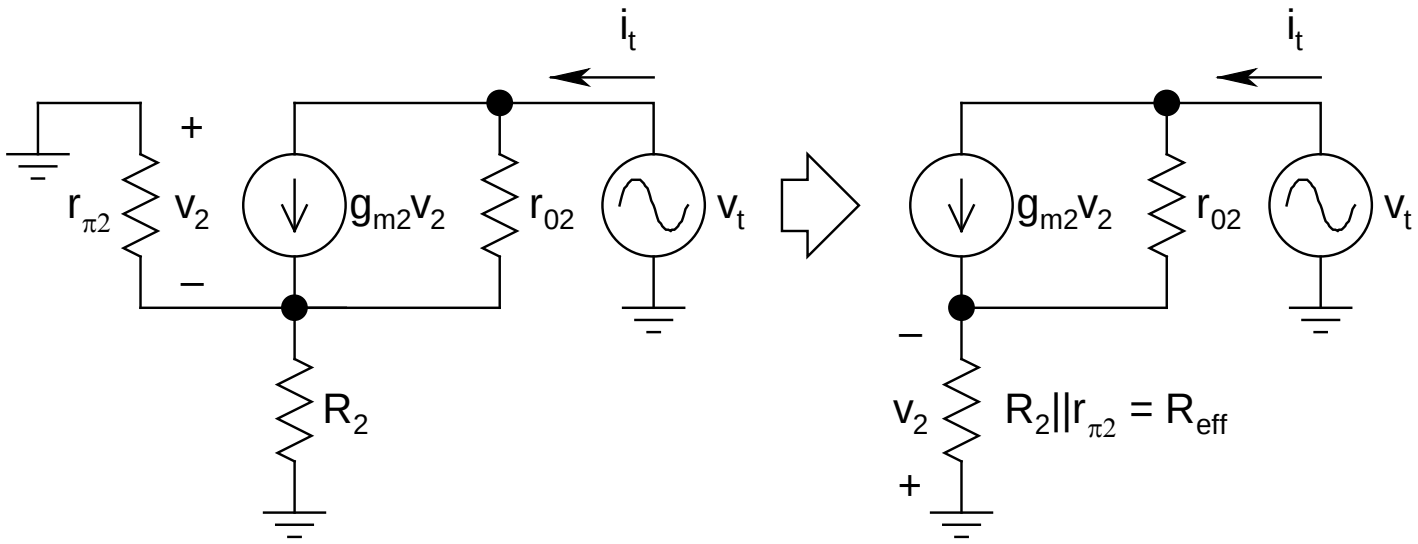
  $\Rightarrow$ ***$I_0 = (R_1/R_2)I_{REF}$*** (***Ratioed Mirror***)
- ***Thus, by tinkering R_1 and R_2, any ratio between I_0 and I_{REF} can be obtained***
  - ***Tremendous advantage***
    - ***Widely used***
- ***By inspection***:

$$V_{0,min} = V_{CE2}(SS) + I_0R_2 = 0.2 + I_0R_2$$

➢ *Calculation of R_0*:

- *Golden Rule can't be used since emitter of Q_2 is not grounded* (*R_2 present there*)
- *Needs analysis*

  $\Rightarrow$ *Leads to a module that is frequently encountered*
- *Base of Q_1-Q_2 at a fixed DC potential* $\Rightarrow$ *ac ground*



$$i_t = g_{m2} v_2 + \left(v_t + v_2\right)/r_{02}$$

$$= v_t/r_{02} + \left(g_{m2} + 1/r_{02}\right) v_2 \simeq v_t/r_{02} + g_{m2} v_2$$

$$v_2 = -i_t R_{eff}$$

$$\Rightarrow i_t = v_t/r_{02} - g_{m2} R_{eff} i_t$$

$$\Rightarrow R_0 = v_t/i_t = r_{02}(1 + g_{m2} R_{eff})$$

- This is a ***Golden Equation***, which would be ***used frequently***
  - ***Carefully note the topology that produces this result***
- ***Exercise***: ***Reverse v_2 and show that the expression for R_0 remains invariant***

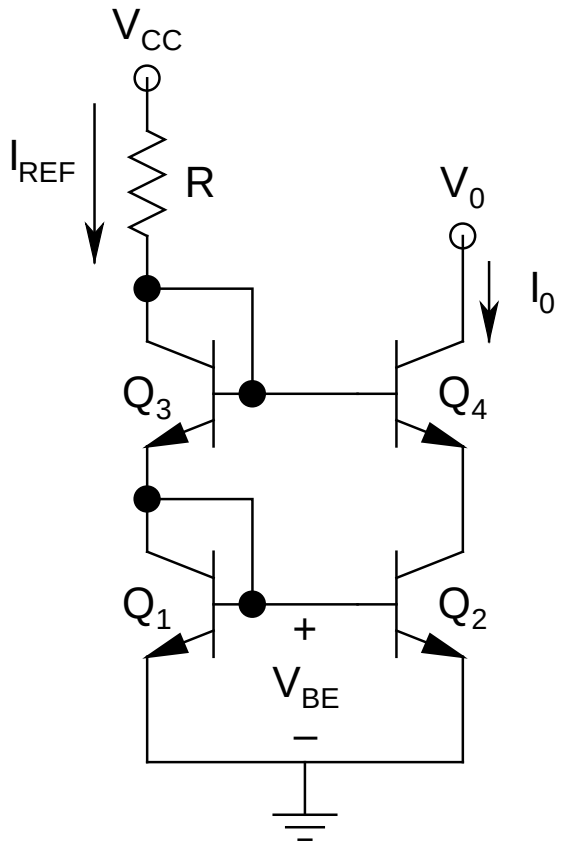
- If $r_{\pi 2} >> R_2$, $R_0 = r_{02}(1 + g_{m2}R_2)$
- If $R_2 >> r_{\pi 2}$, $R_0 \approx \beta_2 r_{02}$ (since $\beta = g_m r_\pi >> 1$)
- ***Under the second condition, the circuit produces enormously large value of R_0 ~ 10s of MΩ or greater***
  - ***Almost approaches a constant current source***!
- ***It's good to check the relative values of R_2 and $r_{\pi 2}$ before using either of the equations***
- ***This circuit does not have any MOS counterpart for obvious reasons***!

- ***Cascode Current Source*:**
  - ***The best and most widely used***
  - ***Almost universal choice for biasing IC stages***
  - ***Produces extremely high R_0***
  - ***Original cascode needs higher values of $V_{0,min}$***
  - ***Modified cascode gets rid of this problem and pushes $V_{0,min}$ down***
  - ***The topology is basically two simple CMs stacked one upon the other***
  - ***Both npn and NMOS implementations exist***

- ***npn Cascode***:
  - ***All Qs are perfectly matched***
  - ***Neglecting I_B and V_A***:

    $I_0 = I_{REF} = (V_{CC} - 2V_{BE})/R$
  - Show that if ***I_B can't be neglected***, but ***all Qs have same β***:

$$I_0 = \frac{I_{REF}}{1+(4\beta+2)/\beta^2}$$



  - Thus, ***β immunity is not that pronounced***

- ***All Qs operate with the same V_{BE}***

  $\Rightarrow V_{B1} = V_{B2} = V_{BE}, V_{B3} = V_{B4} = 2V_{BE}$

  $\Rightarrow V_{E4} = V_{C2} = V_{BE}$

  $\Rightarrow V_{BE2} = V_{CE2}$

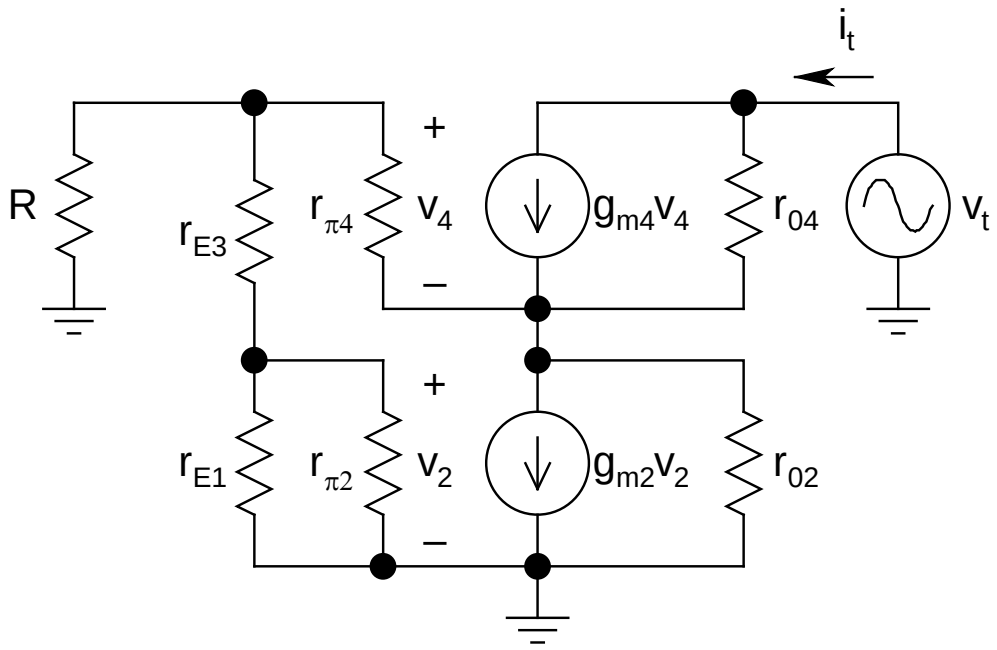
  $\Rightarrow$ ***Q_2 can never saturate, but Q_4 can***!

  $\Rightarrow V_{0,min} = V_{BE} + V_{CE4}(SS) = 0.7 + 0.2 = 0.9$ V

- ***The output voltage swing is sacrificed quite a bit***!

- ***However, the main advantage of this circuit is enormously large R_0***

➢ *Calculation of R_0*:



Exact Equivalent

- ***Q_1 and Q_3 diode-connected*** $\Rightarrow$ r_{E1} and r_{E3}

- Note that to a ***first-order estimate***, ***bases of Q_1-Q_2 and Q_3-Q_4*** can be considered to be at a ***fixed DC potential***, and thus, ***ac ground***

  $\Rightarrow v_2 = 0 \Rightarrow g_{m2}v_2 = 0$

  $\Rightarrow$ Leads to the ***simplified equivalent*** (looks familiar?)

- ***By inspection***:

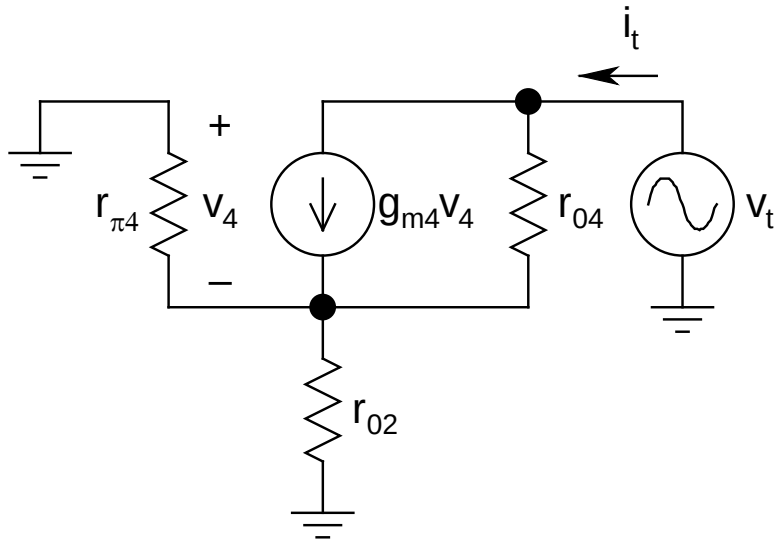
  $R_0 \approx r_{o4}(1 + g_{m4}r_{\pi4})$

  $\approx \beta_4 r_{04}$

  (***assuming $r_{o2} >> r_{\pi4}$***)

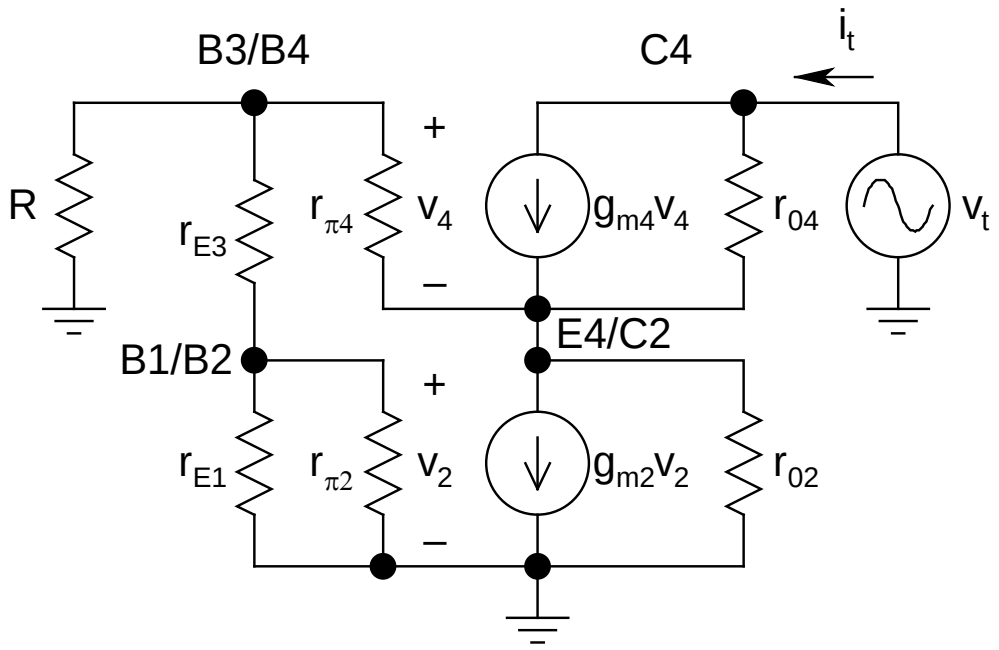
- ***Actual analysis gives***:

  $R_0 = \beta_4 r_{04}/2$ (***large error***!)



Simplified Equivalent

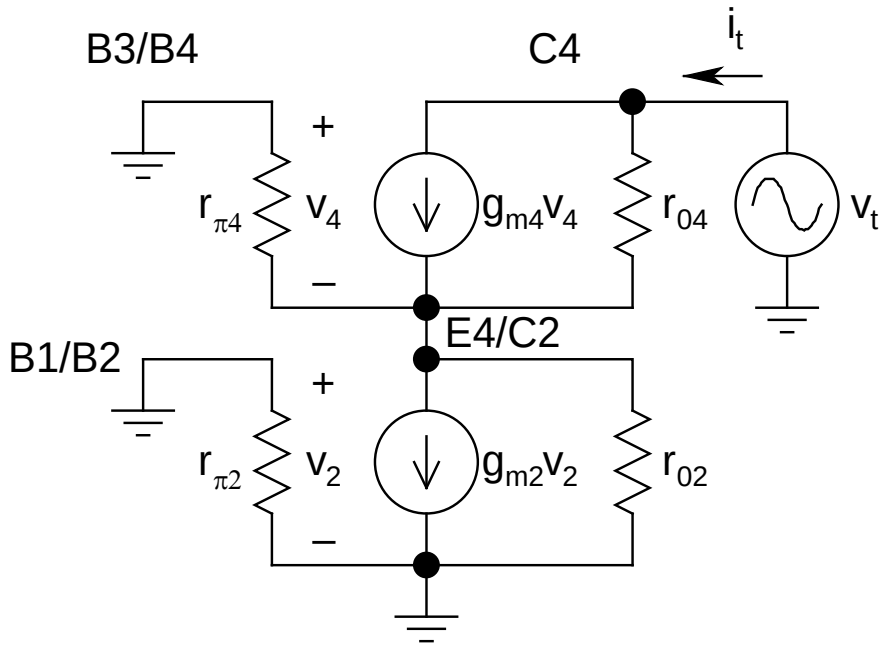
➢ *Calculation of R_0*:



Exact Equivalent

- ***Q_1 and Q_3 diode-connected*** $\Rightarrow$ r_{E1} and r_{E3}

- ***Simplification***:
  - ***Bases of Q_1-Q_2 and Q_3-Q_4 can be approximated to be at ac ground*** (***a first-order estimate***)



Equivalent after First-Order Simplification

- $\Rightarrow v_2 = 0 \Rightarrow g_{m2}v_2 = 0$

  $\Rightarrow$ Leads to the ***simplified equivalent*** (looks familiar?)

- ***By inspection***:

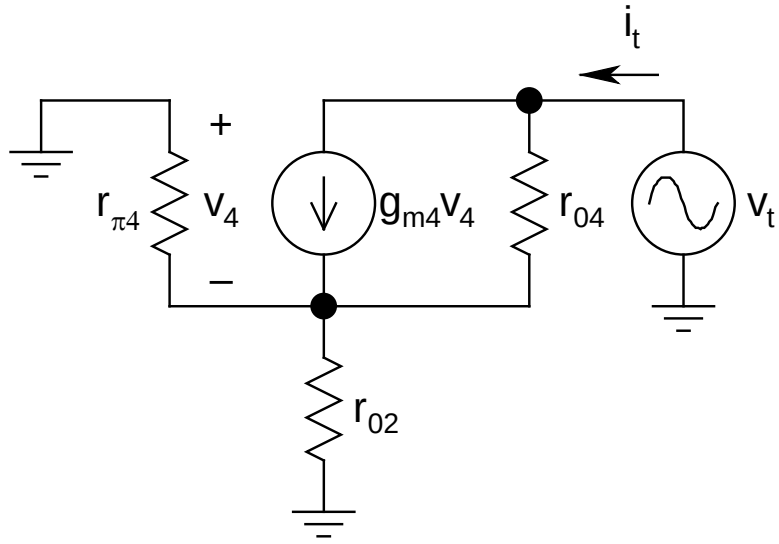
  $R_0 \approx r_{o4}(1 + g_{m4}r_{\pi 4})$

  $\approx \beta_4 r_{04}$

  (***assuming $r_{o2} >> r_{\pi 4}$***)

- ***Actual analysis gives***:

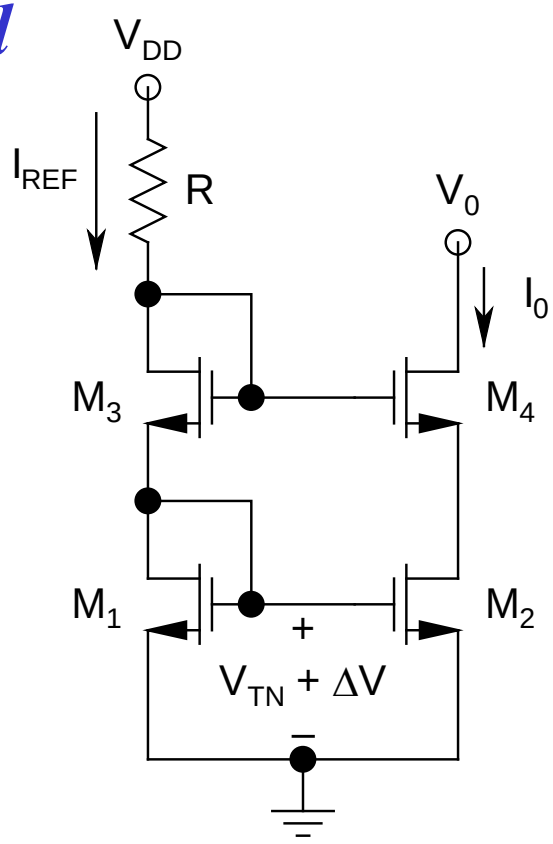
  $R_0 = \beta_4 r_{04}/2$ (***large error***!)



Simplified Equivalent

- ***NMOS Cascode***:
  - ***All Ms perfectly matched***
  - ***All bodies connected to ground***
    - ***M_1-M_2 does not have body effect, but M_3-M_4 does!***
    - ***Makes hand analysis quite tedious***

      $\Rightarrow$ ***Neglect body effect***
  - ***All Ms operate with same V_{GS}***
  - Define $\Delta V = V_{GS} - V_{TN} = V_{GT}$
    - ΔV = ***Gate Overdrive***



- ***The reference current***:

$$I_{REF} = \frac{V_{DD} - 2V_{GS}}{R} = \frac{k_N}{2} V_{GT}^2 \quad (\textit{neglecting } \lambda)$$

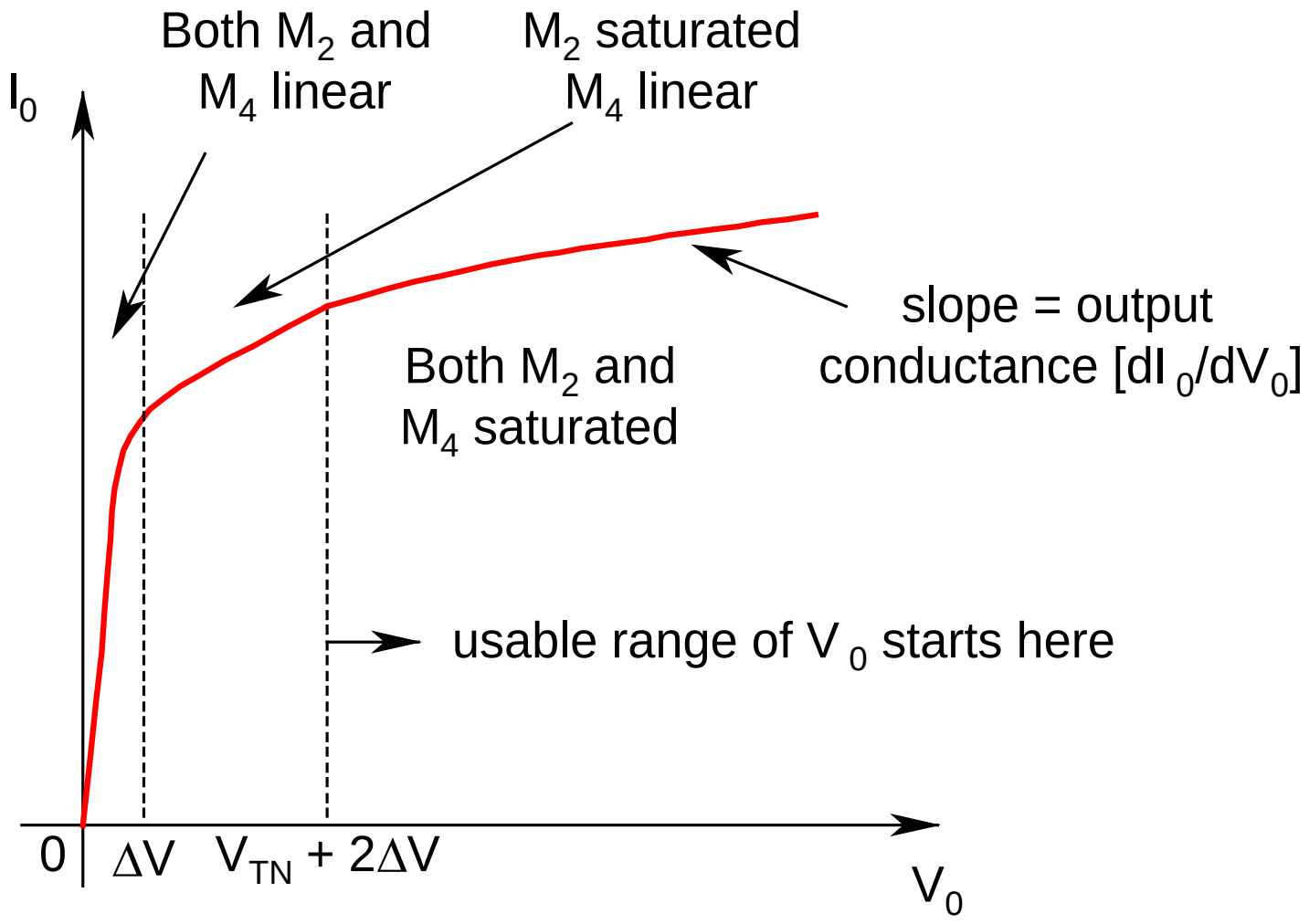
- ***V_{GS} and I_{REF} can be found*** $\Rightarrow I_0 = I_{REF}$
- $V_{G1} = V_{G2} = V_{GS} = V_{TN} + \Delta V$
- $V_{G3} = V_{G4} = 2V_{GS} = 2(V_{TN} + \Delta V)$
- $V_{S4} = V_{D2} = V_{TN} + \Delta V$

  $\Rightarrow V_{GS2} = V_{DS2}$

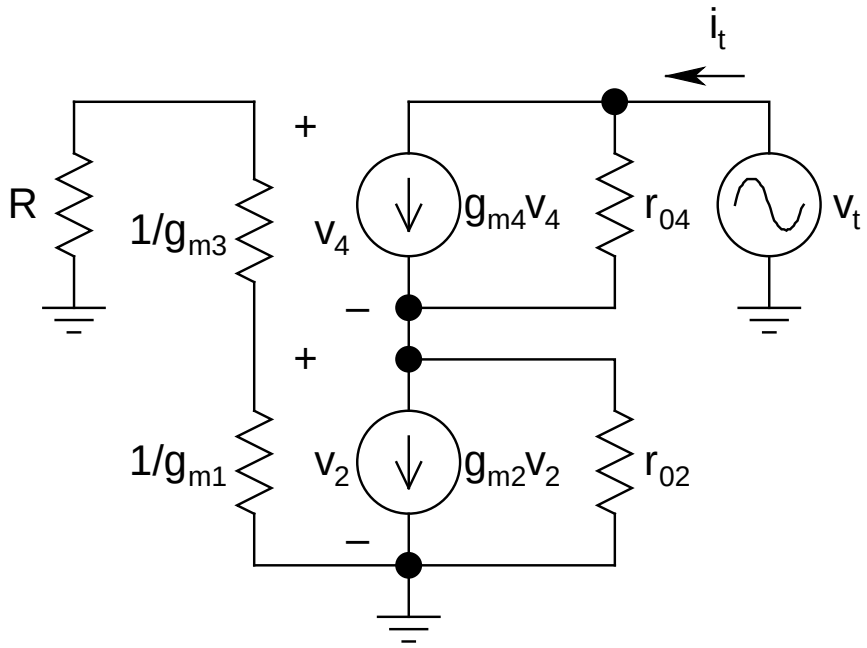
  $\Rightarrow$ ***M_2 can never enter linear region***

  $\Rightarrow V_{0,min} = V_{DS2} + V_{DS4} = V_{TN} + 2\Delta V$

- ***This can be quite significant, since V_{TN} is added to ΔV***
  - ***Assuming $\Delta V \sim 0.1$ V and $V_{TN} \sim 0.7$ V, $V_{0,min} \sim 0.8$ V, which is very large***
  - ***This is one of the drawbacks of this simple cascode circuit (modified cascode doesn't have this problem)***
- ***If V_0 drops below $(V_{TN} + 2\Delta V)$, first M_4 enters linear region, and circuit performance starts to get affected***
- ***For further drop in V_0, M_2 also enters linear region, and the current mirror collapses!***


Both M_2 and
M_4 linear
M_2 saturated
M_4 linear
I_0
slope = output
conductance [dI_0/dV_0]
Both M_2 and
M_4 saturated
usable range of V_0 starts here
0
ΔV
$V_{TN} + 2\Delta V$
V_0

➢ *Calculation of R_0*:



Exact Equivalent

- ***M_1 and M_3 diode-connected*** $\Rightarrow$ $1/g_{m1}$ and $1/g_{m3}$

- ***The left part of the circuit has no source***

  $\Rightarrow v_2 = 0 \Rightarrow g_{m2}v_2 = 0$

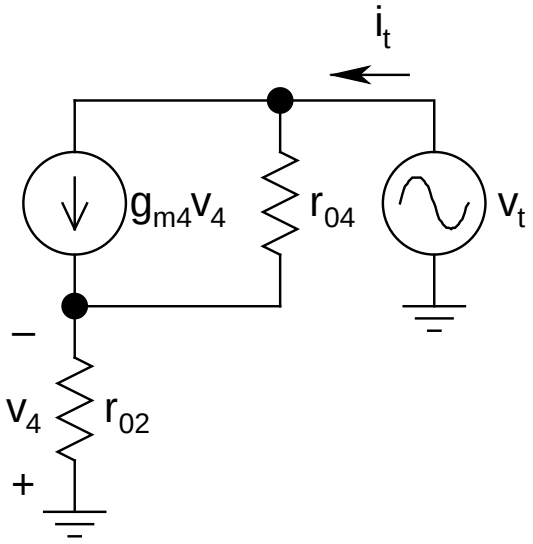
  $\Rightarrow$ ***Leads to the simplified equivalent*** (now should look very familiar!)

- ***By inspection***:

  $R_0 \approx r_{o4}(1 + g_{m4}r_{02})$

  $\approx g_{m4}r_{02}r_{04}$

- ***Can be huge***!



Simplified Equivalent

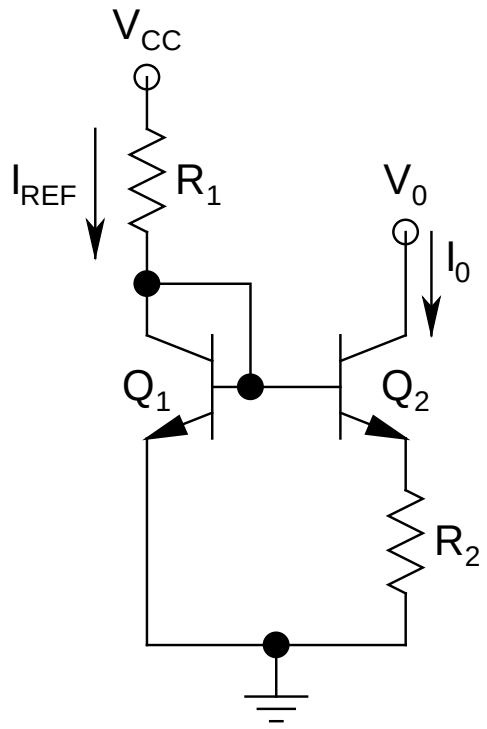
- ***Double Cascode*:**
  - ***Can be implemented in both BJT & MOS***
  - ***In npn Double Cascode, another pair Q_5-Q_6 stacked upon Q_3-Q_4***
    - ***Find $V_{0,min}$ and R_0***
  - ***In NMOS Double Cascode, another pair M_5-M_6 stacked upon M_3-M_4***
    - ***Find $V_{0,min}$***
    - $R_0 \approx g_{m6}r_{06}R_0$ ($R_0 \approx g_{m4}r_{02}r_{04}$)
  - ***Hence, show that double cascode in BJT offers absolutely no advantage in terms of R_0***

- ***Low Value Current Source***:
  - ***Current thrust***: ***Low-power circuits***

    $\Rightarrow$ ***Increase in battery life***
  - ***If bias current can be reduced from mA to μA, for the same power supply voltage, power drawn reduces by three orders of magnitude***!
  - ***Normal CMs can also produce bias current in μA range***, however, ***the required resistance will be huge*** $\Rightarrow$ ***uneconomical for ICs***
  - ***Most common***: ***Widlar Current Source***
    - ***After its inventor Bob Widlar*** (***father of op-amp***)

- ***Widlar Current Source***:
  - ***Q_1-Q_2 matched pair***
  - $I_{REF} = (V_{CC} - V_{BE1})/R_1$
  - If $I_0 = I_{REF}$, then $V_{BE1} = V_{BE2}$
    - ***No drop across R_2***!

      $\Rightarrow I_0 \neq I_{REF}$
  - ***Actually, the difference between V_{BE1} and V_{BE2} drops across R_2***



- ***KVL around Q_1-Q_2 BE loop***:

$$V_{BE1} = V_{BE2} + I_0 R_2$$

$$\Rightarrow I_0 = \frac{V_{BE1} - V_{BE2}}{R_2} = \frac{V_T}{R_2} \ln\left(\frac{I_{REF}}{I_0}\right)$$

(***since $I_{S1} = I_{S2}$***)

- ***Transcendental equation in I_0***
- ***If I_0 is known***, ***finding R_2 is absolutely easy***!
- On the other hand, ***if R_2 is given***, ***to find I_0***, ***need to iterate***, ***but the solution will converge rapidly*** (***Why***?)

- ***The ln function compresses a large difference between I_{REF} and I_0 into a small range***
  - For I_{REF} ~ mA, I_0 ~ μA, with R_1 ~ few kΩs and R_2 ~ few 10s of kΩ

    ⇒ ***Significant flexibility***!
- $V_{0,min} = V_{CE2}(SS) + I_0R_2$

  ~ ***0.3-0.4 V for practical values of I_0 and R_2***
- ***R_0 can be obtained by sheer inspection of the circuit by noting that the base of Q_2 is approximately at ac ground***
- Also, $r_{\pi 2} >> R_2$ (***Why***?)

- Thus,

  $R_0 \approx r_{02}(1 + g_{m2}R_2)$

- ***Note***: ***To approximate this as $g_{m2}r_{02}R_2$, first make sure that $g_{m2}R_2 >> 1$*** (***may not be***!)
- ***Actual expression***:

  $R_0 \approx r_{02}(1 + g_{m2}R_{eff})$ with $R_{eff} = R_2 \| r_{\pi 2}$

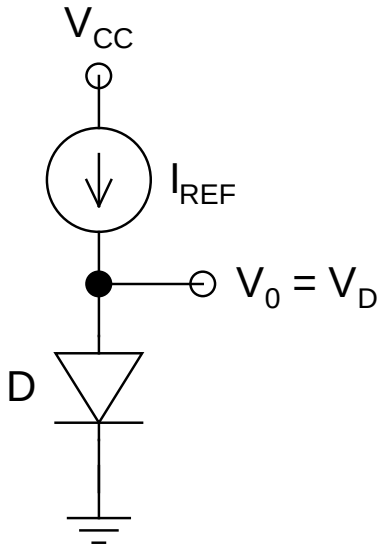
- ***During further simplification***, ***always check the validity of your assumption/approximation***
  - ***Otherwise it may lead to large errors***!
- ***Counterpart of this circuit in MOS technology does not exist*** (***Why***?)

DC Voltage References

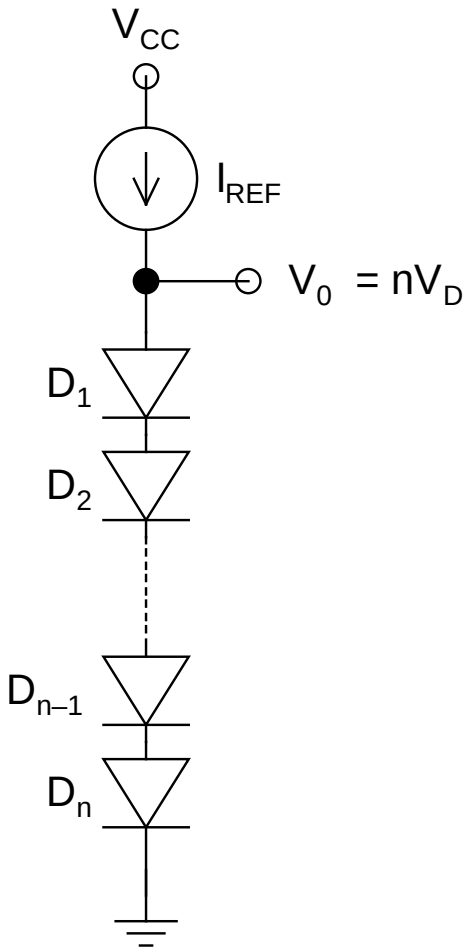
- ***Along with current sources/sinks*, *also need stable and precise DC voltage references***
- ***Provides DC bias voltages at specific points of the circuit***
- ***Should be independent of power supply and temperature***
- ***Can range from –ve to +ve power supplies***
- ***On-Chip*: *Generated within the chip itself***

- ***In ICs**, diodes are not fabricated as such*
  - ***BJTs/MOSFETs are used as diodes by shorting their B/G and C/D terminals***
- ***Various Voltage References**:*
  - ***Single Diode Reference***
  - ***Multiple Diode Reference***
  - ***V_{BE} (or V_D) Multiplier***
  - ***Saturated Transistor***
  - ***NMOS Voltage Reference***

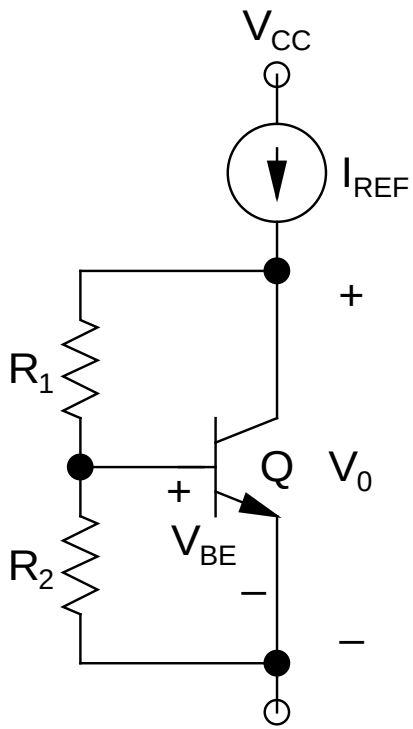
- ***Single Diode Reference***:
  - I_{REF}: ***DC Bias Current***
  - ***Creates a voltage drop of V_D (or V_{BE}) across the diode of ~ 0.7 V***
  - ***Known as V_{BE} (or V_D) Reference***
  - ***Precision quite poor***
  - ***Thermal tracking poor***



- ***Multiple Diode Reference***:
  - ***Putting multiple diodes in series***
  - ***DC bias current I_{REF} pushed through them***
  - ***Each diode creates a drop of V_D across it***
  - ***Has same problems as Single Diode Reference***
  - ***Note***: ***n can only be an integer***



- ***V_{BE} (or V_D) Multiplier Circuit*:**
  - ***Previous two circuits provide $V_0 = nV_D$, with n being an integer ≥ 1***
  - ***For any arbitrary value of n (≥ 1), this circuit becomes useful***
  - ***Immensely popular because of its simplicity and effectiveness***
  - ***Biased by a DC current source I_{REF}***



- ***Neglecting base current***:

$$V_{BE} = \frac{R_2}{R_1 + R_2} V_0$$

$$\Rightarrow V_0 = \left(1 + \frac{R_1}{R_2}\right) V_{BE}$$

$\Rightarrow$ ***V_{BE} Multiplier*** with ***multiplication factor ($1 + R_1/R_2$)***

- ***Any arbitrary ratio of R_1 and R_2 can be used, but the multiplication factor is always ≥ 1***

- ***Least possible*** $V_0 = V_{BE}$ [$R_1 = 0$ (***short-circuit***) and $R_2 \rightarrow \infty$ (***open-circuit***)]

  $\Rightarrow$ ***Diode-Connected BJT***

- ***Has excellent thermal tracking***, ***since*** TC_F ***of*** R_1 ***and*** R_2 ***cancel each other***, ***but the*** TC_F ***of*** V_{BE} ***remains***

- ***So far, we have got voltage references having*** $V_0 \geq V_{BE}$

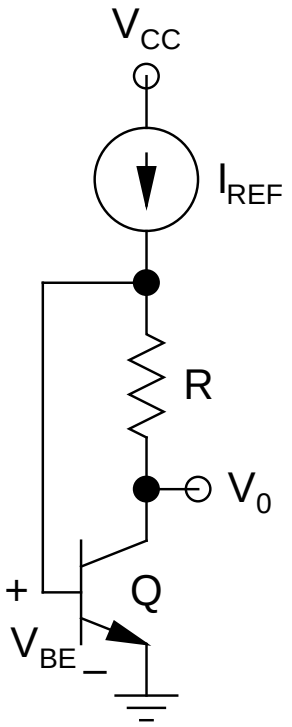
- ***How to have a voltage reference having*** $V_0 < V_{BE}$***?***

- ***Saturated Transistor***:
  - ***Neglecting base current***:

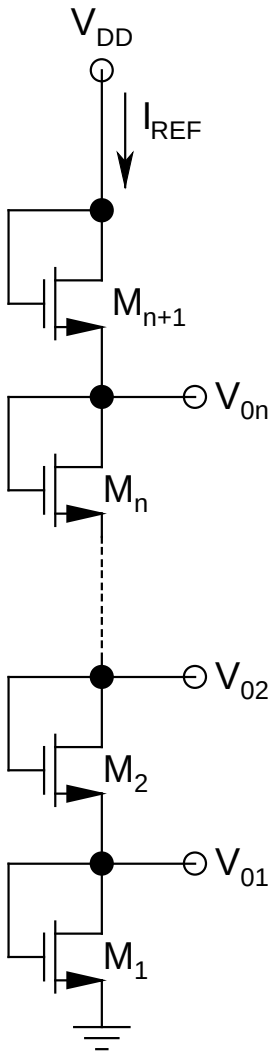
    $V_0 = V_{BE} - I_{REF}R$
  - ***Note***: ***V_0 is actually V_{CE}, which is < V_{BE}***

    $\Rightarrow$ ***Q saturated***

    $\Rightarrow$ ***Analysis highly approximate, since base current can't be neglected in saturation***
  - ***Typical range of V_0 ~ 0.2-0.7 V***



- ***NMOS Voltage Reference*:**
  - ***Highly popular due to its simplicity and effectiveness***
  - ***Can generate n voltage references from (n + 1) MOSFETs***
  - ***All MOSFETs diode-connected***
    ⇒ Always saturated
  - ***No resistors needed***
  - ***All bodies connected to ground***



- ***Only for M_1***, $V_{TN1} = V_{TN0}$
- ***All other MOSFETs will have body effect***,

  e.g., $V_{TN2} = V_{TN0} + \gamma\left(\sqrt{2\phi_F + V_{01}} - \sqrt{2\phi_F}\right)$
- Generally, ***all λs also same***, but ***aspect ratios are different***
- $V_{01}, V_{02}, \ldots, V_{0n}$ are the ***needed reference taps***
- $V_{GS1} = V_{DS1} = V_{01}$, $V_{GS2} = V_{DS2} = V_{02} - V_{01}$, $V_{GS3} = V_{DS3} = V_{03} - V_{02}, \ldots$
- $V_{SB1} = 0$, $V_{SB2} = V_{01}$, $V_{SB3} = V_{02}, \ldots$
- ***Same DC current I_{REF} flows through all MOSFETs***

- Assuming that ***all MOSFETs*** have ***same*** λ and ***same*** k'_N:

$$I_{REF} = \frac{k'_N}{2}\left(\frac{W}{L}\right)_1 \left(V_{01} - V_{TN1}\right)^2 \left(1+\lambda V_{01}\right)$$

$$= \frac{k'_N}{2}\left(\frac{W}{L}\right)_2 \left(V_{02} - V_{01} - V_{TN2}\right)^2 \left[1+\lambda\left(V_{02} - V_{01}\right)\right]$$

•••

- ***First I_{REF} needs to be found by ensuring that the circuit dissipates least DC power***
- ***Then, all (W/L)s can be calculated***

- ***Choice depends on several design paradigms***
- $P_D = V_{DD} \times I_{REF}$

  $\Rightarrow$ ***For minimum P_D, I_{REF} should be minimum***
- ***Need to pick up a reference MOSFET to start the design process***
- ***Area of a MOSFET*** = W × L
- ***For minimum area***, W = L = MFS
  - ***MFS***: ***Minimum Feature Size*** (***that is allowed by the technology***)
- Pick the ***reference MOSFET*** by choosing its ***(W/L) = 1***, and having the ***least*** $V_{GT}^2\left(1+\lambda V_{DS}\right)$

- ***This will yield minimum P_D***
- ***Once the reference MOSFET is chosen, I_{REF} becomes known***, and ***(W/L)s of all other MOSFETs can be calculated***
- ***Total area taken up by the circuit***:

$$\sum_{n}\left(W \times L\right)_{n}$$

- ***Care***: ***No dimension can be < MFS***
- ***Then what to do if (W/L) < 1***?