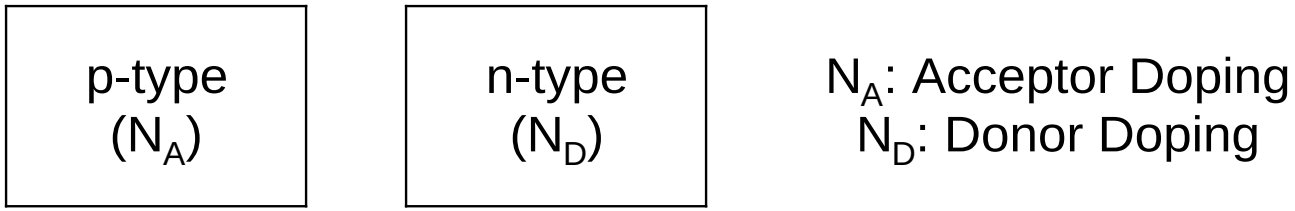
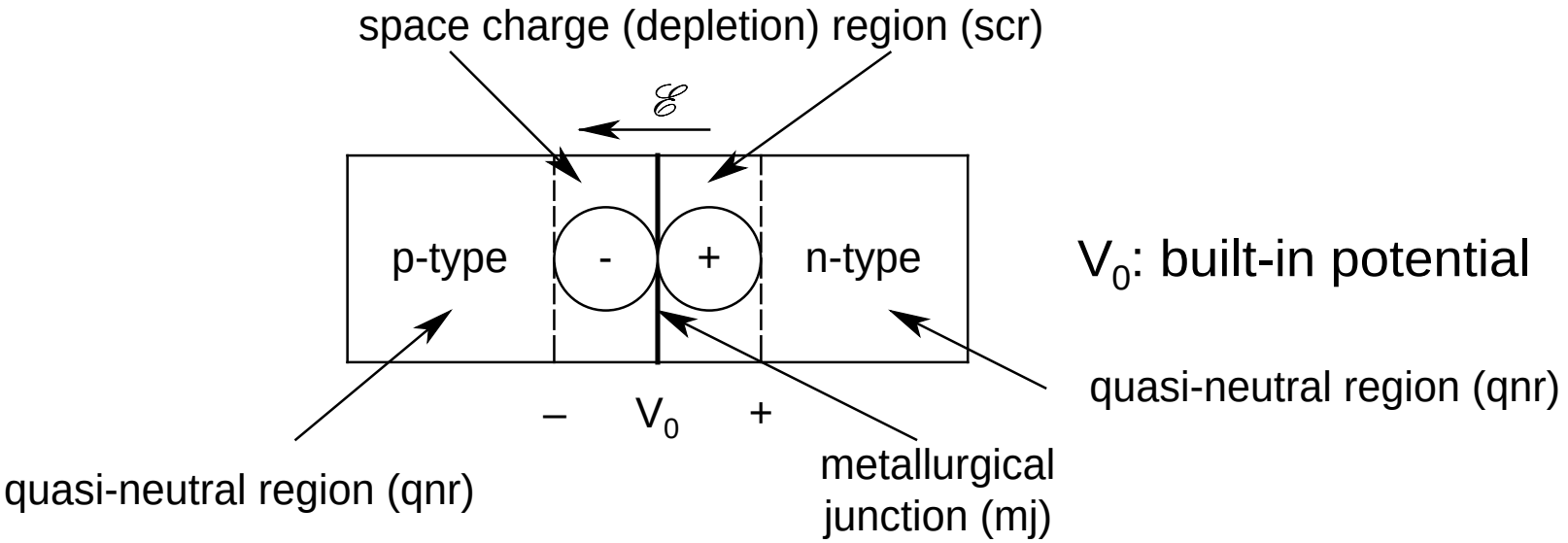
DIODE



Before Joining

- ***p-side***:
  - ***Holes majority carriers***
  - ***Electrons minority carriers***
- ***n-side***:
  - ***Electrons majority carriers***
  - ***Holes minority carriers***
- ***Holes***: ***Anti-particles*** of ***electrons***



After Joining (**In Equilibrium**)

- ***Dissociation Relations***:

$$N_A \leftrightarrow N_A^- + \text{hole}$$

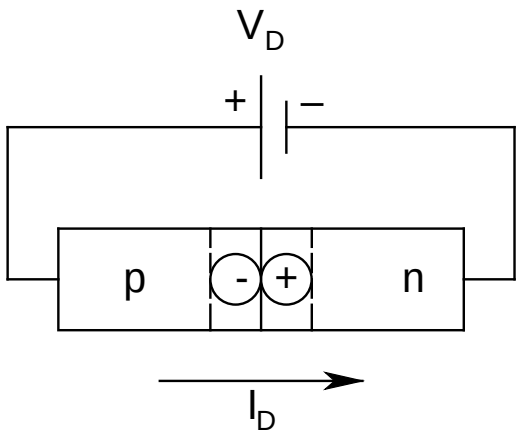
$$N_D \leftrightarrow N_D^+ + \text{electron}$$

Establishment of Equilibrium

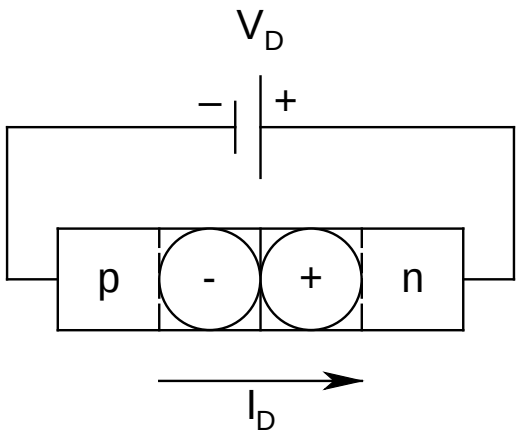
- ***Holes diffuse from p to n***
  - ***Negatively charged acceptor ions uncovered near MJ***
- ***Electrons diffuse from n to p***
  - **Positively charged donor ions uncovered near MJ**
- ***Establishment of a charge dipole around MJ***
  - ***Generation of an electric field $\mathscr{E}$ around MJ***
  - ***Creation of built-in potential V_0***

- ***$\mathscr{E}$ creates drift components of carriers***
  - ***Holes pushed back to p***
  - ***Electrons pushed back to n***
- When these two motions (***drift and diffusion***) completely ***balance out***
  - ***Equilibrium*** is reached
- Under this condition, the ***net fluxes*** of ***both electrons and holes*** across MJ are ***zero***
  - ***No net current flows through the device***

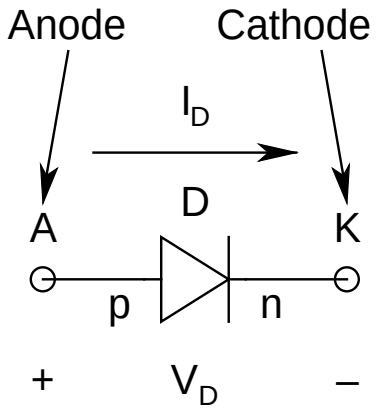
Diode Under Bias



Forward Bias:
p-side positive w.r.t. n-side



Reverse Bias:
n-side positive w.r.t. p-side



Symbol and current-voltage convention

Voltage and Current Conventions:
V_D: **0** (**Equilibrium**), **Positive** (**Forward Bias**), **Negative** (**Reverse Bias**)
I_D: **p to n** (**Positive**), **n to p** (**Negative**)

- ***Forward Bias*** (***V_D positive***):
  - ***p positive w.r.t. n***
  - ***Depletion region width*** $\downarrow$
  - ***Electric field across MJ*** $\downarrow$
    - ***Barrier height*** $(V_0 - V_D)\downarrow$
  - ***Injection of holes from p to n and electrons from n to p*** $\uparrow\uparrow$ (***thermionic emission***)
    - ***Diffusion component*** $\uparrow\uparrow$ ***while drift current remains more or less same***
  - ***Net current from p to n*** (***can be large***)
    - Known as ***forward current*** (***I_D positive***)

- ***Reverse Bias*** (***V_D negative***):
  - ***p negative w.r.t. n***
  - ***Depletion region width*** $\uparrow$
  - ***Electric field across MJ*** $\uparrow$
    - ***Barrier height*** $(V_0 + |V_D|) \uparrow$
  - ***Injection of holes from p to n and electrons from n to p*** $\downarrow\downarrow$ (known as ***carrier extraction***)
    - ***Diffusion component*** $\downarrow\downarrow$ ***while drift current remains more or less same***
  - ***Net current from n to p*** (***miniscule***!)
    - Known as ***reverse current*** (***I_D negative***)

More on Forward & Reverse Currents

- ***Injection of carriers***: Inj $\propto$ exp[– BH/V_T)
  - BH: ***Barrier Height***
  - V_T (= kT/q): ***Thermal Voltage*** [26 mV at room temperature (300 K)]
- ***Under equilibrium***:
  - Inj $\propto$ exp(–V_0/V_T)
  - ***Exactly balanced by the opposing drift component*** $\Rightarrow$ ***net current = 0***

- ***Under forward bias***:
  - ***BH reduces to*** $(V_0 - V_D)$
  - ***Inj that creates current flow*** $\propto \exp(V_D/V_T)$
  - Note the ***exponential dependence***
    - ***Possibility of large injection for large*** V_D
  - ***Drift component remains more or less same***, since it is ***dependent on the minority carriers***
  - ***Current increases exponentially with*** V_D
  - V_D ***can never equal or exceed*** V_0
    - ***Thermodynamically untenable situation***

- ***Under reverse bias***:
  - ***Inj↓↓ due to negative V_D***
  - ***Drift component remains same***
    - Function of ***minority carriers*** available on the two sides, which is a ***constant*** (***function only of temperature***)
  - ***Current becomes small and independent of bias***
- In ***forward bias***, ***both injection components*** create ***current from p to n***
- In ***reverse bias***, ***both minority carrier drift components*** create ***current from n to p***

Current-Voltage Characteristic

- $I_D = I_0[\exp(V_D/V_T) - 1]$
  - I_0: ***Reverse Saturation Current*** (~ nA-fA)
- In ***equilibrium***: $V_D = 0 \Rightarrow I_D = 0$
- Under ***forward bias***: ***V_D positive***
  - I_D ***positive*** (***flows from p to n***) (~ mA)
  - For $V_D > 4V_T$ (~ 100 mV at 300 K):
    - $I_D \approx I_0[\exp(V_D/V_T)]$ (***A True Exponent***)

- Under ***reverse bias***: ***V_D negative***
  - I_D ***negative*** (***flows from n to p***)
  - For $|V_D| > 4V_T$:
    - $I_D \approx -I_0$ (note the ***negative sign***)
    - ***Extremely small***, almost negligible
- ***Depending on V_D, the ratio of the forward current to the reverse current can range from 5 to 14 orders of magnitude***!
- ***Primary applications***:
  - ***Rectification*** and various types of ***waveshaping***

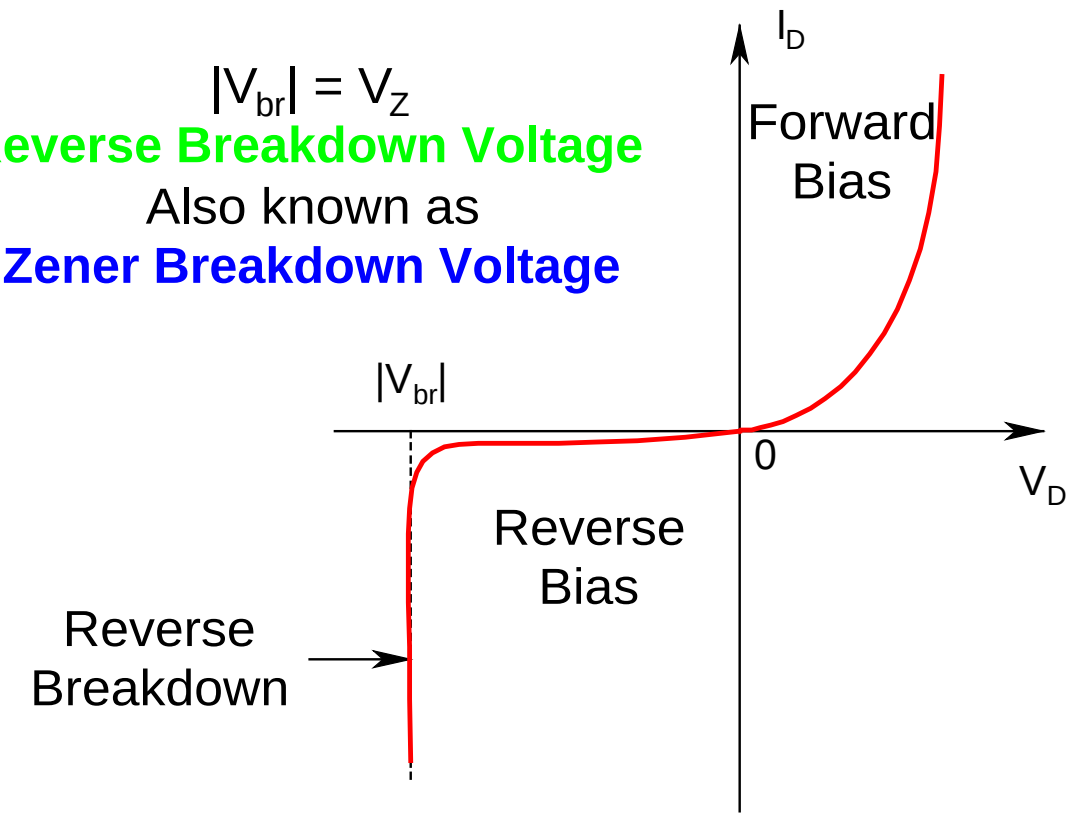
Complete I-V Characteristic

$|V_{br}| = V_Z$

Reverse Breakdown Voltage

Also known as

Zener Breakdown Voltage



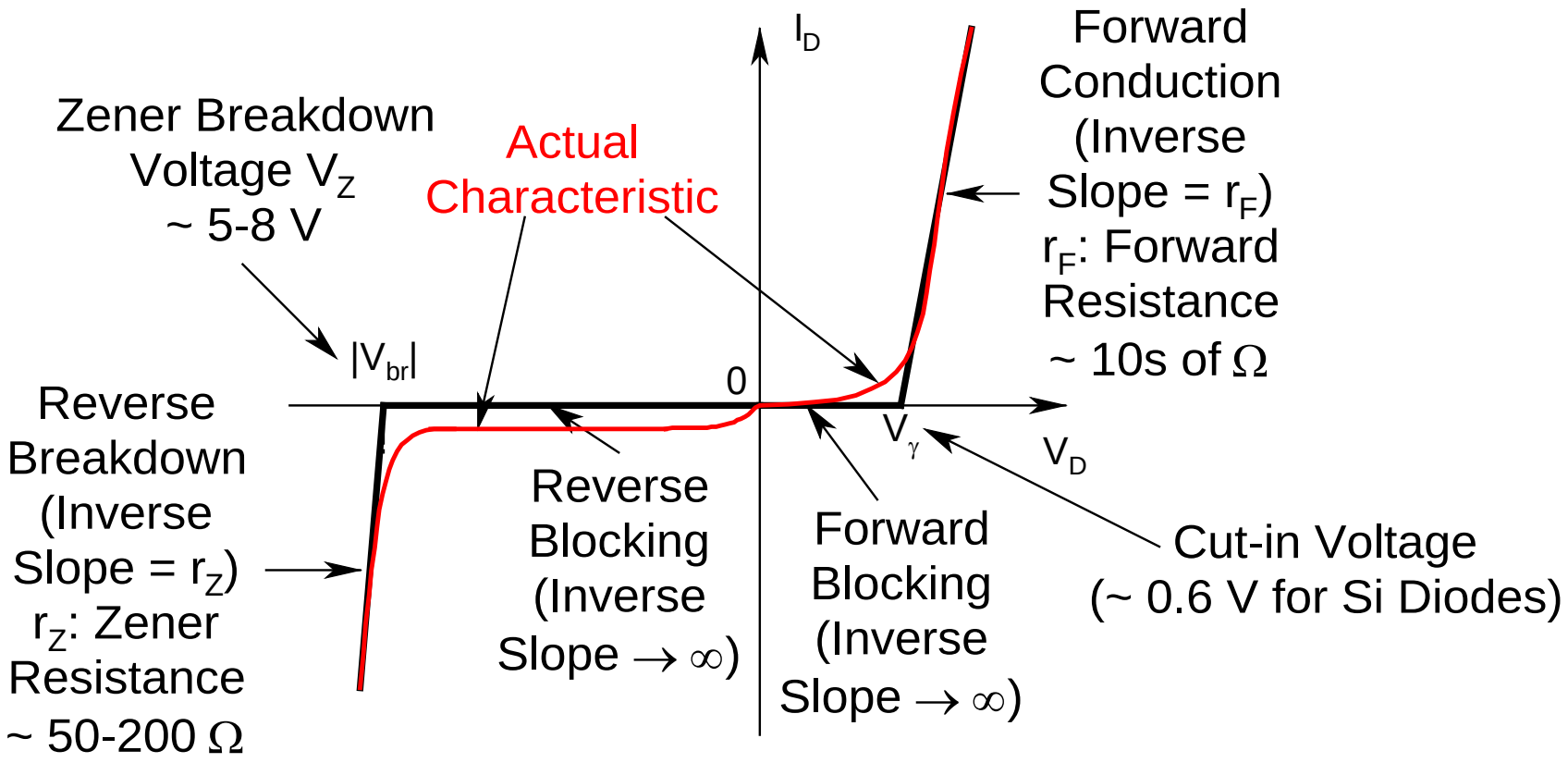
Note that the forward and reverse current scales are not same

Reverse Breakdown

- ***2 Mechanisms***:
  - ***Zener***
  - ***Avalanche***
- ***Zener***:
  - ***For junctions with both sides very heavily doped***
  - ***Thin depletion region***, through which carriers ***tunnel through*** (***quantum mechanical process***)
  - ***Typical $|V_{br}| < 3$ V***

- ***Avalanche***:
  - ***Classical breakdown process***
  - ***At least one side must be lightly doped***
  - ***Carrier multiplication*** due to ***impact ionization***
  - ***Typical $|V_{br}| > 5$ V***
- For diodes having $|V_{br}|$ ***in between 3 V and 5 V***, ***a combination of these two processes***
- ***Breakdowns*** are generally ***destructive***, unless the ***current*** is ***controlled*** by ***external means***, e.g., by a ***resistor***

Piece-Wise Linear (PWL) Model



Note: The forward and reverse current scales are not same

PWL Regions

- $0 \leq V_D \leq V_\gamma$: ***Forward Blocking***
  - V_γ: ***Cut-in Voltage*** (~ ***0.6 V for Si diodes***)
  - $I_D = 0$
- $V_D \geq V_\gamma$: ***Forward Conduction***
  - I_D ***increases linearly with*** V_D with an ***inverse slope of*** r_F
  - r_F: ***Diode Forward Resistance*** (~ 10s of Ω)
    $= [dI_D/dV_D]^{-1}$

- Diodes under ***forward bias*** and for $V_D \geq V_\gamma$, offer ***small resistance*** (results from the ***exponential*** I-V characteristic)
- V_D negative and $0 \leq |V_D| \leq |V_{br}|$: ***Reverse Blocking***
  - $I_D = 0$
- V_D negative and $|V_D| \geq |V_{br}|$: ***Reverse Breakdown***
  - $|I_D|$ ***increases linearly with*** $|V_D|$ with an ***inverse slope of*** r_Z

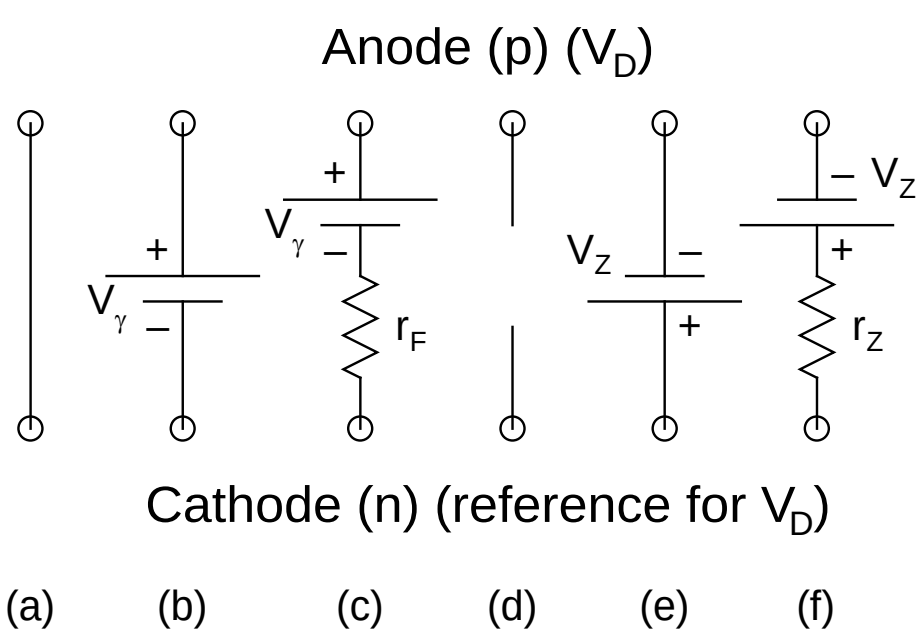
- r_Z: ***Zener Resistance*** (~ 50-200 Ω)
  $= [d|I_D|/d|V_D|]^{-1}$

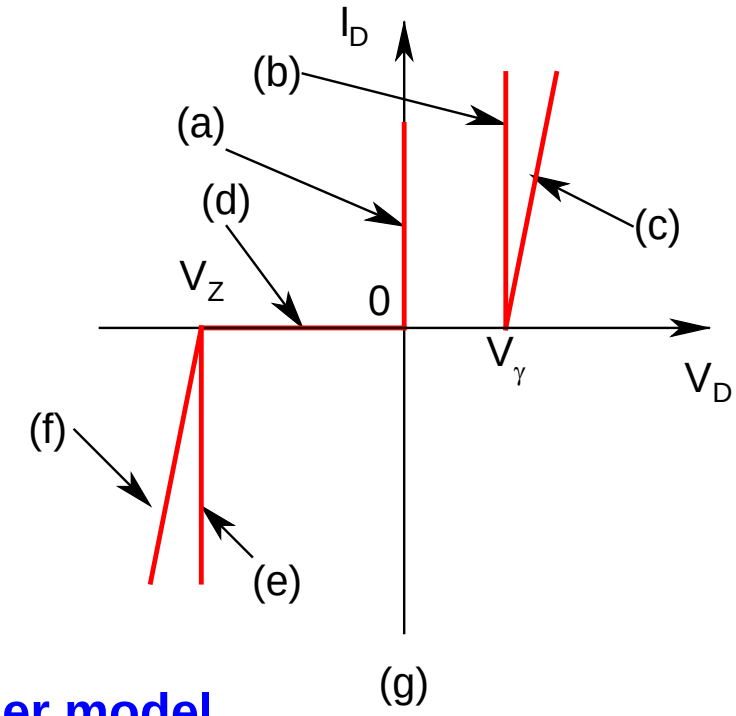
- Diodes under ***reverse bias*** and for $|V_D| \geq |V_{br}|$, offer ***small resistance***

  $\Rightarrow$ ***If current is not controlled by external means, then it may damage the device completely***

- Generally, diodes, unless they are to be operated in ***breakdown mode***, e.g., in a ***voltage regulator***, have ***very high*** $|V_{br}|$, typically of the order of ***100s of V***

PWL Circuit Models

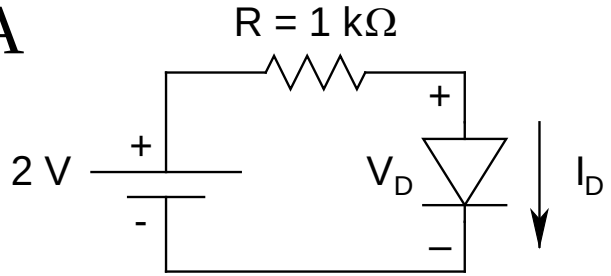




Forward Bias : **V_D positive**: (a) **0^{th} order model**, (b) **1^{st} order model**, (c) **2^{nd} order model**, **Reverse Bias** : **V_D negative**: (d) **0^{th} order model**, **Breakdown** : (e) **1^{st} order model**, (f) **2^{nd} order model** (g) **Corresponding piecewise linear models**

0^{th}-Order Model: **Ideal Diode**

- Ex.: Find I_D and V_D, using: i) 0^{th} order, ii) 1^{st} order, and 2^{nd} order diode models. [V_γ = 0.6 V, $r_F = 50\ \Omega$]



i) ***0th order model***: $I_D = 2/(1\ \text{k}\Omega) = 2\ \text{mA}$

$V_D = 0\ \text{V}$

ii) ***1st order model***:

$I_D = (2-0.6)/(1\ \text{k}\Omega) = 1.4\ \text{mA}$ and $V_D = 0.6\ \text{V}$

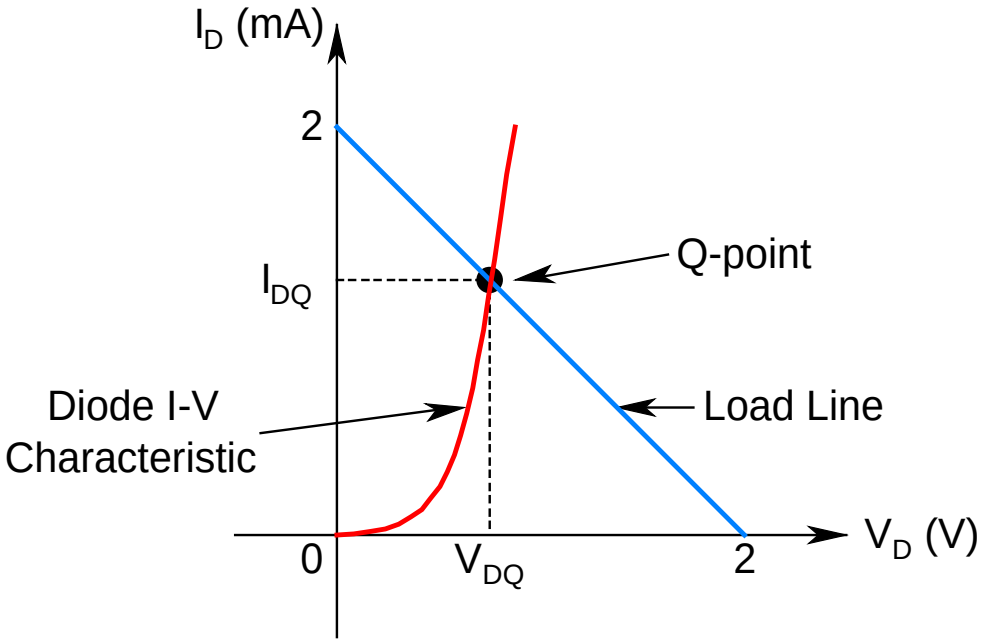
iii) ***2nd order model***:

$I_D = (2-0.6)/(1\ \text{k}\Omega + 50\ \Omega) = 1.33\ \text{mA}$

$V_D = V_\gamma + I_D r_F = 0.667\ \text{V}$

Finding the DC Operating Point

- Known as the ***Q-point*** (***quiescent point***)
- ***Defined by (I_D, V_D)***
- ***Two solution techniques***:
  - ***Graphical Method*** (***Using Load Line***)
  - ***Iterative Method*** (***Self-Consistent***)
- ***Graphical Method***:
  - ***Use diode I-V relation***: $I_D = I_0 \exp(V_D/V_T)$
  - ***Use Load Line equation***: $I_D = (2 - V_D)/(1\ \text{k}\Omega)$
  - ***Intersection point is the operating point***



Graphical Method

V_{DQ}, I_{DQ}: Quiescent values of V_D, I_D = 0.7 V, 1.3 mA (obtained from iterative method using I_0 = 3 fA)

DC Quiescent Power Dissipation = $V_{DQ} \times I_{DQ}$ = 0.9 mW

The two ***end points*** of the ***load line***:

1. $V_D = 0$: $I_D = 2/(1\text{ k}) = 2$ mA
2. $I_D = 0$: $V_D = 2$ V

- ***Iterative Method***:
  - Also known as ***self-consistent analysis***
  - ***I-V relation*** and ***load line equation*** form a set of ***transcendental equations***
    - ***Analytical solution not possible***
    - Have to resort to ***numerical*** (***iterative***) analysis
  - ***Procedure***:
    - ***Choose V_D = 0.7 V*** and ***find I_D*** from ***load line equation***
    - ***Use this I_D*** to ***find V_D*** from ***I-V relation*** (***convert to ln form first***)
    - ***Repeat till convergence is achieved*** (pretty quick!)

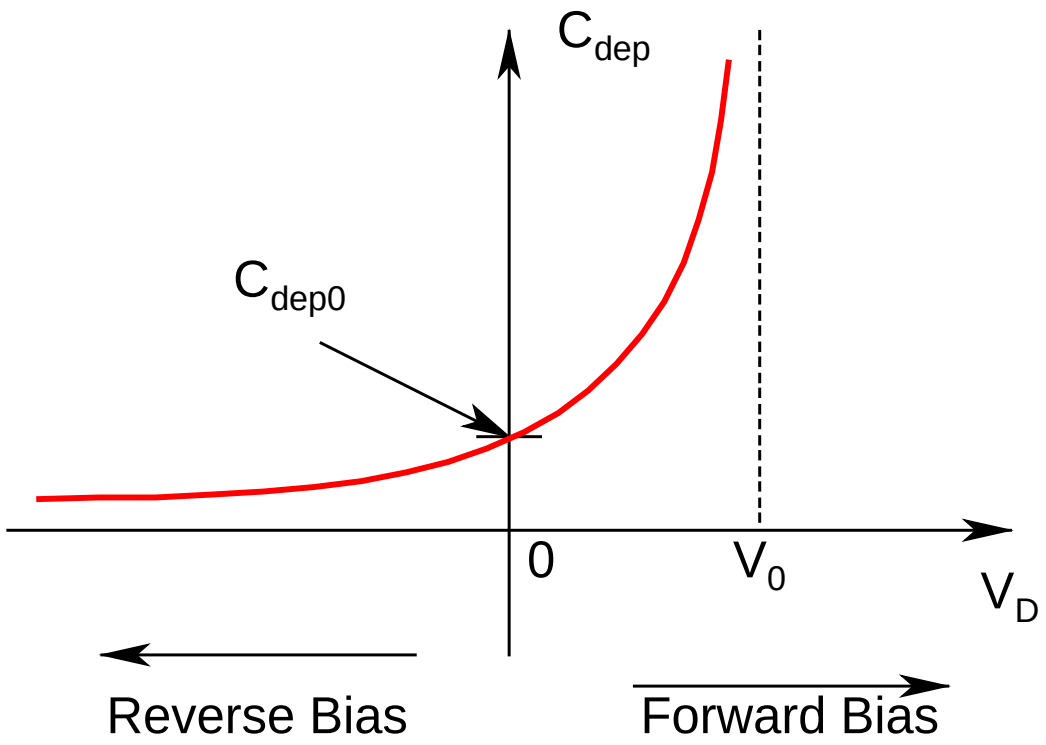
Series Resistance Effect

- The two ***quasi-neutral regions*** (p and n) have their own ***bulk resistances***
- ***Denoted as r_p and r_n***
- ***For small I_D***, their ***effects are negligible***
- However, ***for large I_D***, the ***potential dropped*** across them ***reduces*** the ***actual voltage*** appearing across the ***junction*** of the diode
- Known as the ***Series Resistance Effect***

- The ***actual voltage*** appearing across the ***junction***:
  - $V_{D,eff} = V_D - I_D(r_p + r_n)$
  - V_D: ***Diode terminal voltage***
- The ***new diode I-V relation***:
  - $I_D = I_0 \exp(V_{D,eff}/V_T)$
- ***Simultaneous solution*** of the above ***two equations*** would yield the ***Q-point***
- ***In presence of r_p and r_n, V_D may exceed V_0,*** but ***$V_{D,eff}$ would always be less than V_0***

Diode Capacitances

- ***Two components***:
  - ***Depletion Capacitance*** C_{dep}
  - ***Diffusion Capacitance*** C_{diff}
- ***Depletion Capacitance***:
  - Due to ***depletion charge dipole*** across the ***junction***
  - ***Expressed by***: $C_{dep} = C_{dep0}/(1 - V_D/V_0)^{1/2}$
    - $C_{dep0} = C_{dep}$ for $V_D = 0$
  - ***Present under both forward and reverse bias***



* C_{dep} diverges as $V_D \rightarrow V_0$

* C_{dep} in reverse bias < C_{dep} in forward bias

* **Rule of Thumb**: C_{dep} in forward bias $\approx 2C_{dep0}$

- ***Diffusion Capacitance***:
  - Due to ***charge injection*** in ***both sides of the junction*** (in the ***quasi-neutral regions***)
  - ***Expressed by***: $C_{diff} = I_D\tau/V_T$
    - τ: ***Injected carrier lifetime***
  - ***Present only in forward bias***, ***negligible in reverse bias***
  - ***Much larger than C_{dep}***
- ***Total Diode Capacitance*** C_D:
  - $C_D = C_{dep} + C_{diff}$

Small-Signal Model

- ***Needed for ac analysis***
- ***Electrical equivalent*** at the ***DC bias point***
- Represented as a ***network***, having various ***circuit components*** (***resistors***, ***capacitors***, ***current sources***, etc.)
- Also known as ***incremental model***
- ***Evaluated at (I_{DQ},V_{DQ})***
- Appropriate for ***small variations*** of the ***ac signal*** around the ***Q-point***

Small-Signal Model Parameters

- ***Diode Resistance*** (r_D)/***Diode Conductance*** (g_D):

$$r_D = (g_D)^{-1} = \left(\frac{\partial I_D}{\partial V_D} \right)^{-1} \Bigg|_{I_D = I_{DQ}} = \frac{V_T}{I_{DQ}}$$

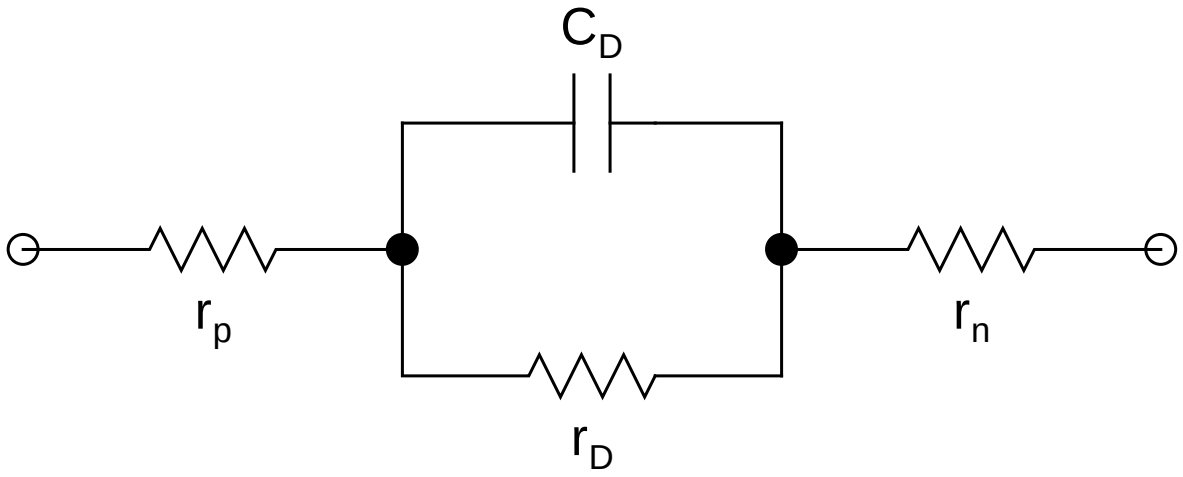
  - For I_{DQ} = 1 mA, r_D = 26 Ω
  - ***Under forward bias***, diode offers ***very small resistance***

- ***Diode Capacitance*** (C_D):
  - $C_D = C_{dep} + C_{diff}$

    $= C_{dep0}/(1 - V_D/V_0)^m + \tau/r_D$
    - m: ***Grading coefficient***

      (1/2 for ***abrupt step junction***, 1/3 for ***linearly graded junction)***
- ***Both r_D and C_D appear in parallel across the junction***
- ***The two quasi-neutral resistance r_p and r_n appear in series with this combination***

Small-Signal Equivalent



- ***In absence of r_p and r_n***, it's just a ***parallel RC circuit***, and ***shorts out*** at ***high frequency***
  - ***Diode time constant*** $\tau_D = r_D C_D = \tau$