• Simple NMOS CM:

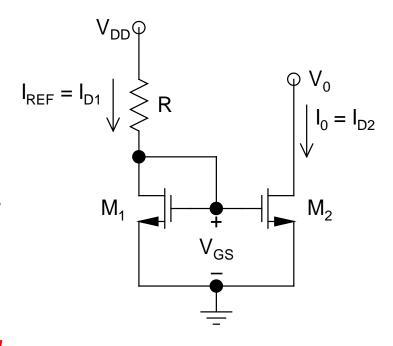
- \triangleright $V_{GS1} = V_{GS2} = V_{GS}$
- \triangleright M₁ has its *D* and *G*

shorted
$$\Rightarrow$$
 $V_{GD1} = 0$

- \Rightarrow always in saturation, since $V_{DS1} > V_{GT1}$
- \Rightarrow Known as *diode-*

connected MOSFET

 \triangleright Even though $I_G = 0$, the analysis is slightly more cumbersome than simple BJT CM



- ➤ In general, for NMOS (PMOS), the B terminal is always connected to the most negative (positive) potential available in the circuit to ensure that SB and DB junctions never get forward biased
- ► Both M_1 and M_2 have their B terminals grounded $\Rightarrow V_{SB1} = V_{SB2} = 0$
 - $V_{TN1} = V_{TN01}$ and $V_{TN2} = V_{TN02}$
- > Thus:

$$I_{REF} = I_{D1} = \frac{k'_{N1}}{2} \left(\frac{W}{L}\right)_{1} (V_{GS} - V_{TN01})^{2}$$

- For a given V_{DD} and R, the equation has 2 unknowns: I_{D1} and V_{GS}
- ➤ Need *another equation* for *unique solution*, which is the *load line equation*:

$$I_{D1} = (V_{DD} - V_{GS})/R$$

- \gt Simultaneous solution of these two equations would give a unique solution for I_{D1} and V_{GS}
 - Caution: 2 roots, out of which, one will be unphysical
- So far, we have *neglected CLM*, which we would include soon!

> Now:

$$V_{GS} = V_{TN01} + \sqrt{\frac{2I_{REF}}{k'_{N1}(W/L)_{1}}} = V_{TN02} + \sqrt{\frac{2I_{0}}{k'_{N2}(W/L)_{2}}}$$

> Thus:

$$I_{0} = \frac{k'_{N2} (W/L)_{2}}{2} \left[(V_{TN01} - V_{TN02}) + \sqrt{\frac{2I_{REF}}{k'_{N1} (W/L)_{1}}} \right]^{2}$$

This is the *exact expression* of I₀, *without* making any assumptions/approximations whatsoever

Now, if $V_{TN01} = V_{TN02} = V_{TN0}$, and $k'_{N1} = k'_{N2} = k'_{N}$:

$$I_0 = \frac{\left(W/L\right)_2}{\left(W/L\right)_1} I_{REF}$$

- ➤ Very similar to BJT CM, but with a big exception:
 - In BJT CM, this ratio could only be an integer
 - In MOS CM, no such restriction exists: $(W/L)_2$ can be >, =, or < $(W/L)_1$ ⇒ any arbitrary current ratio can be obtained

- Finally, if $(W/L)_2 = (W/L)_1$: $I_0 = I_{REF} \Rightarrow Current Mirror!$
- Two MOSFETs are deemed to constitute a *matched pair*, if they have *same* V_{TN0} , γ , ϕ_F , λ , and k'_N
 - Note that all of these are process parameters
 - (W/L) is NOT a process parameter, since it's under designer's control
 - If (W/L)s are also same, then the pair is known as perfectly matched