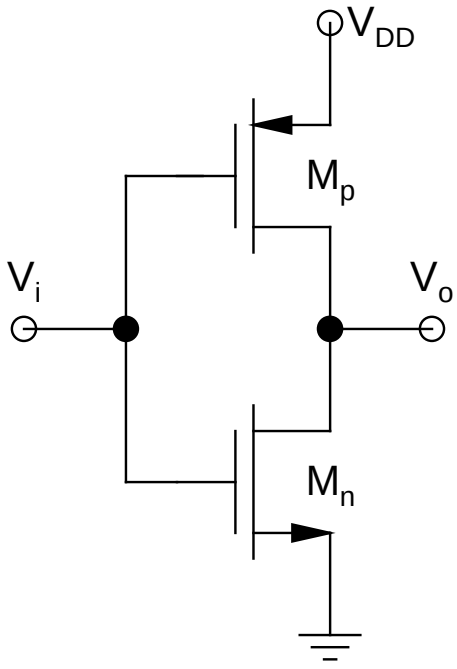
- ***A Better CMOS Gain Stage***:
  - ***No body effect issue***
  - However, there are ***some design issues***
  - M_n-M_p have ***same magnitude*** of the ***threshold voltage***:

    $V_{TN0} = |V_{TP0}|$
  - ***Process transconductance parameters***:

    $k'_N = \mu_n C'_{ox}$ and $k'_P = \mu_p C'_{ox}$



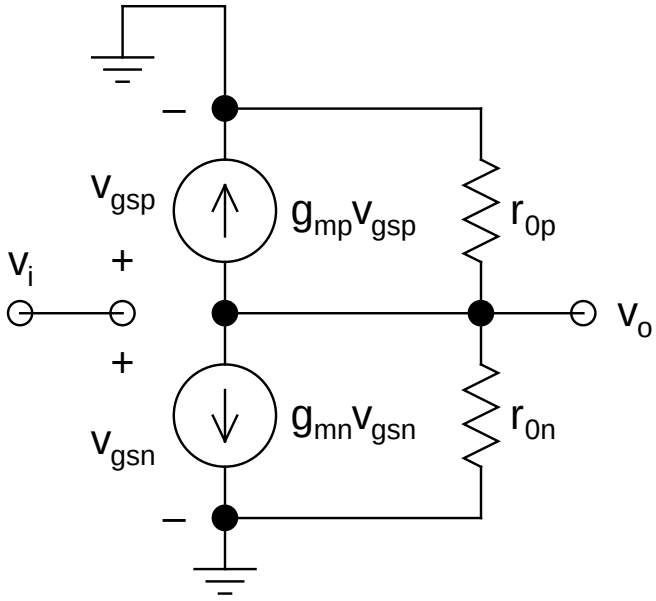
Circuit Schematic

- ***Oxide capacitance per unit area*** $\left(C'_{ox} = \varepsilon_{ox} / t_{ox}\right)$ ***same for both devices***, since they have ***same*** t_{ox}
- However, $\mu_n \sim 2\mu_p$ (***for Si***)
- Thus, $k'_N = 2k'_P$
- ***Ideal DC bias point*** of the circuit is $V_I = V_0 = V_{DD}/2$ (yields $V_{GSn} = |V_{GSp}|$ and $V_{DSn} = |V_{DSp}|$)
- Can be achieved only if the stage is ***completely balanced*** (***same threshold voltage magnitude*** and ***same device transconductance parameter***)
- Thus, k_N ***and*** k_P ***need to be matched***

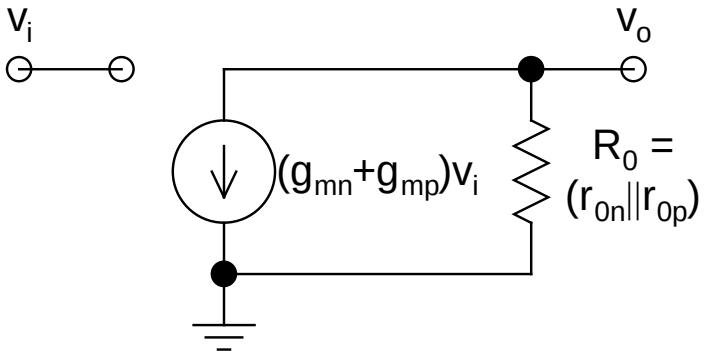
- ***Can be achieved by making $(W/L)_p = 2(W/L)_n$***
- If ***CLM effect*** is ***not that important***, or if $\lambda_n = \lambda_p$, then this procedure works out ***just fine***
- However, if $\lambda_n \neq \lambda_p$, then for ***balancing the circuit***, the following relation ***must hold*** (***show***!):

  $k_P(1 + \lambda_p V_{DD}/2) = k_N(1 + \lambda_n V_{DD}/2)$
- Under this condition, $k_N \neq k_P$, but the circuit will be ***perfectly matched and balanced***
- Known as: ***Stage unmatched by nature, but matched by performance***

➢ *ac Analysis*:



ac Midband Equivalent



Simplified Equivalent

- ***By inspection***:

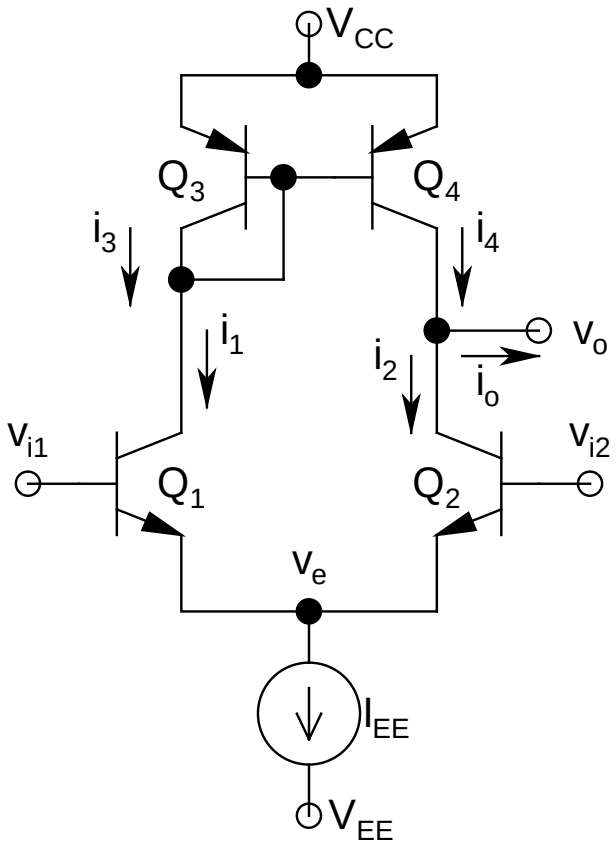
  $A_v = -(g_{mn} + g_{mp})R_0$

  $= -(g_{mn} + g_{mp})/(g_{0n} + g_{0p})$

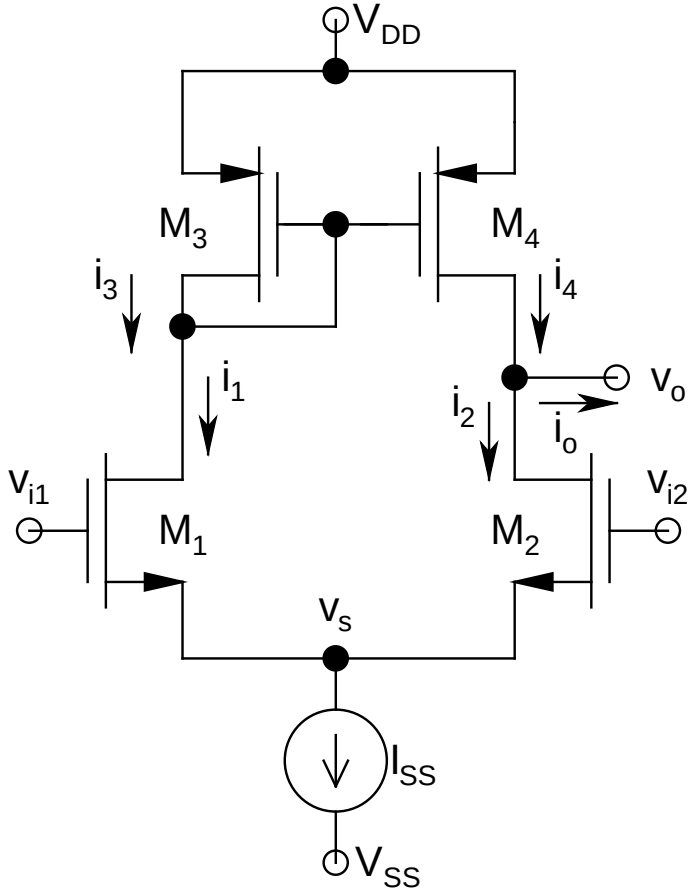
  $R_0 = r_{0n} || r_{0p} = (g_{0n} + g_{0p})^{-1}$

- ***Very high A_v and R_0***
- ***Extremely popular*** and ***widely used circuit***
- Sometimes, ***level shifters*** are used at the ***input*** for ***better ease*** of application

- ***Actively Loaded DA***:



BJT Implementation



MOS Implementation