Department of Electrical Engineering
Indian Institute of Technology, Kanpur

EE 210 **Assignment #7** **Assigned: 17.2.21**

1. Perform an exact ac small-signal low-frequency analysis of the equivalent circuit for an npn cascode current source, as given in class, and show that the actual output resistance of this circuit is half of that given in class.

2. Calculate the output resistance and the equivalent open-circuit voltage of an NMOS cascode current source, as given in class, assuming that I_{REF} = 100 μA, and for all devices, the dimensions are 100 μm/8 μm, and dX_d/dV_{DS} = 0.1 μm/V.

3. It was stated in class that in bipolar topology, double cascode configuration does not provide for any improvement in the output resistance, as compared to a single cascode. Justify this statement, using an ac small-signal low-frequency equivalent of a double cascode stage using npn transistors.

4. In the design of an npn Widlar current source, as given in class, in order to produce a specified output current, two resistors must be selected. Resistor R_1 sets I_{REF}, and the emitter resistor R_2 sets I_0. Assuming a supply voltage of V_{CC} and a desired output current I_0, determine the values of the two resistors so that the total resistance in the circuit is minimized. Your answer should be given as expressions for R_1 and R_2 in terms of V_{CC} and I_0. What values would these expressions give for V_{CC} = 30 V and I_0 = 5 μA? Are these values practical?

5. Show that for a V_D-multiplier circuit, as given in class, if the base current cannot be neglected, then the expression for the output voltage V_0 can be given as

$$V_0 = \left(1 + \frac{R_1}{R_2}\right) V_D + \frac{R_1}{(\beta + 1) R_2} \left(I_{REF} R_2 - V_D\right)$$

   Note that if the base current is neglected (which amounts to assuming that $\beta \to \infty$), then the second term in the above expression vanishes, and it simplifies to the form given in class. Hence, compute the values of V_0 for β = 10, 50, 100, 200, and 250, with R_1 = 9 kΩ, R_2 = 1 kΩ, I_{REF} = 1 mA, and V_D = 0.7 V. Note how closely V_0 approaches the first term for large β.

6. Design an NMOS voltage reference, as given in class, to provide voltage references of 1.5 V, 3 V, and 4.5 V, choosing either i) M_1 or ii) M_4 to have the minimum area. Show that both the designs produce almost identical values of total device area, however, one of them consume much lower dc power than the other (which one? why?). Assume V_{DD} = 6 V, MFS = 1 μm, k'_N = 40 μA/V^2, V_{TN0} = 0.7 V, γ = 0.4 V$^{1/2}$, λ = 0.1 V^{-1}, $2\phi_F$ = 0.6 V, and all transistors have their bodies connected to ground.