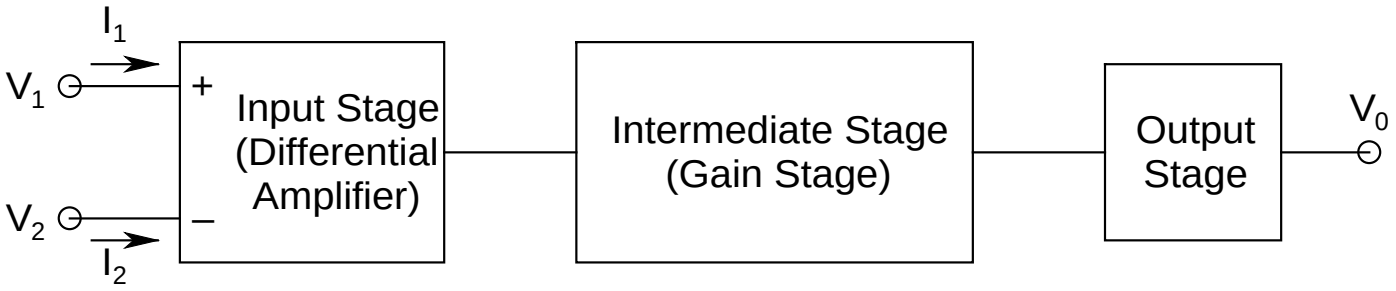
THE OPERATIONAL AMPLIFIER (OP-AMP)

- ***The Ultimate***: A ***phenomenal application*** of everything that we have learnt so far in this course
- ***Op-Amp***: ***Operational Amplifier***
- ***Hugely powerful block***
- ***Capable of performing various circuit functions***
- ***Original inventor***: ***George Philbrick*** of ***Bell Labs*** in ***1952*** using ***vacuum tube technology***

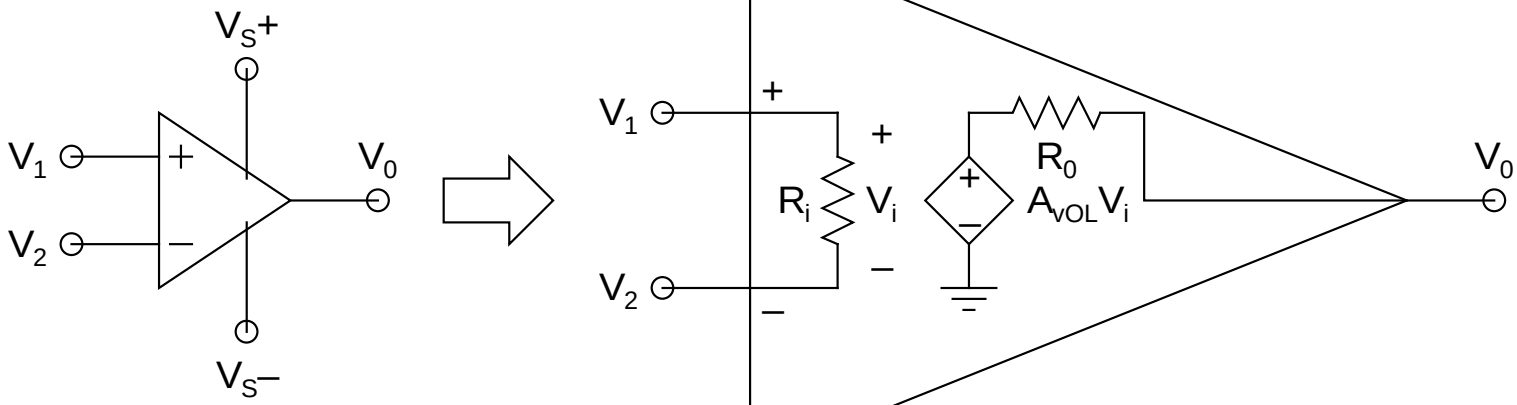
- ***Remarkable innovations*** in ***design*** in the form of an ***IC*** by ***Bob Widlar*** of ***Fairchild Semiconductors*** in ***1963***
- After that, ***several improvements*** took place, and the ***most versatile design***, widely came to be known as the ***741 op-amp***, originated
- Basically a ***three-stage architecture***:
  - ***The Input Stage***
  - ***The Gain Stage***
  - ***The Output Stage***

- ***The Input Stage*:**
  - ***Should be capable of double-ended to single-ended conversion***
  - ***Should have moderate to high gain***
  - ***Must definitely have extremely large CMRR (this is the main requirement)***
  - ***Almost invariably a Differential Amplifier (DA)***

- ***The Gain Stage***:
  - ***Can be any one of the many that we have studied in the chapter on Amplifiers***
  - ***CC-CE Darlington configuration preferred***
  - ***Should have moderate to large gain***
- ***The Output Stage***:
  - ***Needed when the op-amp is expected to either source or sink large amount of current to or from the load***



Basic Three-Stage Architecture of an Op-Amp



Symbol

MacroModel

- ***2 Input Terminals***:
  - V_1 (***non-inverting*** [+])
  - V_2 (***inverting*** [–])
- ***1 Output Terminal***: V_0
- V_1, V_2, and V_0 can be ***simply DC***, or ***simply ac,*** or a ***combination of both***
- I_1, I_2: ***Input currents flowing into the + and – terminals respectively***
- ***Dual symmetric power supplies*** (***V_S+ and V_S–***)

- Refer to the ***MacroModel***:
  - R_i: ***Input Resistance***
    - ***Very high*** (***ideally infinite***)
  - R_0: ***Output Resistance***
    - ***Very small*** (***ideally zero***)
  - A_{vOL}: ***Open-Loop Gain***
    - ***Very large*** (***ideally infinite***)
- ***Input-Output Relation***:

$$V_0 = A_{vOL}(V_1 - V_2)$$

- V_1, V_2, and V_0 are measured ***w.r.t. ground***, but V_i is a ***floating signal*** (***difference*** between V_1 and V_2)
- The ***controlled source*** in the ***MacroModel*** is ***VCVS***
- For $V_1 > (<) V_2$, V_0 is ***positive*** (***negative***)
- ***Typical values for 741 op-amp***:
  - $A_{vOL} \sim 10^5$ (***100 dB***), $R_i >$ ***1 MΩ***, $R_0 <$ ***100 Ω***, CMRR ~ ***80-100 dB***, V_S+ and V_S–: ***±3 V to ±15 V***

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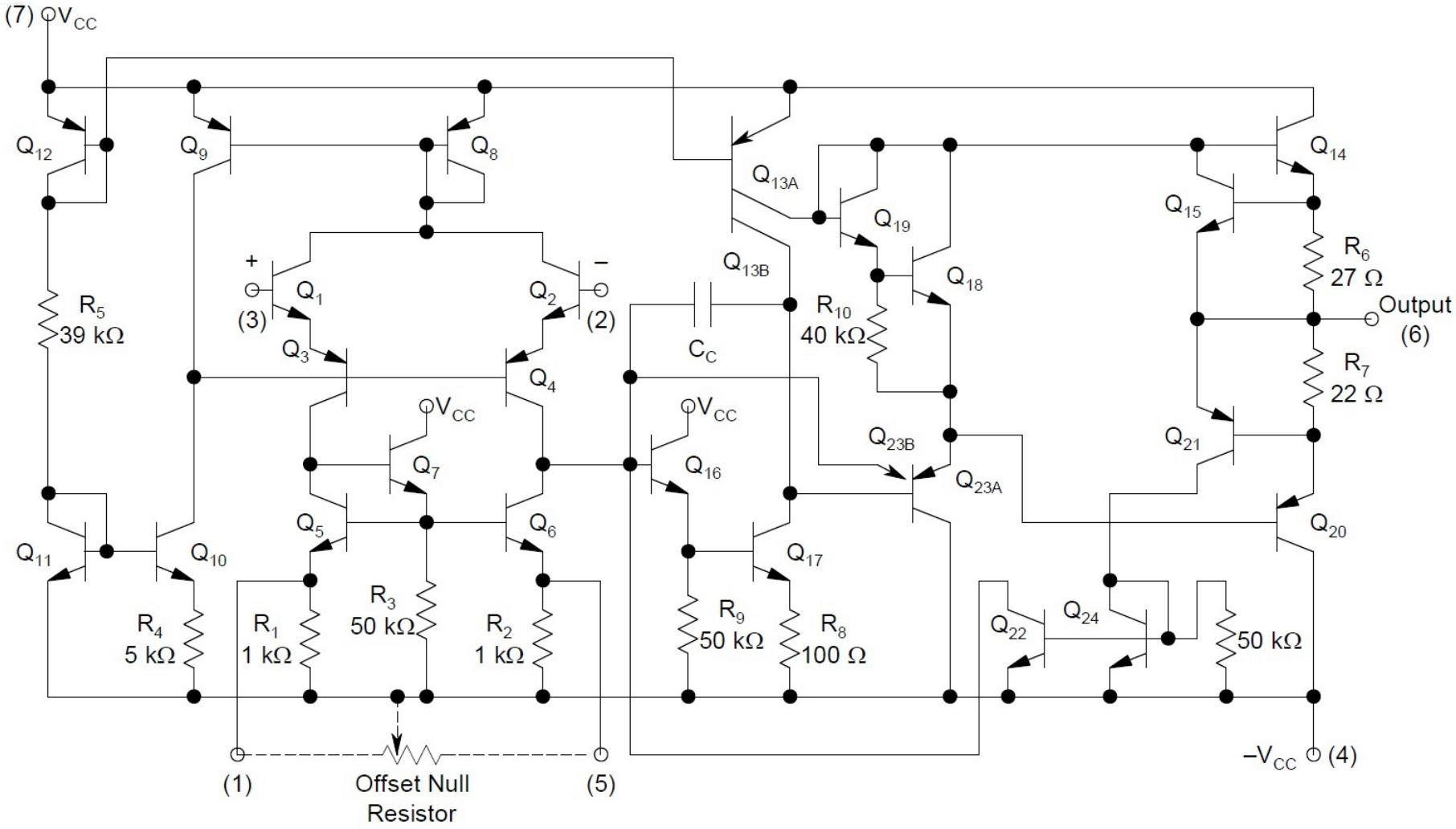
- ***Uncompensated bandwidth*** typically ***larger than 1 MHz***
- Such a ***large gain*** and ***high bandwidth*** system will be prone to ***oscillations*** (***instability***)
- Need adequate ***compensation***
  - ***Compensated bandwidth*** drops to about ***5-10 Hz***

- ***History of 741 Op-Amp***:
  - In ***1965***, ***Bob Widlar*** (remember ***Widlar current source***?) of ***Fairchild Semiconductors*** (now defunct) first came up with the design of a ***monolithic*** (***single substrate IC***) ***op-amp***

- Named it ***μA 709*** (***μA*** was the ***trademark*** of ***Fairchild Semiconductors***)
- Almost immediately thereafter, ***a number of improvements*** were made on the ***original architecture***, and ***μA 741*** evolved
- It became so ***popular*** that ***the term 741*** became a ***legend***
- ***All subsequent op-amp designs continued to be called 741***!
- ***Initial design*** of course was based on ***bipolar technology***, since at that time, ***MOSFETs were not even there***!

- In ***late 70s***, ***JFET version*** of op-amps came into existence, followed by the ***MOSFET version*** in the ***80s***
- The ***design pedagogy*** of the ***original version*** is a ***real beauty***
- So many ***brilliant innovations*** were ***incorporated*** in the ***design***, that it is a ***learner's paradise***!
- In this chapter, we will do a ***detailed analysis*** of the ***bipolar version*** of the ***741 op-amp***
- So, sit tight and enjoy! :)



The schematic of the 741 bipolar op-amp (the pin numbers of the 741 chip is shown in parantheses).

- ***Steps of the Analysis***:
  - First, we need to do the ***DC analysis***
  - For this, we need to find the ***reference branch***
  - This branch should be from ***rail-to-rail*** (i.e., ***between the two power supplies***)
  - It should encounter only ***base-emitter junctions*** and ***resistors***

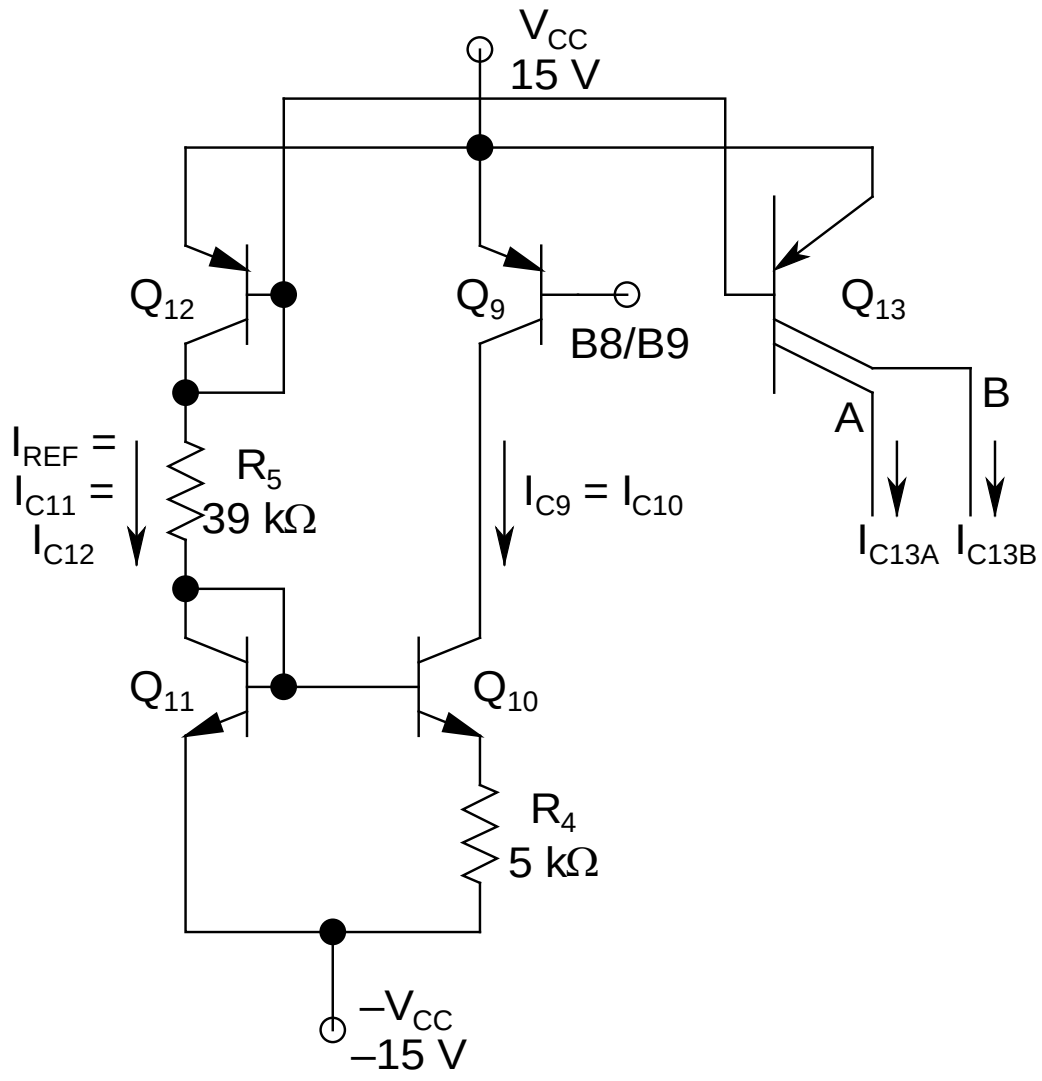
    $\Rightarrow$ The branch Q_{11}-Q_{12}-R_5 is our ***reference branch***
  - ***The DC current flowing through this branch fixes the DC bias current of all other branches***

- Next is ***identification of modules***
- Q_{10}-Q_{11}-R_4 can be identified as the ***Widlar current source***
- Current through Q_{10} is ***same*** as that of Q_9, which forms a ***mirror configuration*** with Q_8
- Current through Q_8 ***biases the DA***, which is the ***combination*** of Q_1-Q_4
- Q_5-Q_6-R_1-R_2 ***combination*** can be identified as a ***ratioed mirror*** with the ***keep-alive resistor*** R_3 and the ***base current boost*** provided by Q_7

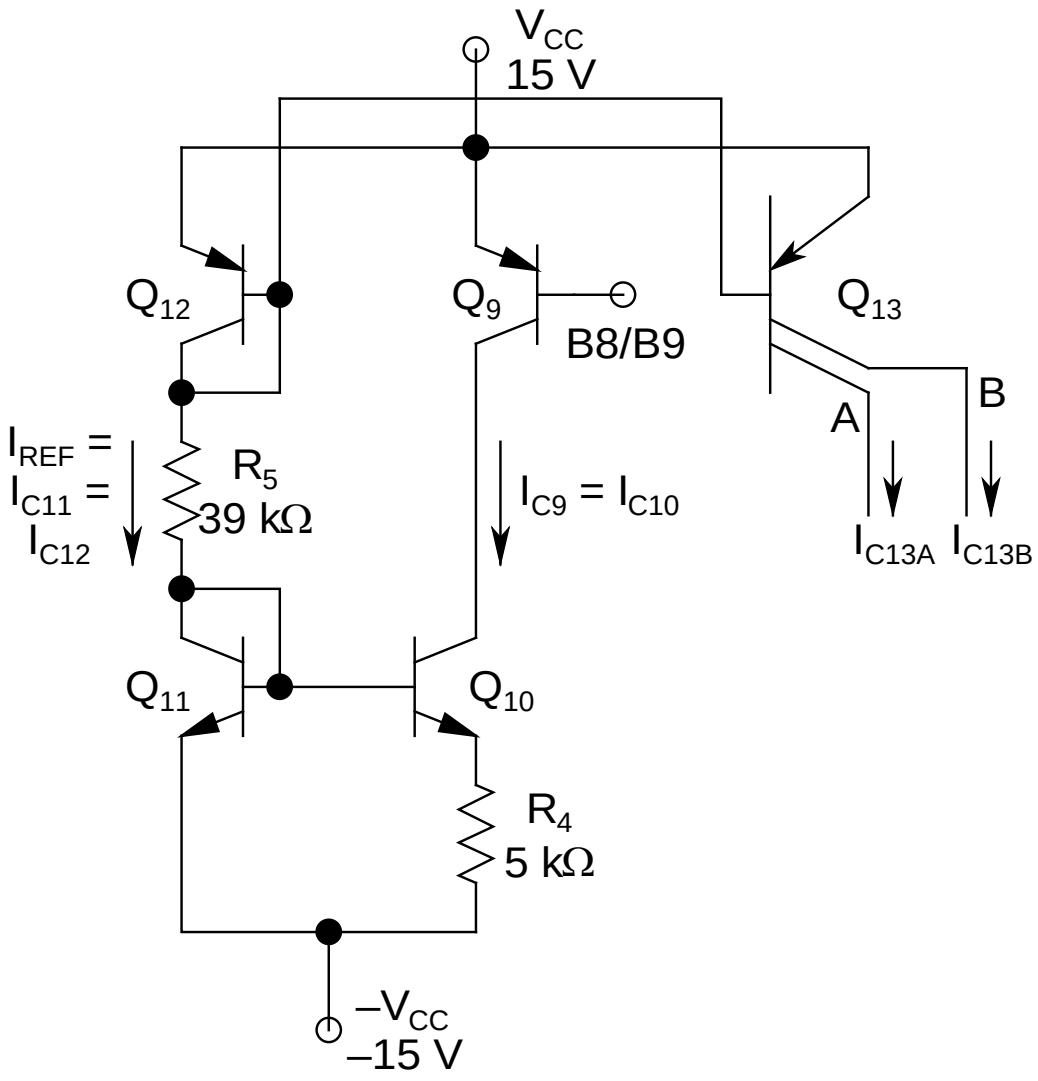
- ***Output of the DA*** is fed to Q_{16}-Q_{17}-R_8-R_9 combination, which is a ***CC-CE Darlington***, and acts as the ***gain stage***
- The ***output of the gain stage*** is fed to the ***Class-AB output stage***, consisting of:
  - Q_{14} and Q_{20}: ***Complementary output transistors***
  - Q_{18}-Q_{19}-R_{10}: ***Prebias circuit for the output stage***
  - Q_{15}-Q_{21}-R_6-R_7: ***Short-circuit protection circuit***
- Q_{13}, Q_{22}-Q_{24}, and the unnumbered 50 kΩ resistor have ***special roles***, which we will discuss about later

- ***DC Analysis***:
  - ***Assumptions***:
    - ***Neglect base current and Early effect***
    - ***Both + and – input terminals grounded***
      - ***Recall that is is the most preferred DC biasing arrangement for DAs***
    - Q_1-Q_2, Q_3-Q_4, Q_8-Q_9, and Q_{10}-Q_{11} ***perfectly matched***
    - ***±15 V power supply***
  - ***Reference branch*** (Q_{11}-Q_{12}-R_5) ***current***:

$$I_{REF} = I_{C11} = I_{C12} = [V_{CC} - V_{EB12} - V_{BE11} - (-V_{CC})]/R_5 = 733.3\ \mu A$$



DC Biasing of the Main Branches



DC Biasing of the Main Branches

- Q_{10}-Q_{11}-R_4 ***combination*** is a ***Widlar current source***:

  $\Rightarrow V_T \ln(I_{REF}/I_{C10}) = I_{C10}R_4$

  $\Rightarrow I_{C10} = (V_T/R_4)\ln(I_{REF}/I_{C10})$

  Solution of this ***transcendental equation***:

  $I_{C10} = 19\ \mu A = I_{C9}$

- Q_{12}-Q_{13} another ***mirror***:

  $\Rightarrow I_{C13} = I_{C12} = I_{REF} = 733.3\ \mu A$

- Q_{13} is a ***special transistor***, having ***split collectors*** (A and B), with their ***area ratios*** 1:3

  $\Rightarrow I_{C13A} = 183.3\ \mu A$ and $I_{C13B} = 550\ \mu A$

➢ *DC Biasing of the Input Stage*:

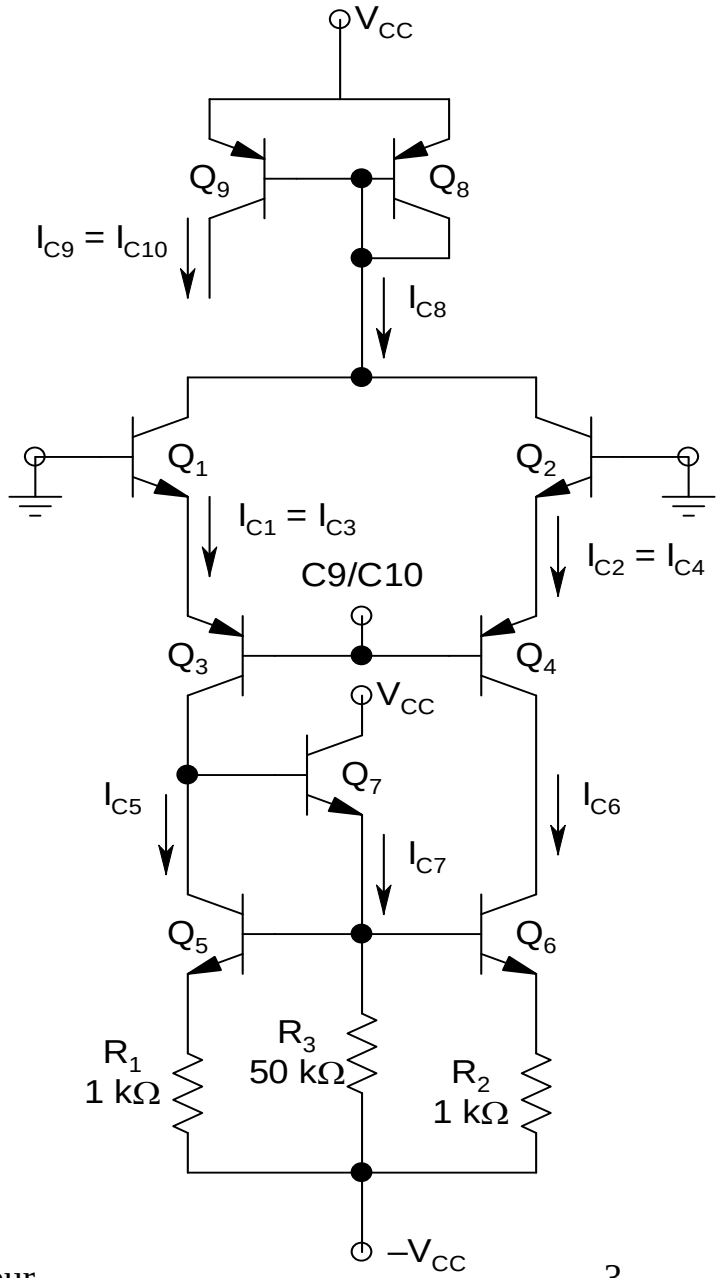
- Q_8-Q_9 form a ***current mirror***:

  $\Rightarrow I_{C8} = I_{C9} = I_{C10} = 19\ \mu A$

- This is the ***bias current*** for the ***DA***:

  $\Rightarrow I_{C1} = I_{C2} = I_{C3} = I_{C4}$
  $= I_{C5} = I_{C6} = I_{C8}/2$
  $= 9.5\ \mu A$

  $I_{C5} = I_{C6}$ (***since $R_1 = R_2$***)



- ***Calculation*** of I_{C7} little more ***involved***
  - ***Neglecting base currents***, $I_{C7} \approx I_{R3}$
  - Assuming $I_{S5} = 1$ fA:

    $V_{BE5} = V_T \ln(I_{C5}/I_{S5}) = 597.3$ mV
  - The ***drop*** across R_3:

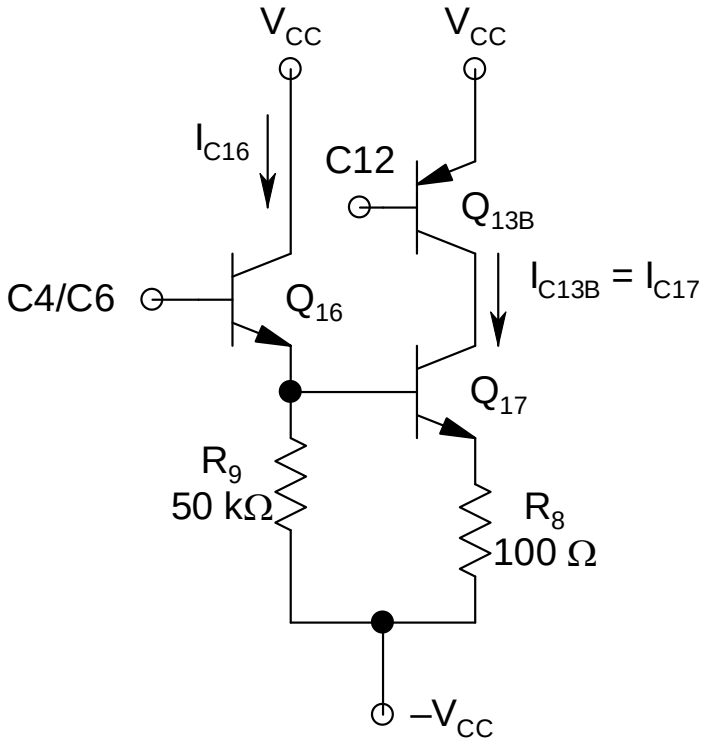
    $V_{R3} = V_{BE5} + I_{C5}R_1 = 606.8$ mV

    $\Rightarrow I_{C7} \approx I_{R3} = V_{R3}/R_3 = 12.1$ μA

➢ *DC Biasing of the Gain Stage*:

- $I_{C17} = I_{C13B} = 550\ \mu A$
- This is a ***large current*** and the ***base current may not be negligible***
- Assuming $\beta_{17} = 200$:

  $I_{B17} = I_{C17}/\beta_{17} = 2.75\ \mu A$
- Assuming $I_{S17} = 1$ fA, the ***base voltage*** of Q_{17}, ***w.r.t. the negative power supply*** ($-V_{CC}$):



$$V_{B17}\ (\text{w.r.t.}\ -V_{CC}) \approx V_T \ln(I_{C17}/I_{S17}) + I_{C17}R_8$$
$$= 757.9\ \text{mV}$$

- Thus:

$I_{R9} = V_{B17}/R_9$

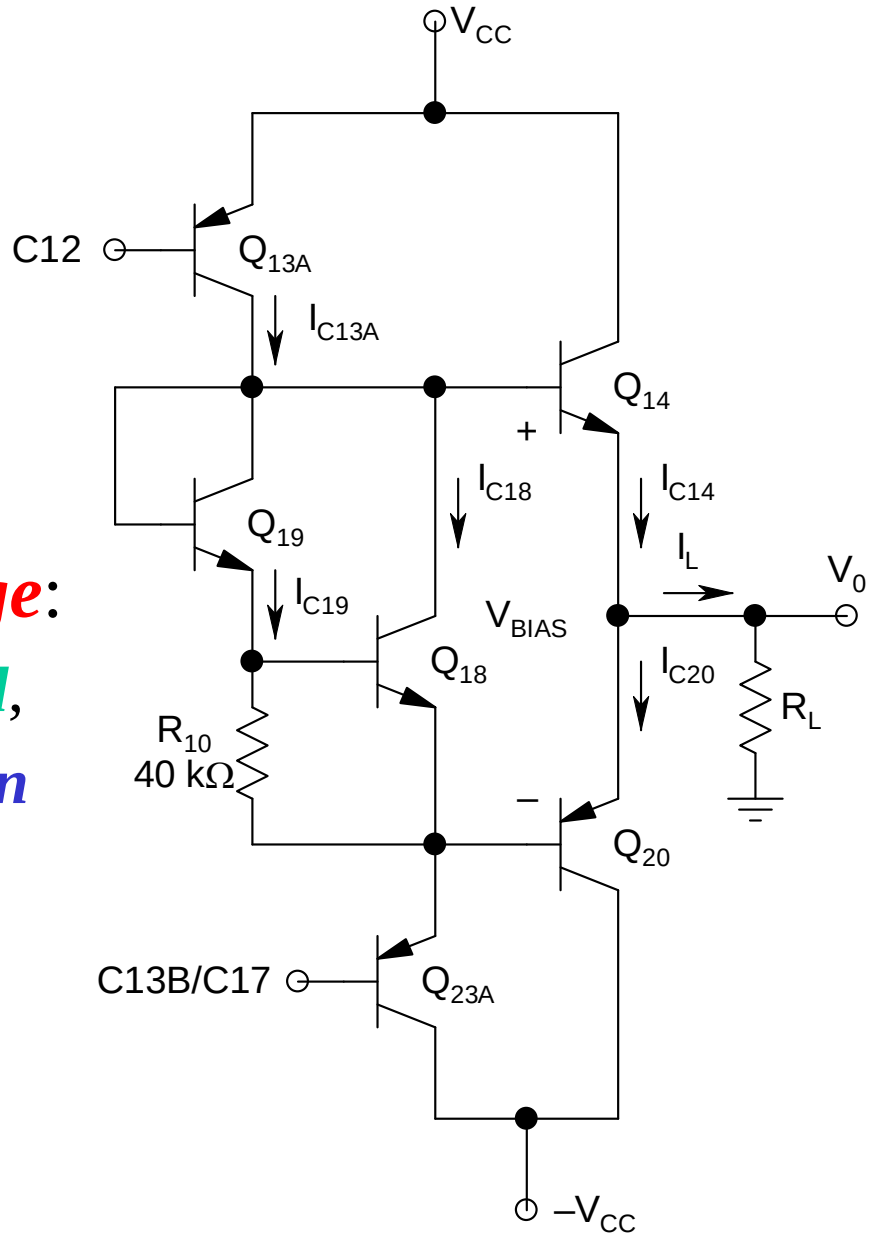
$= 15.16\ \mu A$

$\Rightarrow I_{C16} = I_{R9} + I_{B17}$

$= 17.9\ \mu A$

➢ ***Finally, the output stage***:

- Q_{15}-Q_{21}-R_6-R_7 ***neglected***, since these are ***protection devices***, and ***come into play*** only during ***accidental short-circuiting of the output***



- To find the ***idling current***, R_L is ***removed***, thus making $I_L = 0$

  $\Rightarrow$ ***Standby (Idling) Current*** = $I_{C14} = I_{C20}$

- Q_{18}-Q_{19}-R_{10} is an ***extremely cleverly and innovatively designed block***
  - ❖ It produces a ***prebias voltage*** V_{BIAS} (***close to*** $2V_\gamma$) ***between the bases of*** Q_{14} ***and*** Q_{20}
  - ❖ At the same time, it ***reduces the standby power dissipation of the output branch***
- I_{C13A} = 183.3 μA, and ***splits*** into Q_{18}-Q_{19} combination
- Assuming V_{BE18} = 0.7 V and for the time being, ***neglecting*** I_{B18}:

  $I_{C19} \approx I_{R10} = V_{BE18}/R_{10}$ = 17.5 μA

- Thus:

  $I_{C18} = I_{C13A} - I_{C19} = 165.8\ \mu A$ (***neglecting I_{B19}***)

- Since I_{C18} is ***pretty high***, we need to now ***fine tune*** our analysis by ***including I_{B18}***

- Assuming $I_{S18} = 1$ fA and $\beta = 200$:

  $I_{C19} = I_{B18} + I_{R10} = I_{C18}/\beta_{18} + (V_T/R_{10})\ln(I_{C18}/I_{S18})$

  $= 17.6\ \mu A$

- This is ***sufficiently close*** to our ***initial estimate*** of 17.5 μA

- Thus:

  $I_{C18} = I_{C13A} - I_{C19} = 165.7\ \mu A$

  which is ***almost same*** as our ***original estimate***

- $V_{BIAS} = V_{BE18} + V_{BE19} = V_{BE14} + V_{EB20}$

  $\Rightarrow V_T \ln(I_{C18}/I_{S18}) + V_T \ln(I_{C19}/I_{S19})$

  $= V_T \ln(I_{C14}/I_{S14}) + V_T \ln(I_{C20}/I_{S20})$

- ***Since $I_L = 0$***:

$$\Rightarrow I_{C14} = I_{C20} = \sqrt{\frac{I_{S14} I_{S20}}{I_{S18} I_{S19}}} \sqrt{I_{C18} I_{C19}}$$

- The ***sizes*** of the ***output transistors*** are typically ***much larger*** than the other devices, to be able to ***supply large current to the load*** ***without overheating***
- Assuming $I_{S14} = I_{S20} = 4I_{S18} = 4I_{S19}$:

  $I_{C14} = I_{C20} = 216\ \mu A$
- Thus, the ***idling*** (***standby***) ***power dissipation*** of the ***output branch*** = (30 V) × (216 μA) = 6.5 mW

- $V_{BIAS} = V_{BE18} + V_{BE19} = V_{BE14} + V_{EB20}$

  $\Rightarrow V_T \ln(I_{C18}/I_{S18}) + V_T \ln(I_{C19}/I_{S19})$

  $= V_T \ln(I_{C14}/I_{S14}) + V_T \ln(I_{C20}/I_{S20})$

- ***Since $I_L = 0$***:

$$\Rightarrow I_{C14} = I_{C20} = \sqrt{\frac{I_{S14} I_{S20}}{I_{S18} I_{S19}}} \sqrt{I_{C18} I_{C19}}$$

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- Assuming $I_{S18} = I_{S19} = 1$ fA:

  $V_{BIAS} = V_T \ln[I_{C18}I_{C19}/(I_{S18}I_{S19})] = 1.285$ V
- This produces a ***DC bias*** of ***~ 643 mV*** across the ***BE junctions*** of Q_{14} and Q_{20}, keeping them at the ***verge of conduction***
- Note that instead of the ***prebias combination*** used, if simply ***two diodes*** were used in ***series***, then the ***current*** through that ***branch*** would have been ***183.3 μA***, resulting in a current of ***733.2 μA*** in the ***output branch***, thus creating ***standby power dissipation*** in the ***output branch*** of ***22 mW*** (***3.4 times***)
- Finally, $I_{C23A} = I_{C13A} = 183.3$ μA

Transistor(s)	Magnitude (μA)
I_{C1}, I_{C2}, I_{C3}, I_{C4}, I_{C5}, I_{C6}	9.5
I_{C7}	12.1
I_{C8}, I_{C9}, I_{C10}	19
I_{C11}, I_{C12}	733.3
I_{C13A}, I_{C23A}	183.3
I_{C13B}, I_{C17}	550
I_{C14}, I_{C20}	216
I_{C16}	17.9
I_{C18}	165.7
I_{C19}	17.6

The DC Bias Currents of Different Transistors

- The ***DC power dissipation*** of the circuit:

$$P_{DC} = V_{CC} \times (I_{C12} + I_{C9} + I_{C8} + I_{C13A} + I_{C13B} + I_{C14} + I_{C7} + I_{C16}) + |-V_{CC}| \times (I_{C11} + I_{C10} + I_{C5} + I_{C7} + I_{C6} + I_{R9} + I_{C17} + I_{C23A} + I_{C20})$$

$$= 52.3 \text{ mW}$$

- Note that the ***reference branch*** consumes the ***highest DC power***, followed by the ***Darlington branch***
- On the other hand, the ***least DC power*** is consumed by the ***DA branch***

- ***ac Analysis***:
  - ***Primary Goal***:
    - ***To find R_i, R_0, and A_{vOL}***
  - We will adopt a ***modular approach***:
    - ***Considering each stage individually***
    - ***Finding the 2-port equivalent for each of them***
    - ***Eventually joining them together to get the total response***

- Assumed:

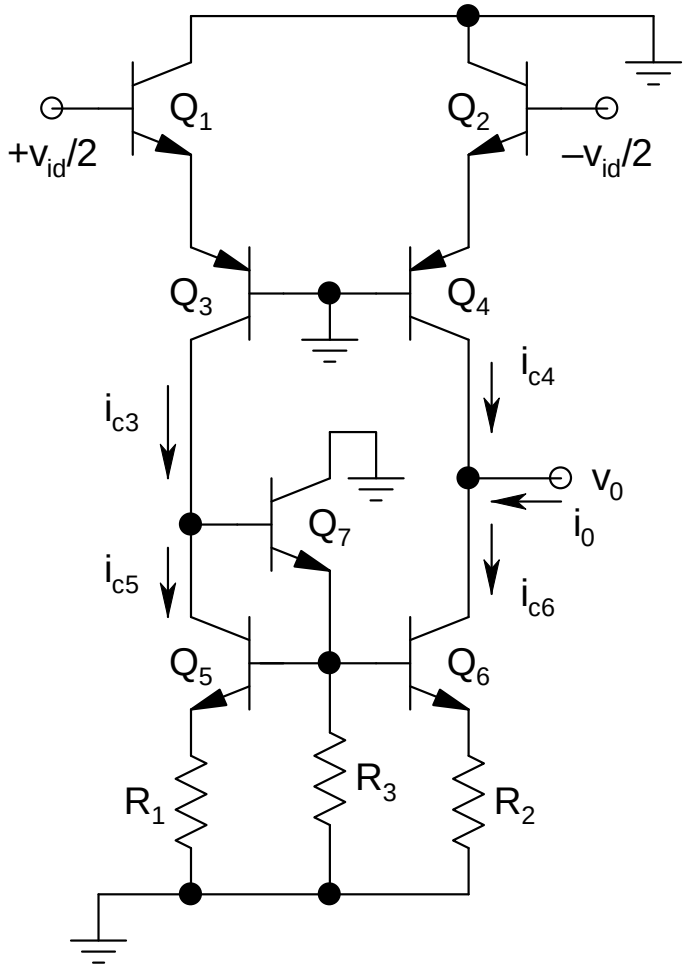
  $\beta_N = 200$, $\beta_P = 100$, $V_{AN} = 130$ V, $V_{AP} = 50$ V

- We will also ***evaluate*** the ***required value*** of the ***compensation capacitor*** C_C

- The ***analysis*** will be ***simple*** and ***highly approximate***, however, the ***results*** will ***definitely lie*** within ***±10%*** of the ***actual***

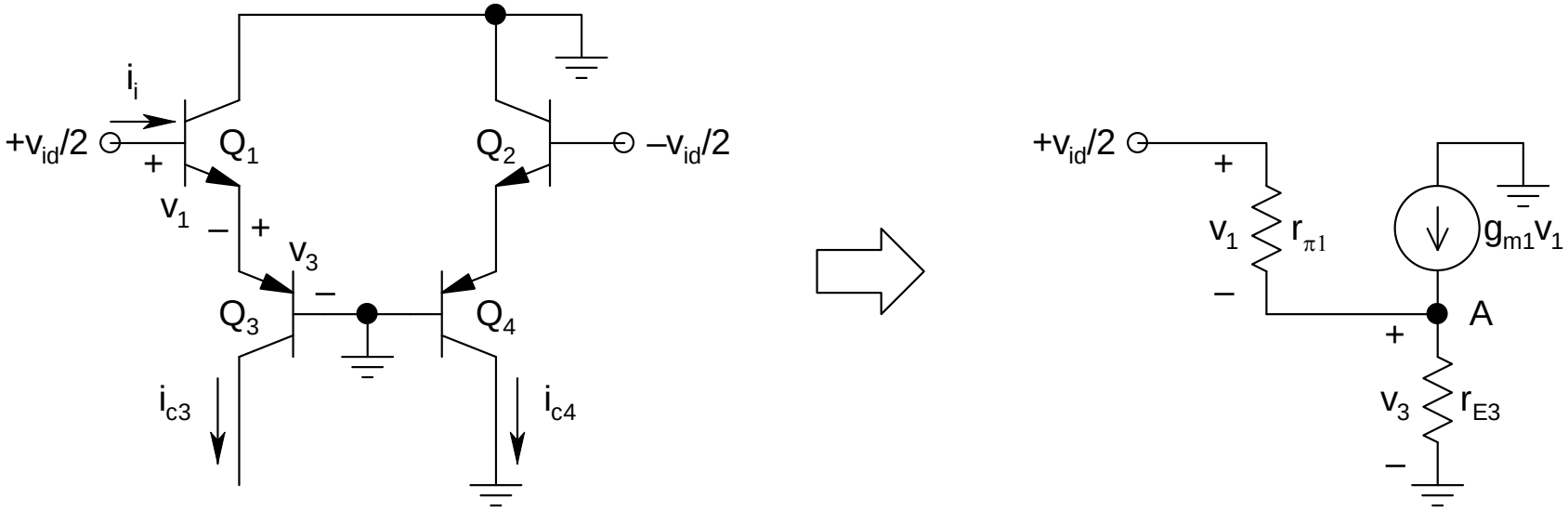
➢ *Input Stage*:

- ***Differential-mode input*** v_{id} ***split*** into $+v_{id}/2$ and $-v_{id}/2$, and ***applied*** at the ***bases*** of Q_1-Q_2
- All ***terminals*** having ***fixed DC potentials*** have been tied to ***ac ground***
- ***Bases*** of Q_3-Q_4 are at ***ac ground*** due to ***perfect symmetry*** of the circuit



- $i_{c3} = i_{c5}$ (***neglecting base current of Q_7***)
- $i_{c6} = i_{c5}$ (***ratioed mirror with $R_1 = R_2$***)
- ***Output current***:

  $i_0 = i_{c6} - i_{c4} = i_{c5} - i_{c4} = i_{c3} - i_{c4}$
- To find the ***short-circuit transconductance*** of this stage, we ***short the output node to ground***



- $v_{id}/2 = v_1 + v_3$
- ***KCL at node A***:

  $v_1/r_{\pi 1} + g_{m1}v_1 = v_3/r_{E3}$

$$\Rightarrow v_1 = \frac{r_{\pi 1}}{r_{E3}}\frac{1}{1+g_{m1}r_{\pi 1}}v_3 = \frac{r_{\pi 1}}{r_{E3}}\frac{1}{1+\beta_1}v_3 \simeq \frac{r_{\pi 1}}{\beta_1}\frac{1}{r_{E3}}v_3 \simeq \frac{r_{E1}}{r_{E3}}v_3 = v_3$$

$$\Rightarrow v_{id} = 4v_3 \Rightarrow v_3 = v_{id}/4$$

$$\Rightarrow i_{c3} = g_{m3}v_3 = g_{m3}v_{id}/4 \text{ and } i_{c4} = -g_{m3}v_{id}/4$$

$$\Rightarrow i_0 = i_{c3} - i_{c4} = +g_{m3}v_{id}/2$$

- Thus, the ***short-circuit transcoductance***:

$$G_{m1} \triangleq \left.\frac{i_0}{v_{id}}\right|_{v_0=0} = \frac{g_{m3}}{2} = \frac{I_{C3}}{2V_T} = 182.7\ \mu\mho$$

- ***Differential-mode input resistance***:

$$R_{id} \triangleq \frac{v_{id}}{i_i} = 2 \times \frac{v_{id}/2}{i_i} = 2(\beta_1 + 1)(r_{E1} + r_{E3}) \simeq 4\beta_1 r_{E1}$$

$$= \frac{4\beta_1 V_T}{I_{C1}} = 2.2 \text{ M}\Omega$$

- This is also the ***input resistance*** R_i of the ***op-amp***
- The ***output resistance*** can be ***calculated*** by following our ***standard procedure*** of ***nulling the independent sources***, ***exciting the output by a test voltage source***, and ***finding the current drawn from it***

- ***Base*** of Q_6 can be considered to be at a ***fixed DC potential***, and thus, ***ac ground***
- ***By inspection***:

$R_{04} = r_{04}[1 + g_{m4}(r_{\pi4}||r_{E2})]$

$R_{06} = r_{06}[1 + g_{m6}(r_{\pi6}||R_2)]$

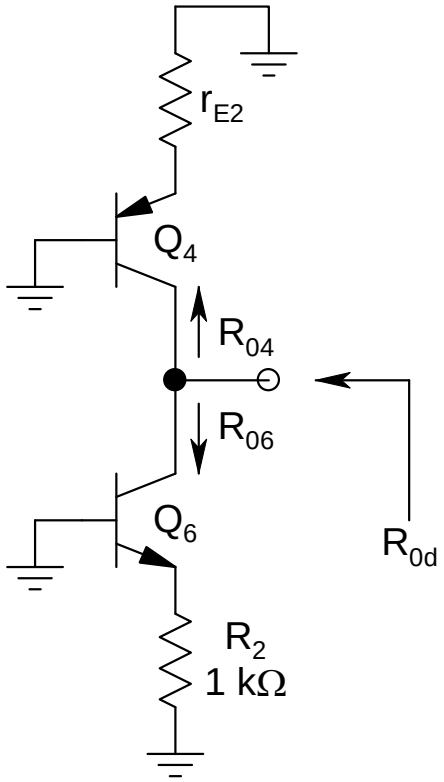
$r_{04} = V_{AP}/I_{C4} = 5.26\ M\Omega$

$g_{m4} = I_{C4}/V_T = 365\ \mu A/V$

$r_{\pi4} = \beta_4/g_{m4} = 273.7\ k\Omega$

$r_{E2} = V_T/I_{C2} = 2.74\ k\Omega$

$\Rightarrow R_{04} \approx 2r_{04} = 10.5\ M\Omega$



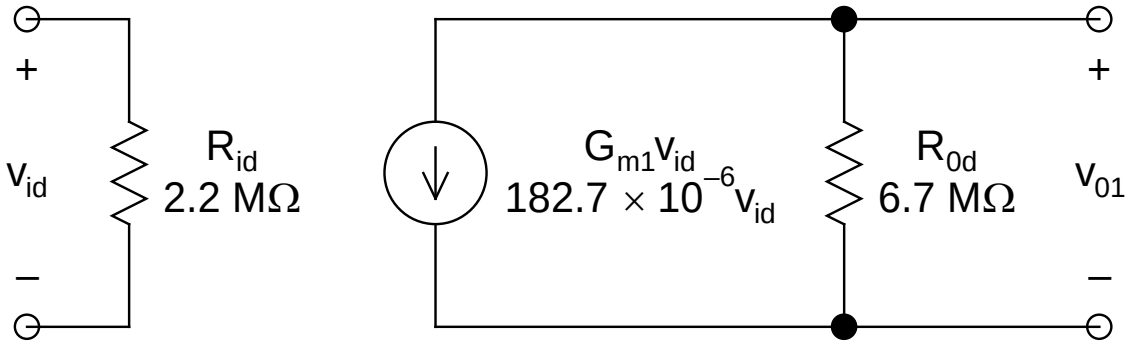
$r_{06} = V_{AN}/I_{C6} = 13.7\ M\Omega$

$g_{m6} = I_{C6}/V_T = 365\ \mu A/V$

$r_{\pi 6} = \beta_6/g_{m6} = 547.9\ k\Omega$

$\Rightarrow R_{06} \approx r_{06}(1 + g_{m6}R_2) = 18.7\ M\Omega$

$\Rightarrow R_{0d} = R_{04} \| R_{06} = 6.7\ M\Omega$



2-Port Equivalent of the Input Stage

➢ *Gain Stage*:

- $r_{E16} = V_T/I_{C16} = 1.45\ k\Omega$

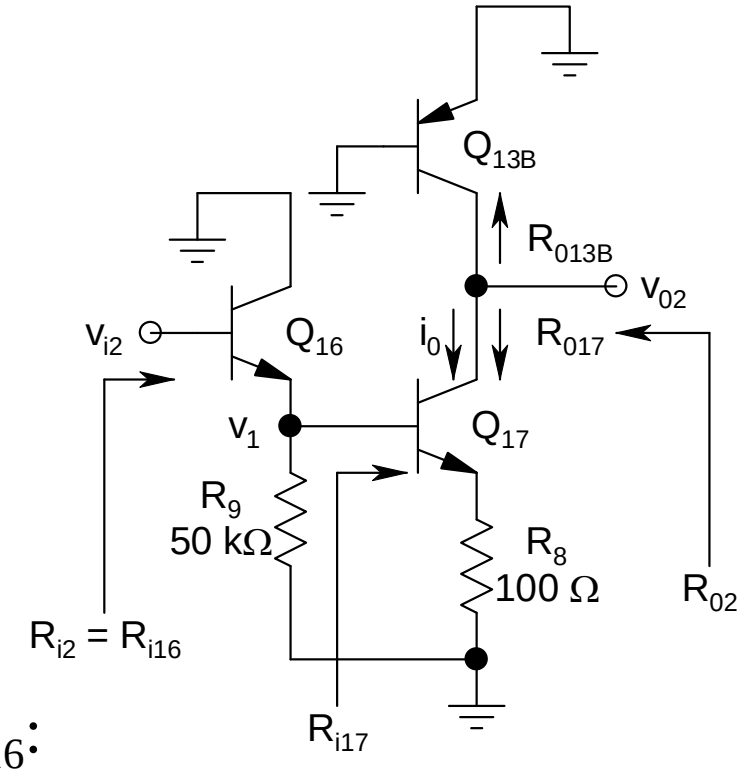
  $r_{\pi 16} = \beta_{16} r_{E16} = 290.5\ k\Omega$

  $r_{E17} = V_T/I_{C17} = 47.3\ \Omega$

  $r_{\pi 17} = \beta_{17} r_{E17} = 9.45\ k\Omega$

  $\Rightarrow R_{i17} = r_{\pi 17} + (\beta_{17} + 1)R_8$

  $= 29.6\ k\Omega$



- ***Effective load resistance*** of Q_{16}:

  $R_{L16} = R_9 || R_{i17} = 18.6\ k\Omega$

- Thus, the ***input resistance*** of the ***gain stage***:

  $R_{i2} = R_{i16} = r_{\pi 16} + (\beta_{16} + 1)R_{L16} = 4.03\ M\Omega$

- Next, we have to ***calculate*** the ***short-circuit transconductance*** G_{m2} $(= i_0/v_{i2})$, with the ***output terminal shorted to ground***
- ***Voltage gain*** of Q_{16}:

  $v_1/v_{i2} = R_{L16}/(R_{L16} + r_{E16}) = 0.93$
- ***Overall transconductance*** of Q_{17}-R_8 combination (***emitter degenerated stage***):

  $G_{m17} = i_0/v_1 = g_{m17}/(1 + g_{m17}R_8) \approx 1/(r_{E17} + R_8)$

  $= 6.8$ mA/V

  $\Rightarrow G_{m2} = i_0/v_{i2} = (i_0/v_1) \times (v_1/v_{i2}) = 6.3$ mA/V
- Next is the ***output resistance*** R_{02}
- ***From inspection***: $R_{02} = R_{013B} \| R_{017}$

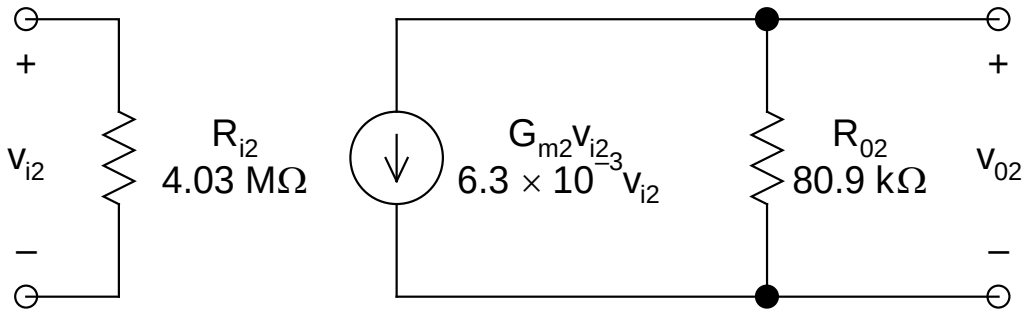
- $R_{013B} = r_{013B} = V_{AP}/I_{C13B} = 90.9\ k\Omega$
- $r_{017} = V_{AN}/I_{C17} = 236.4\ k\Omega$
- Since ***base*** of Q_{17} can be considered to be at ***ac ground***, and $r_{\pi 17} >> R_8$:

  $R_{017} \approx r_{017}(1 + g_{m17}R_8) = r_{017}(1 + R_8/r_{E17})$

  $= 736.2\ k\Omega$

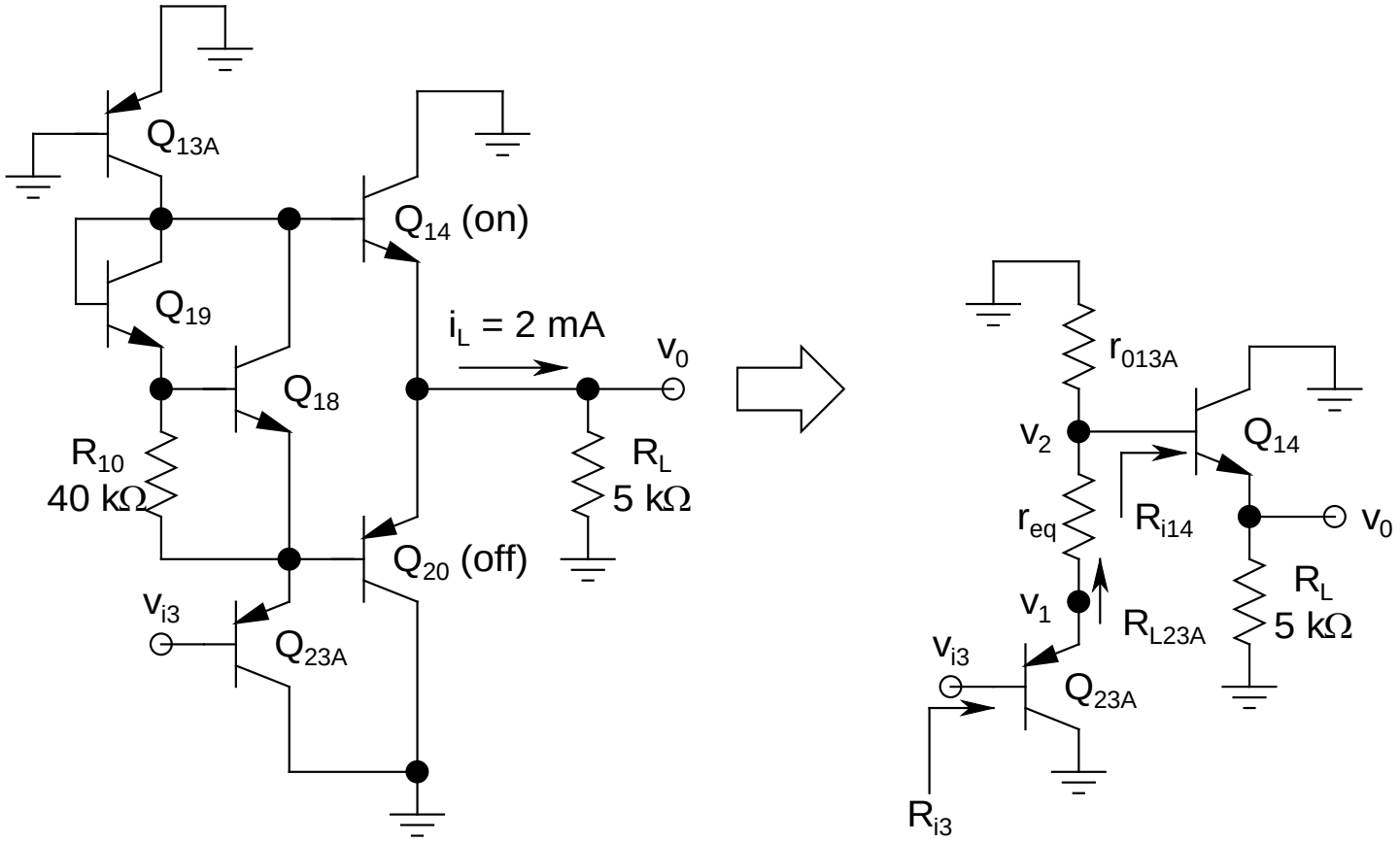
- Thus:

  $R_{02} = R_{013B} \| R_{017} = 80.9\ k\Omega$



2-Port Equivalent of the Gain Stage

➢ *Output Stage*:



Circuit **Schematic**

- ***Analysis slightly different***, since the ***transistors operate with large signal swings***, ***typically from rail-to-rail***, and ***small-signal analysis is not quite valid***
- Will attempt an ***approximate analysis*** under some ***specific assumptions***:
  - v_0 under ***positive excursion***, with Q_{14} ***supplying current to load*** (R_L) and Q_{20} ***off***
  - $R_L = 5\ k\Omega$ and $i_L = 2\ mA$

    $\Rightarrow v_0 = 10\ V$
- ***Ex.***: Show that Q_{18}-Q_{19}-R_{10} ***combination*** effectively appears as a ***resistance*** $r_{eq} = 168.7\ \Omega$
- $r_{E14} = V_T/I_{C14} = 13\ \Omega$
- $r_{013A} = r_{023A} = V_{AP}/I_{C13A} = V_{AP}/I_{C23A} = 272.8\ k\Omega$

- $r_{E23A} = V_T/I_{C23A} = 141.8\ \Omega$
- $r_{\pi 23A} = \beta_{23A} r_{E23A} = 14.2\ k\Omega$
- $R_{i14} = (\beta_{14} + 1)(r_{E14} + R_L) = 1\ M\Omega$
- $R' = r_{013A} \| R_{i14} = 214.3\ k\Omega$
- ***Effective load*** of Q_{23A}:

  $R_{L23A} = r_{eq} + R' = 214.5\ k\Omega$
- R_{L23A} appears in ***parallel*** with r_{023A}

  $\Rightarrow R_{eq} = r_{023A} \| R_{L23A} = 120.1\ k\Omega$

  $\Rightarrow R_{i3} = r_{\pi 23A} + (\beta_{23A} + 1) R_{eq} = 12.1\ M\Omega$

- Note the ***enormously large input resistance*** of the ***output stage***, primarily due to ***two factors***:
  - ***Buffering action*** of Q_{23A}, putting its ***entire emitter load to base after multiplying it by β***
  - ***Relatively large value of R_L***
- Thus, the ***choice*** of putting Q_{23A} in the ***signal path*** is obvious
  - It also provides a ***DC level shift*** of ~ +0.7 V
- Note also that R_{i3} appears as the ***load of the gain stage***, having an ***output resistance*** R_{02} of only 80.9 kΩ

  $\Rightarrow$ ***Negligible loading***

- Since this stage is basically a ***cascade of voltage followers***, hence, it would be ***more prudent*** to find the ***overall voltage gain*** of this stage, rather than the ***short-circuit transconductance***
- Thus:

$$v_1/v_{i3} = R_{eq}/(R_{eq} + r_{E23A}) = 0.9988$$

$$v_2/v_1 = R'/(R' + r_{eq}) = 0.9992$$

$$v_0/v_2 = R_L/(R_L + r_{E14}) = 0.9974$$

$$\Rightarrow A_{v3} = v_0/v_{i3} = (v_0/v_2) \times (v_2/v_1) \times (v_1/v_{i3})$$

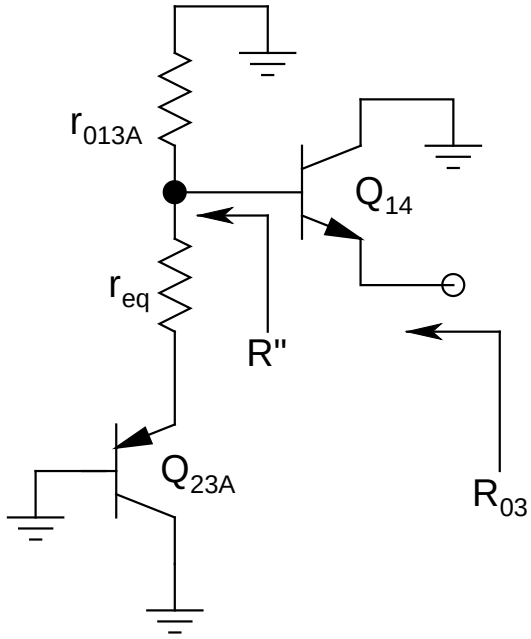
$$= 0.9954 \approx 1$$

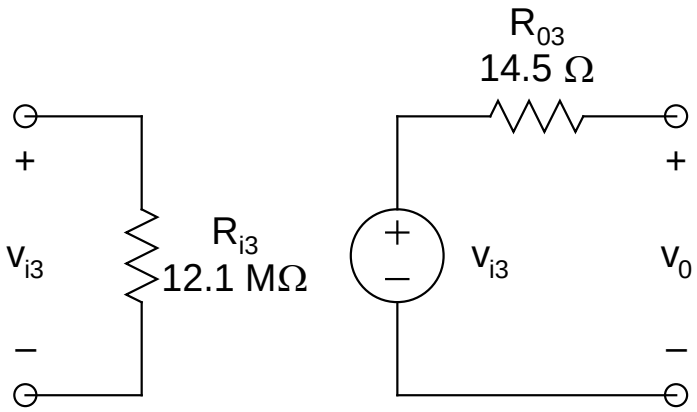
- Note that in spite of ***keeping*** so many ***significant digits*** after the ***decimal point*** in all the ***intermediate results***, the ***end result*** is still ***extremely close to unity***

- The ***output resistance*** R_{03} can be ***evaluated*** from a ***simple inspection*** of the circuit:

$$R'' = r_{013A} \| (r_{eq} + r_{E23A}) = 310.1\ \Omega$$

$$\Rightarrow R_{03} = r_{E14} + R''/(\beta_{14} + 1) = 14.5\ \Omega$$

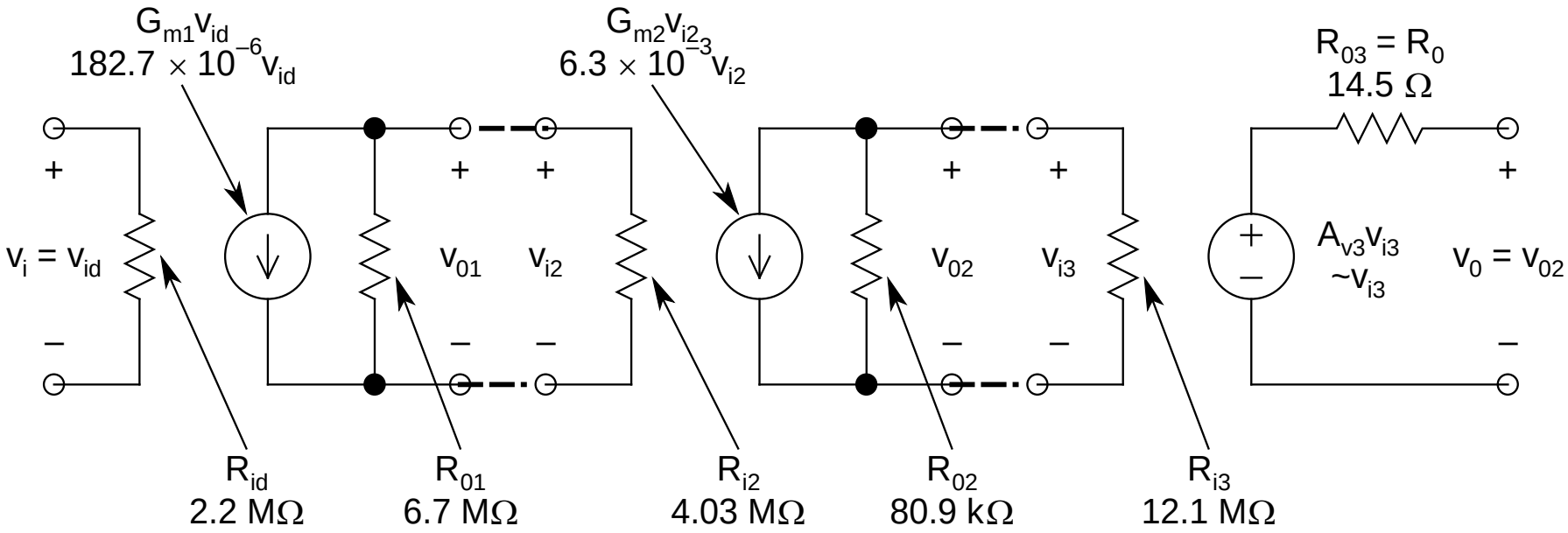




2-Port Equivalent of the Output Stage

➢ *Overall Performance*:

- Just *cascade* the *2-port equivalents* of the *three stages*



Complete 2-Port Representation of 741 Op-Amp

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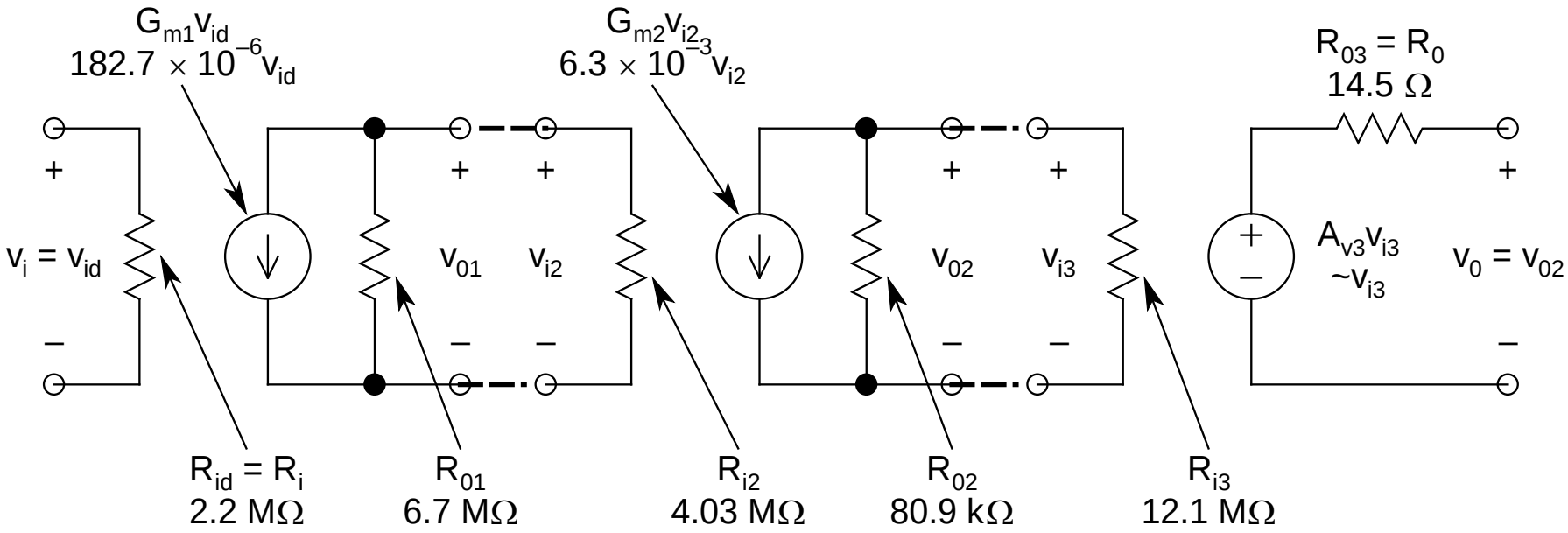


Complete 2-Port Representation of 741 Op-Amp

- ***Voltage gain of the input stage***:

  $A_{v1} = v_{01}/v_{id} = -G_{m1}(R_{01}||R_{i2}) = -459.7$

- ***Voltage gain of the gain stage***:

  $A_{v2} = v_{02}/v_{01} = -G_{m2}(R_{02}||R_{i3}) = -506.3$

- ***Voltage gain of the output stage***:

  $A_{v3} \sim 1$

- Thus, the ***overall voltage gain*** of ***741 op-amp***:

  $A_{vOL} = v_0/v_{id} = (v_0/v_{i3}) \times (v_{i3}/v_{i2}) \times (v_{i2}/v_{id})$

  $= 2.33 \times 10^5$ (107.3 dB)

  Note: $v_{i3} = v_{02}$, and $v_{i2} = v_{01}$

- This is an ***excellent value***, in spite of the ***significant loading effect*** of the ***gain stage*** on the ***input stage***

➢ *Observations*:

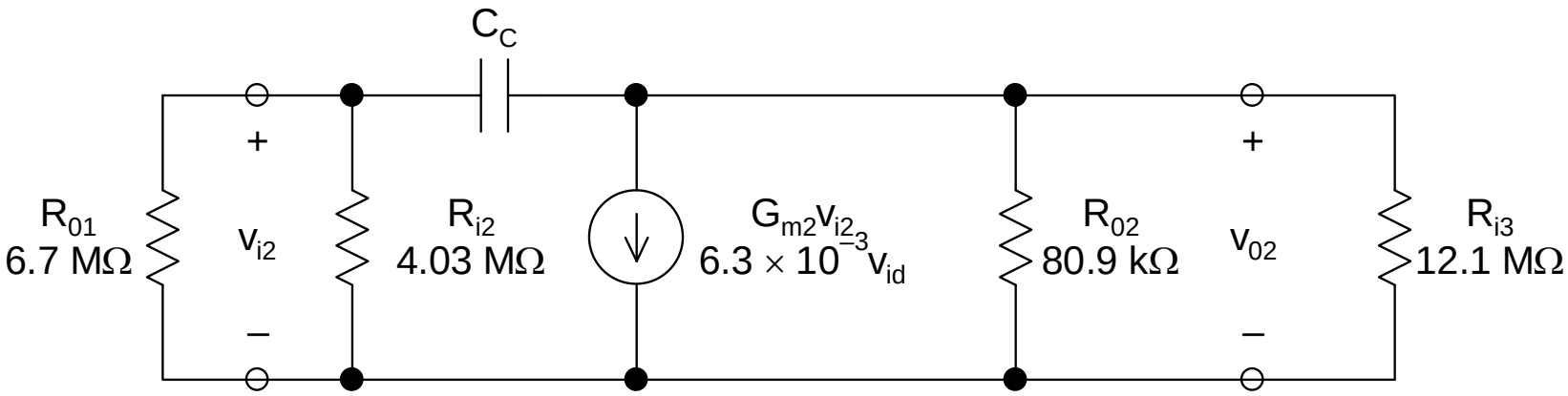
- A_{vOL} is actually the ***differential-mode gain*** (A_{dm})
- It is ***positive***
  - ❖ ***Positive*** v_{id} produces ***positive*** v_0
  - ❖ ***Bases*** of Q_1 and Q_2 are termed as ***non-inverting*** (+) and ***inverting*** (–) terminals respectively
- ***Input and output resistances*** are 2.2 MΩ and 14.5 Ω respectively, both of which are ***excellent values***
- The ***exact value*** of A_{cm} is ***slightly difficult to evaluate***, however, an ***estimate of CMRR can be made***
- Using the ***result*** of our ***simple analysis*** of ***DA***:

  $CMRR \approx 2g_{m1}r_{08} = 1923$ (66 dB)
- This is not too bad!
  - ❖ ***Actual value is much higher than this***

- ***Compensation***:
  - Actual evaluation of the ***frequency response*** characteristic of 741 is a ***huge task***, even with the ***ZVTC technique***
  - There will be ***numerous poles and zeros***, out of which, some will be ***important***, while others will be ***inconsequential***
  - However, there will of course be a ***Dominant Pole*** (DP), and rough calculation shows that it is ~ ***1 MHz***, which is the ***bandwidth*** of the ***uncompensated op-amp***

- Now, ~ ***100 dB open-loop gain*** with ***1 MHz bandwidth*** is a ***ready recipe for disaster*** as far as the ***stability of the system*** is concerned
- Hence, for ***unconditional stability*** under ***unity negative feedback***, e.g., ***voltage follower***, ***compensation is imperative***
- In 741, this task is accomplished by the technique of ***Dominant Pole Compensation*** (DPC) through the use of the ***compensation capacitor*** C_C, ***connected between the input and output of the gain stage***

- To obtain the ***required value*** of C_C, we use the cascade of the ***2-port networks***, as was done earlier to compute the ***overall voltage gain***



- Denote $R' = R_{01} || R_{i2} = 2.5\ M\Omega$ and $R'' = R_{02} || R_{i3} = 80.4\ k\Omega$

- The ***simplified circuit*** can be easily identified as the ***three-legged creature***, and using the ***ZVTC technique***:

$$R_C^0 = R' + R'' + G_{m2} R' R'' = 1.27\ G\Omega$$

- Now, to get an estimate of the ***DPF*** f_d, we assume that the ***open-loop gain*** is exactly 100 dB, and the ***first pole*** of the ***uncompensated op-amp*** is ***exactly 1 MHz***

$$\Rightarrow f_d = 10\ \text{Hz}$$

- Also, $f_d = \omega_d/(2\pi)$, with $\omega_d = 1/\tau$, and

$$\tau = R_C^0 C_C$$

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- Also, $f_d = \omega_d/(2\pi)$, with $\omega_d = 1/\tau$, and

$$\tau = R_C^0 C_C$$

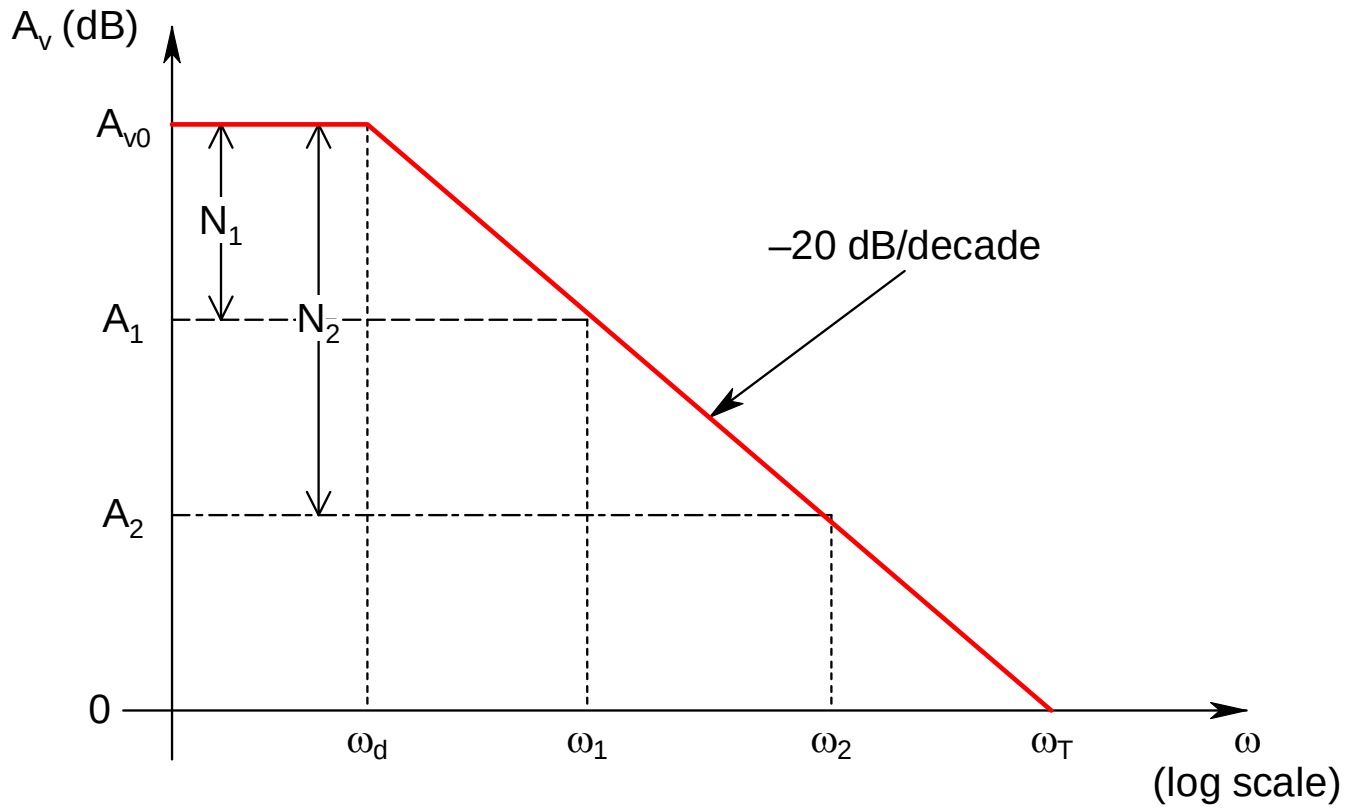
- Thus:

$$C_C = \tau / R_C^0 = 12.5 \text{ pF}$$

- Note that with this ***compensation scheme***, the ***open-loop bandwidth*** of the ***compensated op-amp*** drops all the way down to ***10 Hz*** from ***1 MHz***
- However, this is not really a ***limitation***, since the ***open-loop gain*** is ***so high***, that even with ***negative feedback***, ***sufficiently high values of gain can be achieved***

- ***Unity-Gain Bandwidth (f_T)***:
  - ***Product*** of the ***dominant pole frequency*** and the ***open-loop gain***
  - This is also the ***bandwidth*** of the system when the ***gain is unity*** (hence the name!)
  - Also known as the ***gain-bandwidth product*** (GBP)
  - It is ***1 MHz*** for this case
  - Note that under ***DPC***, it's also the ***first pole*** of ***uncompensated system***
  - With ***negative feedback***, the ***GBP remains constant***

    $\Rightarrow$ ***As gain$\downarrow$, bandwidth$\uparrow$, and vice-versa***



A_{v0}: Midband Gain, ω_d: Compensated Bandwidth, ω_T: Unity-Gain Bandwidth

N_1 and ω_1, N_2 and ω_2: Amount of Feedback and Corresponding Bandwidth

A_1, A_2: Gain With Feedback N_1, N_2

$$A_{v0}\omega_d = A_1\omega_1 = A_2\omega_2 = \omega_T$$

- ***Protection Circuits***:
  - Q_{15}-R_6: ***Overload protection circuit*** for Q_{14}
  - Similar to that discussed in the chapter on ***Output Stages***
  - R_6 ***senses*** the ***current*** being ***sourced*** by Q_{14} to ***load***
  - When the ***drop*** across R_6 ***approaches*** V_γ of Q_{15}, it starts to ***bypass*** the ***base current*** of Q_{14}

    $\Rightarrow$ ***The current does not increase indefinitely***
  - ***Protection scheme of Q_{20} is slightly different***

- For the ***previous case*** of Q_{14}, the ***load current*** was ***flowing out*** of the circuit
- However, for Q_{20}, the ***load current*** is ***flowing into*** the circuit
- Thus, the circuit should be ***protected*** by ***limiting*** the amount of this ***current***
- Here, R_7 ***senses*** the ***current*** being ***sunk*** by Q_{20}
- As soon as the ***drop*** across R_7 ***approaches*** V_γ of Q_{21}, it ***turns on*** and starts to ***bypass*** the ***current*** through Q_{20}

- ***Values of R_6 and R_7 are slightly different to account for the difference in V_γ for npn and pnp BJTs***
- Initially, this ***shunted current*** starts to ***flow*** through the ***unnumbered*** 50 kΩ resistor to $-V_{CC}$
- When the ***drop*** across this 50 kΩ resistor ***approaches*** V_γ of Q_{24}, it starts to ***turn on***, which makes Q_{22} to ***turn on*** too (note that Q_{22} and Q_{24} form a ***mirror***)
- Now, the ***collector*** of Q_{22} is ***connected*** to the ***base*** of Q_{16}

- Thus, Q_{16} starts to ***lose*** its ***base drive***, since a ***part of it*** is ***shunted away*** by Q_{22}
- Hence, Q_{16} ***conducts less***, and produces a ***chain reaction***, which ***limits*** the ***current sinking capability*** of the ***output stage***
- Thus, the ***circuit gets protected***
- Now, about the ***role played by Q_{23B}***
- ***Note***: $V_{B16} = V_{E23B}$, and $V_{C17} = V_{B23B}$

  $\Rightarrow V_{EB23B} = V_{B16} - V_{C17}$
- Also, $V_{C17} = V_{B17} + V_{CB17}$

- Noting that $V_{B17} = V_{E16}$:

  $V_{EB23B} = V_{B16} - V_{E16} - V_{CB17} = V_{BE16} - V_{CB17}$
- Under ***normal operating condition***, $V_{BE16} \sim 0.7$ V
- If Q_{17} also is in the ***FA mode***, which is the ***desired mode of operation***, then the ***CB junction*** of Q_{17} will be ***reverse biased***

  $\Rightarrow V_{CB17}$ is ***positive***

  $\Rightarrow V_{EB23B} < V_{BE16}$, and Q_{23B} would ***remain off***
- Now, if ***for any reason whatsoever***, Q_{17} ***moves towards saturation***, then V_{CB17} would ***decrease***

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  $\Rightarrow V_{CB17}$ is ***positive***

  $\Rightarrow V_{EB23B} < V_{BE16}$, and Q_{23B} would ***remain off***
- Now, if ***for any reason whatsoever***, Q_{17} ***moves towards saturation***, then V_{CB17} would ***decrease***

- As soon as V_{CB17} ***equals zero*** (corresponding to ***onset of saturation*** of Q_{17}):
  - $\Rightarrow$ Q_{23B} would ***turn on*** and ***rob*** the ***base drive away from the base*** of Q_{16}
  - $\Rightarrow$ Q_{17} ***pushed back*** to the ***FA mode of operation***
- This ***chain of events*** is ***pretty complicated indeed***
- Thus, Q_{23B} ***prevents*** Q_{17} from ***saturating***, and thus, ***ensures optimum performance*** of the circuit

- ***Anomalies and Limitations***:
  - ***Common-Mode Rejection***
  - ***Input Offset Voltage/Input Offset Current***
  - ***Saturation Voltages***
  - ***Minimum Allowed Supply Voltage***
  - ***Slew Rate and Full-Power Bandwidth***

➢ *Common-Mode Rejection*:

- An *extremely important parameter* (*CMRR*)
- *Depends on*:
  - ❖ The *output resistance* r_{08} of Q_8
  - ❖ *Matching of the input transistors* (Q_1-Q_2 and Q_3-Q_4)
- *Higher* $r_{08} \Rightarrow$ *Better CMRR*
- *More mismatch in the input transistors* $\Rightarrow$ *Worse CMRR*
- *Exact calculation of* A_{cm} *is pretty tedious*
- A *rough estimate* of A_{cm} can be *obtained* by noting that:
  - ❖ For *common-mode input*, the *common collector point* of Q_1-Q_2 is *not at ac ground*, but *connected to the collector* of Q_8
  - ❖ $r_{o8} = V_{AP}/I_{C8} = 2.6\ M\Omega$

- Now, refer to the ***2-port equivalent*** of the ***differential-input stage***, having the ***input resistance*** R_{i2} of the ***gain stage*** as its ***load***
- Noting that the stage is basically ***CE(D)***:

$$\Rightarrow A_{cm} \simeq \frac{-\left(R_{01} \parallel R_{i2}\right)}{1/G_{m1} + 2r_{08}} = -0.48$$

- Thus:

  CMRR = $|A_{dm}/A_{cm}| = 4.85 \times 10^5$ (113.76 dB)

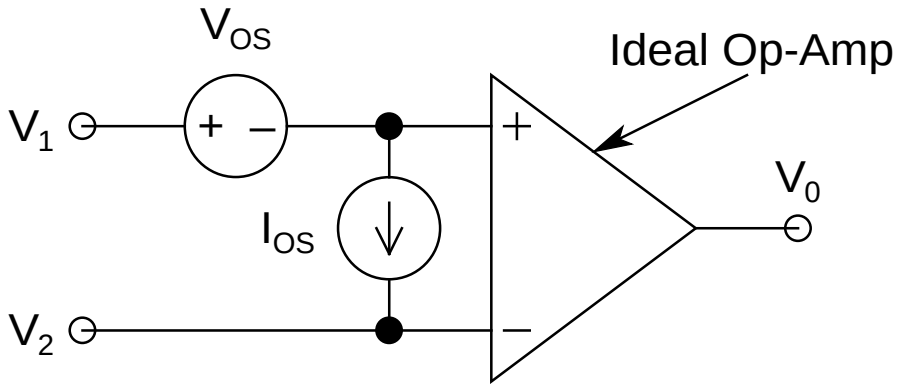
  which is ***phenomenal***
- This figure is ***much higher*** than that ***computed earlier***
- Of course, the ***analysis*** is ***highly simplistic***
- Even then, the ***actual value*** may be ***well above 100 dB***

- ***Input Offset Voltage/Input Offset Current***:
  - Created due to a ***mismatch*** between the ***input transistors***
  - For an ***op-amp*** with $A_{vOL} = 10^5$, operated with a ***power supply*** of ±10 V, V_{id} ***needed*** to cause V_0 to ***reach either of these two extremes*** = ±100 μV
  - The ***mismatch*** between the ***input transistors*** typically create a ***voltage difference*** between the ***inputs***, known as the ***Input Offset Voltage*** (V_{OS})
  - ***Typical value*** of V_{OS} for ***741 op-amp*** ~ 5-10 mV
  - This would ***cause*** V_0 to ***saturate*** at either $+V_{CC}$ or $-V_{CC}$
  - This is known as ***saturation*** or ***latch-up*** problem

- In ***741***, there is a ***provision*** to ***eliminate*** this ***problem***, known as ***offset nulling***
- Refer to the ***circuit*** of 741, and note ***pin numbers*** 1 and 5 ***connected*** to the ***emitters*** of Q_5 and Q_6
- Between these ***two pins***, a ***potentiometer*** is connected, with its ***wiper*** connected to $-V_{CC}$
- This ***potentiometer*** is known as the ***offset null resistor***
- It ***eliminates*** the ***effect*** of V_{OS} by ***creating*** an ***unequal division*** of ***bias currents*** in the ***two branches*** of the ***input circuit***, just enough to ***balance*** the ***difference*** caused due to ***device mismatch***

- ***Procedure***:
  - ***Tie both inputs to ground***: V_0 would most likely ***saturate*** at either $+V_{CC}$ or $-V_{CC}$
  - Next, ***move the wiper*** of the ***potentiometer*** in the ***direction*** that creates a ***magnitude reduction*** of V_0
  - Towards the ***end***, it will become ***very sensitive***, and a ***perfect nulling***, i.e., V_0 becoming ***exactly zero***, ***may not be possible***
  - The ***typically expected minimum value*** of V_0 may be ~ 5-10 mV
  - Leave the ***potentiometer setting*** at the ***best possible*** achieved result
  - ***Done***!

- ***The Input Offset Current (I_{OS})***:
  - ***Difference*** between the ***base currents*** (known as ***Input Bias Currents*** I_1 and I_2) of Q_1 and Q_2
  - ***Extremely small*** (~ ***tens to hundreds of nA***)
- I_{OS} and V_{OS} are actually ***interrelated***, since both of them are created due to ***device mismatch***, and have almost ***identical manifestations***



Both V_{OS} and I_{OS} are not used
V_{OS} (I_{OS}) is used when the input is voltage (current)

Modeling of the Anomalies With Regard to V_{OS} and I_{OS}

➢ *Saturation Voltages*:

- An *ideal op-amp* should have *rail-to-rail swing* at the *output*
- The *actual output swing* of a *real op-amp* is *never between rail-to-rail*
- Refer to the *op-amp schematic*, in conjunction with the *schematics* of the *gain stage* and the *output stage*
- As V_{i2} of the *gain stage* becomes *positive*, V_{02} (= V_{i3}) goes *negative* with a *large gain*

  $\Rightarrow$ V_2 and V_0 *follow* V_{i3} due to *emitter follower* (CC) action
- With V_0 *negative*, Q_{14} *turns off*, and Q_{20} *draws current from the load*

- Assuming that Q_{17} can ***soft saturate***, and neglecting the ***voltage drop*** across R_8, the ***minimum possible value*** of V_0:

  $V_0^- = -V_{CC} + V_{CE17}(SS) + V_{EB23A} + V_{EB20} = -13.4$ V

- Note that it is about ***two diode drops above*** $-V_{CC}$
- Now, for ***negative*** V_{i2}, V_{02} ***swings*** to a ***large positive value***, ***followed by*** V_2 and V_0
- With V_0 ***positive***, Q_{20} ***turns off***, and Q_{14} ***supplies current to load***
- ***Maximum positive limit*** of V_0 is ***reached*** when Q_{13A} ***soft saturates***:

  $V_0^+ = V_{CC} - V_{EC13A}(SS) - V_{BE14} = 14.1$ V

- Note again that it is ***lower*** than V_{CC} by ***little more than one diode drop***
- Also, interesting to note is that the ***positive*** and ***negative*** peaks of V_0 are ***not same***

  $\Rightarrow$ ***Maximum possible output swing is asymmetric***
- These ***two limits*** of V_0 are known as ***positive and negative saturation voltages*** (V_{SAT}^{+} and V_{SAT}^{-} respectively)
- If the ***input drive*** to the ***op-amp*** and the ***gain*** are such that the ***magnitude*** of V_0 becomes ***greater*** than either V_{SAT}^{+} or $|V_{SAT}^{-}|$, then V_0 would get ***clipped*** at either of these ***two values***

➢ *Minimum Allowed Supply Voltage*:

- Circuit for 741 is ***extremely robust***, and can be ***operated*** with a ***very wide range*** of ***supply voltage***
- However, there is a ***lower limit*** of the ***supply voltage***, below which it ***can't be ensured*** that ***all transistors*** operate in the ***FA region***
- To find this, look for the ***branch*** containing the ***most number of transistors***, since ***that branch*** would obviously ***need the largest voltage*** across it to ***ensure*** that all its ***constituent transistors operate in the FA region***
- From the ***circuit schematic*** of 741, ***this branch*** can be very easily identified to be ***either of the two sections of the input stage***

- Considering the ***left branch***, neglecting the ***potential dropped*** across R_1, and not letting ***CE voltage*** of any of the ***transistors*** to ***drop below*** 0.7 V (***onset of saturation***), there would ***four diode drops*** (~ 2.8 V) ***along this branch***

  $\Rightarrow$ ***741 should work satisfactorily for power supply all the way down to about ±3 V***

  $\Rightarrow$ ***Under this power supply***, ***V_0^+ and V_0^- will be 2.1 V and –1.4 V respectively***

- Thus, there is a ***wide range*** of ***power supply***, ***starting from ±3 V***, for which ***741 should work satisfactorily***

  $\Rightarrow$ ***Shows the robustness of the circuit***

➢ *Slew Rate and Full-Power Bandwidth*:

- This *limitation* is *observed* under *large-signal operation*, when the *input signal swing* is *greater* than the *linear range* of the *input differential pair*
- *Recall*: The *linear range* of a *bipolar differential pair* is ~ $\pm 4V_T$
- *Beyond this*, it basically *acts like a switch*, *transferring the bias current between the two branches*, *depending on the sign of the input voltage*
- Under such cases, the *compensation capacitor* C_C *limits* the *maximum possible rate of change* of V_0
- This is known as the *Slew Rate* (SR) of the op-amp:

  $SR = (dV_0/dt)_{max}$

- ***Two*** SRs are defined: SR^+ (***positive SR***) and SR^- (***negative SR***) for ***positive*** and ***negative*** excursions of V_0 respectively, generally expressed in ***V/μsec***
- A ***rough estimate*** of these quantities can be obtained by referring to the ***schematic*** of the op-amp
- Assume that a ***large negative signal*** is applied at the ***base*** of Q_1 (w.r.t. the base of Q_2)
- This will instantly turn the Q_1-Q_3 branch ***off***

  $\Rightarrow$ Q_5, and thus, Q_6, ***turn off***

  $\Rightarrow$ ***Entire bias current*** I_{C8} would ***flow through*** the Q_2-Q_4 branch, and ***start to charge*** C_C

- Note that the ***rate of this charging*** would be ***constant*** (***constant current charging***)

  $\Rightarrow$ ***Collector potential*** of Q_{17} would ***increase linearly with time***

- Due to ***emitter follower*** action of Q_{23A} and Q_{14}, V_0 would also start to ***increase linearly with time***

  - Q_{20} ***remains off***, since V_0 is in its ***positive excursion***

- Thus:

  $SR^+ = I_{C8}/C_C = (19\ \mu A)/12.5\ pF) = 1.52\ V/\mu sec$

- If the ***frequency*** of the ***input signal*** is such that the ***required time rate of change*** of V_0 is ***more*** than this, then V_0 ***won't be able to follow*** the input – rather, it will be ***dictated*** by the SR^+, and will ***change linearly with time***

- Similarly, when a ***large positive signal*** is applied at the ***base*** of Q_1 (w.r.t. the base of Q_2), Q_2-Q_4 branch would ***instantly turn off***

  $\Rightarrow$ ***Entire bias current*** I_{C8} would ***flow*** through the Q_1-Q_3 ***branch***, ***pushing the same current*** through Q_5

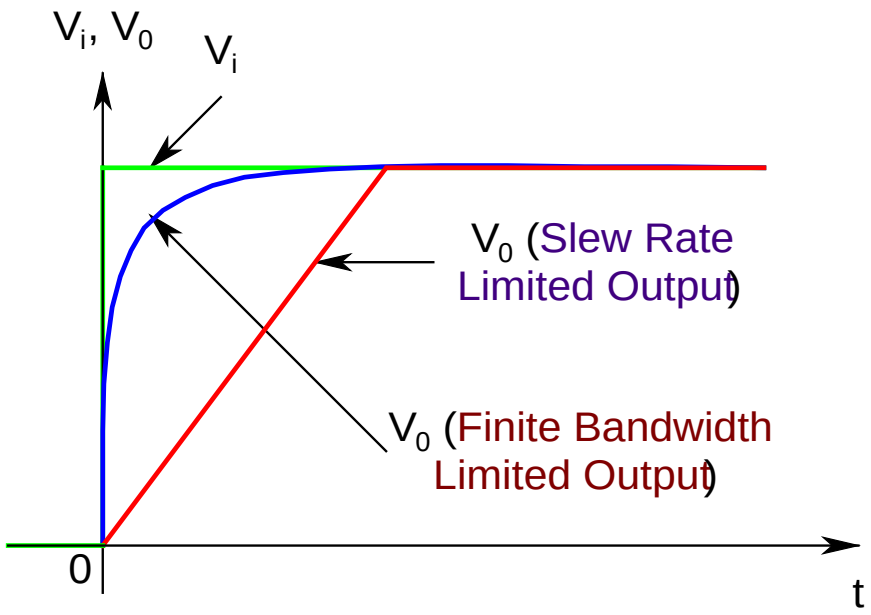
  $\Rightarrow$ Q_6 would ***carry the same current*** (***mirror*** with Q_5)

- This ***current*** would ***flow*** from the ***output node*** through C_C to Q_6

  $\Rightarrow$ C_C would ***start to discharge***, and V_0 would ***start to fall***, going into its ***negative swing***

- Since the ***same current*** (I_{C8}) is used to ***discharge*** the ***output node***:

  $SR^+ = SR^- = 1.52$ V/μsec



Slew Rate Limitation of Op-Amps

- Situation becomes ***more dramatic*** if a ***sinusoidal signal*** is applied at the ***non-inverting input*** of the op-amp, connected in a ***voltage-follower*** configuration
- Let ***input signal*** $V_i = V_M \sin(\omega t)$, with ***large*** V_M

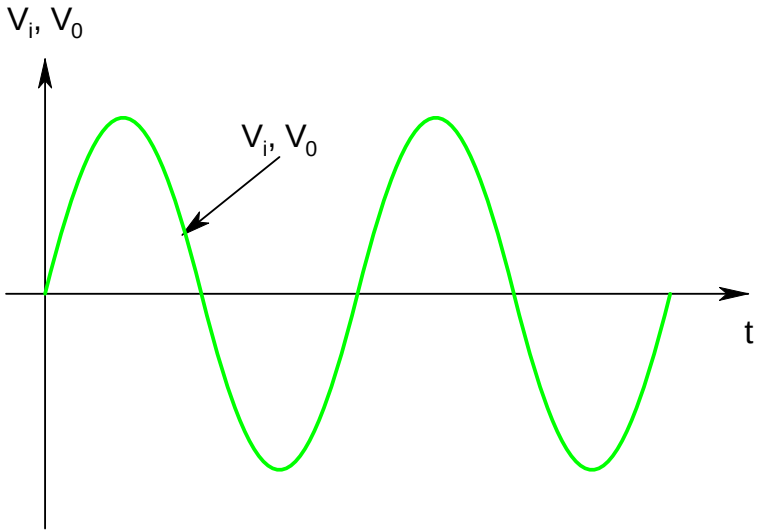
  $\Rightarrow$ ***Transistors*** in the ***differential input stage*** act as ***switches***
- Under ***unity feedback***, V_0 would ***follow*** V_i

  $\Rightarrow dV_0/dt = dV_i/dt = V_M \omega \cos(\omega t)$
- The ***maximum value*** of this ***derivative*** occurs when $\omega t = n\pi$ $(n = 0, 1, 2, \ldots)$

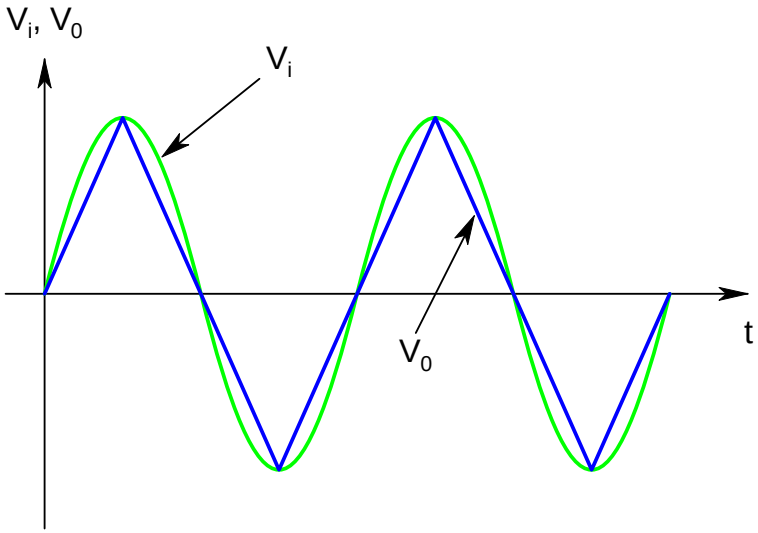
  $\Rightarrow$ It occurs when the ***signal crosses zero***
- So long as ***this rate*** remains ***smaller*** than SR, V_0 would ***follow*** V_i with ***fidelity***

- However, as soon as ***dV_0/dt becomes $\geq SR$***, V_0 ***won't be able to follow*** V_i anymore – rather, it would ***start to become triangular***
- ***Note***: $dV_0/dt\uparrow$ with an ***increase*** of ***either V_M or ω or both***

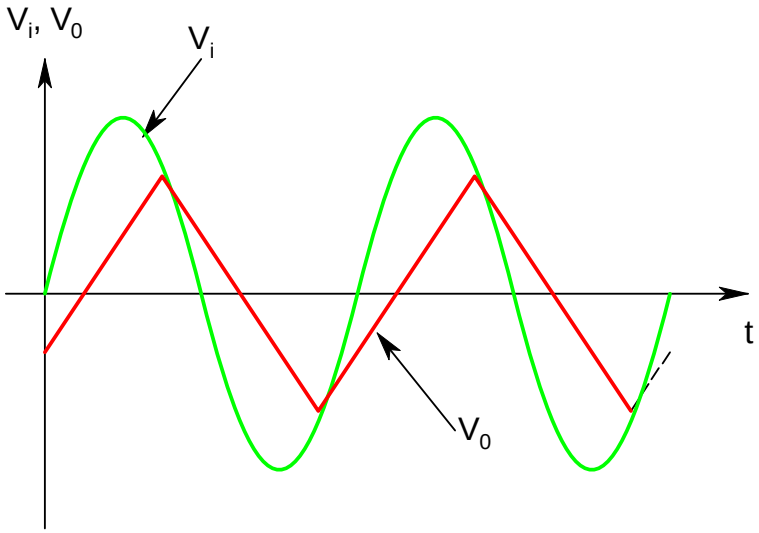
  $\Rightarrow$ ***What essentially matters is the product $V_M\omega$***
- If this ***product*** keeps on ***increasing*** beyond the SR, then V_0 remains ***triangular***, however, ***two major observations*** become apparent:
  - The ***zero crossings*** of V_0 ***do not quite coincide*** with those of V_i
  - The ***peak-to-peak swing*** of V_0 starts to become ***smaller*** than that of V_i due to V_0 ***not getting enough time*** to ***reach its maximum possible value***



Normal Behavior



Onset of Slew Rate Limitation



Severely Slew Rate Limited

- If $V_M\omega$ becomes ***very large***, then there ***may not be any output at all***

  $\Rightarrow V_0$ would ***become zero***, implying that the op-amp is ***not able to keep up with the variation*** of V_i at all!

- ***Mathematical Description***:
  - Let the ***gain*** of the op-amp = A

    $\Rightarrow (dV_0/dt)_{max} = AV_M\omega$
  - This must be ***less*** than the SR of the op-amp to get a ***distortion-free output***
  - ***Maximum possible value*** of $AV_M = V_{SAT}$

    $\Rightarrow$ The ***maximum allowed value*** of ω ($= \omega_M$) of V_i for V_0 to be ***without any distortion*** due to ***slew rate limitation***:

    $\omega_M = SR/V_{SAT}$

- This is an ***extremely important relation***, and ω_M is referred to as the ***full-power bandwidth***
- It is a ***constant*** for a given op-amp
- This ***derivation*** is for V_0 ***swinging*** between $\pm V_{SAT}$
- If the ***swing*** of V_0 is ***less*** than this, then ω can be ***increased*** beyond ω_M, following the ***relation***:

  $SR = \omega_M V_{SAT} = \omega_0 V_0 = \omega_0 A V_i$

  ω_0: ***Frequency till which V_0 won't have any slew rate limited distortion***

  $\Rightarrow$ ***Maximum amplitude*** of V_i (of ***frequency*** ω_0), beyond which ***slew rate limited distortion*** would ***set in at the output***:

  $V_{i,max} = \omega_M V_{SAT}/(\omega_0 A)$


"That's all Folks!"