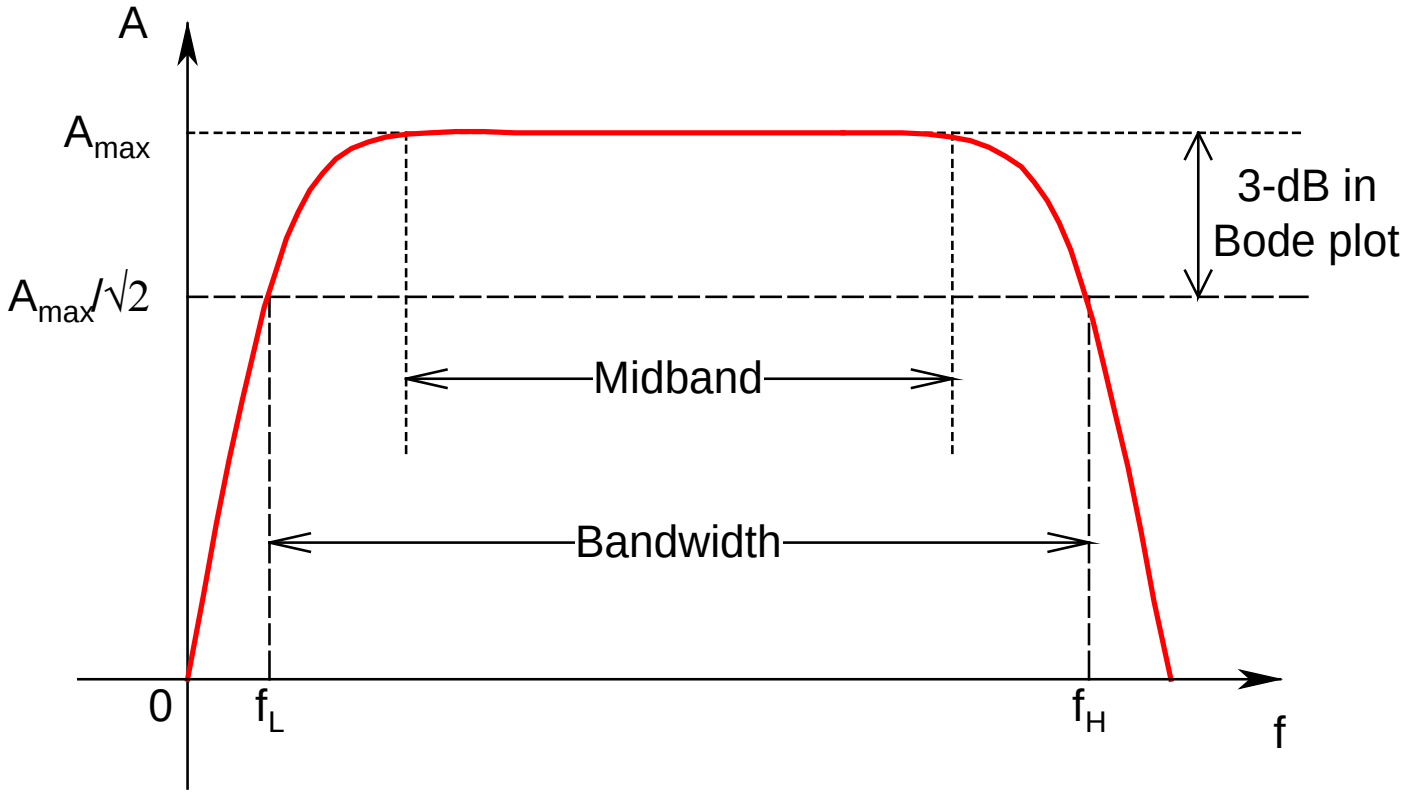
AMPLIFIERS

Outline

- ***Amplification*** of ***ac signals*** (***voltage***, ***current***)
- ***Discrete*** and ***IC***
- ***Single-Stage*** and ***Multi-Stage***
- ***Modular approach***
- Interested in:
  - ***Voltage/Current Gain*** (A_v/A_i)
  - ***Input/Output Resistance*** (R_i/R_0)

Midband Analysis



f_L: Lower Cutoff Frequency

f_H: Upper Cutoff Frequency

Bandwidth = $f_H - f_L$

Single-Stage Topologies

- ***BJT***:
  - ***Common-Emitter*** (CE)
    - ***i/p to B***, ***o/p from C***, ***E common to both i/p and o/p***
  - ***Common-Base*** (CB)
    - ***i/p to E***, ***o/p from C***, ***B common to both i/p and o/p***
  - ***Common-Collector*** (CC)
    - ***i/p to B***, ***o/p from E***, ***C common to both i/p and o/p***
  - ***Common-Emitter (Degeneration)*** [CE(D)]
    - ***Same as CE***, but now with an ***emitter resistance attached***

- ***MOSFET***:
  - ***Common-Source*** (CS)
    - ***i/p to G***, ***o/p from D***, ***S common to both i/p and o/p***
  - ***Common-Gate*** (CG)
    - ***i/p to S***, ***o/p from D***, ***G common to both i/p and o/p***
  - ***Common-Drain*** (CD)
    - ***i/p to G***, ***o/p from S***, ***D common to both i/p and o/p***
  - ***Common-Source (Degeneration)*** [CS(D)]
    - ***Same as CS***, but now with a ***source resistance attached***

- For ***MOSFETs***, an ***additional topology*** possible: ***i/p to Body***, ***o/p from S/D***
  - Known as ***body-driven*** or ***bulk-driven*** stage
- Each of the ***topologies*** has ***specific characteristics*** in terms of ***voltage/current gain*** and ***input/output resistance***
- Each of these will be treated as a ***module***, and will do a ***complete analysis*** for each of these stages

Multi-Stage Topologies

- Also known as ***Compound Connections***
- ***Combination of 2 or more stages***
  - ***A module by itself***
- ***Some widely used topologies***:
  - ***Darlington***
  - ***Cascode***
  - ***Differential Amplifier/Differential Pair*** (DA/DP)

Basic Structure

- Consists of a ***driver*** and a ***load***
- ***Driver***: Universally ***active devices***, e.g., ***BJTs*** or ***MOSFETs***
- ***Load***: Can either be ***resistors*** (***passive***) or ***transistors*** (***active***)
- Generally, ***discrete stages*** have ***passive loads***, while ***IC stages*** have ***active loads***

Resistance Transformation (Only for BJTs)

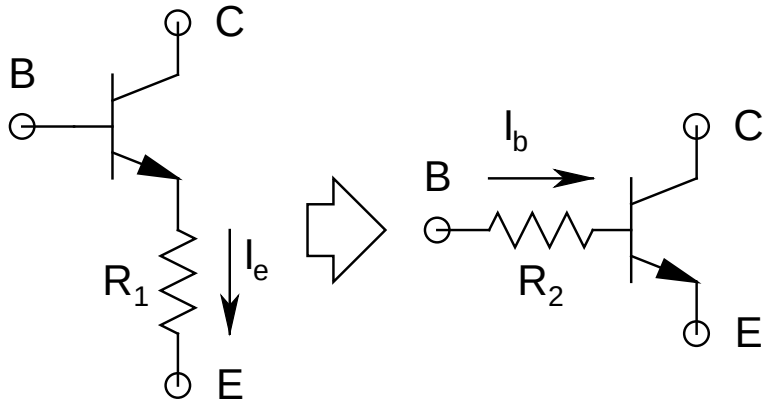
- ***A very useful technique***
- For ***equivalence***:

$$I_b R_2 = I_e R_1$$

$$\Rightarrow R_2 = (\beta + 1) R_1$$

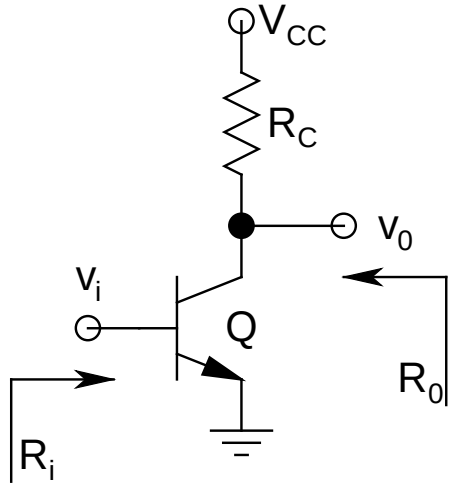
$$\text{or } R_1 = R_2/(\beta + 1)$$

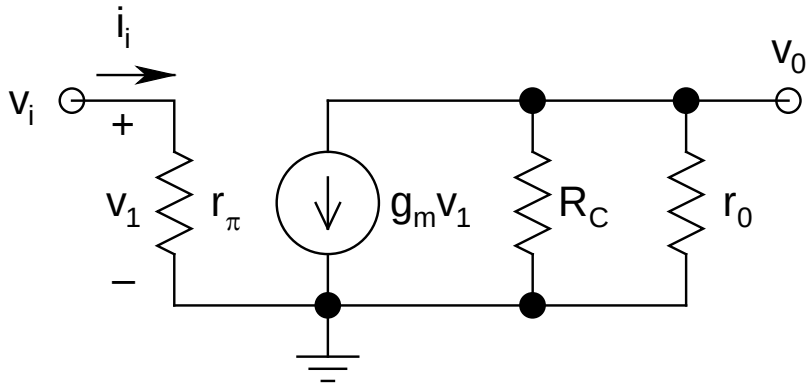
- ***Apply it freely***!



Single-Stage Amplifiers

- ***Common-Emitter*** (CE):





ac Schematic **ac Low-Frequency Equivalent**

➢ ***Biasing circuit not shown***

- By inspection, ***Voltage Gain***:

$$A_v = \frac{v_0}{v_i} = \frac{-g_m v_1 \left(R_C \parallel r_0 \right)}{v_i} = -g_m \left(R_C \parallel r_0 \right)$$

- The ***negative sign*** in front implies ***180° phase shift*** between v_i and v_0
  - ***v_i and v_0 are exactly out of phase***
- For ***discrete circuits***, in general, $R_C << r_0$

  $\Rightarrow A_v = - g_m R_C \approx - R_C / r_E$ (***moderate to large***)
- On the other hand, if $r_0 << R_C$:

  $A_v = - g_m r_0 = - 1/\eta = - V_A / V_T$ (***can be huge***!)
  - ***Theoretical maximum voltage gain of this circuit***

- ***Current Gain***:

  $A_i = i_c/i_b = \beta$ (***large***)

- Thus, ***Power Gain***:

  $PG = A_v \times A_i$ (***very large***)

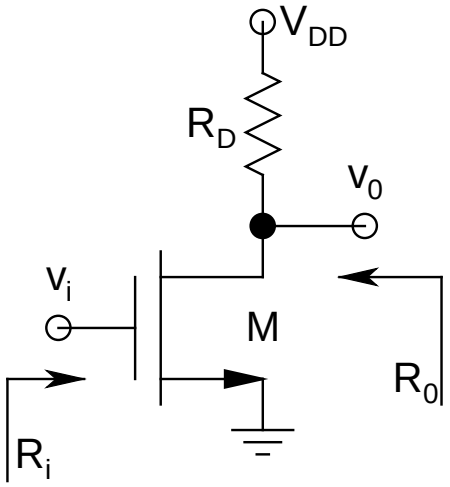
- Therefore, this circuit is ***designers' favorite***!
- Has primary use as ***audio amplifiers***
- ***Input Resistance***:

  $R_i = v_i/i_i = r_\pi$ (***decent***)

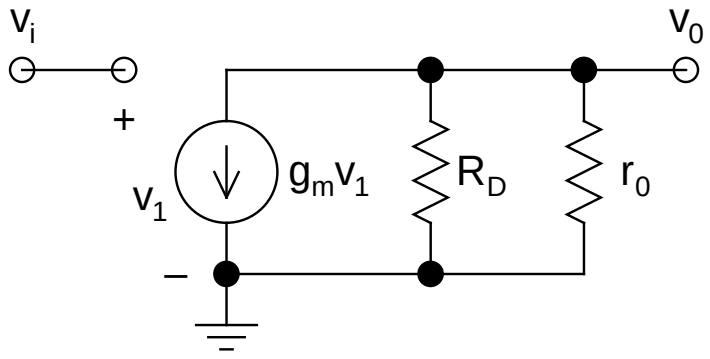
- ***Output Resistance***:

  $R_0 = R_C \| r_0 \approx R_C$

- ***Common-Source*** (CS):



ac Schematic



ac Low-Frequency Equivalent

- ***Biasing circuit not shown***
- ***Body at ground*** $\Rightarrow$ ***No body effect***

- By inspection, ***Voltage Gain***:

$$A_v = \frac{v_0}{v_i} = \frac{-g_m v_1 \left(R_D \| r_0\right)}{v_i} = -g_m \left(R_D \| r_0\right)$$

- The ***negative sign*** in front implies ***180° phase shift*** between v_i and v_0
  - ***v_i and v_0 are exactly out of phase***
- For ***discrete circuits***, in general, $R_D << r_0$

  $\Rightarrow A_v = -g_m R_D$ (***moderate***)
- ***Input Resistance***: $R_i \rightarrow \infty$
- ***Output Resistance***: $R_0 = R_D \| r_0 \approx R_D$
- ***Note the remarkable similarity with CE stage***

- If $R_D >> r_0$:

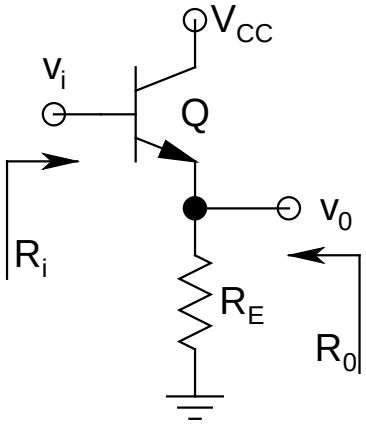
  $A_v = - g_m r_0 = - k_N V_{GT}/(\lambda I_D) = - 2/[\lambda(\Delta V)]$

  (***assuming $\lambda V_{DS} < 0.1$***)

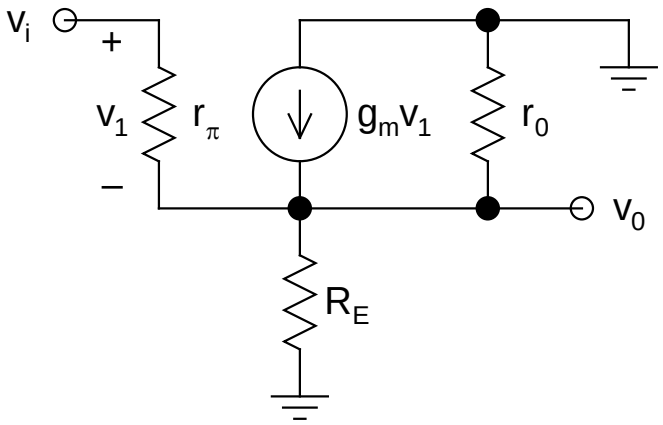
- Thus, ***for small λ and small ΔV, A_v can be large***
  - Keep in mind that ***$\Delta V(min) = 3V_T$***
- Also, $A_v \propto 1/\sqrt{I_D}$

  $\Rightarrow$ ***Lower I_D, higher A_v***
- ***Recall***: For ***CE stage***, A_v(max) was ***independent of I_C***, and ***dependent only on T***

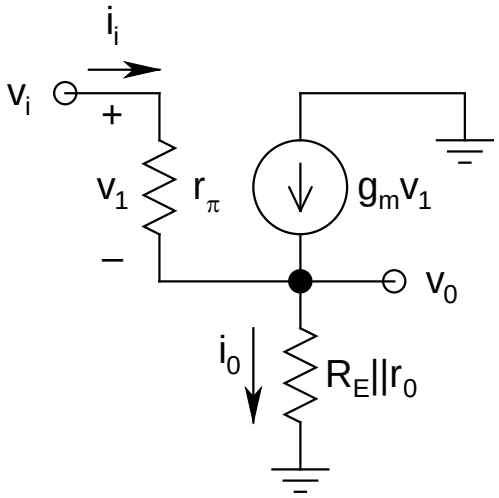
- ***Common-Collector*** (CC):
  - Also known as ***Emitter-Follower***



ac Schematic



ac Low-Frequency Equivalent



Simplified ac Low-Frequency Equivalent

- ***Biasing circuit not shown***

- ***Voltage Gain***:

$$A_v = \frac{v_0}{v_i} = \frac{i_0\left(R_E \parallel r_0\right)}{v_1 + v_0} = \frac{(\beta+1) i_i \left(R_E \parallel r_0\right)}{i_i r_\pi + (\beta+1) i_i \left(R_E \parallel r_0\right)}$$

$$= \frac{R_E \parallel r_0}{r_\pi/(\beta+1) + R_E \parallel r_0} = \frac{R_E \parallel r_0}{r_E + R_E \parallel r_0}$$

- Now, in general, $r_0 >> R_E$

  $\Rightarrow A_v = R_E/(r_E + R_E)$

- ***Two important observations***:
  - $A_v \leq 1$
  - ***No phase shift between v_i and v_0***

- ***Current Gain***:

$A_i = i_e/i_b = \beta + 1$ (***large***)

- ***Input Resistance***:

$$R_i = \frac{v_i}{i_i} = \frac{i_i r_\pi + i_0 \left(R_E \,||\, r_0\right)}{i_i}$$

$$= \frac{i_i r_\pi + \left(\beta + 1\right) i_i \left(R_E \,||\, r_0\right)}{i_i}$$

$$= r_\pi + \left(\beta + 1\right)\left(R_E \,||\, r_0\right)$$

  - If $r_0 >> R_E$, $R_i = r_\pi + (\beta + 1)R_E$

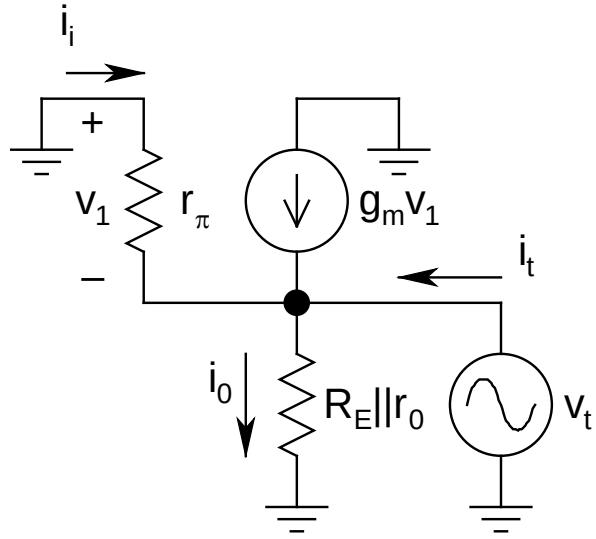
- Note that this result could have been written from ***inspection*** from the ***ac schematic*** using the technique of ***Resistance Transformation***

➢ ***Output Resistance***:

$$i_t = i_0 - g_m v_1 - i_i$$

$$= \frac{v_t}{R_E \,||\, r_0} + g_m v_t + \frac{v_t}{r_\pi}$$

$$\Rightarrow \; R_0 = R_E||r_0||r_E||r_\pi \approx r_E$$

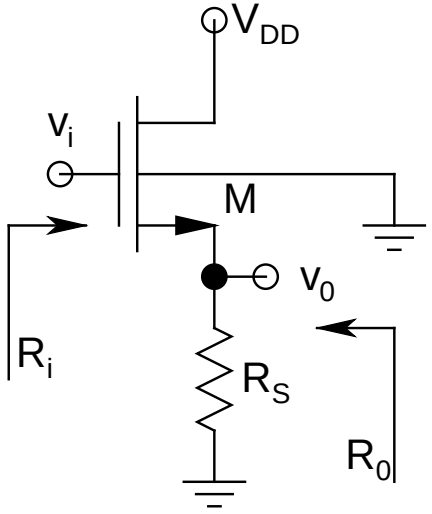


- Note that this expression also could have been written by ***inspection***

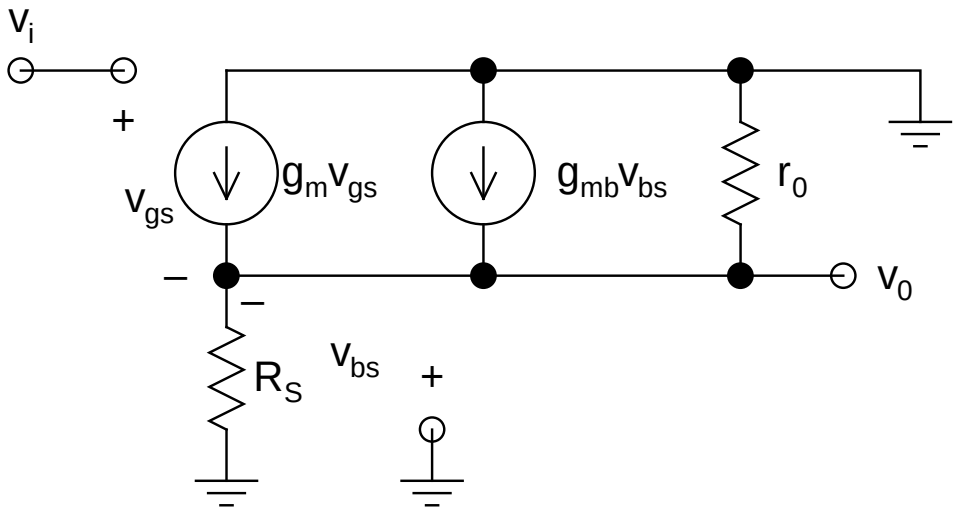
- ***Output excited by a test voltage source v_t***:
  - ***The current has two parallel paths***: ***one going through the parallel combination of r_0 and R_E***, and ***the other into the emitter of Q***
  - The ***resistance in the base lead of Q is r_π***, which ***needs to be transformed to emitter by dividing it by $(\beta+1)$*** $\Rightarrow$ ***yields r_E***
  - Thus, ***R_0 becomes a parallel combination of r_0, R_E, and r_E***, which will be ***typically equal to r_E***, since, in general, ***it's the least among the three***
- ***Understand the inspection technique, it will become immensely useful to analyze circuits***

- ***Some special properties of CC Stage***:
  - $A_v \leq 1$ (***by proper design, it can be made to approach unity very closely***)
  - ***Input and output in phase***
  - ***Quite large input resistance***
  - ***Very small output resistance***
- These properties are ***highly desirable*** to prevent ***loading effect*** of ***cascaded stages*** (to be discussed later)
- Thus, this stage is also known as ***Buffer*** or ***Isolator*** or ***Impedance Matcher***

- ***Common-Drain*** (CD):
  - Also known as ***Source Follower***



ac Schematic



ac Low-Frequency Equivalent

  - ***Biasing circuit not shown***

- ***Note***: ***Body terminal at ground***, but ***source is at a floating potential*** (***it's the output terminal***)

  $\Rightarrow$ ***Body effect will be very much present for M***

  $\Rightarrow$ ***Can be avoided by putting M in its separate island***

- ***Voltage Gain***:
  - ***KCL at output node***:

$$g_m v_{gs} + g_{mb} v_{bs} = v_0/(R_S \| r_0)$$

with $v_{gs} = v_i - v_0$, and $v_{bs} = -v_0$

$$\Rightarrow A_v = \frac{v_0}{v_i} = \frac{g_m (R_S \| r_0)}{1 + (g_m + g_{mb})(R_S \| r_0)}$$

- ***Simplification***:
  - In general, $r_0 >> R_S$:

$$\Rightarrow A_v \simeq \frac{g_m R_S}{1+(g_m+g_{mb})R_S}$$

  - If ***body effect is neglected***:

$$\Rightarrow A_v \simeq \frac{g_m R_S}{1+g_m R_S} = \frac{R_S}{1/g_m + R_S}$$

Note the remarkable similarity with CC stage

  - If $(g_m + g_{mb})R_S >> 1$:

$$\Rightarrow A_v \simeq \frac{g_m}{g_m+g_{mb}} = \frac{1}{1+\chi}$$

- ***Note***:

$$\chi = \frac{\gamma}{2\sqrt{2\phi_F + V_{SB}}}$$

with $V_{SB} = V_0$ (***DC level of v_0***)

- ***Typical values of $\chi \sim 0.1\text{-}0.5$***
- Thus, ***A_v can depart significantly from its ideal value of unity***
- ***No phase shift between input and output***

➢ ***Input Resistance***: $R_i \rightarrow \infty$

➢ ***Output Resistance***: ***By inspection***:

$$R_0 = (g_m + g_{mb} + g_0 + g_S)^{-1} \; (g_0 = 1/r_0, \; g_S = 1/R_S)$$

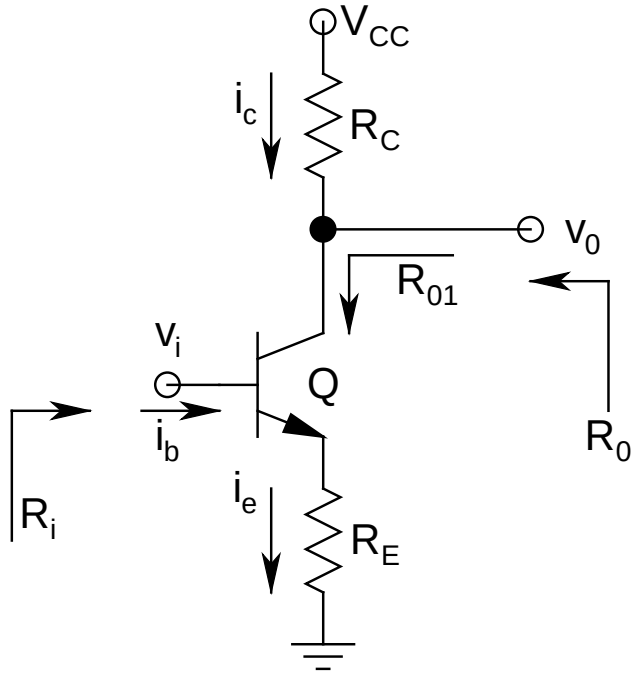
- ***Common-Emitter (Degeneration)*** [CE(D)]:
  - Let's attempt to analyze this circuit by ***inspection***
  - $v_0 = -i_c R_C$

    $v_i = i_e(r_E + R_E)$

    $\Rightarrow \quad A_v = v_0/v_i$

    $\approx -R_C/(r_E + R_E)$

    Piece of cake?
  - $A_i = i_c/i_b = \beta$
  - $R_i = r_\pi + (\beta + 1)R_E = (\beta + 1)(r_E + R_E)$



- $R_0 = R_{01} || R_C$

  Can you identify R_{01} by ***inspection***?

  $R_{01} = r_0[1 + g_m(r_\pi || R_E)]$

  Generally, $R_{01} >> R_C$

  $\Rightarrow R_0 \approx R_C$

- ***Probe A_v further***:

  $A_v = -R_C/(r_E + R_E) \approx -g_m R_C/(1 + g_m R_E)$

  For ***CE stage***, $A_v = -g_m R_C$

  For this stage, A_v is ***lower*** by a ***factor*** $(1 + g_m R_E) \Rightarrow$ ***Gain Degeneration***

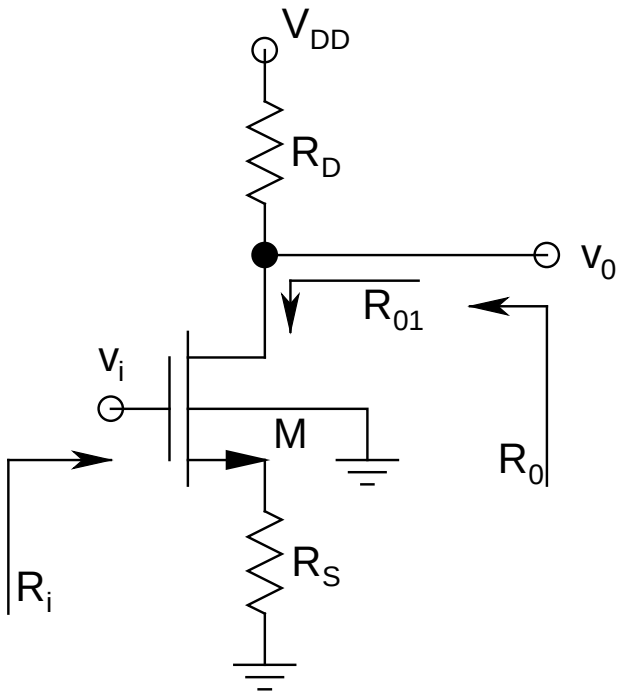
- $(1 + g_m R_E)$ is known as the ***Degeneration Factor***
- R_i can also be written as:

  $R_i \approx r_\pi + \beta R_E = r_\pi(1 + g_m R_E)$

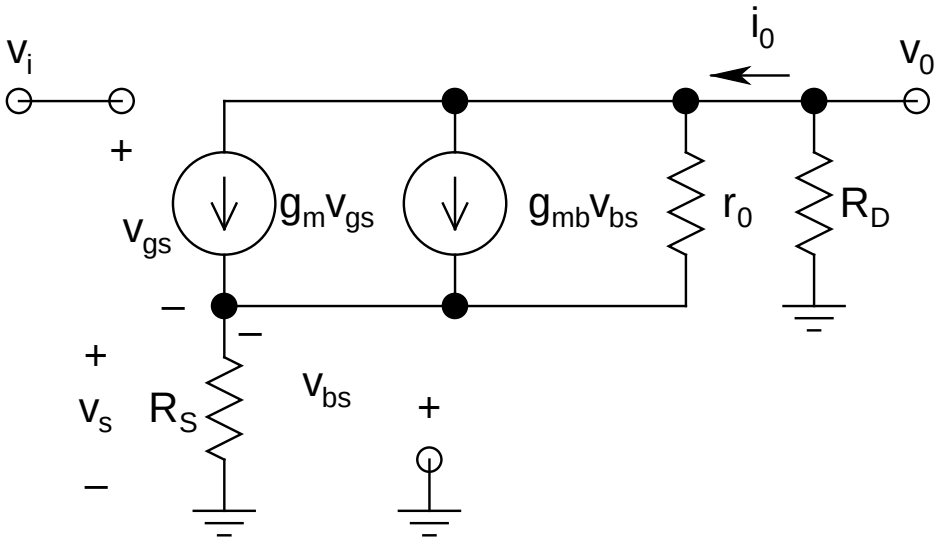
  Thus, $R_i \uparrow$ by the ***Degeneration Factor*** as compared to the ***CE stage***
- ***Interesting to note that the loss in gain is returned by this circuit to its R_i by the same factor***!

- ***Why do we sacrifice gain***?
  - Later on, we will see that this ***sacrifice in gain*** leads to a ***commensurate increase in the bandwidth*** of the circuit
- ***For a given DC bias point***, the ***gain-bandwidth product (GBP) of a circuit remains constant*** (will be explored later)
- This is one of the ***famous paradoxes*** of analog circuits:
  - ***To increase gain, sacrifice bandwidth, and vice versa***

- ***Common-Source (Degeneration)*** [CS(D)]:



ac Schematic



ac Low-Frequency Equivalent

- ***Defining Relations***:

$$v_0 = -i_0 R_D$$

$$i_0 = g_m v_{gs} + g_{mb} v_{bs} + (v_0 - v_s)/r_0$$

$$v_s = i_0 R_S$$

$$v_{gs} = v_i - v_s$$

$$v_{bs} = -v_s$$

$$\Rightarrow A_v = \frac{v_0}{v_i} = -\frac{g_m R_D}{1 + (g_m + g_{mb}) R_S + (R_S + R_D)/r_0}$$

- Pretty ***complicated*** expression, however, ***simplifications*** can be made

- Generally, $(R_S + R_D)/r_0$ can be ***neglected***:

$$\Rightarrow A_v = \frac{v_0}{v_i} \simeq -\frac{g_m R_D}{1+\left(g_m + g_{mb}\right)R_S}$$

- ***Neglect body effect***:

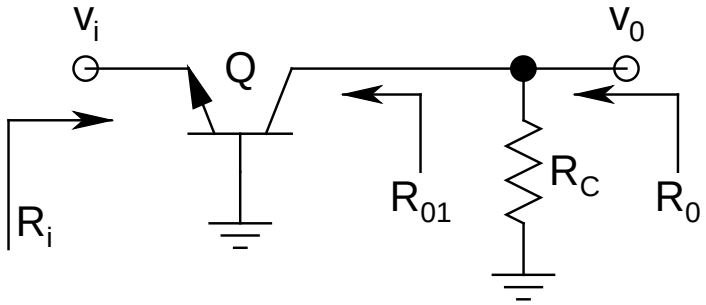
$$\Rightarrow A_v \simeq -\frac{g_m R_D}{1+g_m R_S} = -\frac{R_D}{1/g_m + R_S}$$

- Again, ***remarkable similarity with CE(D) stage***
- ***Golden Observation***:
  - ***MOS stages, in absence of body effect, is absolutely similar to BJT stages, with r_E replaced by $1/g_m$, and both β and $r_\pi \rightarrow \infty$***

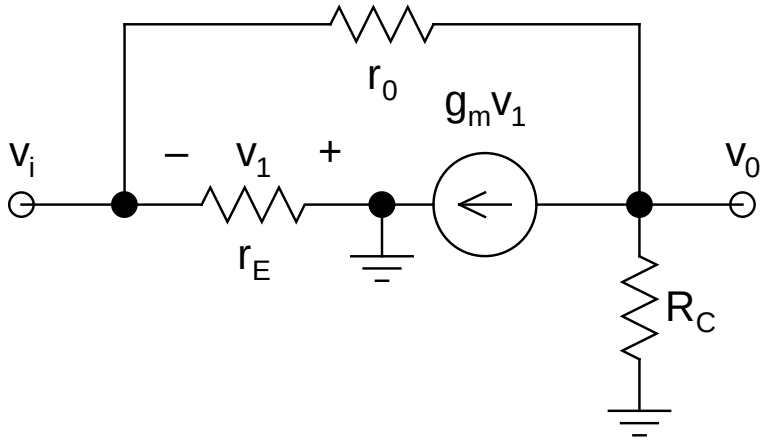
- Note that here the ***Degeneracy Factor*** is $(1 + g_m R_S)$
- $R_i \rightarrow \infty$
- $R_0 = R_{01} \| R_D$

  $R_{01} = r_0[1 + (g_m + g_{mb})R_S]$ (***Show***!)
- Again ***gain is sacrificed*** in order to ***improve the bandwidth*** by the ***same amount***
- The complexity of analysis of this circuit is slightly more than the others encountered so far

- ***Common-Base*** (CB):



ac Schematic



ac Low-Frequency Equivalent

- Note that the ***alternate hybrid-π model appropriate for CB circuit*** has been used
- ***r_0 appears between input and output***

- For now, ***neglect r_0***
- Noting that $v_1 = -v_i$:

$$A_v = \frac{v_0}{v_i} = \frac{-g_m v_1 R_C}{v_i} = +g_m R_C \simeq \frac{R_C}{r_E}$$

- Note that the ***expression*** for A_v is ***identical*** to that for the ***CE stage***, ***without the negative sign in front***
- For this circuit, ***input and output are in phase***
- $A_i = i_c/i_e = \alpha$
- $R_i = r_E$

- $R_0 = R_{01} \| R_C$

  $R_{01} \rightarrow \infty$ (***Why***?)

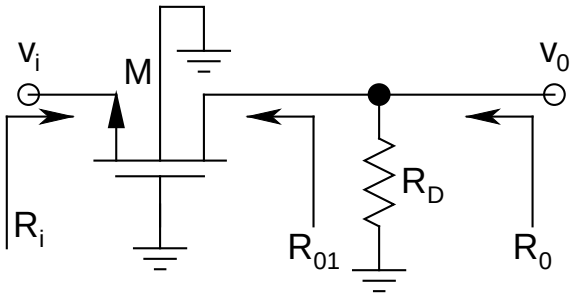
  $\Rightarrow R_0 = R_C$

- ***Ex.: Find A_v and R_i with r_0 included***

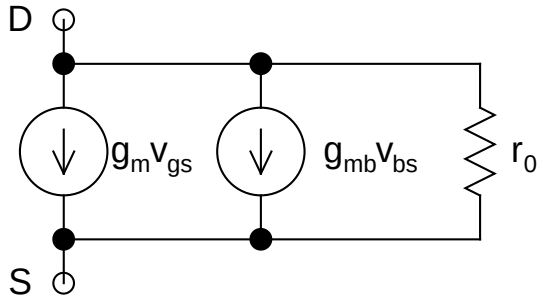
- ***With r_0 included***, the circuit shows ***two different values*** of R_{01}:
  - ***When excited by a voltage source***, $R_{01} = r_0$
  - ***When excited by a current source***, $R_{01} = \beta r_0$ (***Show***)

    [***Hint***: ***For this derivation, need to use $g_m r_E = \alpha$***]
  - ***Thus, possibility of huge R_0 under the second case, but R_C ruins it***!

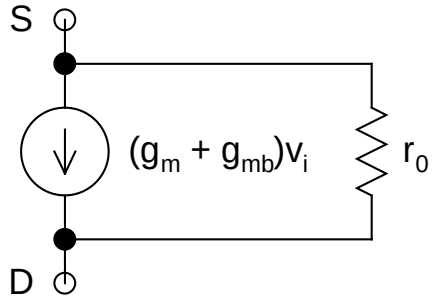
- ***Common-Gate*** (CG):



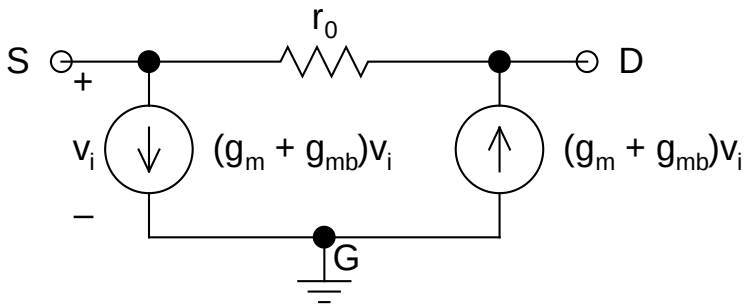
ac Schematic



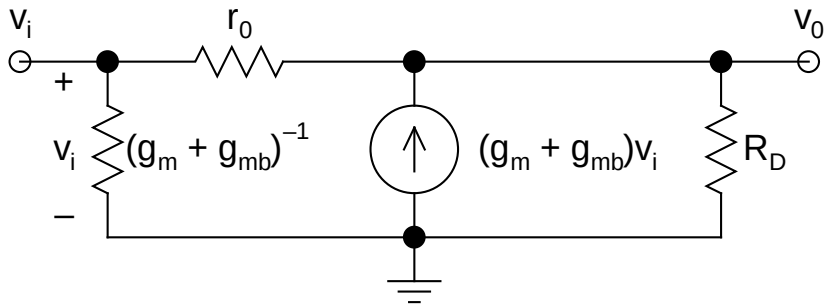
ac Low-Frequency Model for M



Simplified ac Low-Frequency Model for M



Rerouting the current source between S and D to S to G and then from G to D



Final ac Low-Frequency Equivalent for CG Stage

- ***G and B both ground***:

  $\Rightarrow v_{gs} = v_{bs} = -v_i$

  $\Rightarrow g_m v_{gs}$ and $g_{mb} v_{bs}$ can be ***combined to a single current source*** $(g_m + g_{mb})v_i$, ***flowing from S to D***

- ***Reroute this current source from S to G and then from G to D*** (***the circuit remains invariant***)

  $\Rightarrow$ Leads to the ***final ac low-frequency equivalent*** of the CG stage

- ***Note again that r_0 appears between input and output*** (***similar to CB stage***)

- ***Neglect r_0 for now***
- Noting that $v_1 = v_i$:

$$A_v = \frac{v_0}{v_i} = \frac{(g_m + g_{mb}) v_1 R_D}{v_i} = +(g_m + g_{mb}) R_D$$

- ***Identical result to a CB stage***, if ***body effect is neglected***
- $R_i = (g_m + g_{mb})^{-1}$
- $R_0 = R_{01} \| R_D$

  $R_{01} \rightarrow \infty$ (***Why***?)

  $\Rightarrow R_0 = R_D$

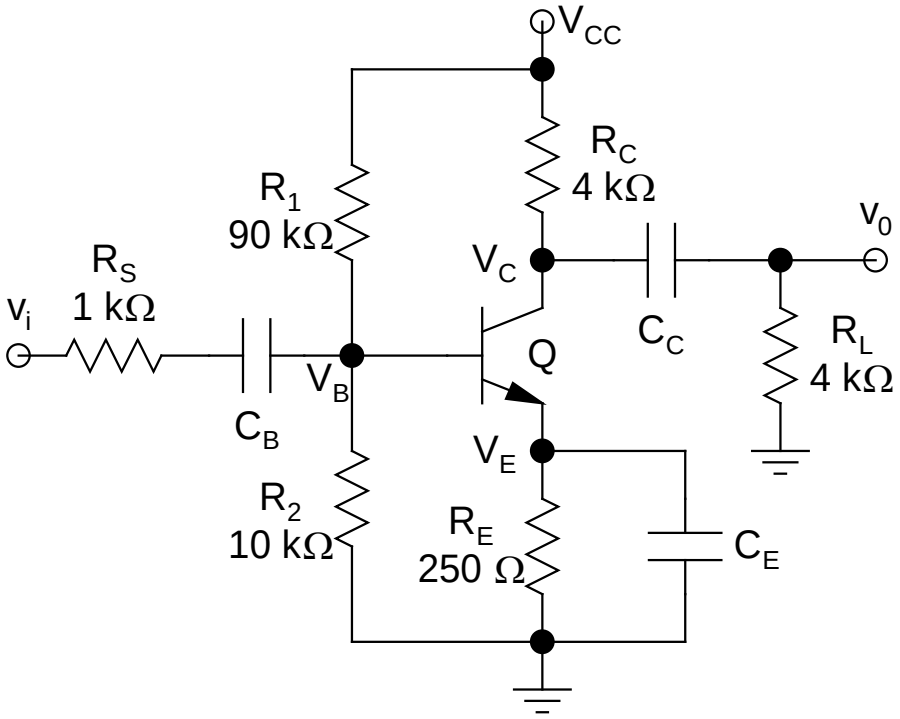
- ***Ex.: Find A_v and R_i with r_0 included***
- ***With r_0 included***, the circuit shows ***three different values*** of R_{01}:
  - ***When excited by a voltage source***, $R_{01} = r_0$
  - ***When excited by an ideal current source***, $R_{01} \rightarrow \infty$ (***Show***)
  - ***If the current source is non-ideal with shunt resistance R_S***:

    $R_{01} = r_0[1 + (g_m + g_{mb})R_S]$ (***Show***)

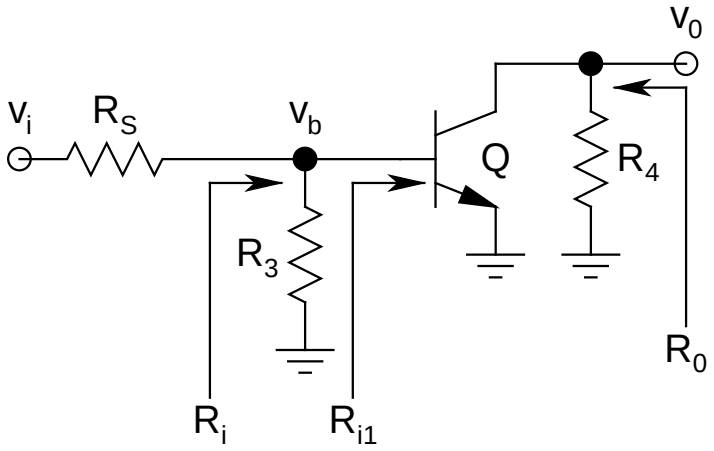
Quick Reckoner for BJT Stages

Topology	A_v	A_i	PG	R_i	R_0
CE	Moderate to Large	Large	Large	Moderate	Moderate
CC	≤ 1	Large	Moderate	Large	Small
CB	Moderate to Large	≤ 1	Moderate	Small	Moderate
CE(D)	Moderate	Large	Moderate	Large	Moderate

- ***The RC-Coupled Amplifier***:
  - ***Immensely popular***, particularly for ***audio circuits***
  - Can be designed to produce ***significant power gain***
  - Several such stages can be ***cascaded*** to produce ***very large gain***
  - Can be used either with ***single-supply*** or ***dual-supply***
  - Used primarily in ***discrete designs*** (***PCB***)

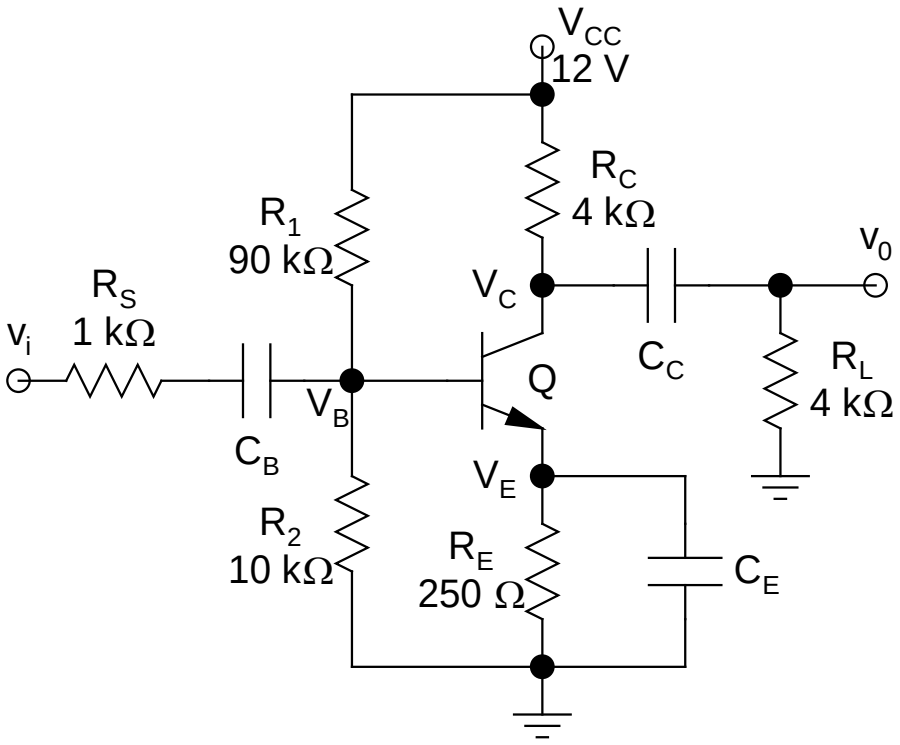


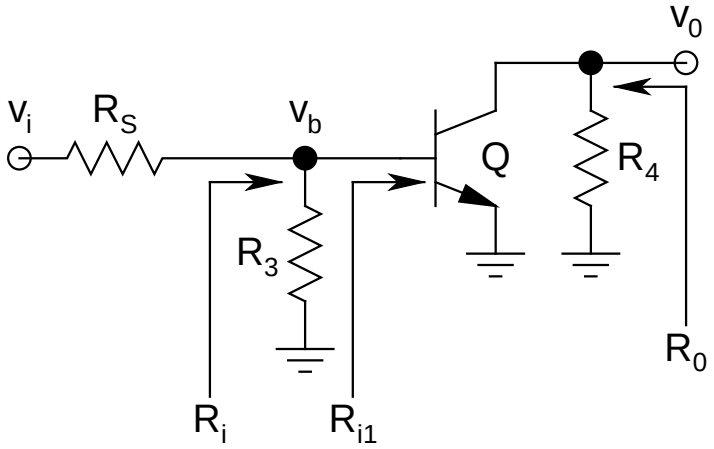
Complete Circuit



ac Schematic

C_B: Base Blocking Capacitor , C_C: Collector Coupling Capacitor
C_E: Emitter Bypass Capacitor , R_S: Source Resistance , R_L: Load Resistance





Complete Circuit

ac Midband Schematic

C_B: Base Blocking Capacitor , C_C: Collector Coupling Capacitor
C_E: Emitter Bypass Capacitor , R_S: Source Resistance , R_L: Load Resistance

- C_B,C_C: Used for ***DC isolation*** of the ***bias circuit*** from ***the source and the load***
  - ***DC biasing becomes independent of source and load***
- C_E: ***Plays no role in DC*** (***opens up***), but ***shorts out R_E in ac*** (will see its effects later)
- These 3 capacitors dictate the ***lower cutoff frequency*** (f_L) of the circuit
- Typically have values in the order of ***μF to 100s of μF*** in order to give ***f_L as close to 0*** (***DC***) as possible

- First need to do the ***DC analysis*** to find the ***operating point***
- ***All capacitors open up for DC analysis***
  - ***R_S and R_L play no role***
- ***Neglecting base current***:

$V_B = V_{CC}R_2/(R_1 + R_2) = 1.2$ V

$\Rightarrow V_E = V_B - V_{BE} = 0.5$ V

$\Rightarrow I_E \approx I_C = V_E/R_E = 2$ mA

$V_C = V_{CC} - I_C R_C = 4$ V

$V_{CE} = 3.5$ V (***quite close to $V_{CC}/3$***)

- ***DC bias point analysis done***!

- Now we can move on to the ***ac analysis***
- ***All capacitors get shorted*** due to their ***high values***, assuming ***frequency of operation*** is ***beyond f_L*** and ***less than f_H***, i.e., ***midband range***
- ***C_E bypasses R_E***

  $\Rightarrow$ ***Emitter of Q goes to ground***

  $\Rightarrow$ ***R_E plays no role in ac analysis***
- ***Refer to the ac schematic***
  - $R_3 = R_1 \| R_2 = 9\ k\Omega$
  - $R_4 = R_C \| R_L = 2\ k\Omega$
- ***Need β for ac analysis*** (***choose 100***)

- $r_E = V_T/I_C = 13\ \Omega$, and $r_\pi = \beta r_E = 1.3\ k\Omega$
- $R_{i1} = r_\pi = 1.3\ k\Omega$
- $R_i = R_{i1} \| R_3 = 1.14\ k\Omega$
- Total resistance ***seen*** by $v_i = R_S + R_i = 2.14\ k\Omega$
- For calculation of ***voltage gain*** A_v, apply ***chain rule***:

$A_v = v_0/v_i = (v_0/v_b) \times (v_b/v_i)$

$v_0/v_b = - R_4/r_E = - 153.85$ (***CE stage***)

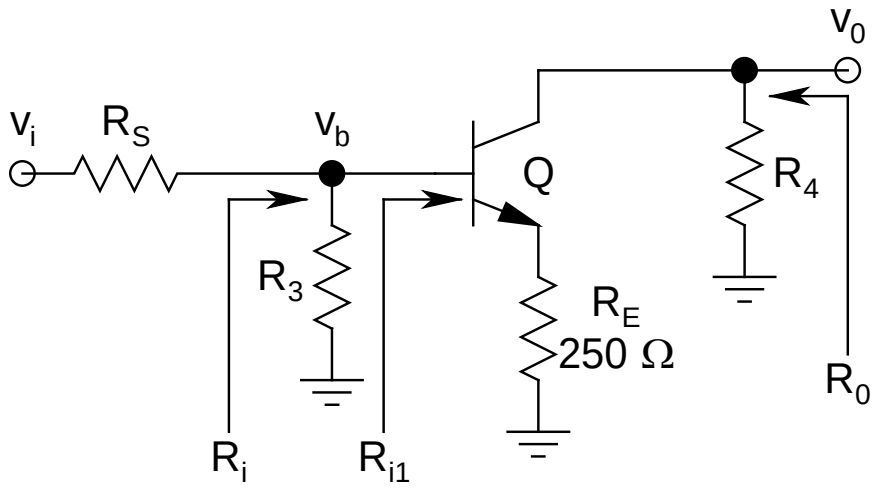
$v_b/v_i = R_i/(R_i + R_S) = 0.533$

$\Rightarrow A_v = - 82$ (***Very Good Gain***!)

- Note that v_i and v_0 are ***exactly out of phase***, which is expected from a ***CE stage***
- $R_0 = r_0 \| R_4 \approx R_4 = 2\ k\Omega$

  (since for ***discrete circuits***, r_0 is generally ***neglected***)
- ***This completes the analysis of the stage***
- ***Summary***:
  - $A_v = -82$
  - $R_i = 1.14\ k\Omega$
  - Resistance ***seen*** by $v_i = 2.14\ k\Omega$
  - $R_0 = 2\ k\Omega$

- Now let's explore what happens if ***C_E were absent***, i.e., ***R_E unbypassed***
- Redraw the ***ac schematic***:

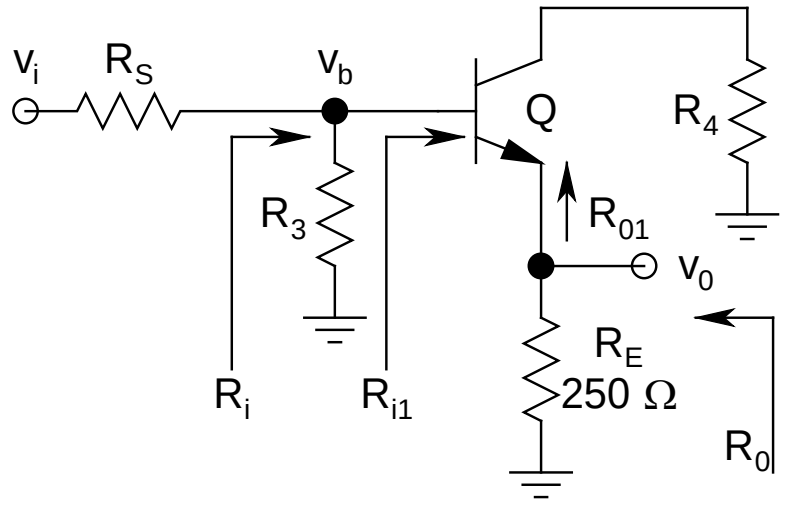


ac Midband Schematic for R_E unbypassed

- ***Note***: ***Degeneration Factor*** = $(1 + g_m R_E) \approx (1 + R_E/r_E) = 20.23$
- $R_{i1} = r_\pi + (\beta + 1)R_E = 26.55\ k\Omega$
  - ***Exactly 20.23 times of the previous case*** (1.3 kΩ)
- $R_i = R_{i1} \| R_3 = 6.72\ k\Omega$
- Total resistance ***seen*** by $v_i = R_S + R_i = 7.72\ k\Omega$
- $v_0/v_b = -R_4/(r_E + R_E) = -7.6$ [***CE(D) Stage***]
  - ***Reduced by exactly 20.23 times of the previous case*** (– 153.85)
- $v_b/v_i = R_i/(R_i + R_S) = 0.87$
  - ***Improvement as compared to previous case*** (0.533)

- $A_v = -6.6$
  - ***Compare with −82 obtained in previous case*** (***significant reduction***)
- $R_0 \approx R_4 = 2\ k\Omega$ (***if r_0 is neglected***)
- ***If r_0 is considered, analysis becomes significantly complicated, since the Golden Rule can't be applied due to the presence of resistance*** (***apart from r_π***) ***in the base of Q***
- ***Summary***:
  - $A_v = -6.6$
  - $R_i = 6.72\ k\Omega$
  - Resistance ***seen*** by $v_i = 7.72\ k\Omega$
  - $R_0 = 2\ k\Omega$

- ***What if the output is taken from emitter***?
- Redraw the ***ac schematic***:



ac Midband Schematic for Output Taken from Emitter

- ***R_4 actually redundant for this case*** (***collector of Q could have been connected to V_{CC} directly***)
- R_{i1} = 26.55 kΩ, R_i = 6.72 kΩ, and resistance ***seen*** by v_i = 7.72 kΩ (***same as before***)
- $v_0/v_b = R_E/(r_E + R_E) = 0.95$ (***CC Stage***)
- $v_b/v_i = R_i/(R_i + R_S) = 0.87$ (***same as before***)
- A_v = 0.827 (<1, as expected, but ***could have been made closer to unity by better design***!)
- $R_0 = R_E \| R_{01}$
- ***Computation of R_{01} is slightly more involved***, ***but quite easy if the trick is understood***!

- ***First, short v_i to ground***

  $\Rightarrow$ ***R_3 comes in parallel with R_S (call this combination R_5)***

  $\Rightarrow R_5 = R_3 \| R_S = 900\ \Omega$

- ***R_5 comes in series with r_π (call this combination R_6)***

  $\Rightarrow R_6 = R_5 + r_\pi = 2.2\ k\Omega$

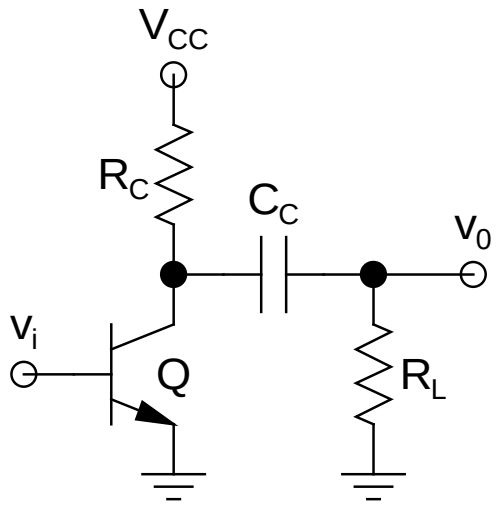
- ***Transform R_6 to emitter by dividing it by (β +1)***

  $\Rightarrow R_{01} = R_6/(\beta + 1) = 21.8\ \Omega$

- Thus, $R_0 = 20\ \Omega$ (***Easy***?)
- ***Summary***:
  - $A_v = 0.827$
  - $R_i = 6.72\ k\Omega$
  - Resistance ***seen*** by $v_i = 7.72\ k\Omega$
  - $R_0 = 20\ \Omega$
- Thus, this circuit has ***voltage gain close to unity***, ***ok input resistance***, and ***very small output resistance***
  - ***Ideal characteristics*** needed for a ***Buffer***/***Isolator***/ ***Impedance Matcher***

- ***Loading Effect***:
  - ***Neglecting r_0***:

    $A_v = -g_m(R_C \| R_L)$
  - ***R_L has no role in DC biasing, but comes into picture in ac calculations***
  - As $R_L \downarrow \Rightarrow |A_v| \downarrow$
    - Known as ***Loading Effect***
  - Similar situation happens when a ***high output resistance driver*** drives a ***low input resistance load*** (e.g., ***CE stage driving a CB stage***)



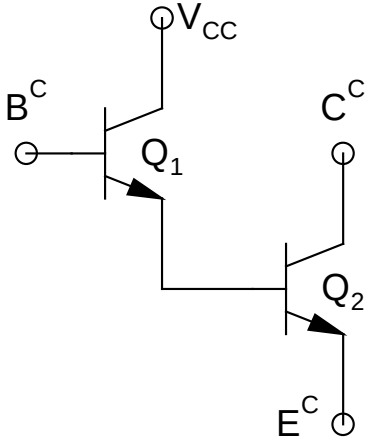
- The ***gain of the CE stage*** will be ***severely compromised*** due to ***low input resistance*** of the ***CB stage***
  - Known as ***Impedance Mismatch*** between ***Driver and Load***
- Under such a situation, need an ***Isolator***/***Buffer***/ ***Impedance Matcher*** between the two stages
- A ***CC stage perfectly fits the bill*** due to its ***high input resistance*** and ***low output resistance***, and ***can be used to couple the CE stage to CB stage***
- ***MOS circuits generally don't have this problem***

Compound Connections

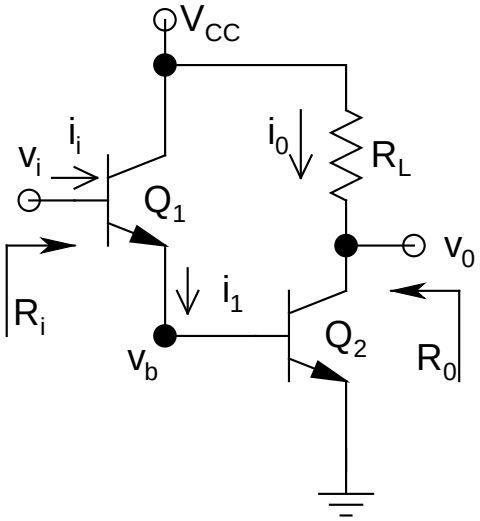
- ***Multi-Stage***
- Have some ***special properties***
- ***Popular Topologies***:
  - ***Darlington***
  - ***Cascode***
  - ***DP*** (or ***DA***)
- ***Modules by themselves***

- ***Darlington***:
  - Cascade of a ***CC*** stage, followed by either a ***CE*** or a ***CC*** stage
  - ***Two biggest advantages***:
    - ***Extremely large R_i***
    - ***Extremely large A_i***
  - ***These two advantages are automatic for MOS stages***

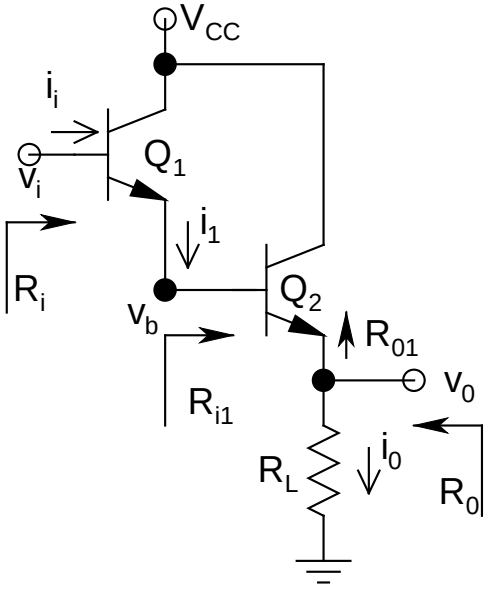
    $\Rightarrow$ ***MOS Darlington has no special use***



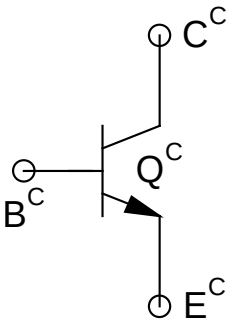
Generic Circuit



CC-CE Stage



CC-CC Stage



Compact Representation

- For ***DC biasing***:

$$I_{C2} = \beta_2 I_{B2} = \beta_2 I_{E1} \approx \beta_2 I_{C1}$$

$$\Rightarrow r_{\pi 2} = \beta_2 r_{E2} = \beta_2 V_T / I_{C2} = V_T / I_{C1} = r_{E1}$$

- For ***ac analysis***:

  CC-CE:

  - $i_1 = (\beta_1 + 1)i_i$ and $i_0 = \beta_2 i_1 = \beta_2(\beta_1 + 1)i_i$

    $\Rightarrow A_i = i_0/i_i = \beta_2(\beta_1 + 1) \approx \beta^2$ (***Huge***!)
  - $R_i = r_{\pi 1} + (\beta_1 + 1)r_{\pi 2} \approx 2r_{\pi 1}$
    - I_{C2} ~ mA, I_{C1} ~ 10s of μA, r_{E1} ~ kΩ, $r_{\pi 1}$ ~ 100s of kΩ (***Huge***!)
  - $v_0/v_b = -R_L/r_{E2}$ and $v_b/v_i = r_{\pi 2}/(r_{\pi 2} + r_{E1}) = 1/2$

    $\Rightarrow A_v = v_0/v_i = -R_L/(2r_{E2})$ (***Moderate***)
  - $R_0 = R_L \| r_{02} \approx R_L$ (***Moderate***)

- Thus, this stage has ***huge A_i and R_i***, and ***moderate A_v and R_0***

- For ***ac analysis***:

  CC-CC:

  - $i_1 = (\beta_1 + 1)i_i$ and $i_0 = (\beta_2 + 1)i_1 = (\beta_2 + 1)(\beta_1 + 1)i_i$

    $\Rightarrow A_i = i_0/i_i = (\beta_2 + 1)(\beta_1 + 1) \approx \beta^2$ (***Huge***!)
  - $R_i = r_{\pi 1} + (\beta_1 + 1)(\beta_2 + 1)(r_{E2} + R_L)$

    $\approx r_{\pi 1} + \beta^2(r_{E2} + R_L)$ (***Astronomical***!)
  - $R_{i1} = r_{\pi 2} + (\beta_2 + 1)R_L$
  - $v_0/v_b = R_L/(R_L + r_{E2})$
  - $v_b/v_i = R_{i1}/(r_{E1} + R_{i1})$
  - $A_v = v_0/v_i \approx \beta_2 R_L/(2r_{E1} + \beta_2 R_L)$ (***Show***!)

- Thus, this stage has ***extremely large A_i and R_i***, and ***A_v is ≤ 1 with no phase shift***

- $R_0 = R_L \| R_{01}$

  $R_{01} = r_{E2} + r_{E1}/(\beta_2 + 1)$ (***by inspection***)

  $\approx 2r_{E2}$

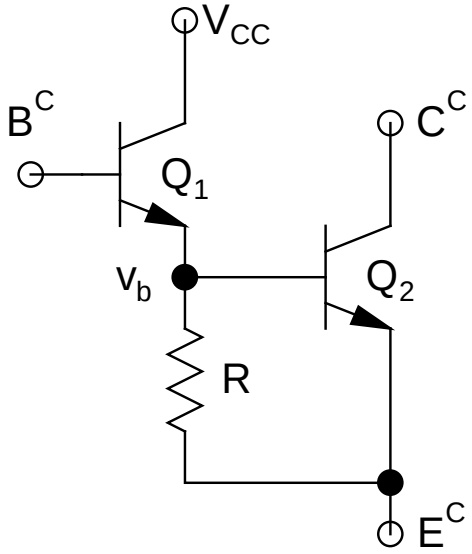
  $\Rightarrow R_0 \approx R_L \| (2r_{E2})$ (***Small***)

- Above analysis is ***pretty straightforward***, and ***assumes that both β_1 and β_2 are high***

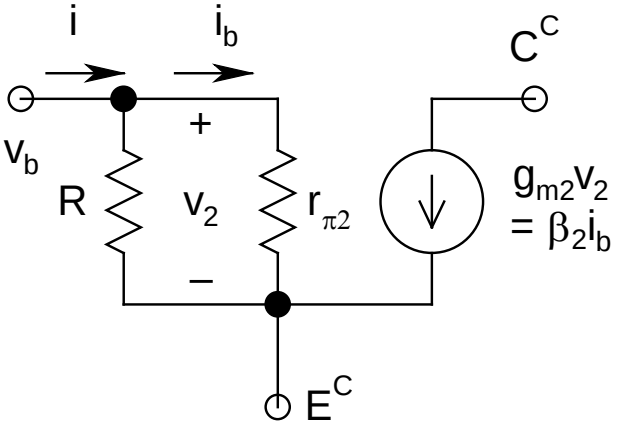
- ***In reality, Q_1 operates with a very low value of I_C*** (~ ***10s of μA***)

  $\Rightarrow$ ***β_1 would drop significantly from its nominal value*** $\Rightarrow$ ***Full advantage of the circuit can't be exploited***

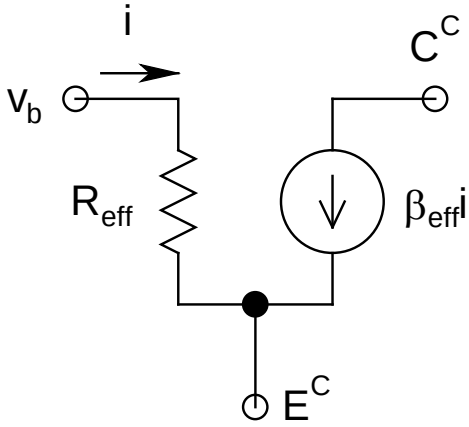
- ***Need to jack up β_1***
  - ***How about using a keep-alive resistor*?**



Darlington with Keep-Alive Resistor R



ac Midband Equivalent of Q_2-R Combination



Simplified Equivalent of Q_2-R Combination

- ***R drains a constant DC current of ~ 0.7/R***
- ***This current is supplied by Q_1, along with I_{B2}***

  $\Rightarrow I_{C1}\uparrow \Rightarrow \beta_1\uparrow$
- ***However, this technique also changes β_2***
- ***Analysis***:

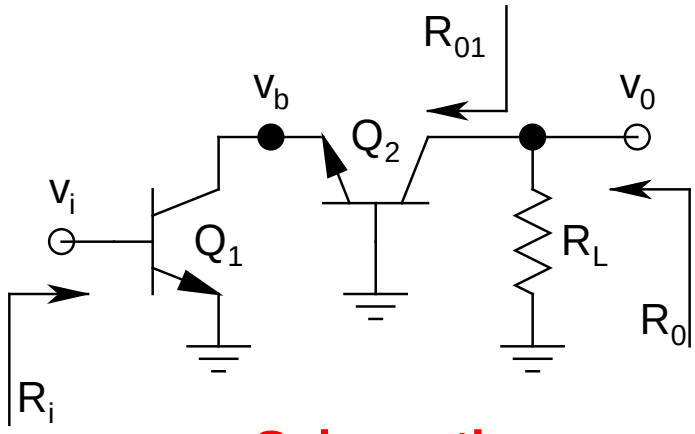
  $i_b = Ri/(R + r_{\pi 2})$

  $\Rightarrow i_c = \beta_2 i_b = \beta_2 Ri/(R + r_{\pi 2}) = g_{m2} r_{\pi 2} Ri/(R + r_{\pi 2})$

  $= g_{m2}(R \| r_{\pi 2})i = g_{m2} R_{eff} i = \beta_{eff} i$

  $\beta_{eff} = g_{m2} R_{eff} < \beta_2 \qquad (R_{eff} = R \| r_{\pi 2})$
- ***Note***: $r_{E2,eff} = R_{eff}/\beta_{eff} = 1/g_{m2} = r_{E2}$ (***unchanged***)

- ***npn Cascode***:
  - ***CE***, followed by ***CB***
  - Known as ***Wideband Amplifier***, due to its ***superior frequency response characteristic***



ac Schematic

  - ***Generally, both Q_1 and Q_2 are biased with the same I_C***
  - ***Assuming Q_1-Q_2 have same β***:

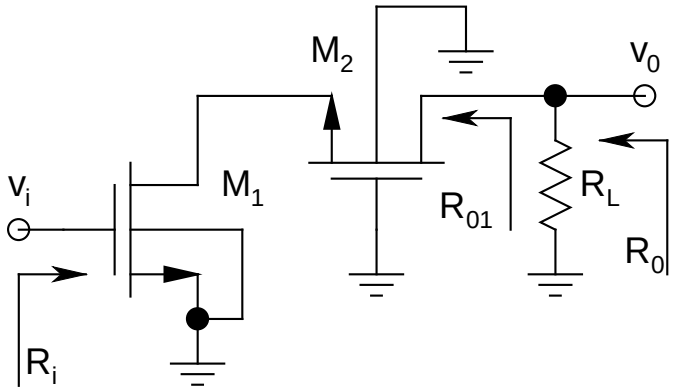
    $r_{E1} = r_{E2} = r_E$ and $r_{\pi 1} = r_{\pi 2} = r_\pi$

- ***This circuit can be analyzed by inspection***
- $R_i = r_{\pi 1}$
- $v_0/v_b = +g_{m2}R_L = R_L/r_{E2}$ (***CB Stage***)
- $v_b/v_i = -r_{E2}/r_{E1} = -1$
  - ***CE Stage with R_i of Q_2 (= r_{E2}) as its load***
- Thus, $A_v = v_0/v_i = -R_L/r_{E2}$
- ***Note that A_v is same as that for a CE stage, however, the bandwidth of this circuit is far superior than a CE stage***

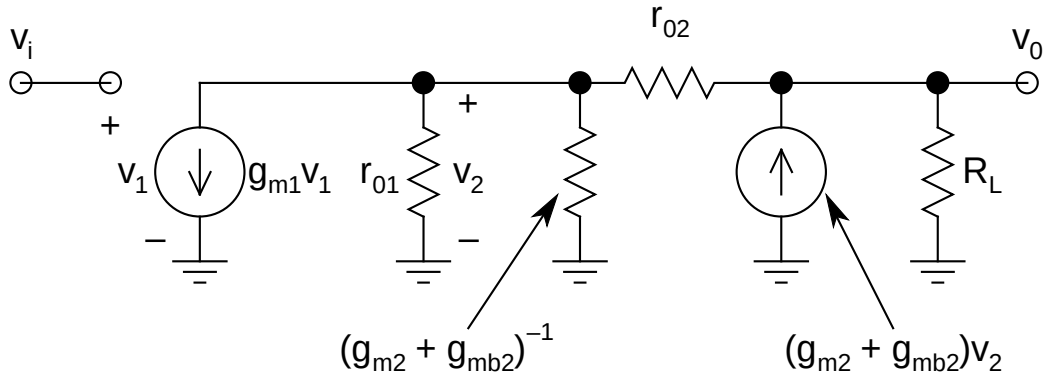
- $R_0 = R_L || R_{01}$
- ***If r_0 is neglected***, then $R_{01} \rightarrow \infty$
- ***If r_0 is included***, then $R_{01} = \beta r_{02}$ (***very high***)
- However, ***it comes in parallel with R_L***

  $\Rightarrow$ ***Overall R_0 is still ~ R_L***
- ***Summary***:
  - ***Moderate voltage gain***
  - ***Moderate input resistance***
  - ***Potential of having very large output resistance***
  - ***Extremely large bandwidth***
  - ***Preferred over a simple CE stage***

- ***NMOS Cascode***:



ac Schematic



ac Midand Equivalent

- ***CS***, followed by ***CG***
- ***Generally, both M_1 and M_2 are biased with the same I_D***
- ***M_1 does not have body effect, but M_2 has***

- ***By inspection***, $R_i \rightarrow \infty$ and $R_0 = R_L \| R_{01}$
- ***With r_{02} present, the analysis becomes a little complicated*** $\Rightarrow$ ***neglect r_{02}*** $\Rightarrow R_0 = R_L$
- ***Neglecting r_{02}***:

$$v_0 = (g_{m2} + g_{mb2}) v_2 R_L$$

$$v_2 = - g_{m1} v_1 / (g_{m2} + g_{mb2} + g_{01}) \quad (g_{01} = 1/r_{01})$$

$$\approx - g_{m1} v_1 / (g_{m2} + g_{mb2})$$

[since, in general, $g_{01} << (g_{m2} + g_{mb2})$]

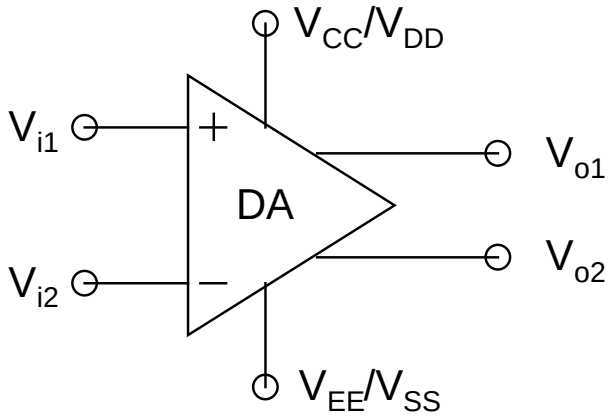
$$\Rightarrow A_v = v_0 / v_i = - g_{m1} R_L \text{ (since } v_1 = v_i)$$

- ***This is same as the CS stage, however, here broad-banding is happening***!

- ***A_v gets affected a little if r_{01} and r_{02} were included***
- ***Since r_{01} comes in parallel with $(g_{m2} + g_{mb2})^{-1}$, its effect on A_v is less pronounced than that of r_{02}***
- ***By inspection***:

  $R_{01} \approx (g_{m2} + g_{mb2})r_{01}r_{02}$ (***Show***!)
- ***Note that if either of r_{01} or $r_{02} \rightarrow \infty$, $R_{01} \rightarrow \infty$*** (***Why***?)

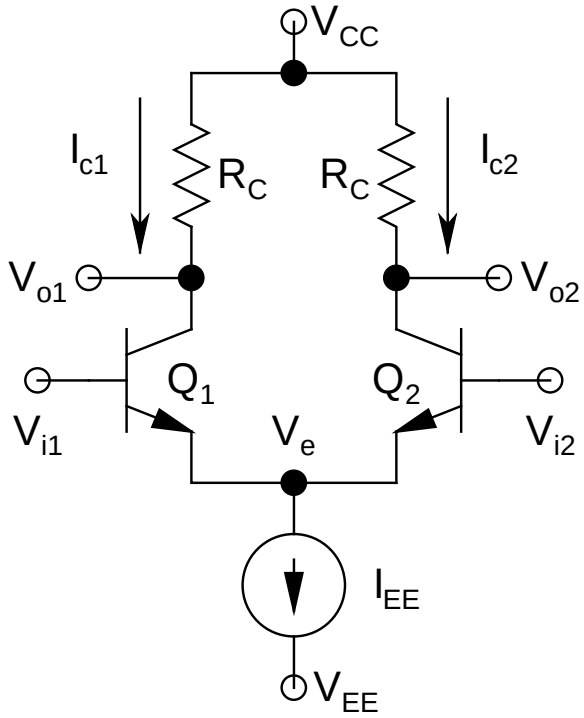
- ***Differential Amplifier (DA)/Differential Pair (DP)***:
  - ***Most versatile analog building block***
  - ***Immensely useful and widely used*** (particularly for ***sensing***/***telemetry***/ ***instrumentation*** applications)
  - ***Two inputs*** (V_{i1}, V_{i2})/***Two outputs*** (V_{o1}, V_{o2})
  - ***Dual Supply*** (V_{CC}/V_{DD}, V_{EE}/V_{SS})



Symbol for DA

- ***Unique Property***:
  - ***Amplifies the difference between V_{i1} and V_{i2}, while rejecting/suppressing signals common to both V_{i1} and V_{i2}***
  - ***Very efficient noise suppressor***
- ***The stage can be direct coupled to the next stage without the need for any coupling capacitor***
- In ***BJT technology***, known as ***Emitter-Coupled Pair*** (***ECP***)
- In ***MOS technology***, known as ***Source-Coupled Pair*** (***SCP***)

- ***npn DA (ECP)***:
  - Q_1-Q_2 constitute a a ***matched pair***, and have their ***emitters connected together***, hence, the name
  - I_{EE}: ***DC bias current source***
  - ***All voltages and currents*** (***apart from those used for biasing***) are ***instantaneous*** (***DC + ac***)



npn DA Topology

- $V_{be1} = V_{i1} - V_e$, and $V_{be2} = V_{i2} - V_e$
- ***KVL around Q_1-Q_2 BE loop***:

  $V_{i1} - V_{be1} + V_{be2} - V_{i2} = 0$

  $\Rightarrow\ V_{be1} - V_{be2} = V_{i1} - V_{i2} = V_{id}$

  V_{id}: ***Differential-Mode Input Voltage***
- ***Neglecting Early effect***:

  $V_{id} = V_T \ln(I_{c1}/I_{c2})$

  $\Rightarrow\ I_{c1}/I_{c2} = \exp(V_{id}/V_T)$ (1)
- ***Neglecting base currents***:

  $I_{c1} + I_{c2} = I_{EE}$ (***always***!) (2)

  This is because I_{EE} is an ideal current source

- ***Solving Eqs.(1) and (2)***:

$$I_{c1} = I_{EE}/[1 + \exp(-V_{id}/V_T)]$$

$$I_{c2} = I_{EE}/[1 + \exp(V_{id}/V_T)]$$

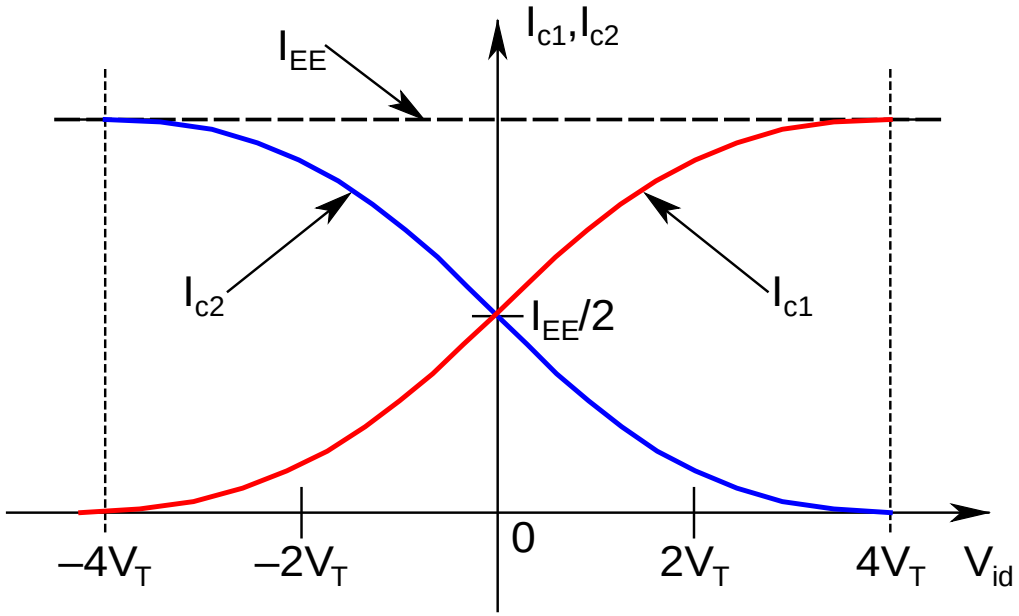
- ***Extremely interesting results***:
  - ***For $V_{id} = 0$, $I_{c1} = I_{c2} = I_{EE}/2$***

    I_{EE} shared equally between Q_1 and Q_2
  - ***For positive V_{id}, $I_{c1}\uparrow$ and $I_{c2}\downarrow$***

    For negative V_{id}, $I_{c1}\downarrow$ and $I_{c2}\uparrow$

    But for both cases, their sum is constant and equal to I_{EE}
  - ***For $V_{id} > 4V_T$, $I_{c1} \rightarrow I_{EE}$*** and ***$I_{c2} \rightarrow 0$***

    For –ve V_{id}, with $\lvert V_{id}\rvert > 4V_T$, $I_{c2} \rightarrow I_{EE}$ and ***$I_{c1} \rightarrow 0$***



The Current Transfer Characteristics of an npn DA

- ***Linear Range*** of the circuit ~ $\pm 4V_T$ (~ ***±100 mV at room temperature***)
- This range is known as the ***analog domain***

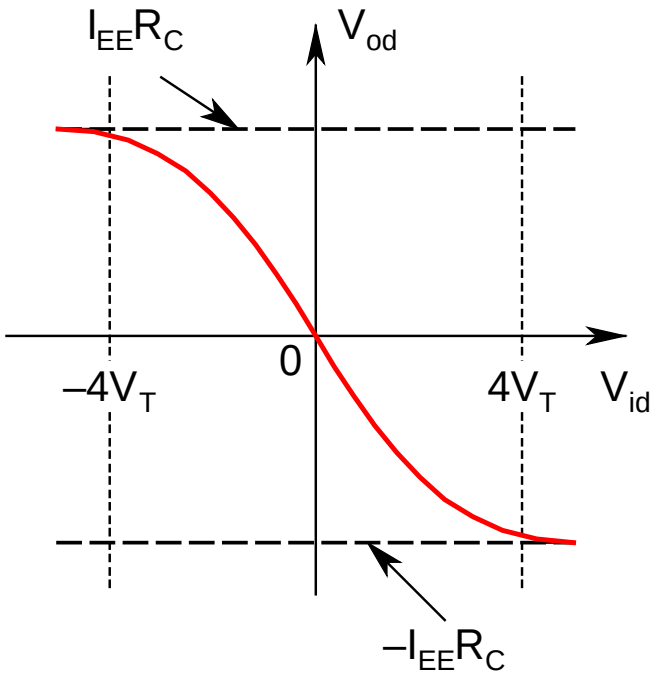
- ***For V_{id} out of this range, either Q_1 or Q_2 carries the entire I_{EE}, with the other remaining off*** $\Rightarrow$ acts as a ***Current Switch***
  - This is the ***digital domain***
- ***For analog applications, both devices must be on and in the linear range of the I_c-V_{id} characteristic***
- ***The highest linearity, which is also the region of the highest g_m ($= \partial I_c/\partial V_{id}$), occurs around $V_{id} = 0$ ($V_{i1} = V_{i2}$)***
- ***This is the most preferred DC bias point***

- ***At this point, $I_{C1} = I_{C2} = I_{EE}/2$, and all small-signal parameters of Q_1 and Q_2 are identical to each other***
- ***This particular biasing scheme leads to a Balanced DA, having properties:***
  - ***Q_1-Q_2 completely matched***
  - ***R_Cs identically equal to each other***
  - ***Both inputs connected to DC ground or to the same DC potential (ground is the best choice, obviously)***
  - ***Both Q_1 and Q_2 biased at $I_{EE}/2$***
- ***We will consider only Balanced DAs***

- ***Unbalanced DAs create anomalies in circuit operation***
- Now, the ***output voltages***:

  $V_{o1} = V_{CC} - I_{c1}R_C$ and $V_{o2} = V_{CC} - I_{c2}R_C$
- Define ***Differential-Mode Output Voltage***:

  $V_{od} = V_{o1} - V_{o2} = I_{EE}R_C\tanh[-V_{id}/(2V_T)]$
  - V_{od} (***positive maximum***) $= I_{EE}R_C$
  - V_{od} (***negative minimum***) $= -I_{EE}R_C$
  - At $V_{id} = 0$, $V_{od} = 0$
    - ***Permits direct coupling of stages without the need of any coupling capacitor***



Linear Range = $\pm 4V_T$ (~ $\pm$100 mV at room temperature)

The Voltage Transfer Characteristics of an npn DA

- ***DC Biasing***:
  - $V_i = V_I + v_i$ (V_I: ***DC bias voltage***, v_i: ***ac small-signal voltage***)
  - $I_c = I_C + i_c$ (I_C: ***DC bias current***, i_c: ***ac small-signal current***)
  - ***The ideal DC bias point should be $V_{I1} = V_{I2}$***

    $\Rightarrow$ ***$I_{C1} = I_{C2} = I_{EE}/2$***
  - ***Thus, any arbitrary DC voltage can be applied at the bases of Q_1-Q_2, provided they are same***

    $\Rightarrow$ ***Ideal choice***: ***ground***

    $\Rightarrow$ ***Necessitates a negative power supply for proper biasing***

- ***Under this condition***:

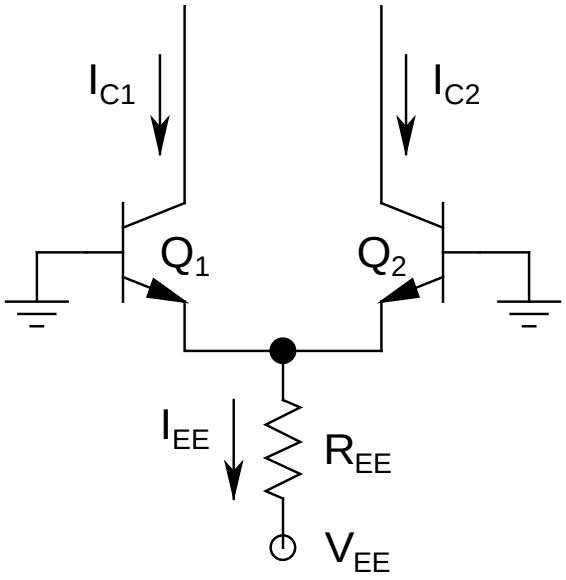
  $V_{01} = V_{02} = V_{CC} - I_{EE}R_C/2$ and $V_{0d} = 0$

- ***The simplest DC biasing scheme is to attach a resistor R_{EE} from the common emitter point to V_{EE}***:

  $\Rightarrow I_{EE} = (-0.7 - V_{EE})/R_{EE}$

  and $I_{C1} = I_{C2} = I_{EE}/2$

  $\Rightarrow$ ***Both Q_1 and Q_2 have same g_m, r_E, r_π and r_0***



Simplest DC Biasing Scheme for npn DA

- ***To improve performance, any of the current sources discussed earlier could be used in place of R_{EE}***

- ***A check is needed to see that Q_1 and Q_2 are biased in the forward active region***
- For this circuit, for ***best biasing***:

  $V_{CE1} = V_{CE2} = (V_{CC} + |V_{EE}|)/3$ (***3-element o/p branch***)

➢ ***ac Analysis***:

- ***Balanced DAs have perfect symmetry around the vertical cut-line going through the middle of the circuit***
- ***Can be analyzed using heuristics***
  - ❖ Known as the ***Half-Circuit Technique***
- ***This technique is based on an algorithm***

  (***Understand it thoroughly to get a clear grasp***!)

➢ *Algorithm for the Half-Circuit Technique*:

- ***Apply inputs v_{i1} and v_{i2} at the bases of Q_1 and Q_2 respectively***
- ***Outputs v_{o1} and v_{o2} taken from the collectors of Q_1 and Q_2 respectively***
- Define $v_{id} = (v_{i1} - v_{i2})$ as the ***pure differential-mode input***
- Define $v_{ic} = (v_{i1} + v_{i2})/2$ as the ***pure common-mode input***
- Thus:

$$v_{i1} = v_{id}/2 + v_{ic}$$

$$v_{i2} = -v_{id}/2 + v_{ic}$$

- Define $v_{od} = (v_{o1} - v_{o2})$ as the ***pure differential-mode output***
- Define $v_{oc} = (v_{o1} + v_{o2})/2$ as the ***pure common-mode output***
- Thus:

  $v_{o1} = v_{od}/2 + v_{oc}$

  $v_{o2} = -v_{od}/2 + v_{oc}$
- ***Now, assuming that pure differential-mode and pure common-mode signals are completely non-interacting***:
  - ***Pure differential-mode output can only be caused by a pure differential-mode input***
  - ***Pure common-mode output can only be caused by a pure common-mode input***

- Based on these, define:
  - ***Differential-Mode Gain***: $A_{dm} = v_{od}/v_{id}$
  - ***Common-Mode Gain***: $A_{cm} = v_{oc}/v_{ic}$
- Thus, from the ***principle of superposition***:
  - $v_{o1} = (A_{dm}/2)v_{id} + A_{cm}v_{ic}$
  - $v_{o2} = -(A_{dm}/2)v_{id} + A_{cm}v_{ic}$
- Thus, ***each output carries both differential- and common-mode signals***, however, the ***differential-mode signals are out of phase***, whereas the ***common-mode ones are in phase***
- ***Hence, the difference between the two outputs carries only the differential-mode signal, with a gain double that of a single output***

- ***The most important property of a DA is to be able to reject common-mode signals (noise), while amplifying the difference between the two signals applied at its two inputs***
- Characterized by a parameter known as the ***Common-Model Rejection Ratio*** (***CMRR***) (***expressed in dB***):

  $$CMRR = 20\log_{10}(|A_{dm}/A_{cm}|)$$

- ***Ideal (Desirable) Properties***:
  - $|A_{dm}| \rightarrow \infty$ ($\sim 10^3$-10^5)
  - $|A_{cm}| \rightarrow 0$ (< 1)
  - $CMRR \rightarrow \infty$ ($\sim$ 40-120 dB)

- ***The circuit has two inputs and two outputs***:

  $\Rightarrow$ ***Four possible configurations***:

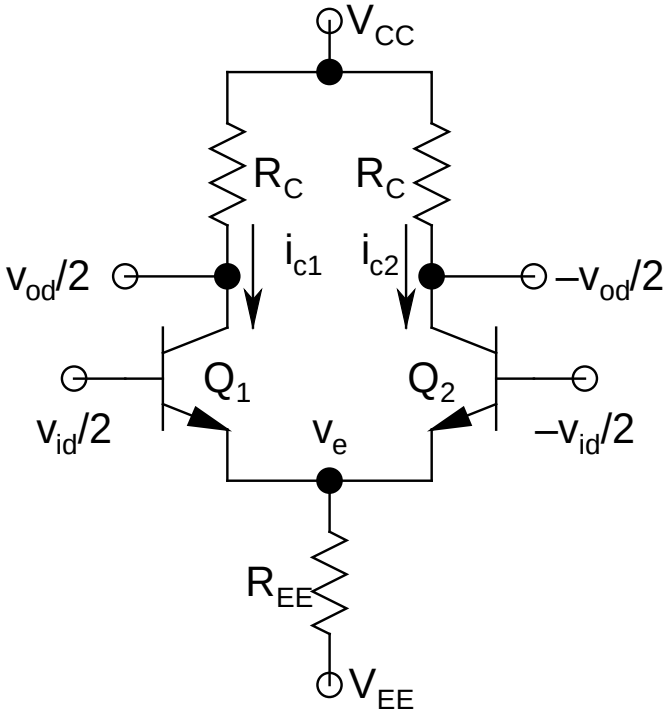
  - ***Single-ended i/p***, ***single-ended o/p***
  - ***Single-ended i/p***, ***double-ended o/p***
  - ***Double-ended i/p***, ***single-ended o/p***
  - ***Double-ended i/p***, ***double-ended o/p***

  $\Rightarrow$ ***Tremendous flexibility***

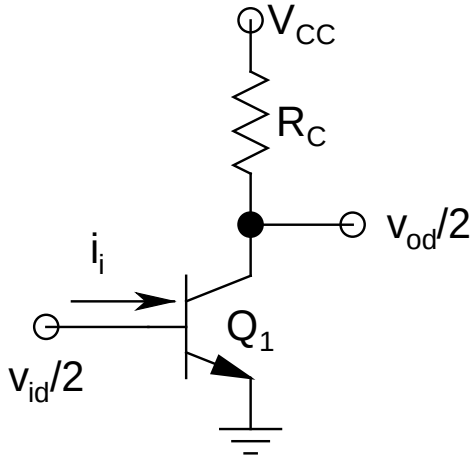
  - ***Double-ended o/p eliminates the common-mode signal completely***
  - ***However, at some point in the circuit, needs to be converted to a single-ended o/p***

    $\Rightarrow$ ***High CMRR is an absolute must***!

➢ *Differential-Mode Half Circuit*: *Calculation of A_{dm}*:



npn DA Under Pure Differential-Mode Input



Differential-Mode Half-Circuit

- ***Can be shown that $v_e = 0$ in three ways***:
  - ***From the symmetry of the circuit***:

    Equal and opposite voltages applied at the bases of Q_1 and Q_2

    $\Rightarrow$ ***The emitter potential v_e got to be an average of the inputs, which is zero***
  - $i_{c1} = g_{m1}(v_{id}/2 - v_e)$ and $i_{c2} = g_{m2}(-v_{id}/2 - v_e)$

    Since $g_{m1} = g_{m2}$, i_{c1} must equal $-i_{c2}$ (***circulating current***) (***this is again from symmetry***)

    $\Rightarrow v_e = 0$
  - ***Drawing the complete ac low-frequency hybrid-π model, and summing currents at the common-emitter node***:

    Show that $v_e = 0$
- ***Caution***: ***$v_e = 0$ will hold true only for a balanced DA***

- ***Thus, the left and right parts of the circuit become absolutely symmetrical***

  $\Rightarrow$ ***Either of the parts can be used***

  $\Rightarrow$ ***Leads to the differential-mode half-circuit***

- $g_{m1} = g_{m2} = g_m = I_{EE}/(2V_T)$, $r_{E1} = r_{E2} = r_E = 2V_T/I_{EE}$, and $r_{\pi 1} = r_{\pi 2} = r_\pi = \beta r_E$

- ***Can be easily identified to be a CE stage***

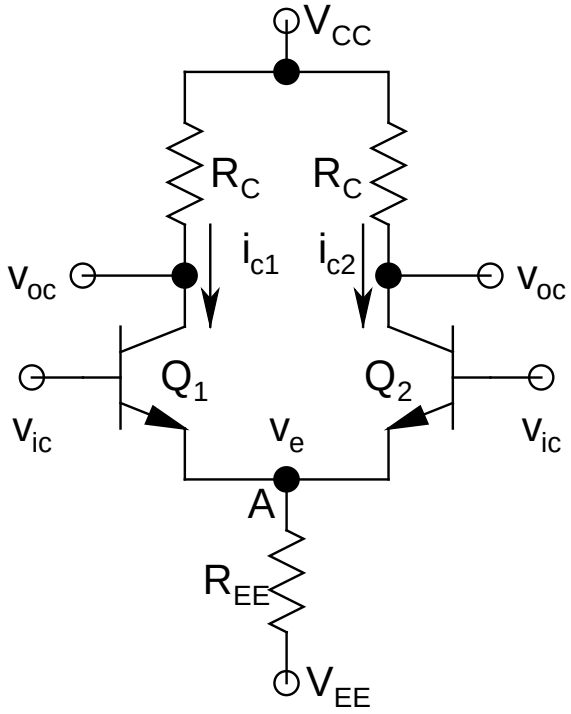
  $\Rightarrow A_{dm} = v_{od}/v_{id} = (v_{od}/2)/(v_{id}/2) = -R_C/r_E$

- ***Differential-mode input resistance***:

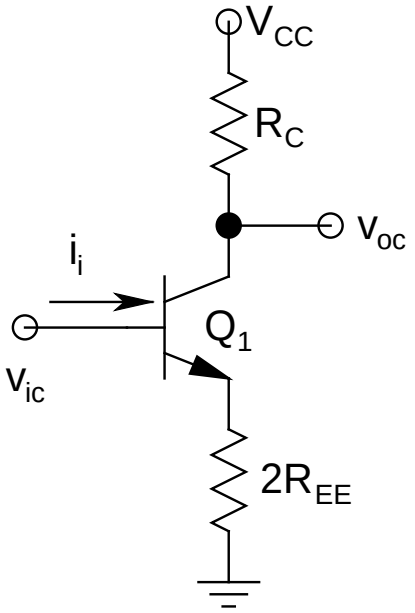
  $R_{id} = v_{id}/i_i = 2(v_{id}/2)/i_i = 2r_\pi$

- ***The simplicity of the analysis is simply mind-boggling***!

➢ *Common-Mode Half-Circuit*: *Calculation of* A_{cm}:



npn DA Under Pure Common-Mode Input



Common-Mode Half-Circuit

- $i_{c1} = i_{c2} = i_c = g_m(v_{ic} - v_e)$
- These two currents ***sum up at node A*** and ***flow through R_{EE}***, ***creating a voltage drop of $2i_cR_{EE}$ across it***
- Thus, ***R_{EE} can be split into two parts***, ***$2R_{EE}$ each***, and ***each part put in the emitter leads of Q_1 and Q_2***
- ***The lead connecting the two parts of R_{EE} would not carry any current, and can be removed***
- ***Thus, the circuit becomes perfectly symmetric along a vertical cut-line going through the middle of the circuit***, and we can ***consider either of them***

  $\Rightarrow$ ***Leads to the common-mode half-circuit***

- ***Can be easily identified to be a CE(D) stage***

  $\Rightarrow A_{cm} = v_{oc}/v_{ic} = -R_C/(r_E + 2R_{EE}) \approx -R_C/(2R_{EE})$

  (since, in general, $R_{EE} >> r_E$)

- ***Common-mode input resistance***:

  $R_{ic} = v_{ic}/i_i = r_\pi + (\beta + 1)2R_{EE} \approx 2\beta R_{EE}$

  (since, in general, $R_{EE} >> r_\pi$)

- ***Input resistance of the npn DA***:

  $R_i = R_{id} \| R_{ic} \approx R_{id} = 2r_\pi$ (***from superposition***)

  (since, in general, $R_{ic} >> R_{id}$)

- ***CMRR*** $= 20\log_{10}(|A_{dm}/A_{cm}|) \approx 20\log_{10}(2R_{EE}/r_E)$

- ***Some insights***:
  - A_{dm} *is independent of* R_{EE}, however, A_{cm} *is a strong function of* R_{EE}
  - *Goal is to make* A_{cm} *as close to zero as possible*

    $\Rightarrow$ *Make* R_{EE} *as large as possible*
  - *High value of* R_{EE} *will automatically ensure high value of CMRR* (*Highly desirable*!)
  - *High CMRR can also be achieved by reducing* r_E

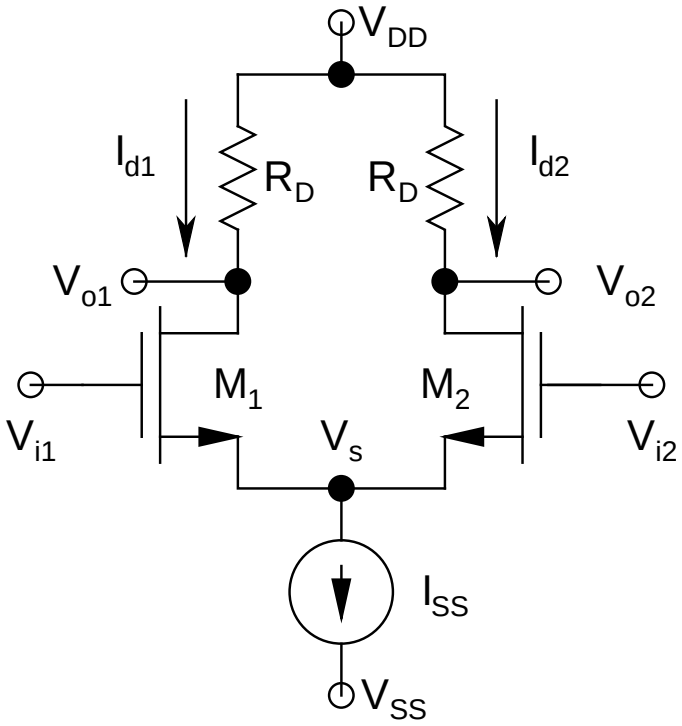
    $\Rightarrow$ *Can be obtained by increasing the DC bias current*

    $\Rightarrow$ *DC power dissipation of the circuit goes up*

    $\Rightarrow$ Also, *DC biasing may become suspect*!

- ***Increasing the Linear Range***:
  - ***Linear Range***: $\pm 4V_T$ (~ ***± 100 mV at room temperature***)
  - ***For some applications, this may not be enough***
  - ***Linear Range can be increased by attaching two identical resistors (R_E) in the emitter branches of Q_1 and Q_2***
  - ***Increases Linear Range by $I_{EE}R_E$*** (***Show***!)
  - ***This method decreases A_{dm}*** (***differential-mode half-circuit becomes CE(D) topology***)
  - ***Has minimal effect on A_{cm}***
  - ***CMRR suffers***! $\Rightarrow$ ***Not an optimal choice***!

- ***NMOS DA (SCP)***:
  - M_1-M_2 constitute a ***perfectly matched pair***, and have their ***sources connected together***, hence, the name
  - I_{SS}: ***DC bias current source***
  - ***All voltages and currents are instantaneous***



NMOS DA Topology

- $V_{gs1} = V_{i1} - V_s$, and $V_{gs2} = V_{i2} - V_s$
- ***KVL around M_1-M_2 GS loop***:

$$V_{i1} - V_{gs1} + V_{gs2} - V_{i2} = 0$$

$$\Rightarrow V_{gs1} - V_{gs2} = V_{i1} - V_{i2} = V_{id}$$

- ***Neglecting CLM Effect***:

$$I_{d1} = \frac{k'_N}{2}\left(\frac{W}{L}\right)\left(V_{gs1} - V_{TN1}\right)^2 \quad \text{and}$$

$$I_{d2} = \frac{k'_N}{2}\left(\frac{W}{L}\right)\left(V_{gs2} - V_{TN2}\right)^2$$

- Ran into a problem, since ***both M_1 and M_2 would have body effect present***
  - ***Both bodies connected to V_{SS}***, but the ***common source node is at a floating potential V_s***

    $\Rightarrow$ ***Analytical evaluation of I_{d1} and I_{d2} becomes pretty tedious***
- ***If the CLM effect is also included***, then ***the problem would need numerical solution***!
- To get a ***first-order estimate***, ***neglect body effect***

  $\Rightarrow V_{TN1} = V_{TN2} = V_{TN0}$

- Thus:

$$V_{id} = \frac{\sqrt{I_{d1}} - \sqrt{I_{d2}}}{\sqrt{\frac{k'_N}{2}\left(\frac{W}{L}\right)}} \qquad (1)$$

- Also:

$$I_{d1} + I_{d2} = I_{SS} \qquad (2)$$

- ***Solving Eqs.(1) and (2)***:

$$I_{d1} = I_{SS}/2 + \xi \quad \text{and}$$

$$I_{d2} = I_{SS}/2 - \xi$$

$$\xi = \frac{k'_N}{4}\left(\frac{W}{L}\right)V_{id}\sqrt{\frac{4I_{SS}}{k'_N(W/L)} - V_{id}^2}$$

- For $V_{id} = 0$, $\xi = 0$, and $I_{d1} = I_{d2} = I_{SS}/2$
  - *Most preferred DC bias point of the circuit*
- *For $V_{id} > 0$, $I_{d1}\uparrow$ and $I_{d2}\downarrow$*
- *For $V_{id} < 0$, $I_{d1}\downarrow$ and $I_{d2}\uparrow$*
- But *for both cases*, the *sum of I_{d1} and I_{d2} remains constant at I_{SS}*
- *Linear Range* of this circuit is *defined by the values of V_{id}*, which *turns either M_1 or M_2 off*

- To find the ***Linear Range***, ***use Eq.(1)*** and ***put either I_{d1} or I_{d2} equal to I_{SS}***:

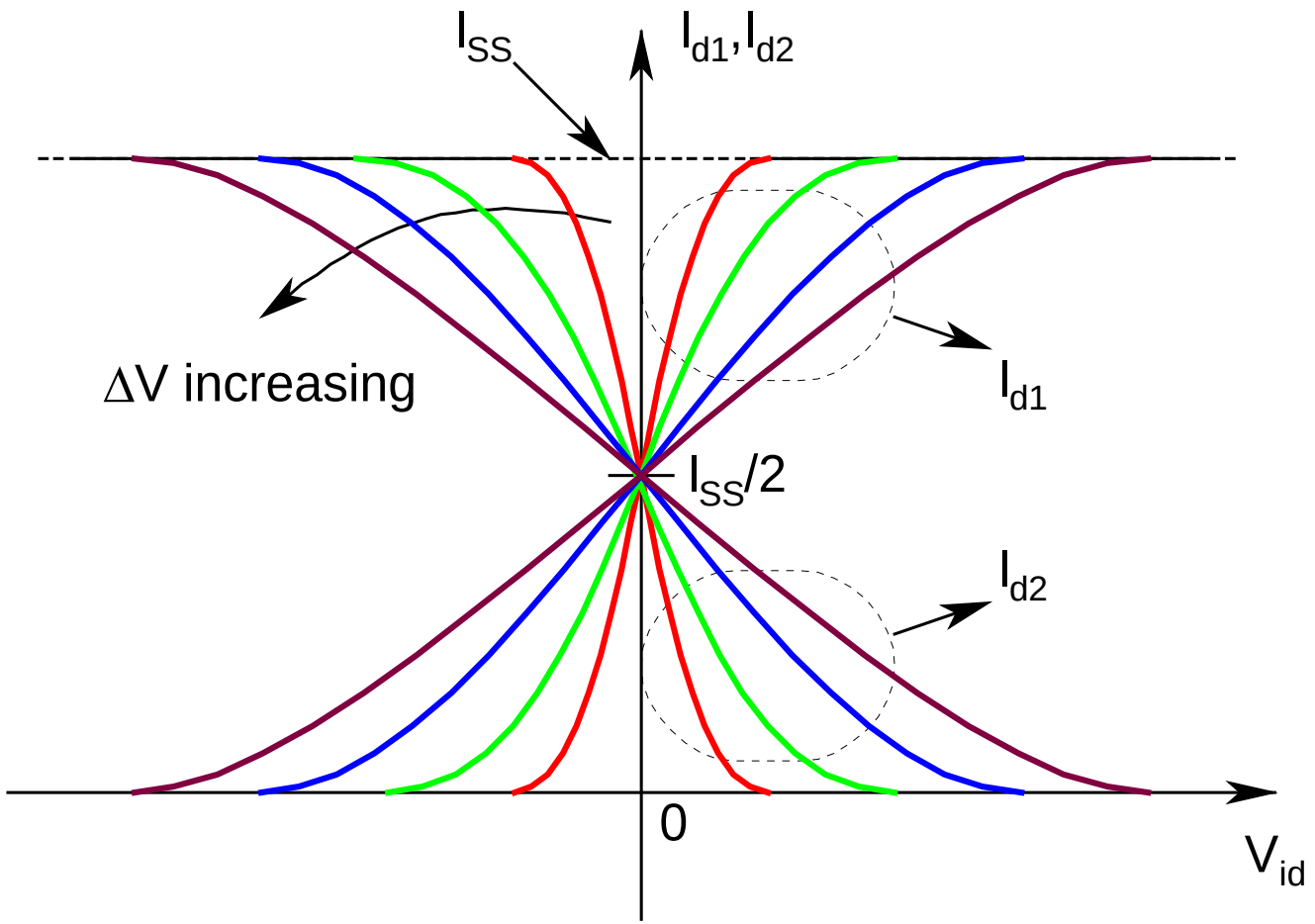
$$\Rightarrow V_{id} = \pm\sqrt{\frac{2I_{SS}}{k'_N(W/L)}} = \pm\sqrt{2}\left(\sqrt{\frac{2I_{d1}}{k'_N(W/L)}}\right)\Bigg|_{V_{id}=0}$$

$$= \pm\sqrt{2}\,(\Delta V)\Big|_{V_{id}=0}$$

since for $V_{id} = 0$, $I_{SS} = 2I_{d1} = 2I_{d2}$

ΔV = ***Gate Overdrive for M_1/M_2 for $V_{id} = 0$***

- ***Thus, the Linear Range is a function of I_{SS} and (W/L)*** $\Rightarrow$ ***Tremendous flexibility***!
- ***Recall***: In ***npn DA***, this ***Linear Range*** was ***$\pm 4V_T$***, and ***depended only on temperature***



The Current Transfer Characteristics of an NMOS DA

- ***Differential Current***:

$$\partial I_d = I_{d1} - I_{d2} = 2\xi$$

- ***Differential-Mode Output Voltage***:

$$V_{od} = V_{o1} - V_{o2} = (V_{DD} - I_{d1}R_D) - (V_{DD} - I_{d2}R_D)$$
$$= -(\partial I_d)R_D = -2\xi R_D$$

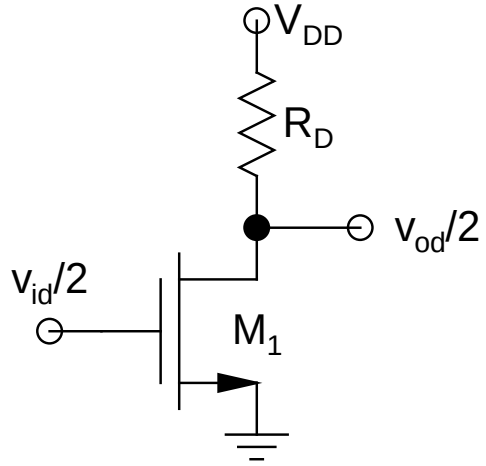
- ***Note***:
  - When $V_{id} = 0$, $\xi = 0$, $\partial I_d = 0$, and $V_{od} = 0$
  - *This is the perfect DC bias point*
  - *No need for interstage coupling capacitor*
  - $I_{D1} = I_{D2} = I_{SS}/2$
  - $V_{Id} = 0 \Rightarrow$ *Tie both gates to ground* and *use a negative power supply*

- ***ac Analysis***:
  - ***The procedure adopted for npn DA can be lifted verbatim***
- ***Differential-Mode Half-Circuit***: ***Calculation of A_{dm}***:
  - ***The common-source node is at ac ground*** (***from symmetry***)
  - ***Body is also at ac ground***

    $\Rightarrow v_{bs} = 0 \Rightarrow g_{mb} v_{bs} = 0$
  - ***Simple CS stage***:

    $\Rightarrow A_{dm} = v_{od}/v_{id} = -g_m R_D$

    $g_m = k_N \Delta V$

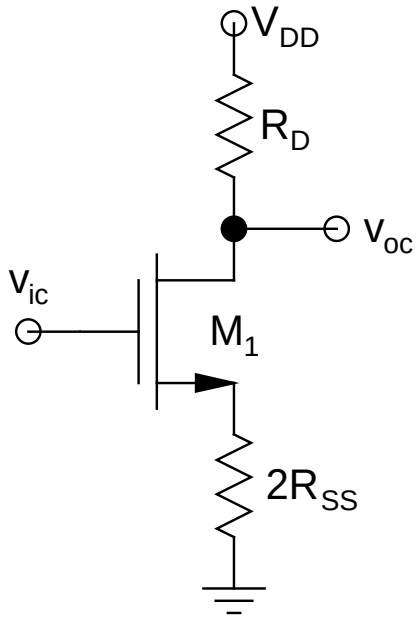


Differential-Mode Half-Circuit

- ***Common-Mode Half-Circuit***: ***Calculation of Acm***:
  - ***CS(D) stage***, but now ***with body effect present***

    $\Rightarrow A_{cm} = v_{oc}/v_{ic}$

    $= -g_m R_D/[1 + (g_m + g_{mb})2R_{SS}]$



Common-Mode Half-Circuit

- Thus:

  $CMRR = 20\log_{10}(|A_{dm}/A_{cm}|)$

  $\approx 20\log_{10}[2(g_m + g_{mb})R_{SS}]$

- Again, ***R_{SS} plays no role in A_{dm}***, but ***determines A_{cm} and CMRR***

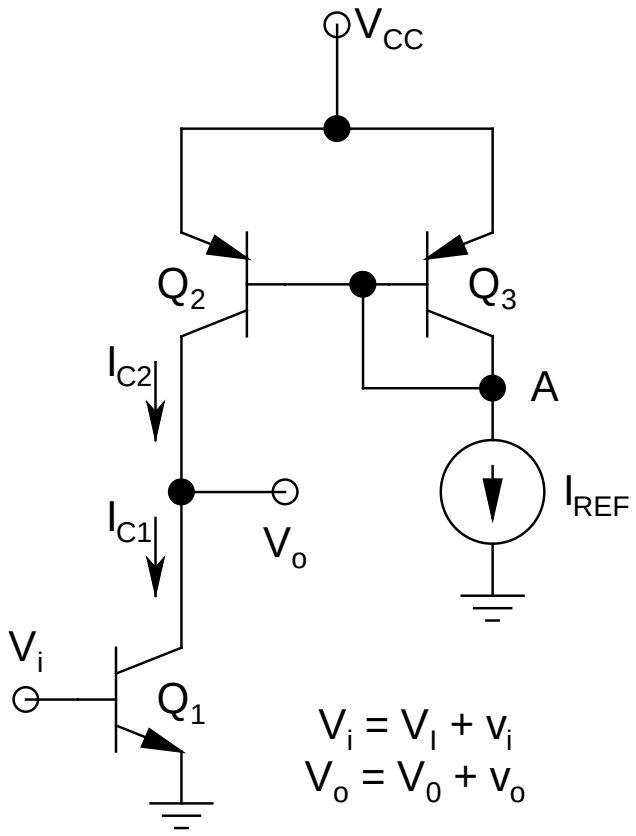
  $\Rightarrow$ ***A high value of R_{SS} highly desirable***

- ***Actual situation is not so rosy and hunky-dory***
- ***The DA can become unbalanced if there is a mismatch between the devices and/or the resistors, and our analysis would fail***!
- Gives rise to ***offset voltage*** (***for both npn and NMOS DA***) and ***offset current*** (***only for npn DA***)
- ***This mismatch is caused by technology and is totally random***
- ***Fortunately, the effect is not that severe, since there are technological innovations to match devices and/or resistors***

Actively Loaded Amplifier Stages

- ***Main Goal***: ***To reduce usage of resistors as much as possible*** and ***use transistors instead as active load***
- Interesting to note that ***transistors offer much higher resistance than physical resistors***, while ***occupying much smaller chip area***

- ***npn CE Stage With pnp Active Load***:
  - Q_1: ***Driver***, Q_2: ***Load***
  - Identify Q_2-Q_3 as a ***pnp current mirror***
  - Q_2-Q_3 constitute a ***matched pair***
  - ***Neglecting base currents***: $I_{C2} = I_{REF}$
  - ***Biasing of the circuit is tricky***



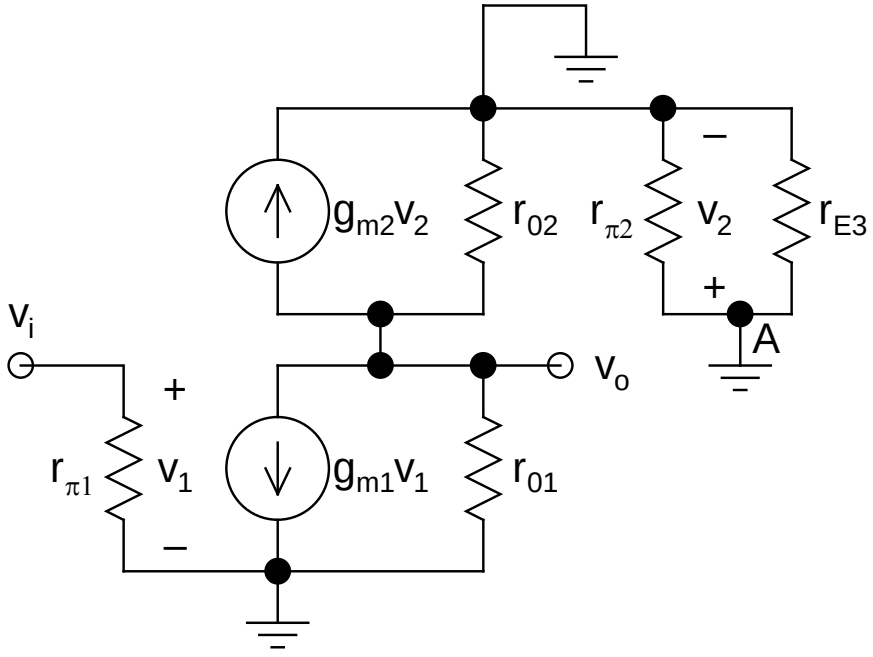
Circuit Diagram

- There is a ***trivial solution*** of $I_{C1} = I_{C2} = 0$, and the ***circuit collapses***
- For ***proper biasing***, I_{C1} ***must equal*** I_{C2} $(= I_{REF})$
- Thus, V_I ***should be properly adjusted***, such that:

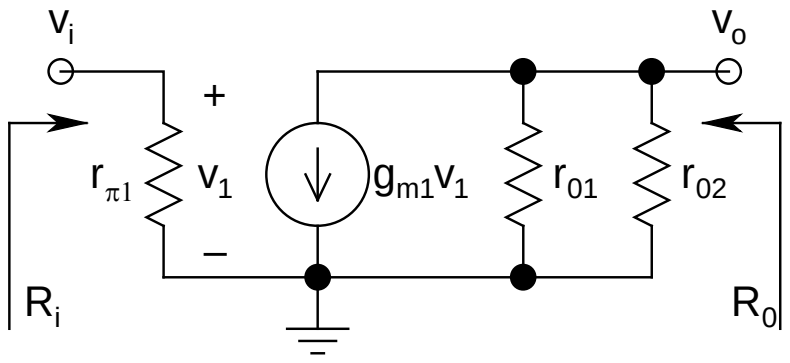
  $V_I = V_T \ln(I_{REF}/I_{S1})$
- ***Such a high precision in*** V_I ***may not be practically achievable***

  $\Rightarrow$ ***Use a resistor in series with*** V_I ***and self-consistently solve for the bias point***

➢ *ac Analysis*:



ac Midband Equivalent



Simplified Equivalent

- First, note that Q_3 is ***diode-connected*** (***BC short***)

  $\Rightarrow$ The ***equivalent*** of Q_3 is simply a ***resistor*** r_{E3}
- ***Node A*** is a peculiar one, and can be considered ***open or short both***!
  - ***Open because the current source I_{REF} is ideal***
  - ***Short because the base of Q_2-Q_3 is at a fixed DC potential, and thus ac ground***
- In either case, ***$v_2 = 0 \Rightarrow g_{m2}v_2$ disappears***!

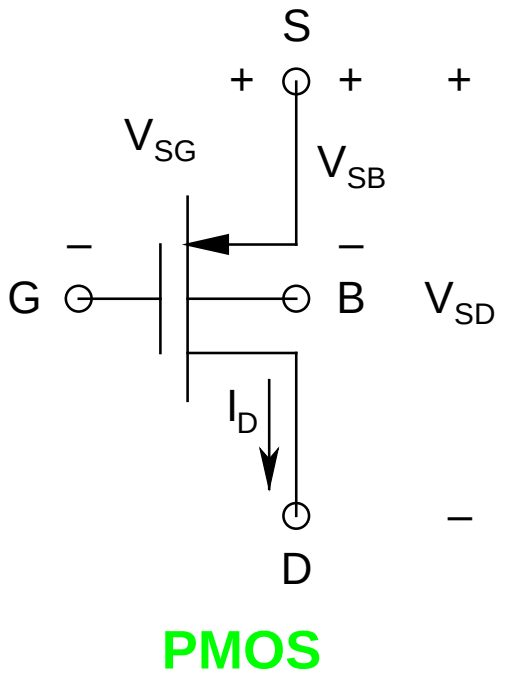
  $\Rightarrow$ Leads to the ***simplified equivalent***
- ***By inspection***: $R_i = r_{\pi 1}$ and $R_0 = r_{01} \| r_{02}$
- $A_v = v_o/v_i = - g_{m1}R_0 = - 1/(\eta_n + \eta_p)$

  $\eta_n = V_T/V_{AN}$ and $\eta_p = V_T/V_{AP}$
- ***Enormously large gain possible***!

p-channel MOSFET (PMOS)

- Before moving to ***NMOS stages with active load***, it will be prudent to visit some details regarding ***PMOS***
- ***Substrate***: ***n-type*** (N_D)
  - ***Bulk Potential***:

    $\phi_F = V_T \ln(N_D/n_i)$
- ***Source/Drain***: p^+
- ***Channel Carriers***: ***Holes***



- ***Threshold Voltage***:

$$V_{TP} = V_{TP0} - \gamma\left(\sqrt{2\phi_F + V_{BS}} - \sqrt{2\phi_F}\right)$$

V_{TP0}: ***Zero back-bias threshold voltage*** (***negative***)

- ***Body effect coefficient***:

$$\gamma = \frac{\sqrt{2q\varepsilon_s N_D}}{C'_{ox}}$$

  - $V_{BS} \geq 0$ (***to prevent forward biasing of SB junction***)

- ***With back bias***, V_{TP} ***becomes more negative***
- V_{GS} ***has to be less than*** V_{TP} ***to turn device on***

- ***Current-Voltage Relation***:
  - ***Both V_{GS} and V_{DS} negative***
  - ***I_D flows from source to drain*** (the ***same direction of flow as holes***)
  - ***In saturation*** $[|V_{DS}| > (|V_{GS}| - |V_{TP}|)]$:

$$I_D = \frac{k'_P}{2}\frac{W}{L}\left(|V_{GSp}| - |V_{TP}|\right)^2\left(1+\lambda_p|V_{DSp}|\right)$$

  - ***In non-saturation*** $[|V_{DS}| < (|V_{GS}| - |V_{TP}|)]$:

$$I_D = k'_P\frac{W}{L}\left[\left(|V_{GSp}| - |V_{TP}|\right)|V_{DSp}| - |V_{DSp}|^2/2\right]$$

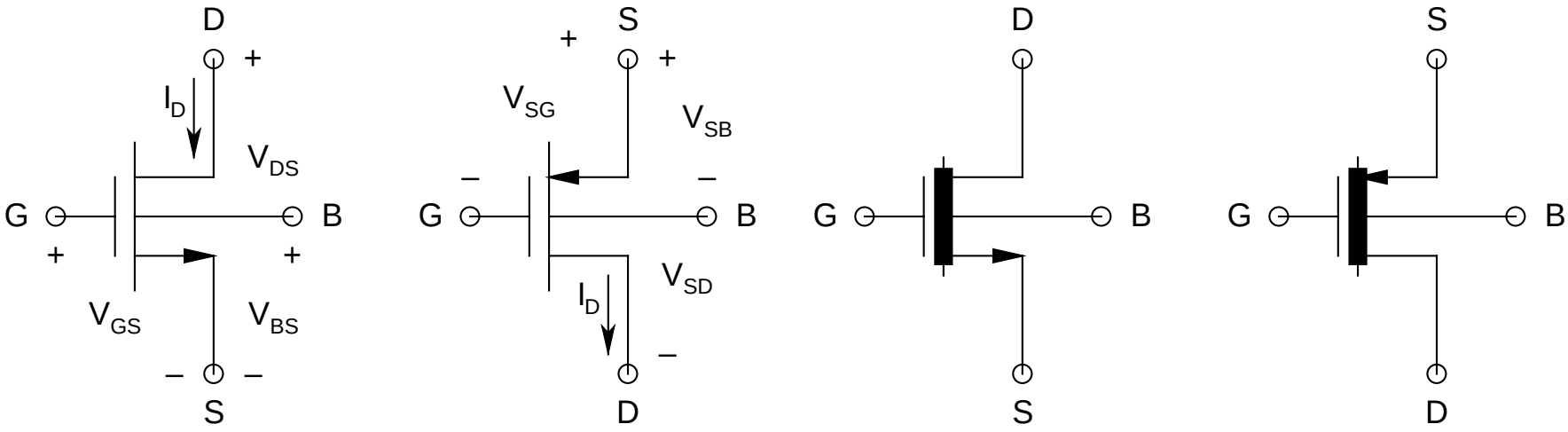
$$k'_P = \mu_p C'_{ox}$$

$=$ ***Process transconductance parameter***

μ_p = ***Channel hole mobility***

- ***Based on the value of V_{TN0} and V_{TP0}***, there are ***two classifications***:
  - ***Enhancement Mode***: ***Normally Off*** (***with $V_{GS} = 0$***)
    - ***V_{TN0} positive*** and ***V_{TP0} negative***
  - ***Depletion Mode***: ***Normally On*** (***with $V_{GS} = 0$***)
    - ***V_{TN0} negative*** and ***V_{TP0} positive***

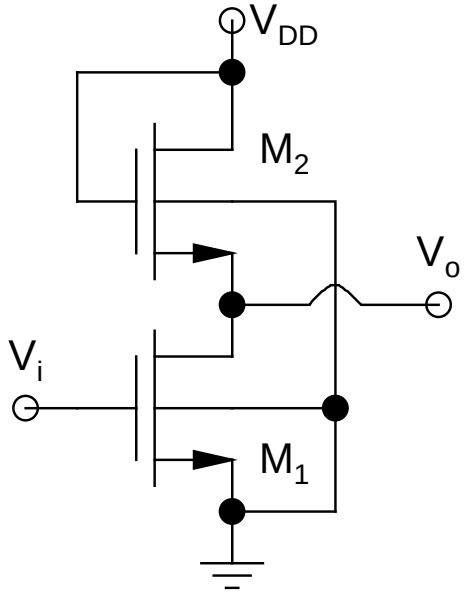
Symbols



- Note the ***thick band*** in the ***channel region*** for ***depletion mode devices***, which implies that ***channel is present*** even ***with $V_{GS} = 0$***

- ***Variants of Actively Loaded CS Stage***:
  - ***Saturated Enhancement Load***
  - ***Depletion Load***
  - ***Complementary PMOS Load***
    - Also known as ***CMOS Gain Stage***
- ***The last one is the most popular***

- ***Saturated Enhancement Load***:
  - ***Both bodies tied to ground***
    - ***For M_1: $V_{SB1} = 0$***
    - ***For M_2: $V_{SB2} = V_o$***
  - ***M_2 is enhancement mode***
    - ***V_{TN02} positive***
  - ***M_2 is also diode-connected***
    - ***Always operates in saturation***
  - ***M_2 has a floating body effect***



Circuit Schematic

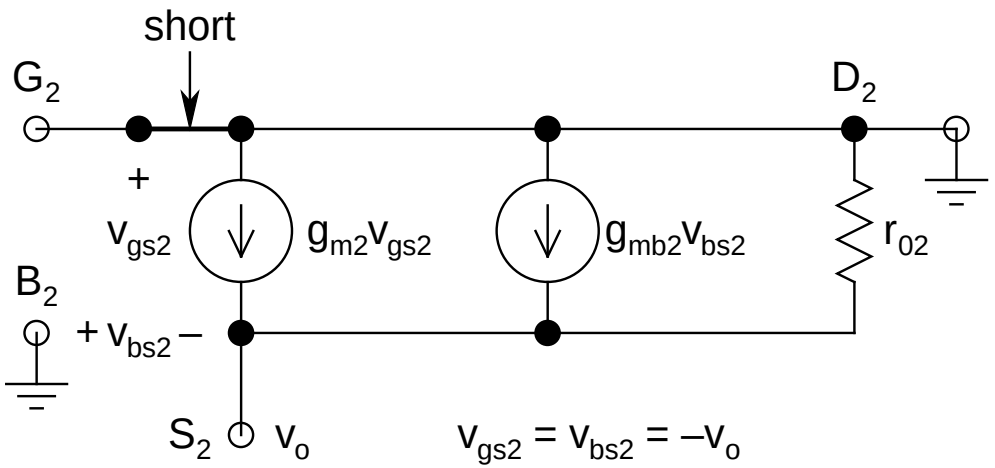
problem: ***V_o is a variable*** and ***V_{TN2} will continuously change with a change in V_o***

- ***For M_2 to remain on, its V_{GS2} ($= V_{DD} - V_o$) must be $> V_{TN2}$***
- Thus, there is a ***maximum possible V_o***, beyond which ***it cannot rise*** (***M_2 would cut off***)
- To estimate this ***maximum V_o***, for the time being, ***neglect that $3V_T$ cushion***
- Then:

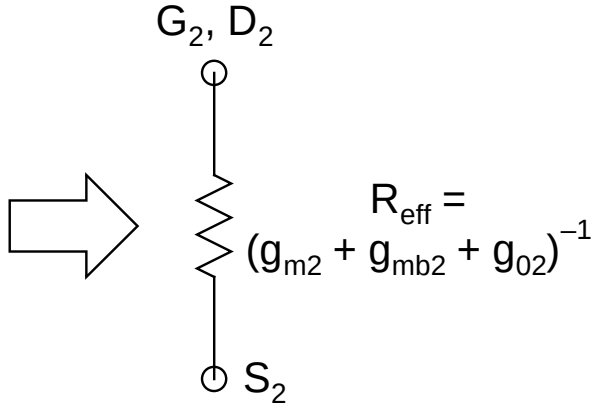
$$V_{DD} - V_{o,max} > V_{TN2} \text{ (with } V_{SB2} = V_{o,max})$$

$$V_{TN2} = V_{TN02} + \gamma\left(\sqrt{2\phi_F + V_{o,max}} - \sqrt{2\phi_F}\right)$$

- ***Solution of this equation would give $V_{o,max}$***
- ***Once $V_{o,max}$ is obtained***, the ***best bias point would be at $V_0 = V_{o,max}/2$***
- Before doing ***ac analysis***, ***let's investigate M_2***:



ac Midband Equivalent of M_2

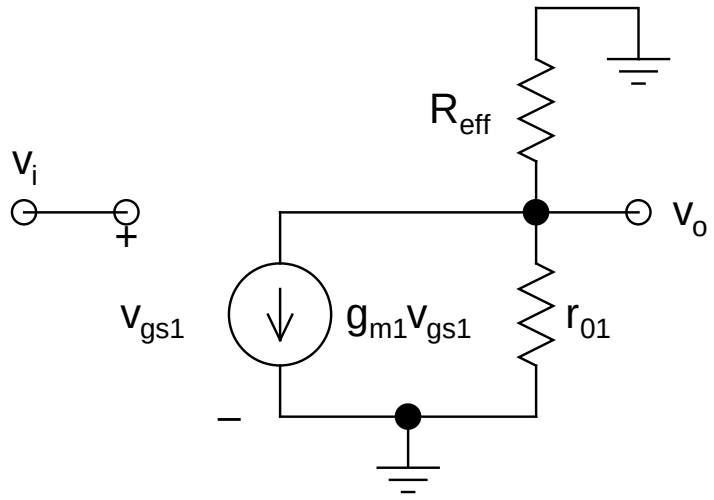


Simplified Equivalent

- Thus, the ***complete equivalent***:
- ***By inspection***:

$$A_v = \frac{v_o}{v_i} = -g_{m1}\left(r_{01} \parallel R_{eff}\right)$$

$$= -\frac{g_{m1}}{g_{m2} + g_{mb2} + g_{01} + g_{02}}$$



Complete Equivalent

- Now, in general,

$$(g_{m2} + g_{mb2}) >> (g_{01} + g_{02})$$

$$\Rightarrow A_v \approx -\frac{g_{m1}}{g_{m2} + g_{mb2}} = -\frac{g_{m1}}{g_{m2}\left(1 + \chi_2\right)}$$

$$\chi_2 = \frac{\gamma}{2\sqrt{2\phi_F + V_{0Q}}}$$

V_{0Q} = ***Quiescent DC output voltage***

- Now, if M_2 can be put in its ***separate island***, then S_2 and B_2 can be ***connected together***

$$\Rightarrow v_{sb2} = 0 \Rightarrow g_{mb2}v_{sb2} = 0$$

$$\Rightarrow A_v \approx -\frac{g_{m1}}{g_{m2}} = -\sqrt{\frac{(W/L)_1}{(W/L)_2}}$$

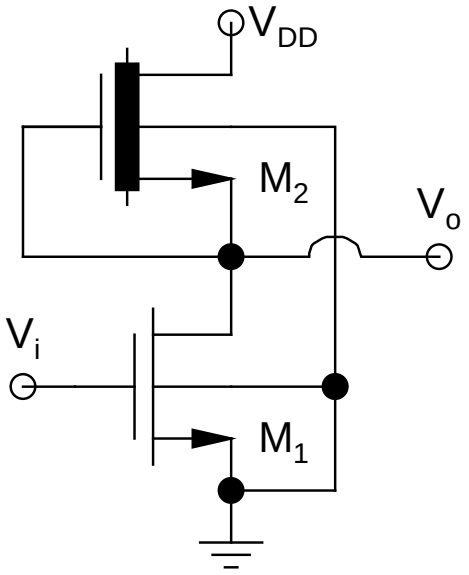
- $R_0 = (g_{m2} + g_{mb2} + g_{01} + g_{02})^{-1}$

- ***Insights***:
  - ***V_o doesn't go all the way to V_{DD}***

    $\Rightarrow$ Full rail-to-rail swing can't be achieved
  - ***When V_o falls below ΔV of M_1, it leaves the saturation region***, and ***enters non-saturation region***

    $\Rightarrow$ Distortion will set in at the output
  - Even for a ***moderate voltage gain of 10***, the ***ratio of the aspect ratios of M_1 and M_2 has to be 100***!
  - ***All these problems coupled together make this circuit highly unattractive for practical use***

- ***Depletion Load***:
  - M_2 is ***depletion mode***, having ***negative*** V_{TN0} (***denoted by*** V_{TD0})
  - ***Back bias of*** M_2: $V_{SB2} = V_o$
  - ***With*** V_o, V_{TD2} ***changes***
  - ***Maximum*** V_o ***desired*** $= V_{DD}$
  - ***This is also the maximum back bias of*** M_2



Circuit Schematic

- M_2 *has GS short* $\Rightarrow$ $V_{GS2} = 0$
- *Even with* $V_o = V_{SB2}(max) = V_{DD}$, V_{TD2} *should remain negative with a cushion of at least 100 mV*

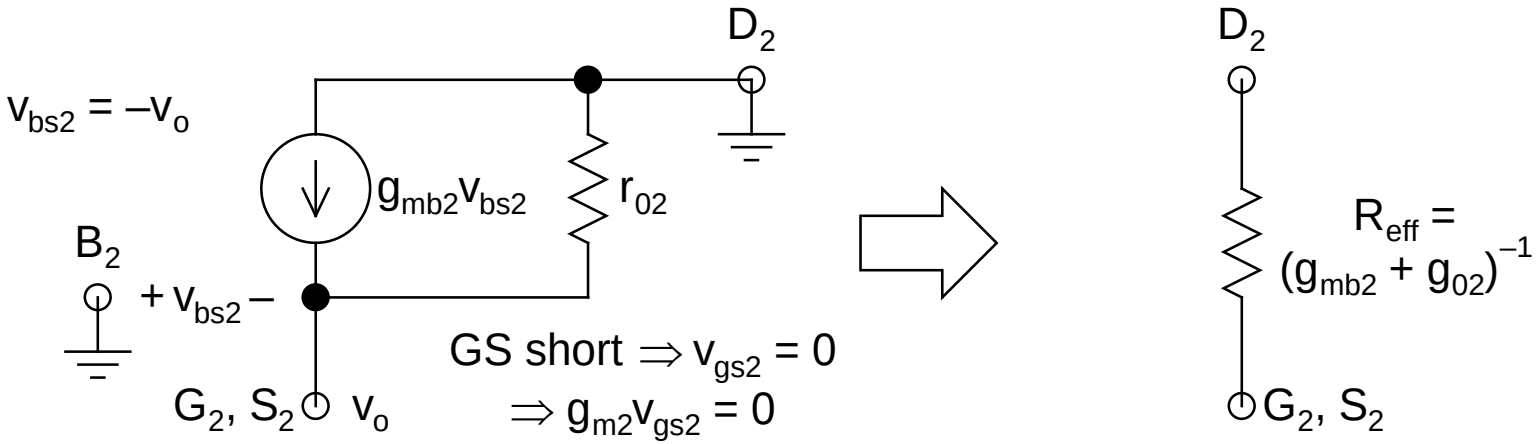
  $\Rightarrow$ V_{TD2} *with* $V_{SB2} = V_{DD}$ *should be –100 mV*

  $\Rightarrow$ V_{TD0} *should be chosen based on this*
- Now, $V_{DS2}(min) = V_{DD} - V_o(max) = 0$
- Under this condition, $V_{GS2} - V_{TD2} = \Delta V_2 = 100$ *mV*

  $\Rightarrow$ M_2 *is in the linear region* (*since* $V_{DS2} < \Delta V_2$)

- ***This has to be lived with***, and ***slight distortion would appear at the output as $V_o \rightarrow V_{DD}$***
- For ***best biasing***, $V_{0Q} = V_{DD}/2$

  $\Rightarrow$ ***Fixes the DC operating point***
- Before doing ***ac analysis***, ***let's investigate M_2***:



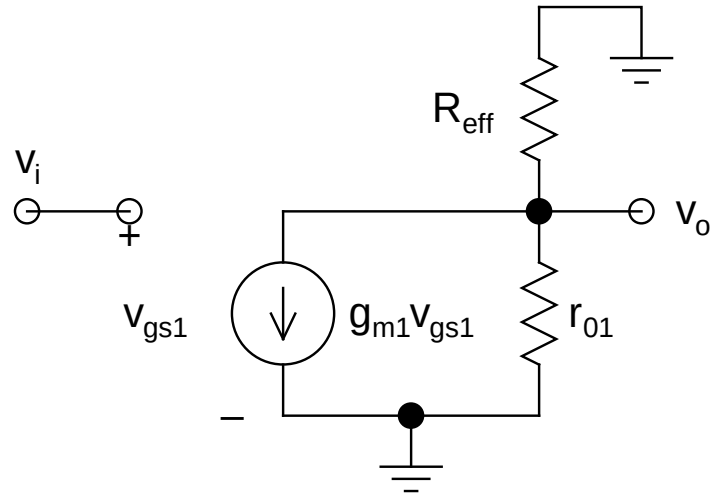
ac Midband Equivalent of M_2

Simplified Equivalent

- Thus, the ***complete equivalent***:
- ***By inspection***:

$$A_v = \frac{v_o}{v_i} = -g_{m1}\left(r_{01} \parallel R_{eff}\right)$$

$$= -\frac{g_{m1}}{g_{mb2} + g_{01} + g_{02}}$$



Complete Equivalent

- Now, in general,

$$g_{mb2} >> (g_{01} + g_{02})$$

$$\Rightarrow A_v \approx -\frac{g_{m1}}{g_{mb2}} = -\frac{g_{m1}}{\chi_2 g_{m2}} = -\frac{1}{\chi_2}\sqrt{\frac{(W/L)_1}{(W/L)_2}}$$

$$\chi_2 = \frac{\gamma}{2\sqrt{2\phi_F + V_{DD}/2}} < 1$$

$\Rightarrow$ ***Improvement*** as compared to previous stage

- Now, if M_2 can be put in its ***separate island***, then ***S_2 and B_2 can be connected together***

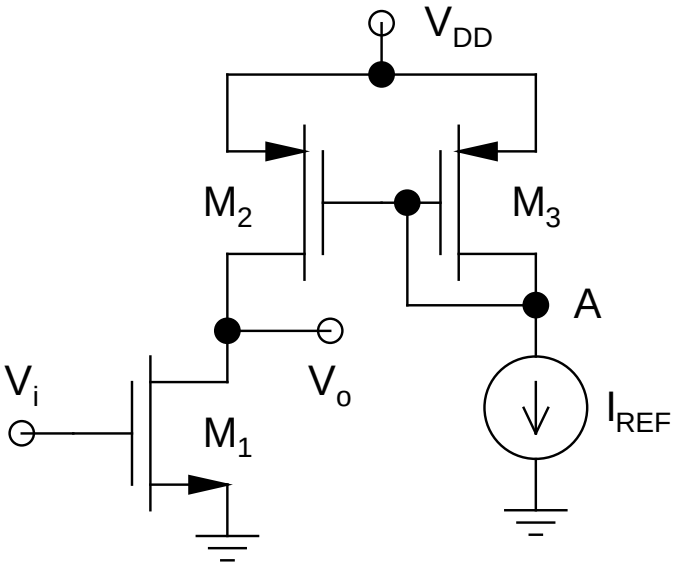
$\Rightarrow$ ***$v_{sb2} = 0$*** $\Rightarrow$ ***$g_{mb2} v_{sb2} = 0$***

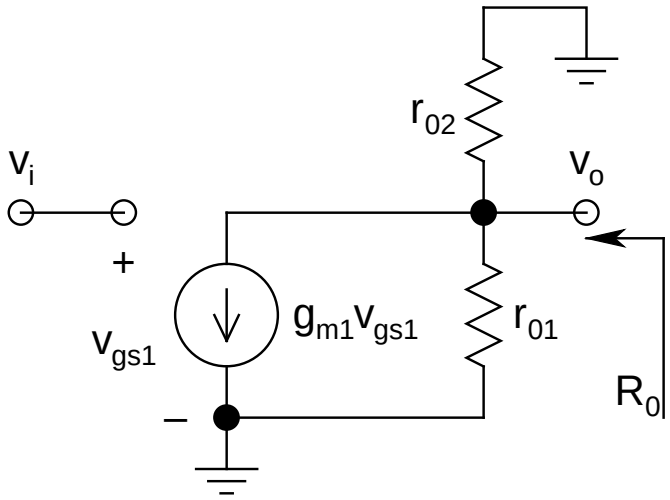
$$\Rightarrow A_v = -\frac{g_{m1}}{g_{01} + g_{02}}$$

  - Can be ***very large*** (***a magnitude greater than 100 is possible***)

- $R_0 = (g_{mb2} + g_{01} + g_{02})^{-1}$ (***with body effect***)
- $R_0 = (g_{01} + g_{02})^{-1}$ (***without body effect***)
- The latter case produces ***very high R_0***
- Thus, this circuit produces ***much superior performance*** as compared to the ***saturated enhancement load***, in terms of:
  - ***Rail-to-rail swing***
  - ***With island technology***:
    - ***Very large A_v and R_0***
  - ***Without island technogy***:
    - ***Moderate A_v and R_0***

- ***Complementary PMOS Load***:
  - Also known as ***CMOS Gain Stage***
    - ***CMOS*** (***Complementary MOS***: ***Having both NMOS and PMOS*** in the circuit)
  - ***The Ultimate***: ***Much superior performance*** and ***outclasses all other gain stages***
  - ***Widely used***
  - ***High A_v and R_0***
  - ***Easy to bias and easy to operate***
  - ***Design also extremely simple***
  - ***Doesn't produce any anomalies***





Circuit Schematic **ac Midband Equivalent**

- ***M_1 body connected to ground, M_2-M_3 bodies connected to V_{DD}***
  - *No body effect problem for any of the devices* (*biggest advantage of this circuit*)

- Identify M_2-M_3 as a ***PMOS current mirror*** (***perfectly matched***)

  $\Rightarrow I_{D1} = I_{D2} = I_{D3} = I_{REF}$

- This gives the ***required value*** of V_I

  $\Rightarrow$ ***DC biasing*** of the circuit is ***pretty straightforward***

- For ***ac analysis***, we note that ***node A*** is ***both open and short*** at the same time (similar to ***npn gain stage*** with ***pnp active load***)

  $\Rightarrow A_v = v_o/v_i = -g_{m1}R_0$

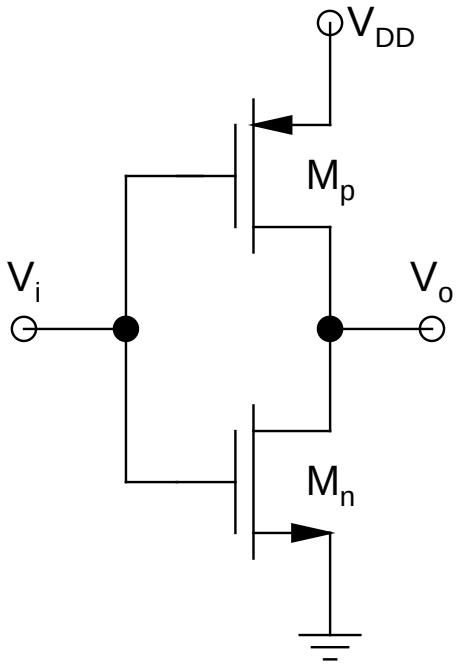
  R_0 $(= r_{01} \| r_{02})$: ***Output resistance*** of the circuit

- ***Caution***: $r_{01} \neq r_{02}$, even though M_1 and M_2 carry the same ***DC bias current***, since $\lambda_n \neq \lambda_p$ (in general)
- This circuit is ***immensely useful*** since it gives ***extremely large voltage gain and output resistance***
- Only ***problem*** is that it needs a ***PMOS current mirror***, thus necessitating use of an ***extra PMOS***
- An ***even better design*** exists, which ***eliminates*** the need for this ***extra PMOS***

- ***A Better CMOS Gain Stage***:
  - ***No body effect issue***
  - However, there are ***some design issues***
  - M_n-M_p have ***same magnitude*** of the ***threshold voltage***:

    $V_{TN0} = |V_{TP0}|$
  - ***Process transconductance parameters***:

    $k'_N = \mu_n C'_{ox}$ and $k'_P = \mu_p C'_{ox}$



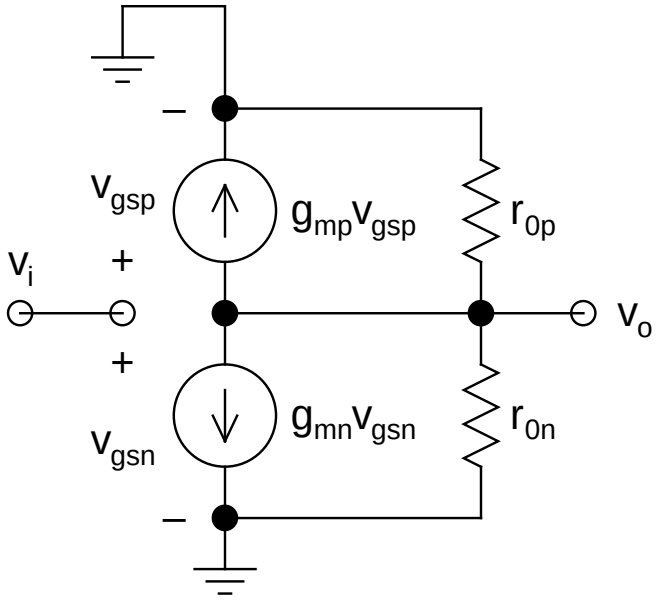
Circuit Schematic

- ***Oxide capacitance per unit area*** $\left(C'_{ox} = \varepsilon_{ox}/t_{ox}\right)$ ***same for both devices***, since they have ***same*** t_{ox}
- However, $\mu_n \sim 2\mu_p$ (***for Si***)
- Thus, $k'_N = 2k'_P$
- ***Ideal DC bias point*** of the circuit is $V_I = V_0 = V_{DD}/2$ (yields $V_{GSn} = |V_{GSp}|$ and $V_{DSn} = |V_{DSp}|$)
- Can be achieved only if the stage is ***completely balanced*** (***same threshold voltage magnitude*** and ***same device transconductance parameter***)
- Thus, k_N ***and*** k_P ***need to be matched***

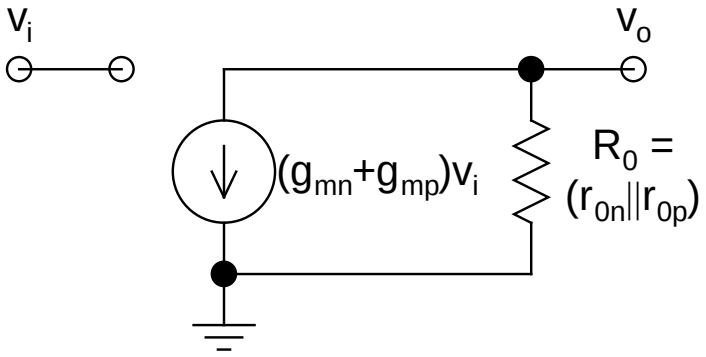
- ***Can be achieved by making $(W/L)_p = 2(W/L)_n$***
- If ***CLM effect*** is ***not that important***, or if $\lambda_n = \lambda_p$, then this procedure works out ***just fine***
- However, if $\lambda_n \neq \lambda_p$, then for ***balancing the circuit***, the following relation ***must hold*** (***show***!):

  $k_P(1 + \lambda_p V_{DD}/2) = k_N(1 + \lambda_n V_{DD}/2)$
- Under this condition, $k_N \neq k_P$, but the circuit will be ***perfectly matched and balanced***
- Known as: ***Stage unmatched by nature, but matched by performance***

➢ *ac Analysis*:



ac Midband Equivalent



Simplified Equivalent

- ***By inspection***:

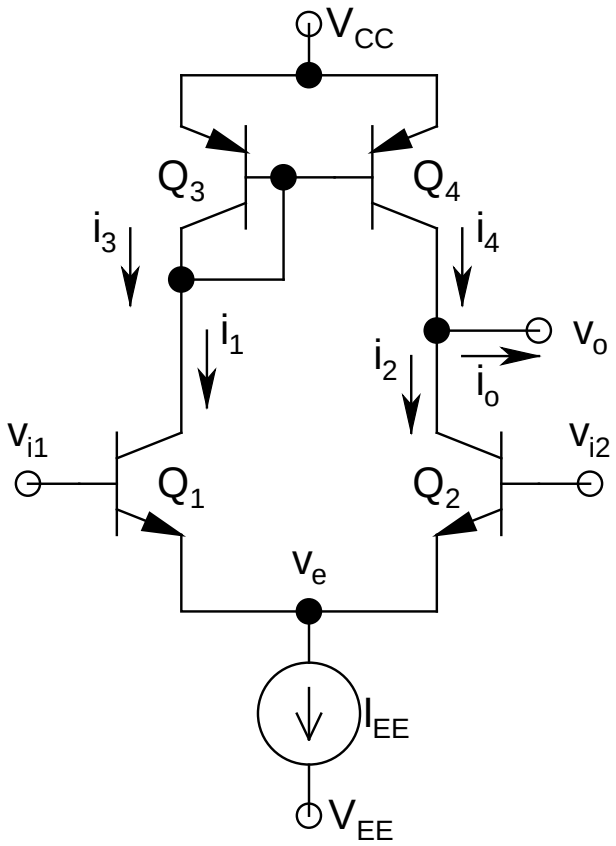
  $A_v = -(g_{mn} + g_{mp})R_0$

  $= -(g_{mn} + g_{mp})/(g_{0n} + g_{0p})$

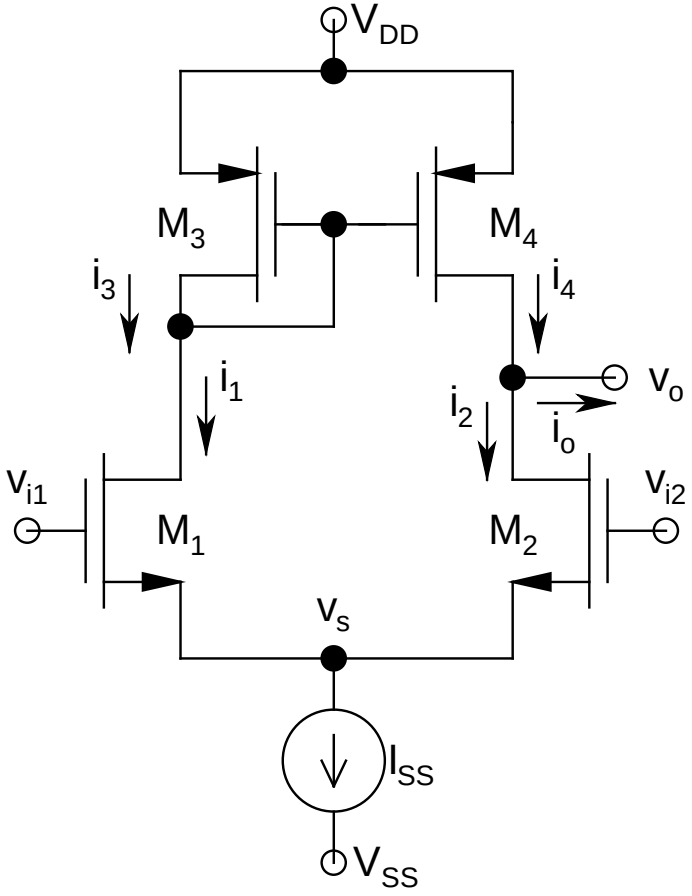
  $R_0 = r_{0n} || r_{0p} = (g_{0n} + g_{0p})^{-1}$

- ***Very high A_v and R_0***
- ***Extremely popular*** and ***widely used circuit***
- Sometimes, ***level shifters*** are used at the ***input*** for ***better ease*** of application

- ***Actively Loaded DA***:



BJT Implementation



MOS Implementation

- Absolutely ***similar topologies*** for ***both BJT and MOS implementations***
- ***Produces double-ended to single-ended conversion***, i.e., ***from two inputs to a single output***
- Q_1-Q_2/M_1-M_2/Q_3-Q_4/M_3-M_4 ***perfectly matched***
- ***Output should never be taken from collector/drain of*** Q_1/M_1 (***Why***?)
- ***DC biasing*** is ***absolutely straightforward*** with ***all branch currents equal to*** $I_{EE}/2$ ***or*** $I_{SS}/2$

- ***Caution***: ***Half-circuit technique can't be used for this circuit***, since ***collector/drain circuits of the two sides are coupled***, i.e., $i_3 = i_4$ (***always***)
- This circuit can be ***analyzed by inspection***
- ***Define*** $v_{id} = v_{i1} - v_{i2}$
- ***Apply*** $+v_{id}/2$ ***at the base of*** Q_1***/gate of*** M_1
- ***Apply*** $-v_{id}/2$ ***at the base of*** Q_2***/gate of*** M_2
- From ***symmetry*** of the circuit ***around the BE/GS loops***, the ***common emitter/source node*** is at ***ac ground*** (i.e., $v_e = v_s = 0$)

- Since $v_s = 0$, M_1-M_2 *won't have any body effect issue*
- Now, $i_3 = i_4$ (*mirror*), $i_3 = i_1$ (*same branch*), and $i_2 = -i_1$ (*symmetry*)
- Also, $i_1 = g_m v_{id}/2$ and $i_2 = -g_m v_{id}/2$

  $g_m = I_{EE}/(2V_T)$ (*BJT Implementation*)

  $= (k_N I_{SS})^{1/2}$ (*MOS Implementation*)
- Hence, the *short-circuit output current* (with the *output terminal shorted to ground*):

  $i_o = i_4 - i_2 = i_1 - i_2 = 2i_1 = g_m v_{id}$

- To find the ***output voltage***, we need to use the ***Thevenin technique***:
  - ***Open-Circuit Voltage*** = ***Short-Circuit Current*** × ***Thevenin Resistance***
- ***Thevenin Resistance*** (***looking from the output***):

  $R_0 = r_{02} \| r_{04}$
- Thus, the ***output voltage***:

  $v_o = i_o R_0 = g_m (r_{02} \| r_{04}) v_{id}$
- Hence, the ***differential-mode gain***:

  $A_{dm} = v_o / v_{id} = +g_m (r_{02} \| r_{04})$
- $R_i = 2r_\pi$ (***BJT Implementation***)

- ***Ex.***: ***Prove the expressions for A_{dm} and R_i from the hybrid-π model***
- ***A_{cm} for this circuit is a little difficult to evaluate***
- However, the ***CMRR can be safely approximated as***:

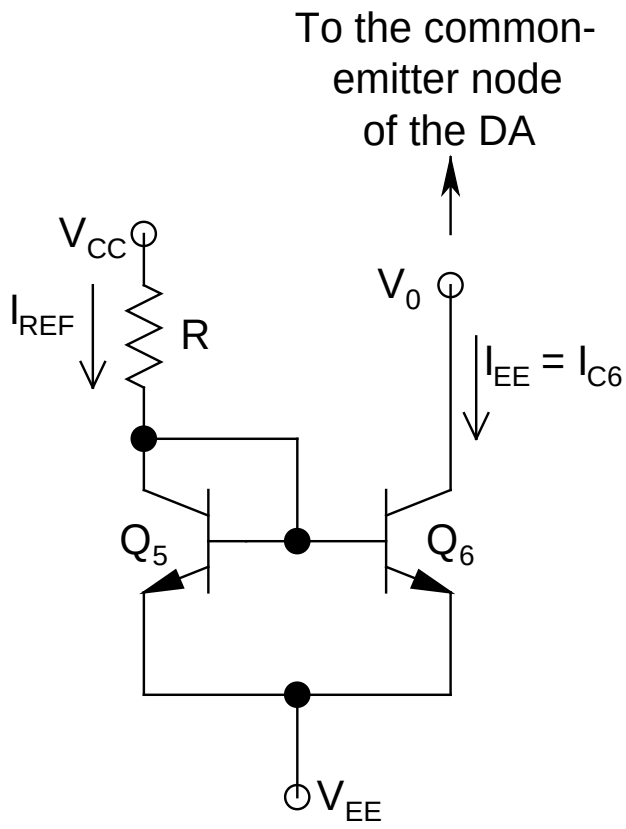
  $$CMRR \approx 20\log_{10}(2g_m R_{EE})$$

  R_{EE}: ***Output resistance of the bias current source I_{EE}/I_{SS}***
- In order to ***improve CMRR***, various ***current source topologies*** can be used

- ***Example***: ***Simple npn CM***
  - ***One of the simpler choices***
  - ***Q_5-Q_6 perfectly matched***
  - ***Neglecting base currents***:

    $I_{REF} = I_{EE} = I_{C6}$

    $= (V_{CC} - V_{BE} - V_{EE})/R$
  - $R_{EE} = r_{06} = V_A/I_{EE}$
  - Acts as a ***current source*** of ***magnitude I_{EE}*** with a shunt ***resistance R_{EE}***



- ***Insights***:
  - ***Recall***: A_{dm} ***independent of*** R_{EE}, but A_{cm} ***and CMRR strongly depend on*** R_{EE}
  - ***To maximize CMRR***, R_{EE} ***should be increased as much as possible***
  - ***To increase*** R_{EE}, other ***current sources*** discussed in class, e.g., ***ratioed mirror***, ***cascode***, ***Widlar***, etc., can be used
  - Note that with ***more advanced architectures***, V_0***(min) increases***, and may become a ***limiting factor***!