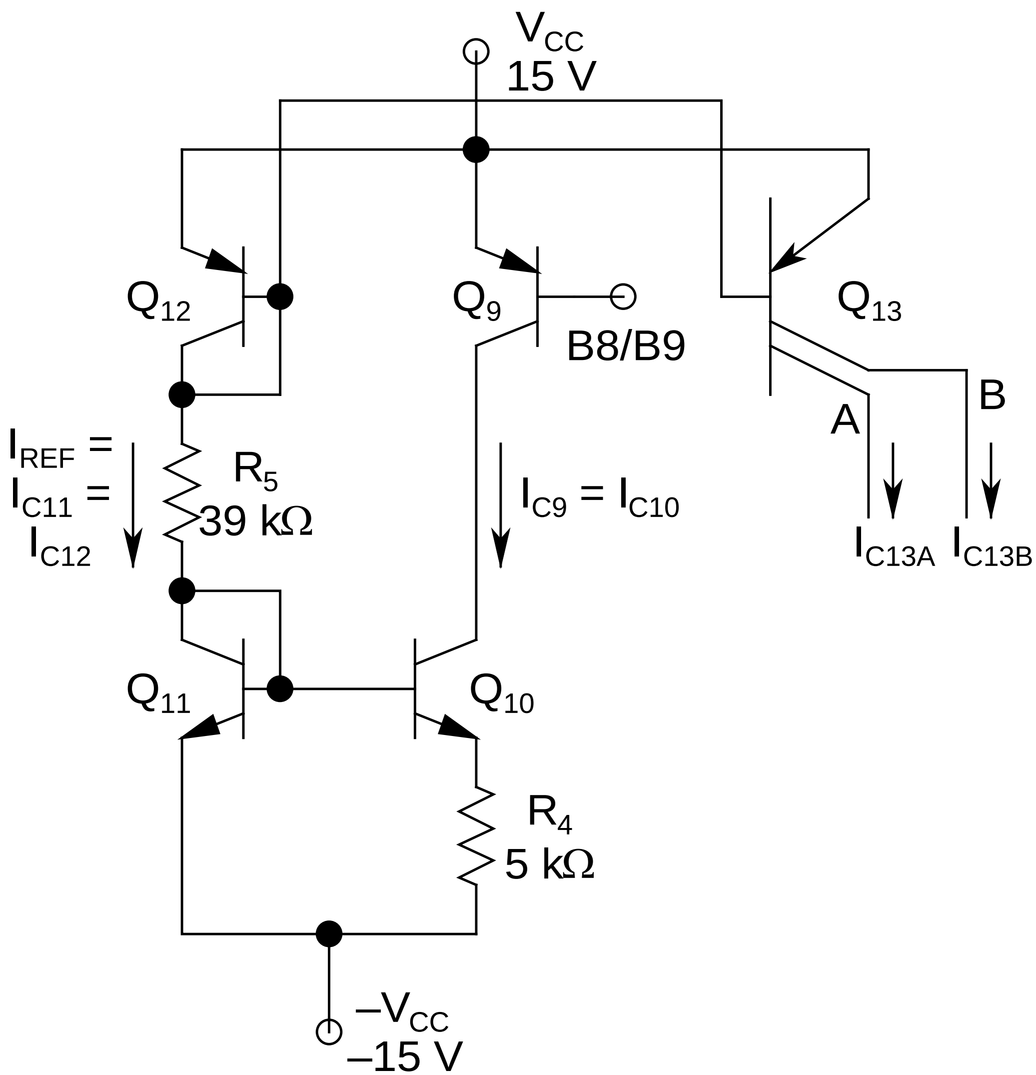


DC Biasing of the Main Branches

- Q_{10}-Q_{11}-R_4 ***combination*** is a ***Widlar current source***:

  $\Rightarrow V_T \ln(I_{REF}/I_{C10}) = I_{C10}R_4$

  $\Rightarrow I_{C10} = (V_T/R_4)\ln(I_{REF}/I_{C10})$

  Solution of this ***transcendental equation***:

  $I_{C10} = 19\ \mu A = I_{C9}$

- Q_{12}-Q_{13} another ***mirror***:

  $\Rightarrow I_{C13} = I_{C12} = I_{REF} = 733.3\ \mu A$

- Q_{13} is a ***special transistor***, having ***split collectors*** (A and B), with their ***area ratios*** 1:3

  $\Rightarrow I_{C13A} = 183.3\ \mu A$ and $I_{C13B} = 550\ \mu A$

➢ *DC Biasing of the Input Stage*:

- Q_8-Q_9 form a *current mirror*:

  $\Rightarrow I_{C8} = I_{C9} = I_{C10} = 19\ \mu A$

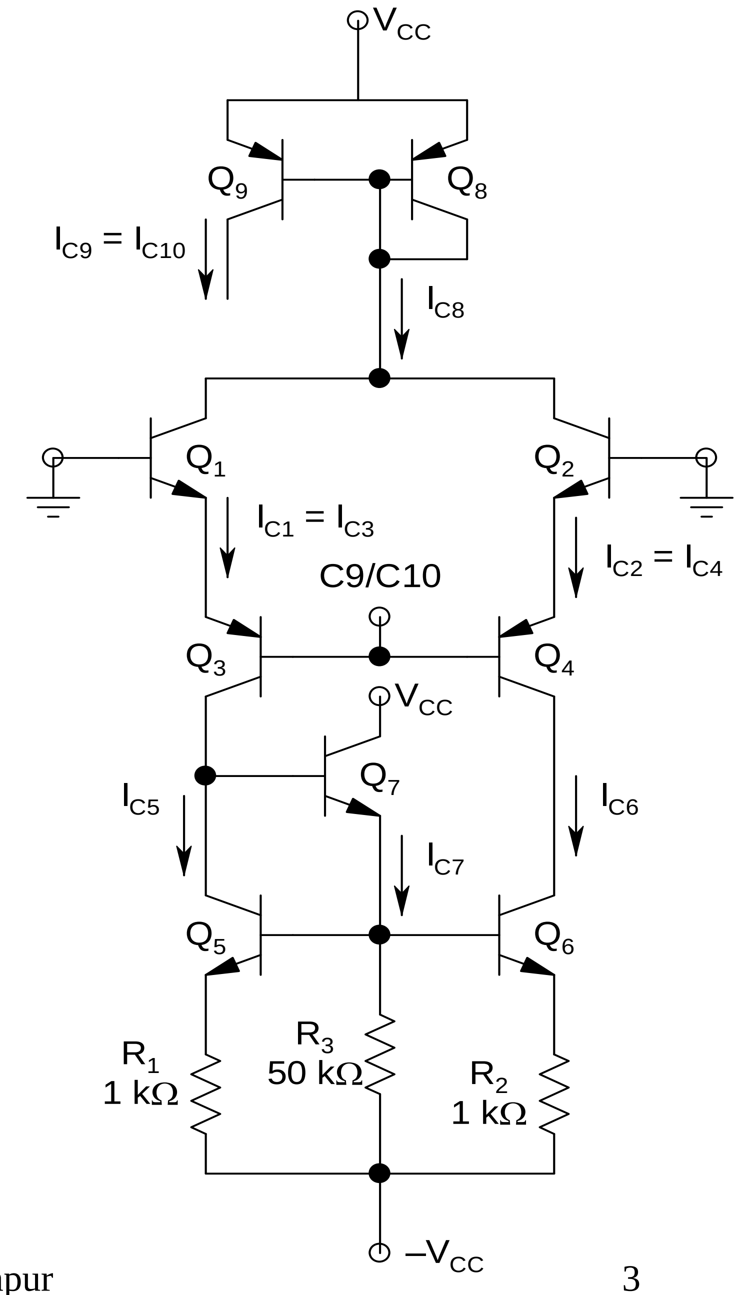
- This is the ***bias current*** for the ***DA***:

  $\Rightarrow I_{C1} = I_{C2} = I_{C3} = I_{C4}$

  $= I_{C5} = I_{C6} = I_{C8}/2$

  $= 9.5\ \mu A$

  $I_{C5} = I_{C6}$ (***since*** $R_1 = R_2$)



- ***Calculation*** of I_{C7} little more ***involved***
  - ***Neglecting base currents***, $I_{C7} \approx I_{R3}$
  - Assuming I_{S5} = 1 fA:

    $V_{BE5} = V_T \ln(I_{C5}/I_{S5}) = 597.3\ mV$
  - The ***drop*** across R_3:

    $V_{R3} = V_{BE5} + I_{C5}R_1 = 606.8\ mV$

    $\Rightarrow I_{C7} \approx I_{R3} = V_{R3}/R_3 = 12.1\ \mu A$

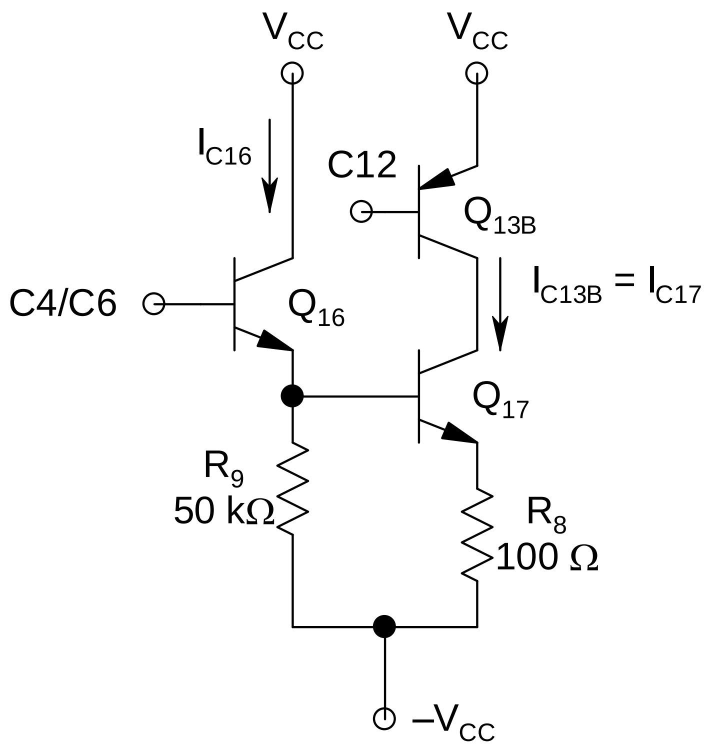
➢ *DC Biasing of the Gain Stage*:

- $I_{C17} = I_{C13B} = 550\ \mu A$
- This is a ***large current*** and the ***base current may not be negligible***
- Assuming $\beta_{17} = 200$:

  $I_{B17} = I_{C17}/\ \beta_{17} = 2.75\ \mu A$
- Assuming $I_{S17} = 1$ fA, the ***base voltage*** of Q_{17}, ***w.r.t. the negative power supply*** $(-V_{CC})$:

  V_{B17} (w.r.t. $-V_{CC}$) $\approx V_T \ln(I_{C17}/I_{S17}) + I_{C17}R_8$

  $= 757.9$ mV



- Thus:

  $I_{R9} = V_{B17}/R_9$

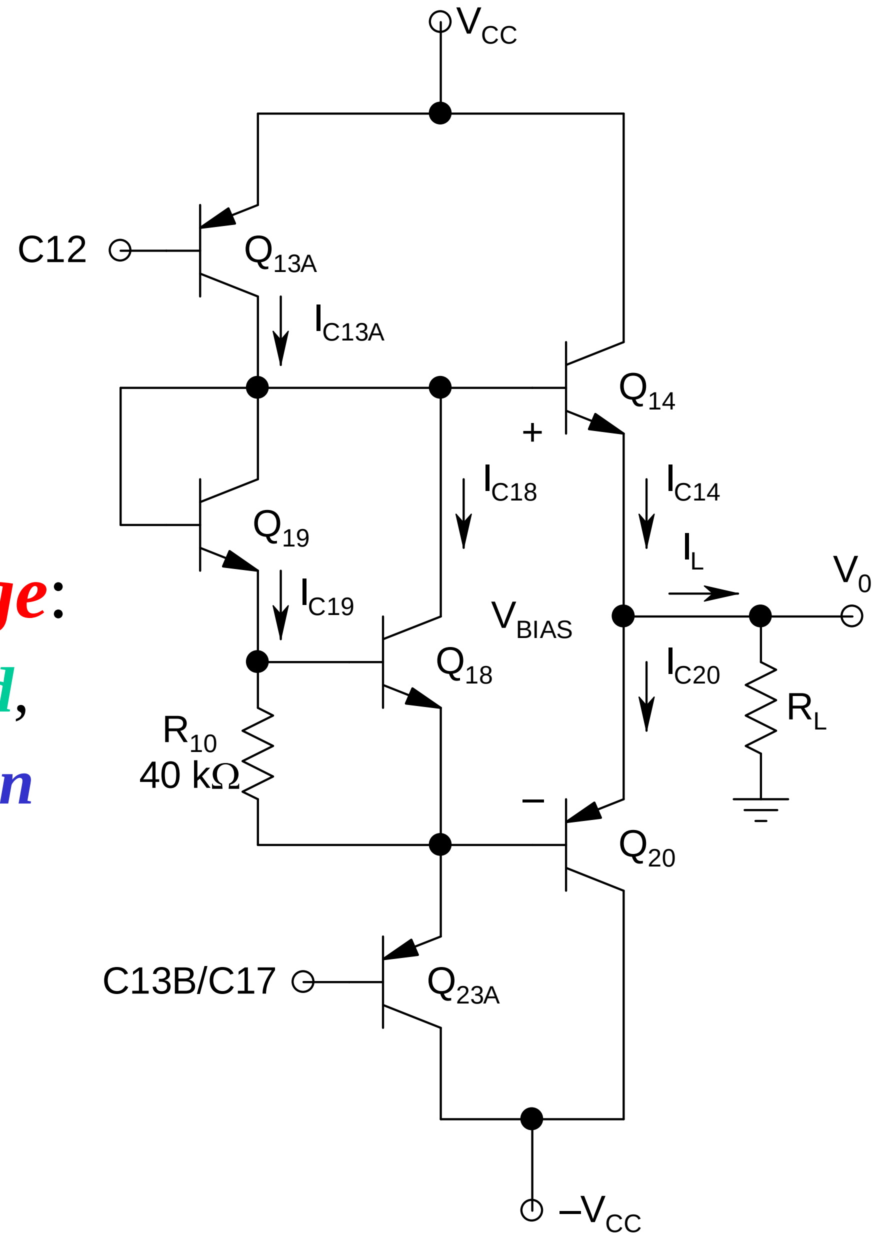
  $= 15.16\ \mu A$

  $\Rightarrow I_{C16} = I_{R9} + I_{B17}$

  $= 17.9\ \mu A$

➢ ***Finally, the output stage***:

- Q_{15}-Q_{21}-R_6-R_7 ***neglected***, since these are ***protection devices***, and ***come into play*** only during ***accidental short-circuiting of the output***



- To find the ***idling current***, R_L is ***removed***, thus making $I_L = 0$

  $\Rightarrow$ ***Standby (Idling) Current*** $= I_{C14} = I_{C20}$

- Q_{18}-Q_{19}-R_{10} is an ***extremely cleverly and innovatively designed block***

  - It produces a ***prebias voltage*** V_{BIAS} (***close to*** $2V_\gamma$) ***between the bases of*** Q_{14} ***and*** Q_{20}

  - At the same time, it ***reduces the standby power dissipation of the output branch***

- $I_{C13A} = 183.3\ \mu A$, and ***splits*** into Q_{18}-Q_{19} combination

- Assuming $V_{BE18} = 0.7$ V and for the time being, ***neglecting*** I_{B18}:

  $$I_{C19} \approx I_{R10} = V_{BE18}/R_{10} = 17.5\ \mu A$$

- Thus:

  $I_{C18} = I_{C13A} - I_{C19} = 165.8\ \mu A$ (***neglecting I_{B19}***)

- Since I_{C18} is ***pretty high***, we need to now ***fine tune*** our analysis by ***including I_{B18}***

- Assuming $I_{S18} = 1$ fA and $\beta = 200$:

  $I_{C19} = I_{B18} + I_{R10} = I_{C18}/\beta_{18} + (V_T/R_{10})\ln(I_{C18}/I_{S18})$

  $= 17.6\ \mu A$

- This is ***sufficiently close*** to our ***initial estimate*** of 17.5 μA

- Thus:

  $I_{C18} = I_{C13A} - I_{C19} = 165.7\ \mu A$

  which is ***almost same*** as our ***original estimate***

- $V_{BIAS} = V_{BE18} + V_{BE19} = V_{BE14} + V_{EB20}$
  $\Rightarrow V_T \ln(I_{C18}/I_{S18}) + V_T \ln(I_{C19}/I_{S19})$
  $= V_T \ln(I_{C14}/I_{S14}) + V_T \ln(I_{C20}/I_{S20})$
- ***Since $I_L = 0$***:

$$\Rightarrow I_{C14} = I_{C20} = \sqrt{\frac{I_{S14} I_{S20}}{I_{S18} I_{S19}}} \sqrt{I_{C18} I_{C19}}$$

- The ***sizes*** of the ***output transistors*** are typically ***much larger*** than the other devices, to be able to ***supply large current to the load without overheating***
- Assuming $I_{S14} = I_{S20} = 4I_{S18} = 4I_{S19}$:
  $I_{C14} = I_{C20} = 216\ \mu A$
- Thus, the ***idling*** (***standby***) ***power dissipation*** of the ***output branch*** = (30 V) × (216 μA) = 6.5 mW