

- $V_{\text{BIAS}} = V_{\text{BE18}} + V_{\text{BE19}} = V_{\text{BE14}} + V_{\text{EB20}}$   
 $\Rightarrow V_T \ln(I_{\text{C18}}/I_{\text{S18}}) + V_T \ln(I_{\text{C19}}/I_{\text{S19}})$   
 $= V_T \ln(I_{\text{C14}}/I_{\text{S14}}) + V_T \ln(I_{\text{C20}}/I_{\text{S20}})$
- *Since  $I_L = 0$ :*  

$$\Rightarrow I_{\text{C14}} = I_{\text{C20}} = \sqrt{\frac{I_{\text{S14}} I_{\text{S20}}}{I_{\text{S18}} I_{\text{S19}}}} \sqrt{I_{\text{C18}} I_{\text{C19}}}$$
- The *sizes* of the *output transistors* are typically *much larger* than the other devices, to be able to *supply large current to the load without overheating*
- Assuming  $I_{\text{S14}} = I_{\text{S20}} = 4I_{\text{S18}} = 4I_{\text{S19}}$ :  
 $I_{\text{C14}} = I_{\text{C20}} = 216 \mu\text{A}$
- Thus, the *idling (standby) power dissipation* of the *output branch*  $= (30 \text{ V}) \times (216 \mu\text{A}) = 6.5 \text{ mW}$

- Assuming  $I_{S18} = I_{S19} = 1 \text{ fA}$ :  

$$V_{\text{BIAS}} = V_T \ln[I_{C18} I_{C19} / (I_{S18} I_{S19})] = 1.285 \text{ V}$$
- This produces a *DC bias* of  $\sim 643 \text{ mV}$  across the *BE junctions* of  $Q_{14}$  and  $Q_{20}$ , keeping them at the *verge of conduction*
- Note that instead of the *prebias combination* used, if simply *two diodes* were used in *series*, then the *current* through that *branch* would have been  $183.3 \mu\text{A}$ , resulting in a current of  $733.2 \mu\text{A}$  in the *output branch*, thus creating *standby power dissipation* in the *output branch* of  $22 \text{ mW}$  ( $3.4 \text{ times}$ )
- Finally,  $I_{C23A} = I_{C13A} = 183.3 \mu\text{A}$

Transistor(s)	Magnitude ( $\mu\text{A}$ )
$I_{C1}, I_{C2}, I_{C3}, I_{C4}, I_{C5}, I_{C6}$	9.5
$I_{C7}$	12.1
$I_{C8}, I_{C9}, I_{C10}$	19
$I_{C11}, I_{C12}$	733.3
$I_{C13A}, I_{C23A}$	183.3
$I_{C13B}, I_{C17}$	550
$I_{C14}, I_{C20}$	216
$I_{C16}$	17.9
$I_{C18}$	165.7
$I_{C19}$	17.6

### The DC Bias Currents of Different Transistors

- The *DC power dissipation* of the circuit:

$$\begin{aligned} P_{DC} &= V_{CC} \times (I_{C12} + I_{C9} + I_{C8} + I_{C13A} + I_{C13B} + \\ &\quad I_{C14} + I_{C7} + I_{C16}) + \\ &\quad |-V_{CC}| \times (I_{C11} + I_{C10} + I_{C5} + I_{C7} + I_{C6} + \\ &\quad I_{R9} + I_{C17} + I_{C23A} + I_{C20}) \\ &= 52.3 \text{ mW} \end{aligned}$$

- Note that the *reference branch* consumes the *highest DC power*, followed by the *Darlington branch*
- On the other hand, the *least DC power* is consumed by the *DA branch*

- *ac Analysis:*
  - *Primary Goal:*
    - *To find  $R_i$ ,  $R_o$ , and  $A_{vOL}$*
  - We will adopt a *modular approach*:
    - *Considering each stage individually*
    - *Finding the 2-port equivalent for each of them*
    - *Eventually joining them together to get the total response*

➤ Assumed:

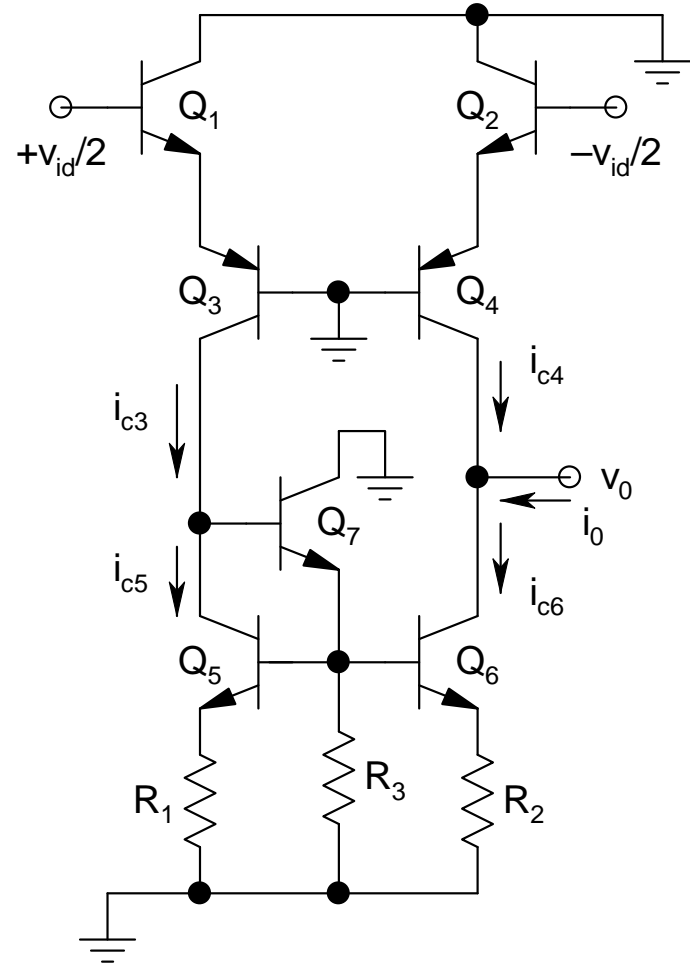
$$\beta_N = 200, \beta_P = 100, V_{AN} = 130 \text{ V}, V_{AP} = 50 \text{ V}$$

➤ We will also *evaluate* the *required value* of the *compensation capacitor*  $C_C$

➤ The *analysis* will be *simple* and *highly approximate*, however, the *results* will *definitely lie* within  $\pm 10\%$  of the *actual*

➤ **Input Stage:**

- *Differential-mode input*  
 $v_{id}$  *split* into  $+v_{id}/2$  and  $-v_{id}/2$ , and *applied* at the *bases* of  $Q_1$ - $Q_2$
- All *terminals* having *fixed DC potentials* have been tied to *ac ground*
- *Bases* of  $Q_3$ - $Q_4$  are at *ac ground* due to *perfect symmetry* of the circuit



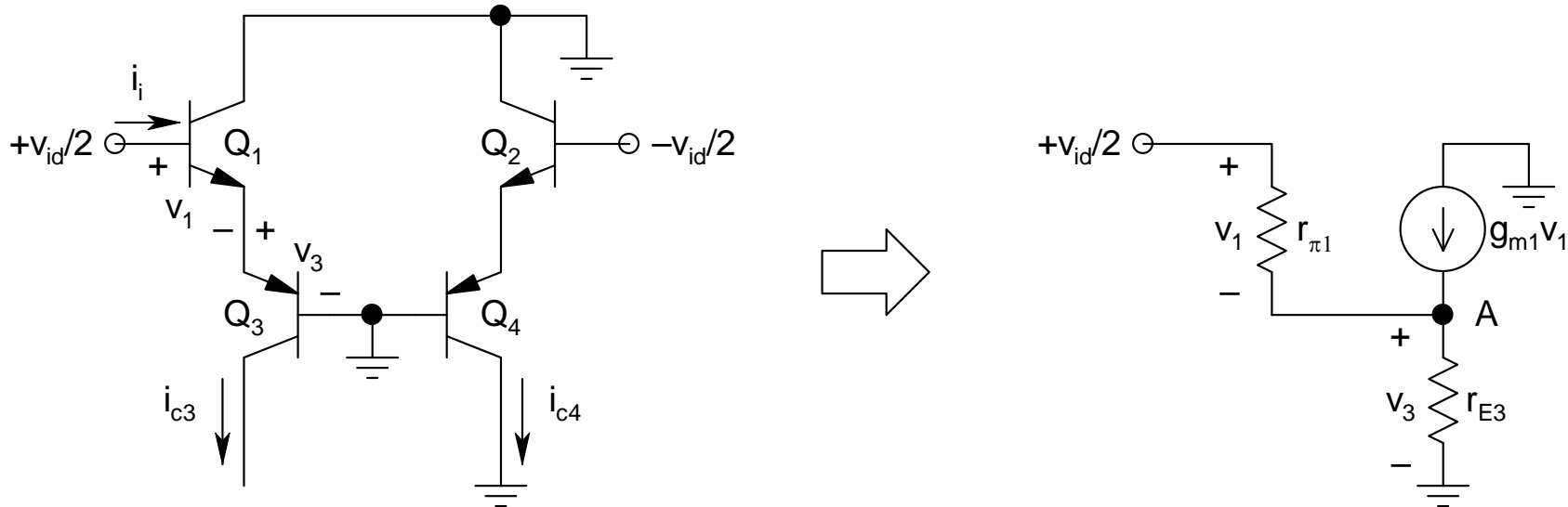
- $i_{c3} = i_{c5}$  (*neglecting base current of  $Q_7$* )

- $i_{c6} = i_{c5}$  (*ratioed mirror with  $R_1 = R_2$* )

- **Output current:**

$$i_0 = i_{c6} - i_{c4} = i_{c5} - i_{c4} = i_{c3} - i_{c4}$$

- To find the *short-circuit transconductance* of this stage, we *short the output node to ground*





- $v_{id}/2 = v_1 + v_3$

- ***KCL at node A:***

$$v_1/r_{\pi 1} + g_{m1}v_1 = v_3/r_{E3}$$

$$\Rightarrow v_1 = \frac{r_{\pi 1}}{r_{E3}} \frac{1}{1 + g_{m1}r_{\pi 1}} v_3 = \frac{r_{\pi 1}}{r_{E3}} \frac{1}{1 + \beta_1} v_3 \approx \frac{r_{\pi 1}}{\beta_1} \frac{1}{r_{E3}} v_3 \approx \frac{r_{E1}}{r_{E3}} v_3 = v_3$$

$$\Rightarrow v_{id} = 4v_3 \Rightarrow v_3 = v_{id}/4$$

$$\Rightarrow i_{c3} = g_{m3}v_3 = g_{m3}v_{id}/4 \text{ and } i_{c4} = -g_{m3}v_{id}/4$$

$$\Rightarrow i_0 = i_{c3} - i_{c4} = +g_{m3}v_{id}/2$$

- Thus, the ***short-circuit transconductance***:

$$G_{m1} \triangleq \left. \frac{i_0}{v_{id}} \right|_{v_0=0} = \frac{g_{m3}}{2} = \frac{I_{C3}}{2V_T} = 182.7 \mu S$$