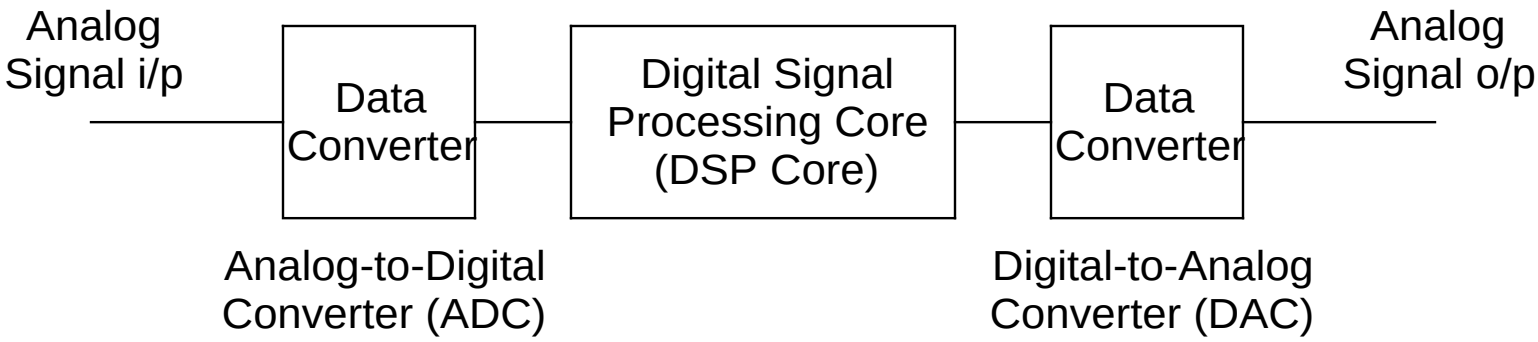
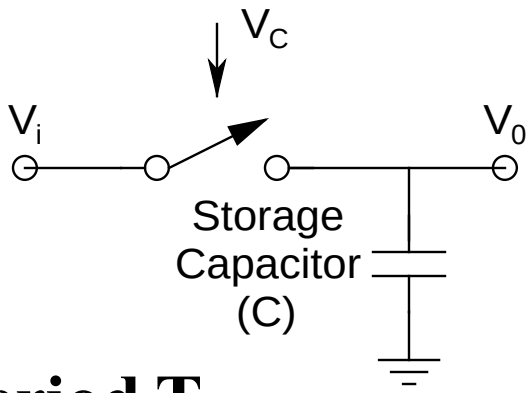
Data Converters

- Signals are of two types: ***Analog*** & ***Digital***
- ***Digital Signal Processing*** (**DSP**) is much easier, since we have to keep track of only ***1s and 0s***
- ***Analog signal processing*** is pretty tedious (Remember BJT Amplifiers?)
- Particularly, in ***communication systems***, **digital data transmission** produces almost ***error-free*** and ***noise-free*** operation

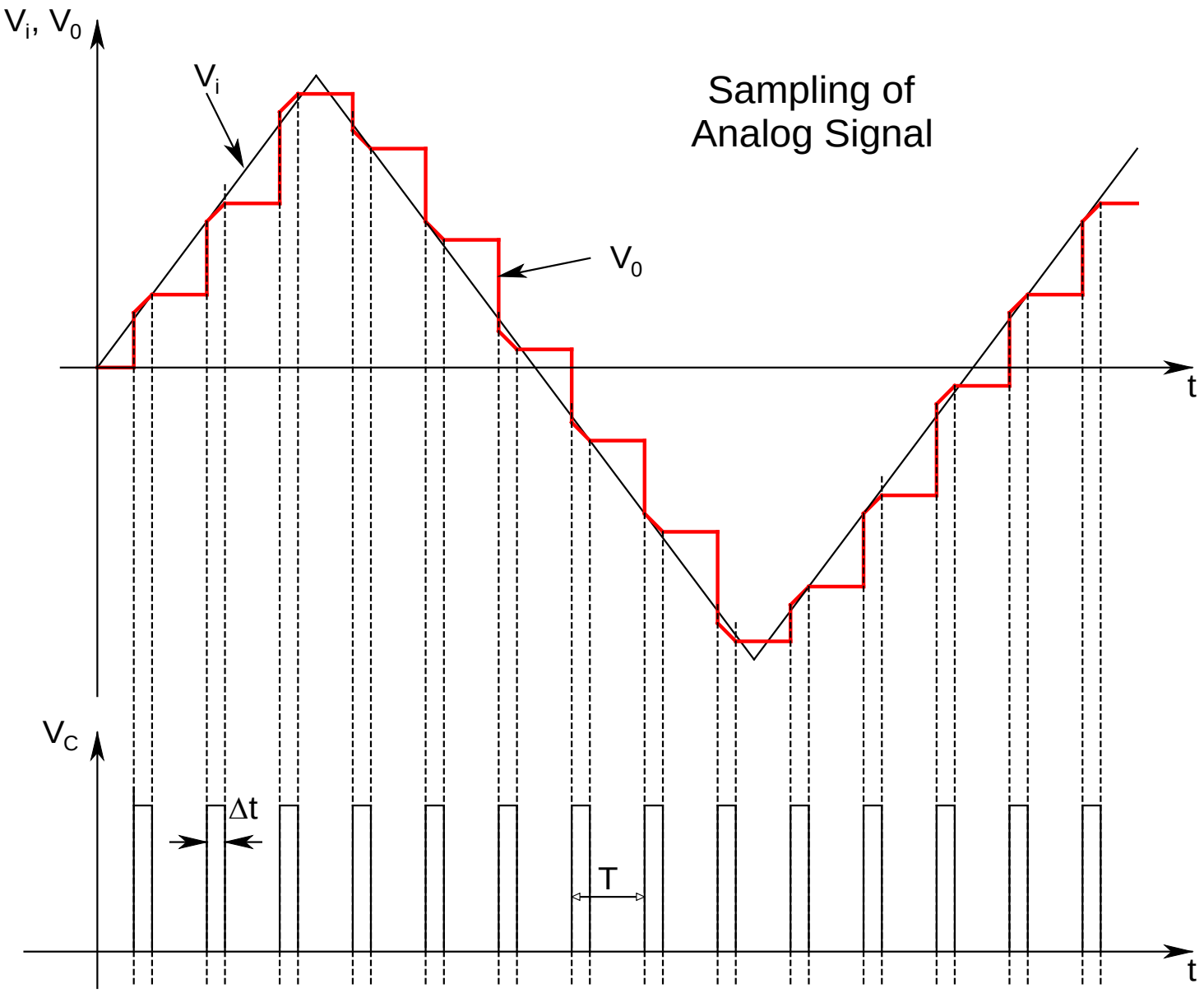
* There is very little chance that digital signals would get ***corrupted by noise*** (Remember Noise Margins?)
* Also, much less chance of ***signal interference*** in **digital transmissions**
* However, after the digital signal is ***processed***, we may still need the o/p in **analog form**, e.g., ***speech***
* Thus, the **basic signal processing architecture**:



Sampling of Analog Signals:



* Known as **Sample-and-Hold Circuit**
* V_C: ***Switch Control Signal***:
  - Makes the switch ***close periodically***
    * **Produces pulses of width Δt and period T**
* Δt: ***Sampling Interval***
* $f_{sampling}$ = ***Sampling Frequency*** = $1/T$
* $(T - \Delta t)$: ***Hold Interval***
  - **During this time, V_0 is fed to an ADC, and converted to corresponding digital signal**
* ***O/p is in N-bit binary form***


Sampling of
Analog Signal
V_i, V_0
V_i
V_0
t
V_C
Δt
T
t

Signal Quantization:

* Let an analog signal range from **0 to 10 V**, which needs to be converted to a **4-bit digital signal**
* ***Recall***: A **4-bit digital signal** can represent **16 equispaced values** (***from 0 to 15***)
* Thus, each value is ***spaced apart*** by $(10\ \text{V})/15$ = **0.67 V**, which corresponds to **1 LSB**
* This is known as **Resolution of Conversion**
* ***Chart***: $0000 \rightarrow 0.00$ V; $0001 \rightarrow 0.67$ V; $0010 \rightarrow 1.34$ V; $0100 \rightarrow 2.68$ V; $1000 \rightarrow 5.36$ V; $1010 \rightarrow 6.7$ V; $1100 \rightarrow 8.04$ V; $1110 \rightarrow 9.38$ V; $1111 \rightarrow$ 10 V

* ***Note***: For **each bit increment**, analog i/p range is **0.67 V**
* What happens if the analog signal lies **within a range**, e.g., let's say ***7 V***?
* Now, **1010 is 6.7 V** and **1011 is 7.37 V**
  - $\Rightarrow$ The o/p can be either of **1010 or 1011**
  - $\Rightarrow$ Either way, there is an ***error***, known as **Quantization Error** (***QE***)
* **QE = (Analog Full Scale) / ($2^N - 1$)**, where ***N = Number of bits***

* ***Obviously, this error can be reduced by increasing*** N
* ***Example***:
  - For $\mathbf{N = 16}$, $\mathbf{QE} = (10\ \mathrm{V})/(2^{16} - 1) = \mathbf{0.15\ mV}$
  - For $\mathbf{N = 32}$, $\mathbf{QE} = (10\ \mathrm{V})/(2^{32} - 1) = \mathbf{2.33\ nV}$

    (***vanishingly small***)
* ***Another way to express QE***: $\mathbf{\pm LSB/2}$
* ***Example***: $\mathbf{N = 4,\ QE = \pm 0.335\ V}$

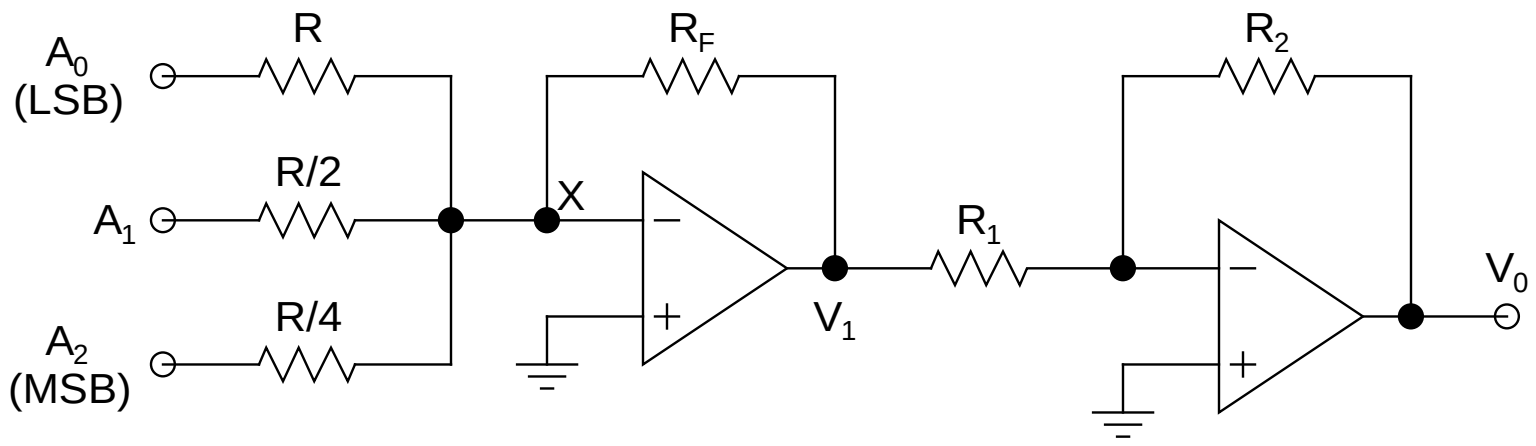
  $\mathbf{N = 16,\ QE = \pm 0.075\ mV}$

  $\mathbf{N = 32,\ QE = \pm 1.165\ nV}$

DAC:

* *Two types*:
  - **Binary Weighted**
  - **R-2R Ladder**

Binary Weighted DAC:



* $A_2\ A_1\ A_0$ are ***digital i/p bits***, which can be **either 0 or 1** (***logically***), equivalent to **0 V** **or some V_{REF}** (***Reference Voltage***)

* ***KCL at node X***:

$$\frac{V_{REF}\times A_0}{R}+\frac{V_{REF}\times A_1}{R/2}+\frac{V_{REF}\times A_2}{R/4}=-\frac{V_1}{R_F}$$

$$\Rightarrow V_1=-\frac{R_F}{R}\times\left(4A_2+2A_1+A_0\right)\times V_{REF}$$

* Thus, the ***output voltage***:

$$V_0=-\frac{R_2}{R_1}\times V_1=\frac{R_2R_F}{R_1R}\times\left(4A_2+2A_1+A_0\right)\times V_{REF}$$

$\Rightarrow$ **Binary Weighting**

* ***Note***: **Maximum weight is assigned to A_2**, which has the **least resistance** (***R*/*4***) attached to it, so that it draws the **maximum current** from the reference voltage $\rightarrow$ **MSB**

* Similarly, **minimum weight is assigned to A_0**, which has the **highest resistance** (***R***) attached to it, so that it draws the **minimum current** from the reference voltage $\rightarrow$ **LSB**

* ***Note***: If $R_1 = R_F$ and $R_2 = R$, then

$$V_0 = \left(4A_2 + 2A_1 + A_0\right) \times V_{REF}$$

Design Example:

* Let $V_0(\text{max}) = 5$ V

  $\Rightarrow$ $A_2A_1A_0 = 111$ should correspond to 5 V

  $\Rightarrow$ $V_{REF} = (5\text{ V})/(4+2+1) = 0.714$ V

* For $A_2A_1A_0 = 000$, $V_0 = 0$, while for $A_2A_1A_0$

  $= 001$, $V_0 = 0.714\text{ V} = (5\text{ V})/(2^3 - 1)$

  $\Rightarrow$ For each bit increment, V_0 jumps by 0.714 V

  $\Rightarrow$ Resolution of the DAC = 0.714 V

* ***Note***: For $A_2A_1A_0 = 100$, $V_0 = 2.856\text{ V} \neq V_0(\text{max})/2$

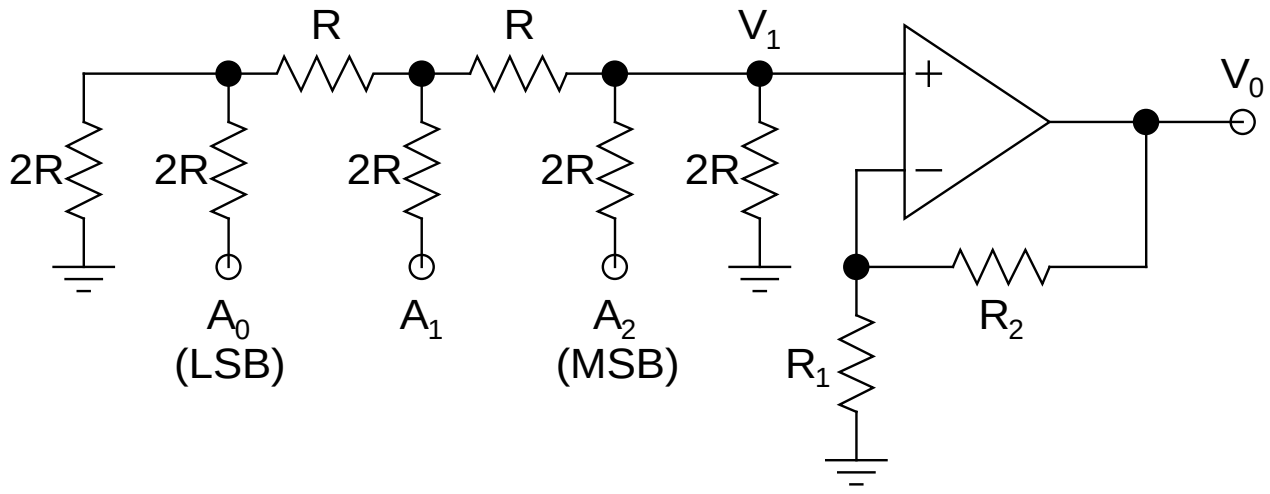
R-2R Ladder DAC:

* For additional i/p bits, the resistors scale as

  R*/*8, ***R*/*16***, ***R*/*32***, and so on

  $\Rightarrow$ Becomes a very ***clumsy*** design

* ***Remedy***: **R-2R Ladder DAC**



* Uses resistors of values ***R and 2R only***, and a ***single op-amp*** (OA)
* **MSB** (A_2) is ***closest*** to the OA, while **LSB** (A_0) is ***furthest*** from it
* A_0 A_1 A_2 connected to **either 0 or V_{REF}** (***logic 0 or 1***)
* ***Show that***:
  - $V_1\big|_{A_2=1 \text{ and } A_1=A_0=0} = \left(A_2/3\right)\times V_{REF}$
  - $V_1\big|_{A_1=1 \text{ and } A_2=A_0=0} = \left(A_1/6\right)\times V_{REF}$
  - $V_1\big|_{A_0=1 \text{ and } A_2=A_1=0} = \left(A_0/12\right)\times V_{REF}$

* Thus, by ***superposition***:
  - $V_1 = (1/12)(4A_2 + 2A_1 + A_0) \times V_{REF}$
* The OA is ***non-inverting***, with gain:

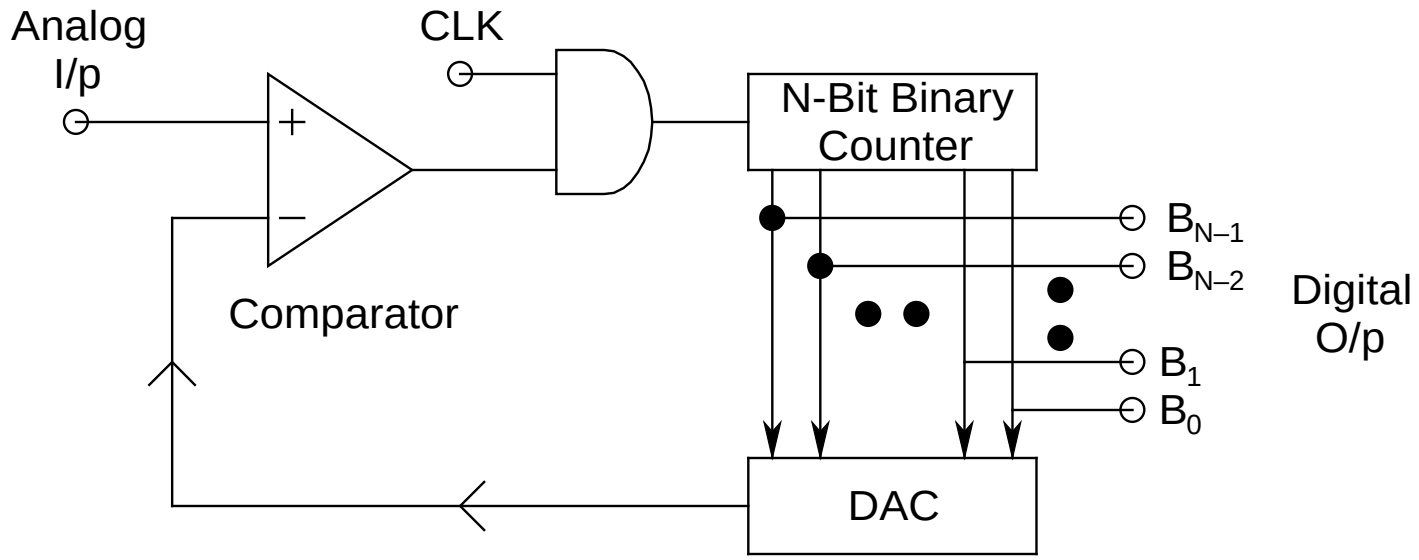
  $V_0/V_1 = 1 + R_2/R_1$
* Choose $R_2/R_1 = 11$

  $\Rightarrow V_0 = (4A_2 + 2A_1 + A_0) \times V_{REF}$
* The result is exactly same as that obtained in the previous case, but using resistors of ***only 2 values*** (**R and 2R**)
* ***Extremely popular DAC and heavily used***

ADC:

* Various options available, out of which, we will be discussing two of them:
  - **Counting Type**
  - **Flash** (or ***Parallel Comparator***)

Counting Type:



* ***Note***: It employs a **DAC** within it

Operating Principle:

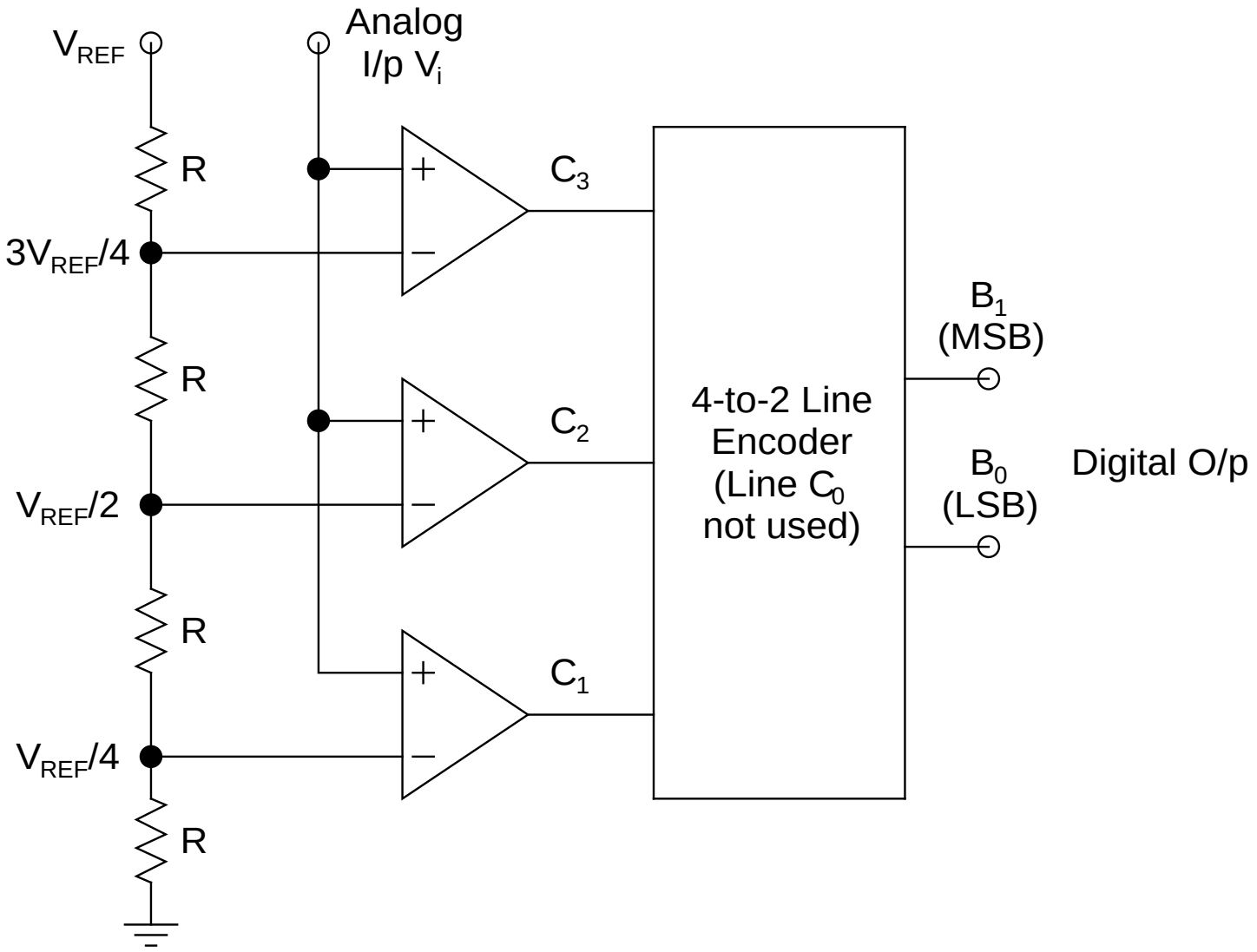
* Initially, the Binary Counter is **reset** (***all o/ps zero***)
* Thus, ***DAC o/p = 0***, fed back to the comparator
* ***Comparator o/p high*** $\Rightarrow$ CLK is allowed to pass to the counter through the AND gate
* The counter ***starts counting*** and ***increments by 1*** at ***each CLK pulse***
* DAC ***converts*** this digital o/p to its ***analog equivalent*** and feeds it back to the comparator, which ***compares*** it with the analog i/p signal

* So long as the analog i/p signal is ***greater*** than the DAC o/p, the o/p of the comparator remains ***high***, and the counter keeps on ***counting***
* As soon as the DAC o/p becomes ***greater*** than the analog i/p signal, the comparator o/p goes ***low***, and the CLK signal is ***prevented*** from reaching the i/p of the counter $\Rightarrow$ the count ***stops***
* At that instant of time, the ***binary o/p is taken out***, and immediately thereafter the ***counter is reset***, which ***starts the counting process again***

* ***Note***: During the entire conversion period, the analog i/p ***should not change***, i.e., it must be held **constant**
* Implemented using a **Sample-and-Hold (S/H) circuit**, with its ***hold time at least equal to or greater than the conversion time of the ADC***
* ***Note***: The conversion time itself is a function of the analog i/p (**smaller value leads to quicker conversion** and vice-versa)

* As soon as the count ***stops***, the **Hold** of the S/H circuit is ***released***, and it samples and holds the ***next*** analog data for conversion
* Needs a maximum of $\left(2^N - 1\right)$ ***CLK cycles for N-bit data***
* ***Quite slow***, if the analog i/p voltage is large, since the **count has to always start from zero**
* ***Advantage***: **Very simple design** and **needs very limited hardware** $\Rightarrow$ ***costs less***

Flash (Parallel Comparator):



* ***Fastest ADC availabe to date***

* ***Note***:

  - For $0 < V_i < V_{REF}/4$:

    $C_1 = C_2 = C_3 = 0$

  - For $V_{REF}/4 < V_i < V_{REF}/2$:

    $C_1 = 1, C_2 = C_3 = 0$

  - For $V_{REF}/2 < V_i < 3V_{REF}/4$:

    $C_1 = C_2 = 1, C_3 = 0$

  - For $V_i > 3V_{REF}/4$:

    $C_1 = C_2 = C_3 = 1$

* The ***4-to-2 Line Encoder*** takes these as i/ps and produces **2-bit binary output**

* ***Encoding Scheme***:

			MSB	**LSB**
C_3	C_2	C_1	B_1	B_0
0	0	0	0	0
0	0	1	0	1
0	1	1	1	0
1	1	1	1	1

* The entire operation is done **parallely** (***in a flash***)

  $\Rightarrow$ Known as a **Parallel Comparator** (or ***Flash***) ADC

* ***Note***: **QE** (or ***Resolution***) = $\pm V_{REF}/8$

* Number of comparators needed = $\left(\mathbf{2^N - 1}\right)$ for

  N-bit digital o/p

  $\Rightarrow$ For **8-bit** digital o/p, need **255** comparators!!!

  $\Rightarrow$ One of the major ***drawbacks*** of flash ADC, i.e., **hardware requirement** (and thus, the **cost**) is ***huge***

  $\Rightarrow$ ***Use limited to 8-bit o/p***

* ***Note***: Needs only **one** clock cycle for data conversion

  $\Rightarrow$ ***Extremely fast***