- ***Gate-Source and Gate-Drain Capacitance*** (C_{gs} and C_{gd}):
  - Each has ***two components***: ***intrinsic*** (i) and ***technological*** (t)
  - ***Total intrinsic gate-body capacitance***:

    $$C_{gbi} = C'_{ox}WL$$

  - Using ***Meyer's model***, ***intrinsic component***:
    - In ***linear region***: $C_{gsi} = C_{gdi} = C_{gbi}/2$
    - In ***saturation region***: $C_{gsi} = (2/3)C_{gbi}$, $C_{gdi} = 0$
  - ***Technology component arises due to gate-source and gate-drain overlap*** (L_D)

- ***Technology components***:

$$C_{gst} = C_{gdt} = C'_{gs0}W = C'_{gd0}W$$

Gate-Source/Drain Overlap Capacitance per unit width: $C'_{gs0} = C'_{gd0} = C'_{ox}L_D$

- Thus, ***total capacitance in saturation***:

$$C_{gs} = (2/3)C'_{ox}WL + C'_{gs0}W$$

$$C_{gd} = C'_{gd0}W$$

- $\boldsymbol{C_{gs} >> C_{gd}}$

- ***Source-Body and Drain-Body Capacitance*** (C_{sb} and C_{db}):
  - ***Both reverse-biased n^+p junctions***

$$C_{sb} = \frac{C_{sb0}}{\left(1+V_{SB}/V_0\right)^m} \quad \text{and} \quad C_{db} = \frac{C_{db0}}{\left(1+V_{DB}/V_0\right)^m}$$

$$C_{sb0} = C_{sb}\big|_{V_{SB}=0} \quad \text{and} \quad C_{db0} = C_{db}\big|_{V_{DB}=0}$$

$$V_{SB} \text{ and } V_{DB} \geq 0$$

- ***Drain/Source Series Resistance*** (R_S and R_D):
  - ***Due to neutral n^+ source/drain regions***

The Hybrid-π Model