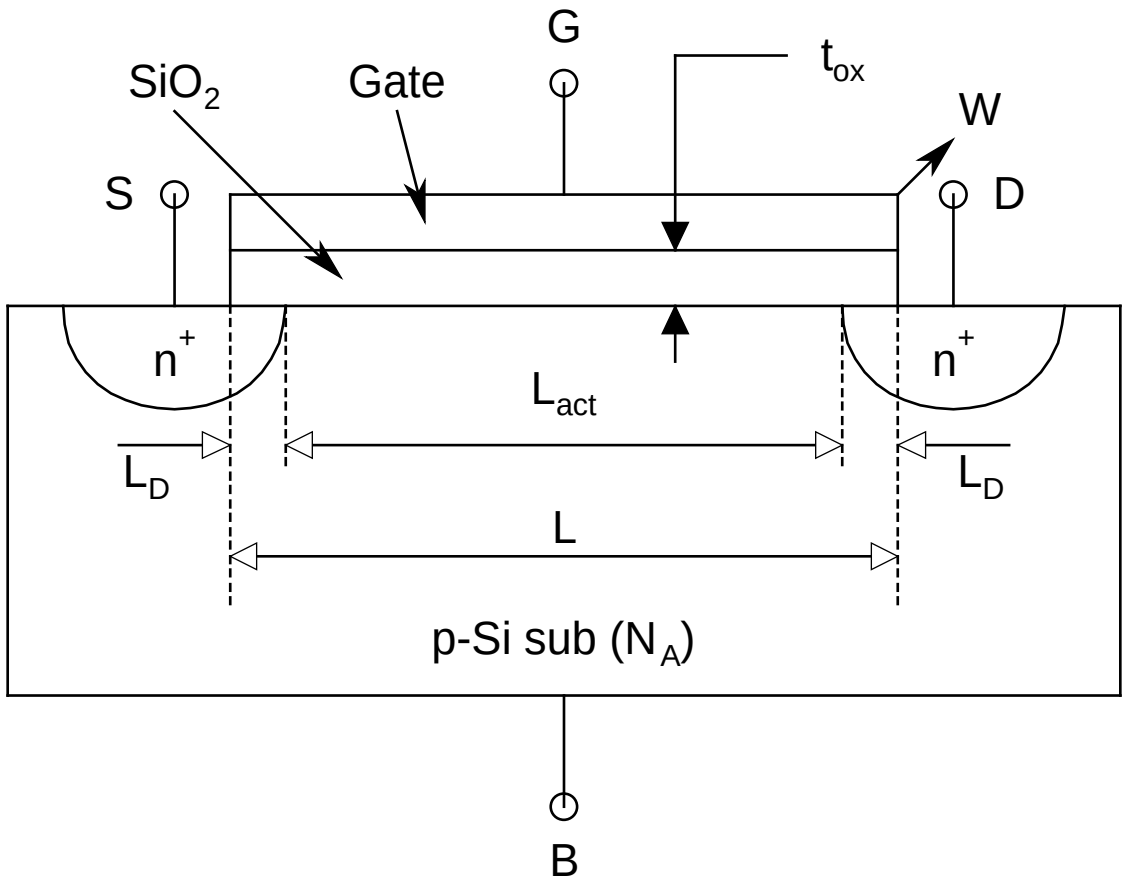
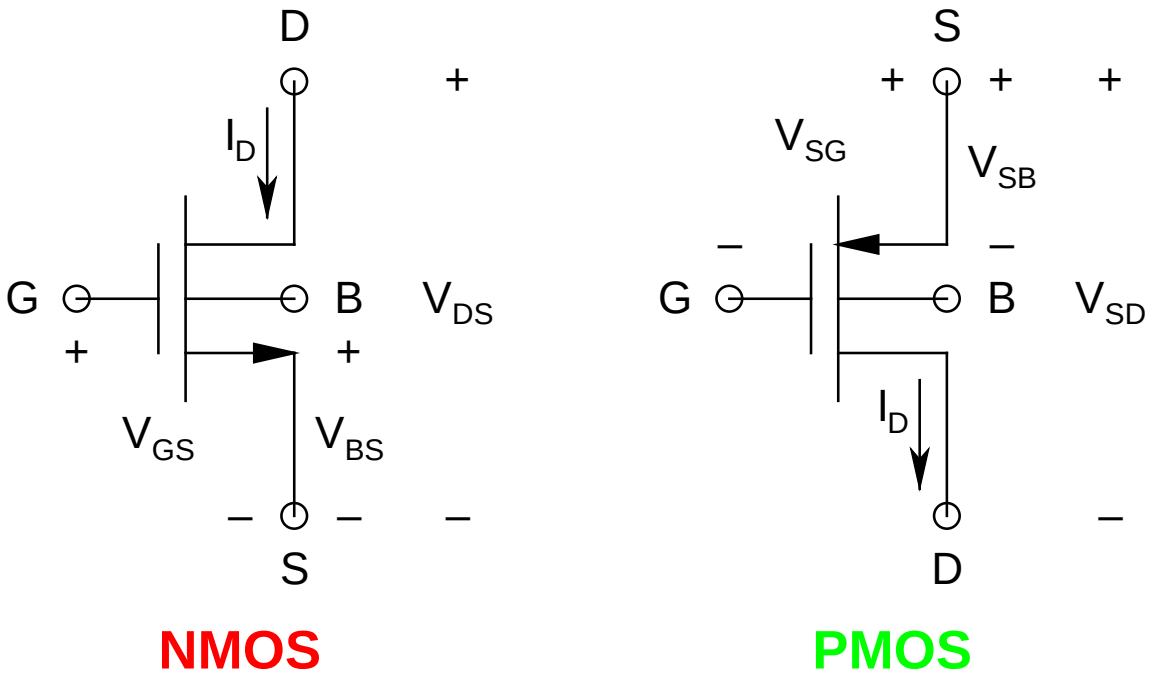
NMOS Structure



- ***Technology Parameters***:
  - ***Channel Length*** (L)
  - ***Channel Width*** (W)
  - ***Oxide Thickness*** (t_{ox})
  - ***Substrate Doping*** (N_A)
- L_D: ***Lateral overlap*** between G and S/D
- ***Actual*** channel length: $L_{act} = L - 2L_D$
- For now, we will assume $L_D = 0$
  - $L_{act} = L$

Symbols and Current-Voltage Conventions



- ***Voltage Convention***:
  - ***NMOS***: V_{GS} (***gate-source voltage***), V_{DS} (***drain-source voltage***), V_{BS} (***body-source voltage***)
  - ***PMOS***: V_{SG} (***source-gate voltage***), V_{SD} (***source-drain voltage***), V_{SB} (***source-body voltage***)
- ***Current Convention***:
  - ***NMOS***: I_D (***drain current***) flows into the ***drain terminal*** and exits from the ***source terminal***
  - ***PMOS***: I_D flows into the ***source terminal*** and exits from the ***drain terminal***

- ***Gate is DC isolated by the insulator***
  - ***Gate Current $I_G = 0$***
  - ***Tremendous advantage***!
- ***Same current I_D flows through the device***
- ***Extremely compact device***
  - ***Saves a lot of area***
- ***Reversible device***:
  - ***D and S terminals are determined by their bias states***