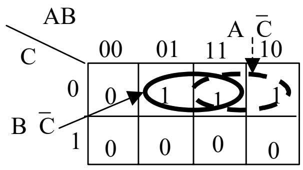
Soln

1.: If w; x; y; z are switches 1,2,3,4 respectively, you will get the function as $f = x\bar{y}z + wyz$.

2. Let A = Fair Weather
B = Instrument Capability
C = Air Controllers Strike
D = Take Off
Rest states are don't care: $D = A\bar{C} + B\bar{C} = \bar{C}(A+B)$



3. Implement using 3X8 decoder and 3 input OR gate

$X = \bar{A}C + B\bar{C} = A\bar{B}C + B\bar{C}(A + \bar{A}) = A\bar{B}C + AB\bar{C} + \bar{A}B\bar{C}$

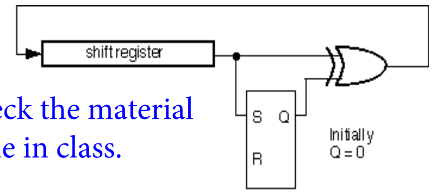
$Y = \bar{B}C + A\bar{C} = \bar{B}C(A + \bar{A}) + A\bar{C}(B + \bar{B}) = A\bar{B}C + \bar{A}\bar{B}C + AB\bar{C} + A\bar{B}\bar{C}$

$Z = AB\bar{C} + \bar{A}B = AB\bar{C} + \bar{A}B(C + \bar{C}) = A\bar{B}C + \bar{A}BC + \bar{A}B\bar{C}$

Use 3-input OR for X and Z and Two 3-input OR gates for Y.

4. The 2's complement of a binary number can be formed by leaving all least significant 0's and the first 1 unchanged and complementing all other higher significant bits. The circuit needs a shift register to store the binary number and an RS flip-flop to be set when the first least significant 1 occurs. An exclusive-OR gate can be used to transfer the unchanged bits or complement the bits.

Check the material done in class.



5. (a) Use an XOR of S&R and AND it with Ck (i.e. same status as the 0,0 inputs) to send to the Ck input to the SR-latch.

5 (b) From the truth table shown of JK Flip-Flop, $Q_{n+1}=1$ for rows 3 ($J_n=1$, $K_n=0$) and row 4(for $Q_n=0$) Or Q_{n+1}=(row3&4) $Q_{n+1} = \bar{Q}_n J_n(\bar{K}_n + K_n)$. Again $Q_{n+1} = Q_n \bar{K}_n(J_n + \bar{J}_n)$ from Row 1(for $Q_n=1$) and 3.

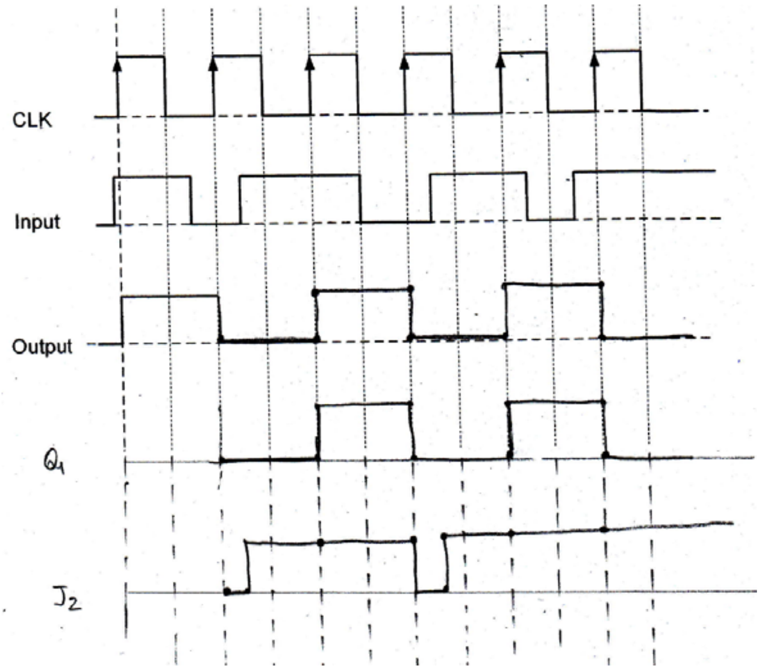
Hence $Q_{n+1} = \bar{Q}_n J_n + Q_n \bar{K}_n$.

J_n	K_n	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	$\bar{Q}_n$

6.

Charocteristic table of J-K flip flop

J	K	Q(t+1)
0	0	Q(t)
0	1	0
1	0	1
1	1	$\overline{Q(t)}$



7.

Excitation Table for D F/F

Q(t)	Q(t+1)	D
0	0	0
0	1	1
1	0	0
1	1	1

State Transition Table

Present State $Q_A(n)$	$Q_B(n)$	$Q_C(n)$	Next State $Q_A(n+1)$	$Q_B(n+1)$	$Q_C(n+1)$	Inputs D_A	D_B	D_C
0	1	0	1	1	0	1	1	0
1	1	0	0	0	1	0	0	1
0	0	1	0	1	1	0	1	1
0	1	1	0	1	0	0	1	0
~~0~~	~~1~~	~~0~~						

D_A

$Q_A \backslash Q_BQ_C$	00	01	11	10
0	X	0	0	1
1	X	X	X	0

D_B

$Q_A \backslash Q_BQ_C$	00	01	11	10
0	X	1	1	1
1	X	X	X	0

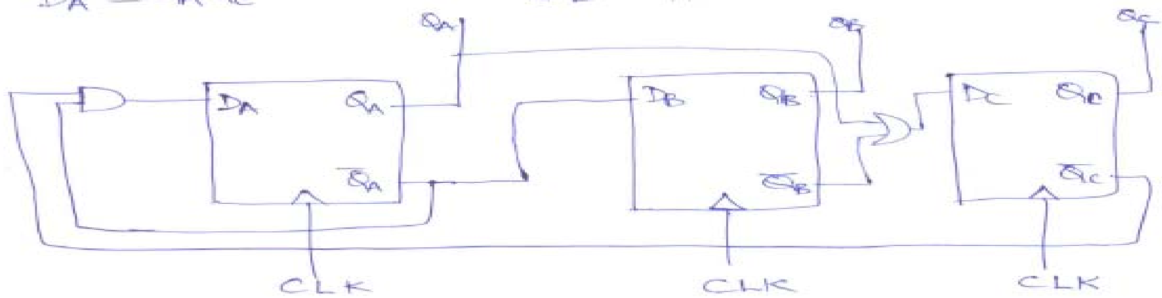
D_C

$Q_A \backslash Q_BQ_C$	00	01	11	10
0	X	1	0	0
1	X	X	X	1

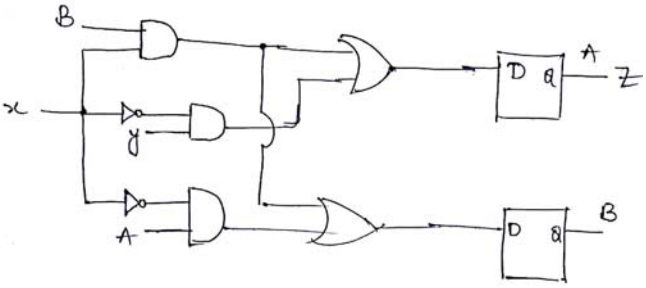
$D_A = \overline{Q_A}\,\overline{Q_C}$

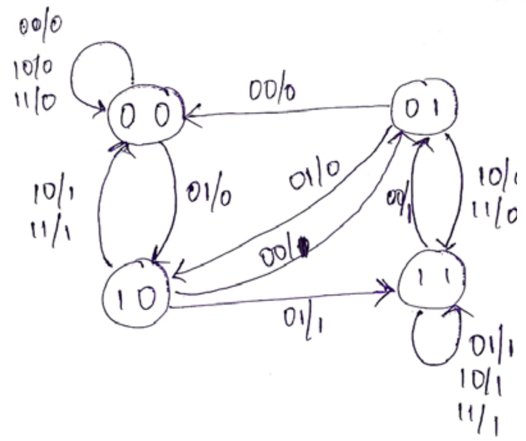
$D_B = \overline{Q_A}$

$D_C = Q_A + \overline{Q_B}$



8.





Present state A	B	Input x	y	Next state A	B	Z
0	0	0	0	0	0	0
0	0	0	1	1	0	0
0	0	1	0	0	0	0
0	0	1	1	0	0	0
0	1	0	0	0	0	0
0	1	0	1	1	0	0
0	1	1	0	1	1	0
0	1	1	1	1	1	0
1	0	0	0	0	1	1
1	0	0	1	1	1	1
1	0	1	0	0	0	1
1	0	1	1	0	0	1
1	1	0	0	0	1	1
1	1	0	1	1	1	1
1	1	1	0	1	1	1
1	1	1	1	1	1	1

9.

X	Y	Q_{n+1}	J	K
1	0	Q_n	0	0
0	1	1	1	0
1	1	0	0	1
0	0	$\overline{Q_n}$	1	1

Express J & K in terms of X & Y

J

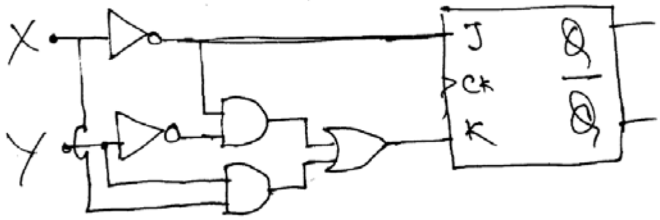
Y \ X	0	1
0	1	0
1	1	0

$J = \overline{X}$

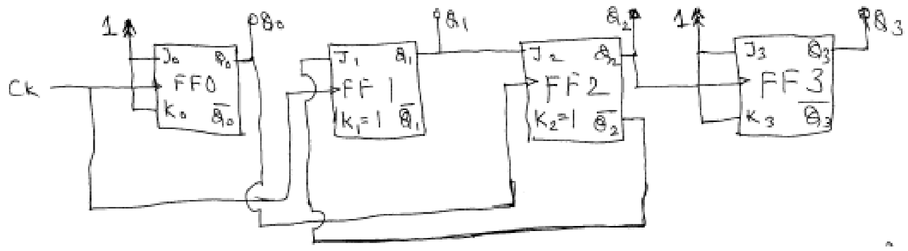
K

Y \ X	0	1
0	1	0
1	0	1

$K = \overline{X}\,\overline{Y} + XY$



10.



	Q_3	Q_2	Q_1	Q_0	J_0	K_0	Ck_0	$J_1=\overline{Q_2}$	K_1	Ck_1	$J_2=Q_1$	$K_2=1$	$Ck_2=Q_0$	$J_3=1$	$K_3=1$	$Ck_3=Q_2$
Pulse 1 →	0	0	0	0	1	1	0	1	1	0	0	1	0	1	1	0
Pulse 2 →	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0
Pulse 3 →	0	1	0	0	1	1	2	0	1	2	0	1	0	1	1	1
Pulse 4 →	1	1	0	1	1	1	3	0	1	3	0	1	1	1	1	1
	0	0	0	0	1	1	4	1	1	4	0	1	0	1	1	0
	0	0	1	1	1	1	5	1	1	5	1	1	1	1	1	0
	0	1	0	0	1	1	6	0	1	6	0	1	0	1	1	1
	1	1	0	1	1	1	7	0	1	7	0	1	1	1	1	1
	0	0	0	0												

Count of 4

11.

Present state			Next state					
A	B	C	A	B	C	T_A	T_B	T_C
0	0	0	0	0	1	0	0	1
0	0	1	0	1	1	0	1	0
0	1	1	1	1	1	1	0	0
1	1	1	1	1	0	0	0	1
1	1	0	1	0	0	0	1	0
1	0	0	0	0	0	1	0	0

T_A

A \ BC	00	01	11	10
0	0	0	1	X
1	1	X	0	0

$T_A = \overline{A}\cdot B + A\cdot\overline{B}$

T_B

A \ BC	00	01	11	10
0	0	1	0	X
1	0	X	0	1

$T_B = \overline{B}\cdot C + B\overline{C}$

T_C

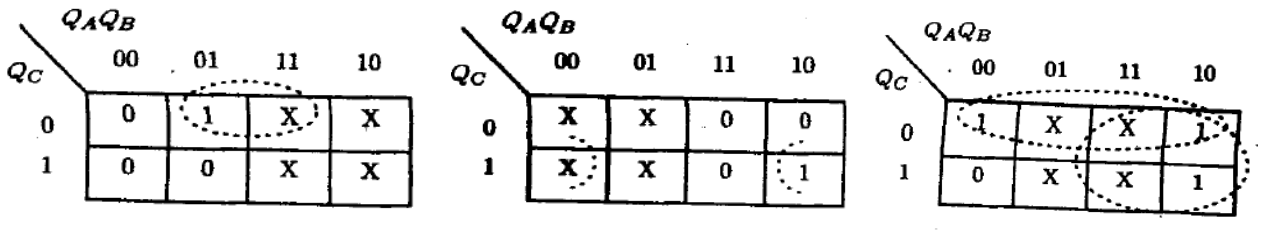
A \ BC	00	01	11	10
0	1	0	0	X
1	0	X	1	0

$T_C = \overline{A}\,\overline{C} + AC$

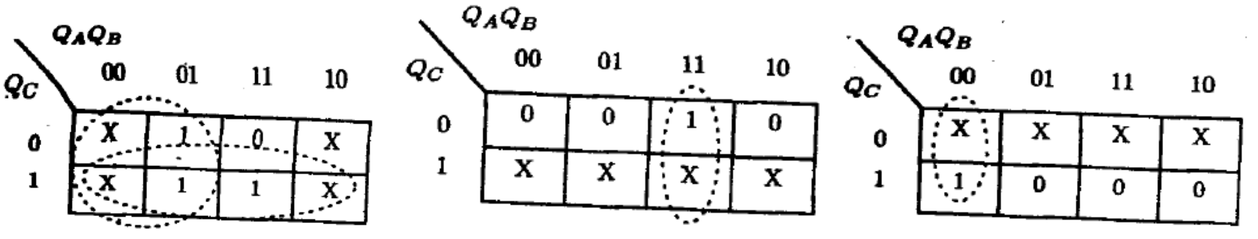
12.

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Time n			Time $n+1$			Required inputs					
Q_A	Q_B	Q_C	Q_A	Q_B	Q_C	J_A	K_A	J_B	K_B	J_C	K_C
0	0	0	0	1	0	0	X	1	X	0	X
0	1	0	1	0	0	1	X	X	1	0	X
1	0	0	1	1	0	X	0	1	X	0	X
1	1	0	1	1	1	X	0	X	0	1	X
1	1	1	1	0	1	X	0	X	1	X	0
1	0	1	0	1	1	X	1	1	X	X	0
0	1	1	0	0	1	0	X	X	1	X	0
0	0	1	0	0	0	0	X	0	X	X	1
0	0	0									



$J_A = Q_B\bar{Q}_C$ $K_A = \bar{Q}_B Q_C$ $J_B = Q_A + \bar{Q}_C$

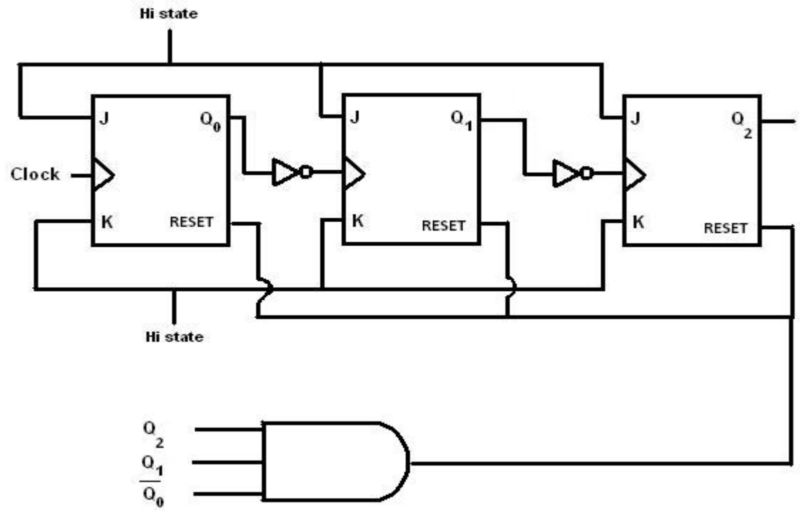


$K_B = \bar{Q}_A + Q_C$ $J_C = Q_AQ_B$ $K_C = \bar{Q}_A\bar{Q}_B$

13

The Reset button is an active high reset so it resets all flip flops to 0 when Reset = 1. The 6 stable states of the above counter are: Note that the Master-slave J-K flip-flops will change state on the negative edge of the clock pulse. So when a preceding Q changes state from 0 to 1 no toggle of the flip-flop results but when the preceding Q changes state from 1 to 0 the flip-flop toggles its output state.

Q_{2n}	Q_{1n}	Q_{0n}	Q_{2n+1}	Q_{1n+1}	Q_{0n+1}
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	1	0	1
1	0	1	0	0	0



14.

Ans b. We need a divide by 10 counter. So, 4 ffs are required. A possible state transition of the counter:

A	B	C	D
0	0	0	0
0	0	0	1
0	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1
1	0	0	0
1	0	0	1

Present state				Next state							
A	B	C	D	A	B	C	D	T_A	T_B	T_C	T_D
0	0	0	0	0	0	0	1	0	0	0	1
0	0	0	1	0	0	1	0	0	0	1	1
0	0	1	0	1	0	1	1	1	0	0	1
1	0	1	1	1	1	0	0	0	1	1	1
1	1	0	0	1	1	0	1	0	0	0	1
1	1	0	1	1	1	1	0	0	0	1	1
1	1	1	0	1	1	1	1	0	0	0	1
1	1	1	1	1	0	0	0	0	1	1	1
1	0	0	0	1	0	0	1	0	0	0	1
1	0	0	1	0	0	0	0	1	0	0	1

$T_D = 1$

FFA output will have the required waveform.

T_A

AB \ CD	00	01	11	10
00	0	0	X	1
01	X	X	X	X
11	0	0	0	0
10	0	1	0	X

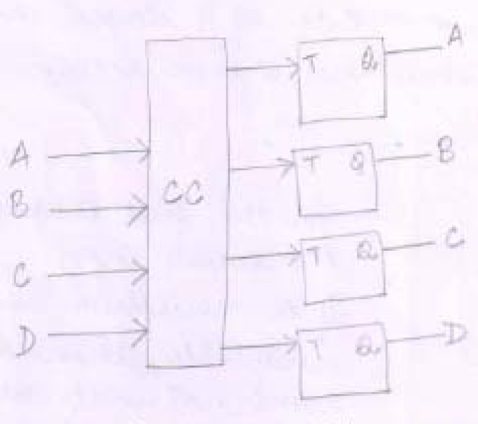
T_B

AB \ CD	00	01	11	10
00	0	0	X	0
01	X	X	X	X
11	0	0	1	0
10	0	0	1	X

T_C

AB \ CD	00	01	11	10
00	0	1	X	0
01	X	X	X	X
11	0	1	1	0
10	0	0	1	X

$T_A = \bar{A}C + A\bar{B}\bar{C}D$ $\quad$ $T_B = CD$ $\quad$ $T_C = CD + BD + \bar{A}D$



The combinational circuit can be synthesized using the derived expressions.