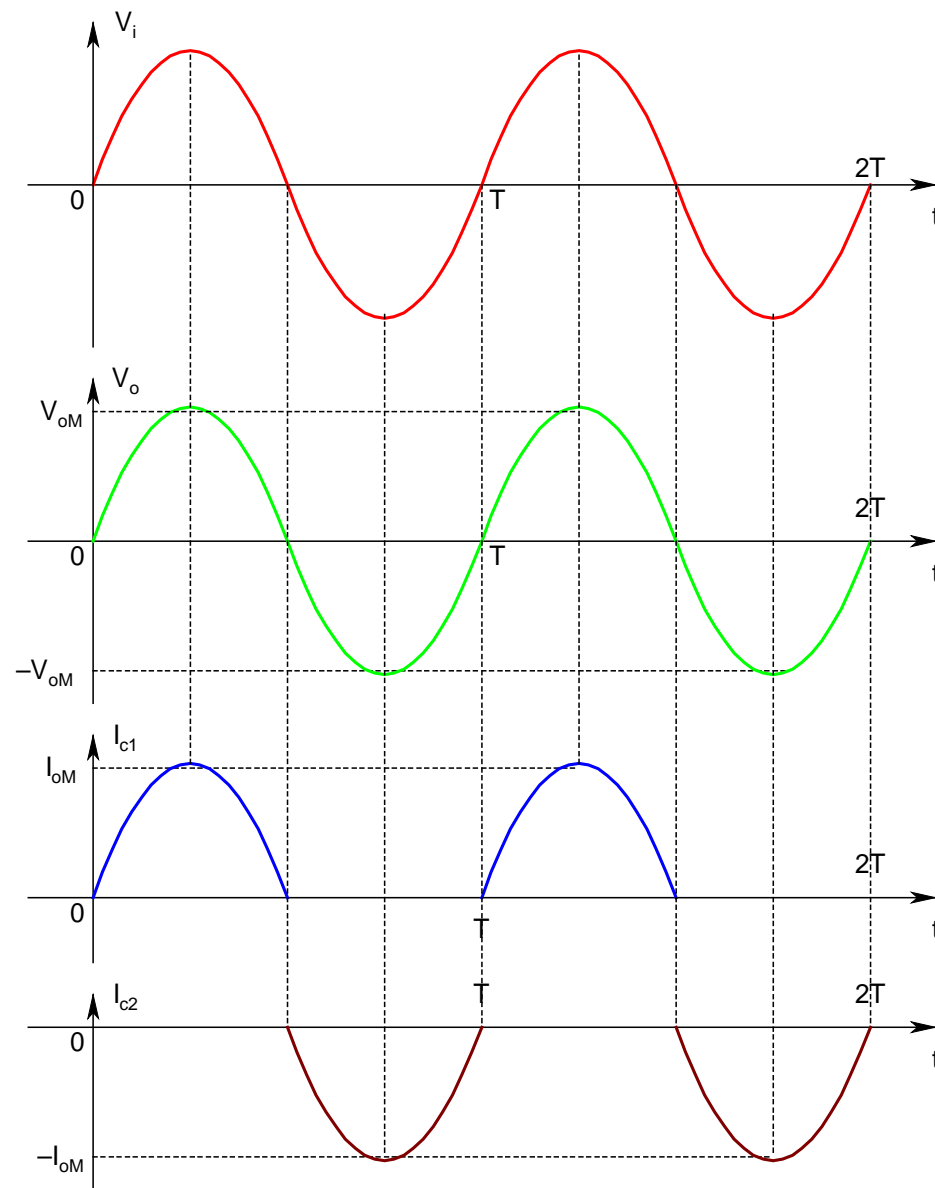


➤ *Power Output and Efficiency:*

- Refer to the figure in the next slide
 - ❖ *The constant offset of $|V_{EB2}|$ is neglected*
- *Both transistors are not ON over the entire cycle*
 - ❖ *Q_1 takes care of the positive half cycle*
 - ❖ *Q_2 takes care of the negative half cycle*
- V_{oM} : *Maximum value of V_o*
 - ❖ *Maximum possible swing between $[V_{CC} - V_{CE1}(HS)]$ and $[V_{EE} + V_{EC2}(HS)]$*
- I_{oM} : *Maximum value of load current* ($= V_{oM}/R_L$)
- *Average rms power P_L delivered to load:*

$$P_L = \frac{V_{oM}}{\sqrt{2}} \times \frac{I_{oM}}{\sqrt{2}} = \frac{V_{oM}^2}{2R_L}$$



- Now, we need to calculate the *power supplied to the stage by the power supplies*
- The *average current I_{supply} drawn by Q_1 from V_{CC} (happens only during the positive half cycle)*:

$$I_{supply} = \frac{1}{T} \int_0^T I_{c1}(t) dt = \frac{1}{2\pi} \int_0^\pi I_{oM} \sin \theta d\theta = \frac{I_{oM}}{\pi} = \frac{V_{oM}}{\pi R_L}$$

- *The same current will also be pushed by Q_2 to V_{EE} ($= -V_{CC}$) during the negative half cycle*
- *Thus, over a complete cycle, the average supply power P_{supply} drawn from the power supplies:*

$$P_{supply} = 2V_{CC} I_{supply} = 2V_{CC} V_{oM} / (\pi R_L)$$

- Thus, the *power conversion efficiency* (η):

$$\eta = \frac{P_L}{P_{\text{supply}}} = \frac{V_{oM}^2 / (2R_L)}{2V_{CC} V_{oM} / (\pi R_L)} = \frac{\pi V_{oM}}{4V_{CC}}$$

- η directly proportional to V_{oM} , and independent of R_L

\Rightarrow *Significant advantage*

- Also, $V_{oM}(\text{max}) \approx V_{CC}$

$\Rightarrow \eta_{\text{max}} = \pi/4 = 0.785$ (or 78.5%)

- *This value may not be attainable in practice*

❖ For $V_{oM} = -V_{CC}$, V_i has to be less than $-V_{CC}$, which *may not be practically achievable*

❖ This analysis *neglects the standby power* (quite small *though*) \Rightarrow *Inclusion of this term will reduce η_{max}*