ESc201A Home Assignment 5 Sept. 06, 2019.

Solutions of the HA#5 will be on Brihaspati on 013/09/19.

Consider all voltage and current sources to be ideal. Consider all diodes to have V_{on}=0.6V, $V_{D_{conducting}}$=0.7V, and r_F=0. All transistors in forward active mode have V_{BE}=0.7V.

1. Consider the circuit of fig. 5.1(a), where the zener diode has V_Z=5V and r_Z=0Ω. Sketch the waveform of v_o for the input voltage given in fig. 5.1(b).

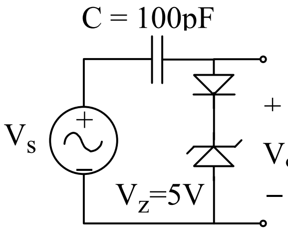


Figure 5.1(a).

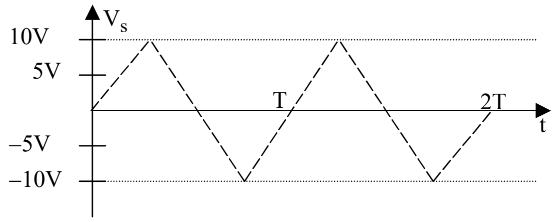


Figure 5.1(b).

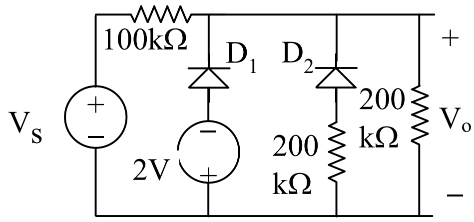


Figure 5.2.

2. Draw the voltage transfer characteristics for the circuit in fig. 5.2.
3. Draw the waveform for V_O in fig. 5.3 for V_S given in fig. 5.1(b).

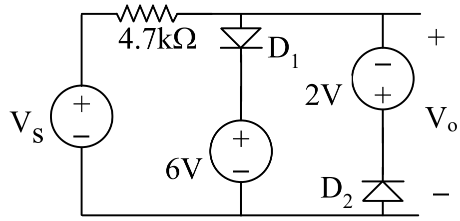


Figure 5.3.

4. For the circuit shown in fig. 5.4, find the output voltage v_o in each of the combination of inputs given. (a) v_1=10V, v_2=0V. (b) v_1=5V, v_2=0V. (c) v_1=10V, v_2=5V. and (d) v_1=5V, v_2=5V.

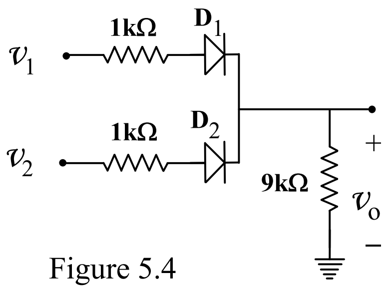


Figure 5.4

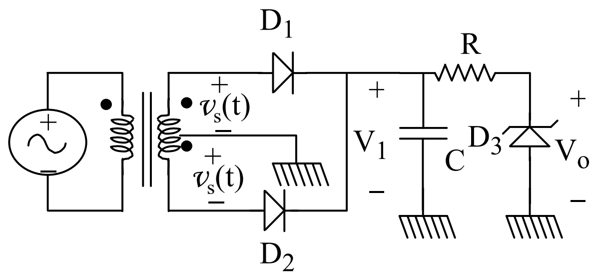


Figure 5.5

5. For the Zener regulated power supply in fig. 5.5 the rms value of v_s = 15V, the operating frequency is 50Hz, R=100Ω, C=1000μF. The Zener voltage of the diode D_3 is 15V with r_z= 0Ω. (a) What type of rectifier is this power-supply circuit ? (b) What is the DC voltage at V_1 ? (c) What is the DC output voltage V_o ? (d) What is the magnitude of the ripple voltage at V_1 ? (e) What is the PIV rating of the rectifier diodes ?

6. What are the DC output voltages V_1 and V_2 for the rectifier circuit shown in fig. 5.6 if v_s=50Sin377t and C=10,000μF?

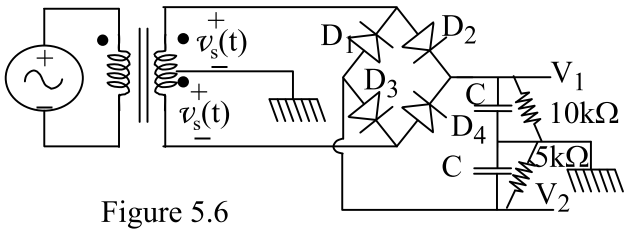
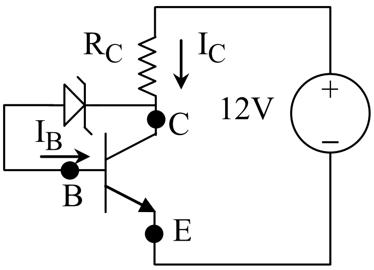
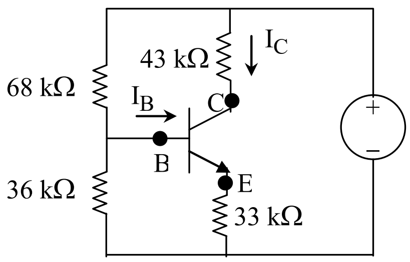


Figure 5.6

7. (a) Find the Q-point for the circuit in fig. 5.8. Assume $\beta_F = 50$ and $V_{BE}=0.7V$. (b) Repeat the calculation if all the resistors are decreased by a factor of 5.





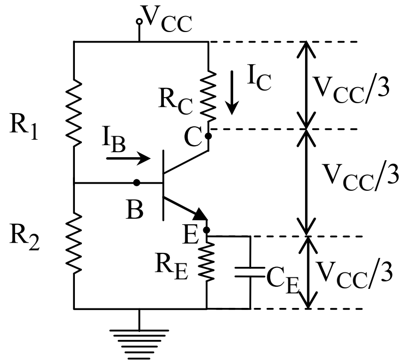


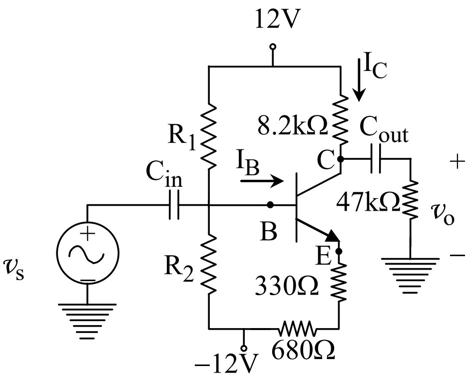
Figure 5.7 Figure 5.8 Figure 5.9

8. Find the Q-point for the circuit in fig. 5.7, considering the Zener diode to have $V_Z=5.0V$ and $r_Z=0\ \Omega$. Use $R_C=500\ \Omega$ and $\beta_F = 100$.

9. (a) From an expansion of the expression for a diode current, show that for an AC voltage v_d applied to a diode forward biased at V_D, the AC current is given by a linear expression $i_d=(I_D + I_S)(v_d/V_T)$ when the condition $(v_d/V_T) >> (1/2)(v_d/V_T)^2$ is used. Hence show that if we assume that this inequality is ten times, then $i_d=0.2I_D$ for V_T = 25mV. This is assumed to be the small signal criterion. **(Note the convention used: I_D is DC and similar is I_S. i_d is AC and i_D is DC and AC mixed.)**

(b) Similar to (a) if one assumes that for small signal $i_c=0.2I_C$ then for the transistor biased as shown in fig.5.9, find the maximum amplitude of the small signal at the collector 'v_c' in terms of V_{CC}. (note the new conventions introduced for the power supply and the ground).

10. (a) Estimate the voltage gain for the inverting amplifier shown in fig. 5.10 assuming C_{in}, C_{out} are very large.β=100, (b) Where should the bypass capacitor be placed such that the gain is approximately −10. (c) Where should the bypass capacitor be placed such that the gain is maximum. Find this gain.



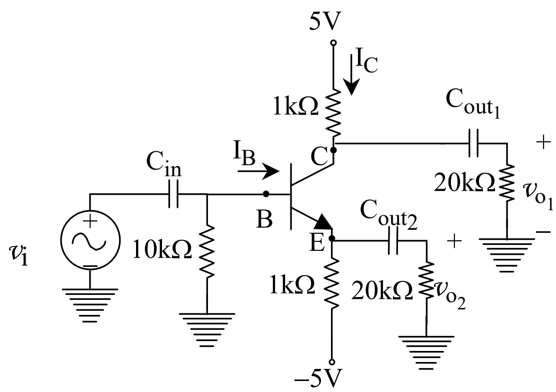


Figure 5.10 Figure 5.11

11. The circuit in fig. 5.11 is biased to operate in the active region.
(a) Find the collector bias current for $\beta_F = 100$.
(b) Assuming C_{in}, C_{out_1}, and C_{out_2} are very large, calculate the voltage gain $A_{v_1} = v_{o1}/v_i$.
(c) What is the largest AC signal that can be developed at the output v_{o1}?

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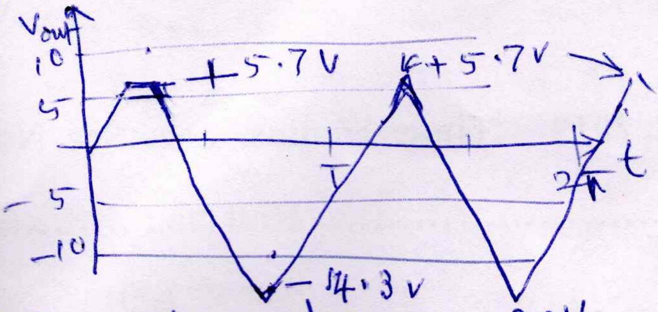
1/ 

As the voltage V_s goes up from $t=0$ V_o also goes up till 5.7V. At this time the diode & Zener conducts and clamps the voltage at 5.7V. When V_s starts coming down at time $t = T/4$ and drops below 5.7V, the capacitor still holds this voltage.

When V_s makes a $-20V$ downward sweep, Vout also makes a downward sweep of $-20V$ from the existing 5.7V. Therefore it ends at $-20 + 5.7 = -14.3$ V, and so on.

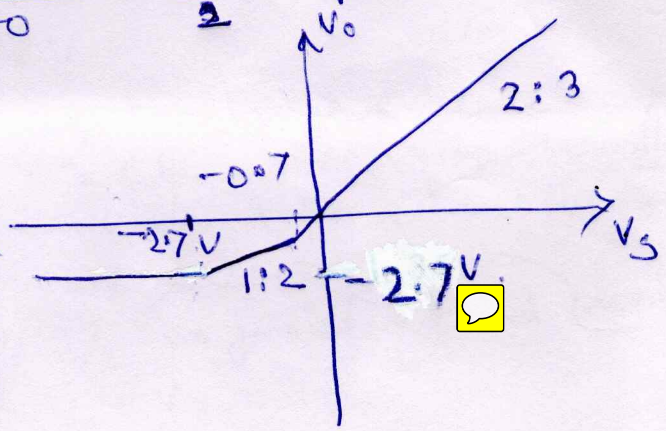
2/ For the +ve voltage of V_s, D_1 & D_2 will not conduct. Hence $V_{out} = \frac{V_s \times 200k\Omega}{100k\Omega + 200k\Omega}$ works as a potential divider

or $V_o = \frac{2}{3} V_s$.

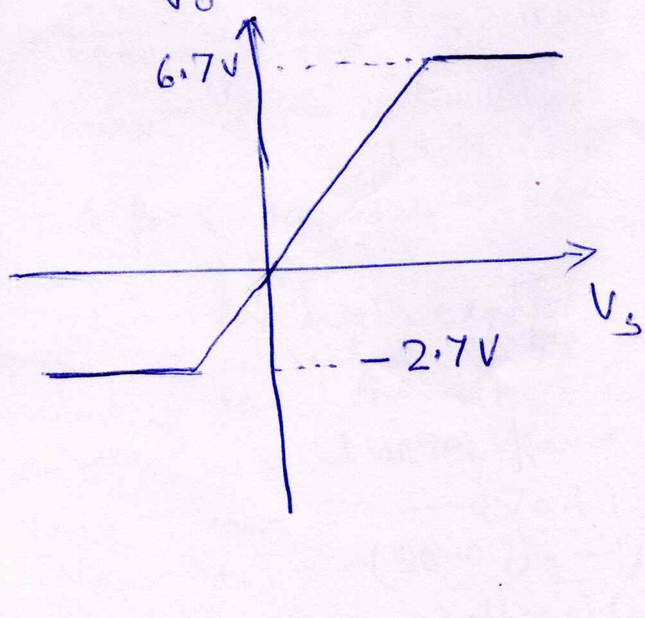
In the -ve voltage of V_s till 0.7V(V_{on}), the 2:3 slope continues in the 3rd quadrant. Beyond $-0.7V$, D_2 conducts and hence

$V_o = \frac{V_s \times 200k \| 200k}{100k + 200k\|200k} = \frac{100 V_s}{200} = \frac{V_s}{2}$ slope till V_s reaches -2.7 V.

For $V_s < -2.7$ V the output V_o gets clamped at this -2.7V as D_1 conducts and there is no resistance in its path. It shorts the two 200kΩ resistances.



3/ There are no resistances in the paths of D_1 & D_2 hence will be no potential divider anywhere.



In the positive cycle D_1 conducts when $V_o = 6.7$ V, whereas in the negative cycle D_2 conducts when $V_o = -2.7$ V.

when $V_o = 6.7$ V, $\frac{V_s - 6.7}{4.7k\Omega} = I_s$

or $V_s = 4.7k \times I_s + 6.7$ V.

Similarly $V_s(-ve) = -2.7 - 4.7k \times I_s(-ve)$

Before clamping only 4.7kΩ linear resistance makes the curve pass through the origin

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4/ (a) Assume D_1 is on and D_2 will be off due to V_o created.

$\therefore I_{D_1} = \frac{10-0.7}{10k\Omega} = 0.97\,mA$, $V_o = 0.97m \times 9k = 8.73\,V$

$10 - 8.76 > 0.7$ $\therefore D_1$ is definitely on & D_2 definitely off.

(b) Again assume D_1 is on & D_2 is off.

$\therefore I_{D_1} = \frac{5-0.7}{10k} = \frac{4.3}{10k} = 0.43\,mA$, $V_o = 0.43m \times 9k = 3.87\,V$

Justifies D_1 on and D_2 off states,

(c) Again assume D_1 is on and D_2 is off, but the latter will depend on V_o due to D_1 on.

If I_{D_1} again is $0.97\,mA$ & $V_o = 8.73\,V$, then obviously D_2 cannot turn on as $(8.73-5) > 0.7\,V$.

(d) Here $V_1 = V_2$ $\therefore$ One has to assume both D_1 & D_2 are on

$\therefore I_{D_1}\times 1k + (I_{D_1} + I_{D_2}) \times 9k \leq 5 - 0.7 = 4.3\,V$.

or $2I_D \times 9k \leq 4.3\,V - 1k \times I_D$ as $I_{D_1} = I_{D_2} = I_D$.

$\therefore I_D = 0.2263\,mA > 0$ $\therefore$ Both D_1 & D_2 conducts.

and $V_o = 2I_D \times 9k = 4.07\,V$

5/ The value of the capacitor is quite large & hence the ripple expected is small. $\tau = CR = 1000\mu \times 100 = 100\,ms$ (large)

$\therefore$ (a) is a full wave rectifier with center tapped transformer.

(b) $V_{DC} \simeq (V_{max} - V_{on}) = 15\sqrt{2} - 0.7 = 20.5\,V$ is valid

for 50Hz $T/2 = 10\,ms$ $\therefore \tau \gg T/2$ is justified and

(c) $r_z = 0$ and $V_z < 20.5\,V$ $\therefore V_o = V_z = 15\,V$.

(d) $V_r = \frac{V_{max} - V_{on}}{R} \cdot \frac{T}{2C} = \frac{20.5}{100} \times \frac{10m}{1000\mu} = \frac{20.5 \times 10}{100} = 2.05\,V$.

Now V_{DC} can be corrected to $V_{max} - \frac{V_r}{2} = 20.5 - 1.025 \cong 19.5\,V$.

(e) $PIV = 2V_{max} = 2 \times 15\sqrt{2}$
$= 42.43\,V$. (Note that for Bridge it would have been only 21.2 V.

6/ This is a full wave bridge rectifier (with center tapped transformer) with the same value of the capacitor but different value of load resistance i.e. $5k\Omega$ & $10k\Omega$ $\therefore \tau_1$ & τ_2 would be different.

It's easy to say that $V_1 = V_{max} - V_{on} = 50 - 0.7 = 49.3\,V$

& $V_2 = -(V_{max} - V_{on}) = -(50 - 0.7) = -49.3\,V$

Its two Fullwave rectifiers

$\omega = 377\,rad/s$ or $T/2 = 8.33\,ms$.

$\tau_1 = 10^{-2} \times 10^4 = 100\,s \rightarrow$ half ripple of V_2 $\therefore$ residual current flowing between V_1 & V_2

$\tau_2 = 10^{-2} \times 5 \times 10^3 = 50\,s$.

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Original version has wrong fig. It should be Fig 5.8

(a) $V_{BQ} = \frac{10}{68+36}\times 36 = \frac{360}{104} = 3.4615V$, $R_{BB} = 68k||36k = 23.54k\Omega$

$V_{BE} = 0.7V \therefore V_E = 2.7615$, $I_E = (\beta+1)I_B\Big|_{\beta=50} = \frac{V_E}{R_E} = \frac{2.7615}{33k} = 83.7\mu A$

$I_B = \frac{83.7}{51} = 1.64\mu A$, $I_C = \beta I_B = 50\times1.64 = 82\mu A$, $V_{CE} = 3.7V$

(b) $R_1 = \frac{68}{5} = 13.6k\Omega$, $R_2 = \frac{36}{5} = 7.2k\Omega$, $R_C = \frac{43}{5} = 8.6k\Omega$, $R_E = 6.6k\Omega$

Again $V_{BQ} = \frac{10\times7.2}{7.2+13.6} = 3.4615V$, $V_{BE} = 0.7$, $V_E = 2.7615V$, $I_E = \frac{V_E}{R_E} = 418.4\mu A$

$I_B = \frac{418.4\mu}{51} = 8.2\mu A$, $I_C = 50\times8.2\mu = 410.2\mu A$, $V_{CE} = 10-2.762-3.53 = 3.71V$.

$R_{BB} = 13.6||7.2 = 4.71K$. (What has changed?)

) $12V = R_C(I_B+I_C)+V_Z+V_{BE} = 500(I_C+\frac{I_C}{100})+5+0.7$

or $500(1.01)I_C = 12-5.7 = 6.3$ or $I_{CQ} = 12.48mA$, $I_B = 0.124mA = 124\mu A$

$I_E = \frac{\beta+1}{\beta}I_C = \frac{101}{100}\times12.48 = 12.6mA$, $V_{CEQ} = 12-R_C(I_B+I_C) = 5.7V$

7/a) D.C. diode voltage is V_D and a.c. bias is v_d then the diode current is $i_D = I_D + i_d = I_S\{e^{(V_D+v_d)/V_T}-1\}$ & Expanding the exponential

$= I_S\{[1+\frac{v_d}{V_T}+\underbrace{\frac{1}{2}(\frac{v_d}{V_T})^2+\frac{1}{6}(\frac{v_d}{V_T})^3\ldots\ldots}_{\text{neglect}}]e^{V_D/V_T}-1\}$

$\simeq I_S\{[1+\frac{v_d}{V_T}]e^{V_D/V_T}-1\} = I_S[e^{V_D/V_T}-1]+I_S\frac{v_d}{V_T}e^{V_D/V_T}$

$= I_D + i_d$ where $i_d = I_S\frac{v_d}{V_T}e^{V_D/V_T} \simeq \frac{v_d}{V_T}I_D$

So for $\frac{v_d}{V_T}/10 = \frac{1}{2}(\frac{v_d}{V_T})^2$, $\frac{v_d}{V_T} = 1/5 = 0.2$ or $i_d = 0.2I_D$

b) $V_{R_C} = \frac{V_{CC}}{3}$ so $I_C = (V_{CC}/3)/R_C$, if $i_b = 0.2I_B$ then

assuming $\beta_{DC} = \beta_{a.c}$, $\beta_{a.c.}i_b = i_c = 0.2\beta_{DC}I_B = 0.2I_C$

$\therefore v_c = i_cR_c$ (Remember discussed in class that V_{CC} is a.c. ground due to large capacitance of the supply)

$= 0.2I_CR_C = 0.2(V_{CC}/3) = V_{CC}/15$

8) a) Assume $V_A = \infty$, For biasing assume $V_C = 0 \therefore 12-8.2kI_C = 0$, $I_C = 1.46mA$.

For large $\beta \simeq 100$, $I_E \simeq I_C = 1.46mA \therefore V_E = -12+(330+680)I_E = -10.5V$

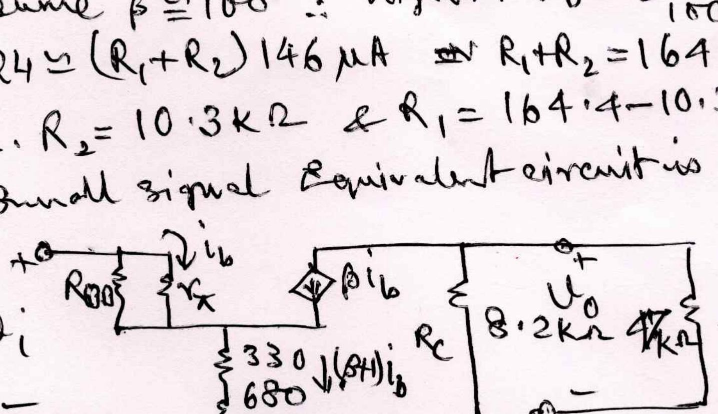
$V_{CEQ} = 10.5V$, $V_B = V_E+0.7V = -9.8V$, or $\frac{24\times R_2}{(R_1+R_2)}-12 = V_B = -10.5$

Assume $\beta \gtrsim 100 \therefore$ highest $I_B = \frac{1.46m}{100} = 14.6\mu A$, $I_{R_1} = 10I_B = 146\mu A$.

$\therefore 24 \simeq (R_1+R_2)146\mu A$ or $R_1+R_2 = 164.4k\Omega$ or $\frac{24R_2}{164.4k} = 1.5$

$\therefore R_2 = 10.3k\Omega$ & $R_1 = 164.4-10.3 = 154.1k\Omega \longrightarrow R_{BB} = R_1||R_2 = 9.65k\Omega$

$\therefore$ Small signal Equivalent circuit is: $r_\pi = \beta\frac{V_T}{I_C} = 100\times\frac{0.026}{1.46m} = 1.78k\Omega$



$\therefore r_\pi << R_{BB} \therefore i_i \cong i_b$

$v_0 = -\beta i_b(8.2k||47k)$

$v_i \cong i_b r_\pi + (\beta+1)i_b(330+680)$

$\therefore \frac{v_0}{v_i} = A_v = -\frac{\beta\times7.13k}{1.78k+(\beta+1)1.01k}\Big|_{\beta=100} = -6.87$

10/ Contd.

(b) $\left.\frac{v_o}{v_i}\right|_{\text{with bypass Cap across } 680\Omega} = A_v = -\frac{\beta \times 7.13k}{1.78k + (\beta+1)0.33k} = -20.3$

$\left.\frac{v_o}{v_i}\right|_{\text{with bypass cap. across } 330\Omega} = A_v = -\frac{\beta \times 7.13k}{1.78k + (\beta+1)\times 0.68k} = -10.12$

$\therefore$ for $A_v \simeq -10$, capacitor should be placed across 330Ω

(c) $\left.\frac{v_o}{v_i}\right|_{R_E=0} = -\frac{\beta \times 7.13k}{1.78k + (\beta+1)\times 0} = -\frac{100\times 7.13k}{1.78k} = -400.56 = A_v$ Max gain

with bypass capacitor across $(680+330)\Omega$

11/ Again as a rule of thumb one can take $V_{cc}/3$ across R_C, V_{CE}, and R_E, but if one would like V_C at 0V, then $R_C I_C = 5V$. As the output is taken from v_o, through a.c. coupling $\therefore$ no need to have V_C at 0V.

(a) $\therefore 1k\Omega \times I_C = \frac{5-(-5)}{3} = V_{CE} = I_E \times 1k\Omega$

To reduce the calculation load, as β is large ~ 100, assume $I_E \simeq I_C$ $\therefore \frac{10}{3}V = 1k\Omega \times I_C$ or $I_C = 3.33mA$.

$V_{CE} = 3.33V$, $V_E = -5 + 3.33V = -1.67V$.

$V_B = -0.97V$ (Note the base current path is from ground through the BE junction to $-5V$)

(b) For new I_C using result from Q10

$r_\pi = \frac{\beta V_T}{I_C} = \frac{100\times 0.026}{3.33m} = 780.8\Omega \ll 10k\Omega$

$\therefore i_b$ can be assumed to pass entirely through r_π without much error, and hence can use the result from Q10 above

or $v_o = -\beta i_b (1k\Omega \| 20k\Omega)$, $v_i = i_b r_\pi + i_b(\beta+1)(1k\Omega\|20k\Omega)$ at C_{out_2}

$\therefore A_{v_1} = \frac{v_o}{v_i} = -\frac{\beta(952.3)}{780.8 + (\beta+1)(952.3)}$ at C_{out_1} $= -0.982$ (Actually Attenuation)

(c) $5V - V_C = 5 - (3.33 - 1.67) = 3.34 \simeq 3.33V$ (As designed) $(2V_{cc}/3)$