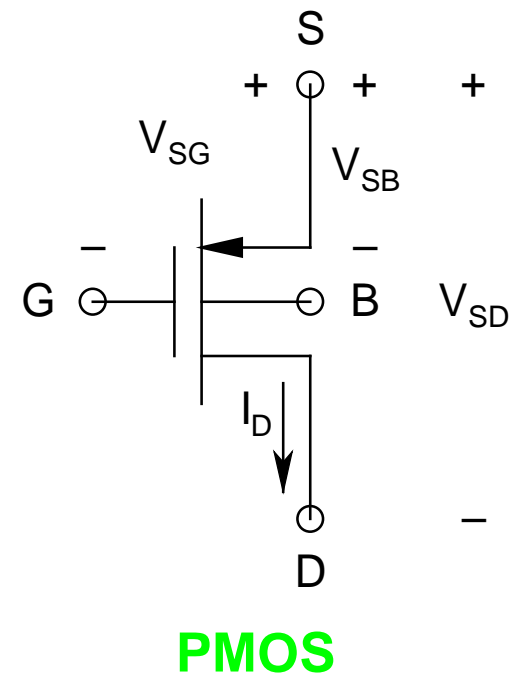


p-channel MOSFET (PMOS)

- Before moving to *NMOS stages with active load*, it will be prudent to visit some details regarding *PMOS*
- *Substrate: n-type* (N_D)
 - *Bulk Potential:*
$$\phi_F = V_T \ln(N_D/n_i)$$
- *Source/Drain: p⁺*
- *Channel Carriers: Holes*



- **Threshold Voltage:**

$$V_{TP} = V_{TP0} - \gamma \left(\sqrt{2\phi_F + V_{BS}} - \sqrt{2\phi_F} \right)$$

V_{TP0} : **Zero back-bias threshold voltage** (*negative*)

➤ **Body effect coefficient:**

$$\gamma = \frac{\sqrt{2q\epsilon_s N_D}}{C'_{ox}}$$

▪ $V_{BS} \geq 0$ (*to prevent forward biasing of SB junction*)

➤ **With back bias**, V_{TP} **becomes more negative**

➤ V_{GS} **has to be less than V_{TP} to turn device on**

- **Current-Voltage Relation:**

- **Both V_{GS} and V_{DS} negative**
- **I_D flows from source to drain (the *same direction of flow as holes*)**
- **In saturation** [$|V_{DS}| > (|V_{GS}| - |V_{TP}|)$]:

$$I_D = \frac{k'_P}{2} \frac{W}{L} \left(|V_{GSp}| - |V_{TP}| \right)^2 \left(1 + \lambda_p |V_{DSp}| \right)$$

- **In non-saturation** [$|V_{DS}| < (|V_{GS}| - |V_{TP}|)$]:

$$I_D = k'_P \frac{W}{L} \left[\left(|V_{GSp}| - |V_{TP}| \right) |V_{DSp}| - \frac{|V_{DSp}|^2}{2} \right]$$

$$k'_p = \mu_p C'_{ox}$$

= *Process transconductance parameter*

μ_p = *Channel hole mobility*

- *Based on the value of V_{TN0} and V_{TP0} , there are two classifications:*

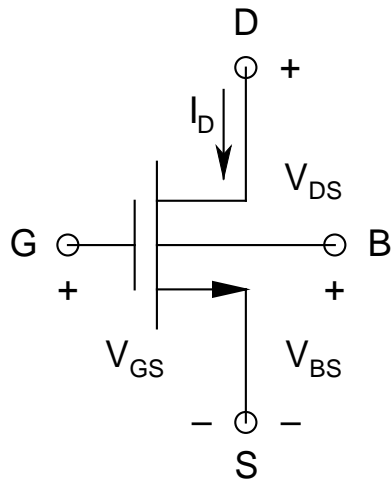
- *Enhancement Mode: Normally Off (with $V_{GS} = 0$)*

- *V_{TN0} positive and V_{TP0} negative*

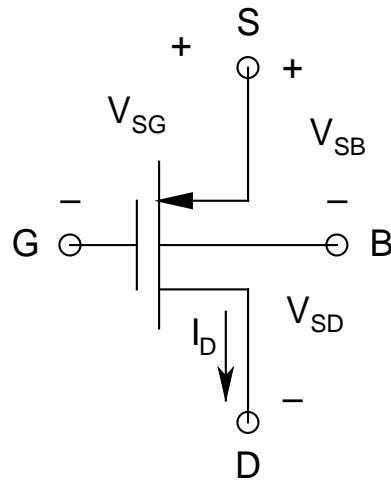
- *Depletion Mode: Normally On (with $V_{GS} = 0$)*

- *V_{TN0} negative and V_{TP0} positive*

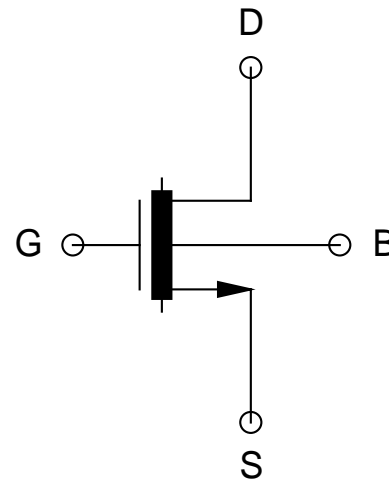
Symbols



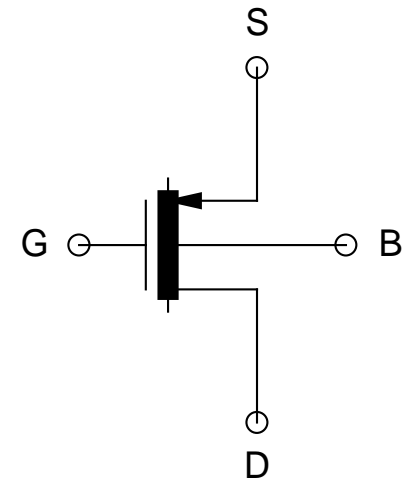
Enhancement
Mode NMOS



Enhancement
Mode PMOS



Depletion
Mode NMOS



Depletion
Mode PMOS

- Note the *thick band* in the *channel region* for *depletion mode devices*, which implies that *channel is present* even *with $V_{GS} = 0$*