**DOCUMENTATION**

**ON**

**DESIGN AND IMPLEMENTATION OF AUTOMATED TELLER MACHINE (FSM) CONTROLLER**

**- BY TECH PIRATES TEAM**

**Title:** ATM Machine Controller Documentation

**1. Introduction**

The ATM Machine module is a hardware design implemented in Verilog HDL (Hardware Description Language) that models the functionality of an Automated Teller Machine (ATM). The module represents the state machine of the ATM and provides various operations such as PIN entry, withdrawal, deposit, balance inquiry, mini statement, and more.

It defines an ATM CONTROLLER module. This module represents the controller for an ATM (Automated Teller Machine) system. It implements the behaviour of the ATM controller using a finite state machine (FSM).

This documentation provides an overview of the ATM Machine module's structure, its states, and the testbench used for verification.

**2. ATM Machine Module**

* **Input Signals**

The ATM Machine module accepts the following input signals:

clk (input): This signal represents the clock input for the module. The module operates on the positive edge of this clock signal.

rst (input): This signal stands for reset. It is an asynchronous input that resets the module to its initial state when asserted.

pin (input [4:0]): This signal is a 5-bit input representing the Personal Identification Number (PIN) entered by the user. The PIN is used for authentication purposes.

amount (input [7:0]): This signal is an 8-bit input that represents the amount of money to be withdrawn from the ATM.

face (input): This signal is not explicitly used in the code you provided. It seems to be unused in the module's functionality.

* **Output Signals**

The ATM Machine module provides the following output signal:

1.lock\_account: Output signal indicating whether the account is locked.

2.balance: 8-bit output representing the current account balance.

3.new\_balance: 16-bit output representing the new account balance after a transaction.

4.mini\_statement: Output signal representing the mini statement for recent transactions.

* **FSM States**

The module defines the following FSM (Finite State Machine) states:

**1. Initial State:**

* When rst is asserted (active high), the FSM enters the initial state. All the registers and outputs are initialized.
* Actions in the initial state:
  + - pin\_count is set to 0.
    - locked is set to 0.
    - old\_balance is set to the initial value of balance (1000).
    - new\_balance is set to the initial value of balance
    - mini\_statement is set to 0.

**2. PIN Check State:**

* When the system is not locked (locked is 0) and the PIN entered (pin) is not equal to 1234:
* If pin\_count is less than 3, the FSM remains in this state and increments pin\_count by 1.
* If pin\_count reaches 3, the FSM transitions to the Lock State.

**3. Withdrawal State:**

* When the system is not locked (locked is 0) and the PIN entered (pin) is equal to 1234:
  + - If pin\_count is less than 3, the FSM remains in this state and increments pin\_count by 1.
    - In this state, the new\_balance is updated by subtracting the amount from the current balance.
    - The mini\_statement is set to 1, indicating a successful withdrawal.
    - After this state, the FSM transitions back to the PIN Check State.

**4. Lock State:**

* When the system reaches the maximum PIN attempts (pin\_count equals 3) and the entered PIN (pin) is not equal to 1234, the FSM enters the Lock State.
* In this state, locked is set to 1, indicating that the system is locked.
* The new\_balance remains unchanged.
* The mini\_statement remains 0.
* Once locked, the FSM stays in this state until a reset (rst) is asserted.
* **Implementation Details**

The ATM Machine module uses a combinational process to determine the next state based on the current state and input signals. It updates the state register at each positive edge of the clock signal.

**3. Testbench (ATM Machine Controller\_TB)**

The ATM Controller\_TB module is used to test and verify the functionality of the ATM Controller module. It provides test scenarios for different operations and verifies the output state.

The testbench includes the following components:

**Clock Generation**: Generates a clock signal to drive the operations of the modules.

**Signals Initialization**: Initializes the input signals with specific values for each test scenario.

**Test Scenarios**: Simulates various test scenarios by modifying the input signals according to the desired operations and expected outcomes.

**Finish Simulation**: Terminates the simulation after a specified time.

**4. Conclusion**

The ATM Machine Controller module provides a hardware representation of an ATM and supports various operations such as PIN entry, withdrawal, deposit, balance inquiry, mini statement, and more. By utilizing the provided testbench, the module's functionality can be thoroughly tested and verified. This documentation serves as a guide to understand the structure and behaviour of the ATM Machine module and its associated testbench.

**Done By: MENTOR**

Team Name: TECH PIRATES Mr. R. Prapulla Kumar

N. Sathya Sai Keerthana Assistant Professor

M. Hema Latha Department of CSE

B. Lakshmi Thanuja