# LAKSHMI PUJITHA CHAGANTI

VLSI Engineer | Full Stack Developer
lakshmipujithachaganti05@gmail.com
https://github.com/Lakshmipujit
https://www.linkedin.com/in/pujithachaganti

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## PROFESSIONAL SUMMARY

ECE undergraduate focused on RTL design and digital system development with hands-on implementation of FIFO and UART modules. Strong foundation in Verilog-based design and digital logic. Additionally skilled in full stack development using React.js and Node.js.

## EDUCATION

B.Tech – Electronics and Communication Engineering (2023–2027) | Rajiv Gandhi University of Knowledge and Technologies | CGPA: 7.78

## TECHNICAL SKILLS

- Digital Design: Verilog, FSM Design, FIFO Architecture, UART Protocol
- Simulation & Tools: Vivado
- Programming: C++, Python, JavaScript
- Full Stack: React.js, Node.js, HTML5, CSS3, SQL
- Version Control: Git, GitHub

## VLSI / RTL PROJECTS

- Parameterized Synchronous FIFO – Configurable data width and depth with full/empty detection logic and simulation verification.
- UART Transmitter (FSM-Based Design) – Baud rate generator with IDLE/START/DATA/STOP states and waveform validation.

## FULL STACK PROJECTS

- Book Hub – React-based application with dynamic search and state management.
- COVID-19 Dashboard – REST API-integrated dashboard with data visualization.
- Movies App – Movie search application with reusable UI components.

## CERTIFICATIONS

NxtWave Course Completion Certificates: JavaScript, Python, Node.js, React.js, HTML/CSS, SQL
FPGA Workshop Certificate