MODULE 2

BJT Biasing

BJT Biasing: DC Load line and Bias Point, Base Bias, Voltage divider Bias, Numerical examples as applicable.

DC load line analysis and Bias point

There are several applications of BJT; one of the applications of BJT is as an amplifier. For amplifier operation the BJT must be used in active region which can be achieved by forward biasing the emitter-base junction and reverse biasing the base-collector junction.

DC load line

The dc load line for a transistor circuit is straight line drawn on the transistor output characteristics. The purpose of drawing the load line is to locate the 'Q' point graphically, where 'Q' point is the point of intersection of load line and the output characteristics of transistor.

For a common emitter (CE) circuit, the load line is a graph of collector current (I_C) versus collector-emitter voltage (V_{CE}) for a given values of collector resistance (R_C) and a given supply voltage (V_{CC}). The 'Q point for CE circuit denotes the voltage V_{CE} across the transistor and current I_C through the transistor.

To draw DC load line

- Consider the common-emitter circuit shown in figure 1a. Applying KVL to the output side of circuit i.e., at the collector terminal.

→ (1)

— — → (2)

- The equation (2) is of the form y=mx+c, equation of straight line with slope m=-1/Rc.
- Since the load line is a straight line, to sketch the line we need two points. The points are found as

  Put Ic = 0 in equation (1) Put V_{CE}=0 in equation (1)

  V_{CC} -0-V_{CE}=0 V_{CC}-I_CR_C=0

  V_{CE}=V_{CC} I_CR_C=V_{CC} → I_C=V_{CC}/R_C

  Point A= (V_{CE},0) and point B= (0, V_{CC}/R_C)

- The above two points are plotted on the output characteristics curve of CE configuration and straight line is drawn joining the two points as shown in figure 1b.

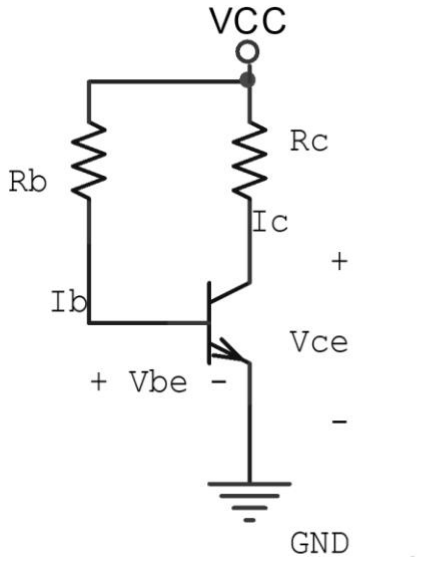

Fig. 1a: Common-Emitter circuit

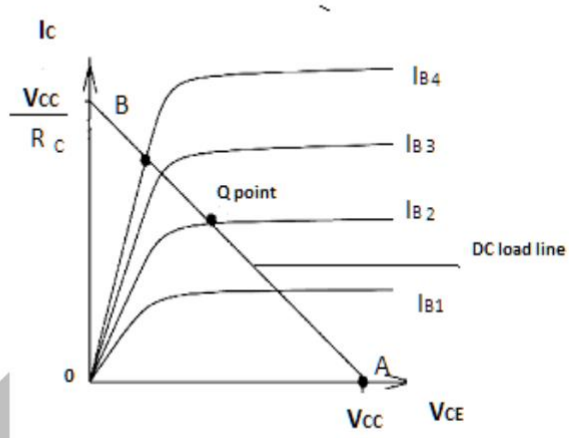

Fig. 1b: DC load line for CE circuit

Effect of R_E o DC load line

- Figure 2 shows the CE circuit where emitter resistor (R_E) is connected in series with the transistor and supply voltage (Vcc) is directly connected to the collector terminal.
- Applying KVL to the output side of the circuit

To plot DC load line

Put then ———. Point A= (0, ———)

Put then . Point B= (

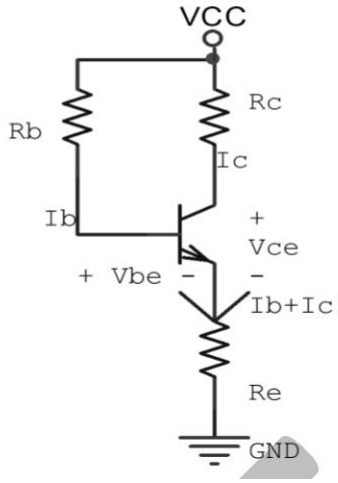

Fig. 2 Common emitter configuration with R_E resistance

BJT biasing

The biasing can be described as connecting external DC power supply and external resistors to work BJT in desired region. For example, for application of BJT as amplifier, the BJT must be used in active region. To obtain this region the base to emitter junction is forward biased and base to collector junction should be reverse biased.

Need for biasing

In order to operate transistor in the designed region .We have to apply external DC voltage of correct polarity and magnitude to the two junction of the transistor, this is called biasing. Biasing circuit is required because

- The circuit design should be provide a degree of temperature stability
- The operating point should be made independent of the transistor parameters(such as β)

The different methods of biasing are

- Base bias (Fixed bias)
- Collector to base bias
- Voltage divider bias

Base bias circuit or Fixed bias

The base bias circuit is shown in figure 3. It consists of two resistors, transistor and a supply V_{CC}. The supply voltage V_{CC} forward biases base to emitter junction and reverse biases collector to emitter junction.

In this circuit, the base current is a constant quantity determined by supply voltage Vcc and base resistor R_B. Hence, this is known as fixed current bias or fixed bias circuit.

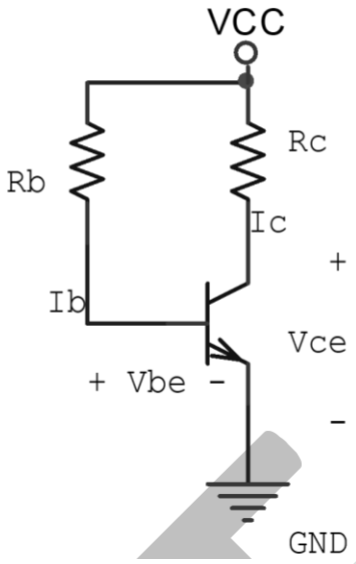

Fig. 3: Base bias circuit using npn transistor Analysis of base bias circuit

- Applying the Kirchhoff's Voltage Law (KVL) to the input side of the circuit, i.e., base terminal side, we get

→(1)

- Then the input current is given by

- The collector current is given by the

→(2)

- Apply the Kirchhoff's Voltage Law (KVL) at the output side of the circuit, i.e., at the collector terminal, we get

→(3)

It is important to note that, the base current is controlled by the value of and is related to by a constant (, the magnitude of is not a function of R_C. Thus changing R_C will not affect on I_B and in turn I_C.

Problems on Base biasing or Fixed biasing

1). For the circuit shown in figure 4a. find the Q-point values and draw DC-Load line where V_{BE}=0.7V and =50

The base bias circuit is shown in figure below. Apply KVL to the input side of the circuit

The collector current is given by the

$$\beta * \quad = 2.35mA$$

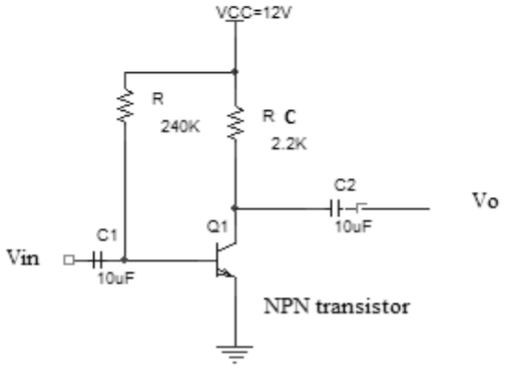

Fig.4a: Base bias circuit

Apply the KVL at the output side of the circuit

Substitute in above equation.

Point A = ( )

Substitute in above equation.

— Point B = (—)

The dc load line is shown in figure 4b.

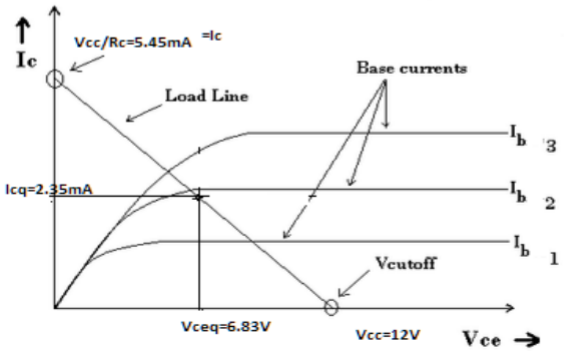

Fig. 4b: DC load line analysis for given circuit

2).The circuit of figure 5a shows a silicon transistor with =100 which is biased by the base bias method. Find the Q-point values and draw DC-Load line.

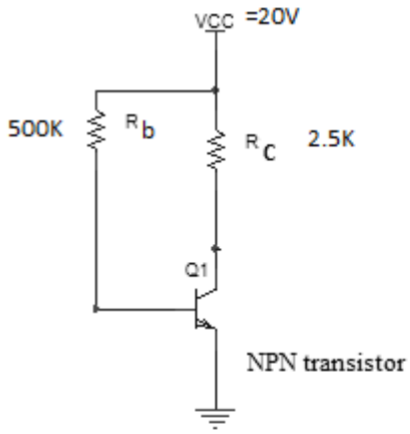

Fig. 5a: Base bias circuit

The base bias circuit is shown in figure below. Apply KVL to the input side of the circuit

The collector current is given by the

$\beta *$ =100* 38.6 A= 3.86 mA

Apply the KVL at the output side of the circuit

The Q-point is = (10.35V, 3.86mA)

Substitute in above equation.

Point A = ( )=(20,0)

Substitute in above equation.

— Point B = (—)=(0,8mA)

The dc load line is shown in figure 5b.

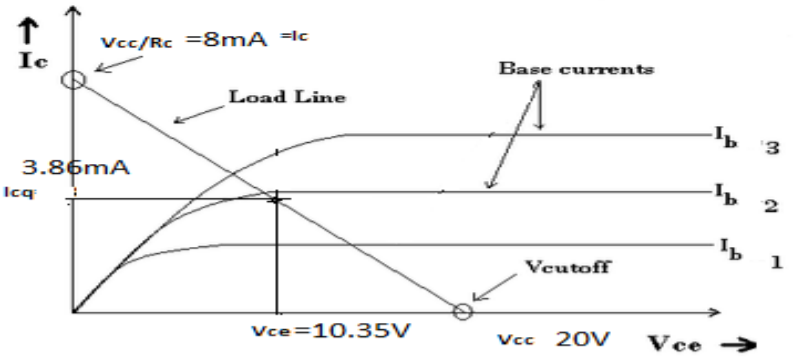

Fig. 5b: DC load line analysis for given circuit

Base Bias circuit Design

1). Designing is finding the resistance values when V_{CC}, V_{CE}, V_{BE} and and I_C is given. The necessary design equations are given explained below.

h_{FE} where h_{FE}=

— -------(1)

Then the base resistance is given by

——— ----------(2)

The collector resistance is given by

——— ----------(3)

The designed circuit is shown in figure 6.

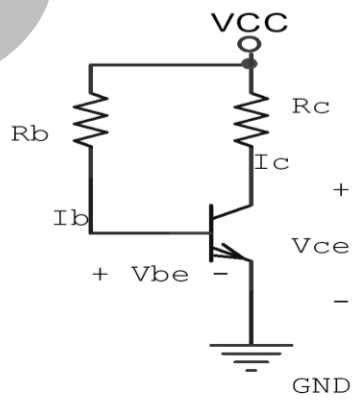

Fig. 6: Base bias circuit design

Problem on Base bias design

1. **A base bias circuit with a 12 V supply uses a transistor with h_{FE}=70. Design the circuit so that I_C=2mA and V_{CE}=9V (Assume R_E=0).**

Given data:

Base bias circuit with a 12 V

Transistor with h_{FE} =70. I_C=2mA and V_{CE}=9V (Assume R_E=0).

The current gain of the CE amplifier is given by

h_{FE} where h_{FE}=

= = 0.285mA

The KVL to the input side of the circuit

Then the base resistance is given by

=———— = 133KΩ

Apply the KVL at the output side of the circuit

The collector resistance is given by

= = 4.5KΩ

The designed values are shown in figure 7 below for the base bias circui.

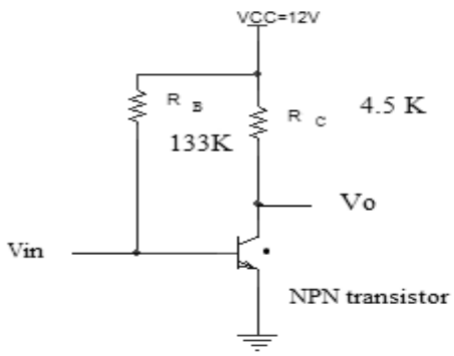

Fig. 7: Base bias circuit

Advantages and disadvantages of base bias circuit

Advantages

- This is simple circuit which uses very few components.
- Operating point can be set anywhere in the active region of the characteristics curve by simply changing the value of R_B. Thus, it provides maximum flexibility in the design.

Disadvantages

- The collector current does not remain constant with variation in temperature or power supply voltage. Hence, operating point is unstable, i.e. thermal stability is not provided by this circuit.
- Changes in V_{BE} will change I_B and thus cause I_C to change. This in turn will alter the operating point.
- When the transistor replaced with another one, considerably change in the value of β is expected which in turns changes I_C thus changes the operating point.
- The stabilization of operating point is very poor in the base bias circuit.

Voltage Divider Bias

Precise Analysis:

The voltage divider bias circuit is shown in the figure 8. It is simplified using the Thevenin's theorem and the simplified Thevenin's equivalent circuit is shown in figure 8.

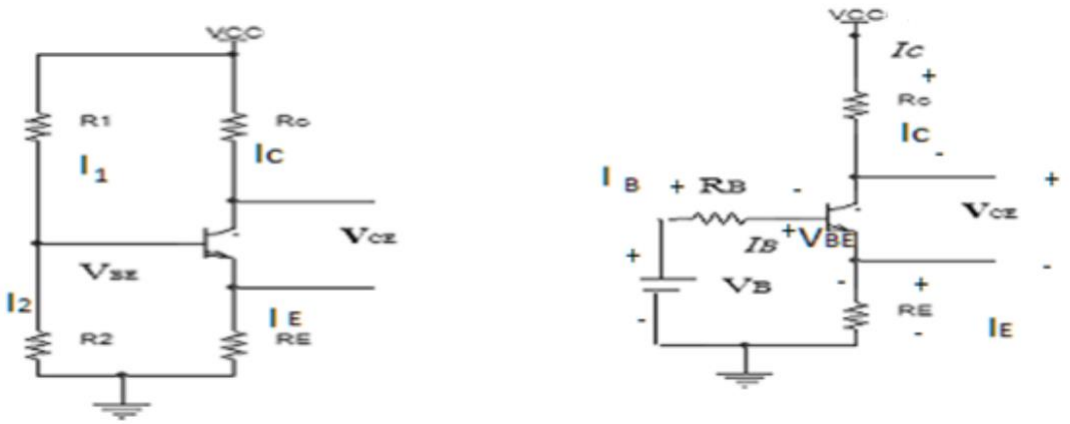

Fig.8 Voltage divider bias circuit and Thevenin's equivalent circuit of VDB

The voltage divider bias circuit is shown in the figure 8.Two resistors are connected to be the base terminals of the transistors. Since the base current is very small it can be neglected, then the current through will be same. Therefore, the two resistors are said to be in series, the voltage across the resistor R_2 can be found by applying the voltage dividing rule.

The voltage across the resistor R_2 forward biases the base to emitter junction. The collector to base junction is reverse biased by the supply voltage V_{CC}. Thus BJT is made to operate in the active region. Hence the transistor is said to be biased. Since there are two resistors connected to the base terminal the circuit can be simplified by applying Thevenin's theorem. The resulting equivalent circuit is shown in figure 8.

The resulting Thevenin's resistance is given by

Apply the KVL (Kirchhoff's Voltage Law) at the input side of the circuit

=0

We know that

The collector current is given by

Apply the KVL at the output side of the circuit

Advantages of voltage divider bias

1. A stable operating point in the active region of operation is obtained using this method.
2. The operating point is independent of the variation.
3. Operating point is stabilized against shift in temperature.
4. Only one dc supply is necessary.

Approximate Analysis of Voltage Divider Bias

Approximate analysis of Voltage divider bias circuit is explained with the help of the VDB circuit as shown below.

Voltage Divider Bias circuit using approximate analysis is as shown in figure8.
voltage across the resistor R_2 can be found by applying the voltage dividing rule.

The resulting Thevenin's resistance is given by

Since value chosen is zero, the is also zero.
Then apply KVL at the input side of the circuit
Then

Then the current

Apply KVL at output side of the circuit

and

Problems on VDB

1. **Determine the emitter voltage, collector voltage and collector emitter voltage of the voltage divider bias circuit shown below in figure 9.**

Given data:

Vcc=18v, R_1=33kΩ, R_2=12kΩ, R_C=1.2kΩ, R_E=1kΩ

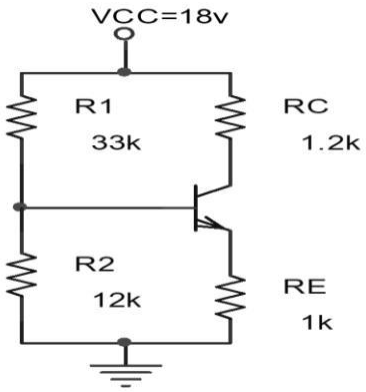

Fig. 9 Voltage divider bias circuit

2. **A voltage divider bias has Vcc=10V, R_1=82kΩ, R_2=18kΩ, R_C=2.2kΩ, R_E=0.5kΩ. Find the Q-point and terminal voltages. Draw the load line and locate the operating point at β=100.**

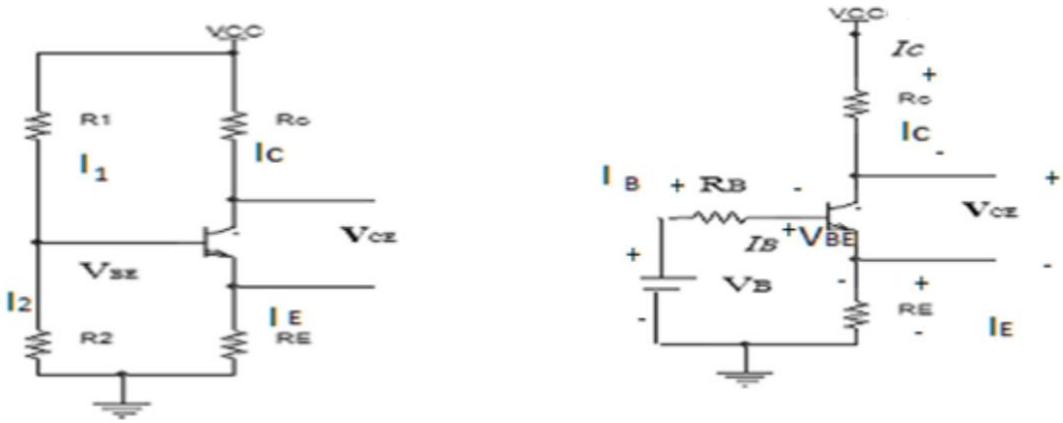

Fig. 10 Voltage divider bias circuit and Thevenin's equivalent circuit of VDB

V

Applying KVL to input circuit

Applying KVL to output circuit

The Q-point is (

To draw DC load line

Put ,

Put

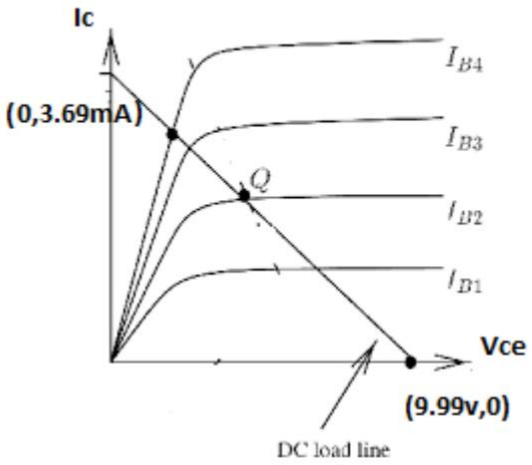

Fig. 11: DC load line analysis

Voltage divider bias circuit Design

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After designing the necessary values draw the circuit and mention the values.

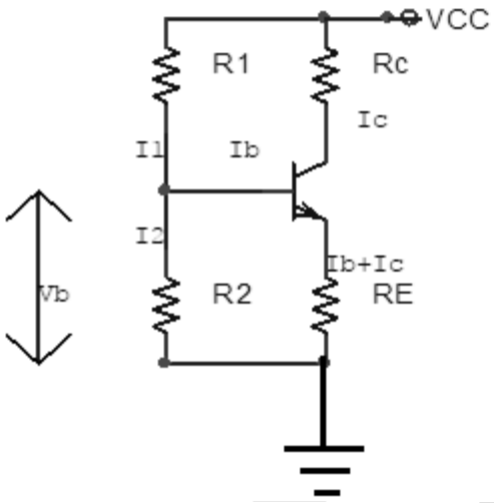

Fig. 12: Design of Voltage divider bias

1). Design a voltage divider bias circuit for the following specifications. V_{CC}=18v, V_{CE}=3v,V_E=5V,I_C=I_E=1mA.

Given Data:
V_{CC}=12 V supply.
The bias conditions are
V_{CE}=3V, V_E=5V, and Ic = 1mA.
Find: R_C, R_E and R_1 and R_2

\The collector resistance is given by

Assume = = 1mA

The designed values re shown in figure 13.

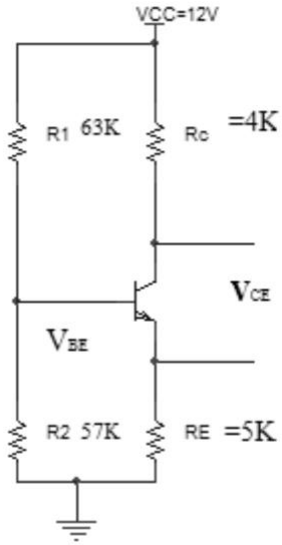

Fig.13. Voltage divider bias circuit Design

2). Design a voltage divider bias circuit to have $V_{CE}=V_E=6V$ and $I_C=I_E=1.5$ mA. The circuit operates from a 20V supply, and the transistor is 100.

The collector resistance is given by

,

the designed values are shown in figure 14.

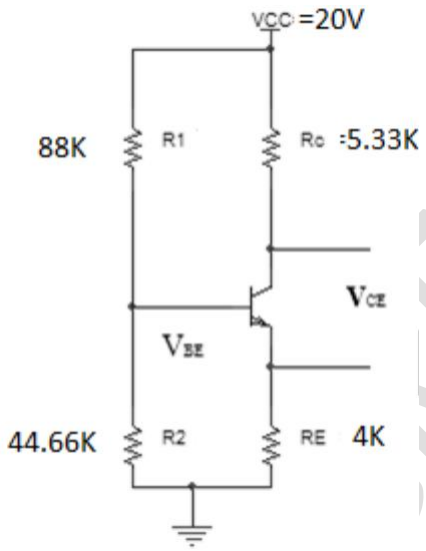

Fig.14. Voltage divider bias circuit Design

MODULE 2

Operational Amplifier

Introduction

- With the help of Integrated Circuit (IC) Operational -Amplifier (Op-Amp) design has become very simple.
- The IC version of Op-Amp uses Bipolar Junction Transistor (BJT's) and Field Effect Transistors (FET's) which are fabricated using semiconductor chip or wafer.
- The circuit design become very simple these are low cost, small size, versatile, flexibility and dependability.
- Op-Amp are used in the field of process control, communications, computer power and Signal source display.

Definition

The Op-Amp can be defined as high gain, direct coupled difference amplifier.

Each term in the definition if define as

- The word gain means the voltage gain Op-Amp which is the ration of output voltage to the input voltage.
- The word direct coupled indicates the Op-Amp can be amplifying signals of zero frequency that means zero DC signal.
- The difference amplifier means that the Op-Amp will have two inputs and the output is proportional to the difference between the two inputs voltage.

The symbol for the Op-Amp is shown in the figure1.

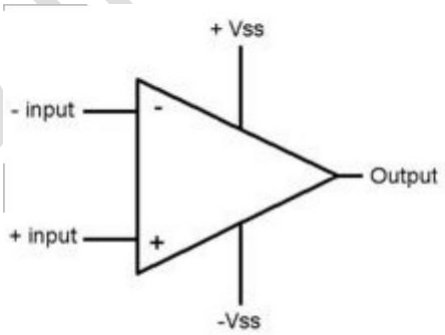

Fig. 1: Symbol of Op-Amp

Architecture of Op-Amp or Block diagram of Op-Amp

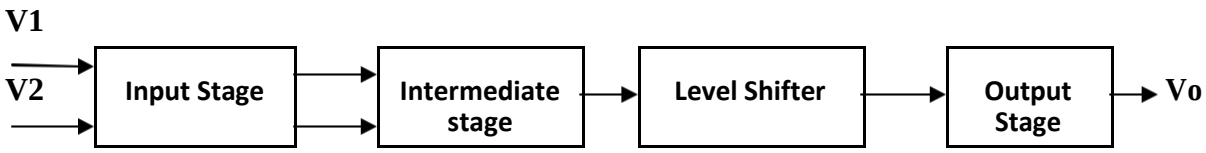

Fig. 2: Block diagram of Op-Amp

The Block diagram of Op-Amp as following elements namely

- Input stage
- intermediate stage
- Level shifter stage
- output stage

Input Stage:

- This is the first block of the Op-Amp with two input and one output stage.
- The output voltage is proportional to the difference between the two input voltages.
- This stage can be amplifying DC voltages hence it is said to be DC coupled.
- The difference amplifier consists of two BJT's with emitter terminal connected together this is also called emitter coupled difference amplifier.
- Since there are two BJTs there are two base terminals hence the circuit will have two input terminal.

Intermediate Stage

- The output of the input stage drives next stage called intermediate stage.
- The overall gain requirement of Op-Amp is very high the input stage alone cannot provide such high gain.
- Intermediate stage provides an additional voltage gain with cascaded amplifiers called multistage amplifier used to get high gain.

Level Shifter

- Shifts the level of output of intermediate stage this stage shifts DC level.
- This similar to clamper circuit.

Output Stage

- The last stage of Op-Amp is the output stage
- The output is connected to the load. This stage is called "Driver Stage" the output stage provides required power output.
- Push pull complementary amplifier are used as the driver stage.
- This is also called as the power the power amplifier.

Ideal Op-Amp

The full form of op-amp is an operational amplifier, is most important and versatile Integrated Circuit. It is used in analog signal processing and analog filtering. The Integrated Circuit version of op-amp uses BJT's and FET's. Op-amps are fabricated using semiconductor chip or wafer. It was used in the analog computer to perform a variety of mathematical operations such as addition, subtraction, multiplication etch, hence the name operational amplifier.

The characteristics of Op-Amp are discussed below.

1. **Infinite input impedance:**
   Infinite input impedance is defined as the impedance seen at the input terminals of the op-amp. The impedance parameter is one which opposes the flow of current. Infinite impedance means that the op-amp draws zero current from the source connected at the input terminals of op-amp. When zero current is drawn from the source, we say that the loading effect is zero.
2. **Infinite Voltage gain**
   The voltage gain, which is ratio of output voltage to input voltage is infinite.
   $A_{OL}=\infty$,
   The differential open loop gain is infinite for ideal op-amp.
   This means that for any input voltage, the output voltage of the op-amp becomes infinite.
3. **Zero output impedance**
   The impedance at the output terminal is zero.
   This means that output voltage is independent of the current at the output terminal.
   Since output impedance is zero, there is no voltage drop inside the op-amp due to the current at the output terminal.
   This phenomenon that the output voltage is independent of the output current is referred to as zero loading effect at the output terminal.
4. **Infinite Bandwidth**
   The bandwidth increases the range frequencies of the input signals that can be amplified by op-amp. The amplifier can amplify any frequency from zero to infinity without attenuation and with equal gain.
5. **Infinite CMMR**
   CMMR means that common mode rejection ratio; it is defined as the ability of the op-amp in rejecting the input signal which are common to both the input terminals.
   The ratio of differential mode gain to the common mode gain is defined as common mode rejection ratio (CMMR).
6. **Matched transistor are used**
   The transistors used in the different amplifier are identical.
7. **Infinite slew rate**
   The slew rate indicates the rate at which the output voltage varies. Infinite slew rate indicates that the output voltage can change instantaneously.
8. **The characteristics of the op-amp are temperature independency**.

The properties of the op-amp do not change with temperature.

The applications of op-amp are

1. Used in the field of process control
2. Communication system
3. Computers
4. Power and signal sources
5. Displays and measuring system.
6. Op-amp can be used as adder, subtractor or integrator or differentiator

Ideal Op-Amp

The ideal Op-Amp is basically an amplifier which amplifies the difference between two inputs hence it is called differential amplifier.

$$Vo \alpha (V1-V2)$$

Differential Gain:

$$Vo=A_d (V1-V2) \qquad A_d=\text{Constant of proportionality}$$

- The A_d is the gain with which differential amplifier amplifies the difference between two input signal hence it is called difference gain.
- The difference between two input voltages

$$V_d=V1-V2$$

$$Vo=A_d * V_d$$

$$A_{d=}$$

A_d in decibel

$A_d=20\log A_d$ in db

Common mode Gain

- Common mode input voltage is the average of the two input voltages, it can be expressed as

$$V_{iCM} =$$

- The common mode voltage is the ratio of the common mode output voltage to common mode input voltage.

——

CMRR (Common Mode Rejection Ratio)

- It is defined as the ratio of differential mode gain to the common mode gain. The symbol used is

=—

- It is the ability of the operational amplifier to reject the common mode signal CMRR is infinity for an ideal op-amp. Because ideal mode Op-amp ensures that zero common mode gain. Due to this common mode noise output voltage is zero for an Op-amp.

Slew Rate

As shown in figure 3 the output voltage varies slowly. The slew rate can be found as ratio of change in output voltage (ΔV_O) to time (Δt) required for the output voltage to change.

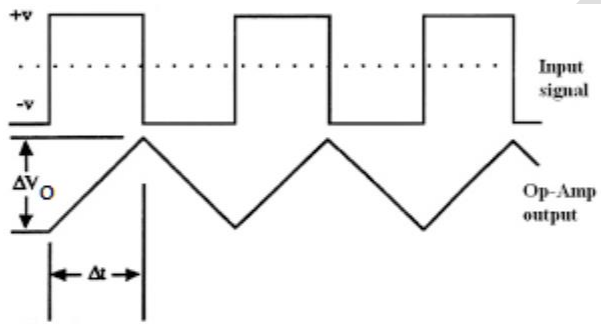

Fig.3:Slew rate

Slew rate = —— for maximum

For a sinusoidal signal $V_O=V_m \sin(\ t)$,

Slew rate, —— = V_m = $2\pi f_m V_m$

Virtual Ground Concept in Op Amp

- Consider the circuit shown in the figure 4 below

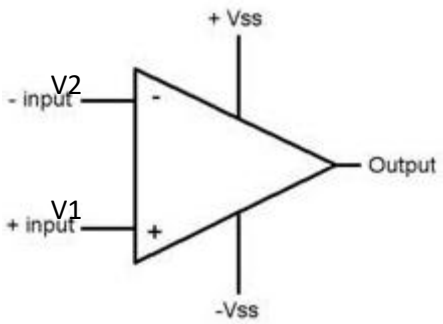

Fig. 4: Op-Amp to explain the Virtual Ground concept

- Let V1 and V2 be the voltage at non inverting and inverting terminal.
- W.K.T

$$Vo \alpha (V1-V2)$$

$$Vo=A (V1-V2) \qquad A=\text{open loop gain of Op-Amp}$$

$$V1-V2= —$$

$$V1-V2= 0$$

$$V1=V2$$

- The Mathematical expression V1-V2= 0 indicates that the potential difference between two input terminal is zero this zero voltage is treated as ground.

Application of Op-Amp

1) Inverting Amplifier

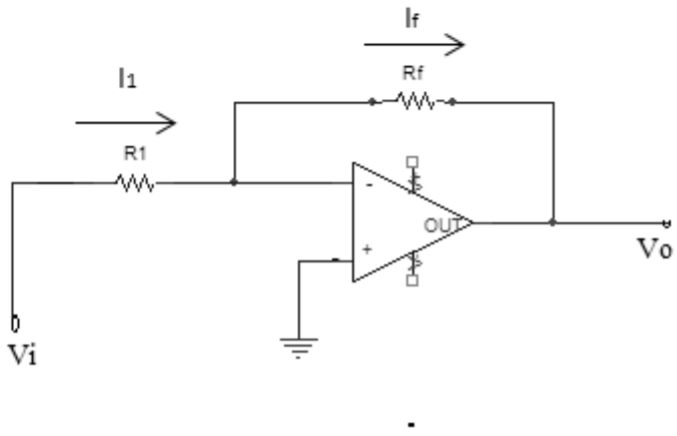

Fig. 5: inverting Op-Amp

- Step1: find the voltage at the Non inverting terminal, the input voltage is applied to non-inverting terminal, hence $V_A=0$
- step2: From the concept of Virtual ground, the voltage at the inverting terminal is equal to the voltage at the non-inverting terminal, $V_B=V_A=0$
- step3: Apply KCL at inverting terminal, Currents entering into the inverting terminal is equal to the currents leaving from the terminal.

- Step4: Replace the current by Ohm's law

- The final expression of the output voltage is given by

$$V_o =$$

- The gain of op-amp is

$$A =$$

2) Non-Inverting Amplifier

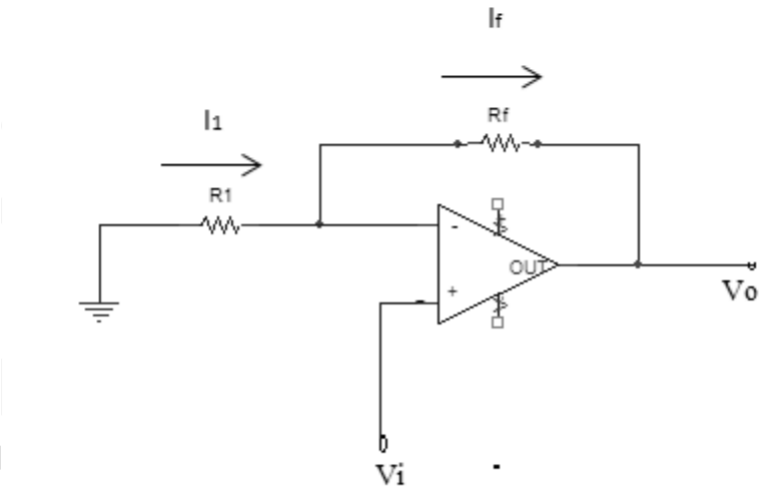

Fig. 7: Non- inverting Op-Amp

- Step1: find the voltage at the Non inverting terminal $V_A=V_i$
- Step2: From the concept of Virtual ground $V_B=V_A=V_i$
- Step3: Apply KCL at Inverting terminal
- Step4: Replace the current by Ohm's law

- The final expression of the output voltage is given by

— — —

Vo= — —

Vo= —

- The gain of op-amp is given by

A=

3) Voltage follower

- The circuit of Voltage follower circuit with non-inverting configuration is shown in figure 8.
- The input is connected to the Non-inverting terminal directly. Science the input signal is connected to the non-inverting terminal, the circuit said to have called as non-inverting configuration.
- The output terminal is connected to inverting terminal directly to provide the negative feedback.

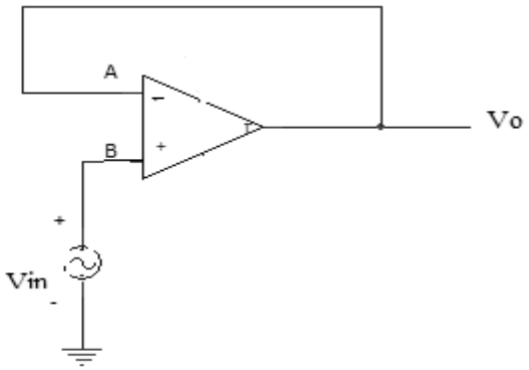

Fig. 8: Voltage follower circuit

To find expression for output voltage of the voltage follower:

- Step1: find the voltage at the non-inverting terminal. The Non-inverting terminal is connected to the input source. Therefore the voltage at the Non-inverting terminal is given by

$V_B=V_{in}$

- Step2: From the concept of Virtual ground the voltage V_A at the inverting terminal is equated to voltage at the non-inverting terminal V_B.

i.e., $V_A=V_B$

$V_A=V_B=V_{in}$

- Step3: Since inverting terminal is connected to the output side, the output voltage is given by

$$V_o = V_A = Vin$$

- Since, the output voltage and input voltages are equal; the changes in the output voltage will be same as that of the input voltage. Hence it is called as Voltage follower or source follower circuit and unity gain amplifier.

4) Summing Circuit

An Op-Amp circuit in which the output voltage is proportional to the sum of the all the input voltage.

Two types of summer circuit are
a) Inverting Summer circuit
b) Non Inverting summer circuit

a) Inverting Summer circuit

- The three input inverting summing amplifier is shown in figure 9 below.

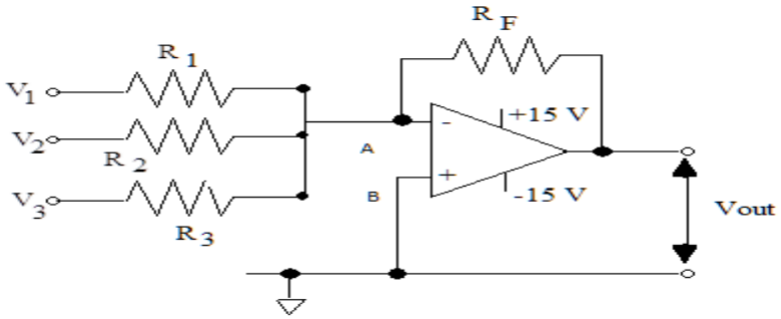

Fig. 9: Inverting Summing amplifier

- Step1:The voltage at the non-inverting terminal is given by $V_B=0$
- Step2: From the concept of virtual ground, the voltage at the inverting terminal is $V_A=V_B=0$
- Step3: Apply KCL at inverting terminal. Let are the currents through the resistors R_1, R_2, R_3. Let I_f is the currents through the resistor R_f. Kirchhoff Currents Law states that the sum of the currents entering a terminal must be equal to the currents leaving the terminal.

$$I_1+I_2+I_3=I_F$$

- The output voltage

Choose $R_1=R_2=R_3=R$

Vo= —

Hence the three input summing circuit can be used as summing amplifier with gain R_f/R.

b) Non Inverting summer circuit

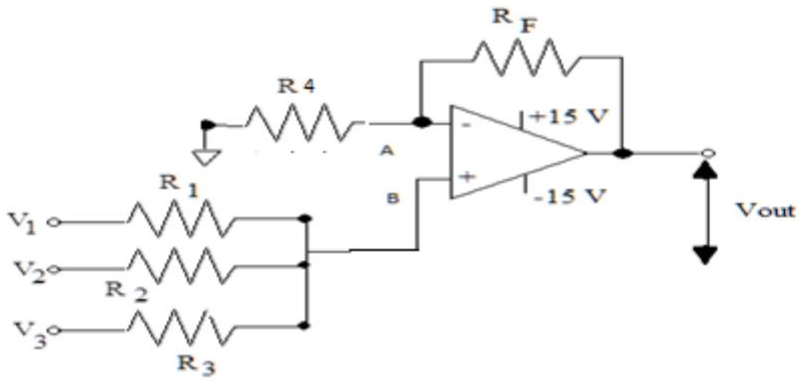

Fig. 10: Non- Inverting Summing amplifier

- Step1:The voltage at the non-inverting terminal is given by applying KCL at node B then $I_1+I_2+I_3=0$
  Replace each current by Ohm's law

Let $R_1=R_2=R_3=R$

$V_1-V_B+V_2-V_B+V_3-V_B=0$

$V_B= (V_1+ V_2+ V_3) / 3$

Step2: From the concept of virtual ground, the voltage at the inverting terminal is $V_A=V_B= (V_1+ V_2+ V_3) / 3$

Step3: Apply KCL at inverting terminal.

$I_4=I_f$

Step 4: Replace the current by Ohm's law.

— — —

Vo= — —

Vo= —

The output voltage ——— —

then $V_0 = V_1+V_2+V_3$

The output voltage is equal to the sum of three input voltages . The polarity of the output voltage is positive. this indicates that the circuits is a non- inverting summer circuit.

5) Integrator

- The operational amplifier can be used as integrator. The op-amp integrator circuit is shown in figure 11.

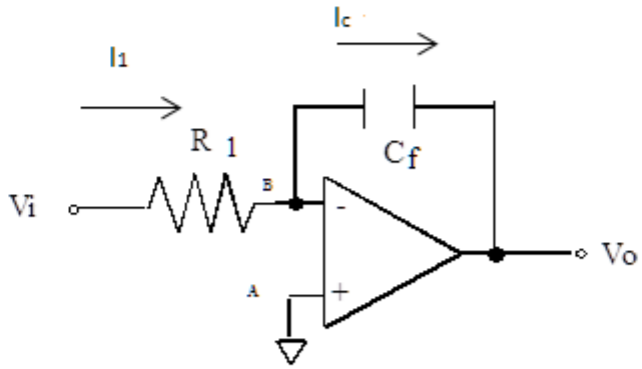

Fig. 11: Integrator

- The input signal V_i is connected to the inverting terminal through a resistor R_1. Since the input is connected to the inverting terminal, the circuit is called as an inverting amplifier. For the circuit to behave like an integrator, a capacitor is necessary. Therefore, the capacitor is connected in feedback path; between the output terminal and the inverting input terminal.
- Step1: Find the voltage at the Non inverting terminal $V_A=0$
- Step2: From the concept of Virtual ground, the voltage at the inverting terminal is same as the voltage at the non-inverting terminal.

$V_B=V_A=0$

- Step3: Apply KCL at inverting terminal
- Step4: Replace all the current by Ohm's law

———

- The final expression of the output voltage is given by

—----------(1)

- The final output voltage is given by

— ----------(2)

- Substitute the I_C value from equation (1) into equation(2)
- Then the output voltage is given by

— —

- Here output voltage is integral of the input voltage and hence the circuit can be called as an integrator

6). Differentiator

- In this circuit V_{in} is connected to inverting terminal through the capacitor C. the resistor R_f is connected in the feedback path between the output terminal and the inverting terminal. The non-inverting terminal is connected to ground. Op-amp differentiator is shown in figure 12.

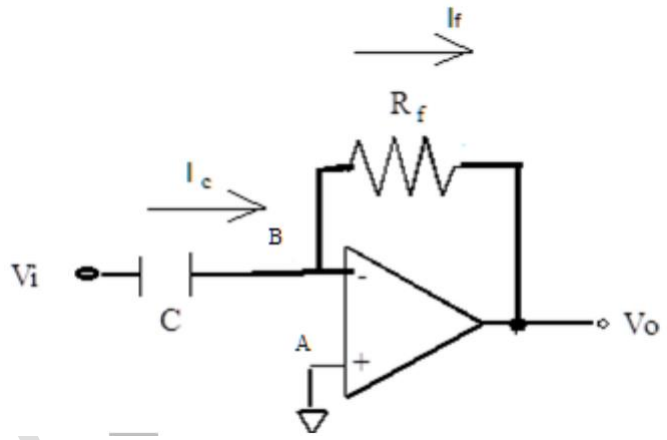

Fig. 12: Differentiator

- Step1: find the voltage at the Non inverting terminal, the non-inverting terminal is connected to ground hence the voltage is given by $V_A=0$
- Step2: From the concept of Virtual ground, the voltage at the inverting terminal is equal to the voltage at the non-inverting terminal.

$$V_B=V_A=0$$

- Step3: Apply KCL at inverting terminal; KCL states that sum of all the currents at the node are zero. Here we have two current. the current entering into the inverting terminal is equal to the current leaving from the inverting terminal then,

- Step4: Replace the current by Ohm's law

$$\frac{\quad}{\quad}$$

$V_B=0,$

$$\frac{\quad}{\quad}$$

Let V_C is the voltage across the capacitor

$$V_C=V_i-V_B$$

$$V_C=V_i-0$$

$$V_C=V_i$$

we know that $I_C = C (V_C)$

(

- Thus the output voltage is derivative of the input voltage and hence the circuit can be called as an differentiator. The negative sign indicates in the output expression indicates that the op-amp is connected as an inverting configuration.

7). Subtractor

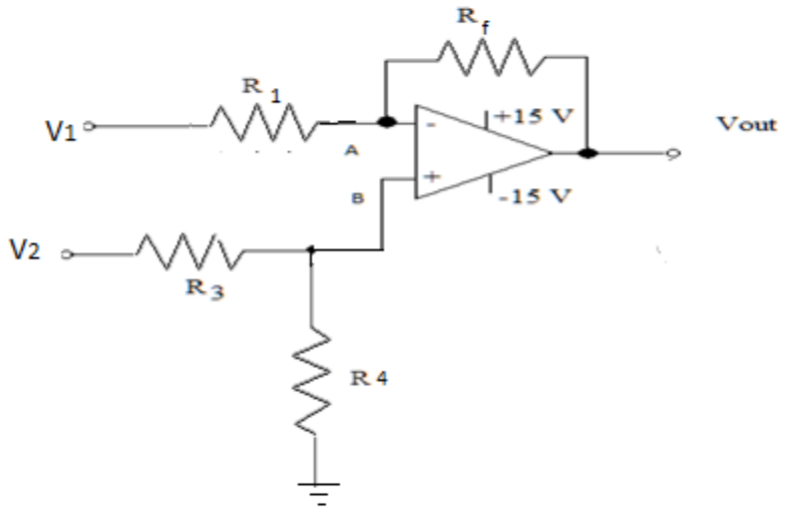

Fig. 13: Subtractor

- Step1:The voltage at the non-inverting terminal is given by applying KCL at node B then $I_1+I_2+I_3=0$
  Replace each current by Ohm's law

Step2: From the concept of virtual ground, the voltage at the inverting terminal is $V_A=V_B=$

Step3: Apply KCL at inverting terminal.

$I_1=I_f$

Step 4: Replace the current by Ohm's law.

Vo= -

if

Vo= -

Vo= — —

Vo= —

Hence the output is proportional to the difference between the two input voltages. the it acts as a subtractor or difference amplifier.

Problems on Operational Amplifier

1). For a non-inverting op-amp. Find the gain of the amplifier if R_F=10KΩ and R_1=1KΩ.

Ans. to Find the gain of the amplifier

Given Data: R_F=10KΩ and R_1=1KΩ.

The output voltage for a non-inverting op-amp is

Vo= —

The gain of op-amp is given by

A=

If R_F=10KΩ and R_1=1KΩ

A= 11= gain of the Non inverting amplifier.

2). Calculate the output voltage of a three input inverting summing amplifier, given R_1=200KΩ, R_2=250KΩ, R_3=500KΩ, R_f=1MΩ, V_1=-2V, V_2=-1V, and V_3=+3V.

The output voltage of three input inverting summing amplifier is given by

Then the output voltage of a three input inverting summing amplifier

=1*

= - [-0.01-0.004+0.006]*1*

1 =8V

3) Find the output of the following op-amp circuit shown in figure Q(3)

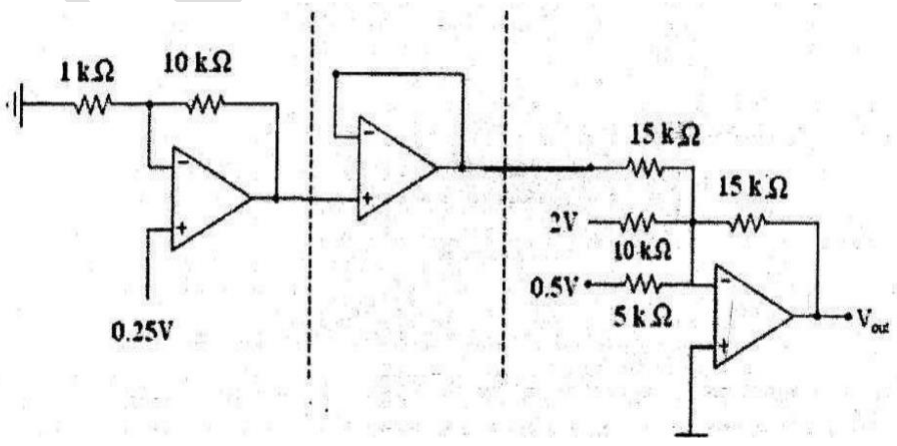

Fig. Q(3). Op-amp circuit

To find the output voltage of the op-amp circuit shown in figure Q(a) is explained below. The first op-amp is a Non-inverting amplifier; the output voltage of this op-amp is given by

V_O= — = —) *0.25V = 2.75V

The middle op-amp is voltage follower hence the voltage remains same Hence the output voltage V_O= 2.75V

The final op-amp is an inverting summing amplifier circuit — — —

—— —— —

15* .4834 = 7.25 V

4).For the op-amp circuit shown in figure Q(4) find the output voltage

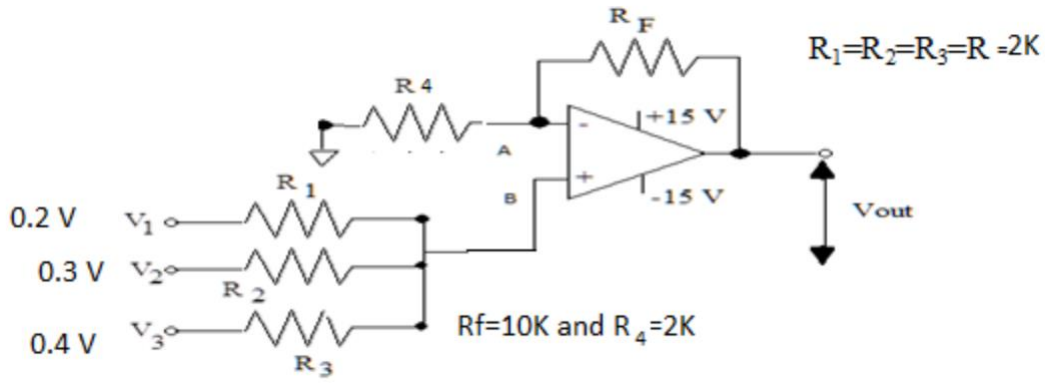

Fig. Q(4). Non inverting summing circuit

The given circuit is a non inverting summer.

the output voltage of the given circuit is given by

The output voltage

V_0=1.8V

5). Find the output voltage of the following circuit shown fig Q(5). given V_1= -10V, V_2=5V and V_3=20V

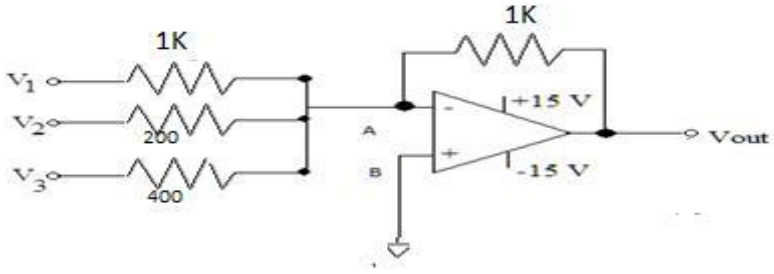

Fig Q(5). inverting summing amplifier

The output voltage of three input inverting summing amplifier is given by

— — —

Then the output voltage of a three input inverting summing

— — — amplifier ~~=1*~~ — —

=-65V

6). Find the output voltage of the following circuit. shown in figure Q(6)

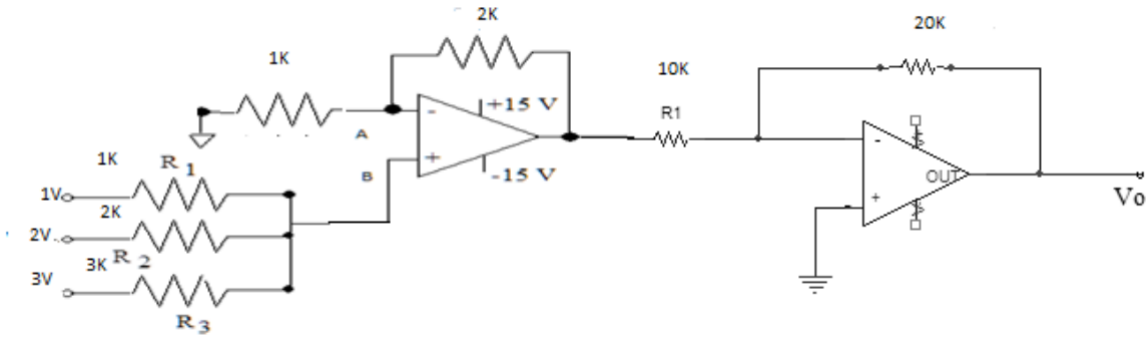

Fig Q(6). op-amp circuit

The first op-amp is a non-inverting summing amplifier and op-amp2 is inverting amplifier.

➢ Step1:The voltage at the non-inverting terminal is given by applying KCL at node B then $I_1+I_2+I_3=0$
Replace each current by Ohm's law

—

Step2: From the concept of virtual ground, the voltage at the inverting terminal is $V_A=V_B$= 1.6363 V

the output voltage is given by

Vo1= — = —

Vo1=4.909V

Op-amp two is a inverting amplifier, the output of second op-amp and the output voltage is given by

-9.8181V

7.) Find the output voltage of the following circuit shown in figure Q(7)

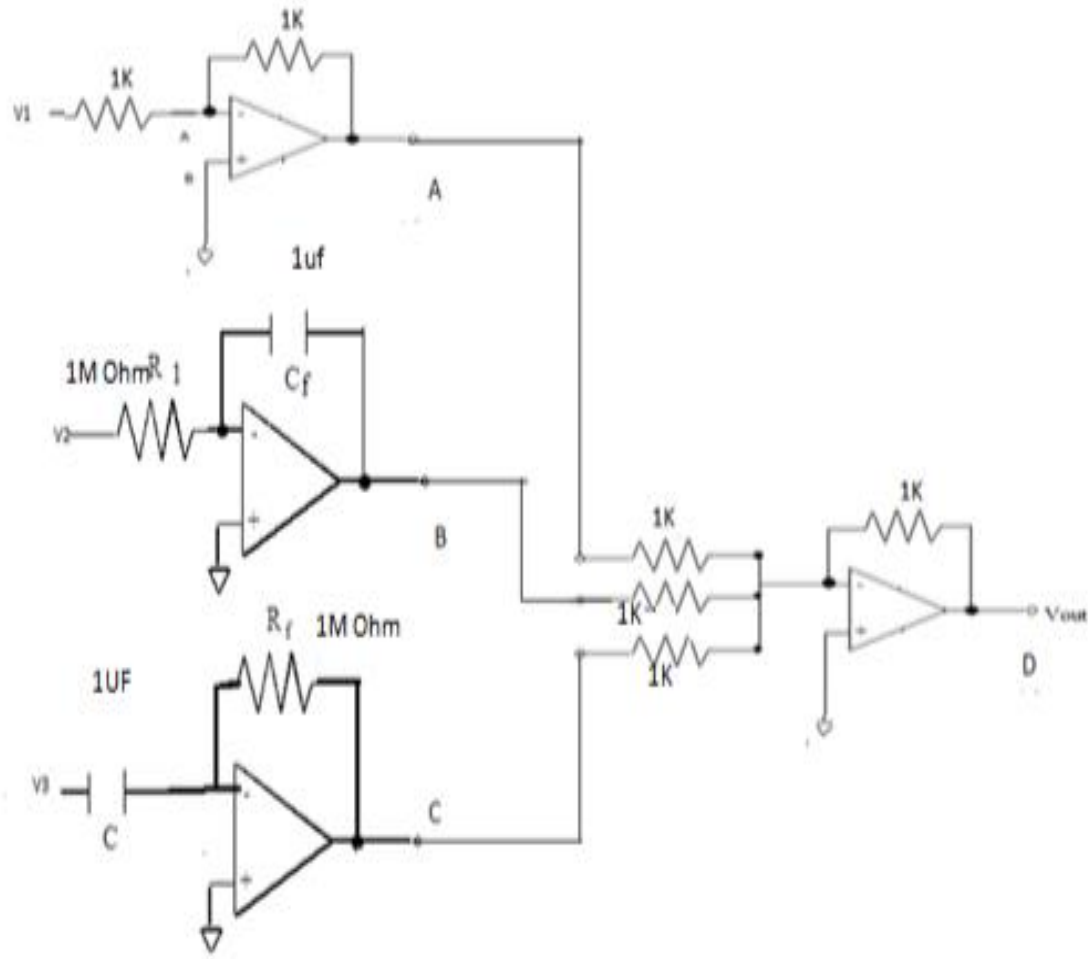

Fig. Q(7) op-amp circuit

Solution:

the A output is produced by inverting amplifier hence the output of op-amp1 is

—

—

----------(1)

The op amp2 is a integrator the output of integrator at point B is given by

The op amp3 is a differentiator the output of differentiator is given by

(

(

(-------(3)

op-amp4 is inverting summing amplifier hence, is given by

----------(4)

((

– (

8.) Find the output voltage of the following circuit shown in figure Q(8)

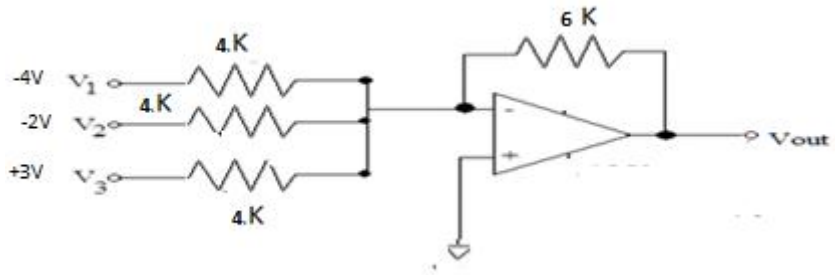

Fig Q(8) op-amp circuit

The output voltage of three input inverting summing amplifier is given by

Then the output voltage of a three input inverting summing

amplifier =1*

=-65V