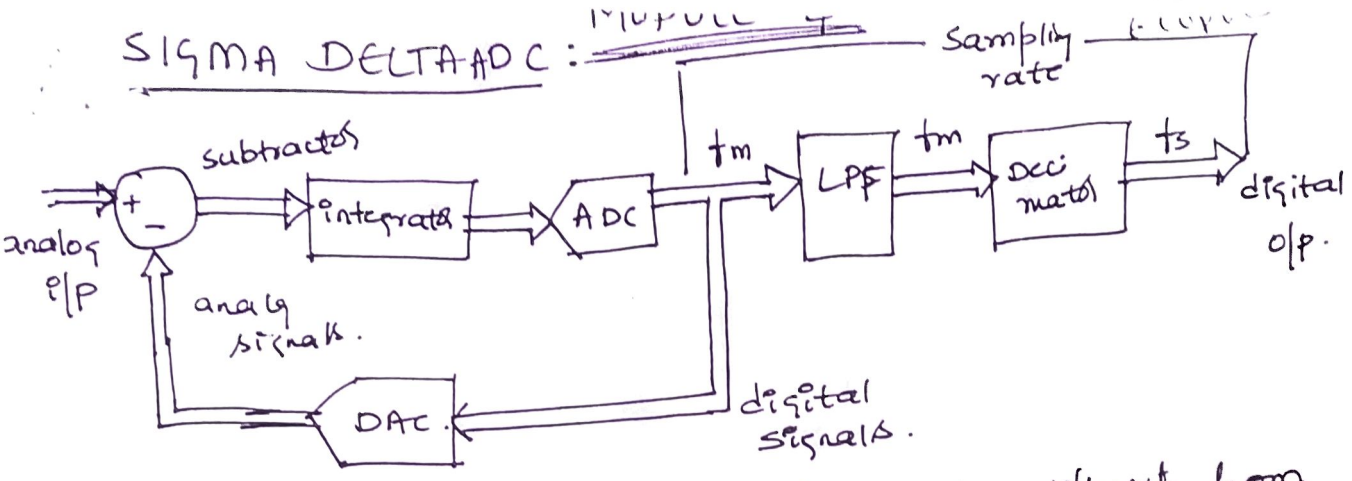
SIGMA DELTA ADC :



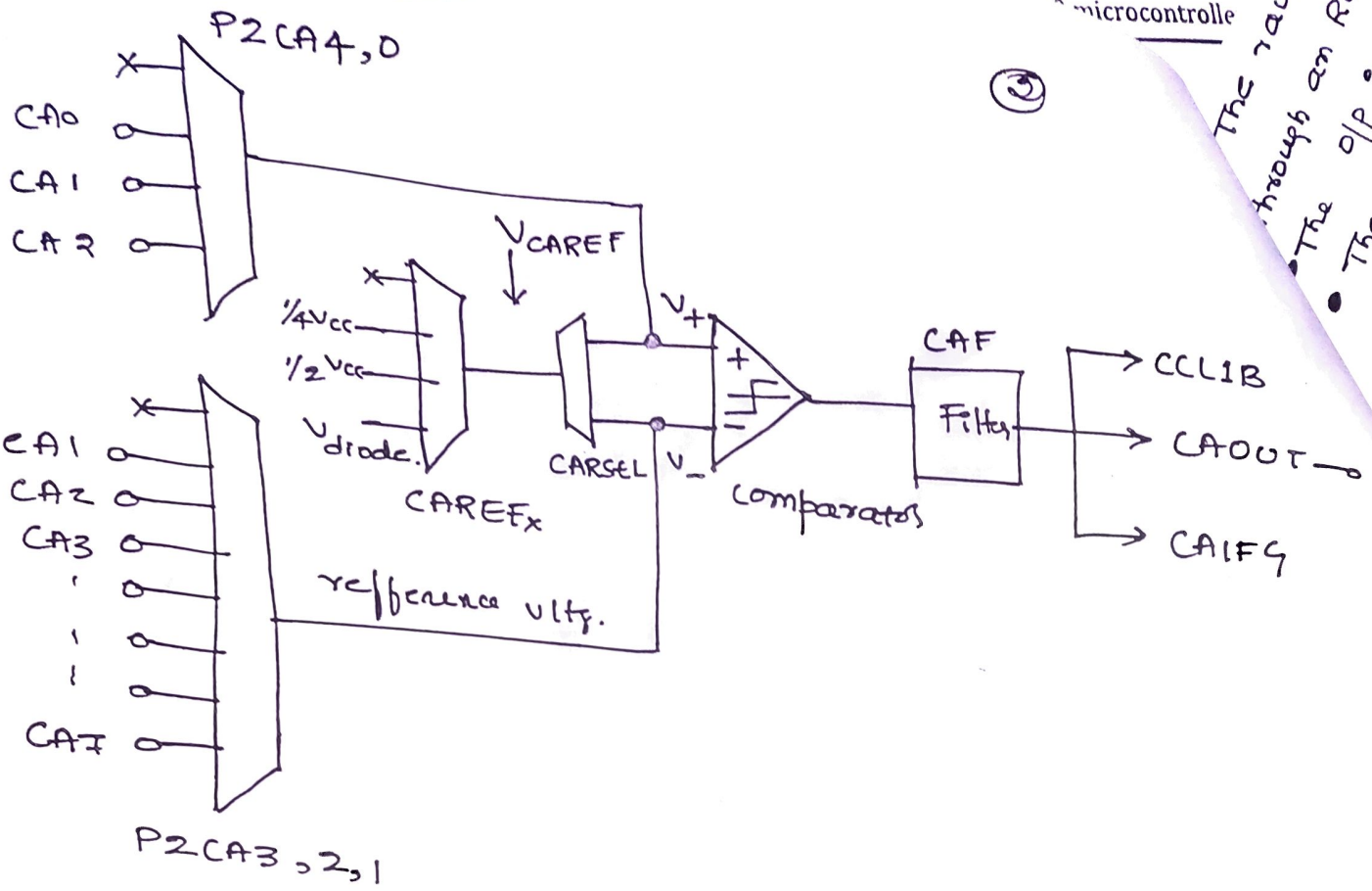
- The operat of the S-D ADC is entirely different from sucessive approximat ADCs.
- The distintinctive characteristics are high precision and low speed, which makes them ideal for many application
- The basic idea behind a S-D converter is to reduce the ADC itself to the simplest ckt possible.
- This is 1-bit ADC.
- The above fig. shows the main blocks of S-D ADC.
- It falls into 2 main parts.

→ The 1st is a feedback loop that forms the S-D modulator

- It handles the analog signals & does the basic A to D conversion.
- t_m/f_s ratio is called oversampling ratio.

→ The 2nd part of the ADC handles purely dig. signals.

- Its job is to take the fast stream of single bits from the modulator & convert them to a slower stream of multibit values.

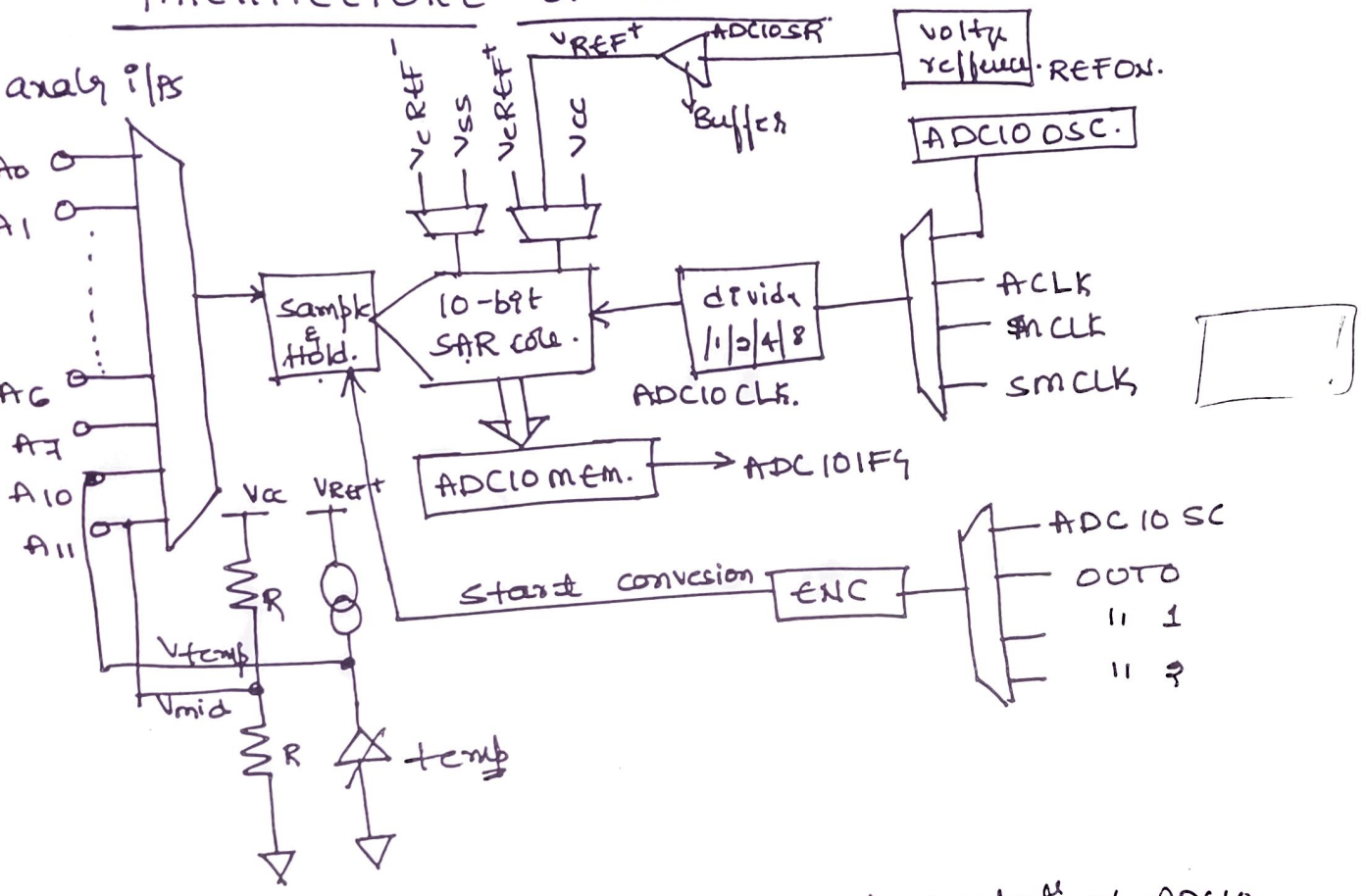


- An analog comparator compares the vltges on its i/p terminals, V_+ and V_-. its o/p is high if $V_+ > V_-$ and low if $V_+ < V_-$
- Thus it provides a basic bridge b/w the analg to dig. domain and acts like a 1-bit ADC.
- Although comparator is fairly simple, the block diagram of Cmp.. A+ in the family users guide looks complicated bcz of the many options provided.
- These are controlled with the 2 pheripheral registers CACTL1 & 2.
- The entire module is switched on & off with the CAON bit. It is off by default to save the current.
- The non-inverting i/p V_+ can be connected to external signals CA0 - CA2 without an external connection. This is selected using P2CA4 & P2CA0.
- Similarly the inverting i/p V_-.
- The internal reference vlty V_{CAREF} can be chosen from 1/4Vcc, 1/2Vcc & a fixed vlty from a transistor V_{diode}.

- The raw o/p of the comparator can optionally be filtered through an RC ckt to reduce oscillations in the signal.
- The o/p is brought to an external pin CAOUT.
- The CAIFG flag is raised on either a rising or falling edge of the comparator o/p.

(3)

ARCHITECTURE OF ADC10.



- Fig shows the block diagramic representation of ADC10. There are more i/ps in the larger device. As in the case of comp.-A+.
- Most of the features are can be configured only when the enable conversion bit ENC is clear to ensure that the ADC is inactive.
- We now look at some simple examples of measurements using the basic hardware of the ADC10.
- More complicated aspects such as triggering from hardware and data transfer controllers.

Three steps are required to make a single conversion with the ADC10.

1. configure the ADC 10, including the ADC10ON bit to enable the module.
The ENC bit must be clear during this operation bcz most of the bits in ADC10CTL0 & 1 can be changed only when ENC=0.

2. Set the ENC bit to enable a conversion.
This cannot be done while the module is being configured in the previous step.

3. Trigger the conversion, either by setting the ADC10SC bit or by an edge from TA. (timer-A).

(4)

ADC 12

- ADC 12 works on the same principles as the ADC10.
- Principal distinctions b/w ADC12 & 10 are.

→ The o/p has 12 bits rather than 10.
→ Higher precision requirement on sampling timer.
→ The internal voltage reference requires an external bypass capacitor. This takes a long time to charge after the reference has been turned on.
→ sampling time can be controlled in two ways (i) by pulse mode, (ii) extended sample mode (SAMPCON)
→ Analog i/ps are enabled with PnSEL rather than a seperate analog enable register.
→ Conversions are specified and the Results are stored in an entirely different way.

ADC12MEMn → 16 memory's.

ADC12MCTLn → Reference voltage
→ i/p channel.

CONSEQ → selects single or multiple conversions.

→ No data transfer control to ADC12 but results can be moved from ADC12MEM. registers.

→ A single interrupt vector is shared by 18 flags.

16 → corresponds to memory

2 → over run.