

## Field effect transistor (FET)

- \* Field effect transistors are three terminal semiconductor device, where the conduction path is controlled by an electric field established by the carriers present in the device.
- \* Concept of FET predates that of BJTs.
- \* The major difference is in BJT the collector current ( $I_C$ ) is a direct function of the base current ( $I_B$ ) whereas in FET the drain current depends on the gate source Voltage  $V_{GS}$ .
- \* Hence BJT are current controlled device and FET are voltage controlled device.

FET are classified into

Varanth Nayak  
ISE | CEC.

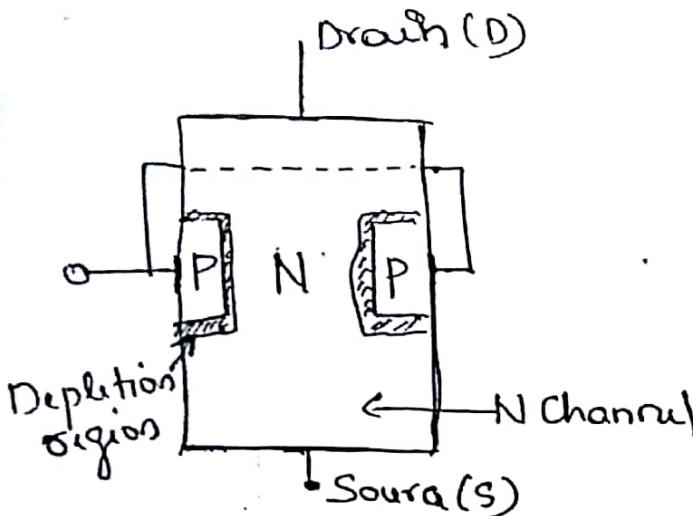
- (1) Junction FET (JFET)
- (2) Metal-oxide-semiconductor FETs (MOSFET)
  - ↳ (a) enhancement MOSFET
  - (b) depletion MOSFET

- \* BJT are bipolar device both electrons and holes contribute to the flow of current
- \* FET are unipolar device here either electrons or holes contribute to the current so it is further classified as
  - (a) N channel FET (electrons)
  - (b) P channel FET (holes)

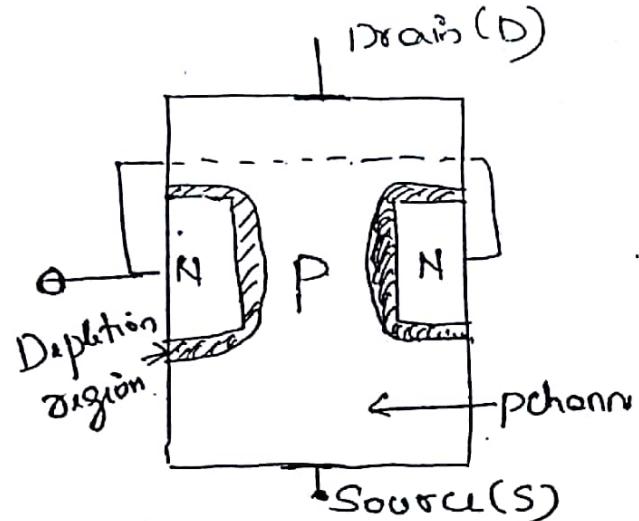
## Junction Field effect transistors :

### Construction and principle of operation:

- \* JFET is a three terminal device where voltage applied at one terminals controls the current at the other two terminals. Depending on the type of channel it is classified as N channel FET or p channel FET.
- \* In N channel JFET N type of semiconductor material forms a channel between embedded layers of p type and in p type P-channel FET p type of semiconductor material forms a channel between embedded layers of N type.
- \* So in each case two p-n junctions are formed.
- \* In an N channel JFET both embedded p type layers are connected and referred as gate (G) and via Verso
- \* Other two terminals are referred as drain (D) and source (S)

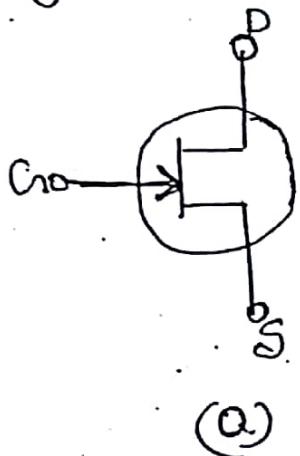


(a)

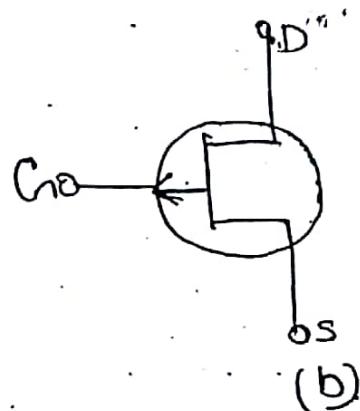


(b)

Fig cross Sectional of N channel and P channel JFET



(a)

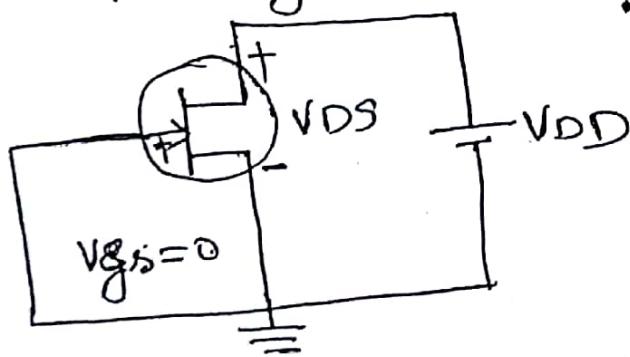


(b)

fig. circuit Symbol of N and P channel JFET

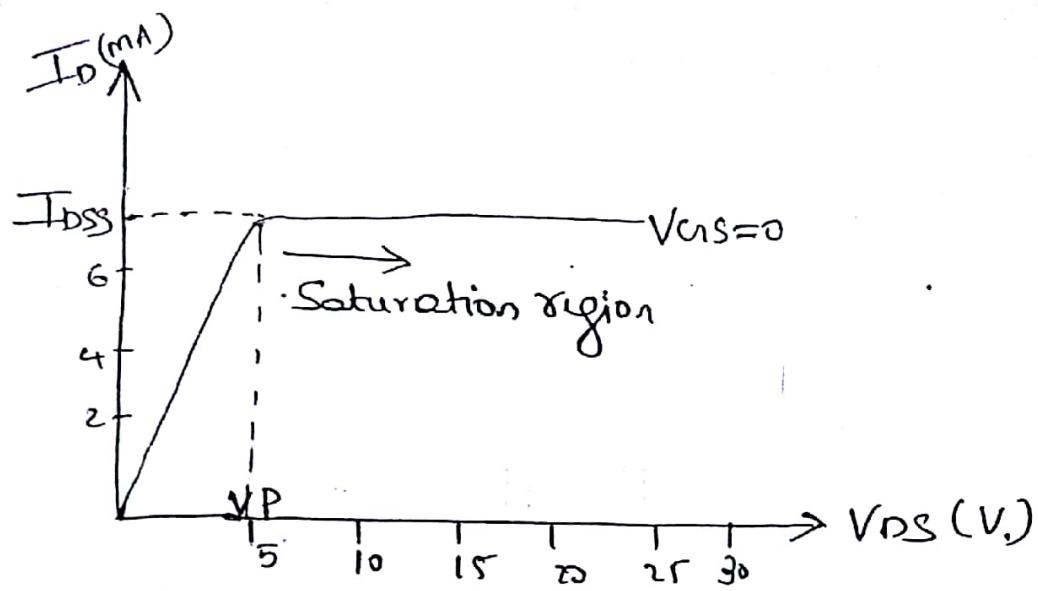
\* In the absence of externally applied potential.

both P-N junction are open circuit

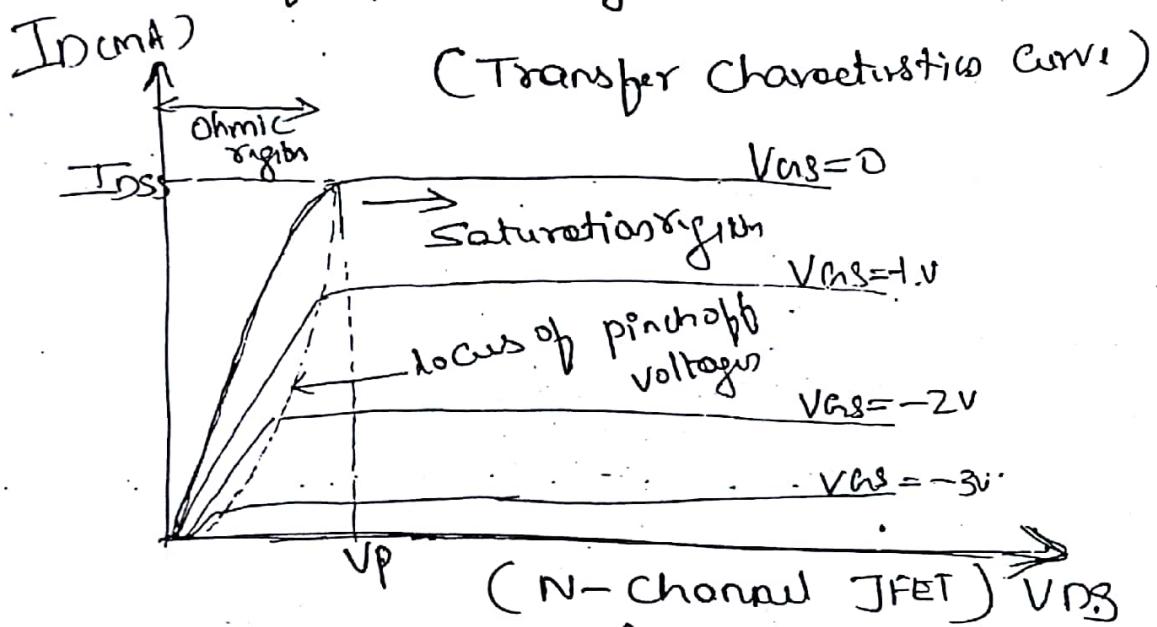


\* When the drain-source voltage is applied, the electrons in the N channel are attracted to the drain terminal establishing the flow of drain current.

- \*  $I_D$  determined by the value of the applied  $V_{DS}$  and the resistance of the N channel between the drain and source terminals
- \* Owing to the flow of  $I_D$  and increase in the channel resistance, which reverse bias the two p-n junctions which in turn results in increase in the depletion region near the drain region than the source region
- \* So for given  $V_{GS}=0$   $I_D$  increases linearly with increase in  $V_{DS}$  till  $V_{DS}$  reaches a value where  $I_D$  saturates.
- \* The value of  $V_{DS}$  at this point is referred as the pinch-off voltage ( $V_p$ )
- \* When  $V_{DS}$  reaches  $V_p$ , the value of  $I_D$  does not change.
- \* Here the  $I_D$  is referred as  $I_{DSS}$ , the drain source current for short circuit connection between gate and source ( $I_{DSS}$ )
- \* This condition is referred as pinch off condition
- \* Fig shows the characteristic curve for  $I_D$  versus  $V_{DS}$  for  $V_{GS}=0$



\* Following fig shows Characteristics curves for different value of  $V_{GS}$  (Negative biased)



The drain resistance ( $r_d$ ) in the saturation region is given by

$$r_d = \frac{r_0}{(1 - V_{GS}/V_P)^2}$$

where  $r_0$  is the resistance at  $V_{GS} = 0$

ii  $r_d$  is the resistance at particular value of  $V_{GS}$ .

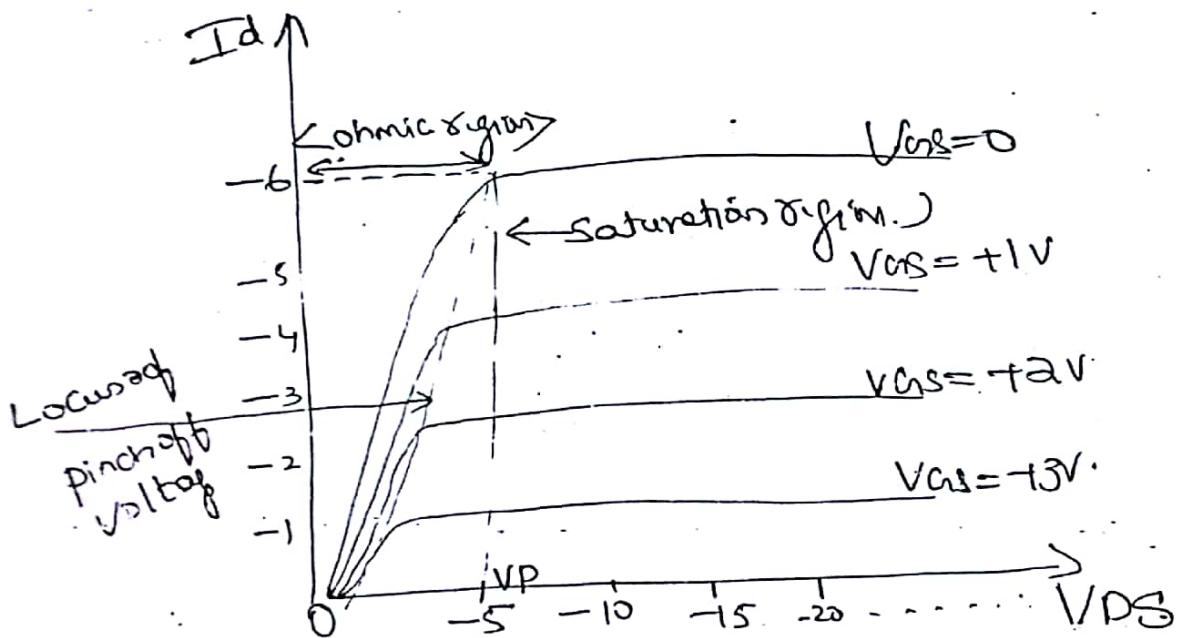
where  $V_P$  is the pinch-off voltage.

The relationship between the off current  $I_D$  in the saturation region for a given value of input  $V_{GS}$  is given by

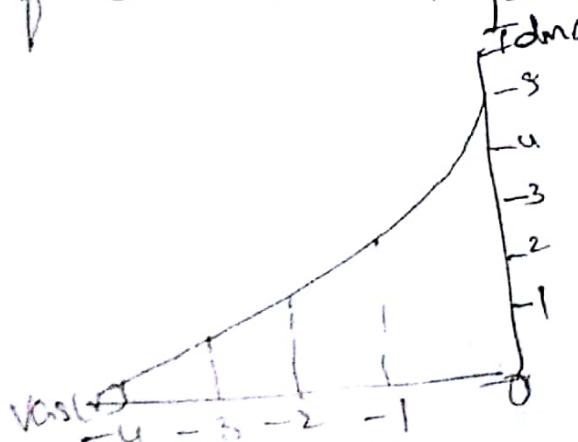
$V_{GS}$  is given by

$$I_D = I_{DSS} \left( 1 - \frac{V_{GS}}{V_P} \right)^2$$

Following fig shows transfer characteristics of P-channel JFET.



- \* Here pchannel JFETs behave in the same manner as the N-channel JFETs with direction of currents and polarities of voltage reversed



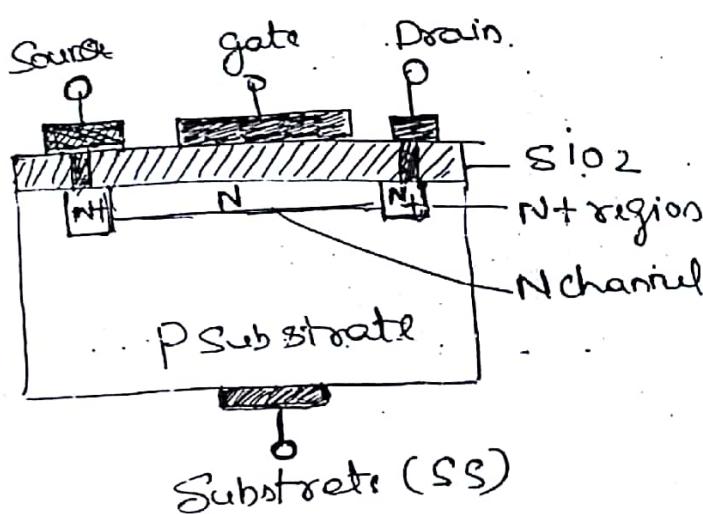
# Metal Oxide Field effect transistors

(4)

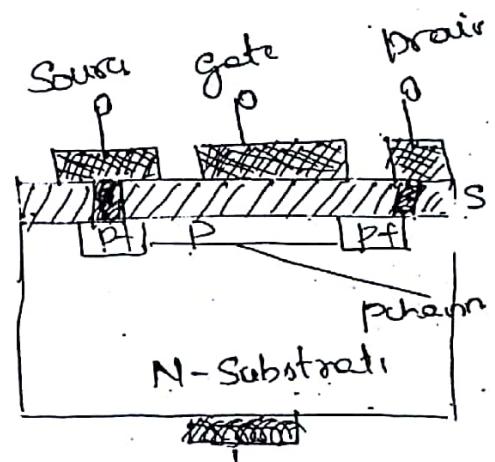
- \* MOSFET is insulated from the semiconductor channel by a very thin oxide layer.
- \* it is also referred as insulated gate field effect transistors (IGFET)
- \* Mosfet are three terminal device, further classified into
  - (1) Depletion MOSFET
  - (2) Enhancement MOSFET

Vasantha Nayak  
IISB / CBC

## Depletion MOSFETs :



Cross section of N-DE MOSFET



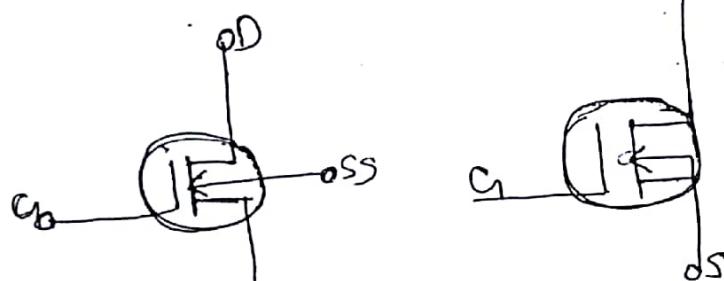
Substrate (SS)  
P-DE MOSFET

- \* Here a channel is physically constructed betw. The drain and source terminals.

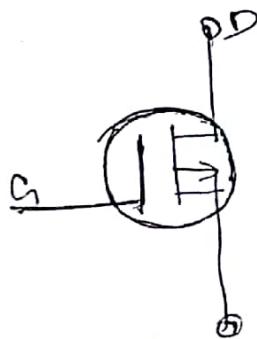
- \* In N channel DE-MOSFET substrate made of P type and vice versa.

- \* The source and drain terminals are formed by connecting metal contact to the two N+ regions.
- \* The gate terminal is connected to the insulating Silicon dioxide ( $\text{SiO}_2$ ) so no direct electrical connection between the gate terminal and channel of DE-MOSFET.
- \* There is a capacitance that exists between gate and the channel. Hence input impedance of a DE-MOSFET is very high of the order of  $10^{10}$  to  $10^{15} \Omega$ .

- \* The construction of pchannel DE-MOSFET is shown in the figure with Substrate is N type of semiconductor material.



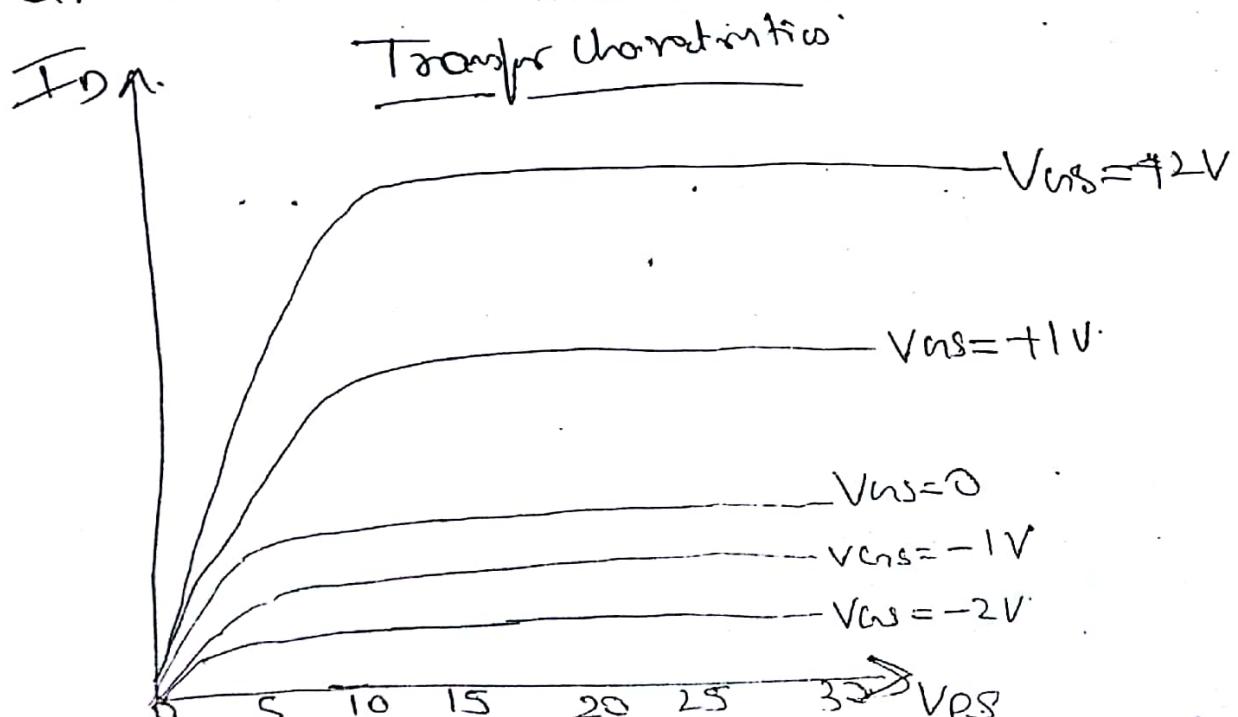
Circuit Symbol of N-channel DE-MOSFET

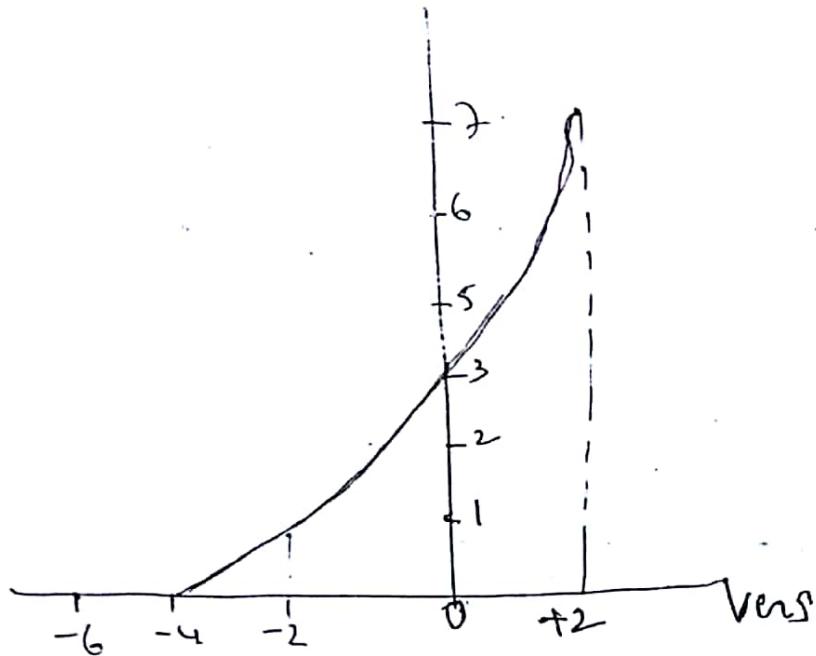


Circuit Symbol of P-channel DE-MOSFET

\* Let us see how the N-Channel DE-MOSFET Operates

- \* When the gate and source terminals are shorted. That is  $V_{GS} = 0$  and  $V_{DS} > 0$ . There will be a flow of current in the N channel as the electrons are attracted by the positive potential at the drain terminal.
- \* The current increases with increase in  $V_{DS}$  and after a certain value of  $V_{DS}$  it becomes constant.
- \* When gate terminal is at negative potential as compared to source terminal. Electrons in N channel are repelled towards p type substrate which results in the combination of holes and electrons and reduces the number of electrons which in turn reduces drain current.
- \* For the positive value of gate source voltage, the drain current increases.

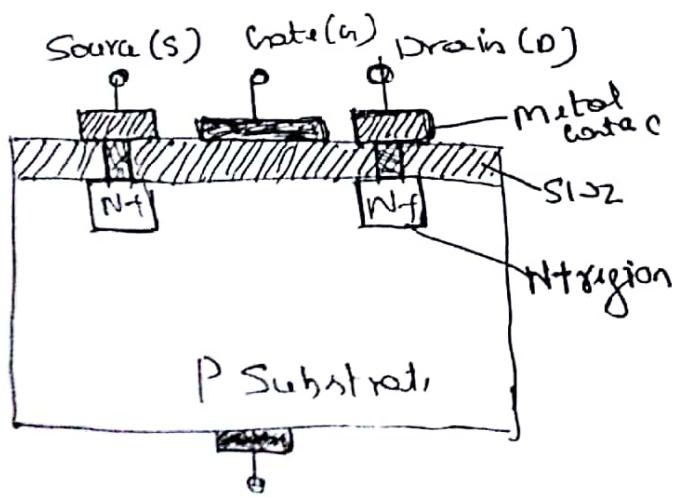




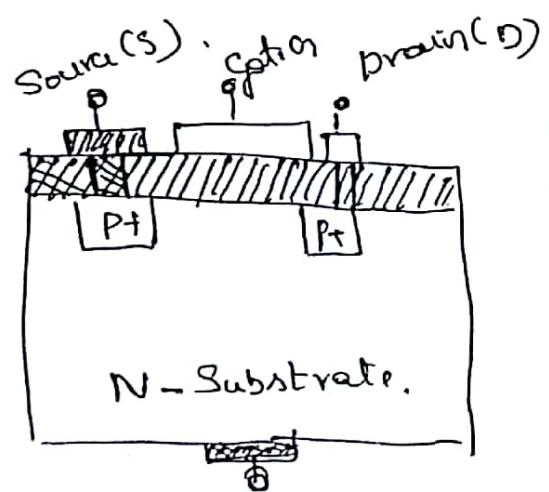
## Enhancement Mosfet

\* Construction of an E-MOSFET is similar to that of a DE-MOSFET with the difference that there is no physical channel between the source and drain terminals in the E-MOSFET.

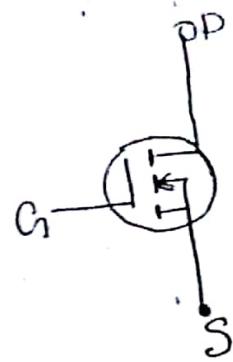
\* The Application of E-MOSFETs - in digital electronics and computers



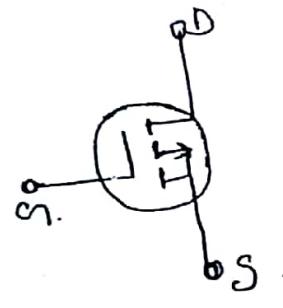
N-EMOSFET



P-E-MOSFET



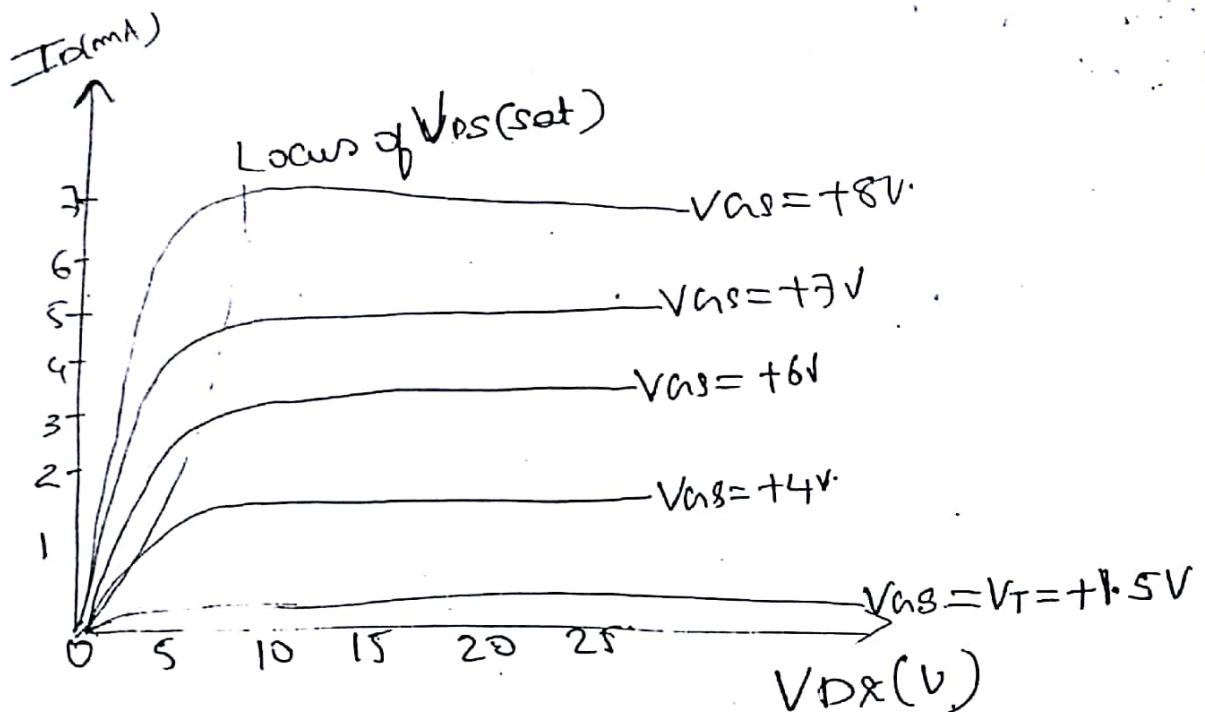
N - E-MOSFET



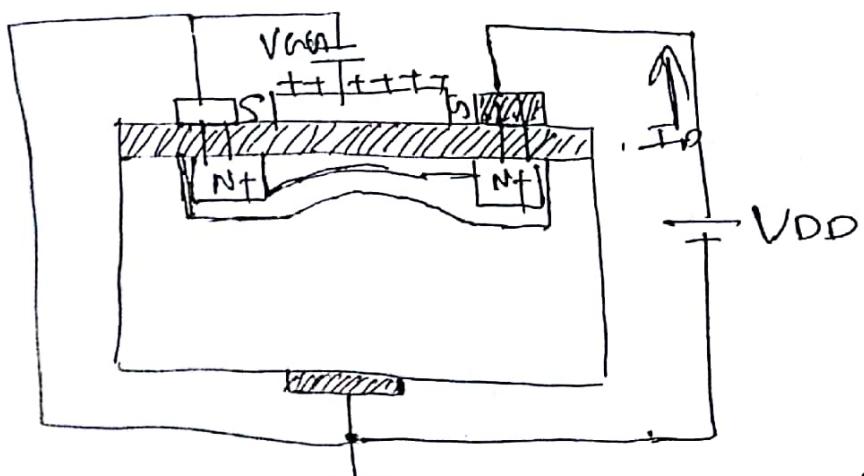
P channel E-MOSFET

Function :

- \* When  $V_{GS}$  is 0 and some positive drain voltage is applied there is no drain current. As there is no channel available for flow of drain current. This stage normally called OFF MOSFET.
- \* The drain current flows only when  $V_{GS} > 0$  as this induces a channel by drawing the electrons in the P-type to accumulate near the surface of the  $\text{SiO}_2$ . Also holes in the P-substrate are forced to move away from the edge of  $\text{SiO}_2$ .
- \* This leads to flow of current between the drain and source terminals.
- \* As  $V_{GS}$  is increased it leads to an enhanced flow of drain current, which eventually saturates due to the reduction in the gate-drain voltage  $V_{GS}$  with increase in the drain-source voltage  $V_D$ .



- \* Reduction in the gate-drain voltage reduces the attractive forces from carriers in the induced channel near the drain region resulting in the reduction of effective channel near the drain region. This is referred as pinching effect.
- \* So pinching effect is nothing but reduction in the width of the channel near the drain region

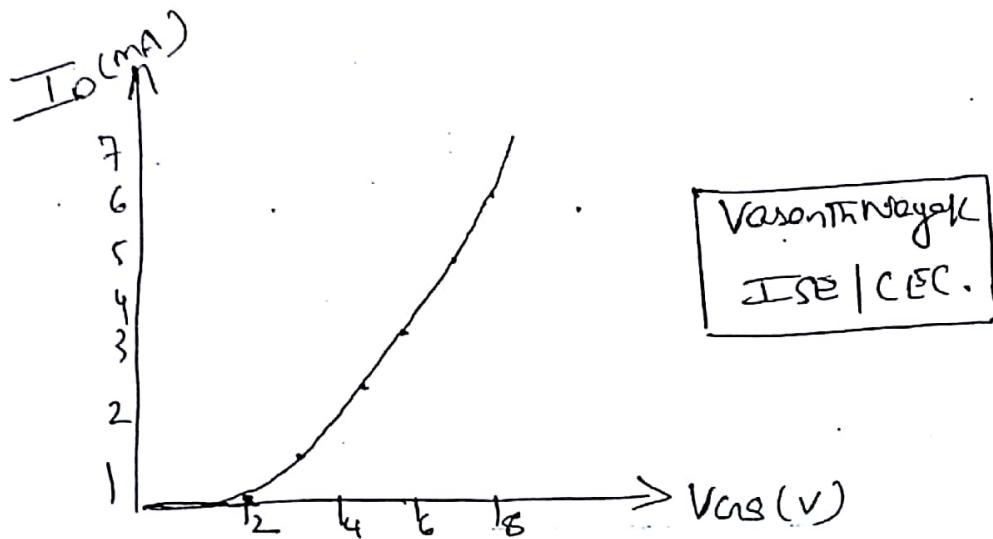


For voltages greater than the threshold voltage, the drain current is given by

$$I_D = k (V_{GS} - V_T)^2$$

(7)

Where  $K$  is a constant.



Transfer characteristic of an N Channel  
E-MOSFET

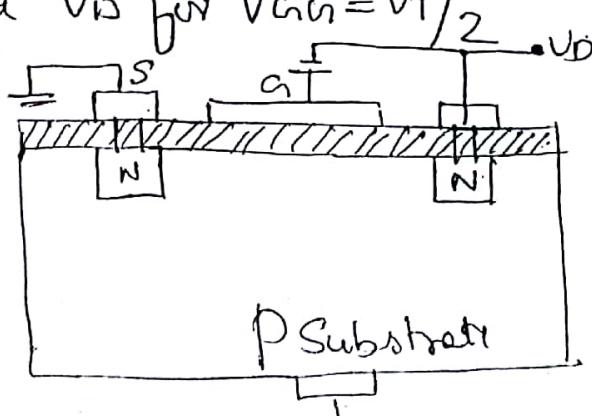
Prob: Identify the MOSFET shown in the figure,

Given that  $V_T$  is the Threshold Voltage of the MOSFET.  $I_{Dg}$  is the drain current of the MOSFET when the gate source voltage is equal to twice the threshold voltage.

(a) Draw the o/p characteristics

(b) An external supply  $V_{DS}$  is applied between the gate and the drain terminals

(c) Draw the curve between the drain current and voltage  $V_D$  for  $V_{GS} = V_T/2$



(1) The Mosfet shown is N channel E-MosFET

We know E-MOSFET conducts for  $V_{DS}$  greater than the Threshold Voltage ( $V_T$ )

The Current is  $I_D = k (V_{DS} - V_T)^2$

But According to given  $I_{DS}$  is the Current for

$$V_{DS} = 2V_T \quad \text{So } k = \frac{I_{DS}}{\frac{V^2}{V_T}}$$

(2) The O/p characteristics can be plotted using

$$I_D = \frac{I_{DS}}{V_T^2} (V_{DS} - V_T)^2$$

$$V_{DS(\text{sat})} = V_{DS} - V_T$$

As an example Consider

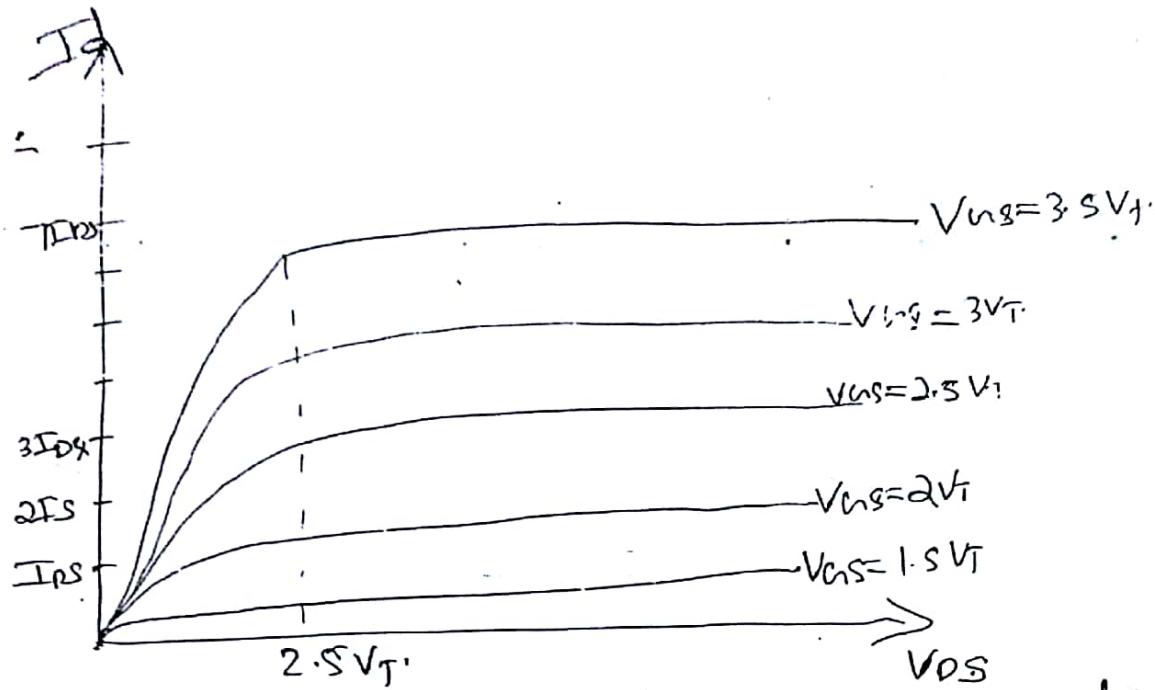
$$V_{DS} = 3.5V_T$$

$$I_D = 6.25 I_{DS} \quad \text{and} \quad V_{DS(\text{sat})} = 2.5V_T$$

By calculating the values of  $I_D$  for different values of  $V_{DS}$  we can plot the O/p characteristics.

$V_D$	$V_{DS}$	$V_{DS}$	$I_D$
0	0	0.5V <sub>T</sub>	0
6.25V <sub>T</sub>	0.5V <sub>T</sub>	V <sub>T</sub>	0
V <sub>T</sub>	V <sub>T</sub>	1.5V <sub>T</sub>	0.25I <sub>DS</sub>
1.5V <sub>T</sub>	1.5V <sub>T</sub>	2V <sub>T</sub>	I <sub>DS</sub>
2V <sub>T</sub>	2V <sub>T</sub>	2.5V <sub>T</sub>	2.25I <sub>DS</sub>
2.5V <sub>T</sub>	2.5V <sub>T</sub>	3V <sub>T</sub>	4I <sub>D</sub>
3V <sub>T</sub>	3V <sub>T</sub>	3.5V <sub>T</sub>	6.25I <sub>DS</sub>

(8)



- (3) The voltage  $V_{DS}$  is applied between the gate and the drain terminals. So.

$$V_{DS} = V_{GATE} + V_{DS} = V_{GATE} + V_D$$

- (4) As  $V_{GATE} = V_T / 2$   
when  $V_D = V_T / 2$   $V_{DS} = V_T$  the Mosfet starts conducting

## Difference between JFETs and MOSFETs

(1) JFETs are operated in depletion mode only  
Whereas

DE-MOSFETs can be operated in both depletion and enhancement modes and E-MOSFETs are operated in enhancement mode only

(2) Input resistance offered by MOSFETs is much higher than JFETs. Input resistance for JFETs is greater than  $10^9 \Omega$  whereas that of MOSFETs is around  $10^{13} \Omega$ .

(3) JFETs have higher drain resistances than MOSFETs and characteristic curve is more flat than MOSFET. Drain resistance for JFETs is in the range of 100k $\Omega$  to 1M $\Omega$  while that for MOSFET is in the range of 1 to 50k $\Omega$ .

(4)漏电流 in MOSFET is much smaller than that in JFETs

For MOSFET ( $100\text{aA}$  to  $10\text{nA}$ )

Whereas

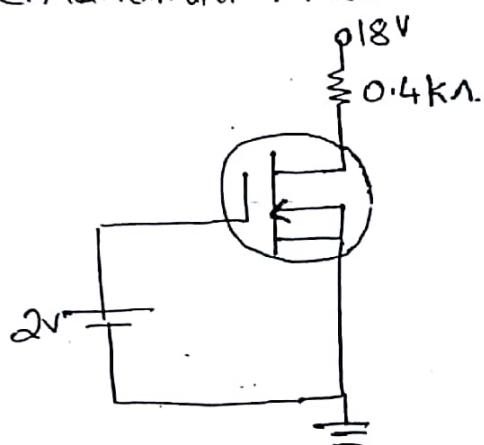
For JFETs ( $10\mu\text{A}$  to  $1\text{mA}$ )

(5) MOSFETs are easier to construct and used more widely than JFETs.

## Biasing MOSFETs

Biasing Schemes for DE-MOSFETs are the same as that for JFET with exception that DE-MOSFETs operate in the enhancement mode.

Problem:



Given Saturation drain current is 8 mA and pinch off voltage is -2V

- determine the value of gate source voltage
- drain current and drain source voltage.

①  $V_{G:S} = 2V$

(2) polarity of the voltage applied between the gate and the source terminals is such that the MOSFET operates in the enhancement region. of its I/V characteristics

(3) In a DE-MOSFET

$$I_D = I_{DSS} \left( 1 - \frac{V_{GS}}{V_P} \right)^2$$

$$I_{DSS} = 8mA \quad V_{GS} = 2V \quad V_P = -2V$$

$$\text{So } I_D = 8 \times 10^{-3} \times \left[ 1 - \frac{2}{(-2)} \right]^2 = 32mA$$

(9)

(4) Applying Kirchhoff's Voltage Law to the opposition

$$18 - 0.4 \times 10^3 \times 32 \times 10^{-3} - V_{DS} = 0$$

$$V_{DS} = 18 - 12.8 = 5.2V$$

Problem:

Design a voltage divider bias network using a BE-MOSFET with supply voltage  $V_{DD} = 16V$

$I_{DSS} = 10mA$   $V_p = -5V$  to have quiescent drain current of  $5mA$  and gate voltage of  $4V$ .

(Assume drain resistor  $R_D$  to be 4 times the source resistor  $R_S$ )

(1) As the quiescent drain current is less than saturation drain current. The MOSFET is operating in the depletion mode.

(2) The drain current ( $I_D$ ) is given by

$$I_D = I_{DSS} \left( 1 - \frac{V_{GS}}{V_p} \right)^2$$

$$5 \times 10^{-3} = 10 \times 10^{-3} \left[ 1 - \frac{V_{GS}}{(-5)} \right]^2$$

$$0.5 = \left( 1 + \frac{V_{GS}}{5} \right)^2$$

$$V_{GS} = -1.5V$$

③ gate - source voltage ( $V_{GS}$ ) is given by

$$V_{GS} = V_G - V_S = V_G - I_D R_S$$

④  $I_D \times R_S = 4 + 1.5 = 5.5 \text{ V}$

⑤  $R_S = 5.5 / 5 \times 10^{-3} = 1.1 \text{ k}\Omega$

⑥  $R_D = 4 \times R_S = 4.4 \text{ k}\Omega$

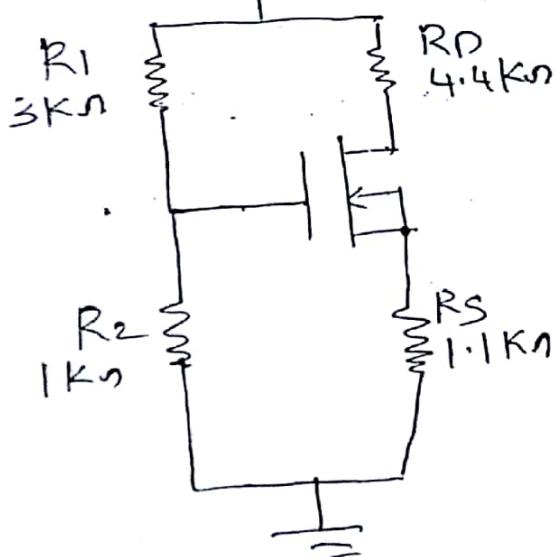
⑦  $V_{OL} = \left[ \frac{R_2}{(R_1 + R_2)} \right] \times 16$

⑧ Let us assume  $R_2 = 1 \text{ k}\Omega$ .

$$I = \frac{16 \times 1 \times 10^3}{(R_1 + 1 \times 10^3)}$$

$$R_1 = 3 \text{ k}\Omega$$

$\because V_{OP} = 16 \text{ V}$



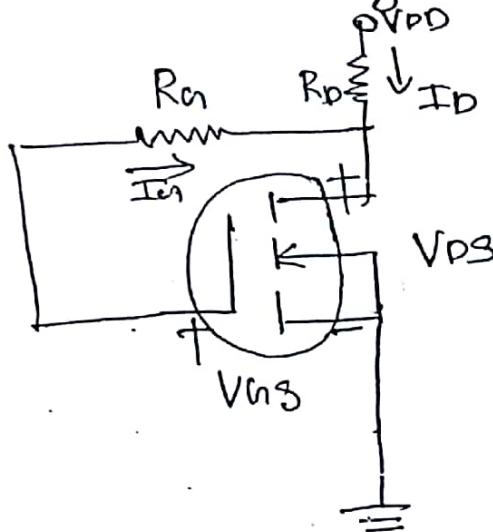
# Biasing Enhancement MOSFETs

---

Two Configuration

(1) feed back biasing

(2) Voltage divider configuration



\* Resistor  $R_s$  provides feedback connection which provides a bias voltage to turn on.

\* Since gate current  $I_{GS}$  is approximately equal to zero. So voltage drop across  $R_s$  is 0

$$V_{DD} - I_D R_D - V_{GS} = 0 \quad V_{GS} = V_{DD} - I_D R_D \rightarrow (1)$$

$$\text{So } V_{GS} = V_{DD} - I_D R_D$$

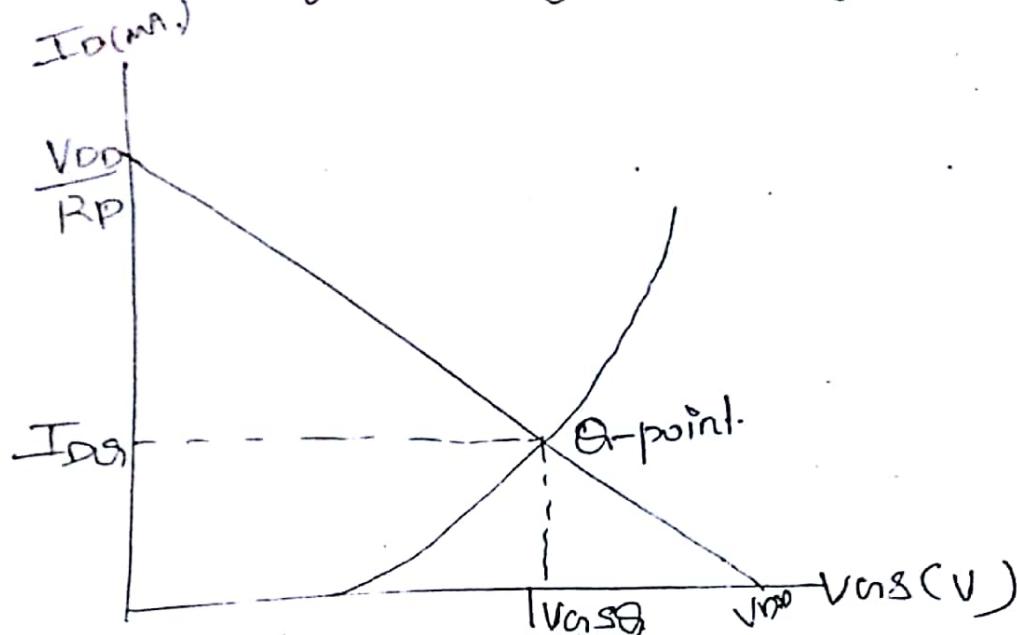
\* From above equation  $V_{GS} = V_{PS}$

② Applying Kirchhoff's Voltage Law to output section

$$V_{PS} = V_{DD} - I_D R_D \rightarrow (2)$$

$$\text{* So } V_{GS} = V_{PS}$$

graphical method for determining operating point.

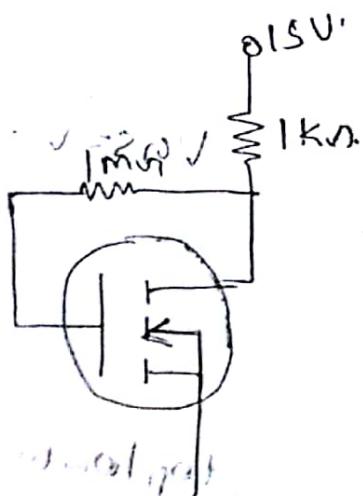


Here Straight line is obtained from

$$V_{DS} = V_{DD} - I_D R_P$$

- \* The point of intersection between the straight line and the transfer curve gives the value of the quiescent gate source voltage, and quiescent drain current.

Problem :



Determine the value of  
Operating point.

NMOSFET — Threshold Voltage is 2V

$$I_D(\text{on}) = 6 \text{mA} \text{ for } V_{DS(\text{on})} = 5 \text{V}$$

(1) Drain current

$$I_D = k(V_{DS} - V_T)^2$$

$$(2) \text{ So } k = 6 \times 10^{-3} / (5-2)^2 = 0.67 \text{ mA/V.}$$

(3) Gate source Voltage in the feedback config is given by

$$V_{GS} = V_{DD} - I_D R_D$$

$$\begin{aligned} V_{GS} &= 15 - I_D \times 1 \times 10^3 \\ &= 15 - 1000 I_D \end{aligned}$$

(4) Substituting this value of  $I_D$

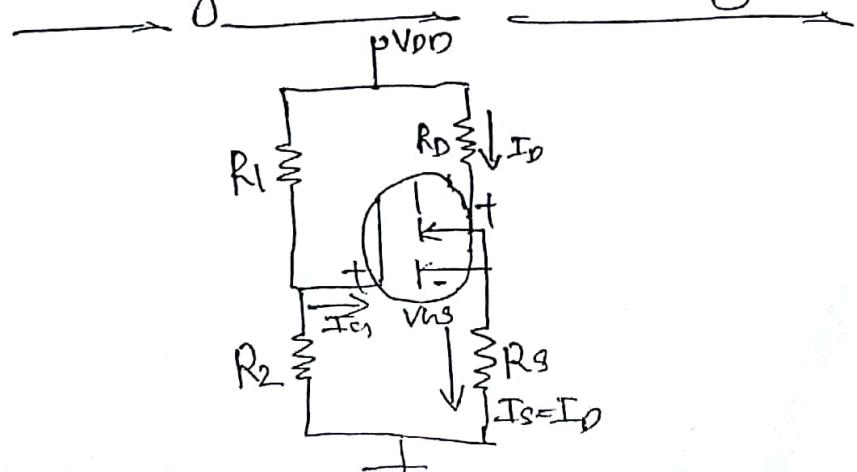
$$I_D = 0.67 \times 10^{-3} (15 - 1000 I_D - 2)^2$$

$$I_D = 9.3 \text{ mA.}$$

$$(5) V_{GS} = V_{DD} - I_D R_D$$

$$\begin{aligned} V_{GS} &= 15 - 9.3 \times 10^{-3} \times 1 \times 10^3 \\ &= \underline{\underline{5.7 \text{ V}}} \text{ (operating point)} \end{aligned}$$

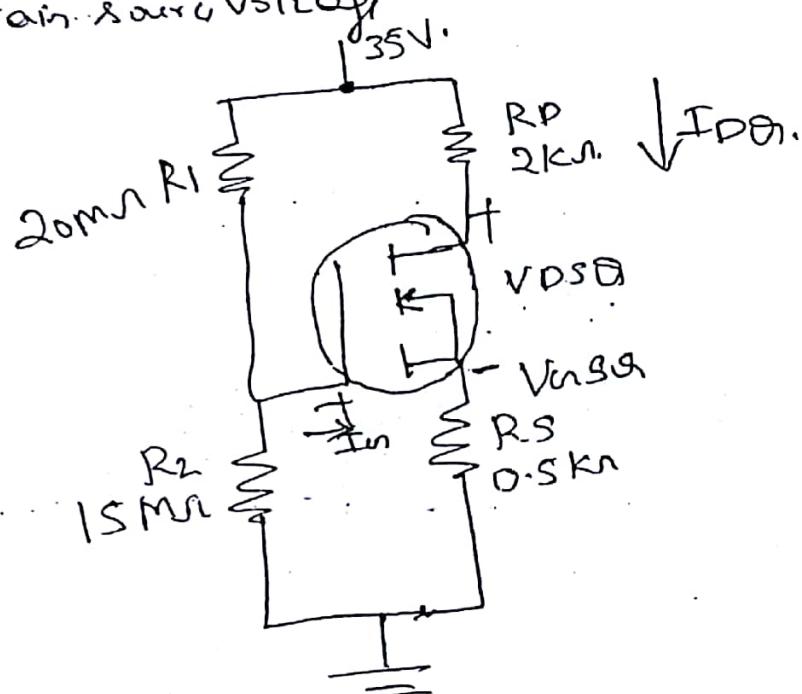
Voltage divider Biasing Configuration



\* Voltage divider Configuration is another popular biasing arrangement with E-MOSFETs

problem: Shows voltage divider configuration for NMOS E-MOSFET given that  $T_h$  threshold voltage  $4V$ , the MOSFET is  $4V$ . and the value of  $I_{D(on)} = 6mA$ . for  $V_{DS(on)} = 8V$ .

use graphical method to determine the value of the quiescent drain current, gate-source voltage and drain-source voltage.



① Transfer characteristics of the MOSFET can be plotted by finding the value of  $k_A$  as

$$k_A = \frac{I_{D(on)}}{(V_{DS(on)} - V_{GS(on)})^2}$$

②  $I_{D(on)} = 6mA$      $V_{DS(on)} = 8V$      $V_{GS(on)} = 4V$ .  
So  $k_A = 6.375 \times 10^{-3} A/V^2$

(T2)

③

$$I_D = 0.375 \times 10^{-3} (V_{DS} - V_{DS(on)})^2$$

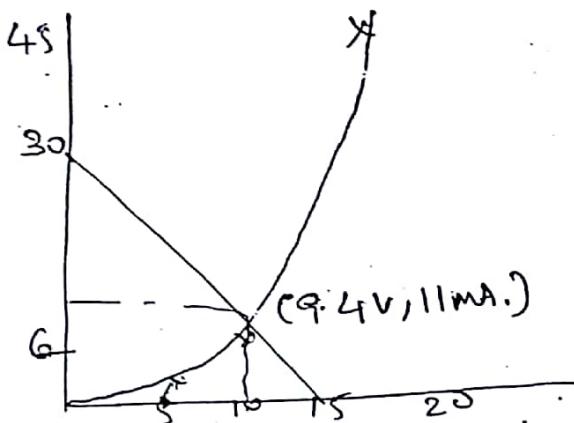
④

For  $V_{DS} = 5V$   $I_D = 0.375$  for  $V_{DS} = 7.5V$ .

$$I_D = 4.59mA \quad V_{DS} = 10V \quad I_D = 13.5mA$$

$$\text{for } V_{DS} = 12.5V \quad I_D = 27.09mA$$

$$\text{for } V_{DS} = 15V \quad I_D = 45.375$$



⑤ To draw load line

$$V_L = \frac{R_2 \times V_{DD}}{R_1 + R_2}$$

$$V_L = 15 \times 10^6 \times 35 / (20 \times 10^6 + 15 \times 10^6) = 15V$$

⑥

$$V_{DS} = V_L - V_S = V_L - I_D R_S$$

$$\text{for } I_D = 0 \quad V_{DS} = 15V$$

$$\text{for } V_{DS} = 0 \quad I_D = 15 / 6.5 \times 10^3 = 30mA$$

(7) Draw the load line with coordinates  $(0, 15V)$  and  $(30mA, 0)$

(8) So quiscent values of gate source voltage and drain current is  $9.4V$  and  $11mA$ .

# FET Applications

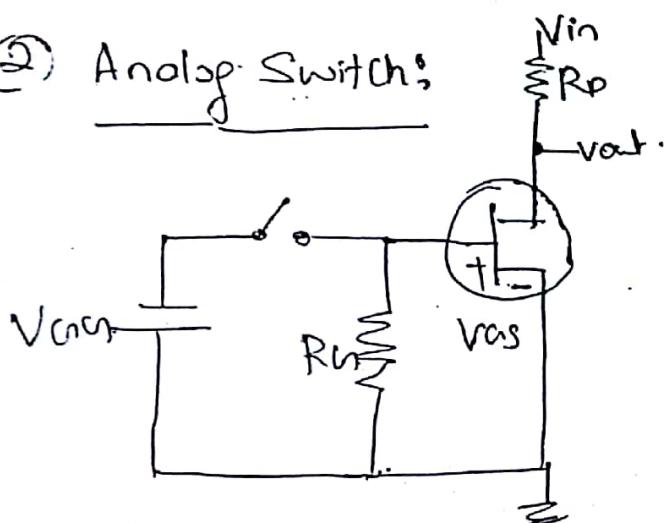
## (1) Amplifier.

Used as low noise amplifier and as buffer amplifier.

FET are low noise transistors in the front end receiver.

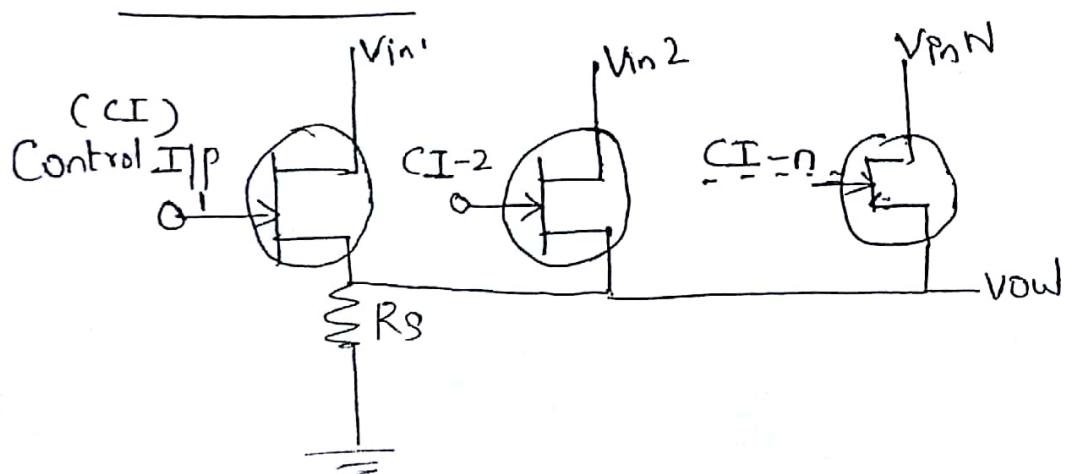
Because of high IIP impedance and low OIP impedance.  
They are used as buffer amplifier.

## (2) Analog Switch:



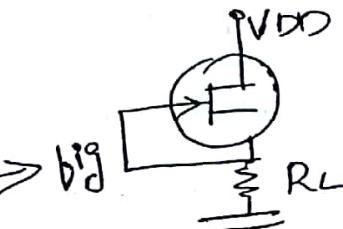
When no gate voltage applied FET operates in the saturation region acts as closed switch when  $V_{ctrl} < 0$  it act like open switch.

## (3) Multiplexer:



- \* I/p Signals are applied to the drain terminals of FET. When Control I/p corresponding to one of the I/p channels is made zero. That I/p is transmitted to o/p

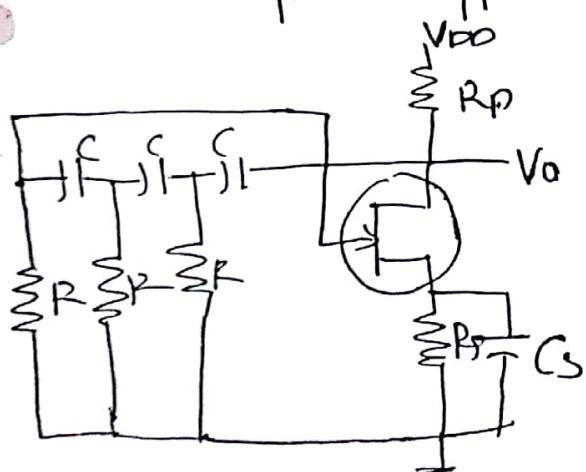
#### (4) Current limiters:



- \* Can be used as in current limiting application
- \* During normal operation it operates in the ohmic region
- \* When load current increases it operates in the saturation region

#### (5) Voltage Variable Resistor: FET when operated in the ohmic region acts as Voltage Variable Resistor.

#### (6) Oscillators: can be used as phase shift oscillator and pierce type of oscillator.



Vasantha Nayak  
ISE | CBC.

END of part 1

- \* MultiVibrator is a oscillator which oscillates between High state and low state producing a continuous output
- \* A stable MV that has no stable states but switches continuously between two states has a duty cycle of 50%. produces square wave at fixed frequency
- \* Monostable A one shot multiVibrator that has only one stable state oscillates triggered externally
- \* Bistable has two stable states

# Integrated circuit MultiVibrator

(APB-modul 1 - part 2.)

## Digital IC based Monostable multivibrator.

Inculde 74121 Single monostable multivibrator

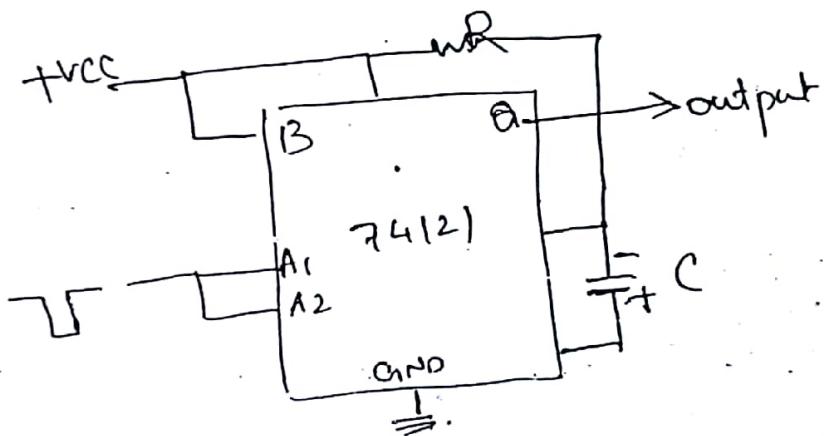
74221 dual monostable multivibrator

74123 (dual retriggerable monostable multivibrator)

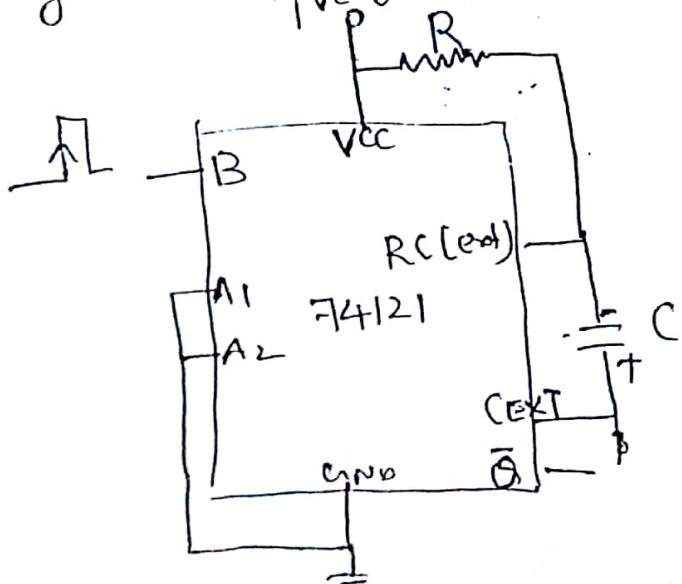
\* Fig shows the use of 74121 as monostable multivibrator

\* it can Low to high or high to low triggered.

\* output pulse width depends on R and C width  
can be computed from  $T = 0.7RC$

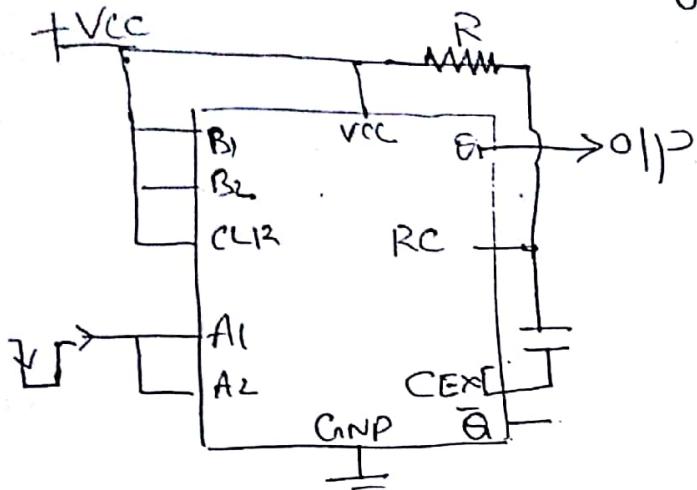


High to Low edge triggering of 74121

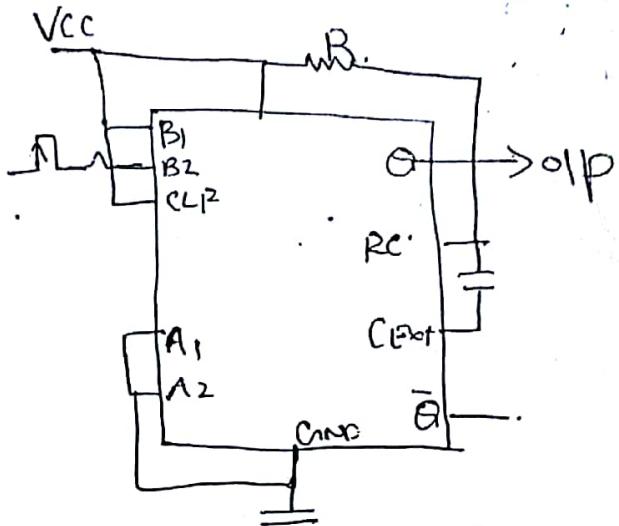


Vasant Nayak  
CEC ISE

74123 a dual Rtriggerable monstable multivibrator



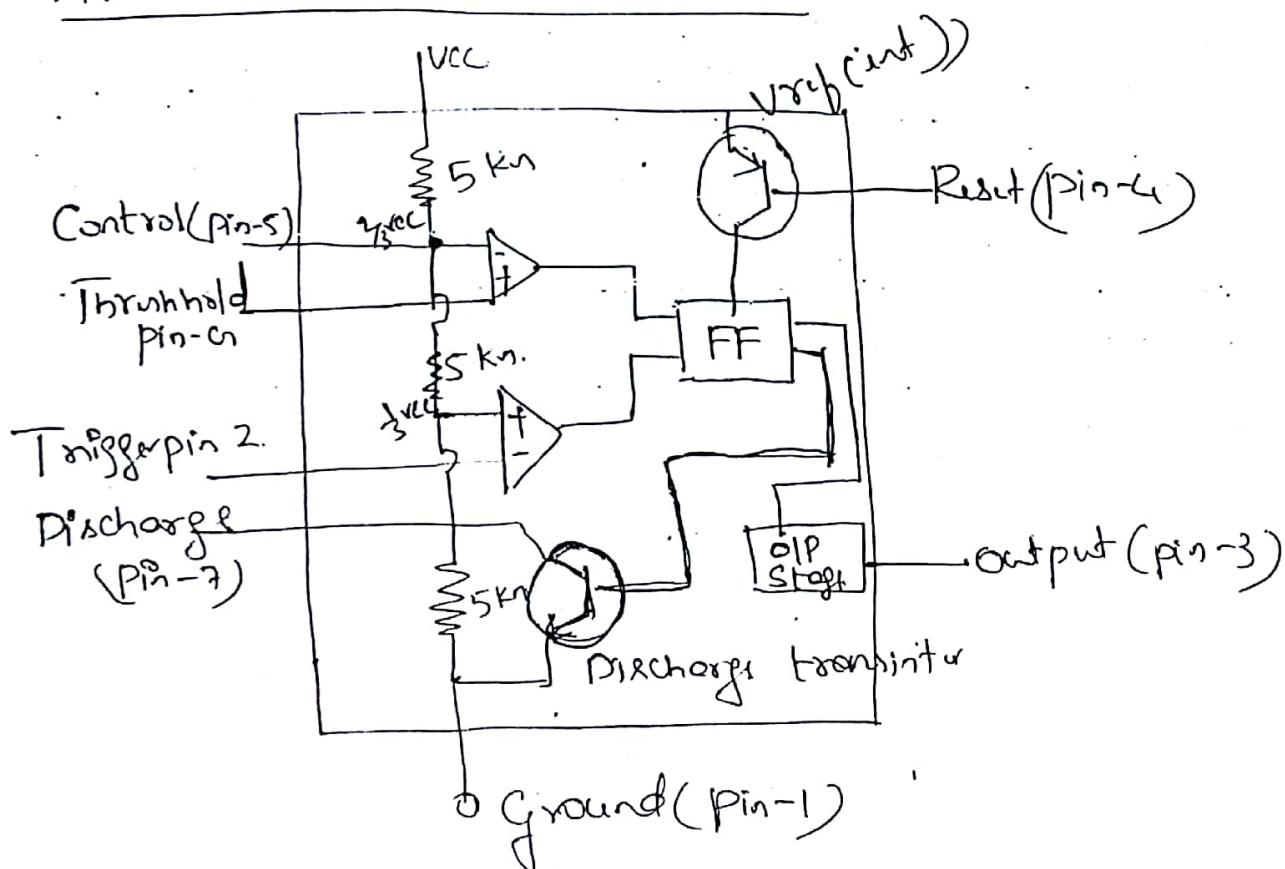
High to Low



Low to High

OIP pulse width depends on  $T = 0.28 RC \times (1 + 0.27/RC)$   
for  $C > 1000 \text{ pF}$   $R$  is  $> 5.50 \text{ k}\Omega$

### Time based multivibrator



(2)

- \* Timer IC 555 can be used to configure monostable and astable multivibrator.
- \* It consists of opamp comparators, a flip flop discharge transistor three identical resistor and op stage
- \* Resistor set Referring voltage for comparator as  $V_{CC}/3$  and  $\frac{2V_{CC}}{3}$  as shown in the figure.
- \* Op of 2 comparators feed SET and RESET input of the flip flop and so final op
- \* Flip flops complimentary op feeds the op stage and the base of the discharge transistor
- \* Thus ensures that when the op is High discharge transistor is OFF otherwise ON.

### Astable Multivibrator

---

- \* Fig shows 555 timer as astable multivibrator
- \* initially capacitor C is fully discharged which forces op to go to the High state
- \* Discharge transistor off allows capacitor C to charge from  $V_{CC}$  through  $R_1$  &  $R_2$
- \* When voltage across C exceeds  $+2V_{CC}/3$  the op goes to Low state and transistor is switched ON.

\* Capacitor begins to discharge through  $R_2$  when it falls below  $+V_{CC}/3$ . The O/P goes back to high state.

High state time period

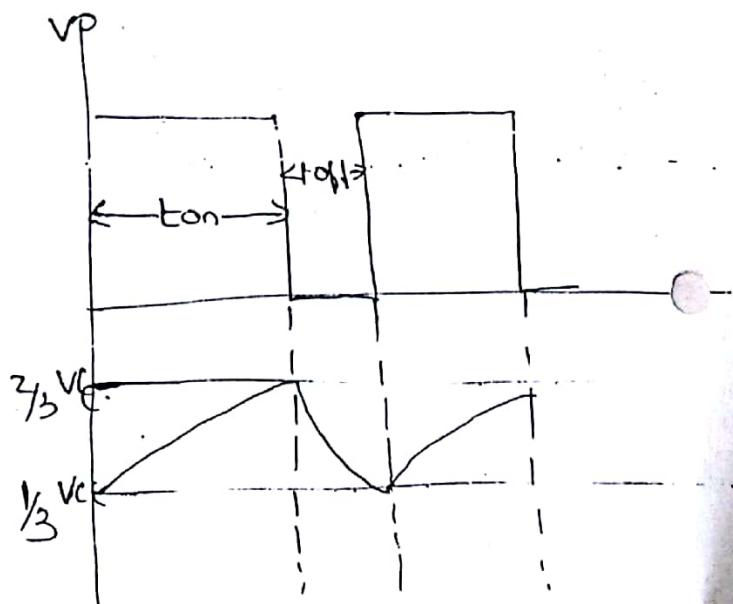
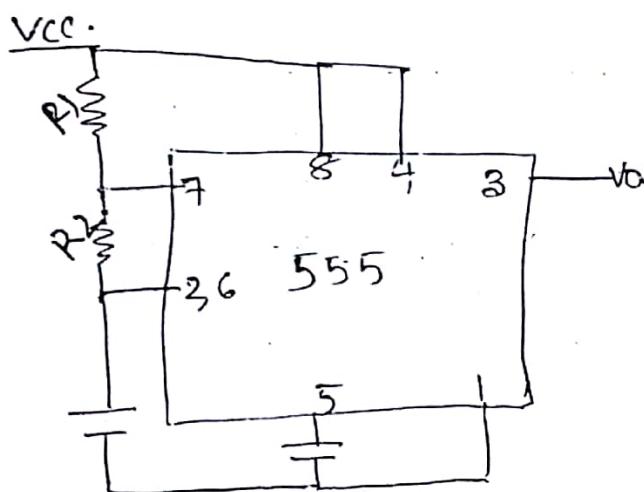
$$T_{High} = 0.69 \times (R_1 + R_2) \times C$$

Low state time period

$$T_{Low} = 0.69 \times R_2 \times C$$

Total time period  $T = 0.69 \times (R_1 + 2R_2) \times C$

Frequency  $f = \frac{1}{0.69 \times (R_1 + 2R_2) \times C}$

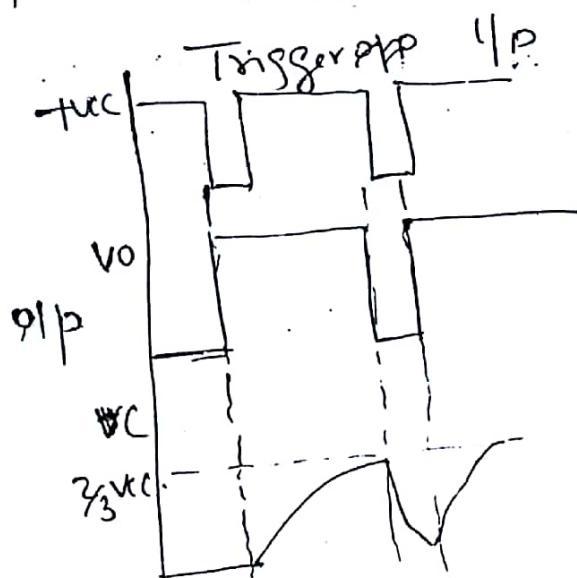
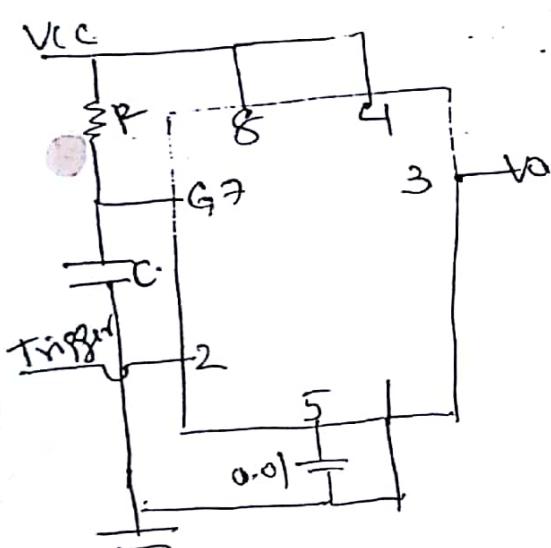


## Monostable multivibrator using timer IC 555

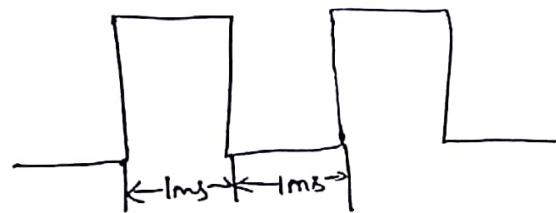
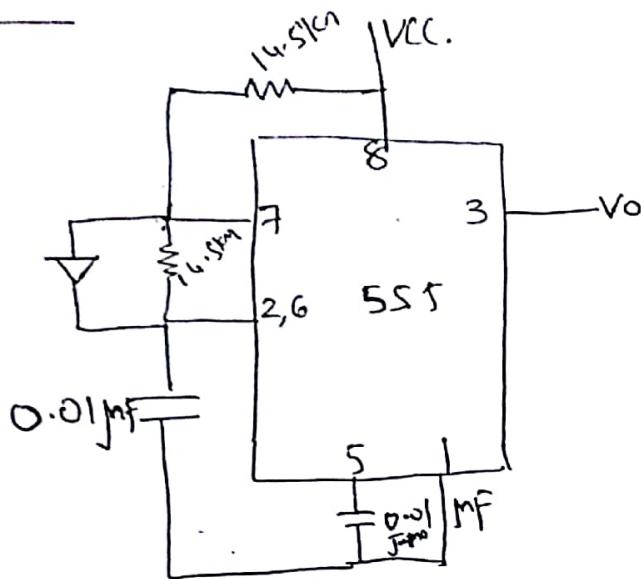
(3)

- \* Fig Shows the basic configuration of monostable multivibrator
- \* It is also referred as monoshot.
- \* Trigger pulse applied to the Terminal 2 of IC.
- \* High at terminal 2 forces the output to low state.
- \* High to low trigger pulse at terminal 2 holds it in high state, allows the capacitor to charge from +Vcc when capacitor voltage exceeds  $+2V_{cc}/3$  it goes back to low state.
- \* So time period is

$$T = 1.1 \times R \times C.$$



problem:

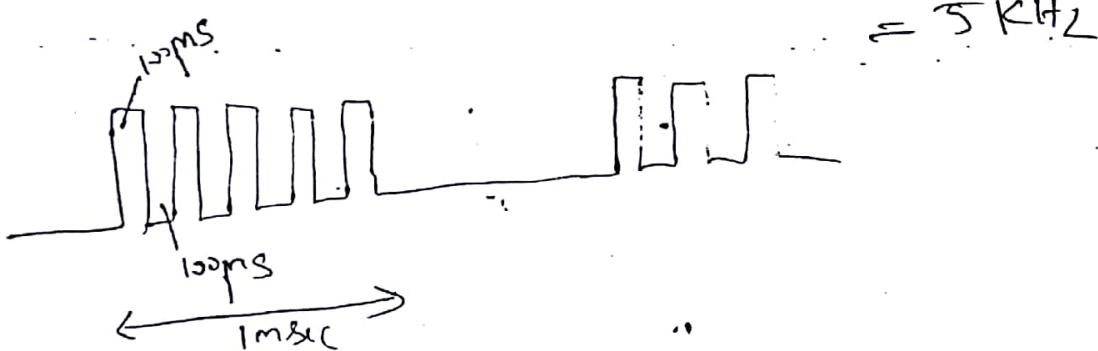


waveform of the fig shown is applied to the RESET terminals of astable multivibrator. Draw o/p waveform

$$\text{Hightime} = 0.69 \times 14.5 \times 10^3 \times 0.01 \times 10^{-6} = 100\mu\text{s}$$

$$\text{Lowtime} = 0.69 \times 14.5 \times 10^3 \times 0.01 \times 10^{-6} = 100\mu\text{s}$$

$$f_{\text{output}} = \frac{1}{T} = \frac{1}{200\mu\text{s}} = 0.005 \times 10^6 \\ = 5 \times 10^3 \\ = 5 \text{ kHz}$$



Extra problem Ref text book

Example 13.16 on page No 542

END OF PART 2

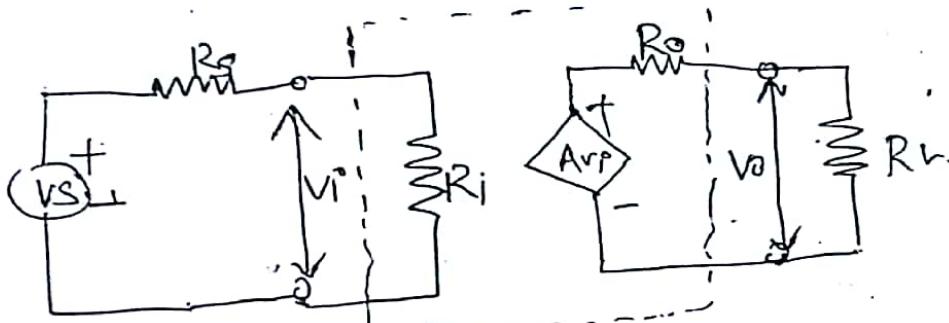
# OPERATIONAL AMPLIFIER

①

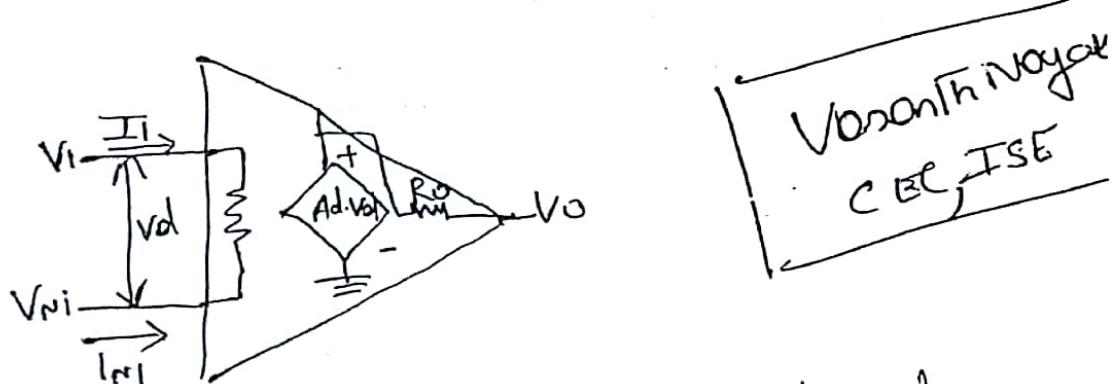
(ADE - module 1 - part 3)

Ideal Versus Practical opamp:

- \* An opamp is a direct-coupled, high gain, high bandwidth differential amplifier with very high value of input impedance and low value of output impedance.



Thevenins equivalent model of a generalized opamp:  
bed at the op from a source with source resistance  
 $R_s$  and the amplified op feeding load resist  
 $R_L$ .



Thevenin's equivalent model of an opamp

where  $Ad$  is open loop gain

ideal opamp makes three assumptions:

- ① Input resistance  $R_i = \infty$       open loop gain  $Ad = \infty$
- ② Output resistance  $R_o = 0$

Here  $R_i = \infty$   $I_o = I_{ni} = 0$   
 $R_o = 0$   $V_o = A_d \times V_d$

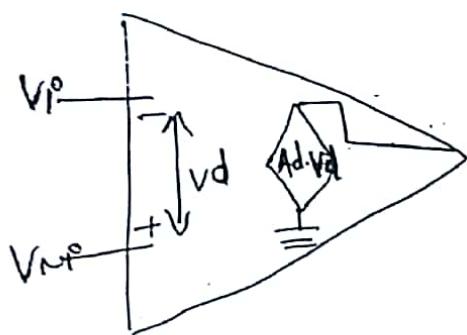
(3) For linear mode of operation of opamp. and infinite o/p voltage and infinite differential gain

$$V_d = 0$$

(4)  $\Rightarrow$  Common mode gain = 0

Since o/p voltage depends on differential input voltage it rejects any voltage common to both inputs so  $\rightarrow$

- \* (S) Bandwidth and slew rate are also infinite.
- (6) DC gain



Thierns equivalent model of Ideal opamp

- \* Infinite open loop differential Voltage gain
- \* Infinite input impedance.
- \* Zero o/p impedance
- \* Infinite bandwidth
- \* Zero DC IIP and o/p offset Voltage
- \* Zero input differential Voltage.

openloop gain is the differential voltage gain in the absence of feed back.

## Performance parameter:

Opamp parameter include following:

1. Bandwidth
2. Slewrate
3. open loop gain
4. Common mode rejection ratio (CMRR)
5. power supply rejection ratio (PSRR)
6. Input impedance
7. OIP impedance
8. Settling time
9. offsets and offset drift

### Bandwidth:

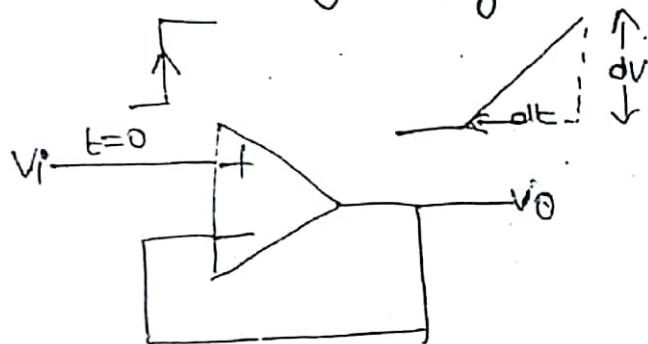
- \* it tells us about the range of frequency it can amplify
- for a given amplifier gain
- \* When opamp is used in the closed loop bandwidth increases with gain
- \* The bandwidth is usually expressed in terms of the unity gain crossover frequency

### Slew rate:

- \* important parameters of opamp
- \* it indicates how well the opamp o/p follows a rapidly changing waveform at its I/P

- \* it is defined as rate of change of o/p voltage with time
- \* it is determined by applying a step input and monitoring the o/p
- \* slew rates of upto  $10V/\mu s$  usually available in general purpose opamps.
- \* slew rate limits the larger signal bandwidth.
- \* peak to peak o/p voltage swing for a sinusoidal signal ( $V_{p2E-p}$ ) slew rate and bandwidth are interrelated by the following equation

$$\text{Bandwidth (highest frequency } f_{\max}) = \frac{\text{Slewrate}}{(\pi \times V_{p2E-p})}$$

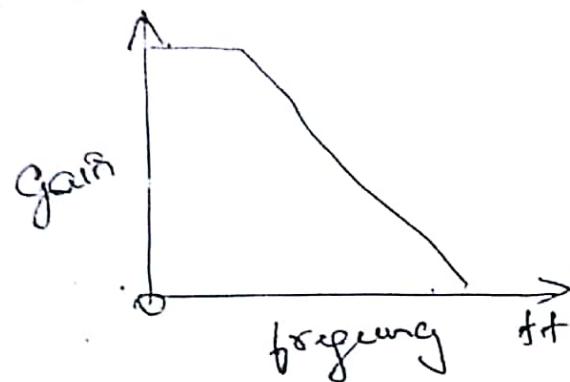


Response to step input.

Open loop gain:

- \* it is the ratio of single-ended o/p to differential i/p
- \* The ratio of the open-loop gain to the closed-loop gain is called the loop gain
- \* Accuracy at any frequency depends on the magnitude of the loop gain
- \* magnitude of the loop gain depends on open-loop gain

(3)



### Common Mode Rejection Ratio:

- Is a measure of the ability of the opamp to suppress common mode.
- \* ratio of the desired differential gain ( $A_d$ ) to the undesired common mode gain ( $A_c$ )
- \* CMRR is given by  $20 \log (A_d/A_c) \text{ dB}$
- \* CMRR is also defined as the ratio of the change in the common mode  $V_{op}$  to the corresponding change in the opamp offset voltage.
- \* Common mode  $V_{op}$  is the average values of the two input voltages.
- \* CMRR specified for a given  $V_{op}$  range.

### POWER SUPPLY REJECTION RATIO

- \* Defined as the ratio of change in power supply voltage to corresponding change in the opamp offset voltage.
- \* PSRR is defined as the ratio of change in one of the power supply voltage to the change in  $V_{op}$  offset voltage with other power supply voltage held constant.

- \* PSRR value falls with increase in frequency.

## Input Impedance:

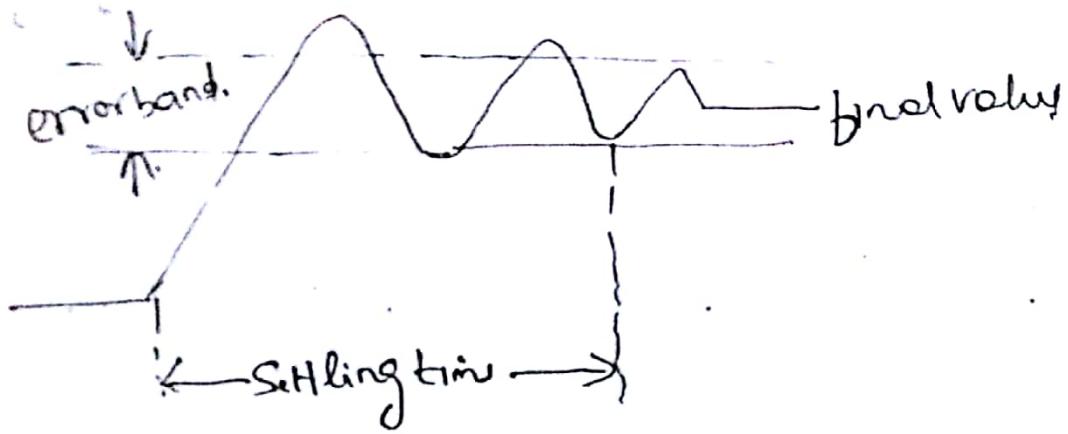
- \* Impedance at the input terminal of the opamp
- \* Expressed in terms of resistance only
- \* In inverting amplifier configuration the effective input impedance equals the input resistance connected externally from source of input signal to the inverting terminal of the opamp.
- \* In the non-inverting amplifier configuration it equals the product of loop gain and the specified opamp input impedance.

## Output impedance:

- \* Defined as the impedance between the output terminal of the opamp and ground.
- \* Output impedance becomes a critical parameter while using rail to rail output opamp

## Settling time:

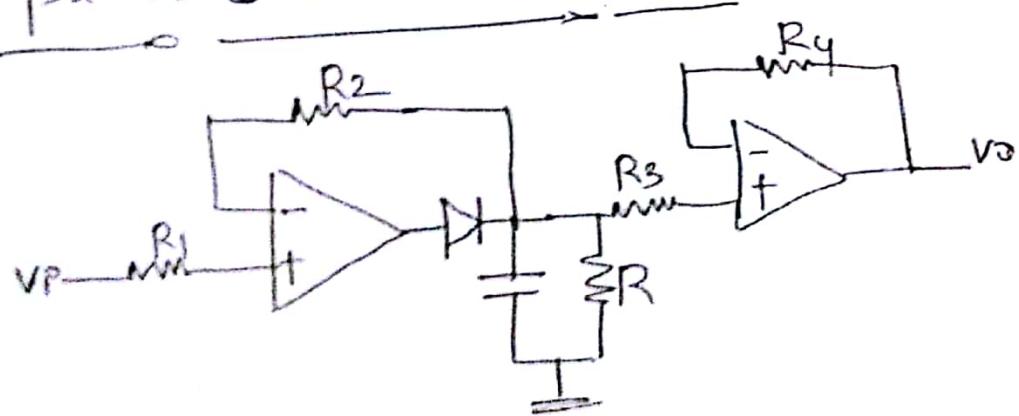
- \* Specified in the case of high speed opamp.
- \* It gives the response of the opamp to large step input.
- \* It is expressed as the time taken by the opamp output to settle within a specified percentage of the



## offsets and offset drifts

- \* Ideal op amp should produce a zero o/p for a zero differential input.
- \* But practically we need to apply a DC differential Voltage externally to get a zero o/p
- \* The externally applied input is referred to as THE input offset Voltage
- \* Output offset Voltage is the Voltage at the o/p with both the input terminals grounded.
- \* Input offset Current is the difference between the two bias currents

## Peak detector circuit :

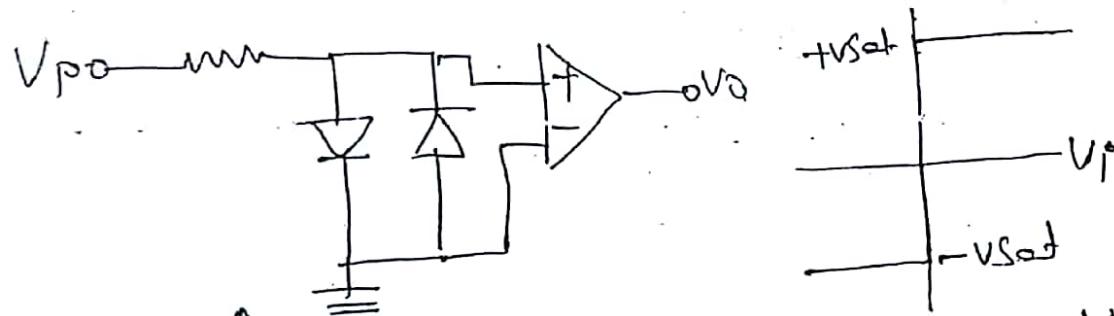


- \* big Shows a positive peak detector circuit.
- \* it is a clipper circuit with  $\parallel$  resistor and capacitor.
- Connect as its opamp
- \* clipper here reproduces the positive half cycles during this period the diode D1 is forward biased and capacitor rapidly charges
- \* After it starts decreasing beyond peak, the diode gets reverse biased thus isolating capacitor from the opamp of the opamp
- \* The capacitor now discharge only through the resistor (R)
- \* The purpose of this resistor is to allow a discharge path.
- \* R-C time constant controls response time
- \* Response time is nothing but the time needed to respond to a decaying peak amplitude of the signal.

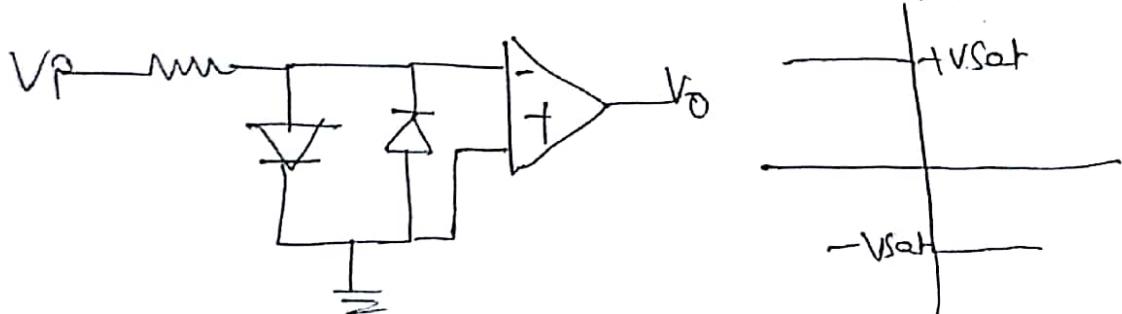
(5)

## Comparators

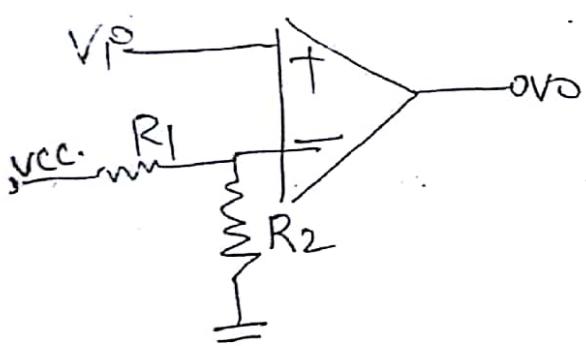
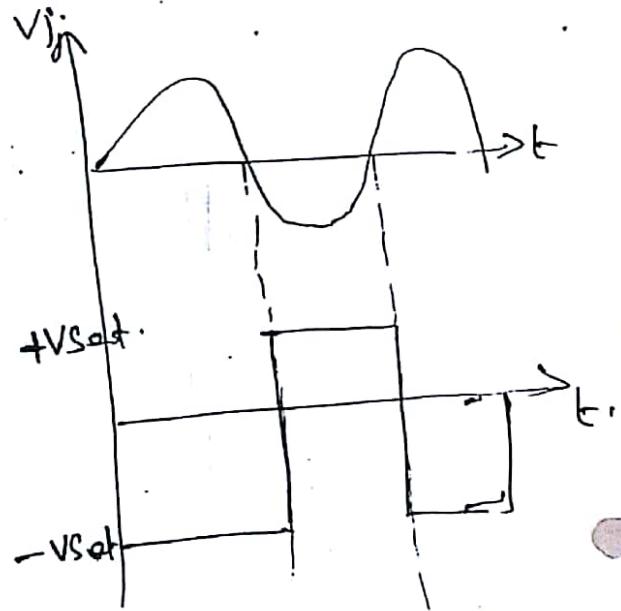
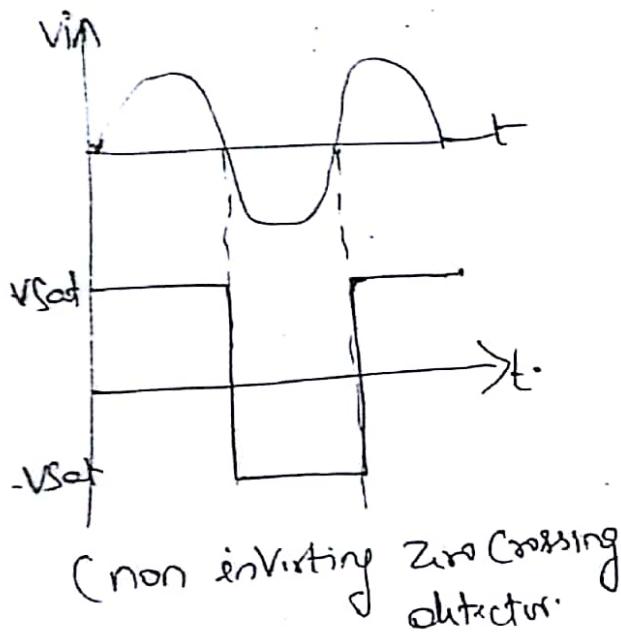
- \* A comparator circuit is a two-input, one Opamp building block that produces a high or low output depending upon the relative magnitudes of the two inputs.
- \* opamp is used here. Because of very large value of open-loop voltage gain it produces either positively or negatively saturated Opamp Voltage.
- \* one input is reference Voltage.
- \* other input is that needs to be compared.



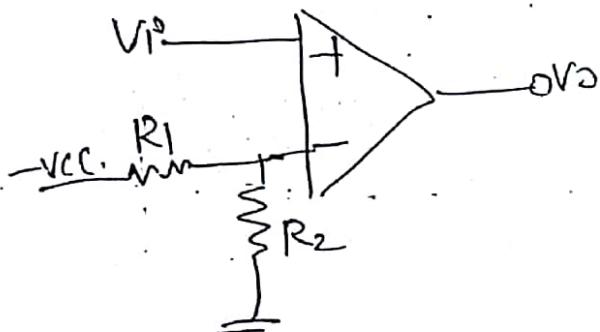
\* it is a <sup>↑</sup> non inverting zero crossing detector because input more positive than zero



\* Above fig Shows inverting inverter.



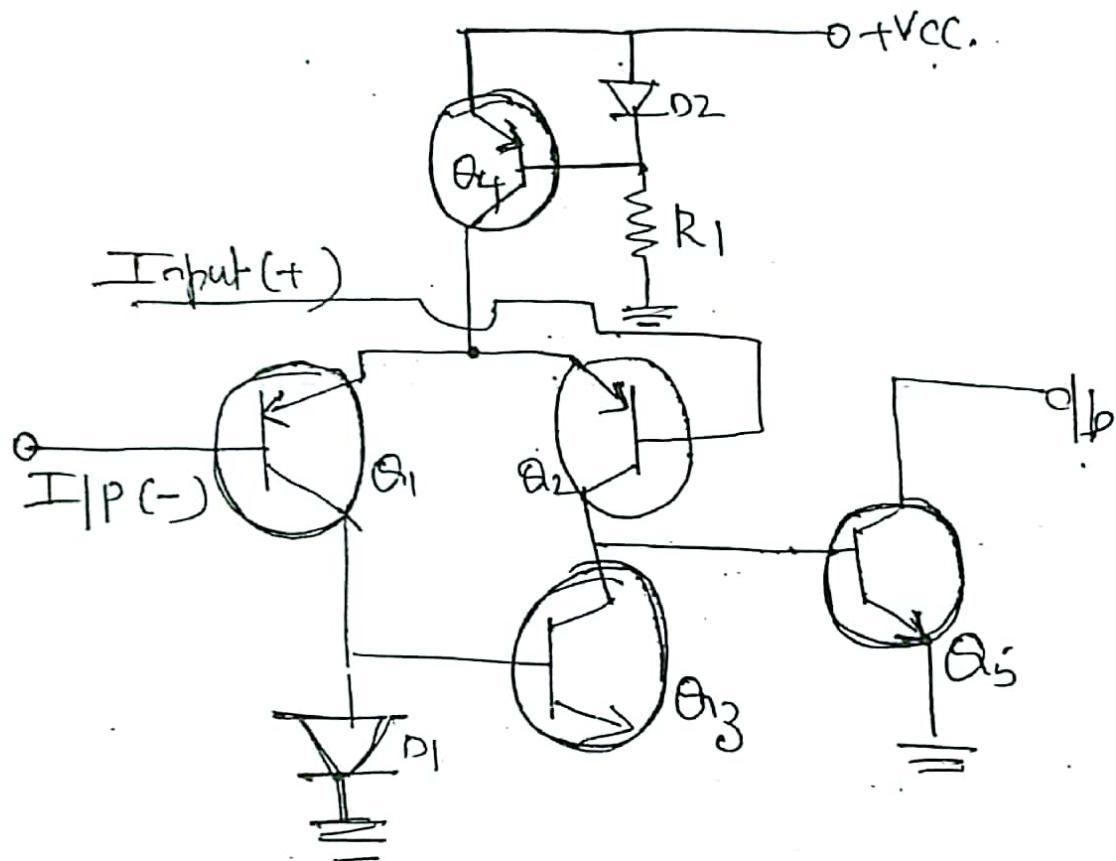
Non inverting comparator  
with positive feedback



Non inverting Comparator  
with negative feedback

(6)

# Basic CKT diagram of opamp comparator



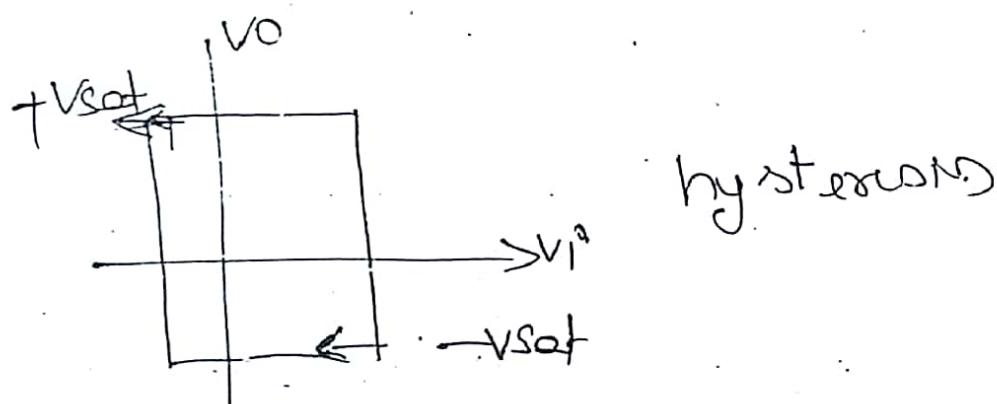
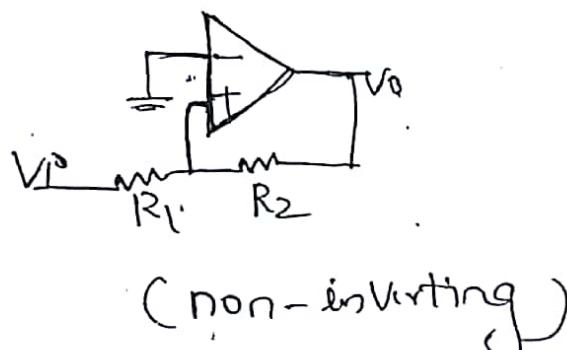
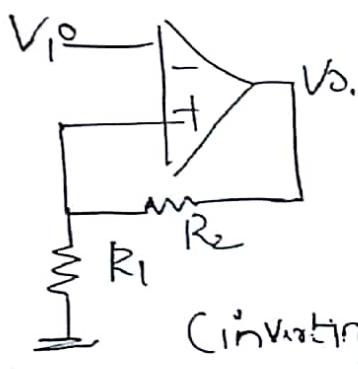
\* Shows THE schematic diagram of opamp Comparator.

\* For the op stage to work properly THE op terminals needs to be connected to THE positive Supply voltage Through An external resistor Called pull-up resistor

\* it is called pull up resistor as it pulls THE op Voltage to THE supply voltage. When THE output transistor Q5 is in cut off state.

## Comparator with hysteresis:

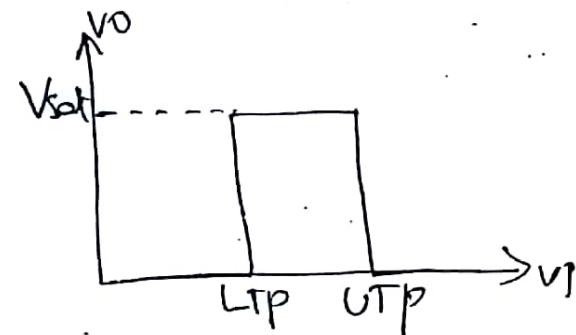
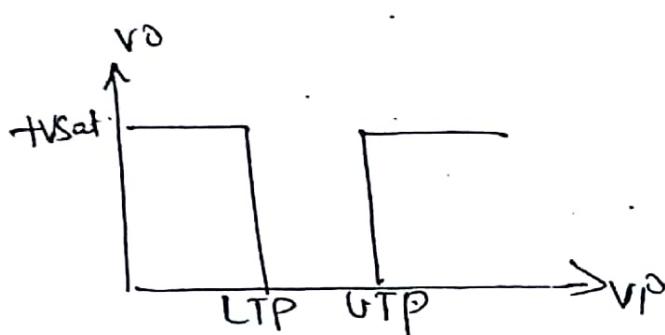
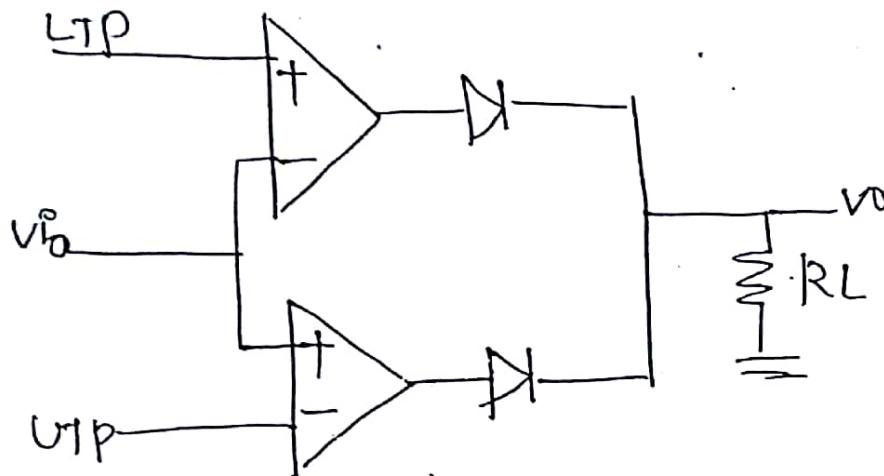
- \* When the op-amp signal applied to the Comparator contains noise, transition at the op-amp becomes highly erratic.



- \* Let us assume op-amp is in positive Saturation ( $+V_{SAT}$ )
- \* Voltage at non-inverting IIP is  $V_{SAT} \times R_1 / (R_1 + R_2)$
- \* Op-amp will stay in positive Saturation
- \* Once the op-amp goes to negative saturation ( $-V_{SAT}$ ) Voltage fed back to non-inverting IIP becomes  $-V_{SAT} \times R_1 / (R_1 + R_2)$
- \* In this manner the circuit offers  $2V_{SAT} \times R_1 / (R_1 + R_2)$

7

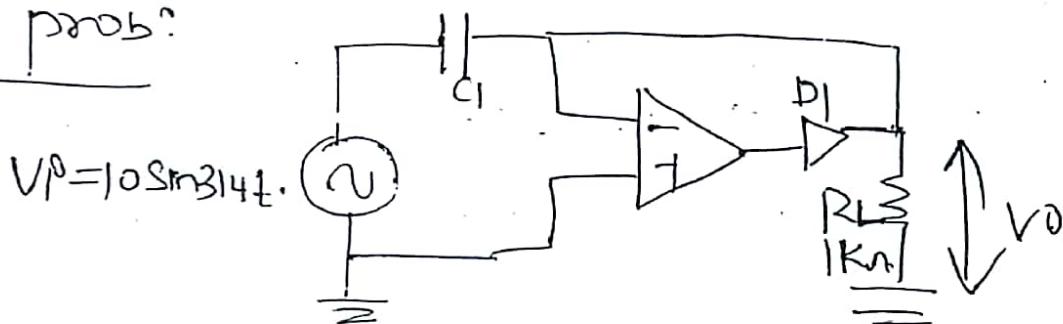
## Window Comparator:



- \* In the case of conventional Comparator, the op-amp changes state when the input voltage goes above or below the preset reference voltage.
- \* In windows Comparator there are two reference voltage, called lower and upper trip points.
- \* Op-amp is in one state when the input is inside the window created by the lower and upper trip points and in other state when it is outside the window.

- \* When the input voltage is less than the voltage reference corresponding to the low trip point (LTP), so o/p of opamp A<sub>1</sub> is at +V<sub>SAT</sub> and that of opamp A<sub>2</sub> is at -V<sub>SAT</sub>
- \* Diodes D<sub>1</sub> & D<sub>2</sub> are forward and reverse biased respectively
- \* When the input voltage is greater than reference voltage corresponding to UTP, the o/p of A<sub>1</sub> is at -V<sub>SAT</sub> and opamp A<sub>2</sub> is at +V<sub>SAT</sub>.
- \* Diodes D<sub>1</sub> and D<sub>2</sub> are reverse and forward biased respectively

Prob:



- \* Determine the peak value of the clamped waveform.
- \* Determine the value of the cap. capacity.

- (1) Peak value of the clamped waveform =  $2 \times 10 = 20V$ . (8)
- (2) Frequency of  $I_{LP}$  =  $314 / 2\pi = 50Hz$ .
- (3) Time period =  $1/50 = 20ms$
- (4) minimum Value of  $C_1$  is  $R_L C_1 = 10T$
- (5)  $C_1(\text{min}) = 1.0T / R_L = 2\mu\text{F}$ .

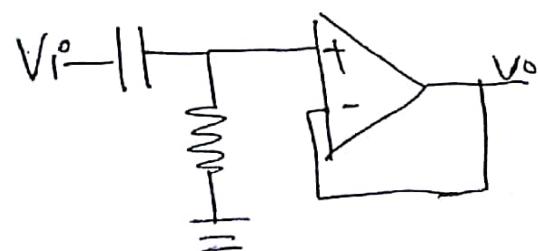
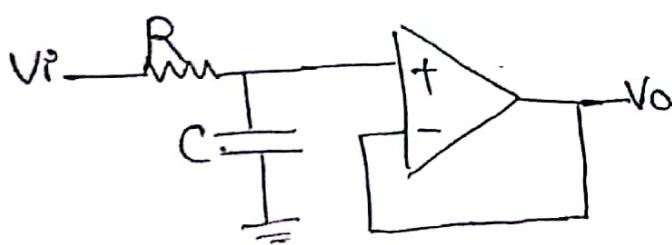
Refer extra problem 677 pages

## Active Filters:

\* order of an active filter is determined by number of R-C Section used in the filter.

### First order filtering

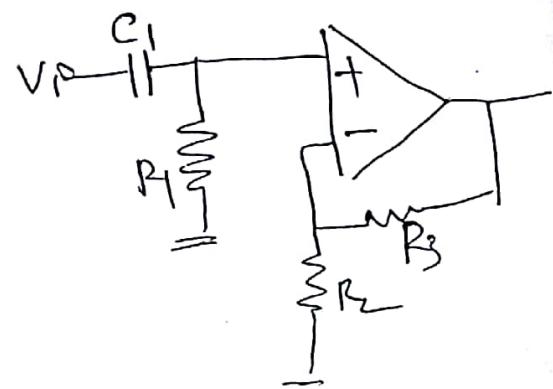
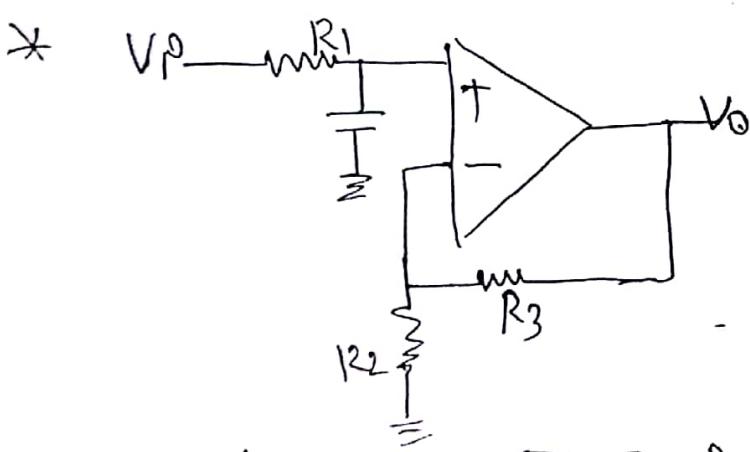
\* Simplest low pass and high pass active filter are constructed by connecting lag and lead type R-C to non inverting IP of opamp.



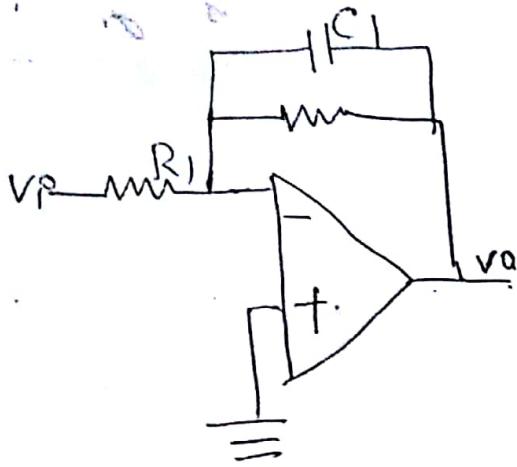
- \* In case of low pass circuit, The reactance offered by the capacitor is much larger than the resistance value, so applied input signal appears at opamp mostly unattenuated.
- \* But in high pass circuit, capacitive reactance is much smaller than the resistance value so opamp to be near zero.
- \* The opamp is 0.707 times ~~less~~ the input when the signal frequency is such as to make the capacitive reactance equal to resistance.
- \* This is called cut-off frequency.
- \* with reference to the above circuit

$$f_c = \frac{1}{2\pi R C}$$

$$A_v = \frac{1 + R_3}{R_2}$$



First order filters with gain (Low pass & High pass)

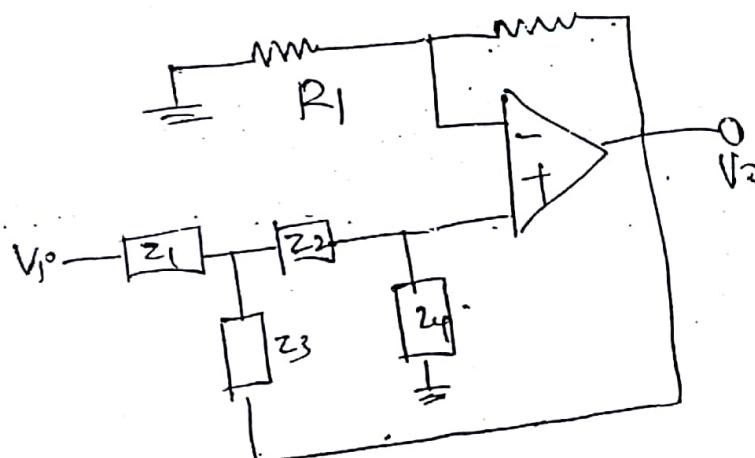


Inverting Configuration

$$\text{So } f_c = \frac{1}{2\pi R_1 C_1}$$

$$A_v = -\frac{R_2}{R_1}$$

Second order filtering: (Butterworth)



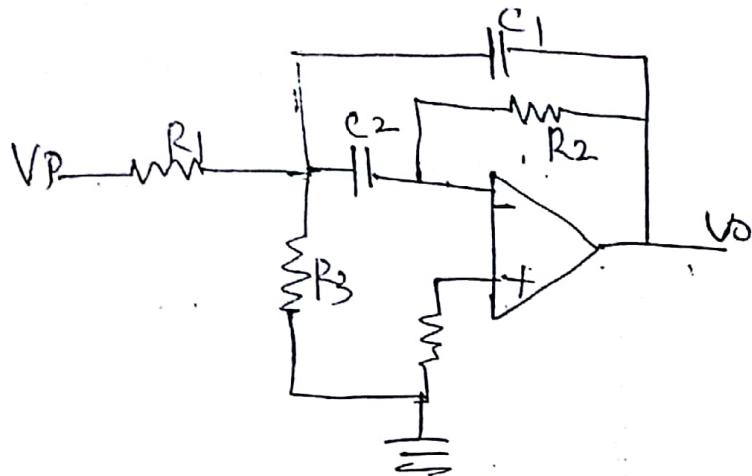
① If  $Z_1 = Z_2 = R$  and  $Z_3 = Z_4 = C$  we get a

second-order low-pass filter

② If  $Z_1 = Z_2 = C$  and  $Z_3 = Z_4 = R$

order high-pass filter

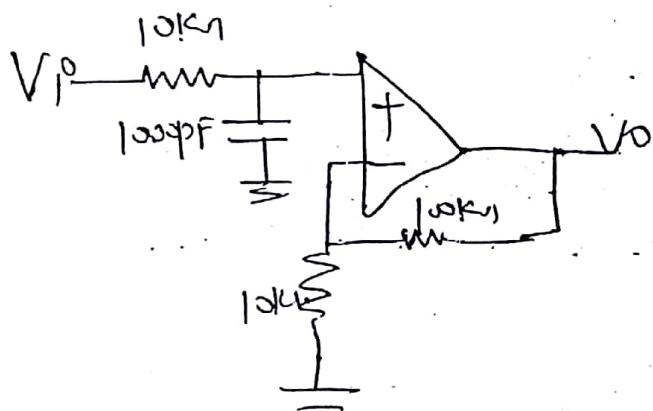
negative second



Narrow band pass filter (2nd order)

problems

Refer to the first order low-pass filter. Determine the cut off frequency and the gain value at four times the cut off frequency.



$$\textcircled{1} \quad f_c(\text{cut off}) = \frac{1}{2\pi \times 10 \times 10^3 \times 1000 \times 10^{-12}} \\ = 15.915 \text{ kHz}$$

$$\textcircled{2} \quad \text{gain } A = \frac{(1 + 100 \times 10^3)}{(10 \times 10^3)} = 2.11 \approx 20.827 \text{ dB}$$

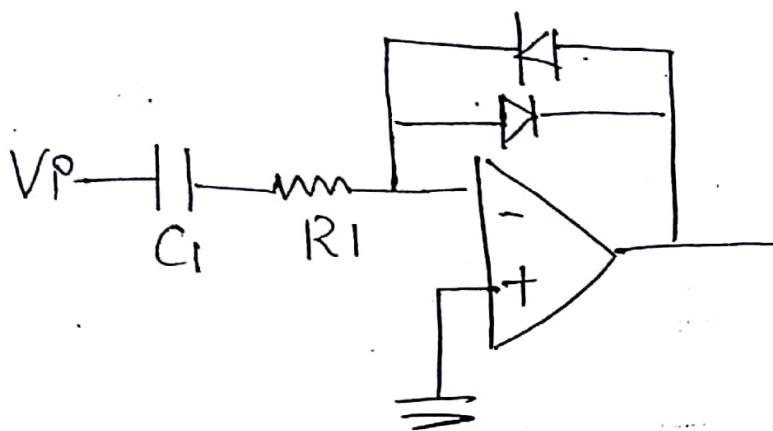
$$\textcircled{3} \quad \text{gain Cut off point} = 20.827 - 3 = 17.827 \text{ dB}$$

$$\textcircled{4} \quad \text{gain at four times the cut off frequency} \\ = 20.827 - 12 = 8.827 \text{ dB}$$

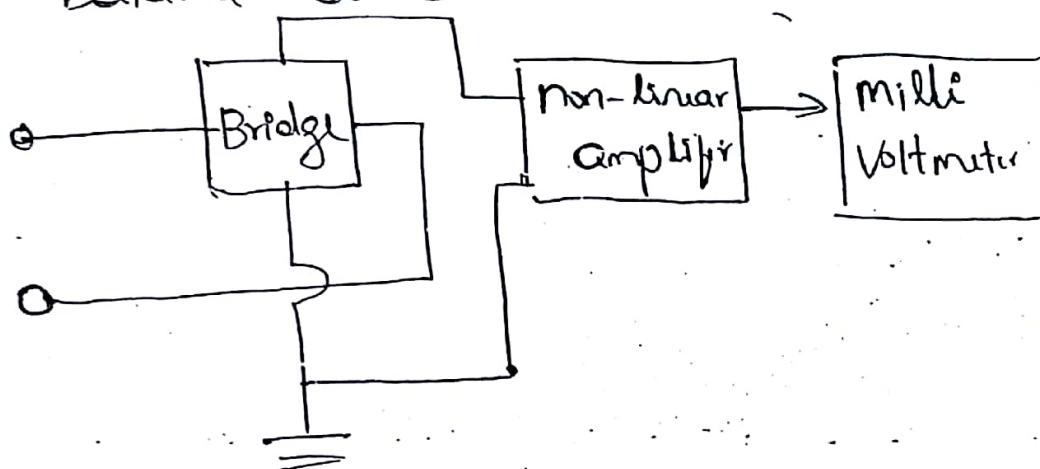
17.18

## Non-linear Amplifier

(10)



Application of Non linear Amplifier in AC bridge  
balance detectors

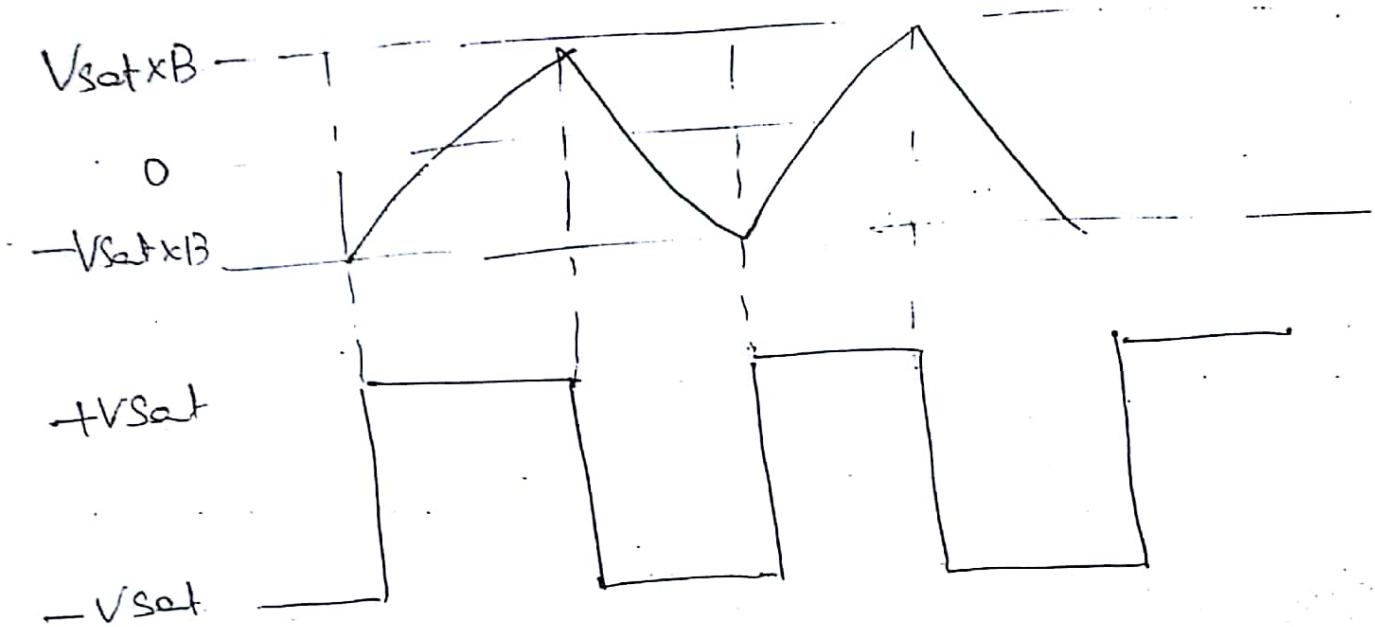
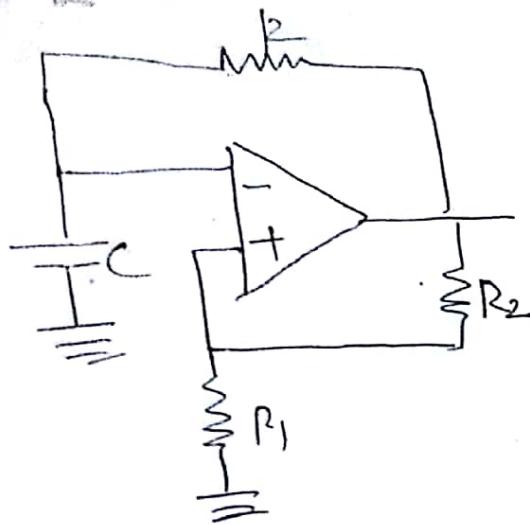


- \* Here gain value is a non-linear function of the amplitude of the signal applied at the IIP.
- \* For example gain may be very large for weak IIP signals and very small for large IIP signals.
- \* That means very large change in the amplitude of IIP signal. Resultant change in the amplitude of OIP signal is very small.

- \* A simple method to obtain non-linear amplification is by connecting a non linear device such as PN junction diode in the feed back path.
- \* for small value of I<sub>IP</sub> Signal diode acts as open circuit and gain is high due to minimum feed back.
- \* for large value of I<sub>IP</sub> Signal diode offers small resistance. Thus gain is low.
- \* Common Application in AC bridge balanced Detectors
- \* The O.P. of bridge may vary over a wide range around its null point.
- \* To obtain null o.p.s given to nonlinear amplifier.
- \* The O.P. of nonlinear amplifier given to millivoltmeter.
- \* Full bridge Version.
- \* for wide range of bridge variation there will be small range of o.p. variation of nonlinear amplifier.

### 7.19 Relaxation oscillator:

CKT that produce a non-sinusoidal o.p. whose time period is dependent on the charging time of a capacitor.



\* The Circuit function as follows:

\* Let us Assume op-amp is in positive saturation

\* As a result Voltage at noninverting terminal is  $+V_{sat} \times R_1 / (R_1 + R_2)$  thus forces op-amp to stay in this state

\* Capacitor C starts charging towards  $+V_s$  at

\* The moment capacitor voltage exceeds the voltage at the non-inverting input the op-amp switches to  $-V_{sat}$ .

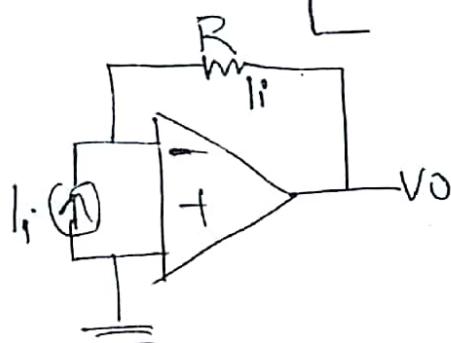
- \* New voltage at non inverting is  $-V_{SAT} \times \frac{R_1}{(R_1 + R_2)}$
- \* Now capacitor discharges towards  $-V_{SAT}$  like this cycle repeats.

### Current Voltage Converter

- \* It is a transimpedance amplifier
- \* Ideally it has zero I/p impedance and zero O/p impedance.
- \* The circuit is characterized by Voltage shunt feedback with feed back factor of unity.

The expression for o/p voltage is

$$V_o = I_i \times R_o \left[ \frac{A_{OL}}{1 + A_{OL}} \right]$$



for  $A_{OL} \gg 1$        $V_o = I_p \times R$

$$Z_{in} = \frac{R}{1 + A_{OL}}$$

$$Z_o = \frac{R_o}{1 + A_{OL}}$$

where  $R$  is  $T_{IN}$   
O/p impedance