

VDF Project Part - II

Group Number - 17

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TOOLS and LIBRARY for Physical Design

1. Physical Design Tool: Innovus (Cadence)
2. Static Timing Analysis Tool: Tempus (Cadence)

Library Used: 90nm Cadence - Slow.lib

Netlist to GDS: The Physical Design Bridge:

Previously, we obtained the netlist, a critical element defining the chip's internal connections. This information now undergoes physical design, a process that translates it into a GDS file. The GDS file serves as a manufacturing blueprint, specifying the exact layout etched onto the silicon wafer. Physical design encompasses several key steps: floor planning (organizing chip components), placement (positioning individual elements), clock tree synthesis (ensuring consistent timing), and detailed routing (connecting components efficiently). Throughout this process, we prioritize factors like performance (timing), chip area utilization, and power consumption to optimize the final product.

Delving into Physical Design: A Step-by-Step Exploration

Physical design transforms the abstract netlist representation of a circuit into a manufacturable layout. Here's a breakdown of the key steps involved:

1. Netlist Integration: The process begins with integrating the netlist, a textual description of the circuit's components and their interconnections, into the physical design environment. This netlist acts as the foundation upon which the chip layout is built.

2. Floorplanning: Floorplanning is the strategic allocation of space on the chip for various functional blocks. Standard cells, memories, and other critical components are positioned with careful consideration of factors like area utilization, performance optimization, and minimization of routing complexity. This initial layout plan forms the backbone for the chip's physical realization.

3. Power Planning: Similar to how a city requires a robust power grid, power planning in physical design ensures the efficient and reliable delivery of electricity throughout the chip. Engineers meticulously design the power and ground networks, optimizing their placement and routing to minimize electrical resistance and noise. This step is crucial for guaranteeing stable operation and minimizing power consumption in the final chip.

4. Placement:

This stage involves strategically positioning numerous standard cells, the building blocks of a chip, within the defined floorplan. The primary objective of placement is to ensure "routability," meaning the ability to efficiently connect all these cells with wires in the next step. Placement algorithms consider factors like minimizing wire length, reducing congestion (overly dense areas), and optimizing performance.

5. Clock Tree Synthesis (CTS): A chip's "heartbeat" is its clock signal, which synchronizes operations across different parts. CTS meticulously designs a clock distribution network that

delivers this crucial signal with minimal delay variation across the entire chip. This minimizes "clock skew," which can lead to timing errors. Special routing techniques and buffers are employed to achieve a balanced and reliable clock network.

6. Global Routing:

Imagine a city's main roads. Global routing defines the initial, high-level paths for connecting various components (cells) within the chip. It considers factors like minimizing overall wire length and avoiding congestion points. The quality of global routing significantly impacts the efficiency of detailed routing in the next step, ultimately affecting the chip's performance and area utilization.

7. Detailed Routing:

Following the "highways" established by global routing, detailed routing lays out the actual physical connections (wires) between all components. This stage ensures all nets (groups of connected pins) are efficiently routed using the available space within the chip, while adhering to design rules and minimizing signal delays.

8. Writing GDS: Finally, the physical design information is captured in a standardized format called GDS (Graphic Design System). This file acts as a blueprint for the chip manufacturer, containing the precise layout of transistors, wires, and other elements. GDS files are essential for transferring design data and enabling chip fabrication.

Layout for 50% core utilization area

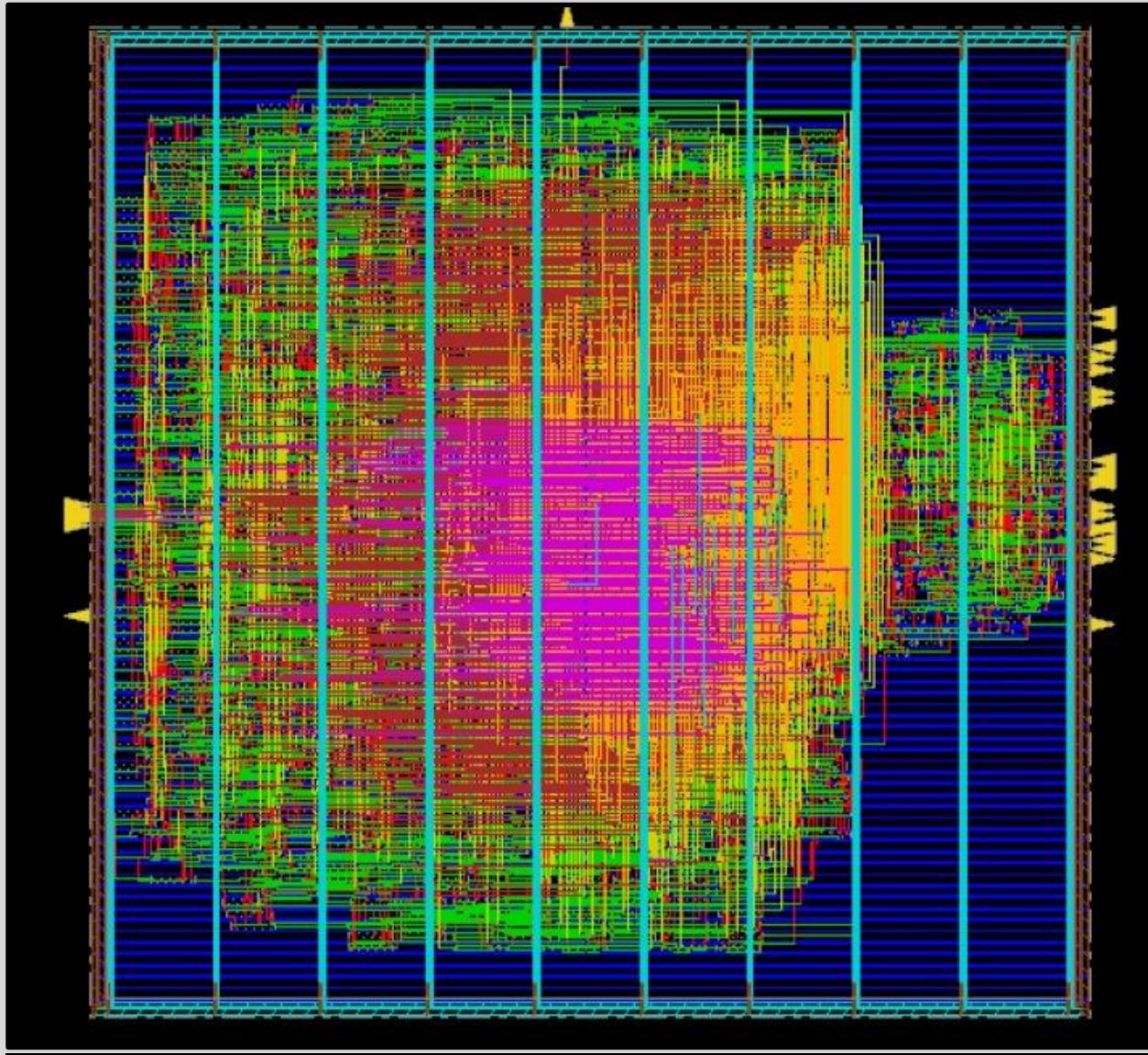


Figure 1.1: Layout for 50% core utilization

Layout for 80% core utilization area

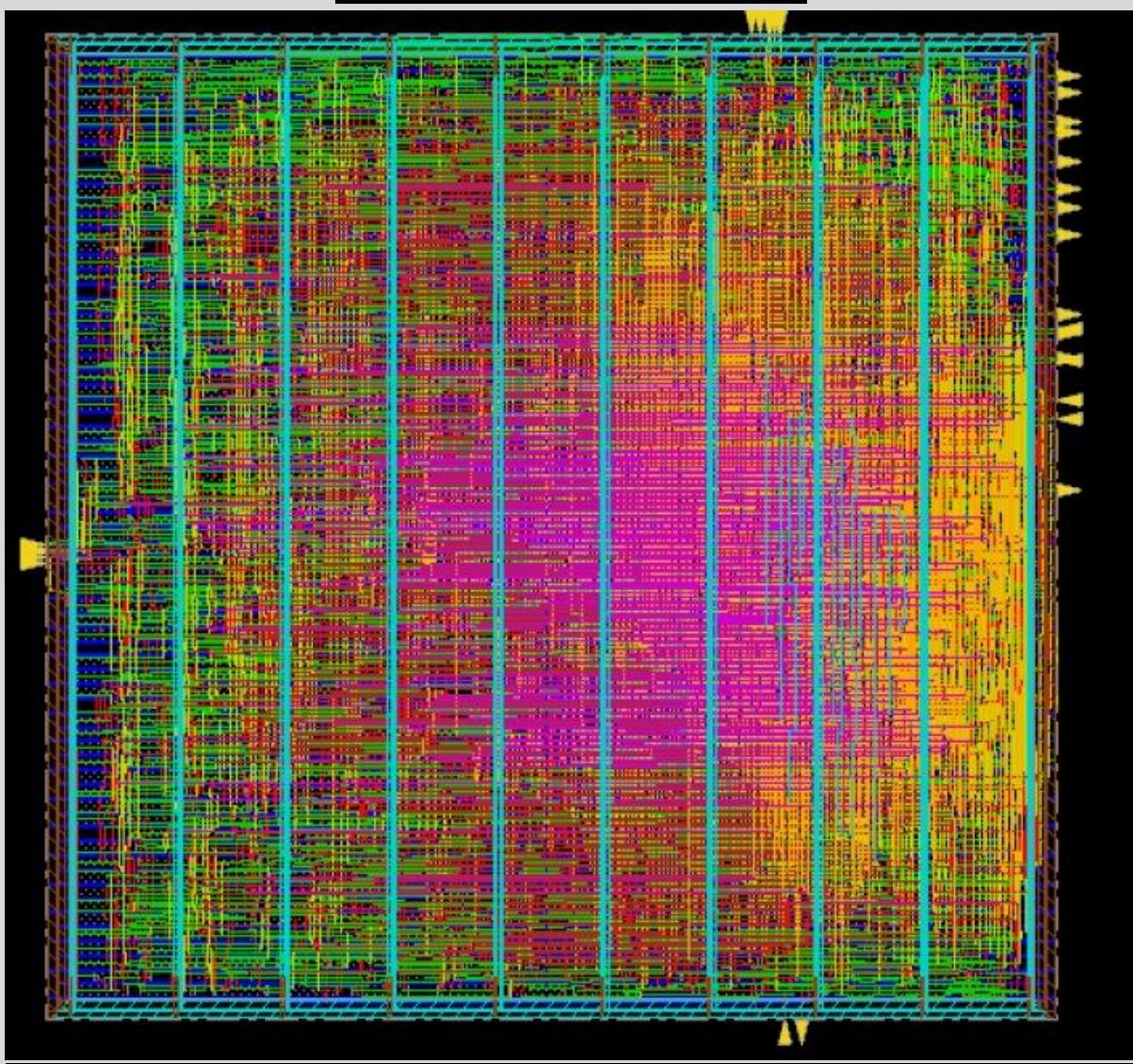


Figure 1.2: Layout for 80% core utilization

Impact of all the parameters is tabulated below due to the utilization factor down the flow from placement to routing.

	PARAMETERS	UTILIZATIO N FACTOR: 0.5	UTILIZATIO N FACTOR: 0.8
AFTER PLACEMENT	SETUP SLACK(ps)	0.016	0.464
	HOLD SLACK (ps)	-0.103	-0.103
	AREA (μm^2)	24320.71	24320.771
	POWER (mW)	32.11	33.60
AFTER CTS	SETUP SLACK(ps)	0.015	0.470
	HOLD SLACK (ps)	0.008	0.008
	AREA (μm^2)	24027.73	22928.772
	POWER (mW)	25.322	25.232
AFTER ROUTING	SETUP SLACK(ps)	0.839	0.862
	HOLD SLACK (ps)	0.007	0.081
	AREA (μm^2)	24027.73	22928.772
	POWER (mW)	25.30	25.20

Table 1.1 Comparison of results for different parameters when modifying the utilization factor

Interpretation of results based on different values of utilization factor:

Impact on Slack: UF = 0.8 denotes 20% of the area that will be used for routing in the design, whereas UF = 0.5 represents 50%. So, the less the area available for routing, the more difficult it will be for the tool to fix violations as the space to place extra buffers, route the circuit differently, etc is less. So, for UF=0.8, it takes time for the tool to fix violations quickly. We can observe that post routing, the hold slack is more remarkable for the utilization factor of 0.5 rather than 0.8, as the tool can quickly fix and optimize for 0.5, which has more routing area. So After placement decreases and after CTS, the area almost gets fixed, and the same goes for power

After placement, the location of standard cells is fixed. One thing to observe is that hold slack becomes fixed as the tool adds buffers in the path to fix violations

2. Before Physical Design

Graph-Based Analysis (GBA) and Path-based analysis(PBA):

In GBA, slack is estimated for the worst path, where arrival time is calculated based on the absolute worst case scenario, however, in PBA, slack is unbiasedly assessed for all paths. The difference between the required time and the arrival time is used to determine slack. Therefore, we need the arrival time to be shorter than required time.

$$\text{Hold Slack} = \text{Arrival time} - \text{Required time}$$

$$\text{Setup Slack} = \text{Required time} - \text{Arrival time}$$

Assuming that one of the paths has negative slack after analysis using GBA, which only takes into account the worst path, we can either analyze the path using PBA, which takes into account all the arrival time of all the paths, and select that path where the arrival time is less than minimum time needed to make the slack positive. Additionally, we can modify the cells utilized or the input transition to make the slack positive.

Timing report of the worst setup slack path(GBA);

Path 1: MET Setup Check with Pin mem_inst/mem_reg[53][5]1437/CK						
Endpoint: mem_inst/mem_reg[53][5]1437/S0 (^) checked with leading edge of 'CLK'						
Beginpoint: rst (v) triggered by leading edge of 'CLK'						
Path Groups: {default}						
Analysis View: view1						
Other End Arrival Time	0.000					
- Setup	0.137					
+ Phase Shift	2.000					
= Required Time	1.863					
- Arrival Time	0.949					
= Slack Time	0.915					
Clock Rise Edge	0.000					
+ Input Delay	0.400					
= Beginpoint Arrival Time	0.400					
Timing Path:						
Pin	Edge	Net	Cell	Delay	Arrival Time	Required Time
rst	v	rst			0.400	1.315
mem_inst/g67717/B	v	rst	NOR2XL	0.000	0.400	1.315
mem_inst/g67717/Y	^	mem_inst/n_18	NOR2XL	0.060	0.460	1.374
mem_inst/g67691/A	^	mem_inst/n_18	NAND2XL	0.000	0.460	1.374
mem_inst/g67691/Y	v	mem_inst/n_45	NAND2XL	0.110	0.570	1.484
mem_inst/g67653/B	v	mem_inst/n_45	NOR2XL	0.000	0.570	1.484
mem_inst/g67653/Y	^	mem_inst/n_73	NOR2XL	0.379	0.949	1.863
mem_inst/mem_reg[53][5]1437/S0	^	mem_inst/n_73	SMDFFHQX1	0.000	0.949	1.863
Clock Rise Edge	0.000					
= Beginpoint Arrival Time	0.000					
Other End Path:						
Pin	Edge	Net	Cell	Delay	Arrival Time	Required Time
clk	^	clk			0.000	-0.915
mem_inst/mem_reg[53][5]1437/CK	^	clk	SMDFFHQX1	0.000	0.000	-0.915

Figure 2.1: Timing report of the worst setup slack(GBA)

Timing Report of Worst setup slack Path (PBA):

```

Path 50: MET Setup Check with Pin mem_inst/mem_reg[5][0]376/CK
Endpoint: mem_inst/mem_reg[5][0]376/S0 (^) checked with leading edge of 'CLK'
Beginpoint: rst (v) triggered by leading edge of 'CLK'
Path Groups: {CLK}
Analysis View: view1
Retime Analysis { Data Path-Slew }
Other End Arrival Time 0.000
- Setup 0.672
+ Phase Shift 4.000
= Required Time 3.329
- Arrival Time 2.283
= Slack Time 1.045
= Slack Time(original) 1.041
    Clock Rise Edge 0.000
    + Input Delay 0.400
    = Beginpoint Arrival Time 0.400
Timing Path:
+-----+
| Instance | Arc | Cell | Retime | Arrival | Required |
|          |     |      | Delay | Time   | Time    |
+-----+
|          |rst v| NOR2XL | 0.000 | 0.400 | 1.445 |
| mem_inst/g67717 | B v -> Y ^ | NOR2XL | 0.182 | 0.582 | 1.627 |
| mem_inst/g67689 | A ^ -> Y v | NAND2XL | 0.000 | 0.582 | 1.627 |
| mem_inst/g67689 | A ^ -> Y v | NAND2XL | 0.470 | 1.051 | 2.096 |
| mem_inst/g67648 | NOR2XL | 0.000 | 1.051 | 1.051 | 2.096 |
| mem_inst/g67648 | B v -> Y ^ | NOR2XL | 1.232 | 2.283 | 3.329 |
| mem_inst/mem_reg[5][0]376 | SMDFFHQX1 | 0.000 | 2.283 | 2.283 | 3.329 |
+-----+
Clock Rise Edge 0.000
= Beginpoint Arrival Time 0.000
Other End Path:
+-----+
| Instance | Arc | Cell | Retime | Arrival | Required |
|          |     |      | Delay | Time   | Time    |
|          |clk ^| SMDFFHQX1 | 0.000 | 0.000 | -1.045 |
| mem_inst/mem_reg[5][0]376 | SMDFFHQX1 | 0.000 | 0.000 | -1.045 |
+-----+
INFO: Path Based Analysis (PBA) performed on total '50' paths

```

Figure 2.2: Timing report of the worst setup slack(PBA)

In the above-reported path, GBA slack is 0.915 and PBA slack is 1.041 at the clock period of 4.the worst delay is considered taking into account the worst slew and worst arrival time and whereas in PBA only the directed path is observed and slack is calculated. In this case, both the w orst delay path and directed path are the same and hence, equal slacks are obtained after PBA and GBA

❖ **Slew Rate: Managing Signal Transition Speed**

Slew rate, the rate of change of a signal's voltage level over time, significantly impacts circuit performance. A slow slew rate, characterized by gradual transitions, introduces delays. This delay arises from the time required for the input signal to reach the switching threshold of the receiving gate. Optimizing the slew rate becomes crucial to minimize these delays and achieve desired timing goals.

❖ **Load Capacitance: The Impact of Connected Gates**

The load capacitance on a node, essentially the total capacitance of connected gates, is crucial in determining the node's switching speed. Imagine charging a capacitor; a higher capacitance requires more time to reach the desired voltage level. Increased load capacitance reduces the signal's ability to switch voltage levels, leading to increased delay. Accurate static timing analysis techniques account for load capacitance to predict realistic delays within the design.

❖ **Unateness: Ensuring Predictable Gate Behavior**

Unateness refers to a specific characteristic of the relationship between the input and output of a logic gate. A positive unate function guarantees that a rising input always results in a rising or unchanged output, and vice versa for a falling input. This predictability simplifies timing analysis because the output behavior is well-defined. Deviations from unateness can complicate timing analysis and potentially introduce unexpected delays due to non-monotonic behavior.

Types of Unateness :

1. Positive Unate:

Definition: A logic gate is considered positive unate for a specific timing arc if a rising transition at the input always results in a rising or no change in the output, and conversely, a falling transition at the input always results in a falling or no change in the output. In simpler terms, the output transition strictly follows or maintains the input transition.

2. Negative Unate:

Definition: A logic gate is considered negative unate for a specific timing arc if a rising transition at the input results in a falling transition at the output, and conversely, a falling transition at the input results in an increasing transition at the output.

Essentially, the output transition is the logical inverse of the input transition.

3. Non-Unate:

Definition:

A logic gate exhibits non-unateness for a specific timing arc if the relationship between the input and output transitions is unpredictable. The output behavior depends on a combination of factors, including the input transition and the previous state of the circuit. Non-unateness can complicate static timing analysis as it introduces uncertainty.

about the output timing.

Understanding Unateness Benefits:

Simplified Timing Analysis: Knowing the unateness of a gate allows for more efficient timing analysis by eliminating the need for complex calculations for predictable input-output behavior.

Improved Design Optimization: By leveraging unateness information, designers can optimize circuit performance by focusing on critical paths with non-unate gates, where timing analysis may require more effort.

Conclusion:

Unateness plays a vital role in understanding the timing characteristics of logic gates in VLSI design. Identifying positive, negative, and non-unate timing arcs allows for efficient and accurate static timing analysis, creating reliable and high-performance electronic devices.

Area breakup of standard cells :

Hinst Name	Module Name	Inst Count	Total Area
top8_module		1670	24320.711
alu_inst	alu	242	1140.648
decoder_inst	decoder	11	158.192
ff_alu_in1	ff_8bit	8	163.490
ff_carry_inst	ff_154	1	20.436
ff_negative_inst	ff_152	1	20.436
ff_pc_rst_inst	ff	2	24.978
ff_zero_inst	ff_153	1	20.436
ir_inst	instr_reg	11	158.192
mem_inst	instr_memory	1369	22258.158
pc_inst	pc	24	355.743

Figure 2.3: Area breakup of standard cells

The total area before placement came to be **24320.711 μm^2** .

Power Analysis:

Total Power						
Total Internal Power:	7.12244494		80.9326%			
Total Switching Power:	1.51773314		17.2461%			
Total Leakage Power:	0.16028826		1.8214%			
Total Power:	8.80046614					
Group	Internal Power	Switching Power	Leakage Power	Total Power	Percentage (%)	
Sequential	6.932	1.406	0.1476	8.486	96.42	
Macro	0	0	0	0	0	
IO	0	0	0	0	0	
Combinational	0.1902	0.1118	0.01268	0.3146	3.575	
Clock (Combinational)	0	0	0	0	0	
Clock (Sequential)	0	0	0	0	0	
Total	7.122	1.518	0.1603	8.8	100	
Rail	Voltage	Internal Power	Switching Power	Leakage Power	Total Power	Percentage (%)
Default	0.9	7.122	1.518	0.1603	8.8	100
* Power Distribution Summary:						
* Highest Average Power: alu_inst/result_reg reg[2] (TLATNX1):					0.1793	
* Highest Leakage Power: mem_inst/mem_reg[0][0]266 (SMDFFHQX1):					0.000198	
* Total Cap: 2.38e-11 F						
* Total instances in design: 1670						
* Total instances in design with no power: 0						
* Total instances in design with no activity: 0						

Figure 2.4: Power Analysis

Internal power = 7.122 mW
Switching power = 1.517 mW
Leakage power = 0.1602 mW
Total power = 8.8004 mW.

3. 0.5 Core Utilization :

3.1 After Placement:

Setup Analysis:

Path 1: MET Setup Check with Pin mem_inst/mem_reg[0][7]273/CK						
Endpoint: mem_inst/mem_reg[0][7]273/S0 (^) checked with leading edge of 'CLK'						
Beginpoint: rst (v) triggered by leading edge of 'CLK'						
Path Groups: {CLK}						
Analysis View: view1						
Other End Arrival Time 0.000						
- Setup 0.136						
+ Phase Shift 2.000						
= Required Time 1.864						
- Arrival Time 1.394						
= Slack Time 0.470						
Clock Rise Edge 0.000						
+ Input Delay 0.400						
= Beginpoint Arrival Time 0.400						
Timing Path:						
Pin	Edge	Net	Cell	Delay	Arrival Time	Required Time
rst	v	rst			0.400	0.870
mem_inst/g67717/B	v	rst	NOR2XL	0.000	0.400	0.871
mem_inst/g67717/Y	^	mem_inst/n_18	NOR2XL	0.157	0.557	1.027
mem_inst/g67689/A	^	mem_inst/n_18	NAND2XL	0.000	0.557	1.028
mem_inst/g67689/Y	v	mem_inst/n_49	NAND2XL	0.292	0.850	1.320
mem_inst/g67601/B	v	mem_inst/n_49	NOR2XL	0.002	0.852	1.322
mem_inst/g67601/Y	^	mem_inst/n_125	NOR2XL	0.540	1.392	1.862
mem_inst/mem_reg[0][7]273/S0	^	mem_inst/n_125	SMDFFHQX1	0.002	1.394	1.864
Clock Rise Edge 0.000						
= Beginpoint Arrival Time 0.000						
Other End Path:						
Pin	Edge	Net	Cell	Delay	Arrival Time	Required Time
clk	^	clk		0.000	-0.470	
mem_inst/mem_reg[0][7]273/CK	^	clk	SMDFFHQX1	0.000	0.000	-0.470

Figure 3.1.1: Setup timing report

- This analysis examines the timing slack for the worst setup path in your design, which originates from the rst signal and terminates at the register mem_inst/mem_reg[0][7]273.
- Key observations:
Arrival Time: 1.394 ns
Required Time: 1.864 ns
Slack: 0.470 ns (positive)
- Interpretation:
The positive slack value (0.470 ns) indicates a healthy timing margin for this path. The data arrives at the register (mem_inst/mem_reg[0][7]273) well before the clock edge that triggers its capture. This ensures a valid setup condition and proper data storage. In simpler terms, the data has sufficient time to settle before it needs to be captured by the register.

Hold Analysis:

```

Path 1: VIOLATED Hold Check with Pin ff_alu_in1/q_reg[1]/CK
Endpoint: ff_alu_in1/q_reg[1]/D (^) checked with leading edge of 'CLK'
Beginpoint: alu_in1_inp[1] (^) triggered by leading edge of '@'
Path Groups: {CLK}
Analysis View: view1
Other End Arrival Time      0.000
+ Hold                      0.103
+ Phase Shift                0.000
= Required Time              0.103
  Arrival Time               0.000
  Slack Time                 -0.103
    Clock Rise Edge          0.000
    + Input Delay            0.000
    = Beginpoint Arrival Time 0.000
Timing Path:
+-----+
|   Pin    | Edge | Net        | Cell     | Delay | Arrival | Required |
|          |      |           |          |       | Time    | Time     |
+-----+
| alu_in1_inp[1] | ^ | alu_in1_inp[1] |          |       | 0.000  | 0.103  |
| ff_alu_in1/q_reg[1]/D | ^ | alu_in1_inp[1] | SDFFQX1 | 0.000 | 0.000  | 0.103  |
+-----+
Clock Rise Edge             0.000
= Beginpoint Arrival Time   0.000
Other End Path:
+-----+
|   Pin    | Edge | Net        | Cell     | Delay | Arrival | Required |
|          |      |           |          |       | Time    | Time     |
+-----+
| clk      | ^ | clk       |          |       | 0.000  | -0.103 |
| ff_alu_in1/q_reg[1]/CK | ^ | clk       | SDFFQX1 | 0.000 | 0.000  | -0.103 |
+-----+

```

Figure 3.1.2: Hold timing report

- This analysis focuses on a critical path in your design with negative setup slack. The path originates from the signal alu_in1_inp[1] and terminates at the data input (D) of the register ff_alu_in1/q_reg[1].
- Key observations:
Arrival Time: 0.000 ns
Required Time: 0.103 ns
Slack: -0.103 ns (negative)
- Interpretation:
The negative slack value (-0.103 ns) signifies a setup timing violation. The data arrives at the register's data input much earlier (0.000 ns) than the required time (0.103 ns) for proper capture by the clock edge. This violation could potentially lead to incorrect data being stored in the register.

Effect on delay before and after placement:

```

Path 1: MET Setup Check with Pin mem_inst/mem_reg[53][5]1437/CK
Endpoint: mem_inst/mem_reg[53][5]1437/S0 (^) checked with leading edge of
'CLK'
Beginpoint: rst (v) triggered by leading edge of
'CLK'
Path Groups: {default}
Analysis View: view1
Other End Arrival Time 0.000
- Setup 0.137
+ Phase Shift 2.000
= Required Time 1.863
- Arrival Time 0.949
= Slack Time 0.915
Clock Rise Edge 0.000
+ Input Delay 0.400
= Beginpoint Arrival Time 0.400
Timing Path:
+-----+
| Pin | Edge | Net | Cell | Delay | Arrival | Required |
|     |     |     |     |       | Time   | Time    |
+-----+
| rst | v   | rst |       |       | 0.400 | 1.315 |
| mem_inst/g67717/B | v   | rst | NOR2XL | 0.000 | 0.400 | 1.315 |
| mem_inst/g67717/Y | ^   | mem_inst/n_18 | NOR2XL | 0.060 | 0.460 | 1.374 |
| mem_inst/g67691/A | ^   | mem_inst/n_18 | NAND2XL | 0.000 | 0.460 | 1.374 |
| mem_inst/g67691/Y | v   | mem_inst/n_45 | NAND2XL | 0.110 | 0.570 | 1.484 |
| mem_inst/g67653/B | v   | mem_inst/n_45 | NOR2XL | 0.000 | 0.570 | 1.484 |
| mem_inst/g67653/Y | ^   | mem_inst/n_73 | NOR2XL | 0.379 | 0.949 | 1.863 |
| mem_inst/mem_reg[53][5]1437/S0 | ^   | mem_inst/n_73 | SMDFFHQX1 | 0.000 | 0.949 | 1.863 |
+-----+
Clock Rise Edge 0.000
= Beginpoint Arrival Time 0.000
Other End Path:
+-----+
| Pin | Edge | Net | Cell | Delay | Arrival | Required |
|     |     |     |     |       | Time   | Time    |
+-----+
| clk | ^   | clk |       |       | 0.000 | -0.915 |
| mem_inst/mem_reg[53][5]1437/CK | ^   | clk | SMDFFHQX1 | 0.000 | 0.000 | -0.915 |
+-----+

```

Fig. 3.1.3 Delay Before placement

```

Path 1: MET Setup Check with Pin mem_inst/mem_reg[0][7]273/CK
Endpoint: mem_inst/mem_reg[0][7]273/S0 (^) checked with leading edge of 'CLK'
Beginpoint: rst (v) triggered by leading edge of 'CLK'
Path Groups: {CLK}
Analysis View: view1
Other End Arrival Time 0.000
- Setup 0.136
+ Phase Shift 2.000
= Required Time 1.864
- Arrival Time 1.394
= Slack Time 0.470
Clock Rise Edge 0.000
+ Input Delay 0.400
= Beginpoint Arrival Time 0.400
Timing Path:
+-----+
| Pin | Edge | Net | Cell | Delay | Arrival | Required |
|     |      |     |     |       | Time   | Time    |
+-----+
| rst | v    | rst | NOR2XL | 0.000 | 0.400 | 0.870 |
| mem_inst/g67717/B | v    | rst | NOR2XL | 0.000 | 0.400 | 0.871 |
| mem_inst/g67717/Y | ^    | mem_inst/n_18 | NOR2XL | 0.157 | 0.557 | 1.027 |
| mem_inst/g67689/A | ^    | mem_inst/n_18 | NAND2XL | 0.000 | 0.557 | 1.028 |
| mem_inst/g67689/Y | v    | mem_inst/n_49 | NAND2XL | 0.292 | 0.850 | 1.320 |
| mem_inst/g67601/B | v    | mem_inst/n_49 | NOR2XL | 0.002 | 0.852 | 1.322 |
| mem_inst/g67601/Y | ^    | mem_inst/n_125 | NOR2XL | 0.540 | 1.392 | 1.862 |
| mem_inst/mem_reg[0][7]273/S0 | ^    | mem_inst/n_125 | SMDFFHQX1 | 0.002 | 1.394 | 1.864 |
+-----+
Clock Rise Edge 0.000
= Beginpoint Arrival Time 0.000
Other End Path:
+-----+
| Pin | Edge | Net | Cell | Delay | Arrival | Required |
|     |      |     |     |       | Time   | Time    |
+-----+
| clk | ^    | clk | SMDFFHQX1 | 0.000 | 0.000 | -0.470 |
| mem_inst/mem_reg[0][7]273/CK | ^    | clk | SMDFFHQX1 | 0.000 | 0.000 | -0.470 |
+-----+

```

Fig.3.1.4 Delay After placement

Slack before placement = 0.915

Slack after placement = 0.470

"This shows a decrease in slack from 0.915 to 0.470 after placement. In other words, there is less buffer time available after components are placed." This clarifies that a decrease in slack signifies less buffer time, making it easier to understand the relationship between slack and placement.

Following table shows the change in delay on instances after placement:

Instance		Delay
g67717	Before placement	0.06
	After placement	0.157
g67689	Before placement	0.110
	After placement	0.292
g67601	Before placement	0.379
	After placement	0.538

Table 3.1.1: Impact on delay due to placement

an increase in delay after placement for all listed instances (g67717, g67689, and g67601). This occurs because placement often optimizes the circuit layout, reducing gate delays (a form of slack) within the individual gates. However, this optimization can introduce new delays due to the increased routing distances between components.

Area Analysis:

Hinst Name	Module Name	Inst Count	Total Area
<hr/>			
top8_module		1670	24320.711
alu_inst	alu	242	1140.648
decoder_inst	decoder	11	158.192
ff_alu_in1	ff_8bit	8	163.490
ff_carry_inst	ff_154	1	20.436
ff_negative_inst	ff_152	1	20.436
ff_pc_rst_inst	ff	2	24.978
ff_zero_inst	ff_153	1	20.436
ir_inst	instr_reg	11	158.192
mem_inst	instr_memory	1369	22258.158
pc_inst	pc	24	355.743

Figure 3.1.5: Area Analysis

Post Placement , **Total Area = 24320.71 um²** .

Power Analysis:

Total Power					
Group	Percentage	Internal Power	Switching Power	Leakage Power	Total Power (%)
Sequential	96.29	30.1	0.5534	0.2657	30.92
Macro	0	0	0	0	0
IO	0	0	0	0	0
Combinational	3.711	0.5549	0.6044	0.03224	1.192
Clock (Combinational)	0	0	0	0	0
Clock (Sequential)	0	0	0	0	0
Total	100	30.65	1.158	0.2979	32.11

Figure 3.1.6: Power Analysis

The post-placement power analysis reveals the following breakdown:

Total Power: 32.11 mW

Internal Power: 30.6532 mW (95.4% of total)

Switching Power: 1.4577 mW (4.5% of total)

Leakage Power: 0.2979 mW (0.9% of total)

Key Observations:

Dominant Internal Power: The analysis indicates that internal power consumption is the primary contributor (over 95%) to the total power usage. This suggests that optimizing the circuit's internal operations could yield the most significant power savings.

Minimal Leakage Power: Leakage power contributes a minor portion (less than 1%) to the total power, implying a well-optimized design in terms of static power consumption

Gate Count:

Gate area 2.2707 um^2			
Level 0 Module top8_module	Gates=10710	Cells=1670	Area= 24320.7 um^2
Level 1 Module alu_inst	Gates=502	Cells=242	Area= 1140.6 um^2
Level 1 Module mem_inst	Gates=9802	Cells=1369	Area= 22258.2 um^2
Level 1 Module pc_inst	Gates=156	Cells=24	Area= 355.7 um^2

Figure 3.1.7: Gate Count report

Number of total gates = 10710

Total number of cells = 1670

Gate area = 24320.7 um^2

Standard Cell location and Placement Strategy :

The precise positioning of cells and the pathways connecting them are influenced by factors such as power supply availability, timing constraints, and interconnection length. The manner in which cells are arranged directly impacts the lengths of the metal wires employed. At this stage of the design process, closely placing cells could potentially result in hold timing violations in the worst-case scenario. Conversely, if the cells are positioned far apart, the routing resources required increase, and the latency escalates due to the longer metal interconnect lengths.

Components are positioned over the die once the floor layout and placement have been completed. These components' locations over the entire die are determined by criteria including timings that adhere to timing specifications, connections between cells, and routing between other components. Mostly the strongly connected instances are placed together to save the resources.

The Below given is the layout for the post placement core containing standard cells only.

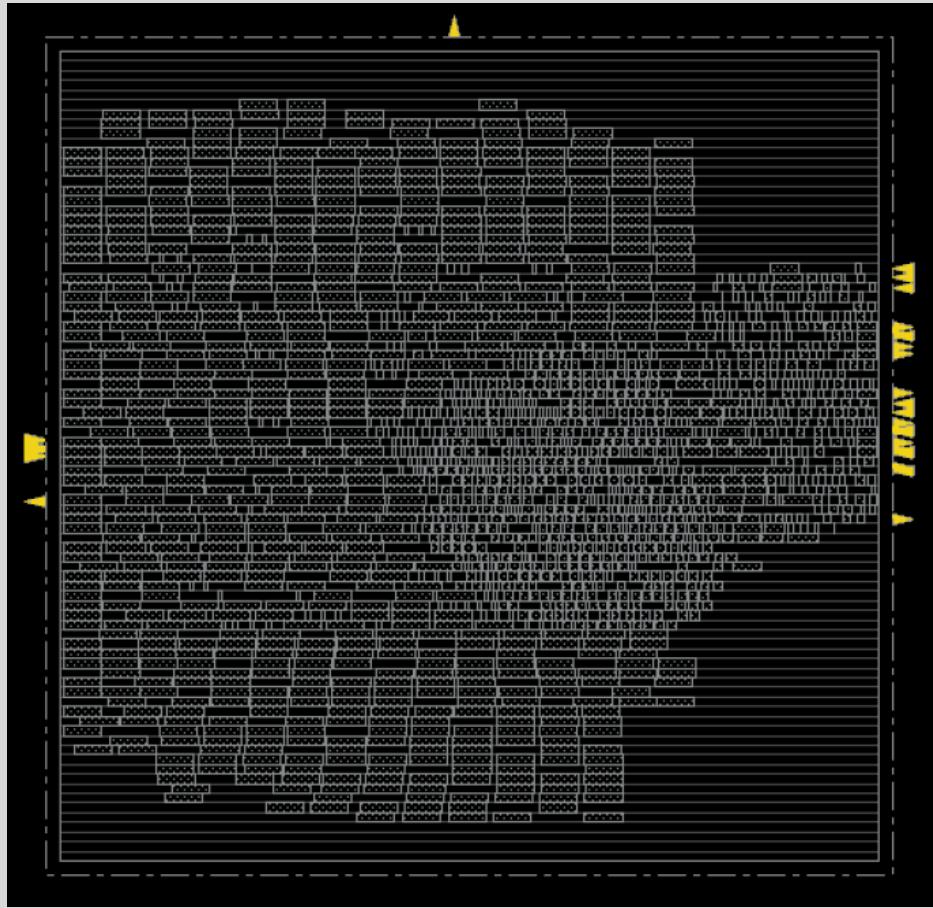


Figure 3.1.8: Standard cells Placement

3.2 After Clock Tree synthesis

Setup Analysis:

```

Path 1: MET Setup Check with Pin mem_inst/mem_reg[0][7]273/CK
Endpoint: mem_inst/mem_reg[0][7]273/S0 (^) checked with leading edge of 'CLK'
Beginpoint: rst (v) triggered by leading edge of 'CLK'
Path Groups: {CLK}
Analysis View: view1
Other End Arrival Time 0.000
- Setup 0.136
+ Phase Shift 2.000
= Required Time 1.864
- Arrival Time 1.393
= Slack Time 0.471
    Clock Rise Edge 0.000
    + Input Delay 0.400
    = Beginpoint Arrival Time 0.400
Timing Path:
+-----+
| Pin | Edge | Net | Cell | Delay | Arrival | Required |
|     |      |     |     |       | Time   | Time    |
+-----+
| rst | v    | rst | NOR2XL | 0.000 | 0.400 | 0.871 |
| mem_inst/g67717/B | v    | rst | NOR2XL | 0.000 | 0.400 | 0.871 |
| mem_inst/g67717/Y | ^    | mem_inst/n_18 | NOR2XL | 0.157 | 0.557 | 1.028 |
| mem_inst/g67689/A | ^    | mem_inst/n_18 | NAND2XL | 0.000 | 0.557 | 1.028 |
| mem_inst/g67689/Y | v    | mem_inst/n_49 | NAND2XL | 0.292 | 0.849 | 1.320 |
| mem_inst/g67601/B | v    | mem_inst/n_49 | NOR2XL | 0.002 | 0.851 | 1.322 |
| mem_inst/g67601/Y | ^    | mem_inst/n_125 | NOR2XL | 0.540 | 1.391 | 1.862 |
| mem_inst/mem_reg[0][7]273/S0 | ^    | mem_inst/n_125 | SMDFFHQX1 | 0.002 | 1.393 | 1.864 |
+-----+
Clock Rise Edge 0.000
= Beginpoint Arrival Time 0.000
Other End Path:
+-----+
| Pin | Edge | Net | Cell | Delay | Arrival | Required |
|     |      |     |     |       | Time   | Time    |
+-----+
| clk | ^    | clk | SMDFFHQX1 | 0.000 | 0.000 | -0.471 |
| mem_inst/mem_reg[0][7]273/CK | ^    | clk | SMDFFHQX1 | 0.000 | 0.000 | -0.471 |
+-----+

```

Figure 3.2.1: Setup Analysis of worst path

- **Key Timing Parameters:**

Arrival Time: 1.393 ns (represents the time it takes for the data signal to reach the memory register)

Required Time: 1.864 ns (minimum amount of time the data signal needs to be stable before the clock edge arrives for proper storage)

Slack: 0.471 ns (positive)

- **Interpretation:**

The positive slack value of 0.471 ns indicates that the data signal arrives at the memory register with a margin of 0.471 ns before the clock edge. In simpler terms, the data has sufficient "buffer time" to be reliably stored before the memory needs it. This signifies a well-functioning design from a timing perspective for this specific path.

Effect on worst setup path after CTS:

Before CTS	After CTS
<pre> Path 1: MET Setup Check with Pin mem_inst/mem_reg[0][7]273/CK Endpoint: mem_inst/mem_reg[0][7]273/S0 (^) checked with leading edge of 'CLK' Beginpoint: rst (v) triggered by leading edge of 'CLK' Path Groups: {CLK} Analysis View: view1 Other End Arrival Time 0.000 - Setup 0.136 + Phase Shift 2.000 = Required Time 1.864 - Arrival Time 1.394 = Slack Time 0.470 Clock Rise Edge 0.000 + Input Delay 0.400 = Beginpoint Arrival Time 0.400 Timing Path: +-----+ Pin Edge Net Cell Delay Arrival Required -----+-----+-----+-----+-----+-----+-----+ rst v rst NOR2XL 0.000 0.400 0.870 mem_inst/g67717/B v mem_inst/n_18 NOR2XL 0.000 0.400 0.871 mem_inst/g67717/Y ^ mem_inst/n_18 NOR2XL 0.157 0.557 1.027 mem_inst/g67689/A ^ mem_inst/n_49 NAND2XL 0.000 0.557 1.028 mem_inst/g67689/Y v mem_inst/n_49 NAND2XL 0.292 0.850 1.320 mem_inst/g67601/B v mem_inst/n_49 NOR2XL 0.002 0.852 1.322 mem_inst/g67601/Y ^ mem_inst/n_125 NOR2XL 0.548 1.392 1.862 mem_inst/mem_reg[0][7]273/S0 ^ mem_inst/n_125 SMDFFHQX1 0.002 1.394 1.864 +-----+ Clock Rise Edge 0.000 = Beginpoint Arrival Time 0.000 Other End Path: +-----+ Pin Edge Net Cell Delay Arrival Required -----+-----+-----+-----+-----+-----+----- clk ^ clk 0.000 -0.470 mem_inst/mem_reg[0][7]273/CK ^ clk SMDFFHQX1 0.000 0.000 -0.470 +-----+ </pre> <p style="text-align: center;">Slack time = 0.470ps</p>	<pre> Path 1: MET Setup Check with Pin mem_inst/mem_reg[0][7]273/CK Endpoint: mem_inst/mem_reg[0][7]273/S0 (^) checked with leading edge of 'CLK' Beginpoint: rst (v) triggered by leading edge of 'CLK' Path Groups: {CLK} Analysis View: view1 Other End Arrival Time 0.000 - Setup 0.136 + Phase Shift 2.000 = Required Time 1.864 - Arrival Time 1.393 = Slack Time 0.471 Clock Rise Edge 0.000 + Input Delay 0.400 = Beginpoint Arrival Time 0.400 Timing Path: +-----+ Pin Edge Net Cell Delay Arrival Required -----+-----+-----+-----+-----+-----+----- rst v rst NOR2XL 0.000 0.400 0.871 mem_inst/g67717/B v rst NOR2XL 0.000 0.400 0.871 mem_inst/g67717/Y ^ mem_inst/n_18 NOR2XL 0.157 0.557 1.028 mem_inst/g67689/A ^ mem_inst/n_18 NAND2XL 0.000 0.557 1.028 mem_inst/g67689/Y v mem_inst/n_49 NAND2XL 0.292 0.849 1.320 mem_inst/g67601/B v mem_inst/n_49 NOR2XL 0.002 0.851 1.322 mem_inst/g67601/Y ^ mem_inst/n_125 NOR2XL 0.540 1.391 1.862 mem_inst/mem_reg[0][7]273/S0 ^ mem_inst/n_125 SMDFFHQX1 0.002 1.393 1.864 +-----+ Clock Rise Edge 0.000 = Beginpoint Arrival Time 0.000 Other End Path: +-----+ Pin Edge Net Cell Delay Arrival Required -----+-----+-----+-----+-----+-----+----- clk ^ clk 0.000 -0.471 mem_inst/mem_reg[0][7]273/CK ^ clk SMDFFHQX1 0.000 0.000 -0.471 +-----+ </pre> <p style="text-align: center;">Slack time = 0.471ps</p>

While it may seem counterintuitive, a slight increase in slack time is sometimes observed after CTS. Here's why this happens:

CTS Optimizes Wire Length: During CTS, buffers are strategically placed throughout the clock path. These buffers effectively shorten the overall wire length by dividing the long path into smaller segments.

Reduced Delay: Shorter wires experience lower resistance and capacitance, leading to faster signal propagation. This translates to a decrease in the arrival time of the clock signal at the endpoint.

Slack and Arrival Time: Slack is the difference between the required arrival time of a signal (e.g., clock) and its actual arrival time. A decrease in arrival time due to CTS can lead to a slight increase in slack.

Hold Analysis :

```

Path 1: MET Hold Check with Pin ff_alu_in1/q_reg[0]/CK
Endpoint: ff_alu_in1/q_reg[0]/SI (v) checked with leading edge of 'CLK'
Beginpoint: DFT_sdi_1 (v) triggered by leading edge of '@'
Path Groups: {CLK}
Analysis View: view1
Other End Arrival Time      0.000
+ Hold                      0.053
+ Phase Shift                0.000
= Required Time              0.053
Arrival Time                 0.060
Slack Time                  0.008
Clock Rise Edge              0.000
+ Input Delay                0.000
= Beginpoint Arrival Time    0.000
Timing Path:
+-----+
|   Pin       | Edge | Net          | Cell | Delay | Arrival | Required |
|             |     |              |      |        | Time   | Time    |
+-----+
| DFT_sdi_1  | v   | DFT_sdi_1   |      |        | 0.000  | -0.008 |
| ff_alu_in1/FE_PHC25_DFT_sdi_1/A | v   | DFT_sdi_1   | DLY1X1 | 0.000  | 0.000  | -0.008 |
| ff_alu_in1/FE_PHC25_DFT_sdi_1/Y | v   | ff_alu_in1/FE_PHN25_DFT_sdi_1 | DLY1X1 | 0.060  | 0.060  | 0.053  |
| ff_alu_in1/q_reg[0]/SI         | v   | ff_alu_in1/FE_PHN25_DFT_sdi_1 | SDFFQX1 | 0.000  | 0.060  | 0.053  |
+-----+
Clock Rise Edge              0.000
= Beginpoint Arrival Time    0.000
Other End Path:
+-----+
|   Pin       | Edge | Net | Cell | Delay | Arrival | Required |
|             |     |     |      |        | Time   | Time    |
+-----+
| clk         | ^   | clk |      |        | 0.000  | 0.008  |
| ff_alu_in1/q_reg[0]/CK | ^   | clk | SDFFQX1 | 0.000  | 0.000  | 0.008  |
+-----+

```

Figure 3.2.2: Hold Analysis of worst path

- The critical path spans from DFT_sdi_1 (begin point) to ff_alu_in1/q_reg[0]/SI (end point).
- **Key Timing Parameters:**
 - Arrival Time: 0.060 ps (represents the time it takes for the data signal to reach the register)
 - Required Time: 0.053 ps (minimum amount of time the data signal needs to be stable before the clock edge arrives for proper storage)
 - Slack: 0.008 ps (positive)
- **Interpretation:** The positive slack value of 0.008 ps indicates that the data signal arrives at the register with a margin of 0.008 ps before the clock edge. In simpler terms, the data has sufficient "buffer time" to be reliably stored. This signifies a well-functioning design from a timing perspective for this specific path, especially after CTS.
- **Impact of CTS:** CTS often optimizes the clock path by strategically placing buffers. While the primary goal is to ensure a uniform clock signal, it can also lead to a slight decrease in data arrival time due to shorter wire lengths. This, in turn, can contribute to a small increase in slack, as observed here.

Effect on worst hold path after CTS:

Before CTS	After CTS
<pre> Path 1: VIOLATED Hold Check with Pin ff_alu_in1/q_reg[1]/CK Endpoint: ff_alu_in1/q_reg[1]/D (^) checked with leading edge of 'CLK' Beginpoint: alu_in1_inp[1] (^) triggered by leading edge of '@' Path Groups: {CLK} Analysis View: view1 Other End Arrival Time 0.000 + Hold 0.103 + Phase Shift 0.000 = Required Time 0.103 Arrival Time 0.000 Slack Time -0.103 Clock Rise Edge 0.000 + Input Delay 0.000 = Beginpoint Arrival Time 0.000 Timing Path: +-----+ Pin Edge Net Cell Delay Arrival Required -----+-----+-----+-----+-----+-----+-----+ alu_in1_inp[1] ^ alu_in1_inp[1] SDFFQX1 0.000 0.000 0.103 ff_alu_in1/q_reg[1]/D ^ alu_in1_inp[1] SDFFQX1 0.000 0.000 0.103 +-----+ Clock Rise Edge 0.000 = Beginpoint Arrival Time 0.000 Other End Path: +-----+ Pin Edge Net Cell Delay Arrival Required -----+-----+-----+-----+-----+-----+-----+ clk ^ clk SDFFQX1 0.000 0.000 -0.103 ff_alu_in1/q_reg[1]/CK ^ clk SDFFQX1 0.000 0.000 -0.103 +-----+ </pre> <p style="text-align: center;">Slack time = -0.103 ps</p>	<pre> Path 1: MET Hold Check with Pin ff_alu_in1/q_reg[0]/CK Endpoint: ff_alu_in1/q_reg[0]/SI (v) checked with leading edge of 'CLK' Beginpoint: DFT_sdi_1 (v) triggered by leading edge of '@' Path Groups: {CLK} Analysis View: view1 Other End Arrival Time 0.000 + Hold 0.053 + Phase Shift 0.000 = Required Time 0.053 Arrival Time 0.060 Slack Time 0.008 Clock Rise Edge 0.000 + Input Delay 0.000 = Beginpoint Arrival Time 0.000 Timing Path: +-----+ Pin Edge Net Cell Delay Arrival Required -----+-----+-----+-----+-----+-----+-----+ DFT_sdi_1 v DFT_sdi_1 0.000 -0.008 ff_alu_in1/FE_PHC25_DFT_sdi_1/A v DFT_sdi_1 0.000 -0.008 ff_alu_in1/FE_PHC25_DFT_sdi_1/Y v ff_alu_in1/FE_PHN25_DFT_sdi_1 DLY1X1 0.060 0.060 0.053 ff_alu_in1/q_reg[0]/SI v ff_alu_in1/FE_PHN25_DFT_sdi_1 DLY1X1 0.060 0.060 0.053 +-----+ Clock Rise Edge 0.000 = Beginpoint Arrival Time 0.000 Other End Path: +-----+ Pin Edge Net Cell Delay Arrival Required -----+-----+-----+-----+-----+-----+-----+ clk ^ clk SDFFQX1 0.000 0.000 0.008 ff_alu_in1/q_reg[0]/CK ^ clk SDFFQX1 0.000 0.000 0.008 +-----+ </pre> <p style="text-align: center;">Slack time = 0.008 ps</p>

Hold slack increases after CTS from **-0.103 ps to 0.008 ps** as the clock nets have been unfolded and the Hold requirement has met. Hence the slack increase is observed..

Hold Slack Improvement After CTS

The text describes a positive change in hold slack after CTS. Here's a breakdown of what's happening:

Hold Time: In digital circuits, hold time refers to the minimum amount of time a data signal needs to be stable before the clock edge arrives for proper capture. A negative hold slack indicates a violation of this requirement.

CTS and Clock Net Unfolding: During CTS, the clock distribution network is optimized. This process can involve "unfolding" the clock nets, essentially breaking them down into smaller segments with buffers strategically inserted.

Improved Hold Slack: By reducing the overall wire length and introducing buffers, CTS can improve the timing characteristics of the clock signal. This can lead to a situation where the data signal now has enough hold time (positive slack) to meet the hold time requirement.

Area Analysis:

Hinst Name	Module Name	Inst Count	Total Area
<hr/>			
top8_module		1653	24027.790
alu_inst	alu	242	1140.648
decoder_inst	decoder	11	158.192
ff_alu_in1	ff_8bit	17	238.424
ff_carry_inst	ff_154	1	20.436
ff_negative_inst	ff_152	1	20.436
ff_pc_rst_inst	ff	2	24.978
ff_zero_inst	ff_153	1	20.436
ir_inst	instr_reg	11	158.192
mem_inst	instr_memory	1330	21831.267
pc_inst	pc	24	355.743

Figure 3.2.3: Area Analysis

The area is found to be **24027.790 μm^2**

Effect on area after CTS:

Before CTS				After CTS			
Hinst Name	Module Name	Inst Count	Total Area	Hinst Name	Module Name	Inst Count	Total Area
innovus 3> report area							
top8_module		1670	24320.711	top8_module		1653	24027.790
alu_inst	alu	242	1140.648	alu_inst	alu	242	1140.648
decoder_inst	decoder	11	158.192	decoder_inst	decoder	11	158.192
ff_alu_in1	ff_8bit	8	163.490	ff_alu_in1	ff_8bit	17	238.424
ff_carry_inst	ff_154	1	20.436	ff_carry_inst	ff_154	1	20.436
ff_negative_inst	ff_152	1	20.436	ff_negative_inst	ff_152	1	20.436
ff_pc_rst_inst	ff	2	24.978	ff_pc_rst_inst	ff	2	24.978
ff_zero_inst	ff_153	1	20.436	ff_zero_inst	ff_153	1	20.436
ir_inst	instr_reg	11	158.192	ir_inst	instr_reg	11	158.192
mem_inst	instr_memory	1369	22258.158	mem_inst	instr_memory	1330	21831.267
pc_inst	pc	24	355.743	pc_inst	pc	24	355.743
Area = 24320.711 μm²				Area = 24027.790 μm²			

Post CTS, as the design was optimized to rectify various timing violations specifically hold violations. Due to optimization, the area was reduced after CTS.

Power Analysis after CTS:

Total Power					
Group	Internal Power	Switching Power	Leakage Power	Total Power	Percentage (%)
Sequential 96.1	23.95	0.1177	0.2657	24.33	
Macro 0	0	0	0	0	
IO 0	0	0	0	0	
Combinational 3.902	0.2495	0.7052	0.03345	0.9882	
Clock (Combinational) 0	0	0	0	0	
Clock (Sequential) 0	0	0	0	0	
Total 100	24.2	0.8229	0.2992	25.32	

Figure 3.2.4: Power Analysis after CTS

Internal power = 24.201 mW

Switching power = 0.823 mW

Leakage power = 0.299 mW

Total power = 25.322 mW.

Effect on power after CTS:

Before CTS	After CTS
<pre>Total Power ----- Total Internal Power: 30.65327992 95.4665% Total Switching Power: 1.15773301 3.6056% Total Leakage Power: 0.29793861 0.9279% Total Power: 32.10895111 ----- Group Percentage) Internal Switching Leakage Total Pe Power Power Power Power (%)) ----- Sequential 30.1 0.5534 0.2657 30.92 Macro 0 0 0 0 IO 0 0 0 0 Combinational 0.5549 0.6044 0.03224 1.192 Clock (Combinational) 0 0 0 0 Clock (Sequential) 0 0 0 0 ----- Total 30.65 1.158 0.2979 32.11 100 -----</pre>	<pre>Total Power ----- Total Internal Power: 24.20069162 95.5690% Total Switching Power: 0.82291121 3.2497% Total Leakage Power: 0.29915131 1.1814% Total Power: 25.32275373 ----- Group Percentage) Internal Switching Leakage Total Pe Power Power Power Power (%)) ----- Sequential 23.95 0.1177 0.2657 24.33 Macro 0 0 0 0 IO 0 0 0 0 Combinational 0.2495 0.7052 0.03345 0.9882 clock (Combinational) 0 0 0 0 clock (Sequential) 0 0 0 0 ----- Total 24.2 0.8229 0.2992 25.32 100 -----</pre>
Total power = 32.11 mW	Total power = 25.32 mW

The total power consumption decreases after CTS due to optimization as area has also decreased.

Gate count:

Gate area 2.2707 um^2	Gates=10581	Cells=1653	Area= 24027.8 um^2
Level 0 Module top8_module	Gates=502	Cells=242	Area= 1140.6 um^2
Level 1 Module alu_inst	Gates=105	Cells=17	Area= 238.4 um^2
Level 1 Module ff_alu_in1	Gates=9614	Cells=1330	Area= 21831.3 um^2
Level 1 Module mem_inst	Gates=156	Cells=24	Area= 355.7 um^2
Level 1 Module pc_inst			

Figure 3.2.5: Gate Count report

Number of total gates = 10581

Total number of cells = 1653

Gate area = 24027.8 um^2

Clock path:

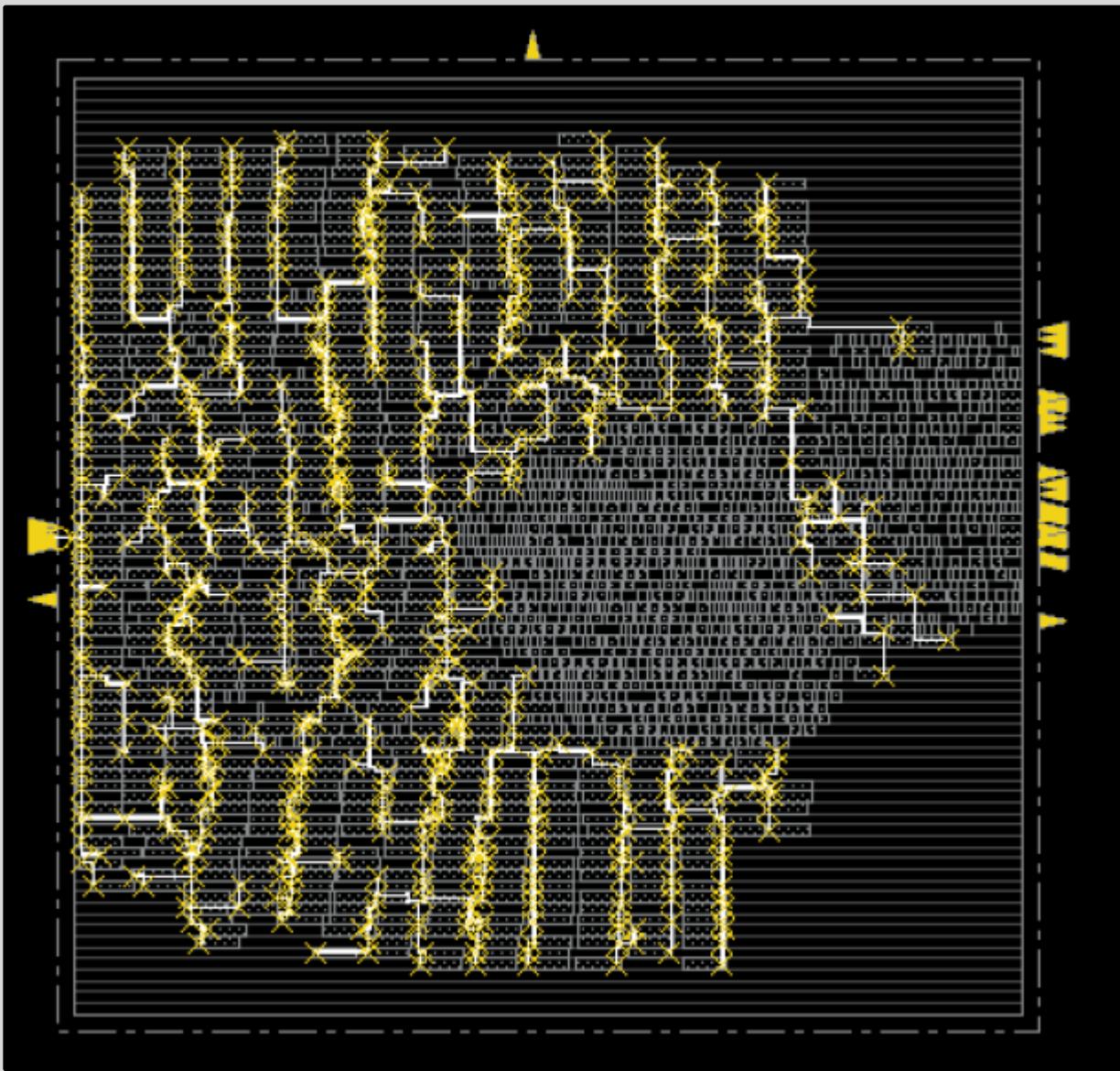


Figure 3.2.6: Snapshot of the path of the routed clock

Clock tree:

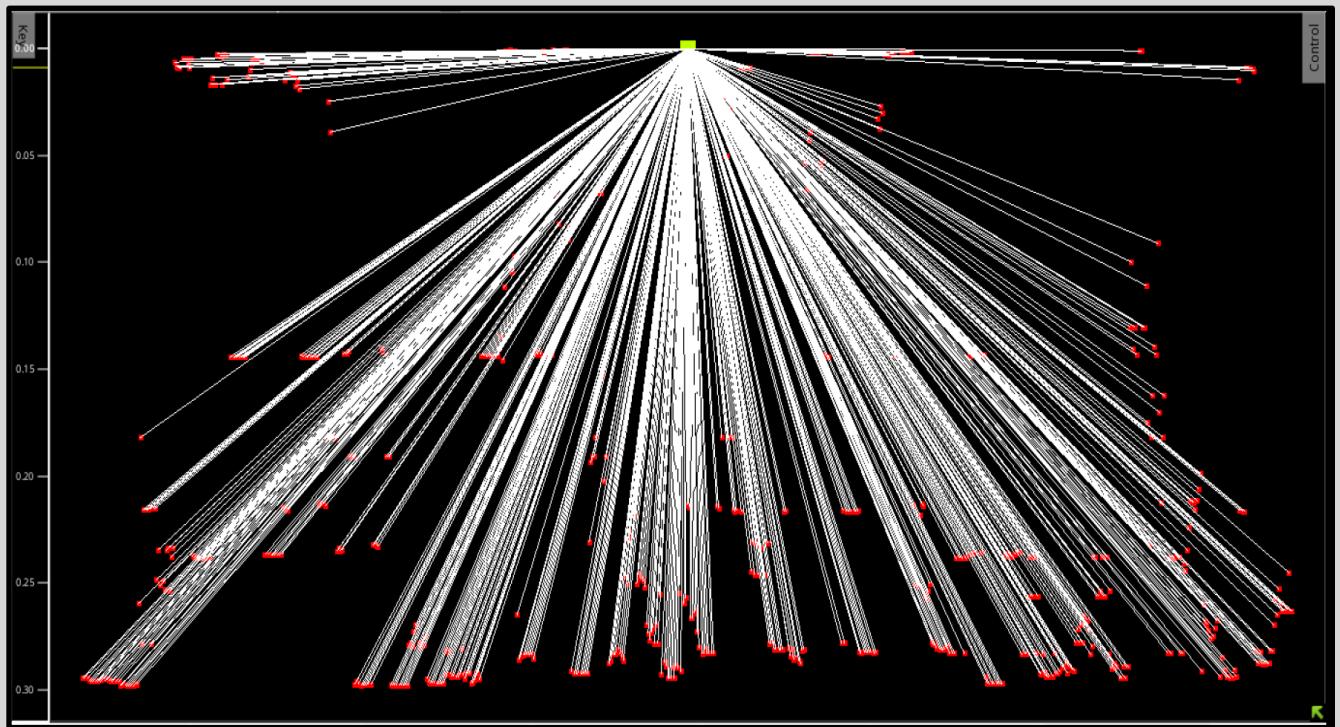


Figure 3.2.7:Snapshot of the generated clock tree for the design

3.3 After detailed routing

Setup Analysis:

Path 1: MET Setup Check with Pin mem_inst/mem_reg[3][8]340/CK						
Endpoint: mem_inst/mem_reg[3][8]340/S0 (^) checked with leading edge of 'CLK'						
Beginpoint: pc_inst/pc_out_addr_reg[1]/Q (^) triggered by leading edge of 'CLK'						
Path Groups: {reg2reg}						
Analysis View: view1						
Other End Arrival Time 0.000						
- Setup 0.136						
+ Phase Shift 2.000						
= Required Time 1.864						
- Arrival Time 1.025						
= Slack Time 0.839						
Clock Rise Edge 0.000						
= Beginpoint Arrival Time 0.000						
Timing Path:						
+-----+-----+-----+-----+-----+-----+-----+						
Pin	Edge	Net	Cell	Delay	Arrival Time	Required Time
clk	^	clk			0.000	0.839
pc_inst/pc_out_addr_reg[1]/CK	^	clk	SDFFRHQX1	0.000	0.000	0.839
pc_inst/pc_out_addr_reg[1]/Q	^	pc_out_addr[1]	SDFFRHQX1	0.121	0.121	0.959
mem_inst/g67716/AN	^	pc_out_addr[1]	NOR2BX1	0.000	0.121	0.959
mem_inst/g67716/Y	^	mem_inst/n_19	NOR2BX1	0.044	0.164	1.003
mem_inst/g67690/B	^	mem_inst/n_19	NAND2XL	0.000	0.164	1.003
mem_inst/g67690/Y	v	mem_inst/n_47	NAND2XL	0.308	0.473	1.311
mem_inst/g67587/B	v	mem_inst/n_47	NOR2XL	0.003	0.476	1.315
mem_inst/g67587/Y	^	mem_inst/n_139	NOR2XL	0.549	1.024	1.863
mem_inst/mem_reg[3][8]340/S0	^	mem_inst/n_139	SMDFFHQX1	0.001	1.025	1.864
+-----+-----+-----+-----+-----+-----+-----+						
Clock Rise Edge 0.000						
= Beginpoint Arrival Time 0.000						
Other End Path:						
+-----+-----+-----+-----+-----+-----+						
Pin	Edge	Net	Cell	Delay	Arrival Time	Required Time
clk	^	clk			0.000	-0.839
mem_inst/mem_reg[3][8]340/CK	^	clk	SMDFFHQX1	0.000	0.000	-0.839
+-----+-----+-----+-----+-----+-----+-----+						

Figure 3.3.1: Setup Analysis of worst path

- Here, the timing arc for the worst setup path is from **pc_inst/pc_out_addr_reg[1]/Q (begin point)** to **mem_inst/mem_reg[3][8]340/S0 (end point)**.
- Arrival time = **1.025 ps**
- Required time = **1.864 ps**
- Slack calculated as the difference between required time and arrival time is **0.839**.
- Here, the **setup slack is positive**.

Hold Analysis:

```

# Generated by: Cadence Innovus 20.10-p004_1
# OS: Linux x86_64(Host ID edaserver4)
# Generated on: Wed Apr 17 12:41:48 2024
# Design: top8_module
# Command: timeDesign -postRoute -hold -pathReports -slackReports -numPaths 50 -prefix top8_module_postRoute -outDir 5postRoute_hold
#####
Path 1: MET Hold Check with Pin ff_alu_in1/q_reg[0]/CK
Endpoint: ff_alu_in1/q_reg[0]/SI (v) checked with leading edge of 'CLK'
Beginpoint: DFT_sdi_1 (v) triggered by leading edge of '@'
Path Groups: {CLK}
Analysis View: view1
Other End Arrival Time 0.000
+ Hold 0.051
+ Phase Shift 0.000
= Required Time 0.051
Arrival Time 0.059
Slack Time 0.007
Clock Rise Edge 0.000
+ Input Delay 0.000
= Beginpoint Arrival Time 0.000
Timing Path:
+-----+
| Pin | Edge | Net | Cell | Delay | Arrival | Required |
| | | | | Time | | Time |
+-----+
| DFT_sdi_1 | v | DFT_sdi_1 | | | 0.000 | -0.007 |
| ff_alu_in1/FE_PHC26_DFT_sdi_1/A | v | DFT_sdi_1 | DLY1X1 | 0.000 | 0.000 | -0.007 |
| ff_alu_in1/FE_PHC26_DFT_sdi_1/Y | v | ff_alu_in1/FE_PHN26_DFT_sdi_1 | DLY1X1 | 0.058 | 0.059 | 0.051 |
| ff_alu_in1/q_reg[0]/SI | v | ff_alu_in1/FE_PHN26_DFT_sdi_1 | SDFFQX1 | 0.000 | 0.059 | 0.051 |
+-----+

```

Figure 3.3.2: Hold Analysis of worst path

Here, the timing arc for the worst setup path is from **DFT_sdi_1 (begin point)** to **ff_alu_in1/q_reg[0] (end point)**.

- Arrival time = **0.059 ps**
- Required time = **0.051 ps**
- Slack calculated as the difference between required time and arrival time is **0.007**.
- Here, the **Hold slack is positive**

Area Analysis:

Hinst Name	Module Name	Inst Count	Total Area
<hr/>			
top8_module		1653	24027.790
alu_inst	alu	242	1140.648
decoder_inst	decoder	11	158.192
ff_alu_in1	ff_8bit	17	238.424
ff_carry_inst	ff_154	1	20.436
ff_negative_inst	ff_152	1	20.436
ff_pc_rst_inst	ff	2	24.978
ff_zero_inst	ff_153	1	20.436
ir_inst	instr_reg	11	158.192
mem_inst	instr_memory	1330	21831.267
pc_inst	pc	24	355.743

Figure 3.3.3: Area

The area is found to be $24027.790 \mu\text{m}^2$

GATE COUNT:

Gate area 2.2707 um^2				
Level 0 Module top8_module	Gates=10581	Cells=1653	Area=	24027.8 um^2
Level 1 Module alu_inst	Gates=502	Cells=242	Area=	1140.6 um^2
Level 1 Module ff_alu_in1	Gates=105	Cells=17	Area=	238.4 um^2
Level 1 Module mem_inst	Gates=9614	Cells=1330	Area=	21831.3 um^2
Level 1 Module pc_inst	Gates=156	Cells=24	Area=	355.7 um^2

Figure 3.3.4: Gate Count report

Number of total gates = 10581

Total number of cells = 1653

Gate area = $24027.8 \mu\text{m}^2$

Key observations:

The circuit after detailed routing contains 10581 gates implemented within 1653 cells. This translates to an average of approximately 6.4 gates per cell. This value suggests a relatively complex cell design, where each cell houses multiple gates. This approach might be a trade-off between area efficiency (achieved by using fewer cells) and logic functionality (accommodated by having more gates per cell)

Power Analysis:

Total Power						
Group	Internal Power	Switching Power	Leakage Power	Total Power	Percentage (%)	
Sequential	23.94	0.1158	0.2657	24.32	96.12	
Macro	0	0	0	0	0	
IO	0	0	0	0	0	
Combinational	0.2485	0.6987	0.03345	0.9806	3.876	
Clock (Combinational)	0	0	0	0	0	
Clock (Sequential)	0	0	0	0	0	
Total	24.19	0.8145	0.2992	25.3	100	
Rail	Voltage	Internal Power	Switching Power	Leakage Power	Total Power	Percentage (%)
Default	1.1	24.19	0.8145	0.2992	25.3	100
* Power Distribution Summary:						
* Highest Average Power: mem_inst/mem_reg[36][7]1065 (SMDFFHQX1): 0.03351						
* Highest Leakage Power: mem_inst/mem_reg[0][0]266 (SMDFFHQX1): 0.0003552						
* Total Cap: 2.58141e-11 F						
* Total instances in design: 1653						
* Total instances in design with no power: 0						
* Total instances in design with no activity: 0						
* Total Fillers and Decap: 0						

Figure 3.3.5: Power Analysis

Internal power = 24.19 mW

Switching power = 0.8145 mW

Leakage power = 0.0299 mW

Total power = 25.3 mW

Key observations:

The breakdown of power consumption reveals that internal power consumption dominates at a staggering 95.61%, highlighting the significance of optimizing internal cell structures for power efficiency. Conversely, leakage power contributes a minimal 0.12% to the total consumption, indicating efficient leakage control mechanisms within the circuit. While switching power accounts for the remaining 4.27%, further investigation might be beneficial to identify potential areas for reducing dynamic power consumption.

DRC Clean after post route:

Following a thorough design rule check (DRC), the circuit layout is now compliant.

We've ensured a manufacturable design by meticulously cleaning up the design rules.

```
#-report top8_module.drc.rpt          # string, default="", user setting
*** Starting Verify DRC (MEM: 1523.3) ***

VERIFY DRC ..... Starting Verification
VERIFY DRC ..... Initializing
VERIFY DRC ..... Deleting Existing Violations
VERIFY DRC ..... Creating Sub-Areas
VERIFY DRC ..... Using new threading
VERIFY DRC ..... Sub-Area: {0.000 0.000 115.200 115.200} 1 of 4
VERIFY DRC ..... Sub-Area : 1 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {115.200 0.000 230.260 115.200} 2 of 4
VERIFY DRC ..... Sub-Area : 2 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {0.000 115.200 115.200 227.360} 3 of 4
VERIFY DRC ..... Sub-Area : 3 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {115.200 115.200 230.260 227.360} 4 of 4
VERIFY DRC ..... Sub-Area : 4 complete 0 Viols.

Verification Complete : 0 Viols.

*** End Verify DRC (CPU: 0:00:00.5  ELAPSED TIME: 0.00  MEM: 0.0M) ***
```

Figure 3.3.6: DRC report after routing

Layout:

Following floorplanning, power grid design, standard cell placement, clock tree synthesis, and routing, this is the finalized integrated circuit layout.

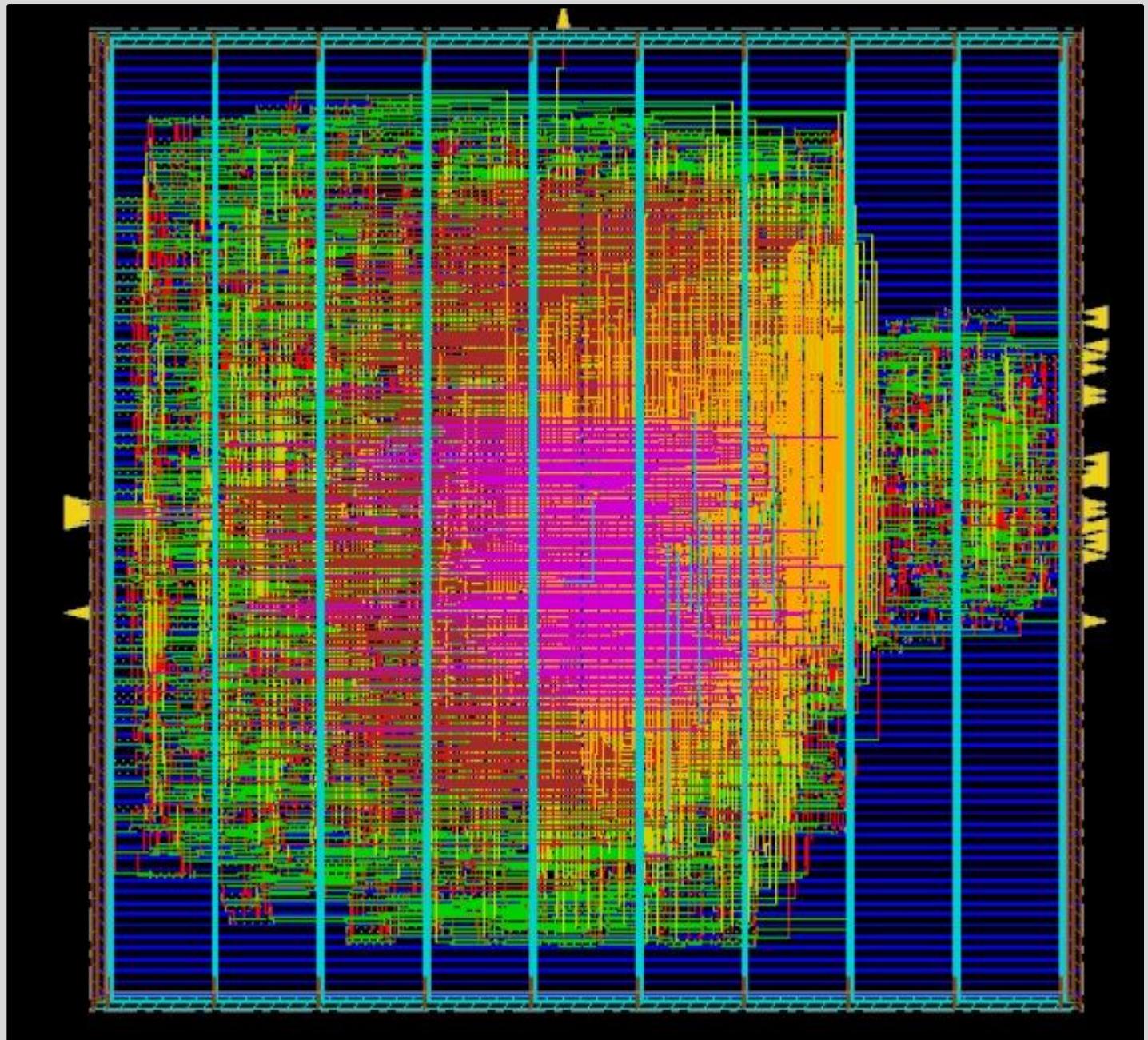


Figure 3.3.7: Layout with the 0.5 utilization factor

Layout with fly-lines:

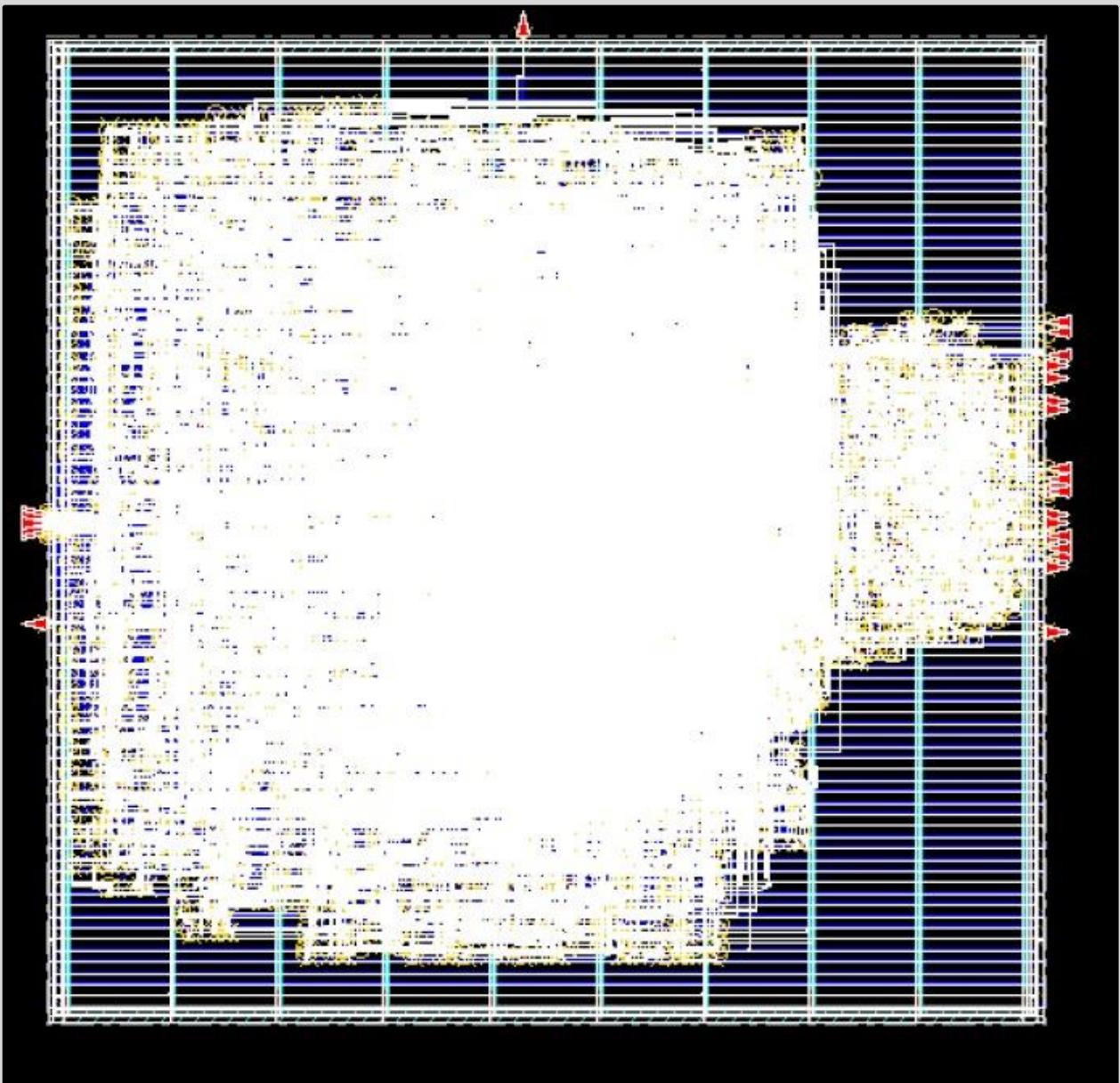


Figure 3.3.8: Snapshot of fly-lines in the layout

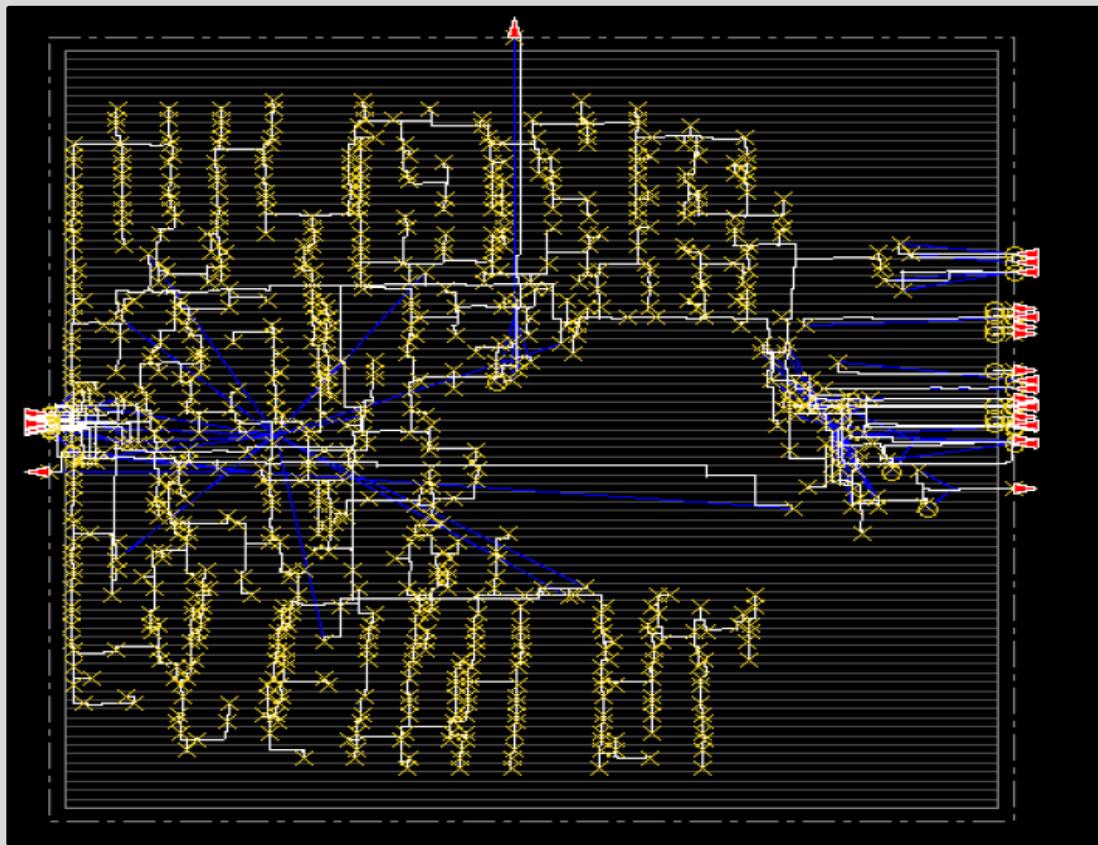
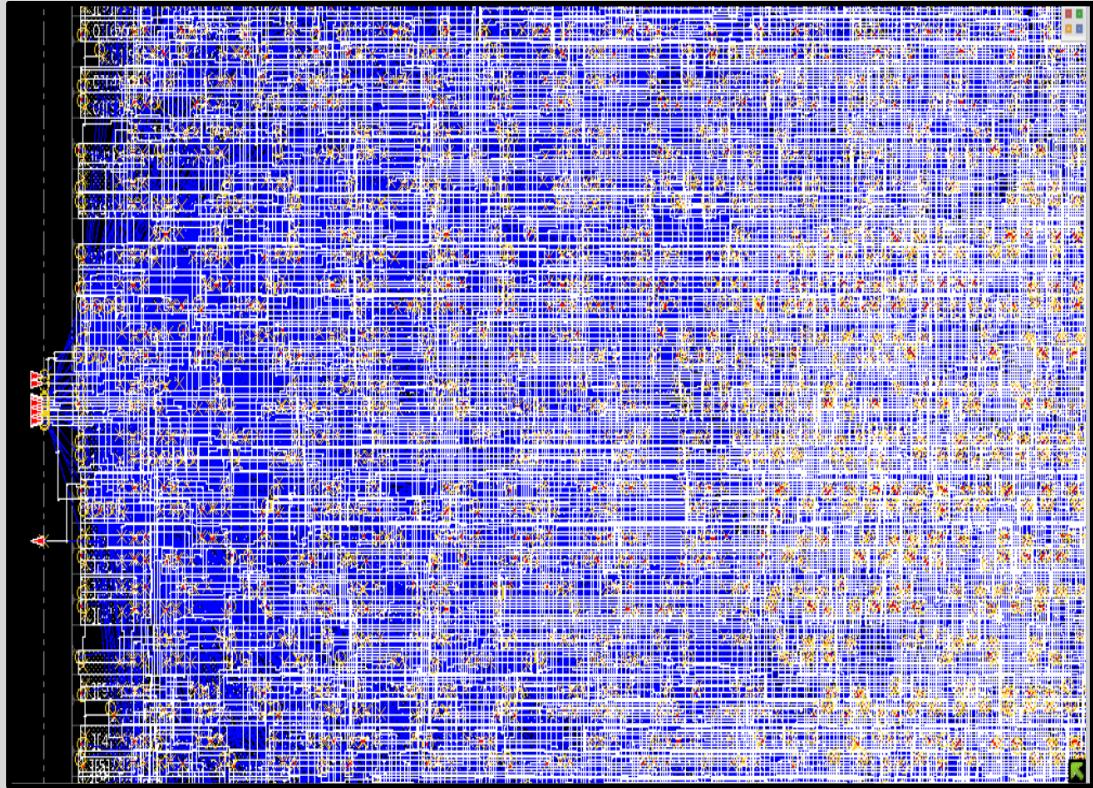
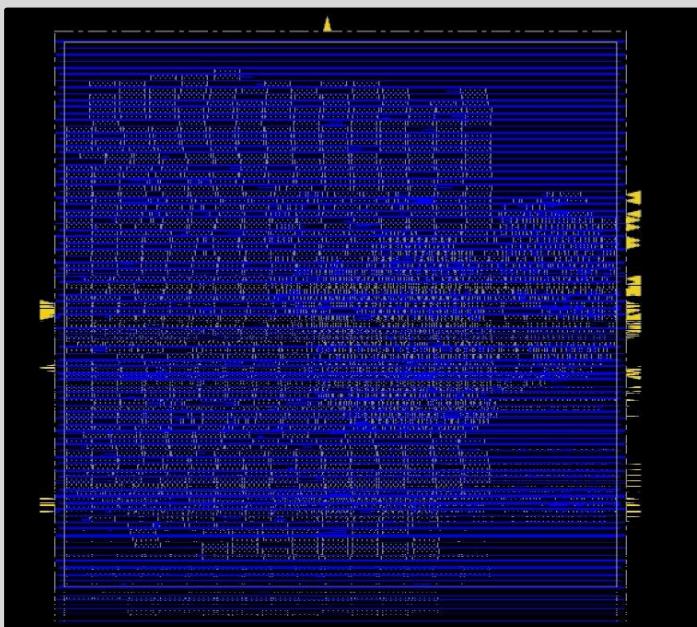


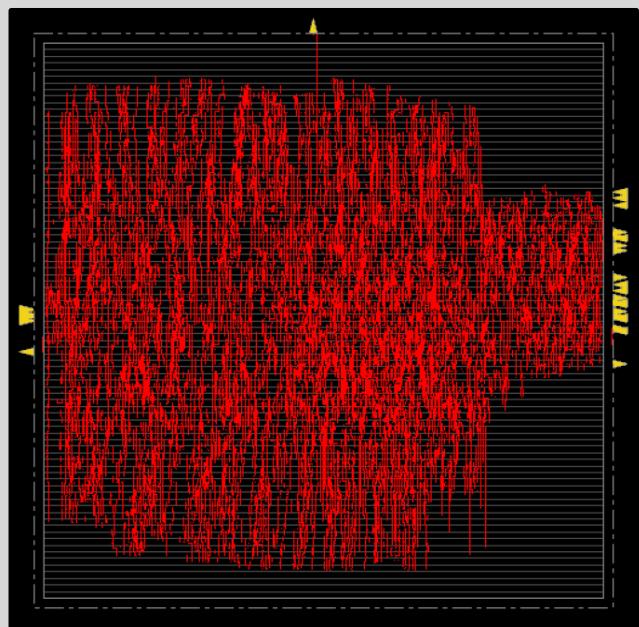
Figure 3.3.9: Close look at the fly-lines in the design

Metal layers along with standard cells:

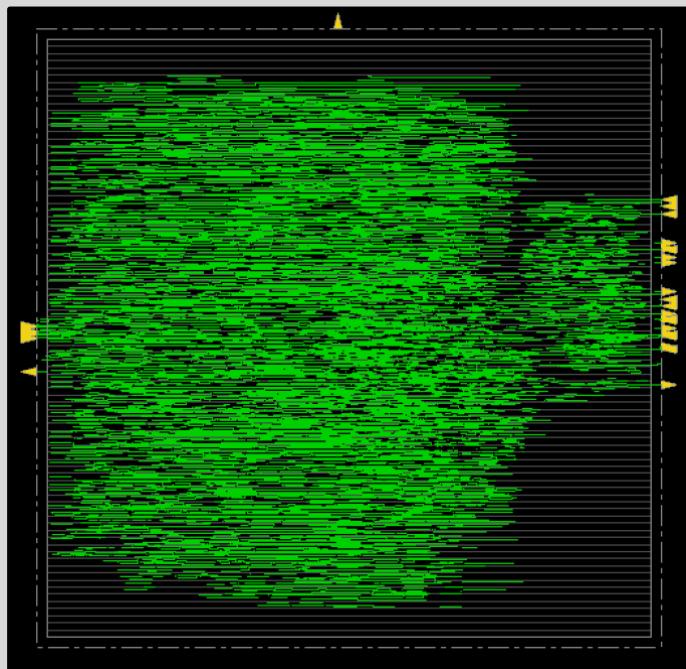
Metal 1



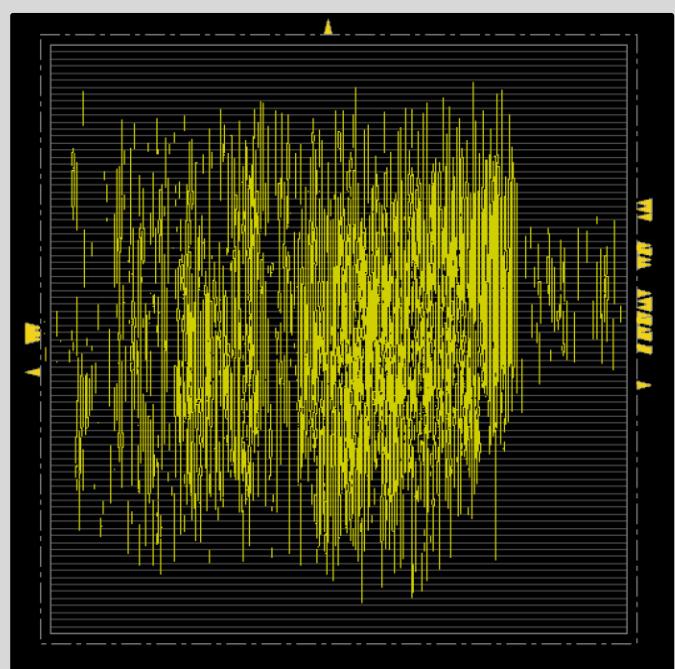
Metal 2



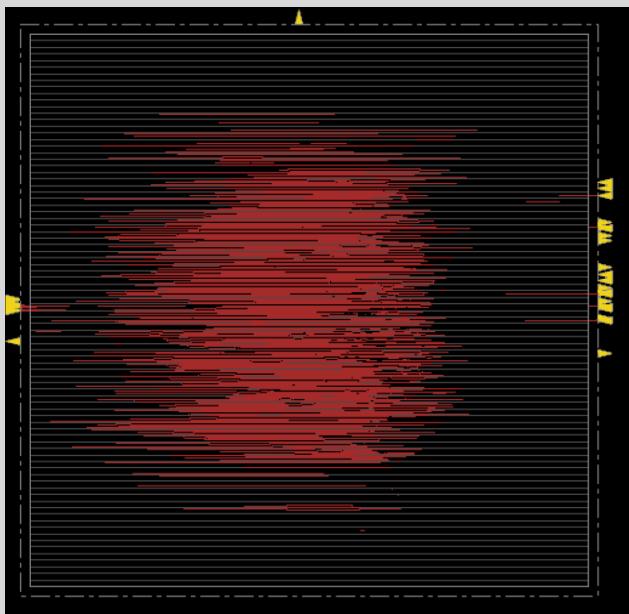
Metal 3



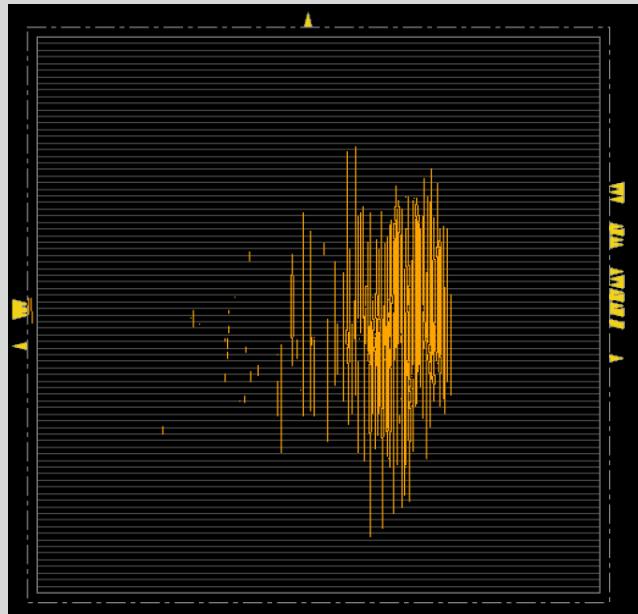
Metal 4



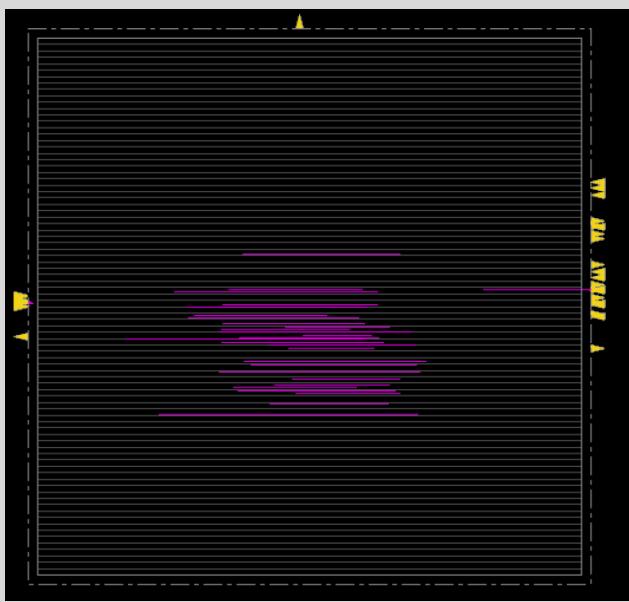
Metal 5



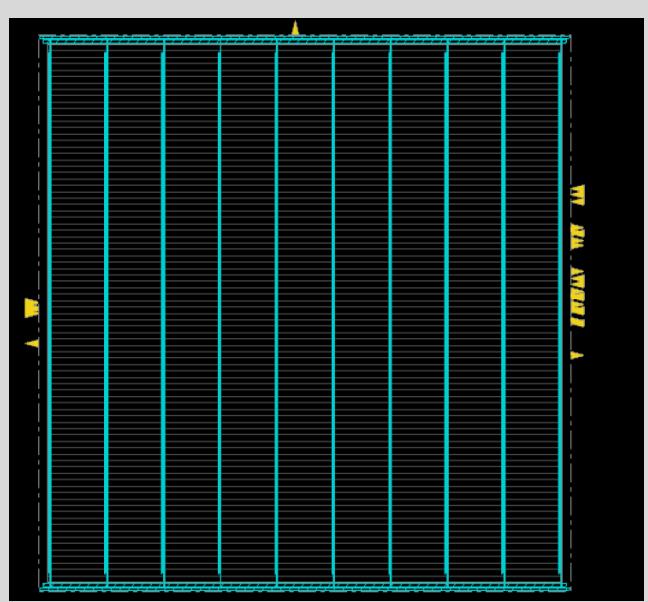
Metal 6



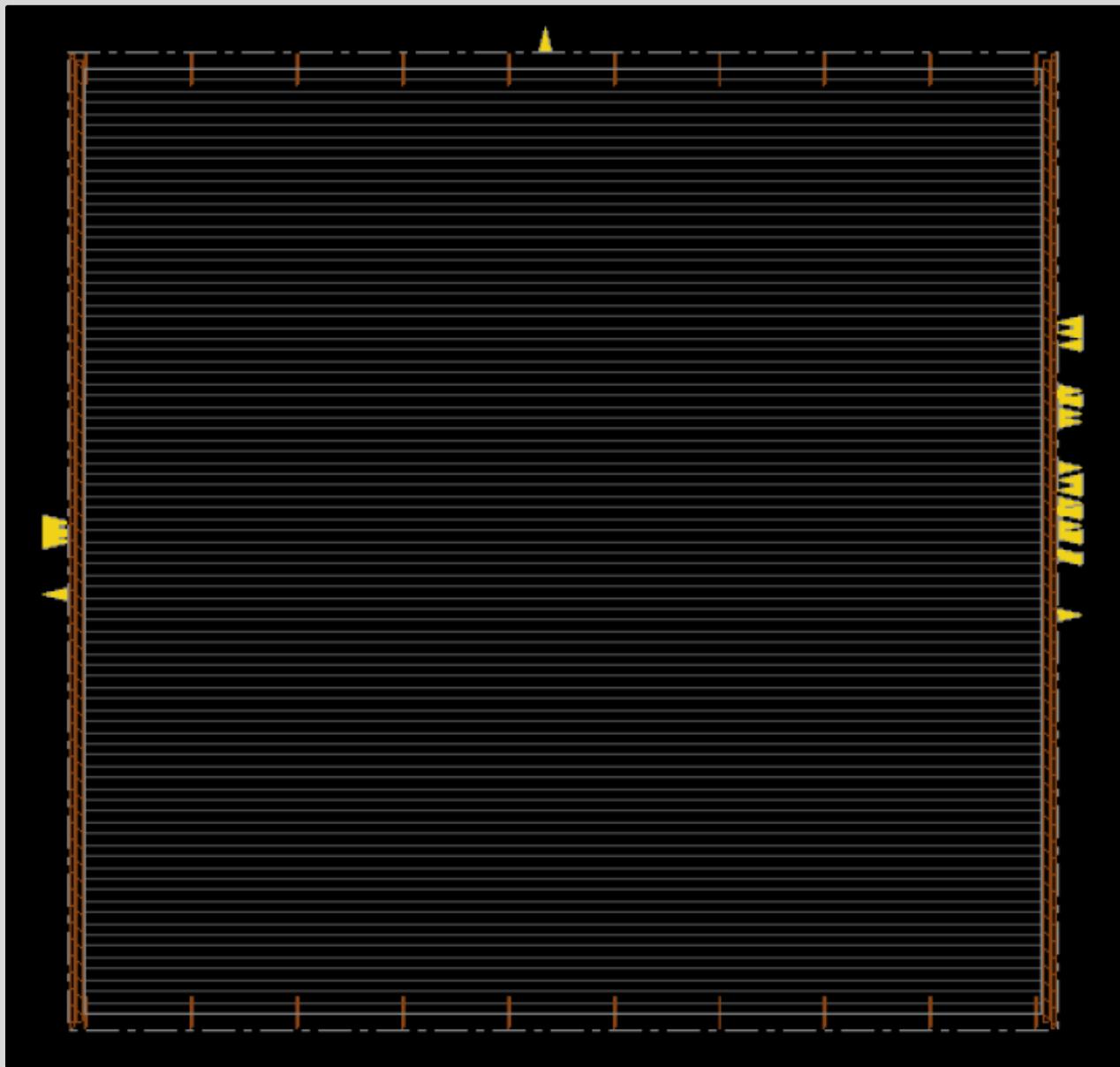
Metal 7



Metal 8



Metal 9



4. For 80 % Core Utilization factor

4.1 After Placement

Setup Analysis:

```

Path 1: MET Setup Check with Pin mem_inst/mem_reg[21][10]738/CK
Endpoint: mem_inst/mem_reg[21][10]738/S0 (^) checked with leading edge of
'CLK'
Beginpoint: rst (v) triggered by leading edge of
'CLK'
Path Groups: {CLK}
Analysis View: view1
Other End Arrival Time 0.000
- Setup 0.136
+ Phase Shift 2.000
= Required Time 1.864
- Arrival Time 1.400
= Slack Time 0.464
Clock Rise Edge 0.000
+ Input Delay 0.400
= Beginpoint Arrival Time 0.400
Timing Path:
+-----+-----+-----+-----+-----+-----+-----+
| Pin | Edge | Net | Cell | Delay | Arrival | Required |
|     |      |     |     |       | Time   | Time    |
+-----+-----+-----+-----+-----+-----+-----+
| rst | v   | rst | NOR2XL | 0.000 | 0.400 | 0.864 |
| mem_inst/g67717/B | v   | rst | NOR2XL | 0.166 | 0.400 | 0.864 |
| mem_inst/g67717/Y | ^   | mem_inst/n_18 | NOR2XL | 0.166 | 0.566 | 1.030 |
| mem_inst/g67689/A | ^   | mem_inst/n_18 | NAND2XL | 0.000 | 0.567 | 1.031 |
| mem_inst/g67689/Y | ^   | mem_inst/n_49 | NAND2XL | 0.292 | 0.859 | 1.323 |
| mem_inst/g67643/B | v   | mem_inst/n_49 | NOR2XL | 0.002 | 0.860 | 1.324 |
| mem_inst/g67643/Y | ^   | mem_inst/n_83 | NOR2XL | 0.538 | 1.399 | 1.863 |
| mem_inst/mem_reg[21][10]738/S0 | ^   | mem_inst/n_83 | SMDFFHQX1 | 0.002 | 1.400 | 1.864 |
+-----+-----+-----+-----+-----+-----+-----+
Clock Rise Edge 0.000
= Beginpoint Arrival Time 0.000
Other End Path:
+-----+-----+-----+-----+-----+-----+
| Pin | Edge | Net | Cell | Delay | Arrival | Required |
|     |      |     |     |       | Time   | Time    |
+-----+-----+-----+-----+-----+-----+
| clk | ^   | clk | SMDFFHQX1 | 0.000 | 0.000 | -0.464 |
| mem_inst/mem_reg[21][10]738/CK | ^   | clk | SMDFFHQX1 | 0.000 | 0.000 | -0.464 |
+-----+-----+-----+-----+-----+-----+

```

Figure 4.3.1.1: Setup Analysis of worth path

- Here, the timing arc for the worst setup path is from **rst (begin point)** to **mem_inst/mem_reg[21][10]738/S0 (end point)**.
- Arrival time = **1.400**
- Required time = **1.864**
- Slack calculated as the difference between required time and arrival time is **0.464**
- Here, the **setup slack is positive**.

Hold Analysis:

```

Path 1: VIOLATED Hold Check with Pin ff_alu_in1/q_reg[1]/CK
Endpoint: ff_alu_in1/q_reg[1]/D (^) checked with leading edge of 'CLK'
Beginpoint: alu_in1_inp[1] (^) triggered by leading edge of '@'
Path Groups: {CLK}
Analysis View: view1
Other End Arrival Time      0.000
+ Hold                      0.103
+ Phase Shift                0.000
= Required Time              0.103
Arrival Time                 0.000
Slack Time                  -0.103
Clock Rise Edge              0.000
+ Input Delay                0.000
= Beginpoint Arrival Time   0.000
Timing Path:
+-----+
|   Pin    | Edge | Net        | Cell | Delay | Arrival | Required |
|          |      |            |      |       | Time    | Time     |
+-----+
| alu_in1_inp[1] | ^  | alu_in1_inp[1] |      |       | 0.000  | 0.103  |
| ff_alu_in1/q_reg[1]/D | ^  | alu_in1_inp[1] | SDFFQX1 | 0.000 | 0.000  | 0.103  |
+-----+
Clock Rise Edge              0.000
= Beginpoint Arrival Time   0.000
Other End Path:
+-----+
|   Pin    | Edge | Net        | Cell | Delay | Arrival | Required |
|          |      |            |      |       | Time    | Time     |
+-----+
| clk      | ^  | clk        |      |       | 0.000  | -0.103 |
| ff_alu_in1/q_reg[1]/CK | ^  | clk        | SDFFQX1 | 0.000 | 0.000  | -0.103 |
+-----+

```

Figure 4.1.1: Hold Analysis of worth path

- Here, the timing arc for the worst setup path is from **alu_in1_inp[1]** (begin point) to **ff_alu_in1/q_reg[1]/D** (end point).
- Arrival time = **0.000**
- Required time = **0.103**
- Slack calculated as the difference between required time and arrival time is **-0.103**.
- Here, the **Hold slack is negative.{Violated prior to CTS}**

Area Analysis:

Hinst Name	Module Name	Inst Count	Total Area
<hr/>			
top8_module		1670	24320.711
alu_inst	alu	242	1140.648
decoder_inst	decoder	11	158.192
ff_alu_in1	ff_8bit	8	163.490
ff_carry_inst	ff_154	1	20.436
ff_negative_inst	ff_152	1	20.436
ff_pc_rst_inst	ff	2	24.978
ff_zero_inst	ff_153	1	20.436
ir_inst	instr_reg	11	158.192
mem_inst	instr_memory	1369	22258.158
pc_inst	pc	24	355.743

Figure 4.1.2: Area AnalysisPost Placement , Total Area = 24320.711 μm^2 .

Power Analysis:

Total Power					
Group	Internal Power	Switching Power	Leakage Power	Total Power	Percentage (%)
Sequential	31.61	0.5487	0.2657	32.42	96.49
Macro	0	0	0	0	0
IO	0	0	0	0	0
Combinational	0.5535	0.5926	0.03224	1.178	3.507
Clock (Combinational)	0	0	0	0	0
Clock (Sequential)	0	0	0	0	0
Total	32.16	1.141	0.2979	33.6	100

Figure 4.1.3: Power Analysis

- Internal power dissipation refers to the power that is consumed within the boundaries of a digital cell during its operation. This power is primarily due to the charging and discharging of internal capacitances within the cell as signals transition between logic states (0 and 1).

Internal power = 32.16 mW

- Switching power refers to the power dissipated specifically due to the charging and discharging of the load capacitance at the output of the cell.

Switching power = 1.141mW

- Leakage power refers to the power consumed by a digital circuit when there is no switching activity, primarily due to the leakage current that flows from the power supply (VDD) to ground (GND) through the transistors in the circuit.

Leakage power = 0.2979mW

Total power = 33.6 mW

GATE COUNT:

Gate area 2.2707 um^2			
Level 0 Module top8_module	Gates=10710	Cells=1670	Area= 24320.7 um^2
Level 1 Module alu_inst	Gates=502	Cells=242	Area= 1140.6 um^2
Level 1 Module mem_inst	Gates=9802	Cells=1369	Area= 22258.2 um^2
Level 1 Module pc_inst	Gates=156	Cells=24	Area= 355.7 um^2

Figure 4.1.4: Gate Count

- **Number of total gates = 10710**
- **Total number of cells = 1670**
- **Gate area = 2.2707 um^2**

Standard Cell location and Placement Strategy:

Cell placement and pathway configuration depend on factors like power availability, timing, and interconnection length. Cell arrangement affects wire lengths; closer placement may lead to timing violations, while farther placement increases routing resources and latency. Components are placed on the die based on floor layout and criteria such as timing specifications and connections between cells. Strongly connected instances are usually grouped to conserve resources. See below for the layout of the post-placement core, featuring only standard cells.

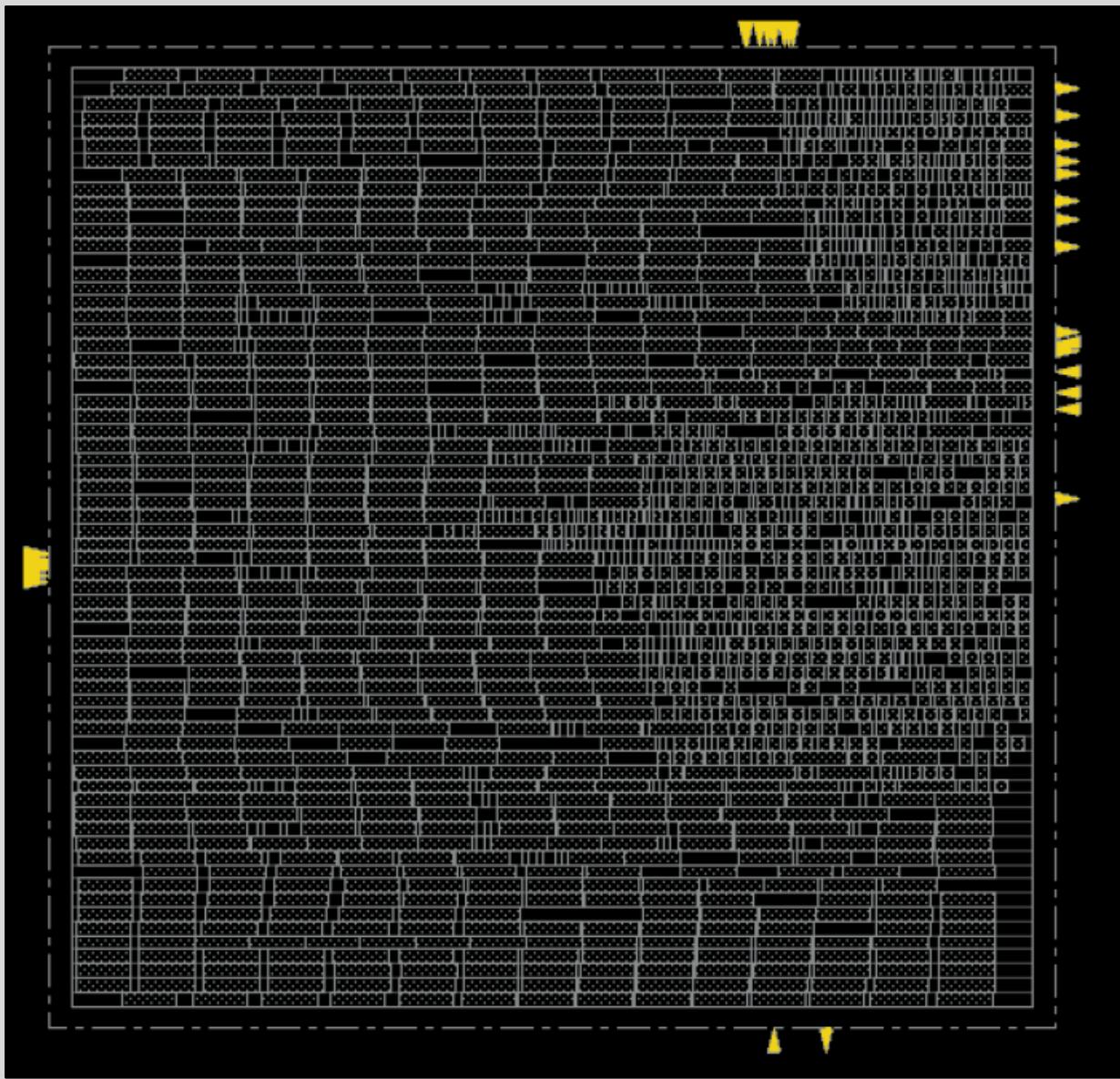


Figure 4.1.5: Standard cells placement

4.2 After Clock Tree synthesis

Setup Analysis

```

Path 1: MET Setup Check with Pin mem_inst/mem_reg[21][10]738/CK
Endpoint: mem_inst/mem_reg[21][10]738/S0 (^) checked with leading edge of
'CLK'
Beginpoint: rst (v) triggered by leading edge of
'CLK'
Path Groups: {CLK}
Analysis View: view1
Other End Arrival Time 0.000
- Setup 0.136
+ Phase Shift 2.000
= Required Time 1.864
- Arrival Time 1.395
= Slack Time 0.470
Clock Rise Edge 0.000
+ Input Delay 0.400
= Beginpoint Arrival Time 0.400
Timing Path:
+-----+
| Pin | Edge | Net | Cell | Delay | Arrival | Required |
|     |     |     |     |       | Time   | Time    |
+-----+
| rst | v   | rst |      |       | 0.400 | 0.870 |
| mem_inst/g67717/B | v   | rst | NOR2XL | 0.000 | 0.400 | 0.870 |
| mem_inst/g67717/Y | ^   |      | NOR2XL | 0.162 | 0.562 | 1.032 |
| mem_inst/g67689/A | ^   | mem_inst/n_18 | NOR2XL | 0.000 | 0.563 | 1.033 |
| mem_inst/g67689/Y | v   | mem_inst/n_18 | NAND2XL | 0.290 | 0.853 | 1.323 |
| mem_inst/g67643/B | v   | mem_inst/n_49 | NAND2XL | 0.002 | 0.855 | 1.325 |
| mem_inst/g67643/Y | ^   | mem_inst/n_49 | NOR2XL | 0.538 | 1.393 | 1.863 |
| mem_inst/mem_reg[21][10]738/S0 | ^   | mem_inst/n_83 | SMDFFHQX1 | 0.002 | 1.395 | 1.864 |
+-----+
Clock Rise Edge 0.000
= Beginpoint Arrival Time 0.000
Other End Path:
+-----+
| Pin | Edge | Net | Cell | Delay | Arrival | Required |
|     |     |     |     |       | Time   | Time    |
+-----+
| clk | ^   | clk |      |       | 0.000 | -0.470 |
| mem_inst/mem_reg[21][10]738/CK | ^   | clk | SMDFFHQX1 | 0.000 | 0.000 | -0.470 |
+-----+

```

Figure 4.2.1: Setup Analysis of worst path

- Here, the timing arc for the worst setup path is from **rst (begin point)** to **mem_inst/mem_reg[21][10]738/S0 (output port)**.
- The arrival time is **1.395ps**, the required time is **1.864ps** and the slack calculated as the difference between required time and arrival time is **0.470**.
- Here, the **setup slack is positive**.

Effect on setup slack after CTS:

Before CTS

```

Path 1: MET Setup Check with Pin mem_inst/mem_reg[21][10]738/CK
Endpoint: mem_inst/mem_reg[21][10]738/S0 (^) checked with leading edge of
'CLK'
Beginpoint: rst (v) triggered by leading edge of
'CLK'
Path Groups: {CLK}
Analysis View: view1
Other End Arrival Time 0.000
- Setup 0.136
+ Phase Shift 2.000
= Required Time 1.864
- Arrival Time 1.400
= Slack Time 0.464
Clock Rise Edge 0.000
+ Input Delay 0.400
= Beginpoint Arrival Time 0.400
Timing Path:
+-----+
| Pin | Edge | Net | Cell | Delay | Arrival | Required |
|-----+-----+-----+-----+-----+-----+-----+
| rst | v | rst | NOR2XL | 0.000 | 0.400 | 0.864 |
| mem_inst/g67717/B | v | rst | NOR2XL | 0.400 | 0.864 |
| mem_inst/g67717/Y | ^ | mem_inst/n_18 | NOR2XL | 0.166 | 0.566 | 1.030 |
| mem_inst/g67689/A | ^ | mem_inst/n_18 | NAND2XL | 0.000 | 0.567 | 1.031 |
| mem_inst/g67689/Y | v | mem_inst/n_49 | NAND2XL | 0.292 | 0.859 | 1.323 |
| mem_inst/g67643/B | v | mem_inst/n_49 | NOR2XL | 0.002 | 0.860 | 1.324 |
| mem_inst/g67643/Y | ^ | mem_inst/n_83 | NOR2XL | 0.538 | 1.399 | 1.863 |
| mem_inst/mem_reg[21][10]738/S0 | ^ | mem_inst/n_83 | SMDFHQQX1 | 0.002 | 1.400 | 1.864 |
+-----+
Clock Rise Edge 0.000
= Beginpoint Arrival Time 0.000
Other End Path:
+-----+
| Pin | Edge | Net | Cell | Delay | Arrival | Required |
|-----+-----+-----+-----+-----+-----+-----+
| clk | ^ | clk | NOR2XL | 0.000 | 0.000 | -0.464 |
| mem_inst/mem_reg[21][10]738/CK | ^ | clk | SMDFHQQX1 | 0.000 | 0.000 | -0.464 |
+-----+

```

Slack time = 0.464 ps

After CTS

```

Path 1: MET Setup Check with Pin mem_inst/mem_reg[21][10]738/CK
Endpoint: mem_inst/mem_reg[21][10]738/S0 (^) checked with leading edge of
'CLK'
Beginpoint: rst (v) triggered by leading edge of
'CLK'
Path Groups: {CLK}
Analysis View: view1
Other End Arrival Time 0.000
- Setup 0.136
+ Phase Shift 2.000
= Required Time 1.864
- Arrival Time 1.395
= Slack Time 0.470
Clock Rise Edge 0.000
+ Input Delay 0.400
= Beginpoint Arrival Time 0.400
Timing Path:
+-----+
| Pin | Edge | Net | Cell | Delay | Arrival | Required |
|-----+-----+-----+-----+-----+-----+-----+
| rst | v | rst | NOR2XL | 0.000 | 0.400 | 0.870 |
| mem_inst/g67717/B | v | rst | NOR2XL | 0.400 | 0.870 |
| mem_inst/g67717/Y | ^ | mem_inst/n_18 | NOR2XL | 0.162 | 0.562 | 1.032 |
| mem_inst/g67689/A | ^ | mem_inst/n_18 | NAND2XL | 0.000 | 0.563 | 1.033 |
| mem_inst/g67689/Y | v | mem_inst/n_49 | NAND2XL | 0.296 | 0.853 | 1.323 |
| mem_inst/g67643/B | v | mem_inst/n_49 | NOR2XL | 0.002 | 0.855 | 1.325 |
| mem_inst/g67643/Y | ^ | mem_inst/n_83 | NOR2XL | 0.538 | 1.393 | 1.863 |
| mem_inst/mem_reg[21][10]738/S0 | ^ | mem_inst/n_83 | SMDFHQQX1 | 0.002 | 1.395 | 1.864 |
+-----+
Clock Rise Edge 0.000
= Beginpoint Arrival Time 0.000
Other End Path:
+-----+
| Pin | Edge | Net | Cell | Delay | Arrival | Required |
|-----+-----+-----+-----+-----+-----+-----+
| clk | ^ | clk | NOR2XL | 0.000 | 0.000 | -0.470 |
| mem_inst/mem_reg[21][10]738/CK | ^ | clk | SMDFHQQX1 | 0.000 | 0.000 | -0.470 |
+-----+

```

Slack time = 0.470 ps

After CTS, AT increases due to insertion of buffers etc in the path. So slack increases.

Hold Analysis

Path 1: MET Hold Check with Pin ff_alu_in1/q_reg[0]/CK							
Endpoint: ff_alu_in1/q_reg[0]/SI (v) checked with leading edge of 'CLK'							
Beginpoint: DFT_sdi_1 (v) triggered by leading edge of '@'							
Path Groups: {CLK}							
Analysis View: view1							
Other End Arrival Time	0.000						
+ Hold	0.053						
+ Phase Shift	0.000						
= Required Time	0.053						
Arrival Time	0.060						
Slack Time	0.008						
Clock Rise Edge	0.000						
+ Input Delay	0.000						
= Beginpoint Arrival Time	0.000						
Timing Path:							
	Pin	Edge	Net	Cell	Delay	Arrival Time	Required Time
DFT_sdi_1	v	DFT_sdi_1				0.000	-0.008
ff_alu_in1/FE_PHC25_DFT_sdi_1/A	v	DFT_sdi_1	DLY1X1	0.000	0.000	-0.008	
ff_alu_in1/FE_PHC25_DFT_sdi_1/Y	v	ff_alu_in1/FE_PHN25_DFT_sdi_1	DLY1X1	0.060	0.060	0.053	
ff_alu_in1/q_reg[0]/SI	v	ff_alu_in1/FE_PHN25_DFT_sdi_1	SDFFQX1	0.000	0.060	0.053	
Clock Rise Edge	0.000						
= Beginpoint Arrival Time	0.000						
Other End Path:							
	Pin	Edge	Net	Cell	Delay	Arrival Time	Required Time
clk	^	clk			0.000	0.008	
ff_alu_in1/q_reg[0]/CK	^	clk	SDFFQX1	0.000	0.000	0.008	

Figure 4.2.2: Hold Analysis of worst path

- Here, the worst path for the hold slack is from **DFT_sdi1 (begin point)** to **ff_alu_in1/q_reg[0]/SI**.
- The arrival time is **0.060 ps**, the required time is **0.053 ps** and the slack calculated as the difference between required time and arrival time is **0.008**.
- Here, the **hold slack is positive**.

Effect on hold slack after CTS:

Before CTS

```

Path 1: VIOLATED Hold Check with Pin ff_alu_in1/q_reg[1]/CK
Endpoint: ff_alu_in1/q_reg[1]/D (^) checked with leading edge of 'CLK'
Beginpoint: alu_in1_inp[1] (^) triggered by leading edge of '@'
Path Groups: {CLK}
Analysis View: view1
Other End Arrival Time      0.000
+ Hold                      0.103
+ Phase Shift                0.000
= Required Time              0.103
Arrival Time                 0.000
Slack Time                  -0.103
Clock Rise Edge              0.000
+ Input Delay                0.000
= Beginpoint Arrival Time    0.000
Timing Path:
+-----+-----+-----+-----+-----+
|   Pin | Edge | Net | Cell | Delay | Arrival | Required |
|       |     |     |     |     | Time | Time |
+-----+-----+-----+-----+-----+
| alu_in1_inp[1] | ^ | alu_in1_inp[1] |     | 0.000 | 0.103 |
| ff_alu_in1/q_reg[1]/D | ^ | alu_in1_inp[1] | SDFQX1 | 0.000 | 0.000 | 0.103 |
+-----+-----+-----+-----+-----+
Clock Rise Edge              0.000
= Beginpoint Arrival Time    0.000
Other End Path:
+-----+-----+-----+-----+-----+
|   Pin | Edge | Net | Cell | Delay | Arrival | Required |
|       |     |     |     |     | Time | Time |
+-----+-----+-----+-----+-----+
| clk | ^ | clk |     | 0.000 | -0.103 |
| ff_alu_in1/q_reg[1]/CK | ^ | clk | SDFQX1 | 0.000 | 0.000 | -0.103 |
+-----+-----+-----+-----+-----+

```

After CTS

```

Path 1: MET Hold Check with Pin ff_alu_in1/q_reg[0]/CK
Endpoint: ff_alu_in1/q_reg[0]/SI (v) checked with leading edge of 'CLK'
Beginpoint: DFT_sdi_1 (v) triggered by leading edge of '@'
Path Groups: {CLK}
Analysis View: view1
Other End Arrival Time      0.000
+ Hold                      0.053
+ Phase Shift                0.000
= Required Time              0.053
Arrival Time                 0.060
Slack Time                  0.008
Clock Rise Edge              0.000
+ Input Delay                0.000
= Beginpoint Arrival Time    0.000
Timing Path:
+-----+-----+-----+-----+-----+
|   Pin | Edge | Net | Cell | Delay | Arrival | Required |
|       |     |     |     |     | Time | Time |
+-----+-----+-----+-----+-----+
| DFT_sdi_1 | v | DFT_sdi_1 |     | 0.000 | -0.008 |
| ff_alu_in1/FE_PHC25_DFT_sdi_1/A | v | DFT_sdi_1 |     | 0.000 | -0.008 |
| ff_alu_in1/FE_PHC25_DFT_sdi_1/Y | v | ff_alu_in1/FE_PHN25_DFT_sdi_1 | DLY1X1 | 0.060 | 0.053 |
| ff_alu_in1/q_reg[0]/SI | v | ff_alu_in1/FE_PHN25_DFT_sdi_1 | DLY1X1 | 0.060 | 0.053 |
+-----+-----+-----+-----+-----+
Clock Rise Edge              0.000
= Beginpoint Arrival Time    0.000
Other End Path:
+-----+-----+-----+-----+-----+
|   Pin | Edge | Net | Cell | Delay | Arrival | Required |
|       |     |     |     |     | Time | Time |
+-----+-----+-----+-----+-----+
| clk | ^ | clk |     | 0.000 | 0.008 |
| ff_alu_in1/q_reg[0]/CK | ^ | clk | SDFQX1 | 0.000 | 0.000 | 0.008 |
+-----+-----+-----+-----+-----+

```

Slack time = -0.103 ps

Slack time = 0.008 ps

One thing to observe is that the worst hold path before CTS and after CTS has not remained the same. The hold slack improved as the AT reduced drastically due to optimization done at the end of the stage.

Area Analysis:

Hinst Name	Module Name	Inst Count	Total Area
<hr/>			
top8_module		1461	22928.772
alu_inst	alu	242	1140.648
decoder_inst	decoder	11	158.192
ff_alu_in1	ff_8bit	17	238.424
ff_carry_inst	ff_154	1	20.436
ff_negative_inst	ff_152	1	20.436
ff_pc_rst_inst	ff	2	24.978
ff_zero_inst	ff_153	1	20.436
ir_inst	instr_reg	11	158.192
mem_inst	instr_memory	1135	20714.082
pc_inst	pc	24	355.743

Figure 4.2.3: Area Analysis

The area is found to be **22928.772 μm^2**

Effect on area after CTS:

Before CTS				After CTS			
Hinst Name	Module Name	Inst Count	Total Area	Hinst Name	Module Name	Inst Count	Total Area
top8_module		1670	24320.711	top8_module		1461	22928.772
alu_inst	alu	242	1140.648	alu_inst	alu	242	1140.648
decoder_inst	decoder	11	158.192	decoder_inst	decoder	11	158.192
ff_alu_in1	ff_8bit	8	163.490	ff_alu_in1	ff_8bit	17	238.424
ff_carry_inst	ff_154	1	20.436	ff_carry_inst	ff_154	1	20.436
ff_negative_inst	ff_152	1	20.436	ff_negative_inst	ff_152	1	20.436
ff_pc_rst_inst	ff	2	24.978	ff_pc_rst_inst	ff	2	24.978
ff_zero_inst	ff_153	1	20.436	ff_zero_inst	ff_153	1	20.436
ir_inst	instr_reg	11	158.192	ir_inst	instr_reg	11	158.192
mem_inst	instr_memory	1369	22258.158	mem_inst	instr_memory	1135	20714.082
pc_inst	pc	24	355.743	pc_inst	pc	24	355.743
Area = 24328.711 μm^2				Area = 22928.772 μm^2			

Since optimization is also done, Area significantly reduced even after doing Clock Tree Synthesis.

Power Analysis:

Total Power					
Group percentage)	Internal Power	Switching Power	Leakage Power	Total Power	Pe (%)
Sequential 96.26	23.91	0.1162	0.2657	24.29	
Macro 0	0	0	0	0	
IO 0	0	0	0	0	
Combinational 3.739	0.242	0.6745	0.02709	0.9436	
Clock (Combinational) 0	0	0	0	0	
Clock (Sequential) 0	0	0	0	0	
Total 100	24.15	0.7907	0.2928	25.23	

Figure 4.2.4: Power Analysis

Internal power = 24.15 mW

Switching power = 0.7907 mW

Leakage power = 0.2928 mW

Total power = 25.23 mW

Effect on power after CTS:

Before CTS					After CTS																																																																																				
Total Power <hr/> Total Internal Power: 32.16400503 95.7169% Total Switching Power: 1.14132112 3.3965% Total Leakage Power: 0.29793861 0.8866% Total Power: 33.60326433					Total Power <hr/> Total Internal Power: 24.14951476 95.7062% Total Switching Power: 0.79865488 3.1334% Total Leakage Power: 0.29278875 1.1603% Total Power: 25.23295799																																																																																				
<table border="1"> <thead> <tr> <th>Group</th> <th>Internal Power</th> <th>Switching Power</th> <th>Leakage Power</th> <th>Total Power (%)</th> </tr> </thead> <tbody> <tr> <td>Sequential</td> <td>31.61</td> <td>0.5487</td> <td>0.2657</td> <td>32.42 96.49</td> </tr> <tr> <td>Macro</td> <td>0</td> <td>0</td> <td>0</td> <td>0 0</td> </tr> <tr> <td>IO</td> <td>0</td> <td>0</td> <td>0</td> <td>0 0</td> </tr> <tr> <td>Combinational</td> <td>0.5535</td> <td>0.5926</td> <td>0.03224</td> <td>1.178 3.507</td> </tr> <tr> <td>Clock (Combinational)</td> <td>0</td> <td>0</td> <td>0</td> <td>0 0</td> </tr> <tr> <td>Clock (Sequential)</td> <td>0</td> <td>0</td> <td>0</td> <td>0 0</td> </tr> <tr> <td>Total</td> <td>32.16</td> <td>1.141</td> <td>0.2979</td> <td>33.6 100</td> </tr> </tbody> </table>					Group	Internal Power	Switching Power	Leakage Power	Total Power (%)	Sequential	31.61	0.5487	0.2657	32.42 96.49	Macro	0	0	0	0 0	IO	0	0	0	0 0	Combinational	0.5535	0.5926	0.03224	1.178 3.507	Clock (Combinational)	0	0	0	0 0	Clock (Sequential)	0	0	0	0 0	Total	32.16	1.141	0.2979	33.6 100	<table border="1"> <thead> <tr> <th>Group Percentage)</th> <th>Internal Power</th> <th>Switching Power</th> <th>Leakage Power</th> <th>Total Pe Power (%)</th> </tr> </thead> <tbody> <tr> <td>Sequential 96.26</td> <td>23.91</td> <td>0.1162</td> <td>0.2657</td> <td>24.29</td> </tr> <tr> <td>Macro 0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>IO 0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>Combinational 3.739</td> <td>0.242</td> <td>0.6745</td> <td>0.02709</td> <td>0.9436</td> </tr> <tr> <td>Clock (Combinational) 0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>Clock (Sequential) 0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>Total 100</td> <td>24.15</td> <td>0.7907</td> <td>0.2928</td> <td>25.23</td> </tr> </tbody> </table>					Group Percentage)	Internal Power	Switching Power	Leakage Power	Total Pe Power (%)	Sequential 96.26	23.91	0.1162	0.2657	24.29	Macro 0	0	0	0	0	IO 0	0	0	0	0	Combinational 3.739	0.242	0.6745	0.02709	0.9436	Clock (Combinational) 0	0	0	0	0	Clock (Sequential) 0	0	0	0	0	Total 100	24.15	0.7907	0.2928	25.23
Group	Internal Power	Switching Power	Leakage Power	Total Power (%)																																																																																					
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Clock (Sequential) 0	0	0	0	0																																																																																					
Total 100	24.15	0.7907	0.2928	25.23																																																																																					
Total power = 33.003 mW					Total power = 25.232 mW																																																																																				

Total power decreases in this case, after CTS because of optimization.

Gate Count:

Gate area 2.2707 um^2	Gates=10097	Cells=1461	Area= 22928.8 um^2
Level 0 Module top8 module	Gates=502	Cells=242	Area= 1140.6 um^2
Level 1 Module alu_inst	Gates=105	Cells=17	Area= 238.4 um^2
Level 1 Module ff_alu_in1	Gates=9122	Cells=1135	Area= 20714.1 um^2
Level 1 Module mem_inst	Gates=156	Cells=24	Area= 355.7 um^2
Level 1 Module pc_inst			

Figure 4.2.5: Gate Count

- Number of total gates =10097
- Total number of cells =1461

- Gate area = $2.2707 \text{ }\mu\text{m}^2$

Clock tree:

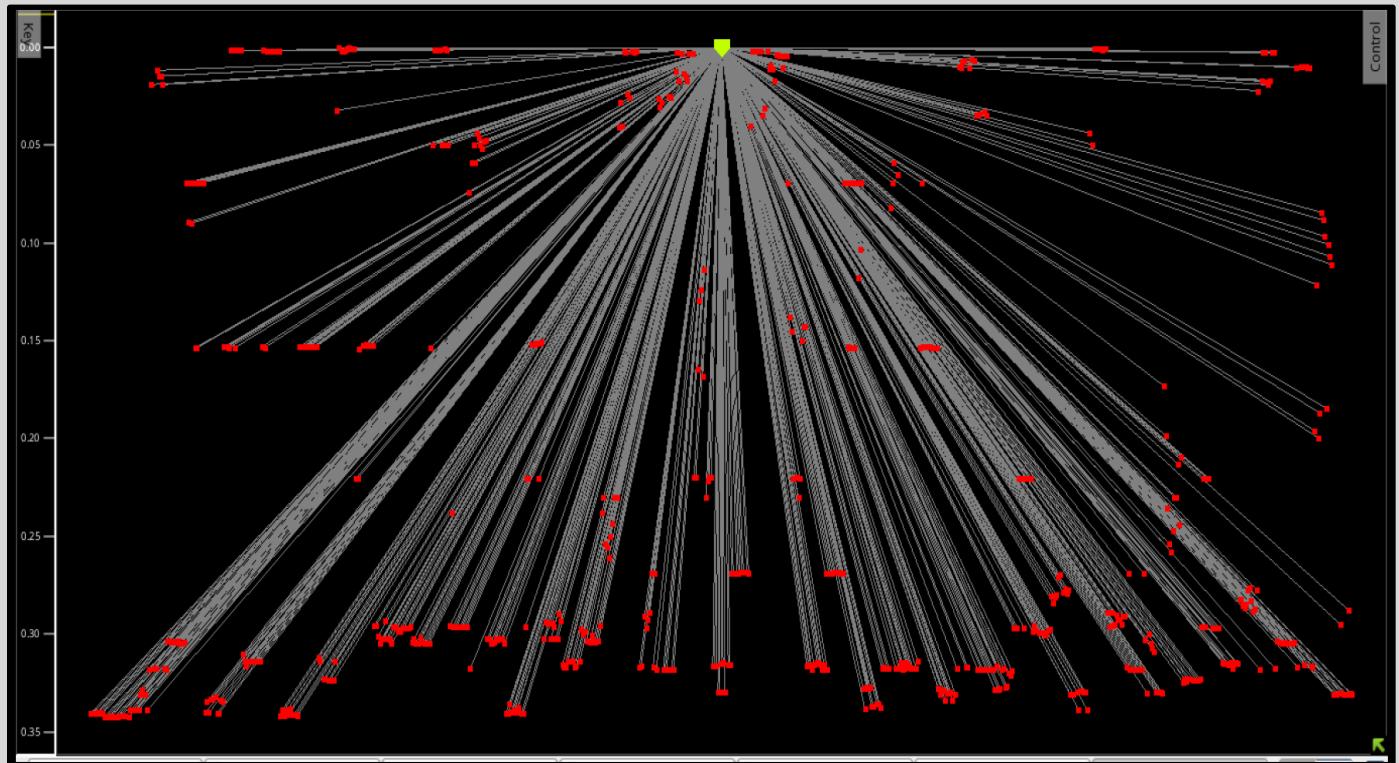


Figure 4.2.6: Snapshot of the generated clock tree for the design

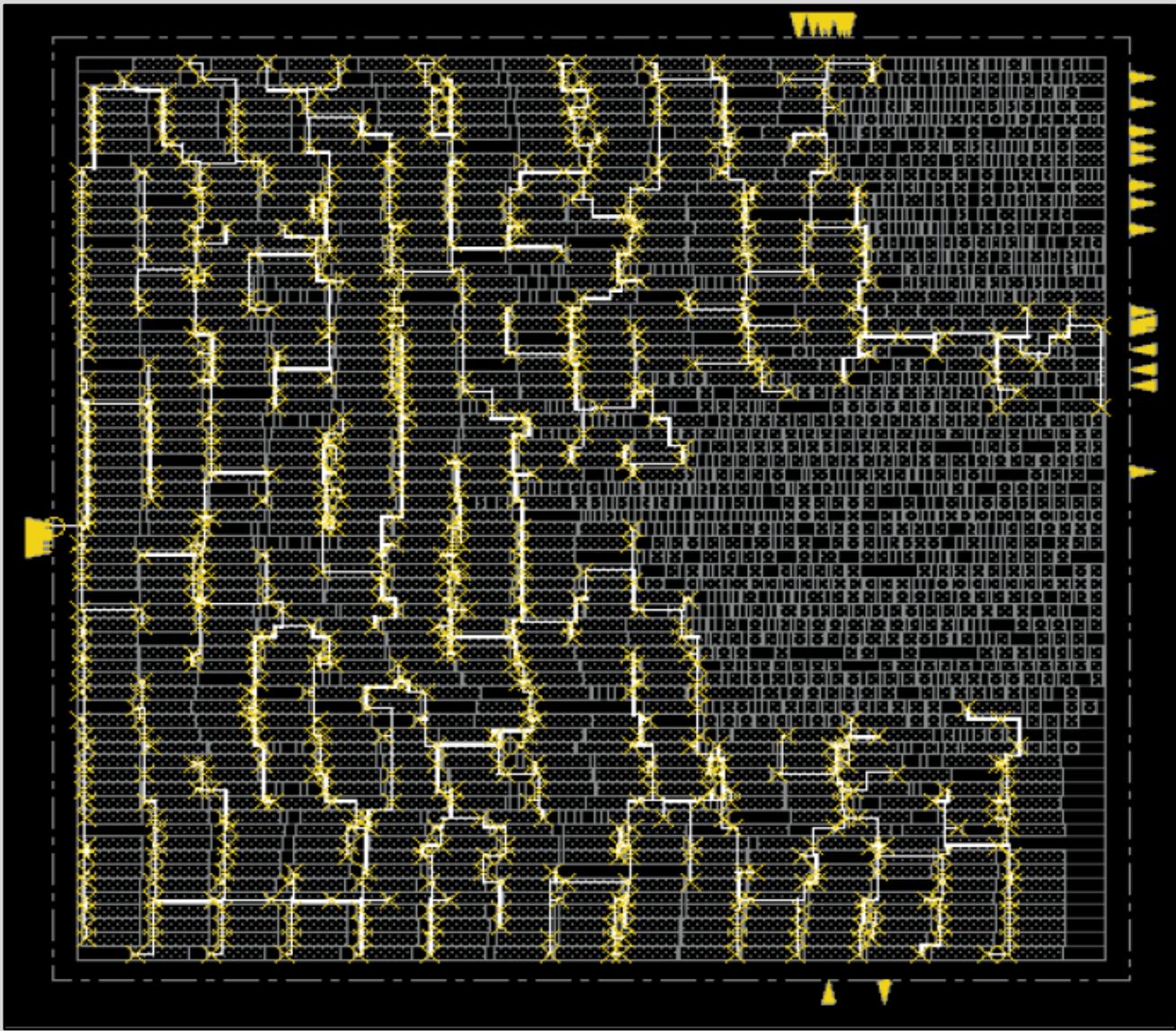


Figure 4.2.7: Routing of the clock path is highlighted

4.3 After detailed routing

Setup Analysis

```

Path 1: MET Setup Check with Pin mem_inst/mem_reg[40][10]1156/CK
Endpoint: mem_inst/mem_reg[40][10]1156/S0 (^) checked with leading edge of
'CLK'
Beginpoint: pc_inst/pc_out_addr_reg[5]/Q (^) triggered by leading edge of
'CLK'
Path Groups: {reg2reg}
Analysis View: view1
Other End Arrival Time      0.000
- Setup                      0.136
+ Phase Shift                2.000
= Required Time              1.864
- Arrival Time               1.002
= Slack Time                 0.862
Clock Rise Edge              0.000
= Beginpoint Arrival Time    0.000
Timing Path:
+-----+
|   Pin   | Edge | Net     | Cell    | Delay | Arrival | Required |
|         |     |          |          |       | Time    | Time     |
+-----+
| clk     | ^   | clk     | SDFFRHQX1 | 0.000 | 0.000 | 0.862 |
| pc_inst/pc_out_addr_reg[5]/CK | ^   | clk     | SDFFRHQX1 | 0.138 | 0.000 | 0.862 |
| pc_inst/pc_out_addr_reg[5]/Q  | ^   | DFT_sdo_2 | SDFFRHQX1 | 0.138 | 0.138 | 1.000 |
| mem_inst/g67723/AN           | ^   | DFT_sdo_2 | NOR2BX1  | 0.000 | 0.138 | 1.000 |
| mem_inst/g67723/Y            | ^   | mem_inst/n_15 | NOR2BX1  | 0.045 | 0.183 | 1.045 |
| mem_inst/g67691/B             | ^   | mem_inst/n_15 | NAND2XL   | 0.000 | 0.183 | 1.045 |
| mem_inst/g67691/Y             | v   | mem_inst/n_45 | NAND2XL   | 0.274 | 0.457 | 1.320 |
| mem_inst/g67600/B             | v   | mem_inst/n_45 | NOR2XL    | 0.006 | 0.463 | 1.325 |
| mem_inst/g67600/Y             | ^   | mem_inst/n_126 | NOR2XL   | 0.537 | 1.000 | 1.862 |
| mem_inst/mem_reg[40][10]1156/S0 | ^   | mem_inst/n_126 | SMDFFHQX1 | 0.002 | 1.002 | 1.864 |
+-----+
Clock Rise Edge              0.000
= Beginpoint Arrival Time    0.000
Other End Path:
+-----+
|   Pin   | Edge | Net     | Cell    | Delay | Arrival | Required |
|         |     |          |          |       | Time    | Time     |
+-----+
| clk     | ^   | clk     |          |       | 0.000 | -0.862 |
| mem_inst/mem_reg[40][10]1156/CK | ^   | clk     | SMDFFHQX1 | 0.000 | 0.000 | -0.862 |
+-----+

```

Figure 4.3.1: Setup Analysis of the worst path

- Here, the timing arc for the worst setup path is from **pc_inst/pc_out_addr_reg[5]/Q** (begin point)

to **mem_inst/mem_reg[40][10]1156/S0 (output port)**.

- The arrival time is **1.002 ps**, the required time is **1.864 ps** and the slack calculated as the difference between required time and arrival time is **0.862**.
- Here, the setup slack is positive.

Hold Analysis

```

Path 1: MET Hold Check with Pin ff_alu_in1/q_reg[5]/CK
Endpoint: ff_alu_in1/q_reg[5]/D (v) checked with leading edge of 'CLK'
Beginpoint: alu_in1_inp[5] (v) triggered by leading edge of '@'
Path Groups: {CLK}
Analysis View: view1
Other End Arrival Time      0.000
+ Hold                      0.073
+ Phase Shift                0.000
= Required Time              0.073
Arrival Time                 0.097
Slack Time                  0.024
Clock Rise Edge              0.000
+ Input Delay                0.000
= Beginpoint Arrival Time   0.000
Timing Path:
+
|     Pin          | Edge | Net           | Cell | Delay | Arrival | Required |
|     |             |     |               |       |        | Time    | Time     |
+-----+-----+-----+-----+-----+-----+-----+
| alu_in1_inp[5] | v   | alu_in1_inp[5] |       |       | 0.000  | -0.024 |
| ff_alu_in1/FE_PHC188_alu_in1_inp_5/A | v   | alu_in1_inp[5] | CLKBUFX2 | -0.001 | -0.001 | -0.024 |
| ff_alu_in1/FE_PHC188_alu_in1_inp_5/Y | v   | ff_alu_in1/FE_PHN188_alu_in1_inp_5 | CLKBUFX2 | 0.097  | 0.097  | 0.073  |
| ff_alu_in1/q_reg[5]/D | v   | ff_alu_in1/FE_PHN188_alu_in1_inp_5 | SDFFQX2 | 0.000  | 0.097  | 0.073  |
+
Clock Rise Edge              0.000
= Beginpoint Arrival Time   0.000
Other End Path:
+
|     Pin          | Edge | Net           | Cell | Delay | Arrival | Required | |
|     |             |     |               |       |        | Time    | Time     |
|     |             |     |               |       |        |          |
+-----+-----+-----+-----+-----+-----+-----+
| clk            | ^   | clk           |       |       | 0.000  | 0.024 |
| ff_alu_in1/q_reg[5]/CK | ^   | clk           | SDFFQX2 | 0.000  | 0.000  | 0.024 |
+

```

Figure 4.3..2: Hold Analysis of the worst path

- Here, the worst path for the hold slack is from **alu_in1_inp[5]** (**begin point**) to **ff_alu_in1/q_reg[5]/D**.
- The arrival time is **0.097 ps**, the required time is **0.073 ps** and the slack calculated as the difference between required time and arrival time is **0.024**.
- Here, the hold slack is positive.

Effect on hold slack after detailed routing:

Before Routing

```

Path 1: MET Hold Check with Pin ff_alu_in1/q_reg[0]/CK
Endpoint: ff_alu_in1/q_reg[0]/SI (v) checked with leading edge of 'CLK'
Beginpoint: DFT_sdi_1 (v) triggered by leading edge of 'q'
Path Groups: {CLK}
Analysis View: view1
Other End Arrival Time 0.000
+ Hold 0.053
+ Phase Shift 0.000
= Required Time 0.053
Arrival Time 0.060
Slack Time 0.008
Clock Rise Edge 0.000
+ Input Delay 0.000
= Beginpoint Arrival Time 0.000
Timing Path:
+-----+
| Pin | Edge | Net | Cell | Delay | Arrival | Required |
| | | | | Time | | Time |
+-----+
| DFT_sdi_1 | v | DFT_sdi_1 | | 0.000 | -0.008 | |
| ff_alu_in1/FE_PHC25_DFT_sdi_1/A | v | DFT_sdi_1 | DLYIX1 | 0.000 | 0.000 | -0.008 |
| ff_alu_in1/FE_PHC25_DFT_sdi_1/Y | v | ff_alu_in1/FE_PHN25_DFT_sdi_1 | DLYIX1 | 0.060 | 0.060 | 0.053 |
| ff_alu_in1/q_reg[0]/SI | v | ff_alu_in1/FE_PHN25_DFT_sdi_1 | SDFFOX1 | 0.000 | 0.060 | 0.053 |
+-----+
Clock Rise Edge 0.000
= Beginpoint Arrival Time 0.000
Other End Path:
+-----+
| Pin | Edge | Net | Cell | Delay | Arrival | Required |
| | | | | Time | | Time |
+-----+
| clk | ^ | clk | | 0.000 | 0.008 |
| ff_alu_in1/q_reg[0]/CK | ^ | clk | SDFFOX1 | 0.000 | 0.000 | 0.008 |
+-----+

```

Slack time = 0.008 ps

After Routing

```

Path 1: MET Hold Check with Pin ff_alu_in1/q_reg[5]/CK
Endpoint: ff_alu_in1/q_reg[5]/O (v) checked with leading edge of 'CLK'
Beginpoint: alu_in1_inp[5] (v) triggered by leading edge of 'q'
Path Groups: {CLK}
Analysis View: view1
Other End Arrival Time 0.000
+ Hold 0.073
+ Phase Shift 0.000
= Required Time 0.073
Arrival Time 0.097
Slack Time 0.024
Clock Rise Edge 0.000
+ Input Delay 0.000
= Beginpoint Arrival Time 0.000
Timing Path:
+-----+
| Pin | Edge | Net | Cell | Delay | Arrival | Required |
| | | | | Time | | Time |
+-----+
| alu_in1_inp[5] | v | alu_in1_inp[5] | | 0.000 | -0.024 | |
| ff_alu_in1/FE_PHC188_alu_in1_inp_5/A | v | alu_in1_inp[5] | CLKBUF2 | -0.001 | -0.061 | -0.024 |
| ff_alu_in1/FE_PHC188_alu_in1_inp_5/Y | v | ff_alu_in1/FE_PHN188_alu_in1_inp_5 | CLKBUF2 | 0.097 | 0.097 | 0.073 |
| ff_alu_in1/q_reg[5]/O | v | ff_alu_in1/FE_PHN188_alu_in1_inp_5 | SDFFOX2 | 0.000 | 0.097 | 0.073 |
+-----+
Clock Rise Edge 0.000
= Beginpoint Arrival Time 0.000
Other End Path:
+-----+
| Pin | Edge | Net | Cell | Delay | Arrival | Required |
| | | | | Time | | Time |
+-----+
| clk | ^ | clk | | 0.000 | 0.024 |
| ff_alu_in1/q_reg[5]/CK | ^ | clk | SDFFOX2 | 0.000 | 0.000 | 0.024 |
+-----+

```

Slack time = 0.024 ps

After detailed routing slack time improved because of optimization which added buffers to increase the arrival time.

Area Analysis:

Hinst Name	Module Name	Inst Count	Total Area
<hr/>			
top8_module		1461	22928.772
alu_inst	alu	242	1140.648
decoder_inst	decoder	11	158.192
ff_alu_in1	ff_8bit	17	238.424
ff_carry_inst	ff_154	1	20.436
ff_negative_inst	ff_152	1	20.436
ff_pc_rst_inst	ff	2	24.978
ff_zero_inst	ff_153	1	20.436
ir_inst	instr_reg	11	158.192
mem_inst	instr_memory	1135	20714.082
pc_inst	pc	24	355.743

Figure 4.3.3: Area Analysis

The area is found to be **22928.772 um²**

GATE COUNT:

Gate area 2.2707 um^2				
Level 0 Module top8_module	Gates=10097	Cells=1461	Area=	22928.8 um^2
Level 1 Module alu_inst	Gates=502	Cells=242	Area=	1140.6 um^2
Level 1 Module ff_alu_in1	Gates=105	Cells=17	Area=	238.4 um^2
Level 1 Module mem_inst	Gates=9122	Cells=1135	Area=	20714.1 um^2
Level 1 Module pc_inst	Gates=156	Cells=24	Area=	355.7 um^2

Figure 4.3.4: Gate Count

- Number of total gates = **10097**
- Total number of cells = **1461**
- Gate area = **2.2707 um²**

Power Analysis:

Total Power						
Total Internal Power:	24.12756657	95.7228%				
Total Switching Power:	0.78530103	3.1156%				
Total Leakage Power:	0.29278875	1.1616%				
Total Power:	25.20565596					
<hr/>						
Group	Internal Power	Switching Power	Leakage Power	Total Power	Percentage (%)	
Sequential	23.89	0.1151	0.2657	24.27	96.28	
Macro	0	0	0	0	0	
IO	0	0	0	0	0	
Combinational	0.2414	0.6702	0.02709	0.9388	3.724	
Clock (Combinational)	0	0	0	0	0	
Clock (Sequential)	0	0	0	0	0	
Total	24.13	0.7853	0.2928	25.21	100	
<hr/>						
Rail	Voltage	Internal Power	Switching Power	Leakage Power	Total Power	Percentage (%)
Default	1.1	24.13	0.7853	0.2928	25.21	100

Figure 4.3.5: Power Analysis

Internal power = 24.13 mW

Switching power = 0.7853 mW

Leakage power = 0.2928 mW

Total power = 25.21 mW

Before Routing

After Routing

Total Power					
Group Percentage		Internal Power	Switching Power	Leakage Power	Total Power (%)
Sequential	96.26	23.91	0.1162	0.2657	24.29
Macro	0	0	0	0	0
IO	0	0	0	0	0
Combinational	3.739	0.242	0.6745	0.02709	0.9436
Clock (Combinational)	0	0	0	0	0
Clock (Sequential)	0	0	0	0	0
Total	100	24.15	0.7907	0.2928	25.23

Total power = 25.23 mW

Total Power					
Group		Internal Power	Switching Power	Leakage Power	Total Power (%)
Sequential		23.89	0.1151	0.2657	24.27 96.28
Macro		0	0	0	0 0
IO		0	0	0	0 0
Combinational		0.2414	0.6702	0.02709	0.9388 3.724
Clock (Combinational)		0	0	0	0 0
Clock (Sequential)		0	0	0	0 0
Total		24.13	0.7853	0.2928	25.21 100

Rail	Voltage	Internal Power	Switching Power	Leakage Power	Total Power (%)
Default	1.1	24.13	0.7853	0.2928	25.21 100

Total power = 25.21 mW

Power remains almost the same due to the fact that optimization was explicitly done after the stage.

DRC Clean after post route:

```
VERIFY DRC ..... Starting Verification
VERIFY DRC ..... Initializing
VERIFY DRC ..... Deleting Existing Violations
VERIFY DRC ..... Creating Sub-Areas
VERIFY DRC ..... Using new threading
VERIFY DRC ..... Sub-Area: {0.000 0.000 94.080 90.240} 1 of 4
VERIFY DRC ..... Sub-Area : 1 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {94.080 0.000 184.730 90.240} 2 of 4
VERIFY DRC ..... Sub-Area : 2 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {0.000 90.240 94.080 180.380} 3 of 4
VERIFY DRC ..... Sub-Area : 3 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {94.080 90.240 184.730 180.380} 4 of 4
VERIFY DRC ..... Sub-Area : 4 complete 0 Viols.
```

Verification Complete : 0 Viols.

```
*** End Verify DRC (CPU: 0:00:00.5 ELAPSED TIME: 1.00 MEM: 0.0M) ***
```

Figure 4.3.6: DRC report after routing

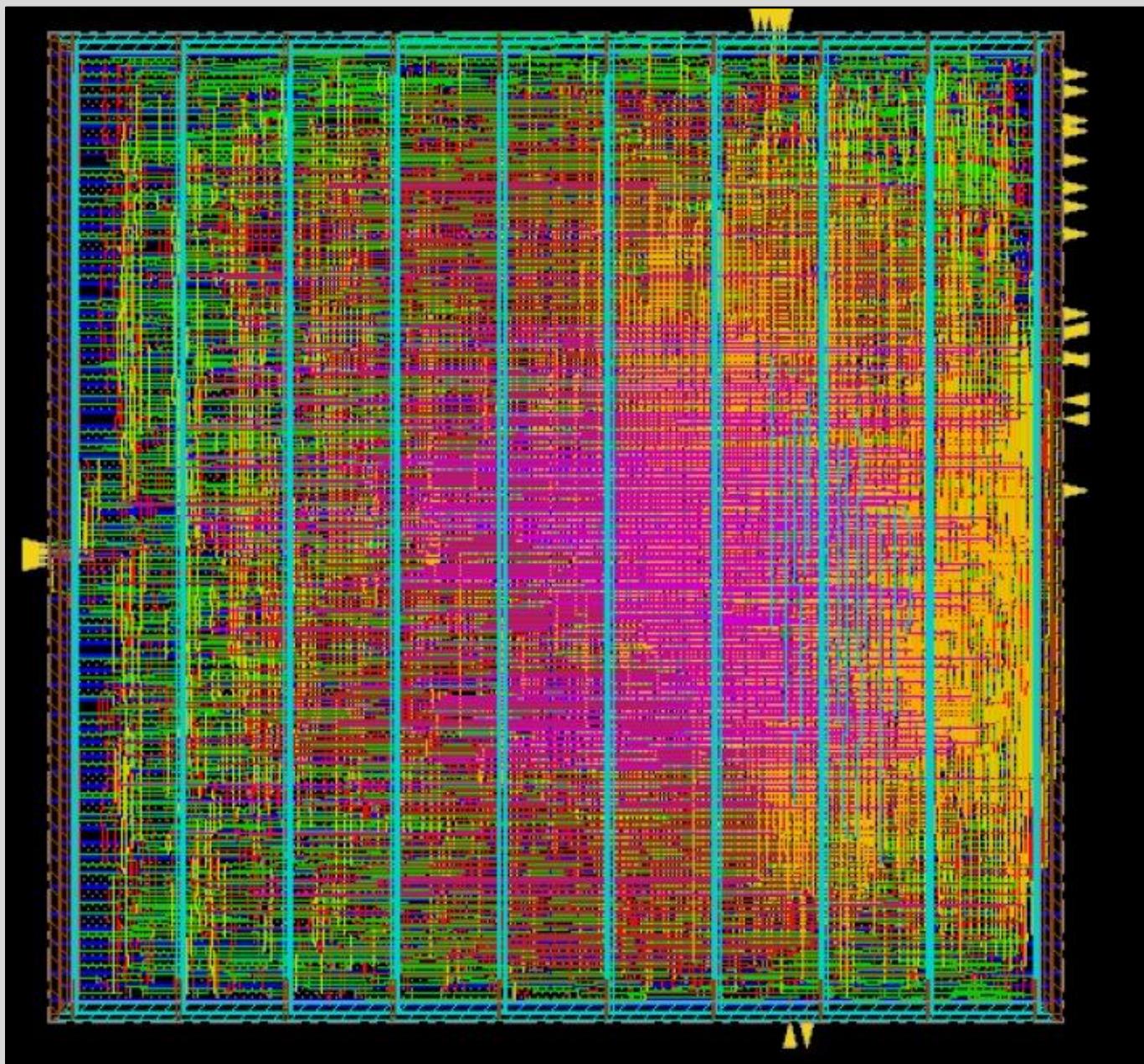
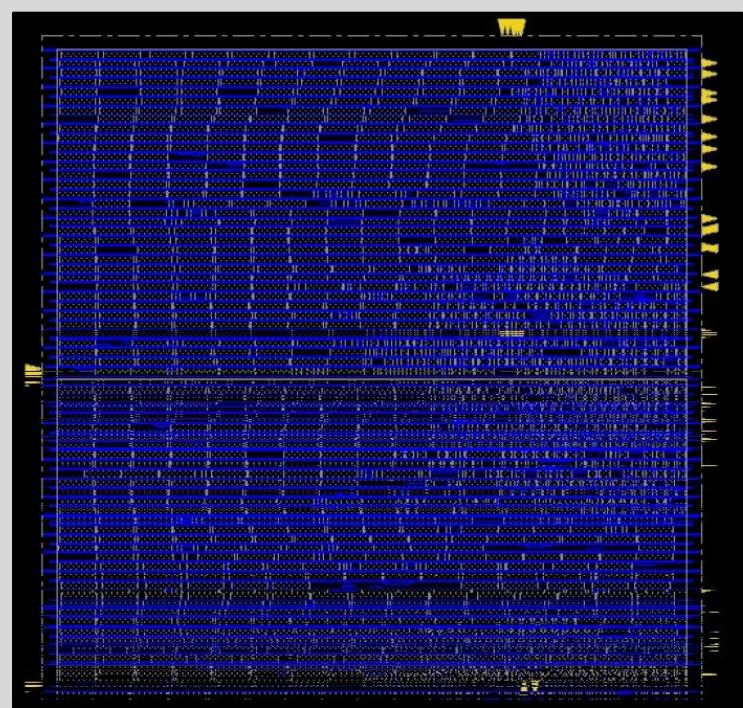


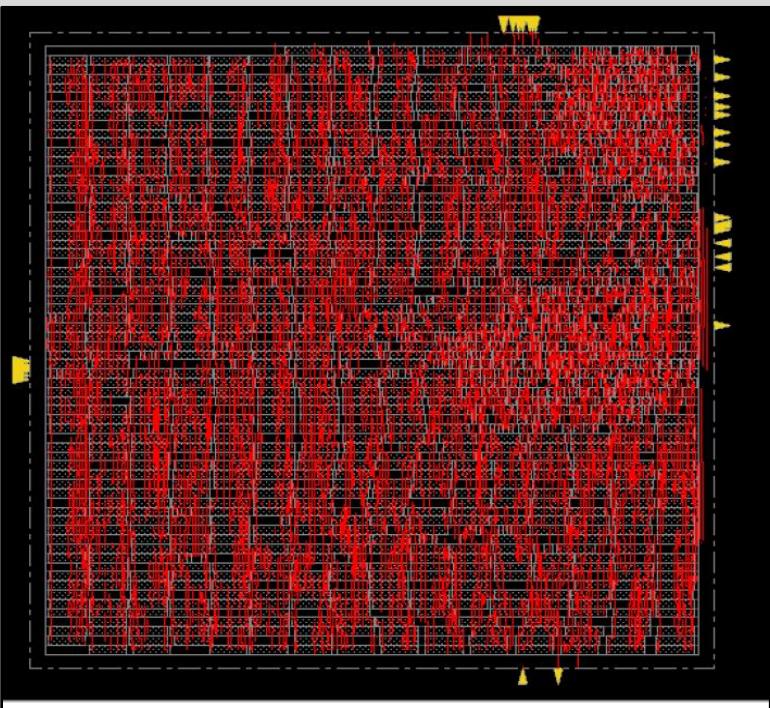
Figure 4.3.7: Layout of the design with 0.8 core utilization area

Metal layers along with standard cells:

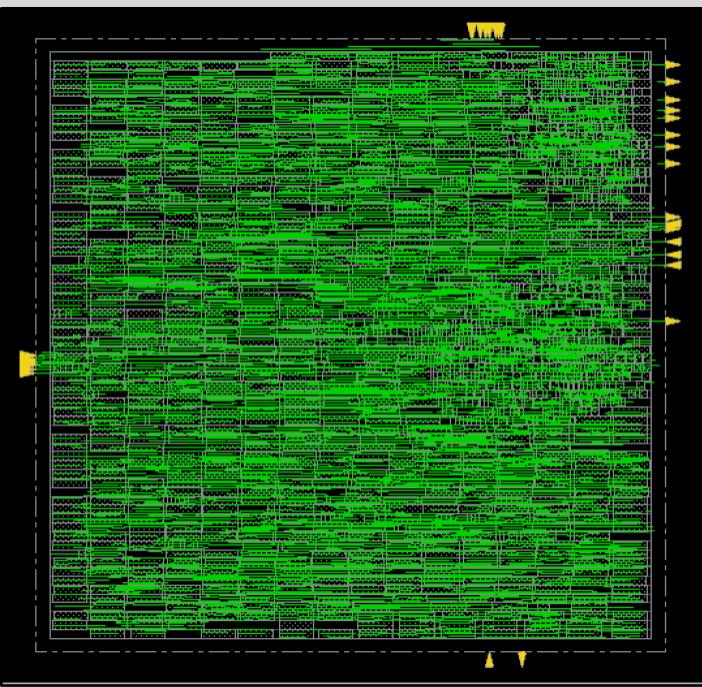
Metal 1



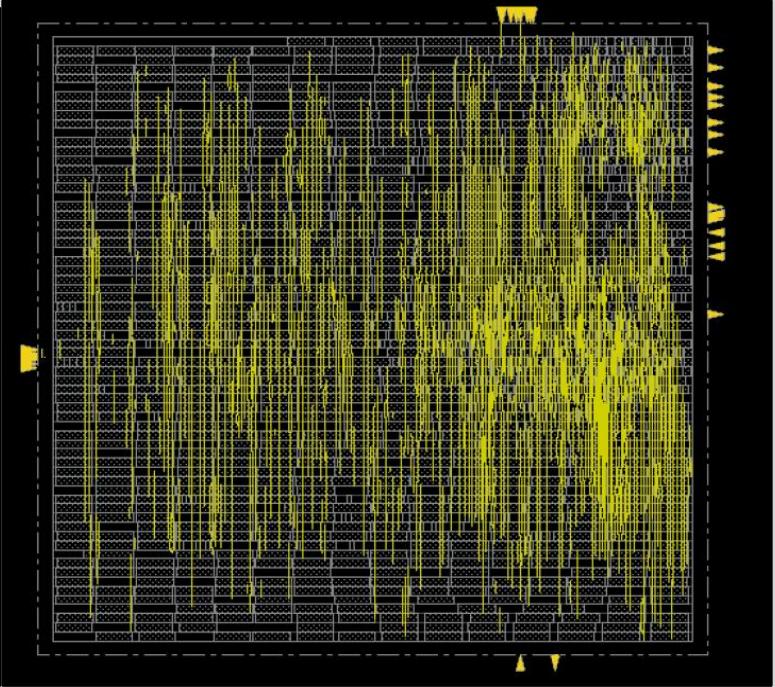
Metal 2



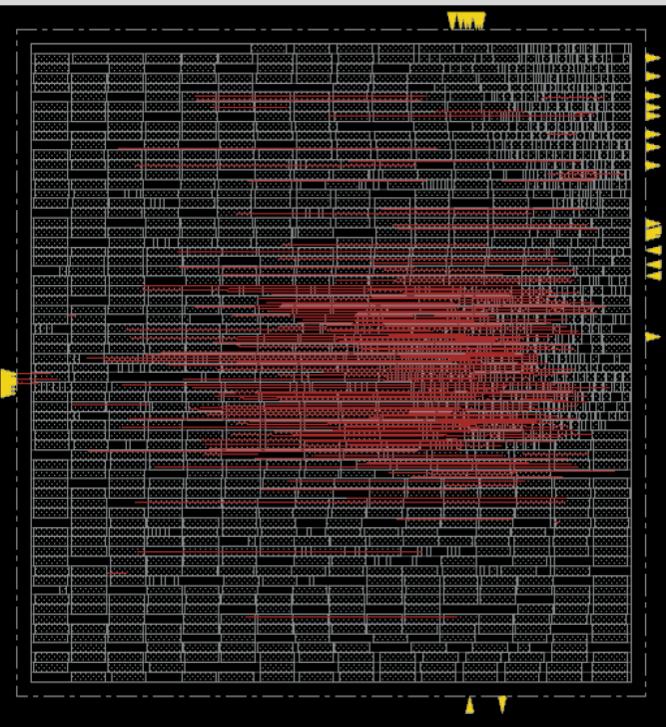
Metal 3



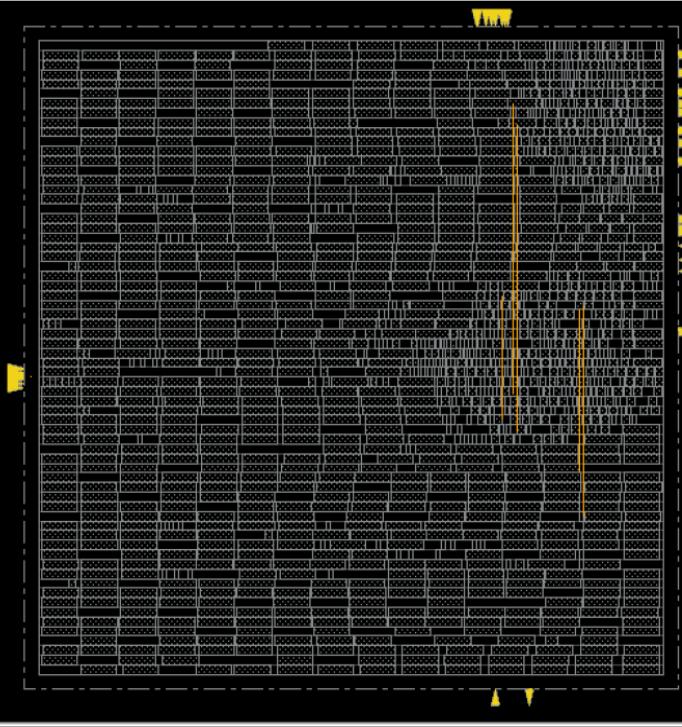
Metal 4



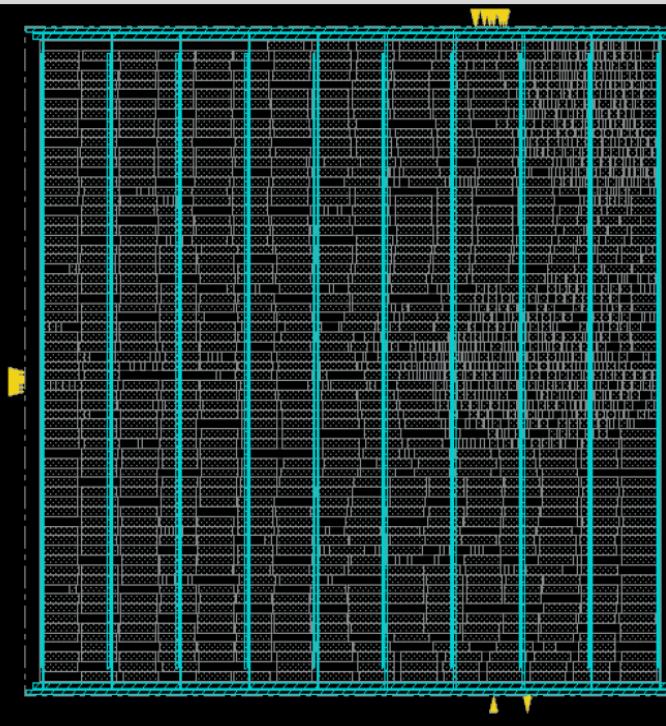
Metal 5



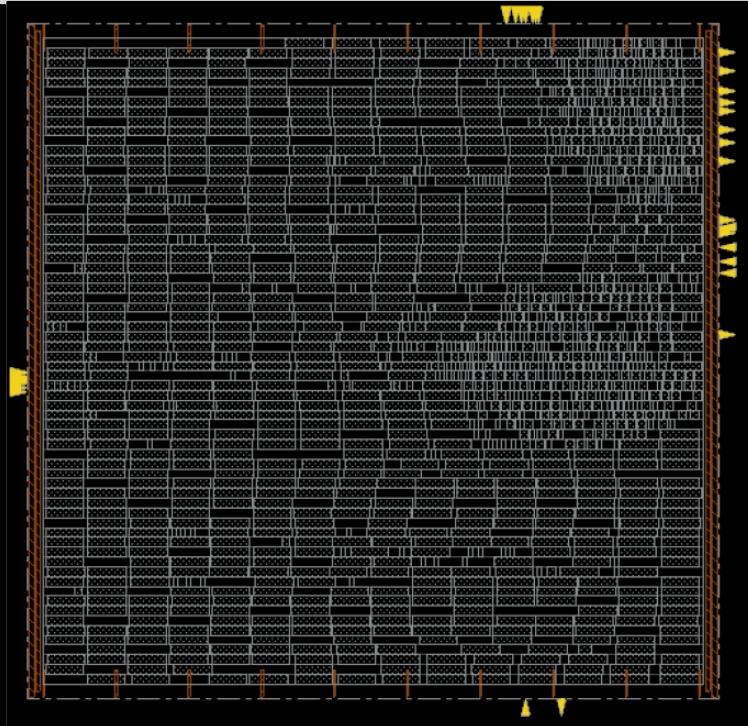
Metal 6



Metal 8



Metal 9



Effect of Different Metal Layers on Timing of the Path:-

As higher metal layers have less resistance so they have less delay. For VDD and ground connection metal 8 and metal 9 layers are used. So the delay in the circuit depends on the resistance of the metal layers used. As observed from the analysis that as higher metal layers are used the resistance falls and the delay reduces as a result. The slack in the circuit is the direct measure of the metal layer being used. Slack is higher if higher metal layers are used in the design.

Layout with fly-lines:

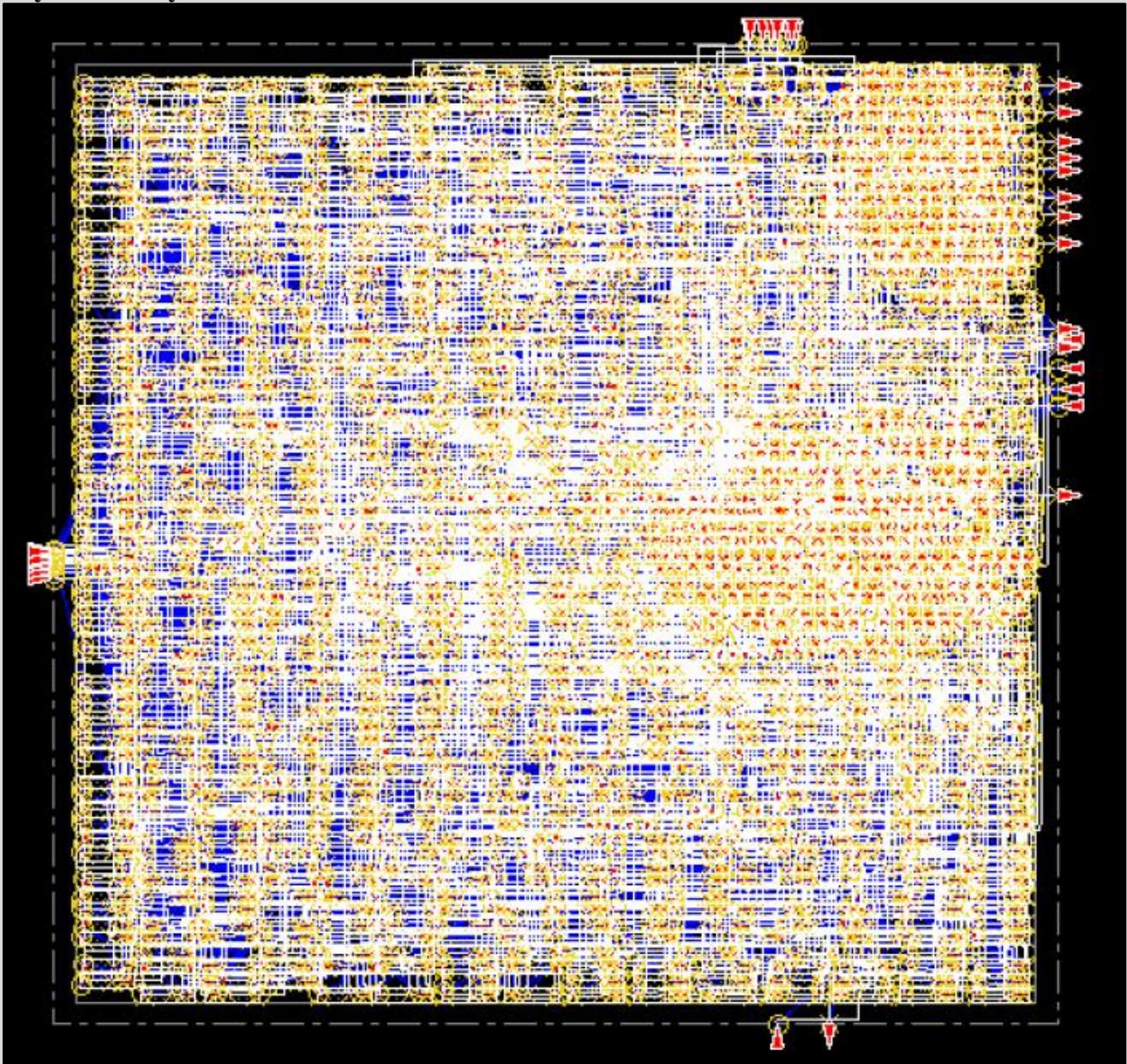


Figure 4.3.8: fly-lines in the design

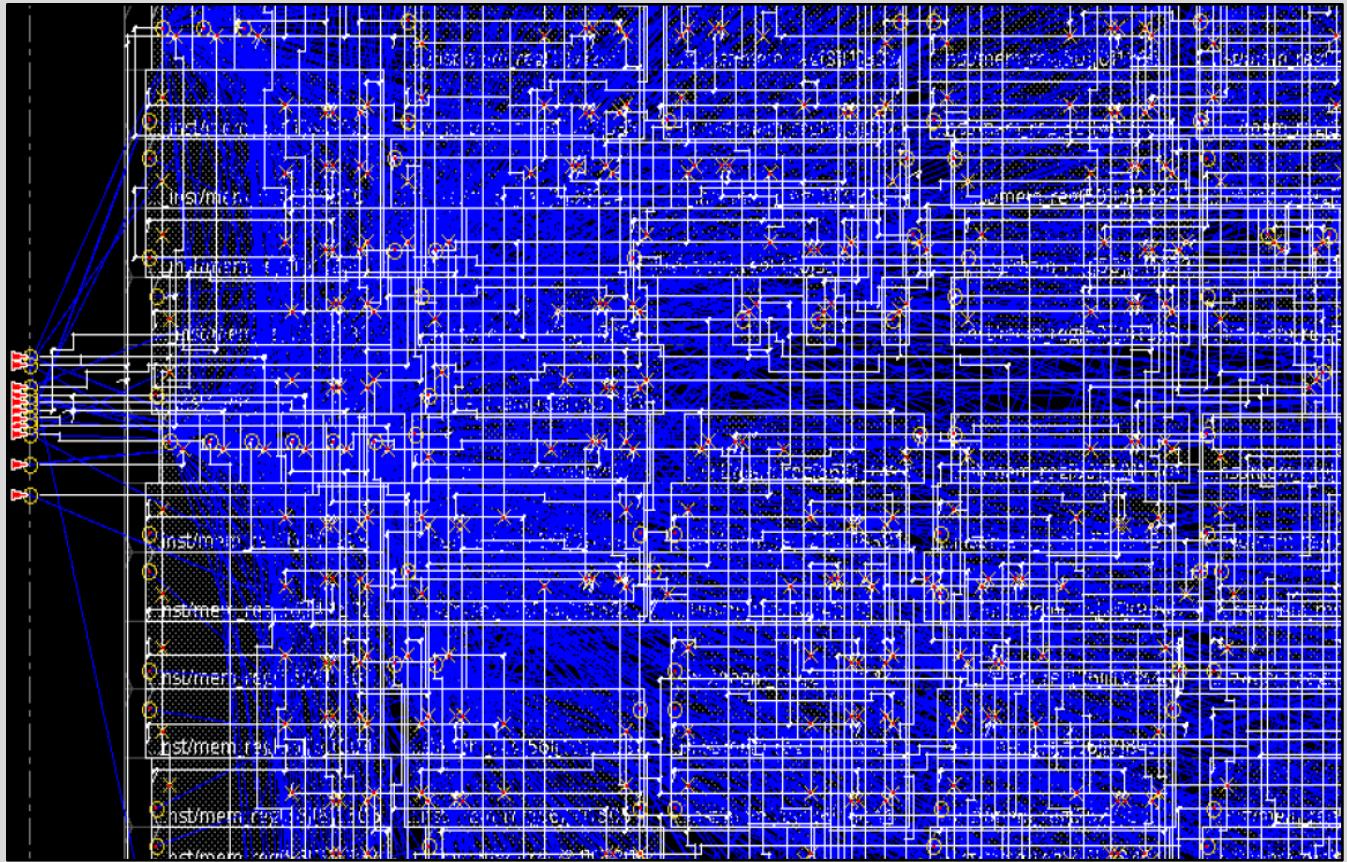


Figure 4.3.9:Closer look at the fly-lines in the design

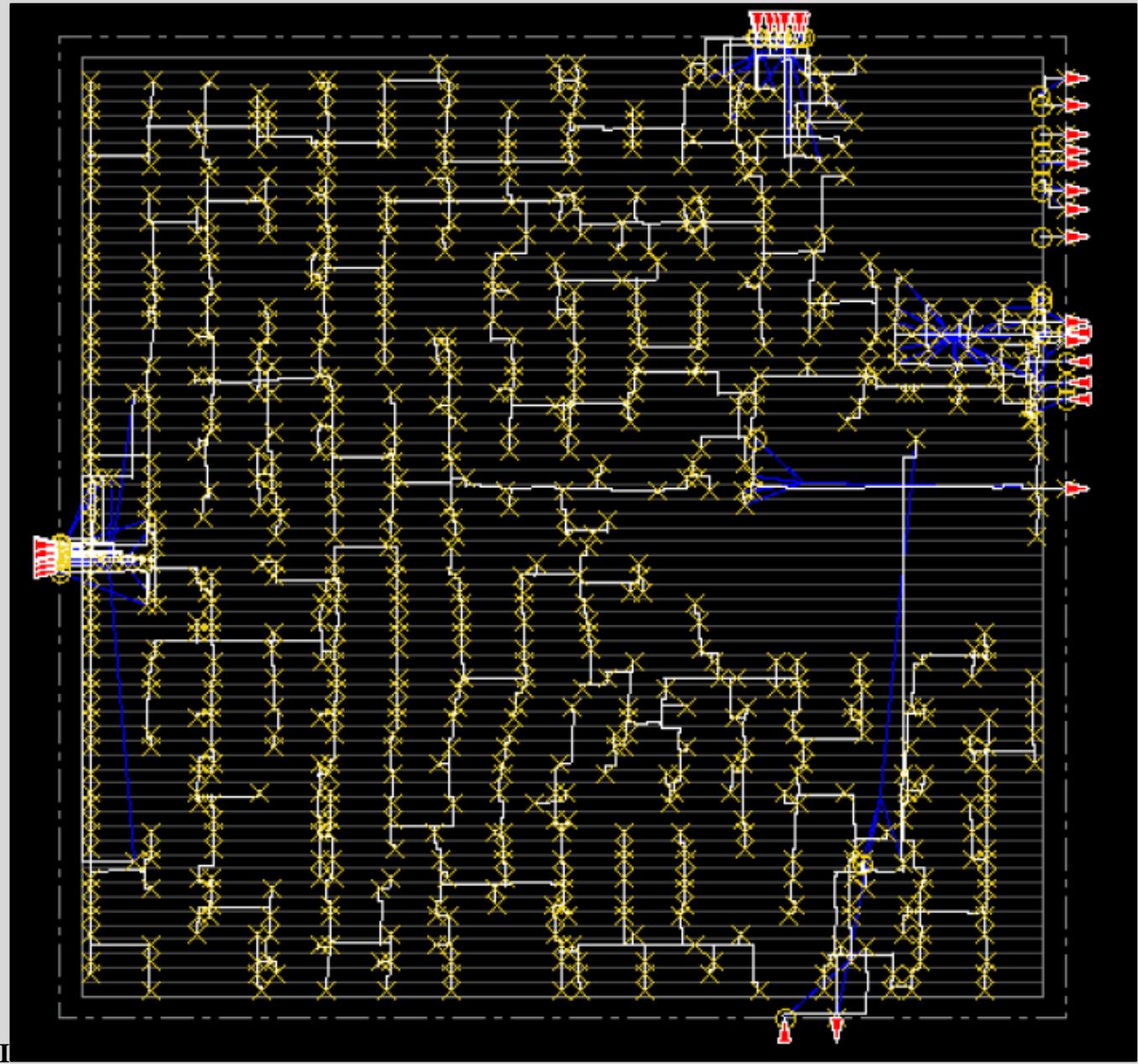


Figure 4.3.10: Connectivity with different ports

- A flyline represents the total number of connections between a pair of macros or I/O cells. It helps in deciding the locations for the macros.