CP1 Progress Report

Work breakdown and implementation of functionalities

Mridul has worked on the top level files (top.sv and mp4.sv), connecting everything within the design - some of the things ended up being signals not needed within this first checkpoint; these have been pushed to a new branch - Lakshya finalized these connections. Lakshya has also worked on pipelined registers - he created the interface and modules for the appropriate registers. Peter has worked on the datapath and control. He also led the debugging effort, though all three team members did that.

Testing strategy

The testing strategy was to compare the outputs of the CPU with the outputs of the CPU from previous MPs. Specifically, MP3 was the main code used for comparison.

CP2 Roadmap

Projected work breakdown

Mridul will work on the arbiter, as well as the hazard detection. The arbiter will coordinate memory requests from I-cache and D-cache. The hazard unit will detect potential data hazard or control hazard, and it will stall the pipeline when necessary. Lakshya will work on forwarding. The forwarding unit will forward previous outputs directly to the ALU before they are written to the registers. Peter will work on the static branch predictor and L1 cache. The I-cache will serve memory requests for the instructions and the D-cache will serve memory requests for other data. The branch predictor will try to predict the current branching outcome based on previous outcomes.