ASSIGNMNET-6

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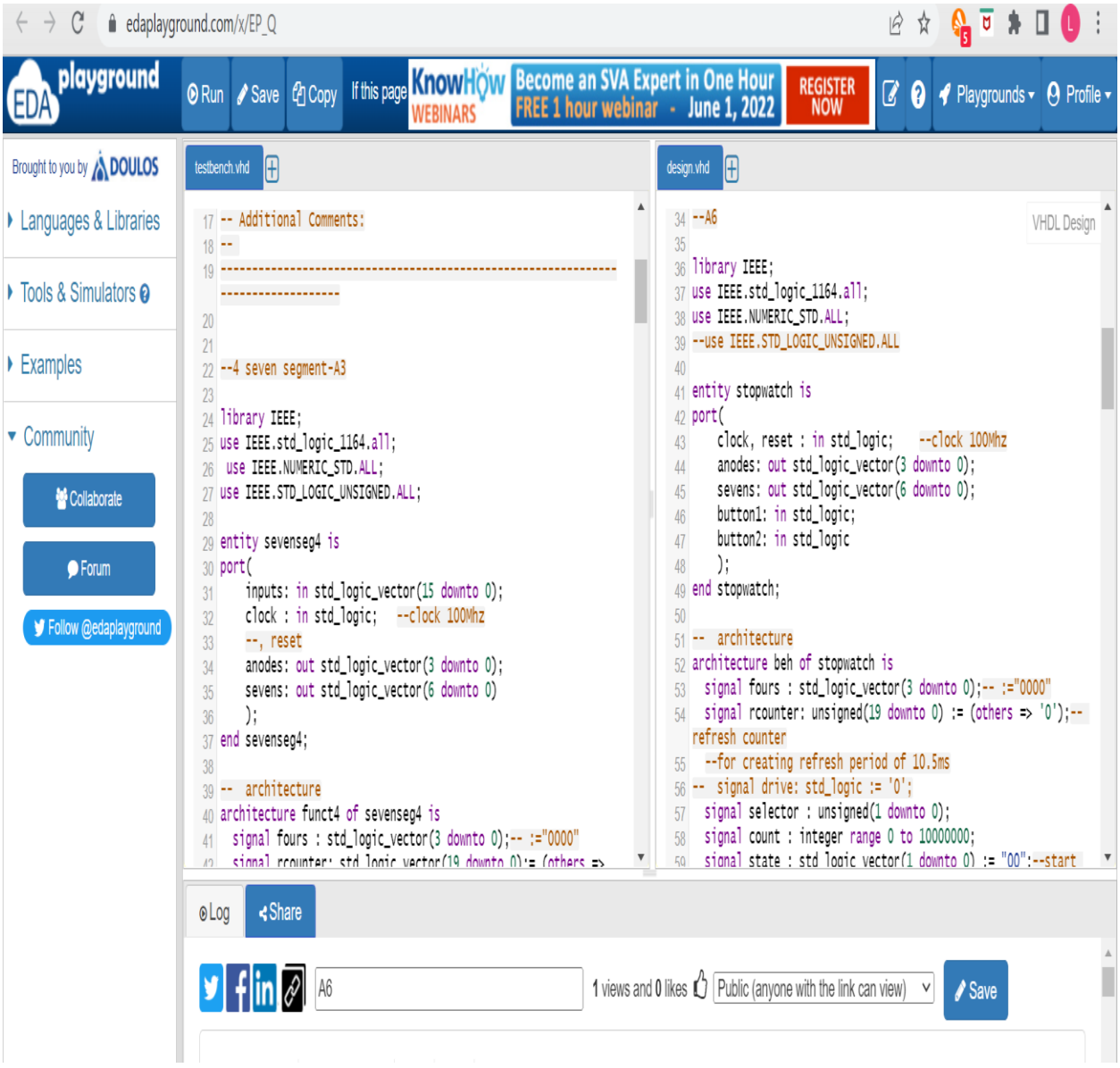
In this assignment we designed a stopwatch and implement it on BASYS 3 board, using 7-segment display already implemented module in A3 and push buttons.

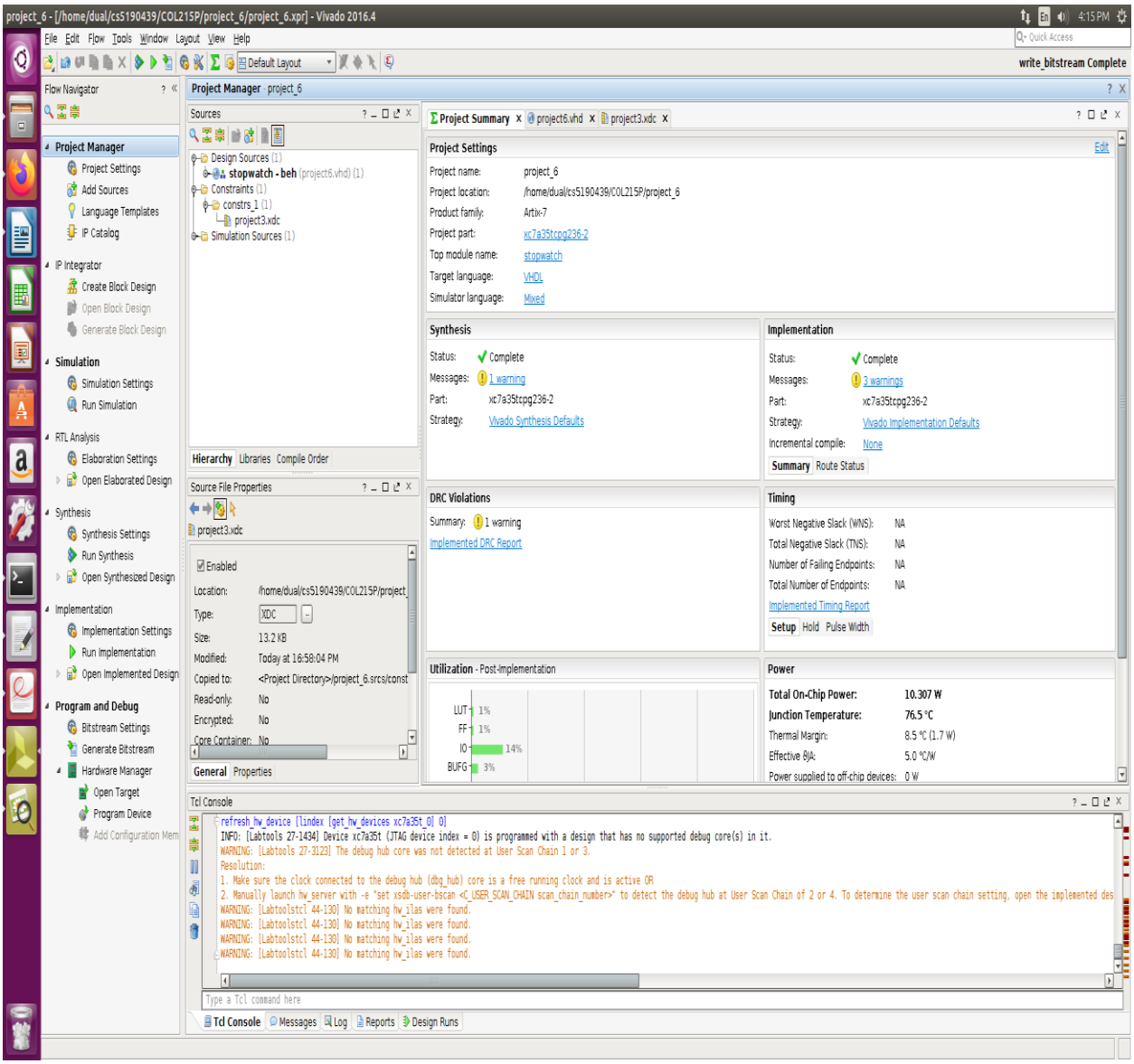
Submission folder (2019CS50439_2019CS50434) contains -

- **project6.xdc - constraint file**
- **a6.vhd -vhdl code file**
- **stopwatch.bit - bitstream file**
- **A6_report.pdf- report file**

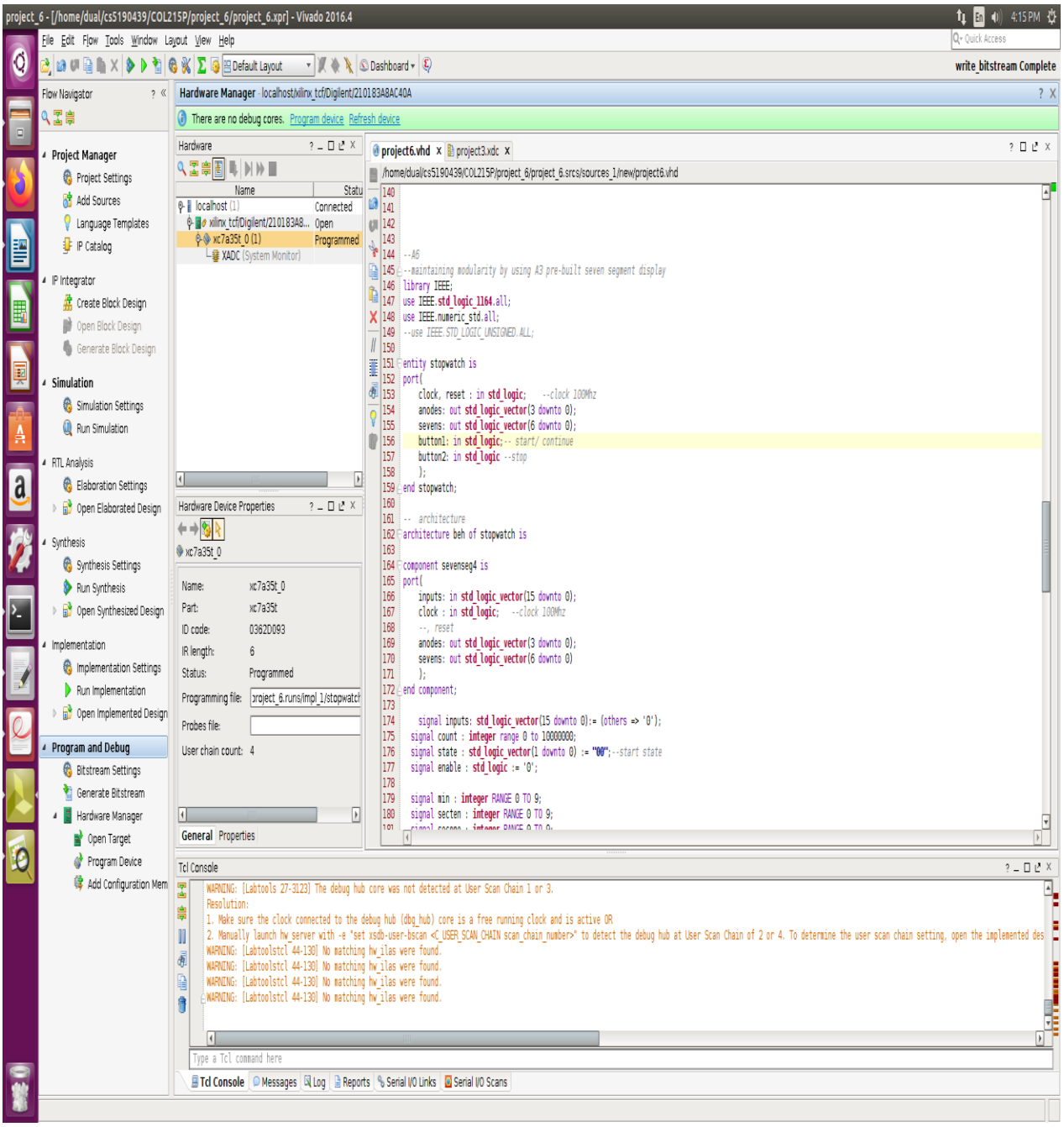
EDA PLAYGROUND Code and simulation-



New project6 on Vivado-



VHDL code on Vivado -



The code is also provided in the submission file

DESCRIPTION

Here we assumed normal indexing of segments of seven segment display(B-2,etc)

What we have done is take a counter that increments every clock rising edge and after 10^7 –1 increments it increases the value of first LED (one-tenth of a second) then after 10 such increments the second LED is increased by one (one second), then after ten such seconds the third LED is increased by one (tens digit seconds) then after 6 such increases the fourth LED is increased by one (the minute one).

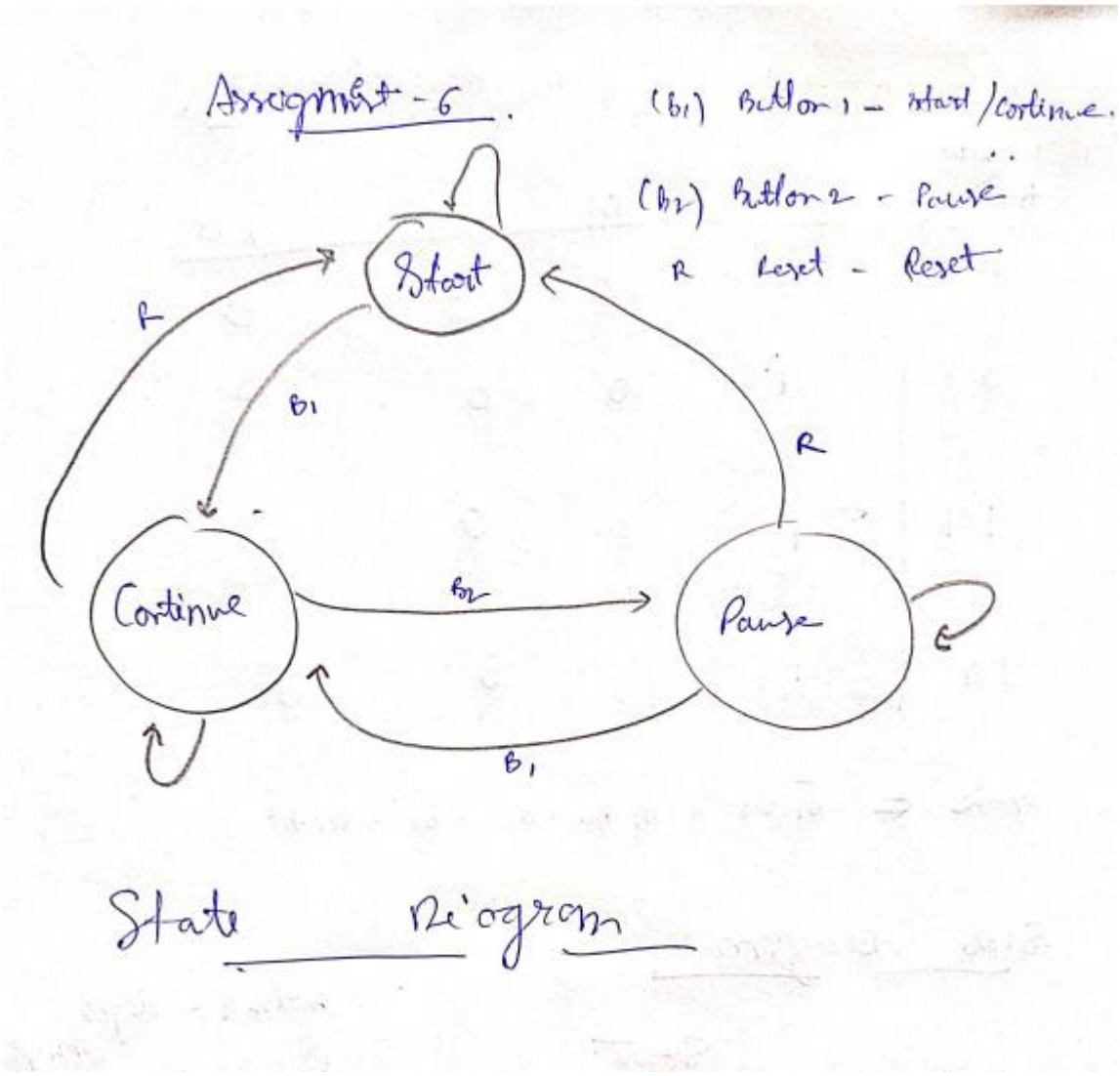
All the LEDs are reseted back to zero when they reach their limit (as per given in the assignment requirement). All of them are also reseted when reset button is pushed.

timing for refreshing the 4-digit seven-segment display on Basys 3 FPGA is same as A3,used same 4 digits sement display module-

Design decision

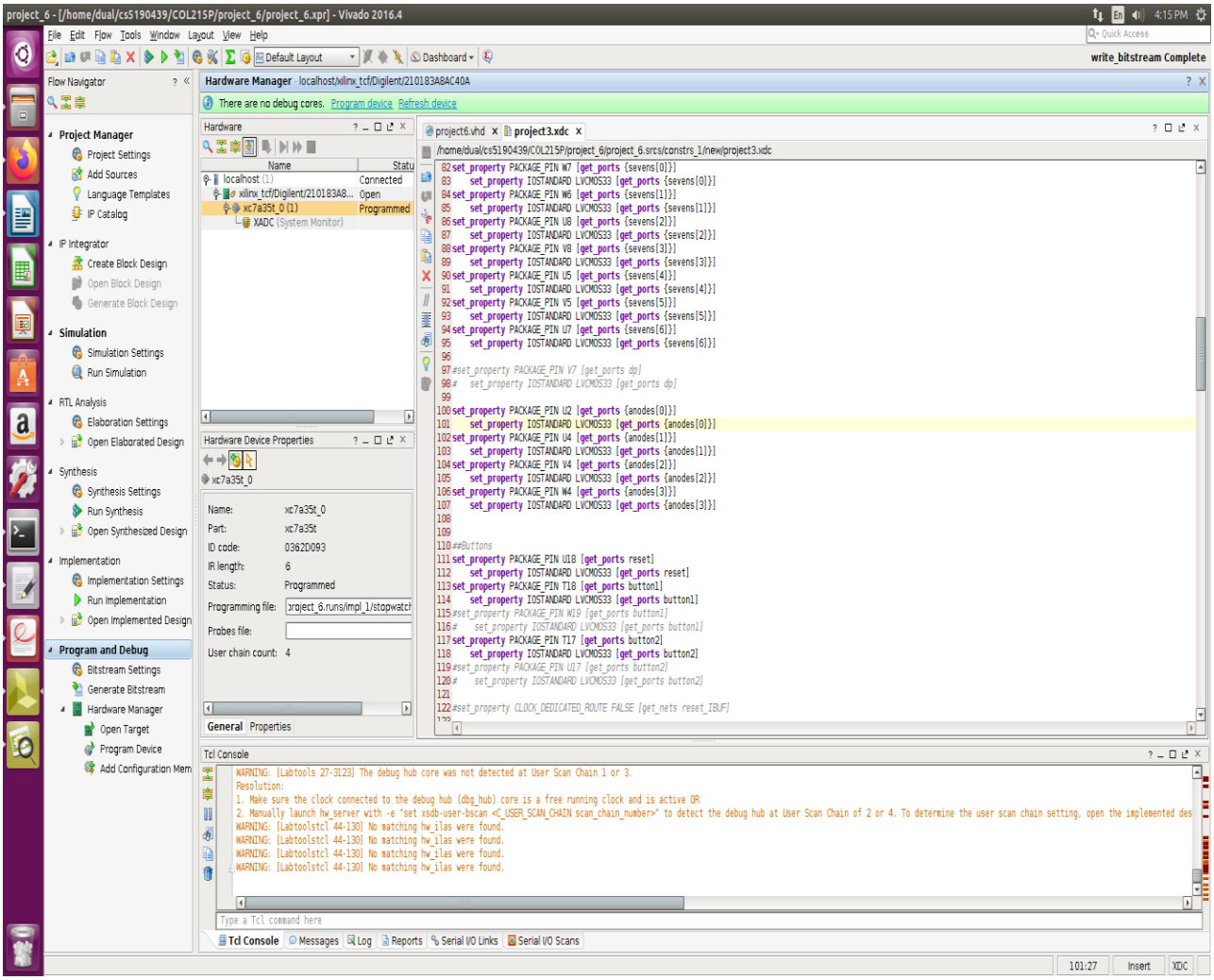
There is three button for implementation.
There are three states – START(on also reset),CONTINUE(on button1),PAUSE (on button2).
Start is from uniform 0000 digits.
When button1 pressed ,then stopwatch get start or continue on display.
When button2 pressed ,then pause the stopwatch

STATE DIAGRAM



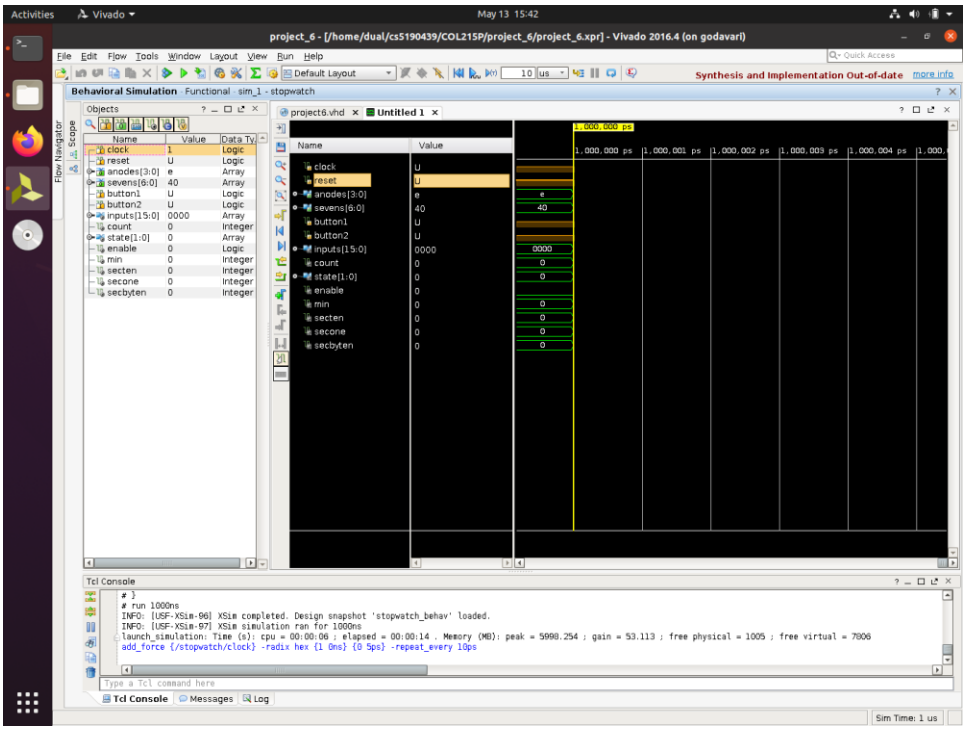
Constraint file

Anodes and cathodes matching-



Simulation on vivado

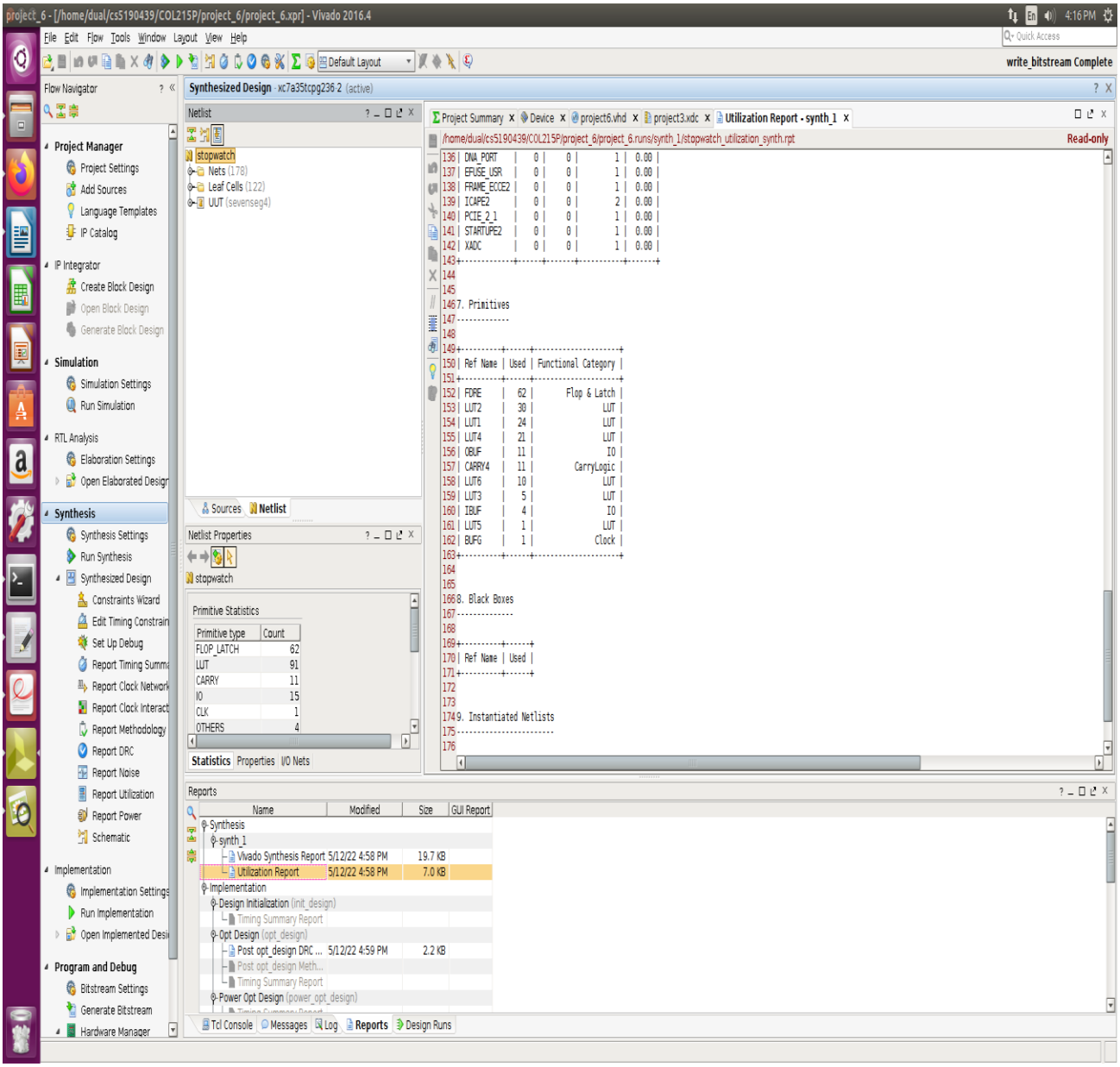
For simulation tried to use fasterb clock 10ps type and reduced counter maximum values.



But also not able to simulate large time on stopwatch as Vivado crashes unfortunately.

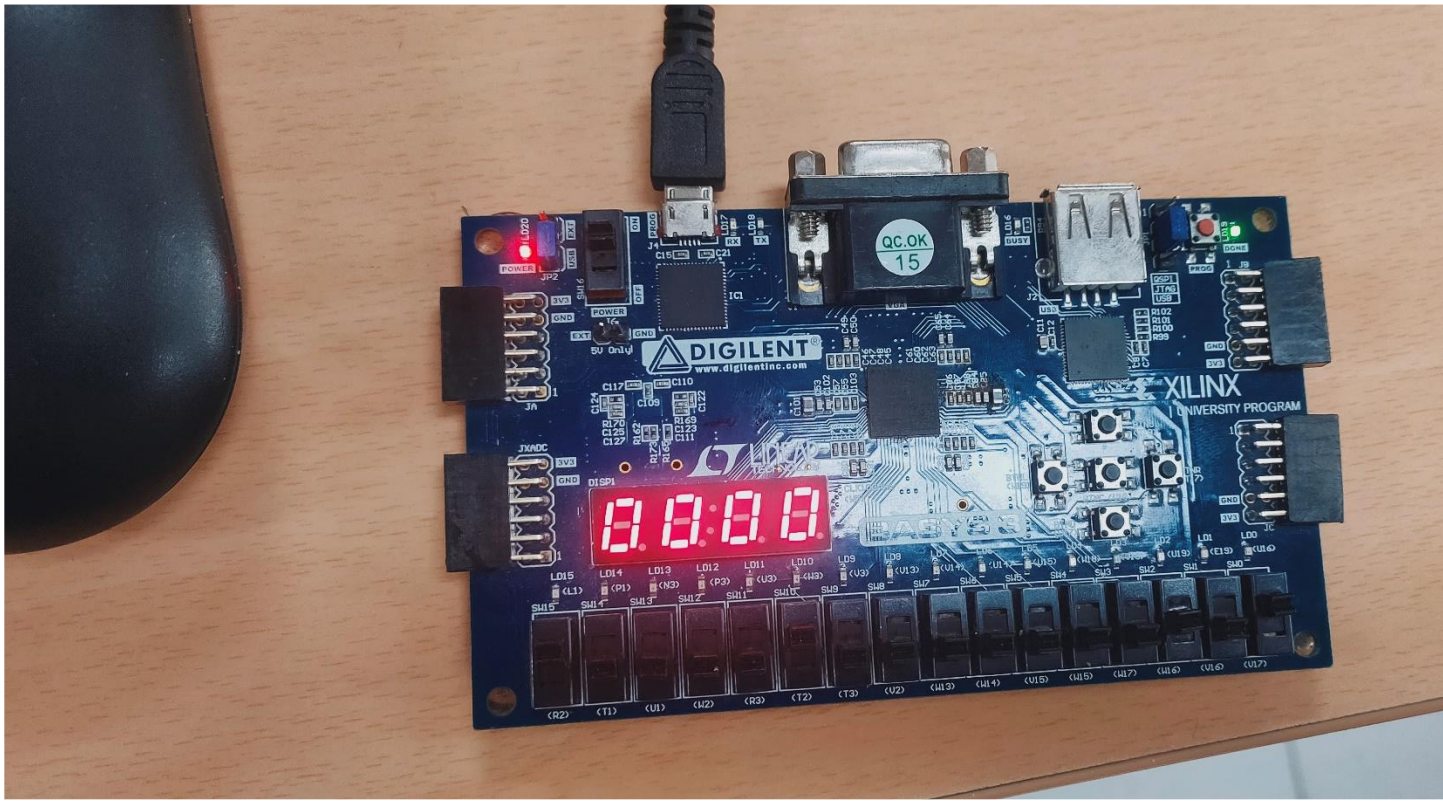
After doing above steps or till simulation work,then for implementing design on basys board, we first synthesized design, ran the implementation ,then generated Bitstream and finally opened the hardware manager to program device.

Resources utilization-

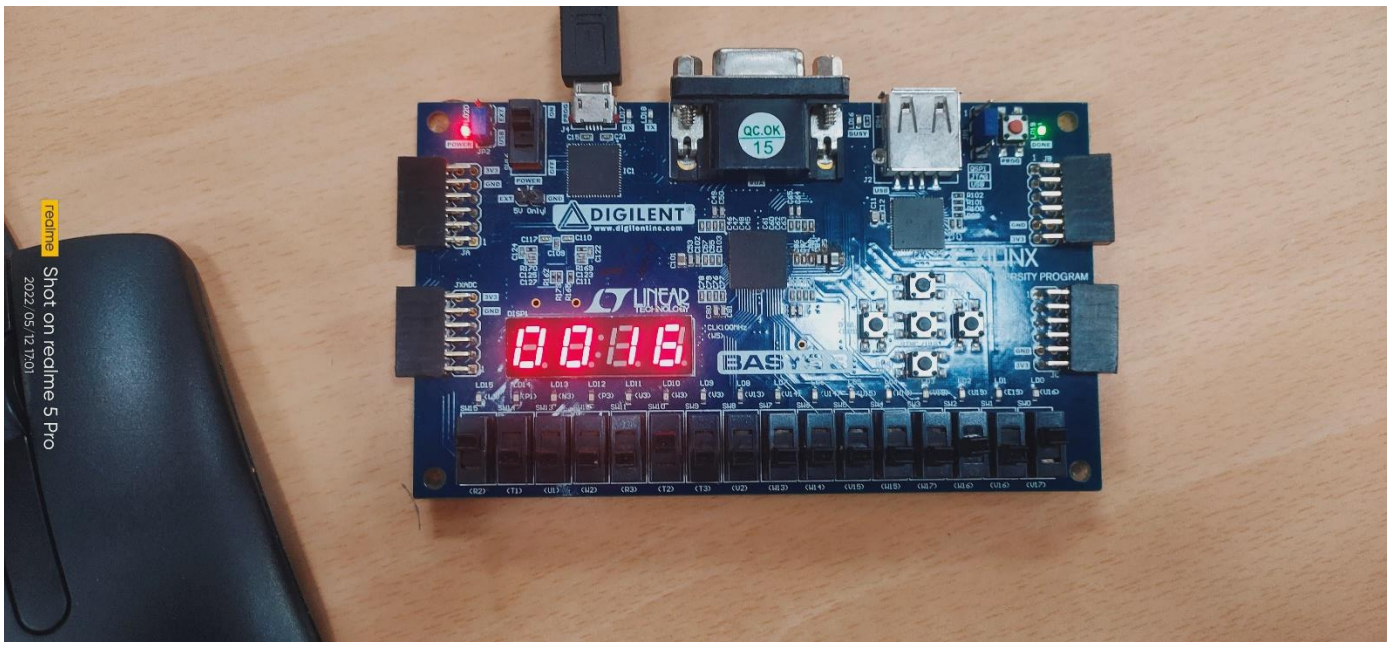


Testing on Basys3 board-

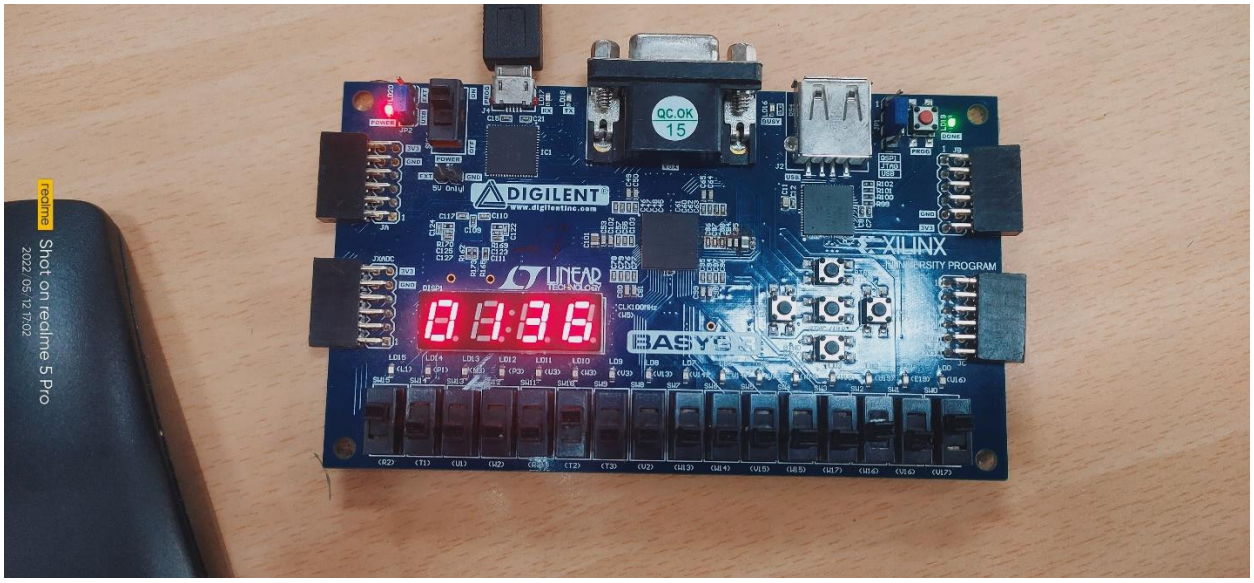
Start state-



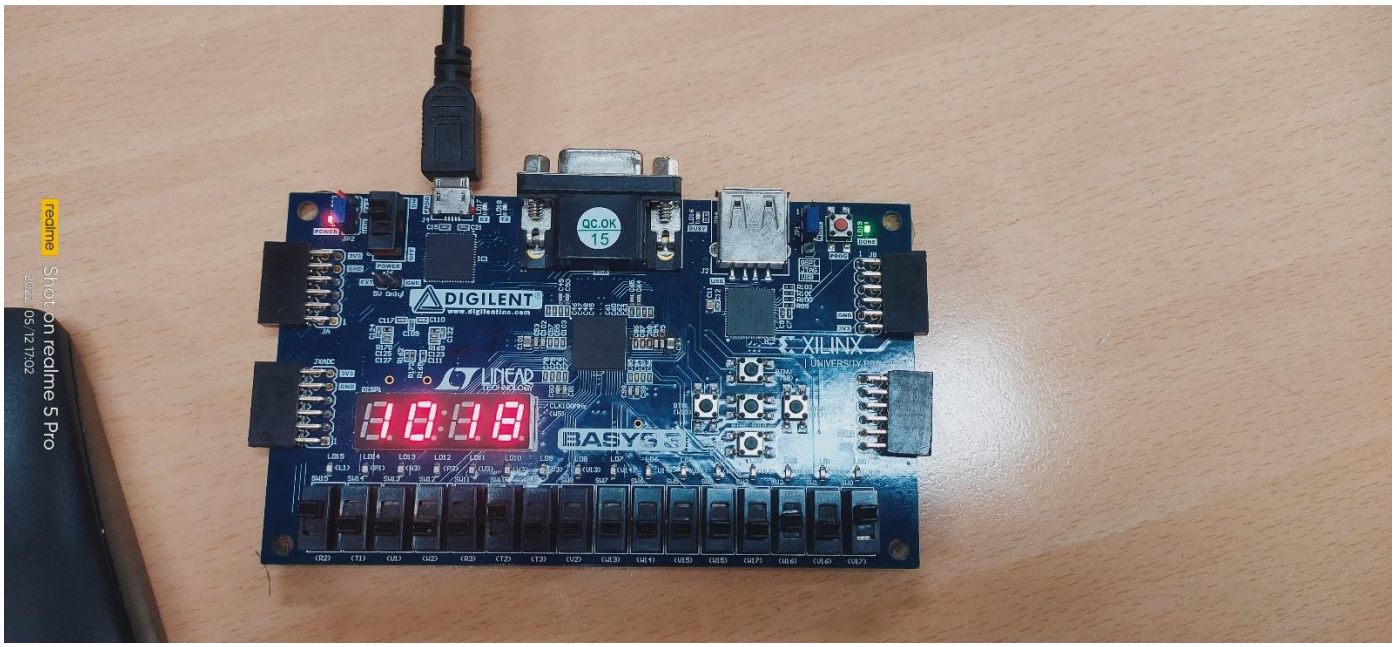
Tenth of sec and ones position of sec-



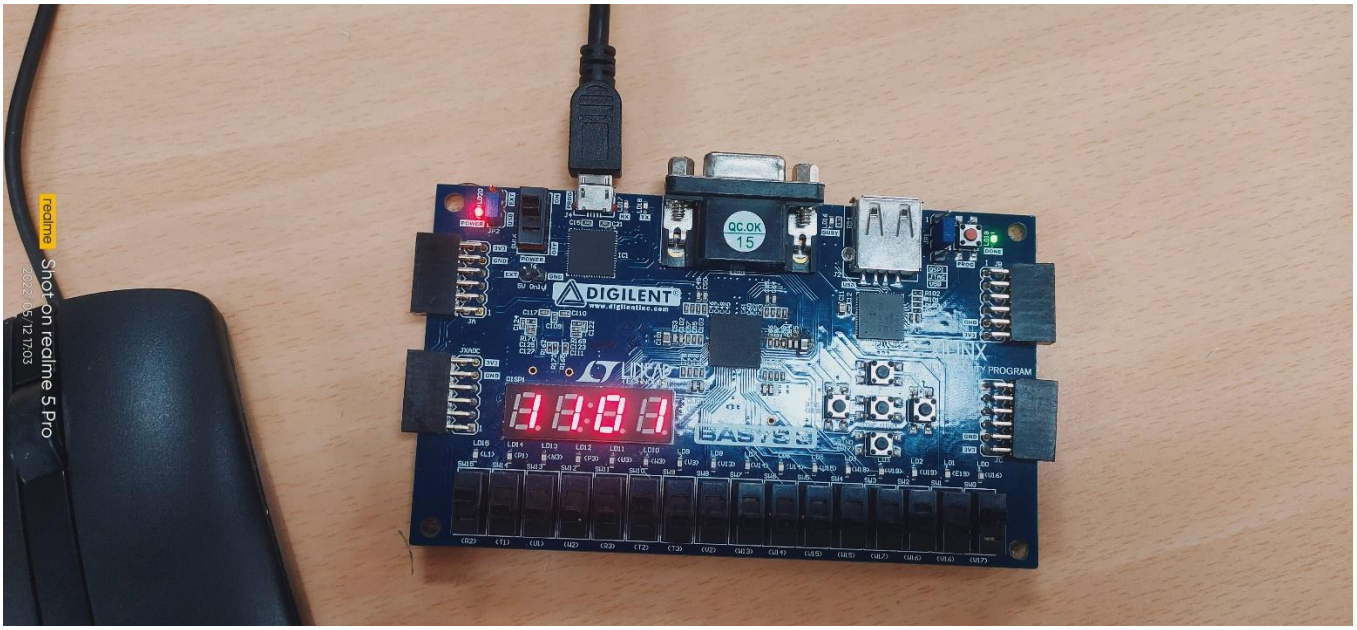
10th position of sec-

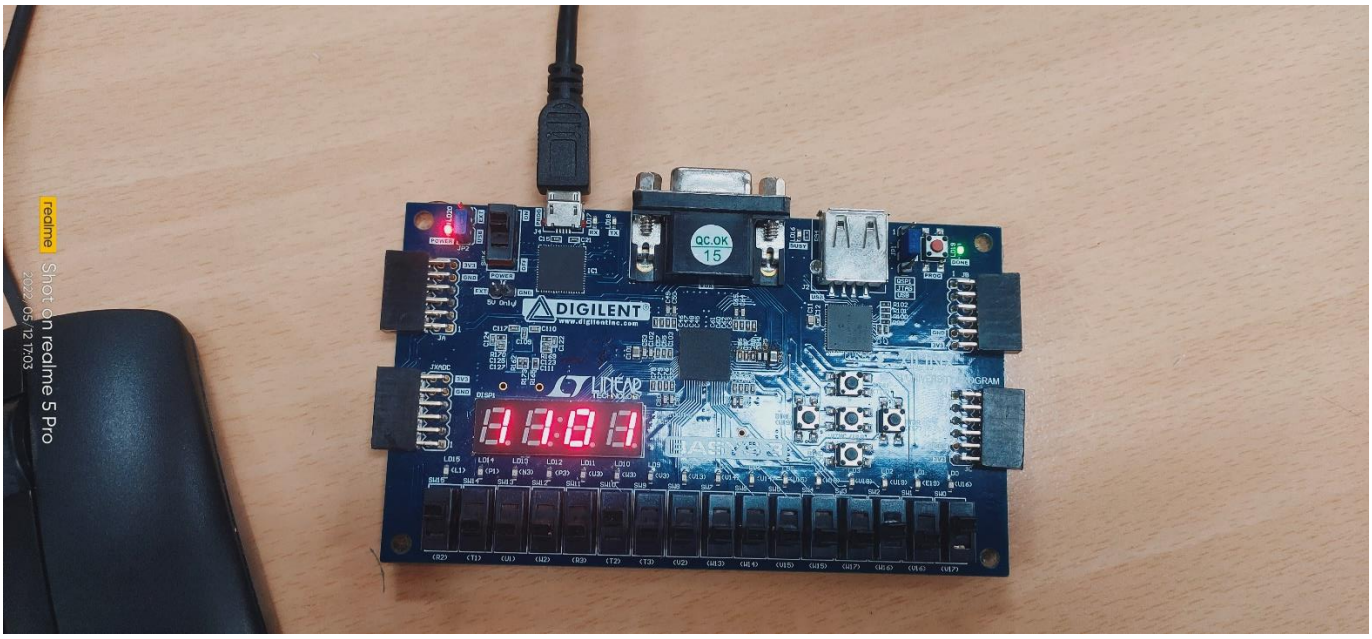


Minutes position-

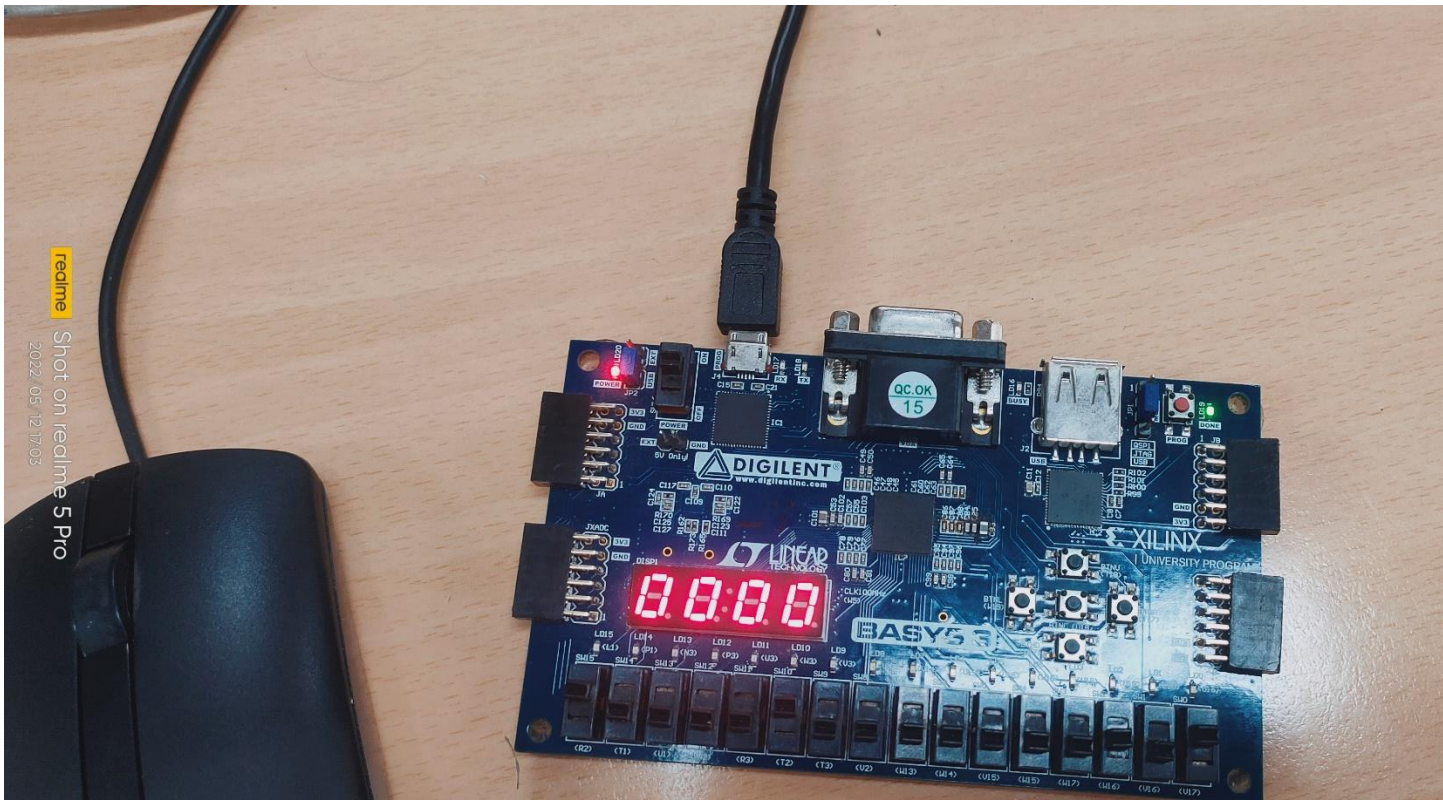


Use of pause button





Use of reset button-


realme
Shot on realme 5 Pro
2022 05 12 17:03
QC.OK
15
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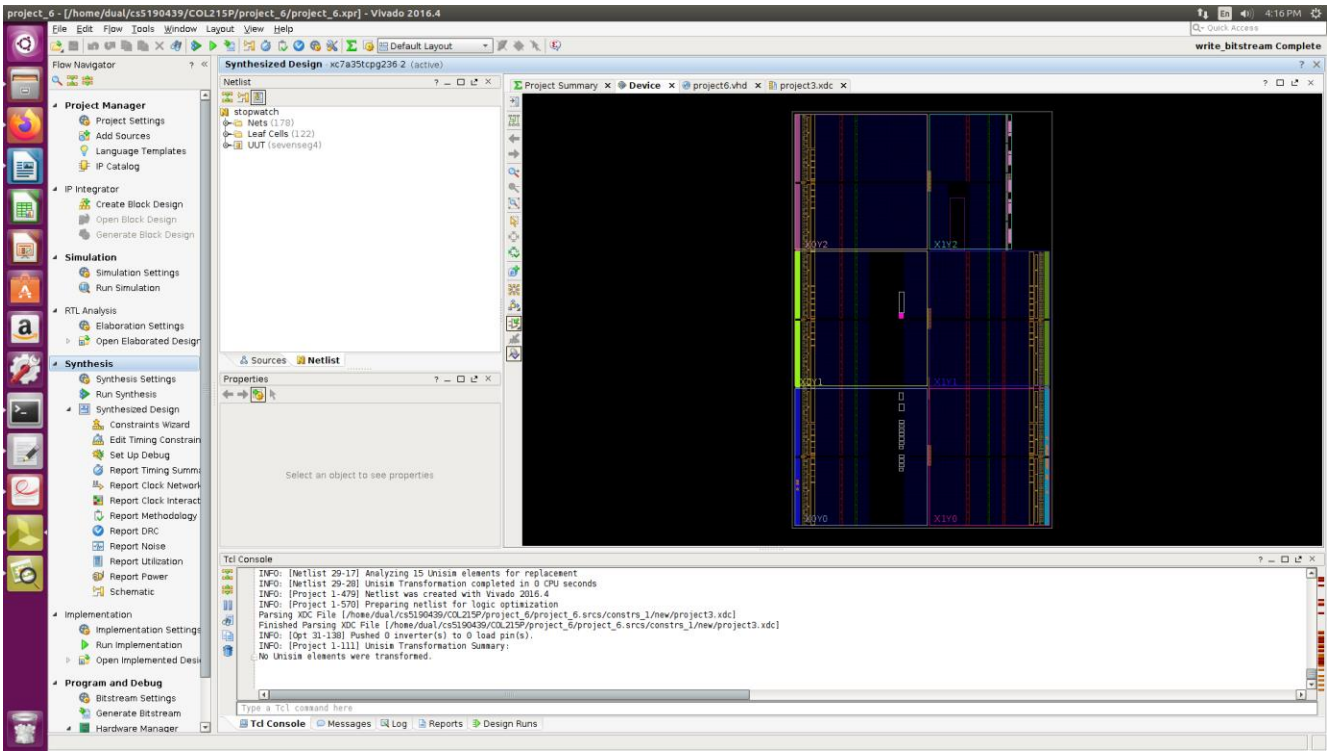
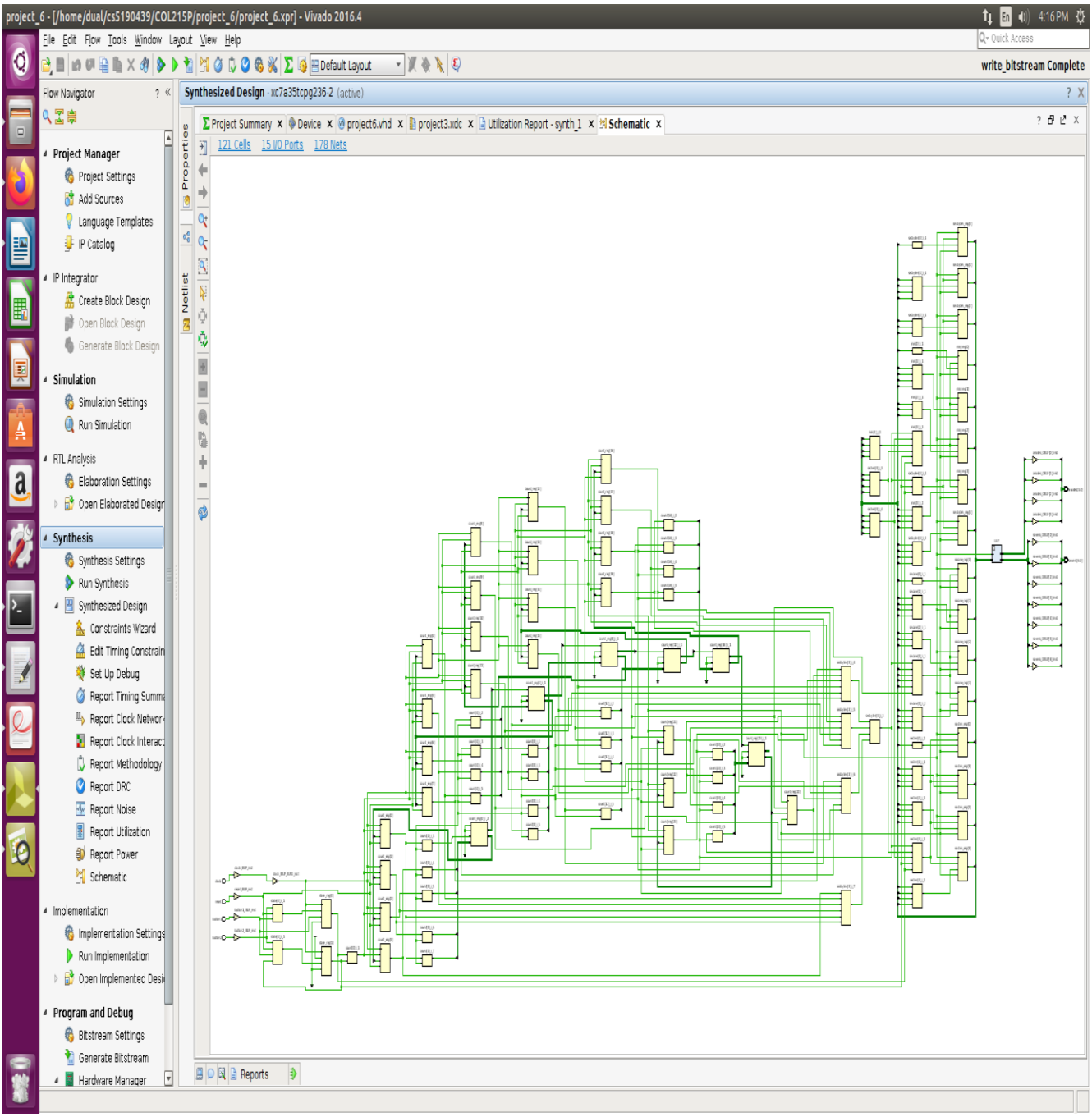
XILINX
UNIVERSITY PROGRAM
BASYS 3

Device view-



SCHEMETIC VIEW-

Here is the circuit


project_6 - [/home/dual/cs5190439/COL215P/project_6/project_6.xpr] - Vivado 2016.4
File Edit Flow Tools Window Layout View Help
Default Layout
write_bitstream Complete
Flow Navigator
Project Manager
Project Settings
Add Sources
Language Templates
IP Catalog
IP Integrator
Create Block Design
Open Block Design
Generate Block Design
Simulation
Simulation Settings
Run Simulation
RTL Analysis
Elaboration Settings
Open Elaborated Design
Synthesis
Synthesis Settings
Run Synthesis
Synthesized Design
Constraints Wizard
Edit Timing Constrain
Set Up Debug
Report Timing Summ
Report Clock Network
Report Clock Interact
Report Methodology
Report DRC
Report Noise
Report Utilization
Report Power
Schematic
Implementation
Implementation Settings
Run Implementation
Open Implemented Desi
Program and Debug
Bitstream Settings
Generate Bitstream
Hardware Manager
Synthesized Design - xc7a35tcpg236-2 (active)
Project Summary
Device
project6.vhd
project3.xdc
Utilization Report - synth_1
Schematic
121 Cells
15 I/O Ports
178 Nets
Properties
Netlist
Reports

Thank you!