ASSIGNMNET-8

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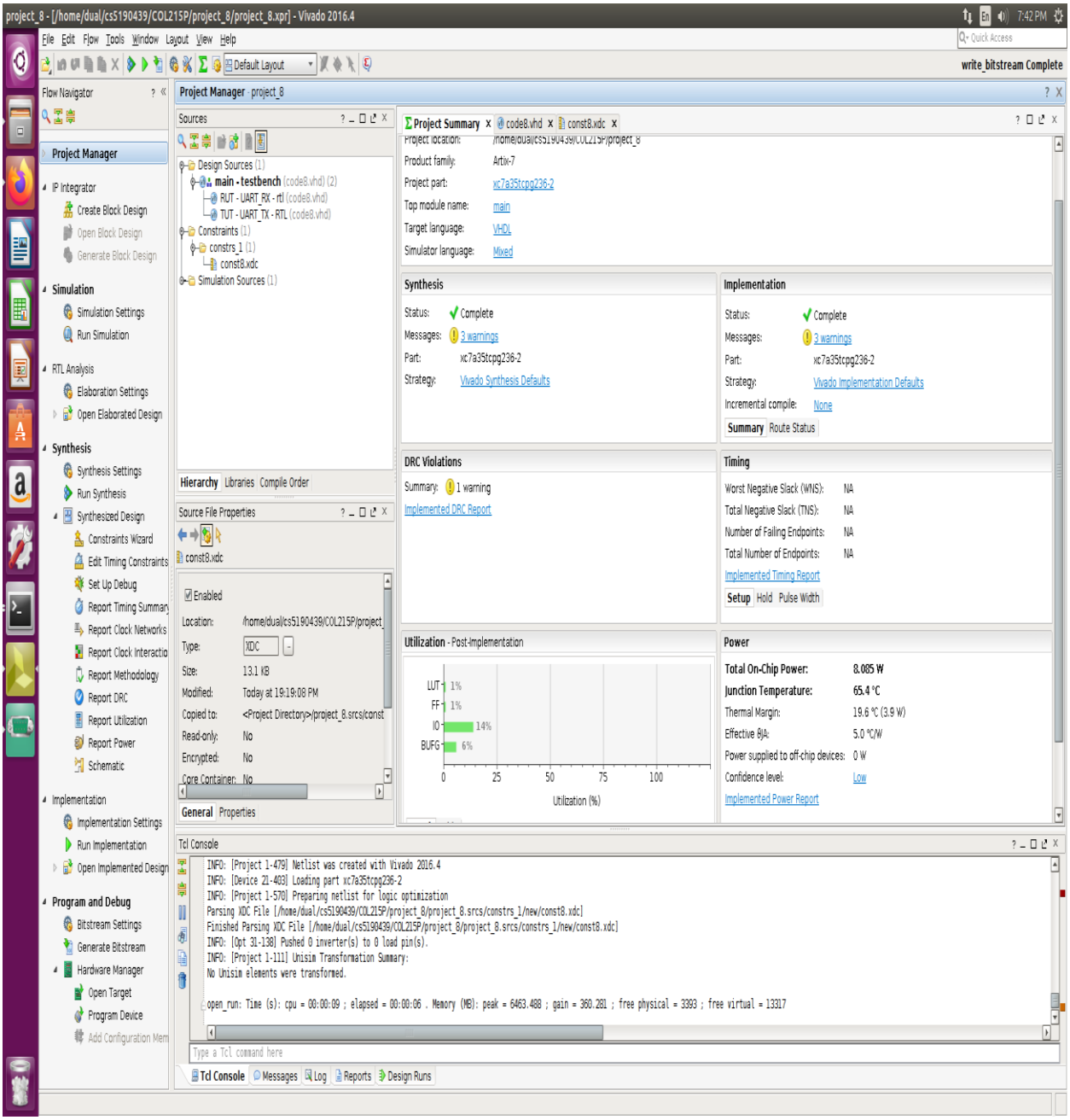
In this assignment we have learned to send serial information without a shared clock. Also designed asynchronous serial transmitter to create a loop with the receiver developed in the previous assignment

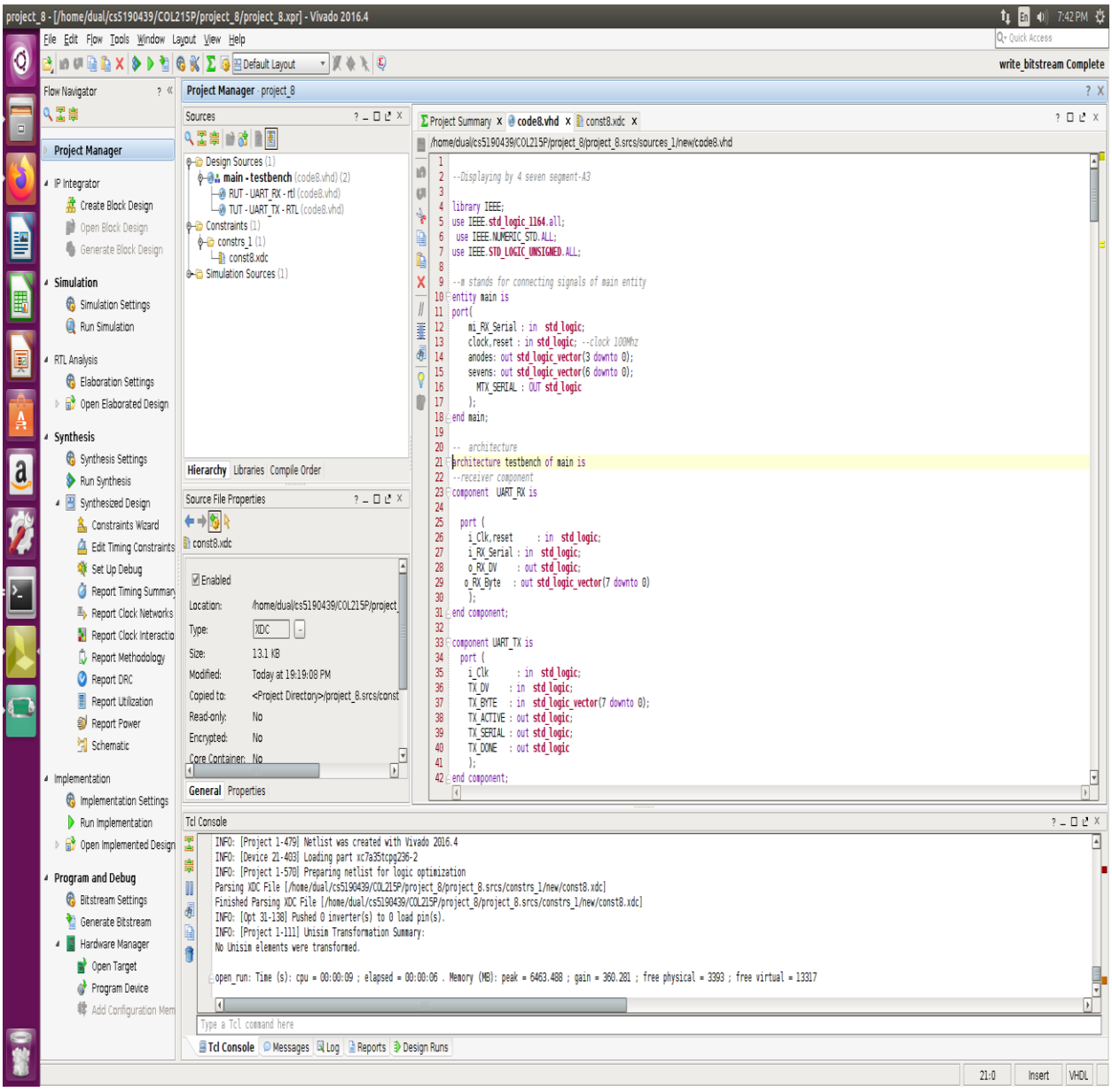
Submission folder (2019CS50439_2019CS50434) contains -

- **Const8.xdc - constraint file**
- **code_8.vhd -vhdl code file**
- **main.bit - bitstream file**
- **A8_report.pdf- report file**

New project8 on Vivado-



VHDL code on Vivado -



The code is also provided in the submission file

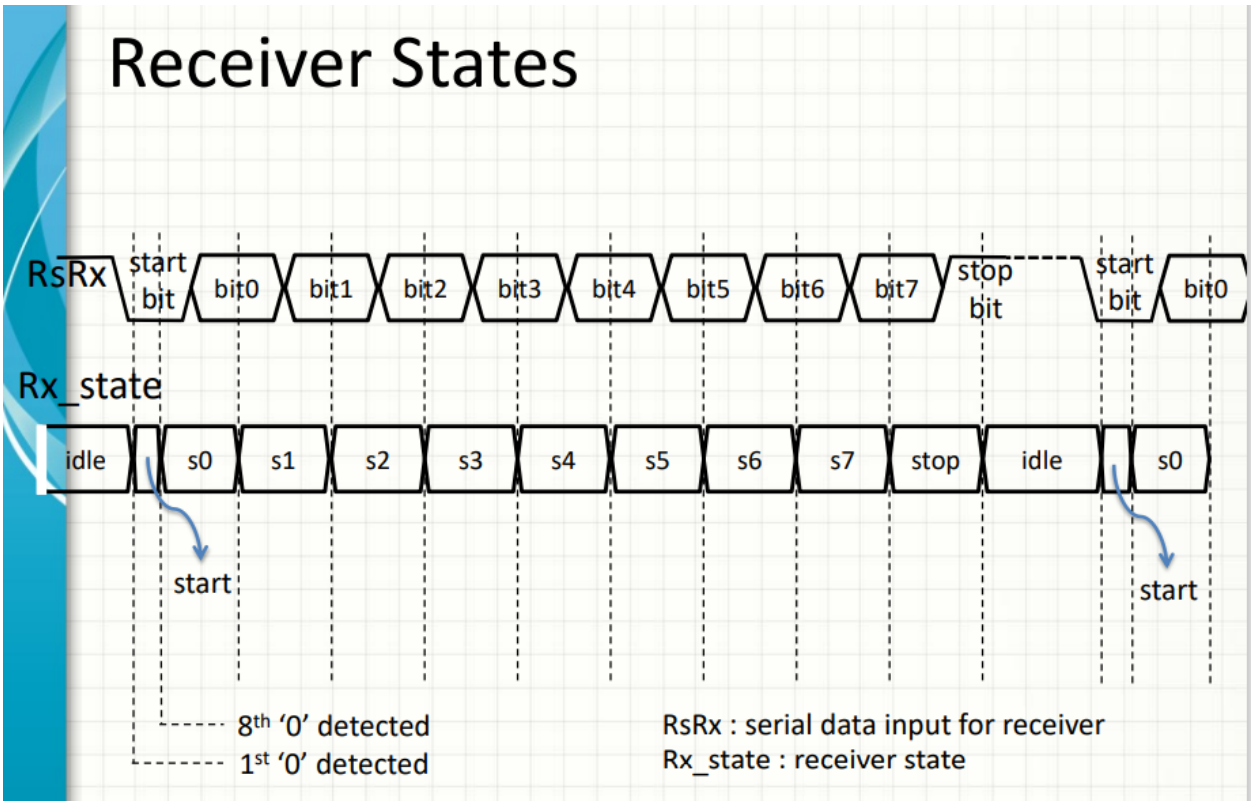
DESCRIPTION

Here we assumed normal indexing of segments of seven segment display(B-2,etc)

Design decision

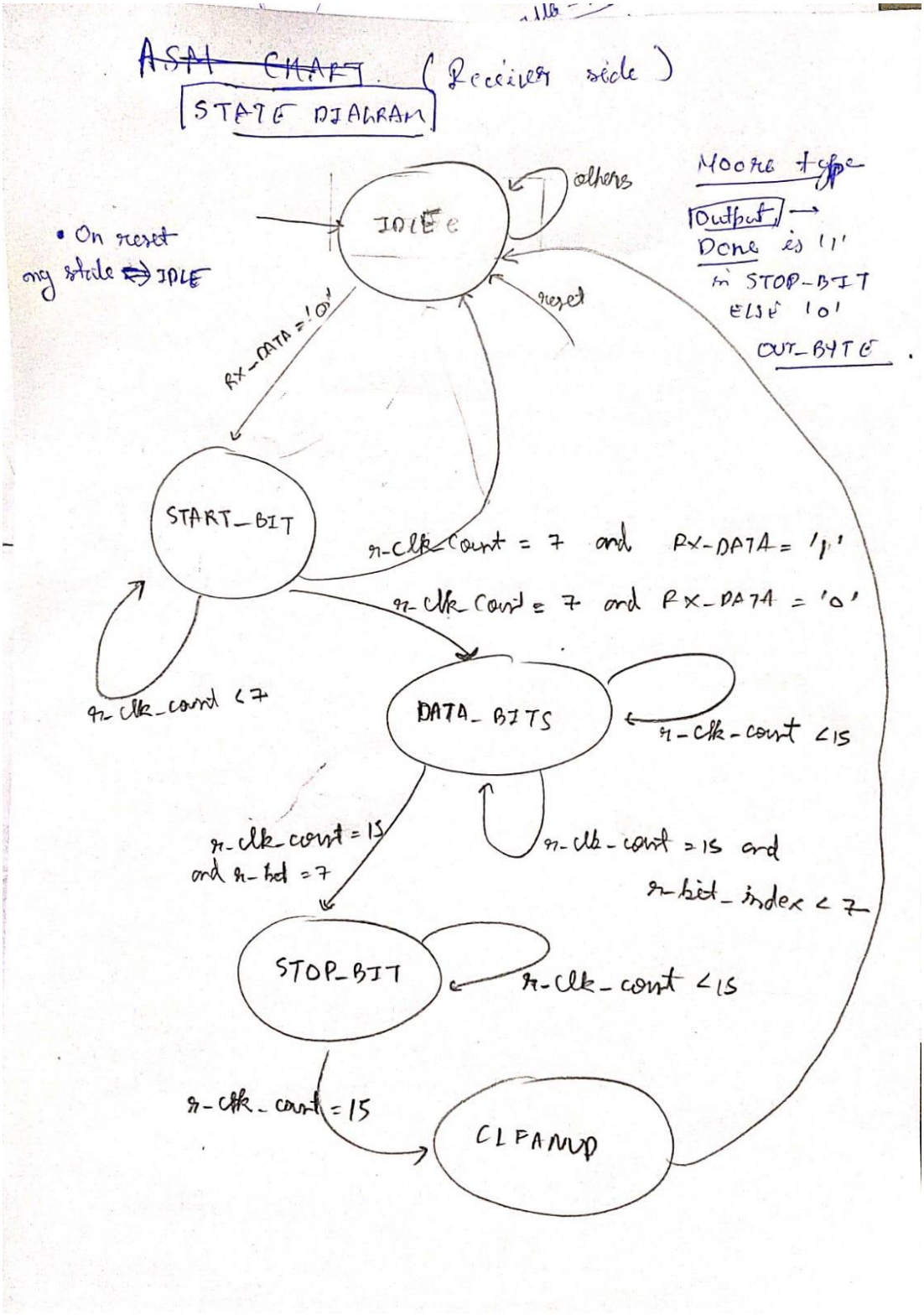
Designed asynchronous serial receiver/transmitter with baud rate = 9600, 8 data bits, no parity bits and 1 stop bit.
Made a provision for resetting the FSM to idle state by a push button(display “00”),

Receiver-
Receiver component have serial input and parallel byte output,which we are storing to display on seven segment display.
For others Simply followed states idea learned from lectures(below image)-



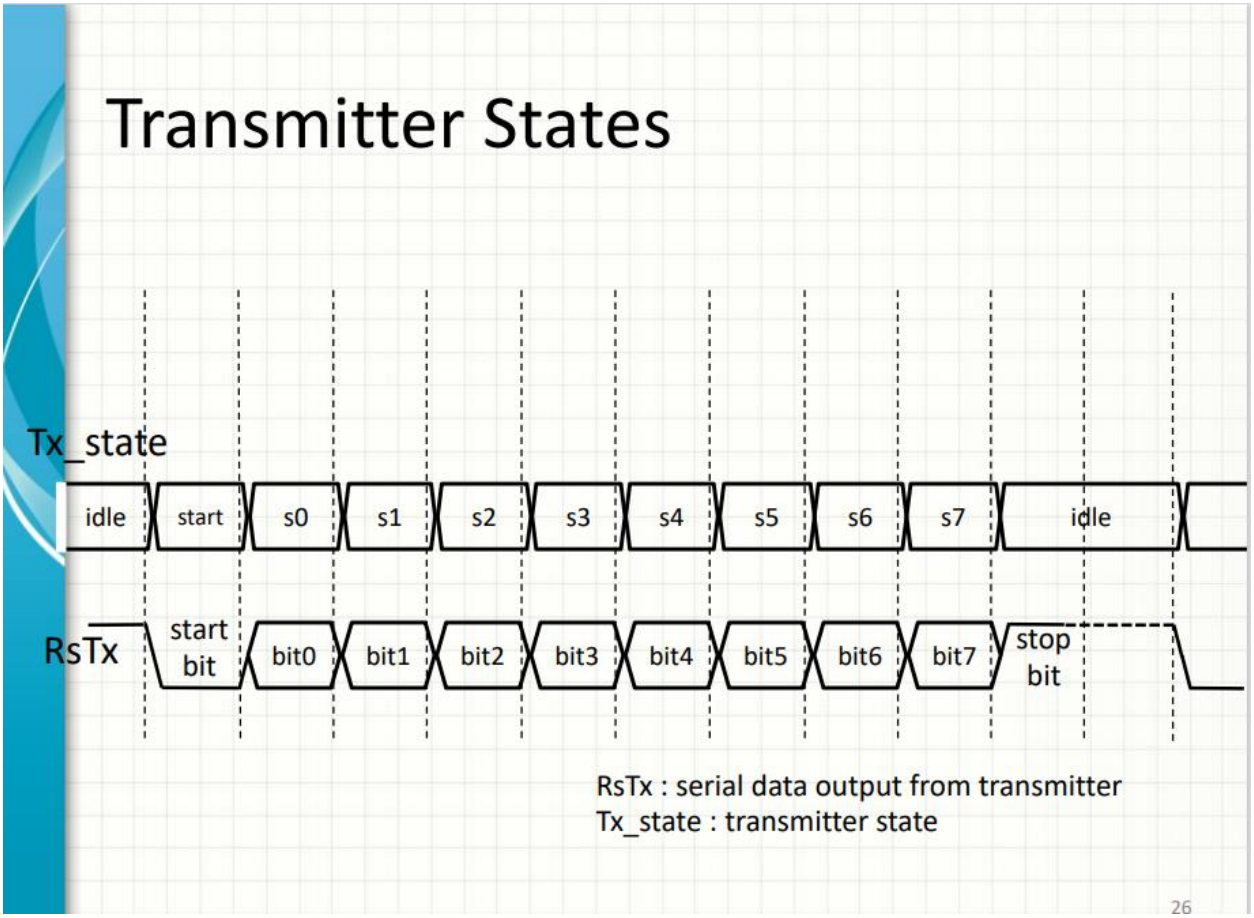
Here in state diagram ,we can find how these total 5 states related (IDLE,START_BIT,DATA_BITS,STOP_BIT,CLEANUP)-

STATE DIAGRAM-Receiver

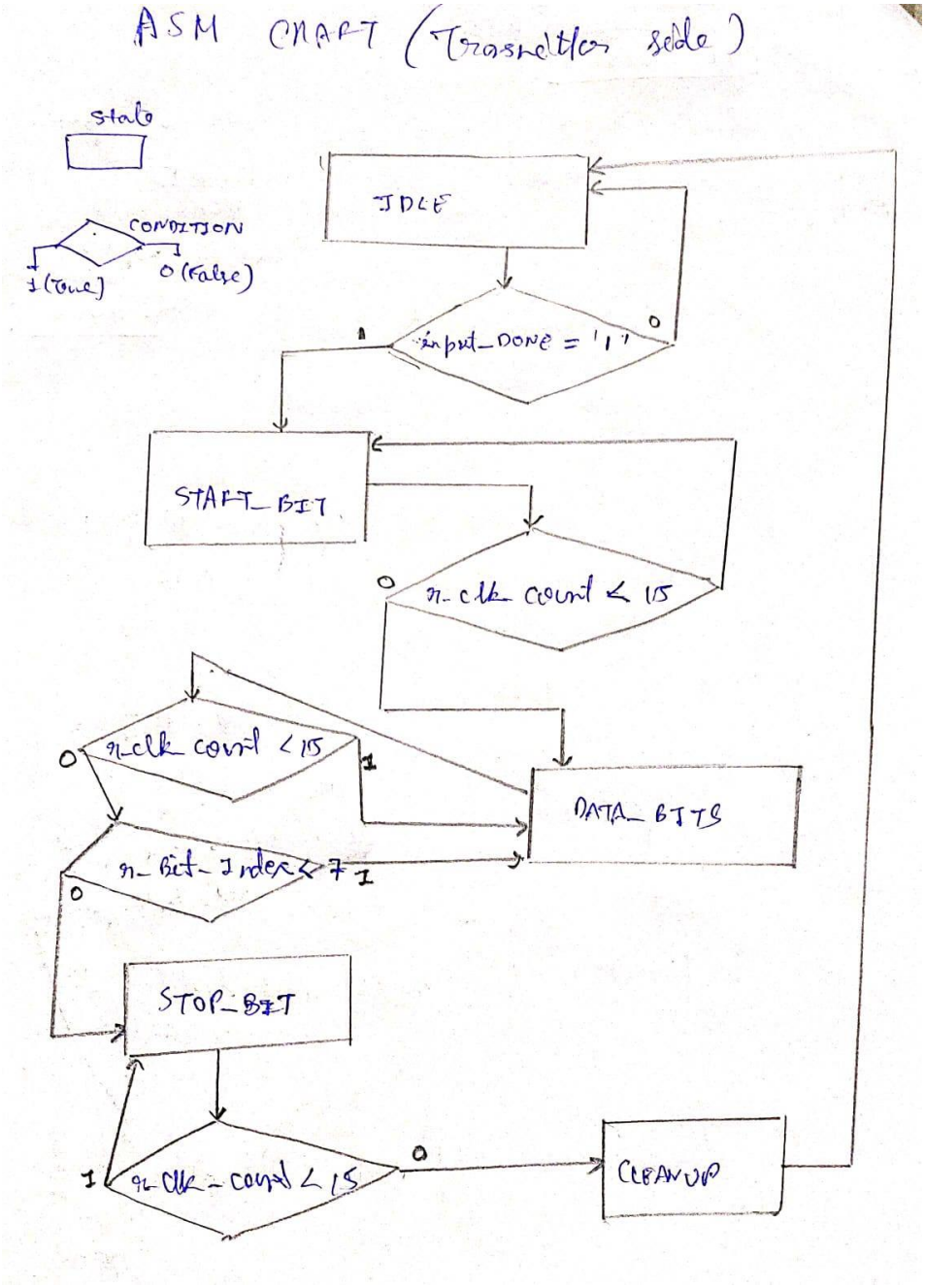


Transmitter-

Transmitter component also have similar 5 states with tstate type and related as-(IDLE,START_BIT,DATA_BITS,STOP_BIT,CLEANUP).

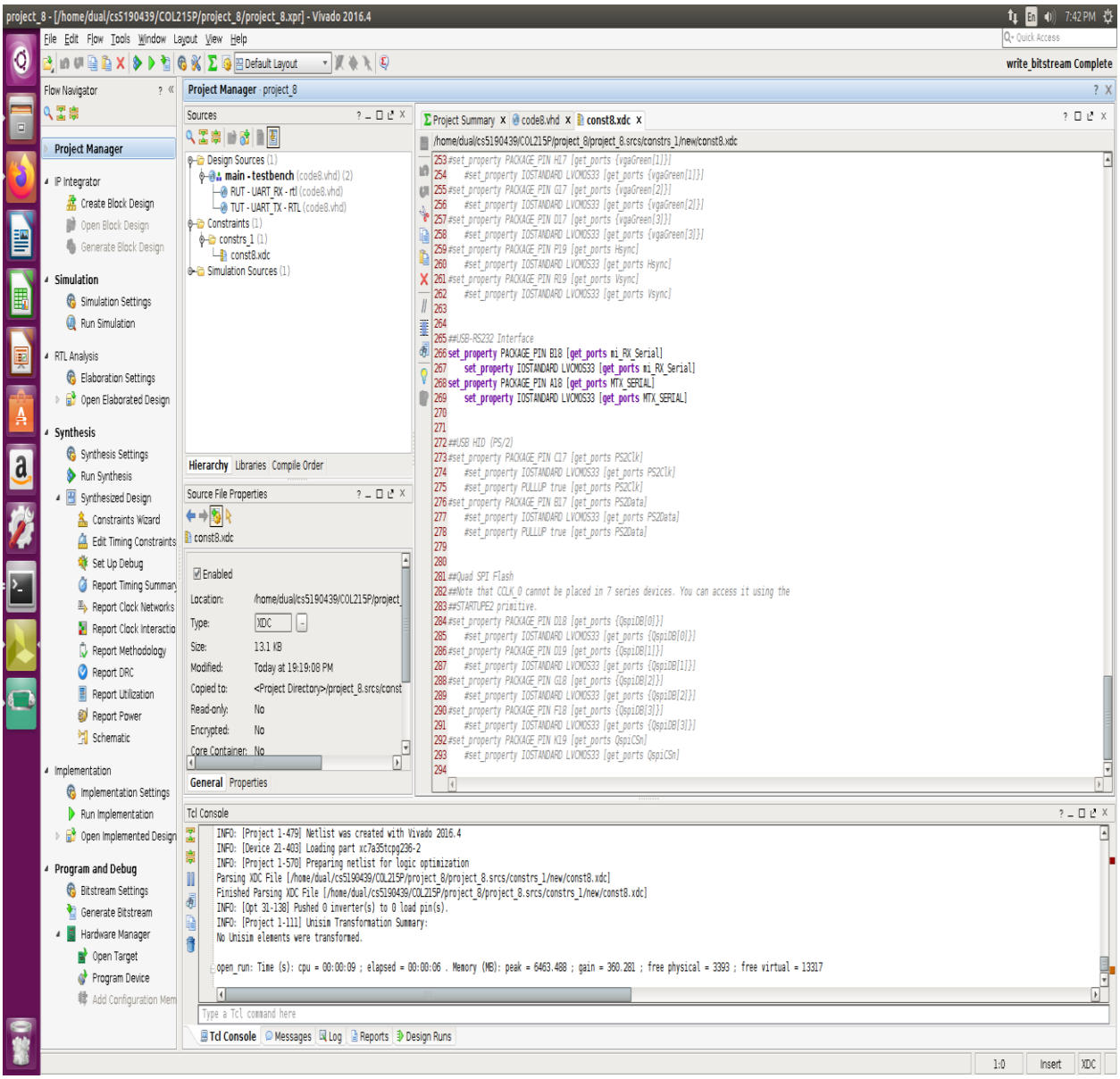


STATE DIAGRAM/ASM CHART-Transmitter



Constraint file

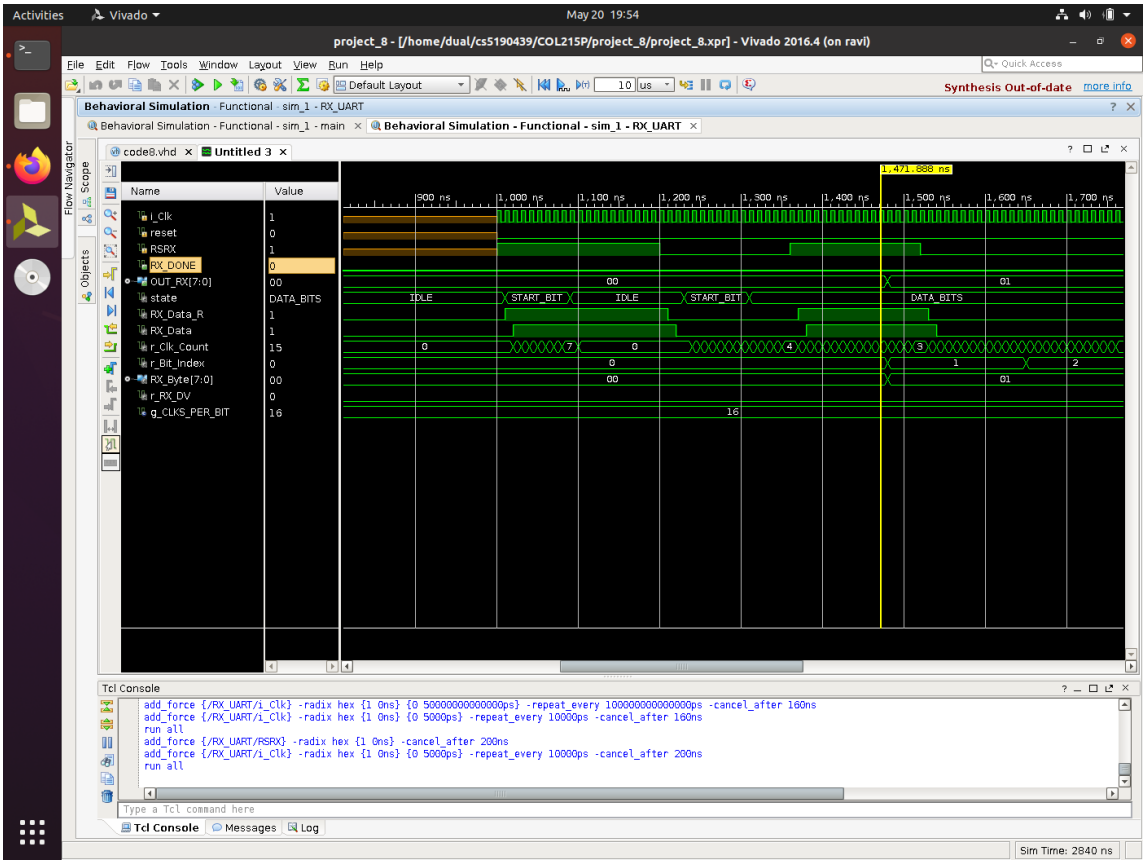
Matched receiver serial input port and transmitter serial output port in addition to previous A3 ports of displaying 7 segment display

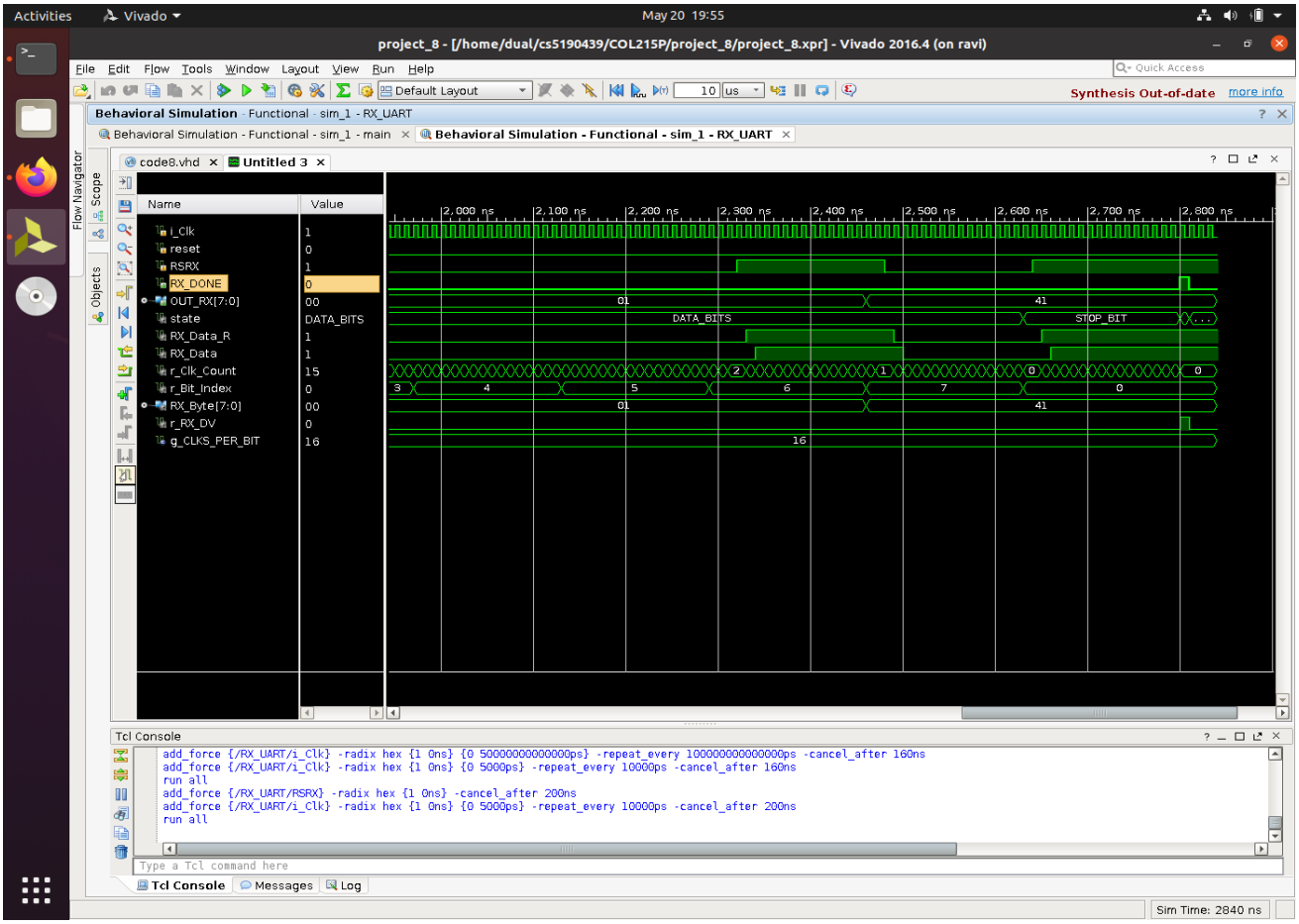


Simulation on vivado

For simulation tried to use one clock of 16* baud rate for single “A” character

Here wave generated can be found similar to theoretical conceptual diagram told above.

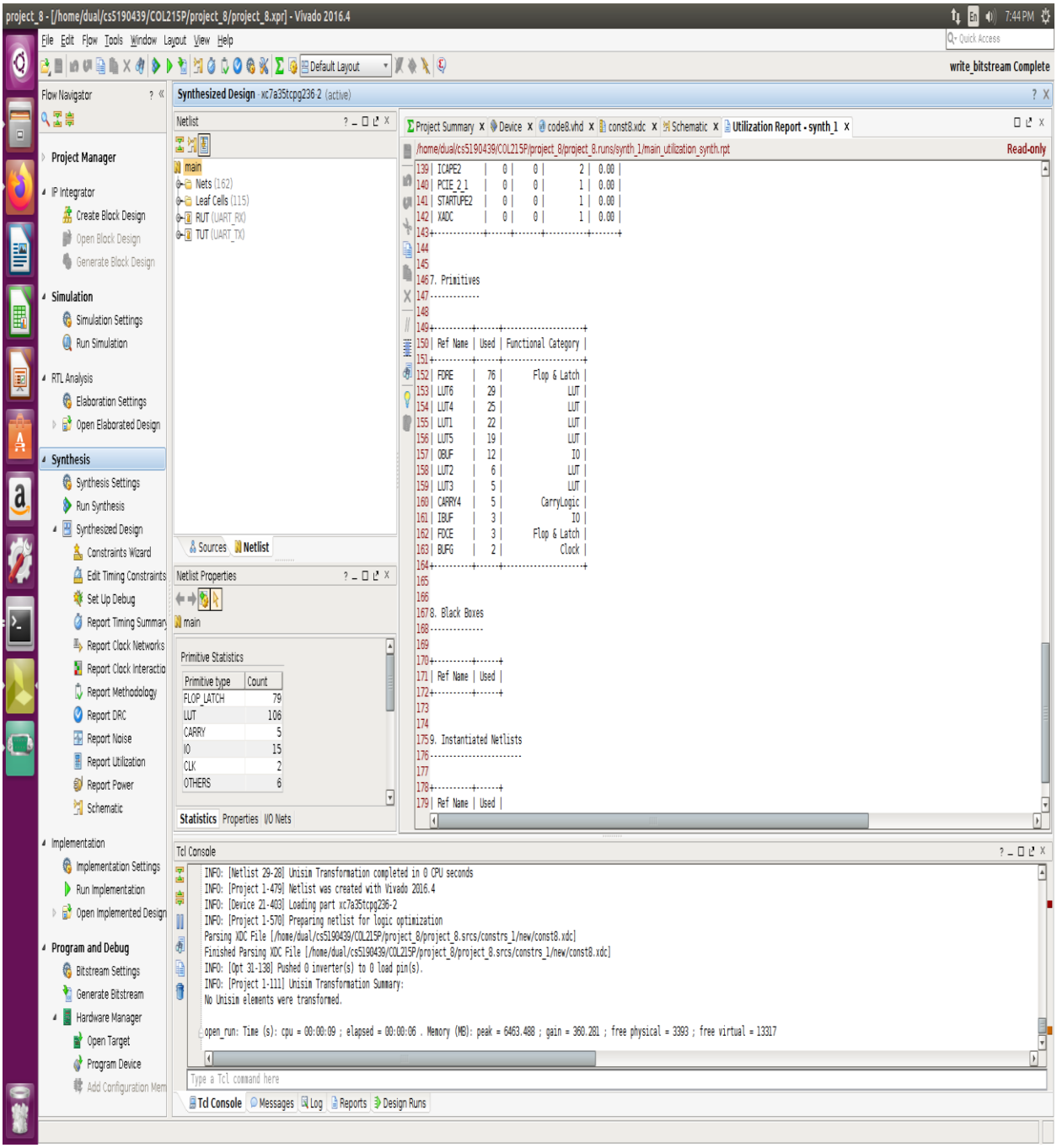




Similarly simulation of transmitter component also have wave similar to theoretical told image above in description.

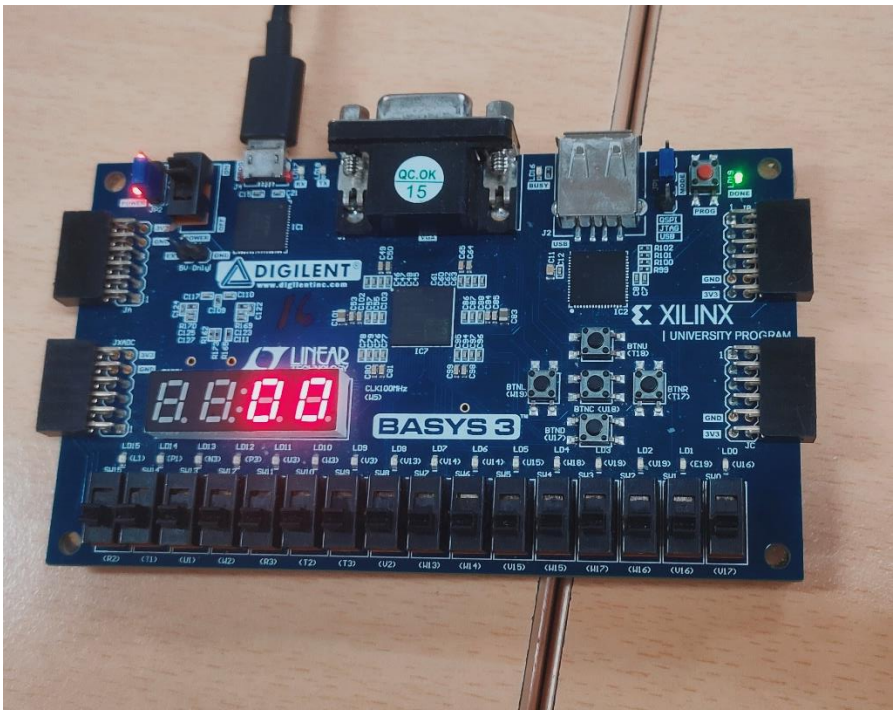
After doing above steps or till simulation work,then for implementing design on basys board, we first synthesized design, ran the implementation ,then generated Bitstream and finally opened the hardware manager to program device.

Resources utilization-

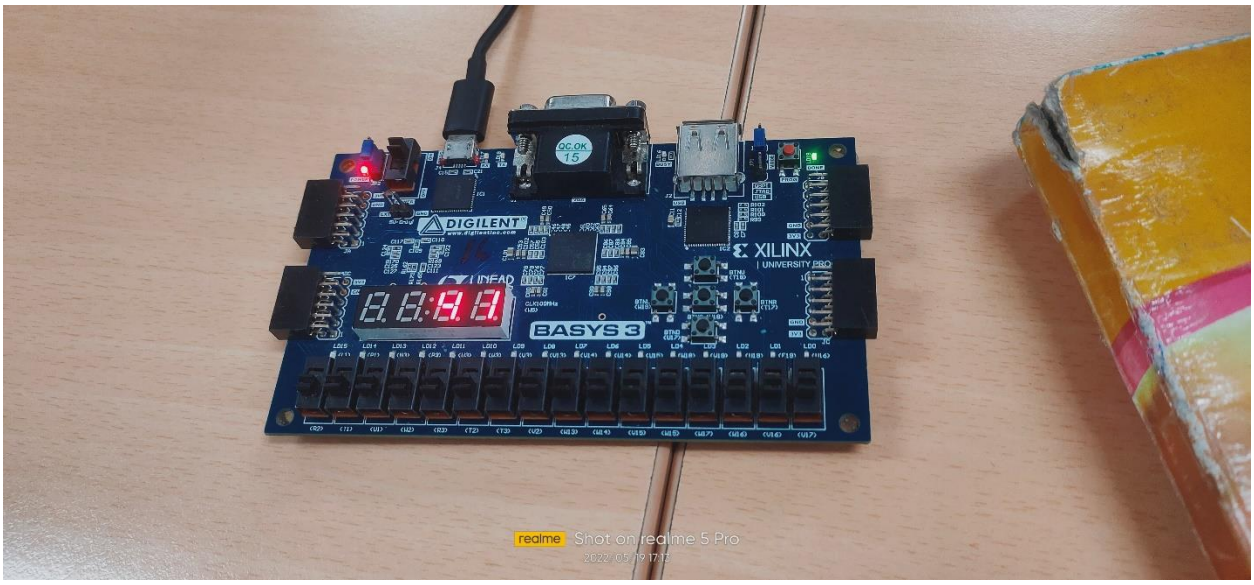


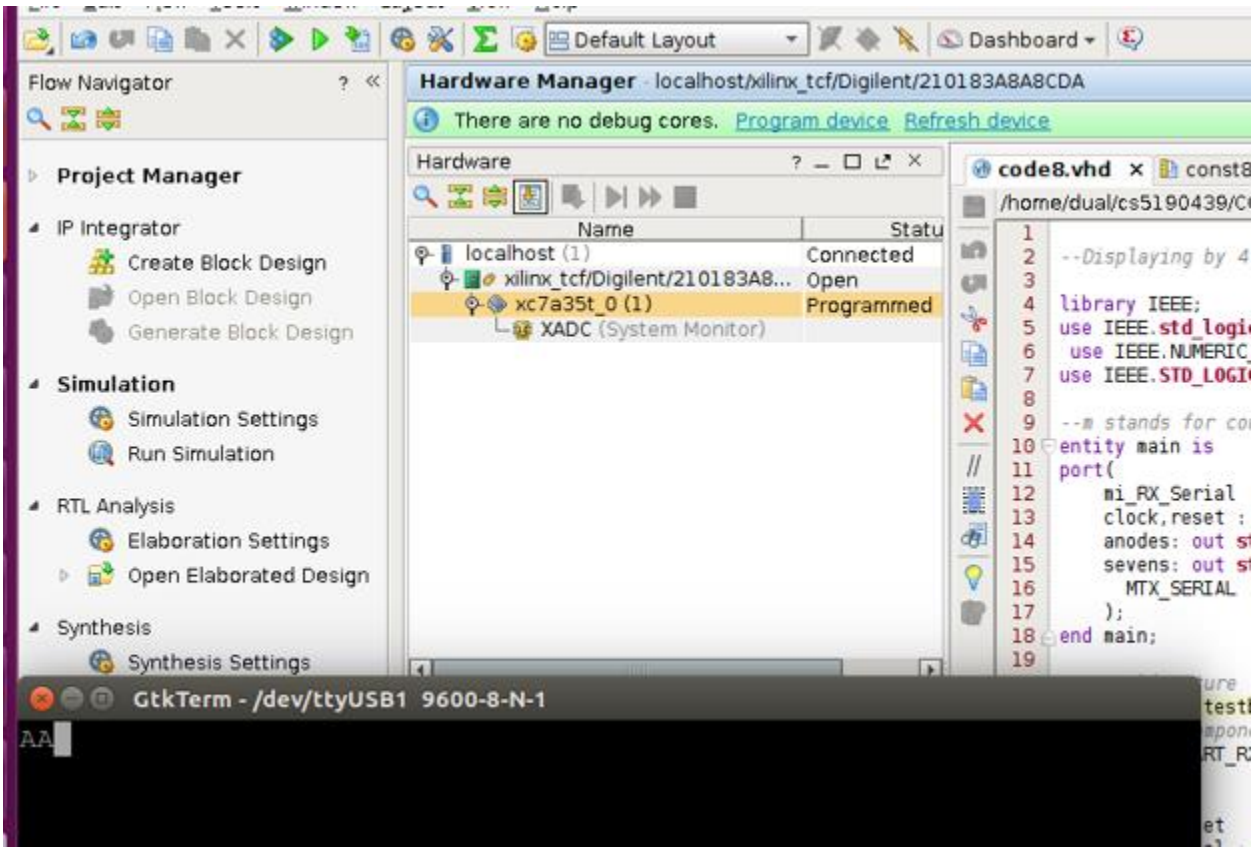
Testing on Basys3 board and gtk-

initial state-

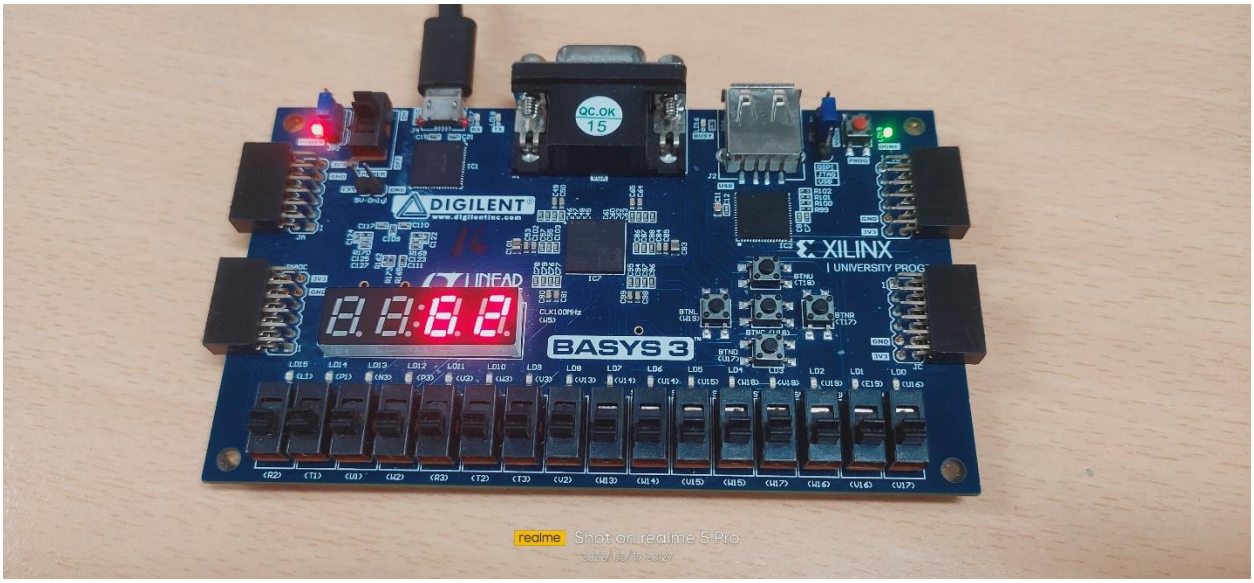


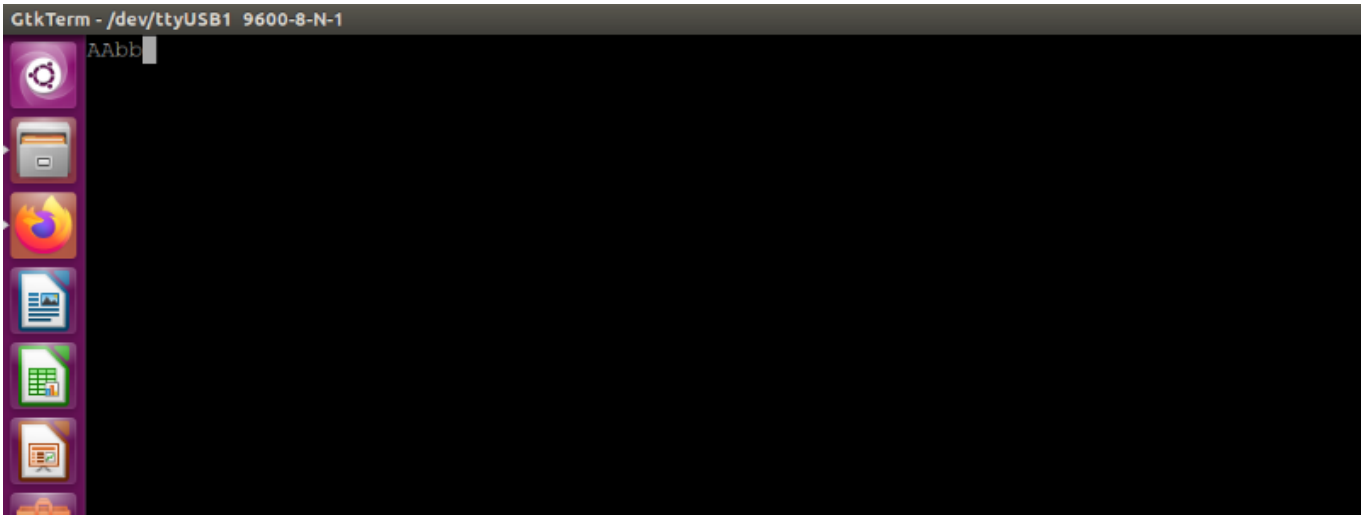
When A,ASCII Char pressed on keyboard,then display showing hexadecimal representation-



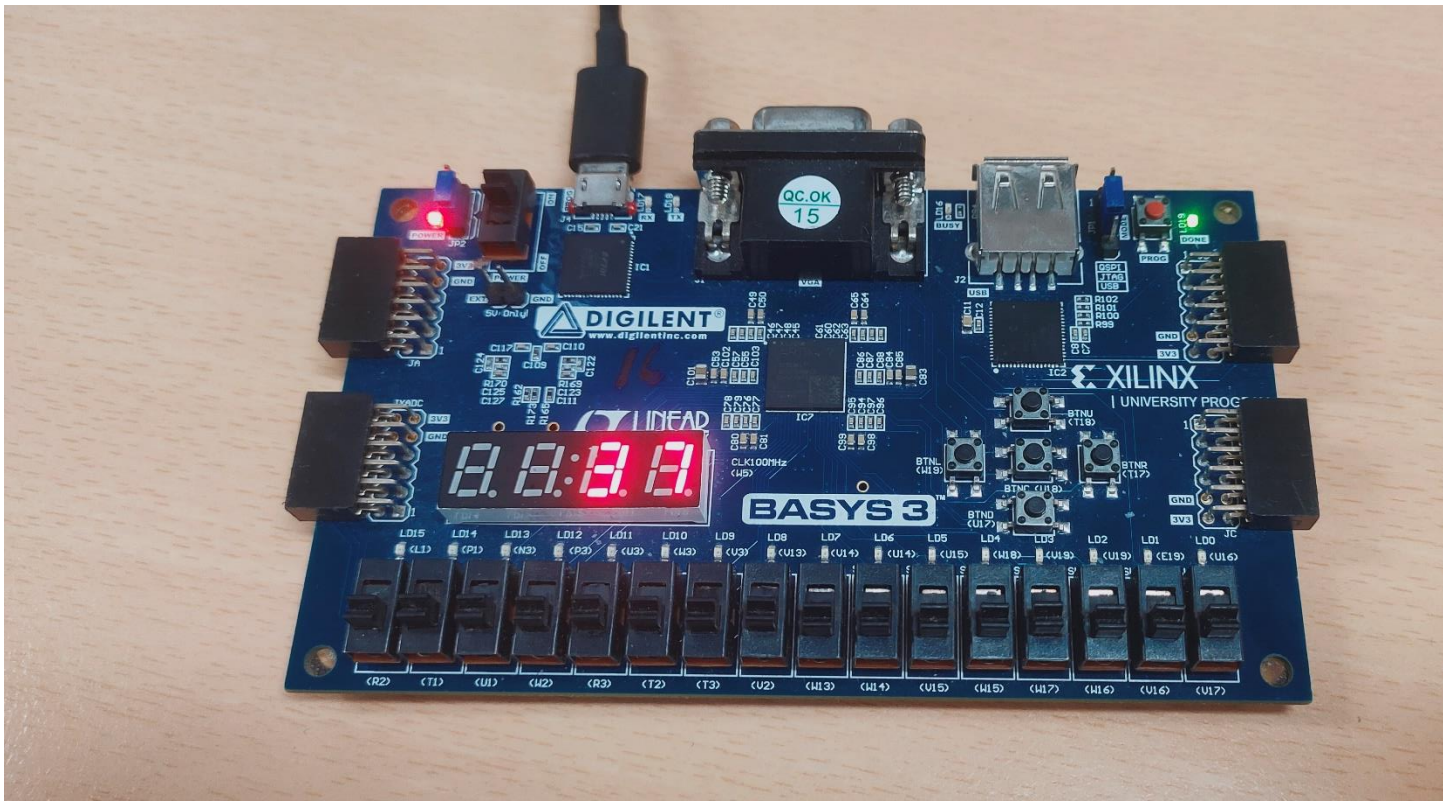


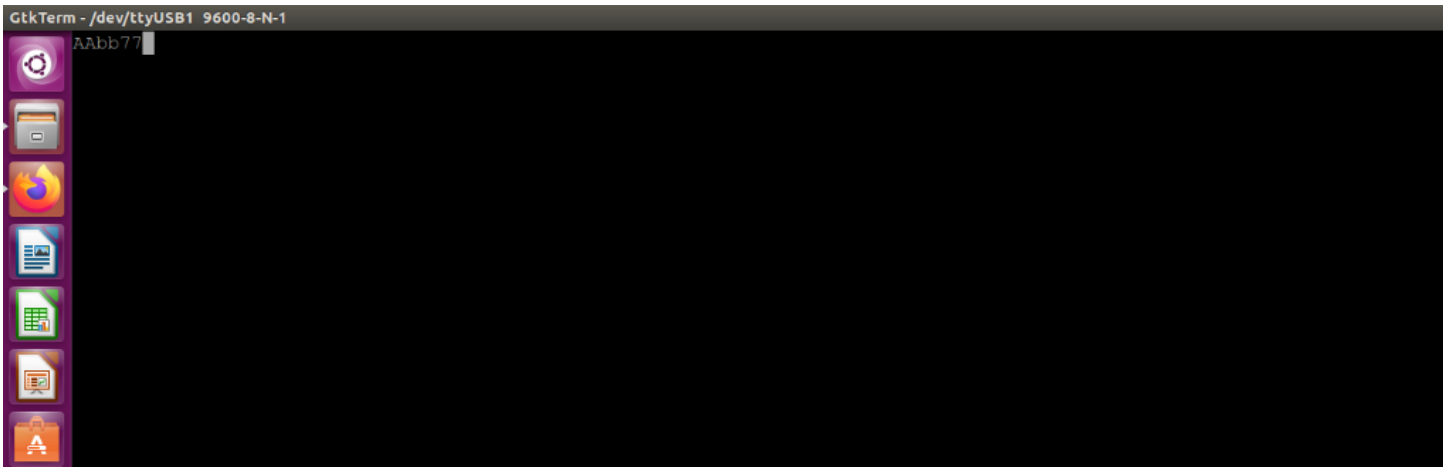
When b,ASCII Char pressed on keyboard,then display showing hexadecimal representation-





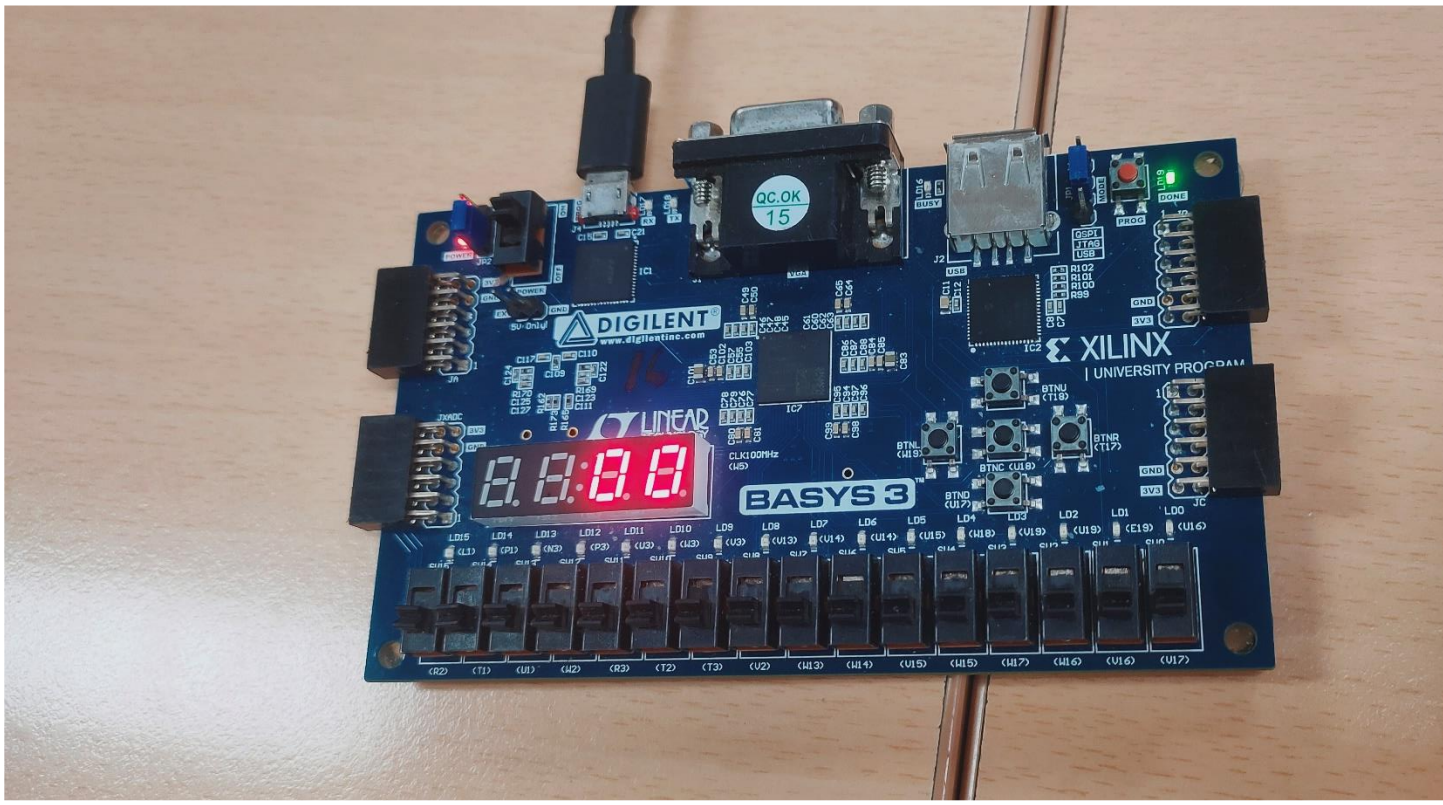
When 7,ASCII Char pressed on keyboard,then display showing hexadecimal representation-



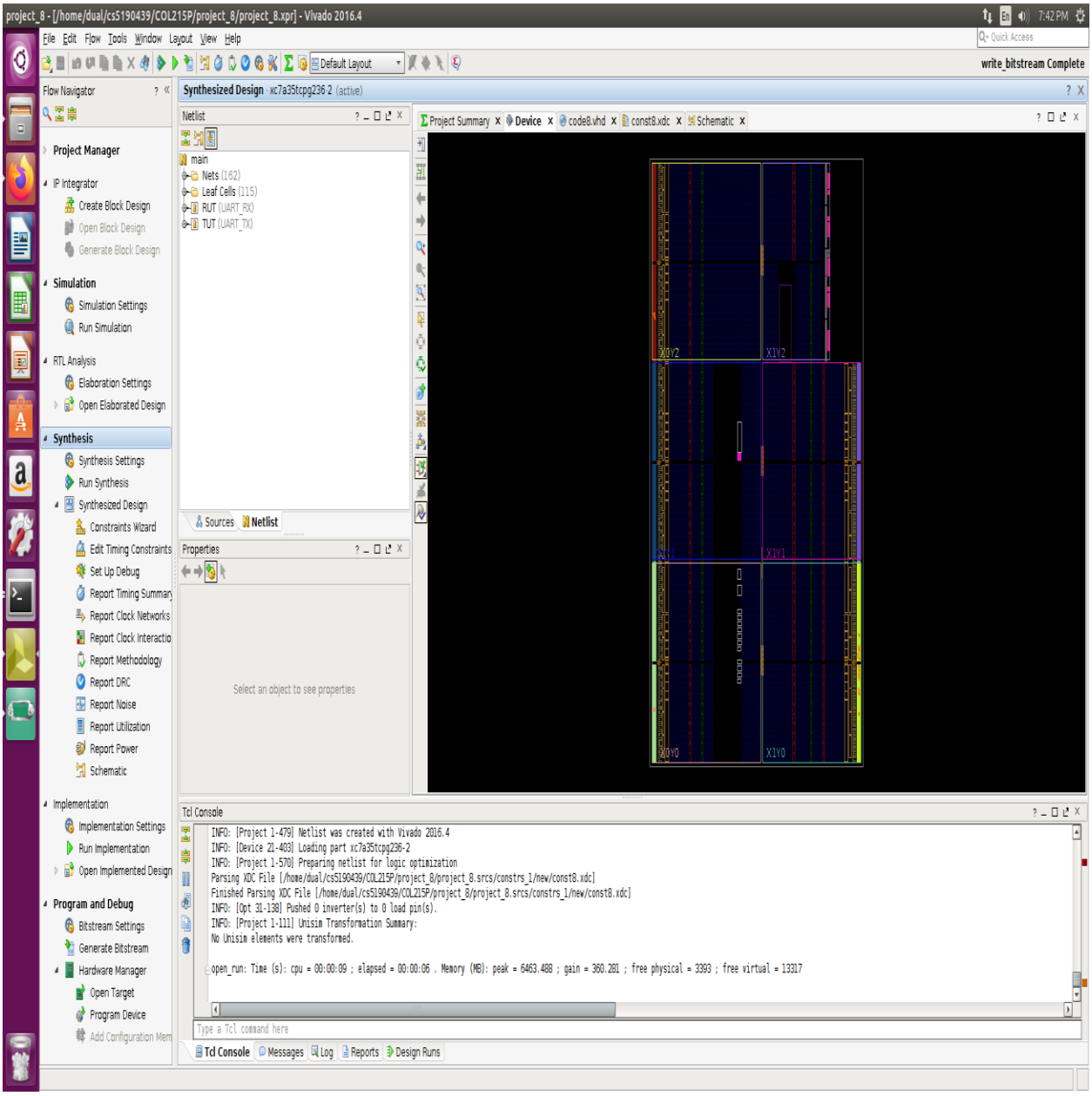


Here we tested with the help of gtk by echoing the receiver serial input .

On reset button,screen of fpga will be seen as with change to State idle-

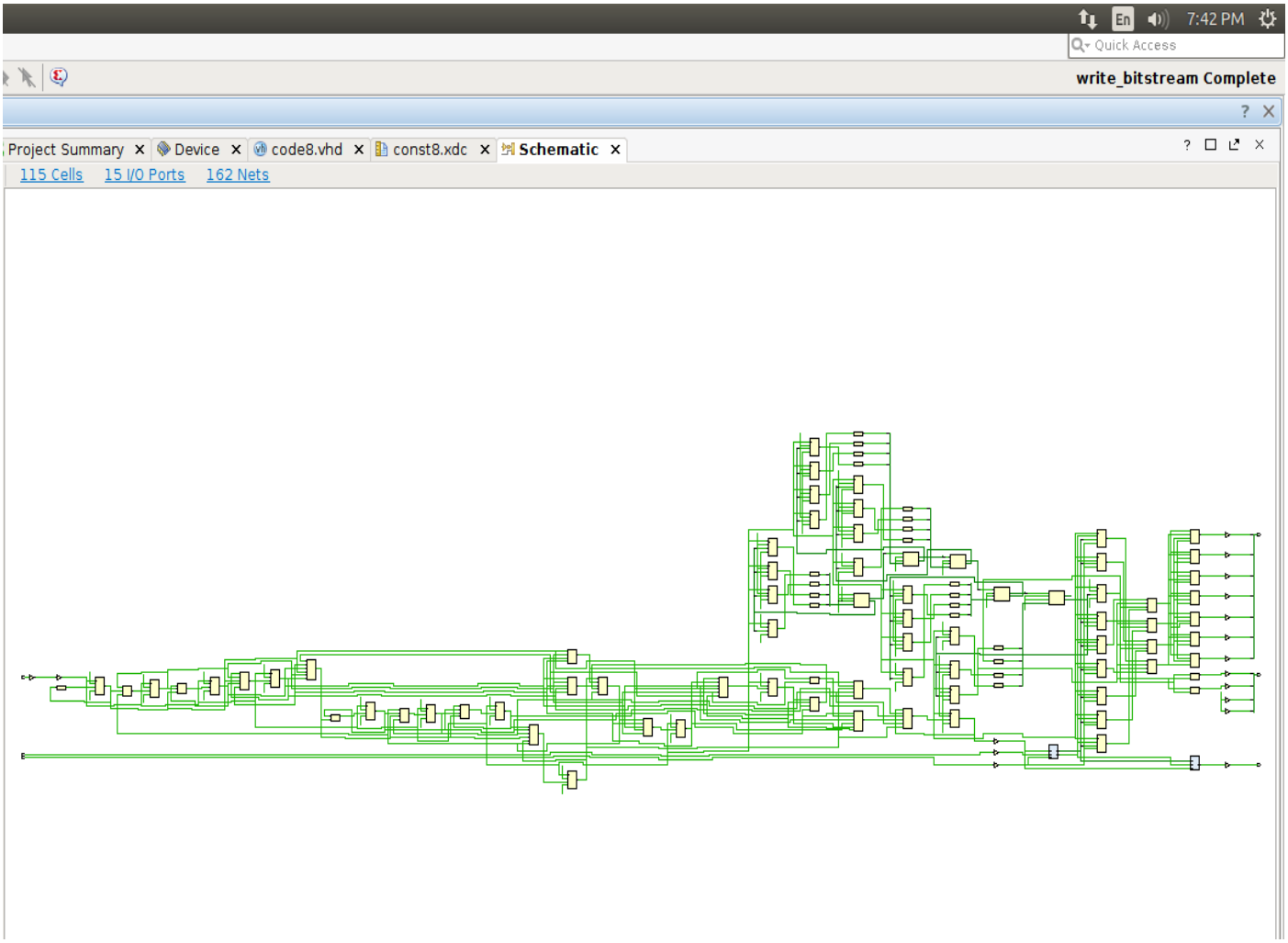


Device view-


project_8 - [/home/dual/cs5190439/COL215P/project_8/project_8.xpr] - Vivado 2016.4
File Edit Flow Tools Window Layout View Help
Default Layout
write_bitstream Complete
Flow Navigator
Project Manager
IP Integrator
Create Block Design
Open Block Design
Generate Block Design
Simulation
Simulation Settings
Run Simulation
RTL Analysis
Elaboration Settings
Open Elaborated Design
Synthesis
Synthesis Settings
Run Synthesis
Synthesized Design
Constraints Wizard
Edit Timing Constraints
Set Up Debug
Report Timing Summary
Report Clock Networks
Report Clock Interactio
Report Methodology
Report DRC
Report Noise
Report Utilization
Report Power
Schematic
Implementation
Implementation Settings
Run Implementation
Open Implemented Design
Program and Debug
Bitstream Settings
Generate Bitstream
Hardware Manager
Open Target
Program Device
Add Configuration Mem
Synthesized Design - xc7a35tcpg236-2 (active)
Netlist
main
Nets (162)
Leaf Cells (115)
RUT (UART_RX)
TUT (UART_TX)
Sources
Netlist
Properties
Select an object to see properties
Project Summary
Device
code8.vhd
const8.xdc
Schematic
X0Y2
X1Y2
X0Y1
X1Y1
X0Y0
X1Y0
Tcl Console
INFO: [Project 1-479] Netlist was created with Vivado 2016.4
INFO: [Device 21-403] Loading part xc7a35tcpg236-2
INFO: [Project 1-570] Preparing netlist for logic optimization
Parsing XDC File [/home/dual/cs5190439/COL215P/project_8/project_8.srcs/constrs_1/new/const8.xdc]
Finished Parsing XDC File [/home/dual/cs5190439/COL215P/project_8/project_8.srcs/constrs_1/new/const8.xdc]
INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
INFO: [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.
open_run: Time (s): cpu = 00:00:09 ; elapsed = 00:00:06 . Memory (MB): peak = 6463.488 ; gain = 360.281 ; free physical = 3393 ; free virtual = 13317
Type a Tcl command here
Tcl Console
Messages
Log
Reports
Design Runs

SCHEMETIC VIEW-

Here is the circuit



Thank you!