

ASSIGNMENT-7

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In this assignment we have learned to receive serial information without a shared clock.

Submission folder (2019CS50439_2019CS50434) contains -

const7.xdc - constraint file

code_7.vhd -vhdl code file

main.bit - bitstream file

A7_report.pdf- report file

New project7 on Vivado-

project_7 - [J:/home/dual/cs5190439/COL215P/project_7/project_7.xpf] - Vivado 2016.4

File Edit Flow Tools Window Layout View Help

Default Layout

Synthesis and Implementation Out-of-date [more info](#)

Flow Navigator

- Project Manager
 - Project Settings
 - Add Sources
 - Language Templates
 - IP Catalog
- IP Integrator
 - Create Block Design
 - Open Block Design
 - Generate Block Design
- Simulation
 - Simulation Settings
 - Run Simulation
- RTL Analysis
 - Elaboration Settings
 - Open Elaborated Design
- Synthesis
 - Synthesis Settings
 - Run Synthesis
 - Open Synthesized Design
- Implementation
 - Implementation Settings
 - Run Implementation
 - Open Implemented Design
- Program and Debug
 - Bitstream Settings
 - Generate Bitstream
 - Open Hardware Manager

Project Manager project_7

Sources

Waiting to Update Source File Hierarchy...

Constraints (1)

Project Summary

Project Settings

Project name: project_7

Project location: J:/home/dual/cs5190439/COL215P/project_7

Product family: Artix-7

Project part: xc7a35tqpg236-2

Top module name: main

Target language: VHDL

Simulator language: Mixed

Synthesis

Status: Out-of-date

Messages: 3 warnings

Part: xc7a35tqpg236-2

Strategy: Vivado Synthesis Defaults

Implementation

Status: Complete

Messages: 3 warnings

Part: xc7a35tqpg236-2

Strategy: Vivado Implementation Defaults

Incremental compile: None

Summary Route Status

DRC Violations

Summary: 1 warning

[Implemented DRC Report](#)

Timing

Worst Negative Slack (WNS): NA

Total Negative Slack (TNS): NA

Number of Failing Endpoints: NA

Total Number of Endpoints: NA

[Implemented Timing Report](#)

Setup Hold Pulse Width

Utilization - Post-Implementation

LUT	1%
FF	1%
IO	13%
BUFG	3%

Power

Total On-Chip Power: 7.566 W

Junction Temperature: 62.8 °C

Thermal Margin: 22.2 °C (4.4 W)

Effective θJA: 5.0 °C/W

Power supplied to off-chip devices: 0 W

Design Runs

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAM	URAM	PCle %	Start	Elapsed
synth_1	constrs_1	Synthesis Out-of-date													5/19/22 5:31 PM	00:00:29 Vivado Synthe
impl_1	constrs_1	write_bitstream Complete													5/19/22 5:32 PM	00:00:43 Vivado Implem

Tcl Console Messages Log Reports Design Runs

Initializing project...

VHDL code on Vivado -

The screenshot displays the Vivado IDE interface for a project named 'project_7'. The left sidebar contains a 'Project Manager' pane with a tree view showing 'main - testbench (code6.vhd)' and 'RUT - UART_RX - rtl (code6.vhd)'. Below this is a 'Hierarchy' pane showing the 'code6.vhd' file. The main editor window displays the VHDL code for 'code6.vhd', which includes a testbench and a UART module. The code is as follows:

```
1 --Displaying by 4 seven segment-A3
2
3 library IEEE;
4 use IEEE.std_logic_1164.all;
5 use IEEE.NUMERIC_STD.ALL;
6 use IEEE.STD_LOGIC_UNSIGNED.ALL;
7
8 --stands for connecting signals of main entity
9
10 entity main is
11 port(
12     m1_RX_Serial : in std_logic;
13     clock,reset : in std_logic; --clock 100Mhz
14     anodes: out std_logic_vector(3 downto 0);
15     sevens: out std_logic_vector(6 downto 0)
16 );
17 end main;
18
19 -- architecture
20 architecture testbench of main is
21 --receiver component
22 component UART_RX is
23
24 port (
25     clock,reset : in std_logic;
26     i_RX_Serial : in std_logic;
27     o_RX_DV : out std_logic;
28     o_RX_Byte : out std_logic_vector(7 downto 0)
29 );
30 end component;
31
32 signal fours : std_logic_vector(3 downto 0);-- "0000"
33 signal rcouter: std_logic_vector(19 downto 0):= (others => '0');-- refresh counter
34 --for creating refresh period of 10.5ms
35 signal selector : std_logic_vector(1 downto 0);
36 signal no_RX_DV : std_logic;
37 signal inputs: std_logic_vector(15 downto 0):= (others => '0');
38 signal no_RX_Byte : std_logic_vector(7 downto 0); --no_RX_Byte
39 begin
40
41 --receiver component initialization
42 RUT : UART_RX MAP (clock,reset,m1_RX_Serial,no_RX_DV,no_RX_Byte );
```

The bottom of the window shows a 'Design Runs' table with the following data:

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAM	URAM	PCle %	Start	Elapsed
synth_1	constrs_1	Synthesis Out-of-date	NA	NA	NA	NA	NA	7.566	0	76	60	0	0	0.000	5/19/22 5:31 PM	00:00:29 Vivado Synthe
impl_1	constrs_1	write_bitstream Complete	NA	NA	NA	NA	NA			0	57	60	0	0.000	5/19/22 5:32 PM	00:00:43 Vivado Implem

The code is also provided in the submission file

DESCRIPTION

Here we assumed normal indexing of segments of seven segment display(B-2,etc)

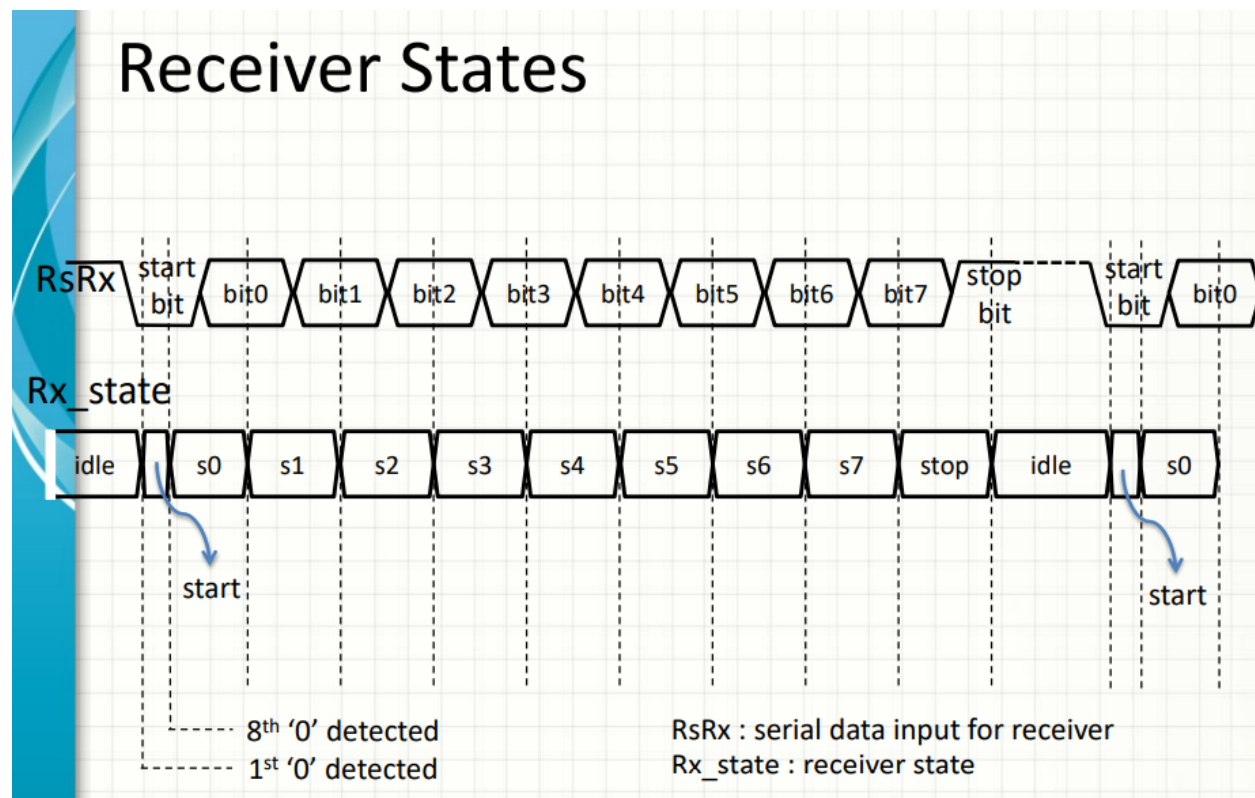
Design decision

Designed asynchronous serial receiver with baud rate = 9600, 8 data bits, no parity bits and 1 stop bit.

Made a provision for resetting the FSM to idle state by a push button(display "00"),

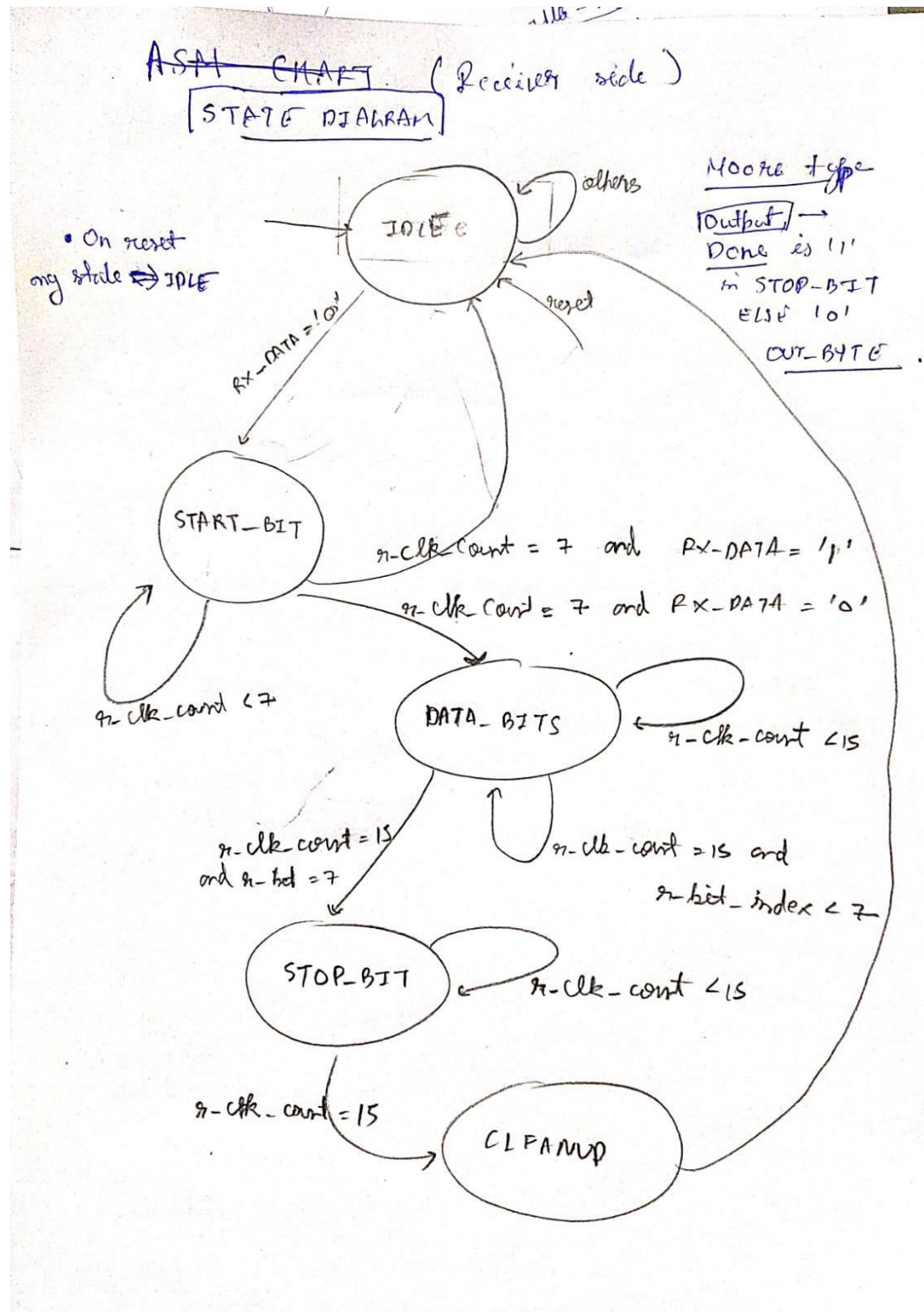
Receiver component have serial input and parallel byte output,which we are storing to display on seven segment display.

For others Simply followed states idea learned from lectures(below image)-



Here in state diagram ,we can find how these total 5 states related (IDLE,START_BIT,DATA_BITS,STOP_BIT,CLEANUP)-

STATE DIAGRAM



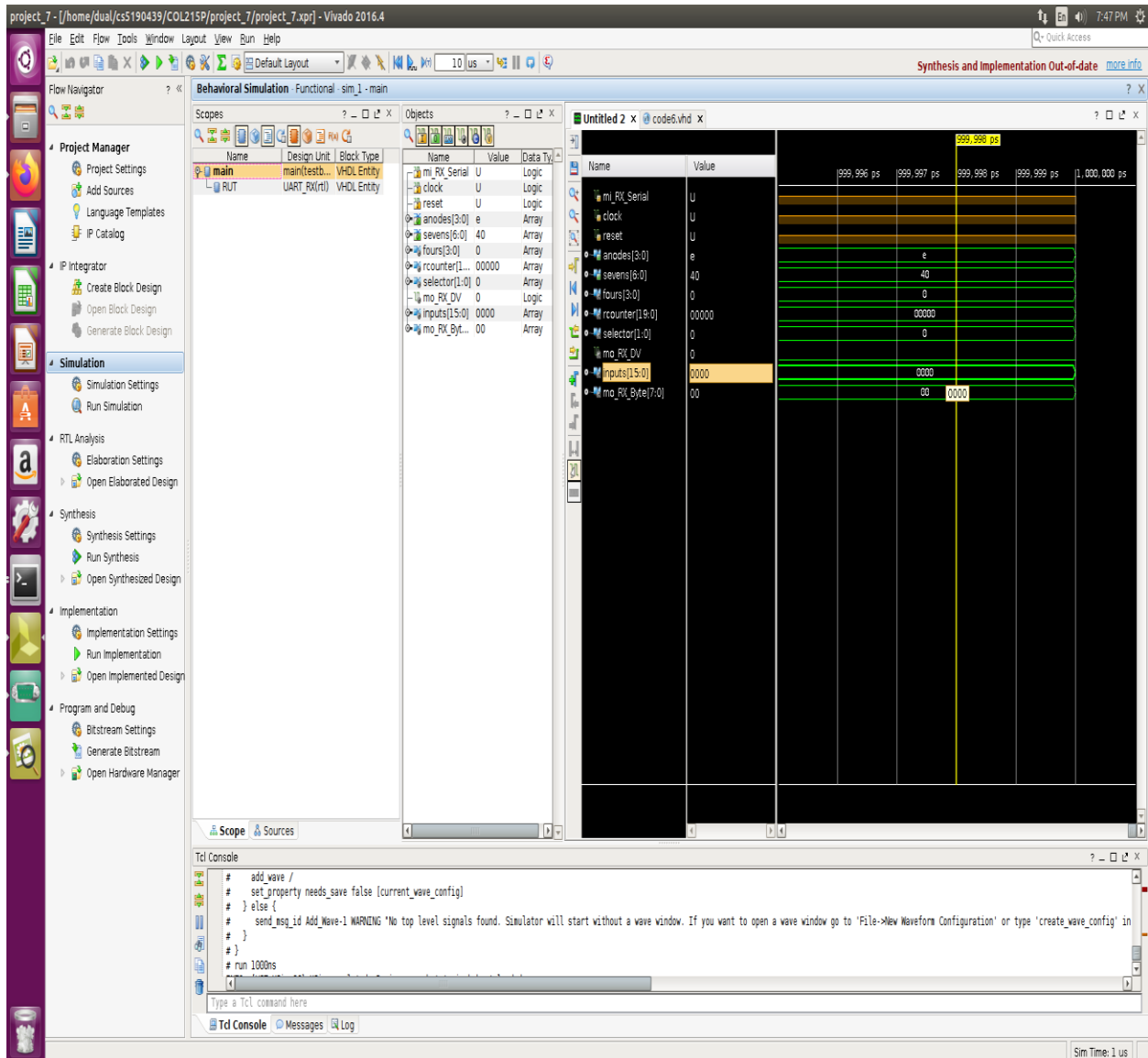
Constraint file

Matched receiver serial input port only in addition to previous A3 ports of displaying 7 segment display

```
53 #set_property PACKAGE_PIN H17 [get_ports {vgaGreen[1]}]
54     #set_property IOSTANDARD LVCMOS33 [get_ports {vgaGreen[1]}]
55 #set_property PACKAGE_PIN G17 [get_ports {vgaGreen[2]}]
56     #set_property IOSTANDARD LVCMOS33 [get_ports {vgaGreen[2]}]
57 #set_property PACKAGE_PIN D17 [get_ports {vgaGreen[3]}]
58     #set_property IOSTANDARD LVCMOS33 [get_ports {vgaGreen[3]}]
59 #set_property PACKAGE_PIN P19 [get_ports Hsync]
60     #set_property IOSTANDARD LVCMOS33 [get_ports Hsync]
61 #set_property PACKAGE_PIN R19 [get_ports Vsync]
62     #set_property IOSTANDARD LVCMOS33 [get_ports Vsync]
63
64
65 ##USB-RS232 Interface
66 set_property PACKAGE_PIN B18 [get_ports mi_RX_Serial]
67     set_property IOSTANDARD LVCMOS33 [get_ports mi_RX_Serial]
```

Simulation on vivado

For simulation tried to use faster clock 10ps type and reduced counter maximum values.



More about simulation is shown in Assignment 8 with receiver and transmitter both side and their connection there .

But also not able to simulate well as Vivado crashes unfortunately.

After doing above steps or till simulation work, then for implementing design on basys board, we first synthesized design, ran the implementation, then generated Bitstream and finally opened the hardware manager to program device.

Resources utilization-

The screenshot displays the Vivado 2016.4 IDE with the following components:

- Project Manager (Left):** Shows the project hierarchy with folders for Project Settings, Simulation, RTL Analysis, Synthesis, and Implementation.
- Netlist View (Center):** Displays the synthesized design for 'xc7a35tpg236-2'. It includes a table of resources used:

Ref Name	Used	Functional Category
134	BSCAN2	0
135	CAPTURE2	0
136	DMA_PORT	0
137	EFUSE_USR	0
138	FRAME_ECCE2	0
139	ICAPE2	0
140	PCIE_2_1	0
141	STARTUP2	0
142	XADC	0
143	-----	
144		
145		
146	Primitives	
147	-----	
148		
149	-----	
150	Ref Name	Used
151	-----	
152	FBCE	57
153	LUT6	23
154	LUT1	21
155	LUT4	19
156	LUT5	16
157	IOBUF	11
158	LUT2	6
159	CARRY4	5
160	LUT3	3
161	IOBUF	3
162	FBCE	3
163	IOBUF	1
164	-----	
165		
166	Black Boxes	
167	-----	
168		
169		
170	-----	
171	Ref Name	Used
172	-----	
173		
174		

- Primitive Statistics (Bottom Left):**

Primitive type	Count
FLOP_LATCH	60
LUT	88
CARRY	5
IO	14
CLK	1
OTHERS	4
- Reports Panel (Bottom):**

Name	Modified	Size	GUI Report
Synthesis			

synth_1			

Vivado Synthesis Report			

Utilization Report			

Implementation			

Design Initialization (init_design)			

Timing Summary Report			

Opt Design (opt_design)			

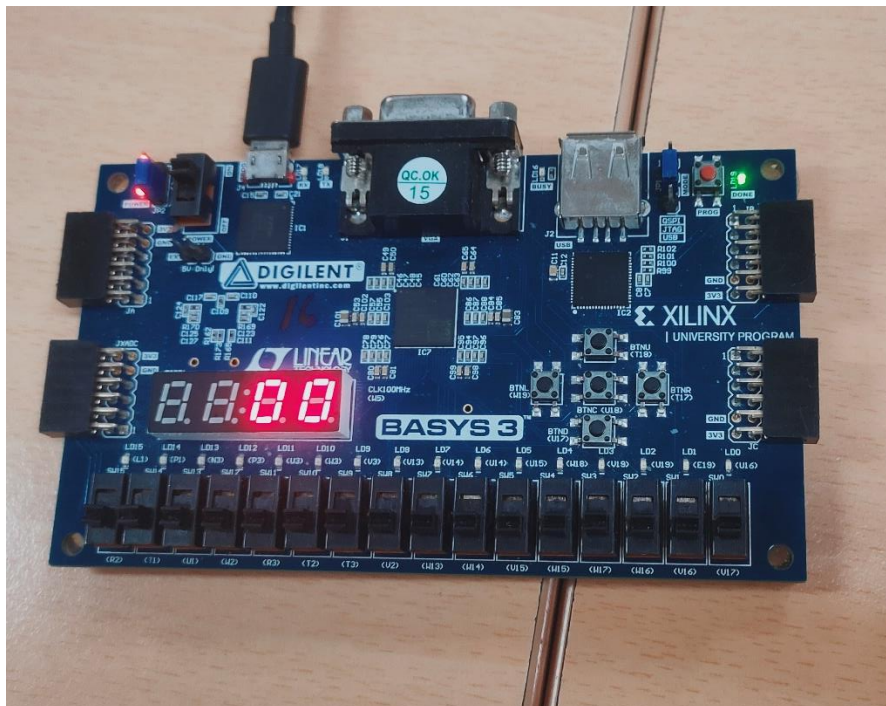
Post opt_design DRC ...			

Post opt_design Meth...			

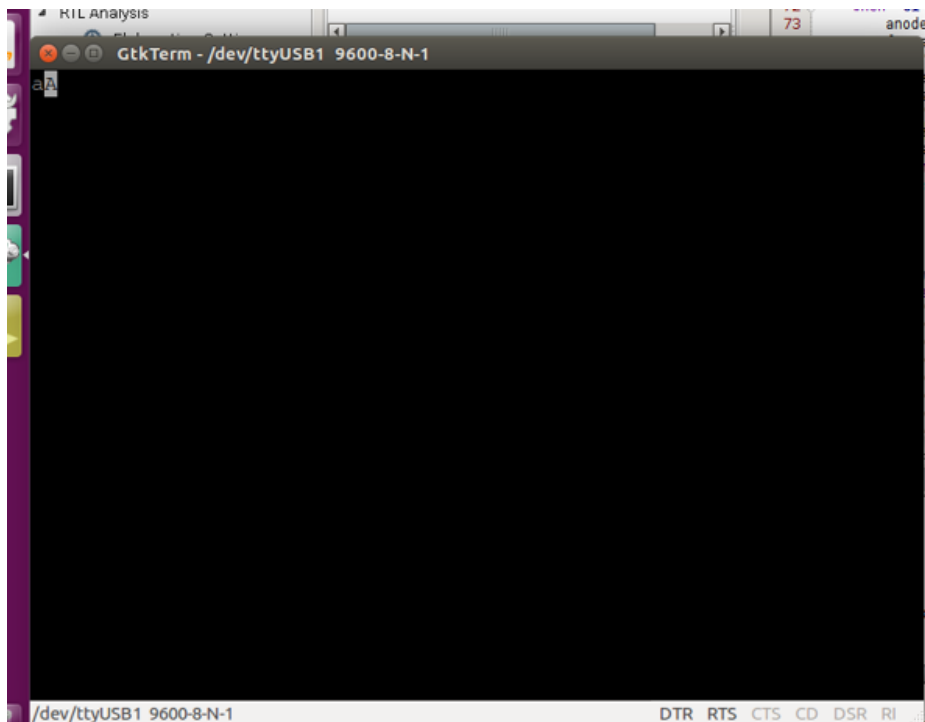
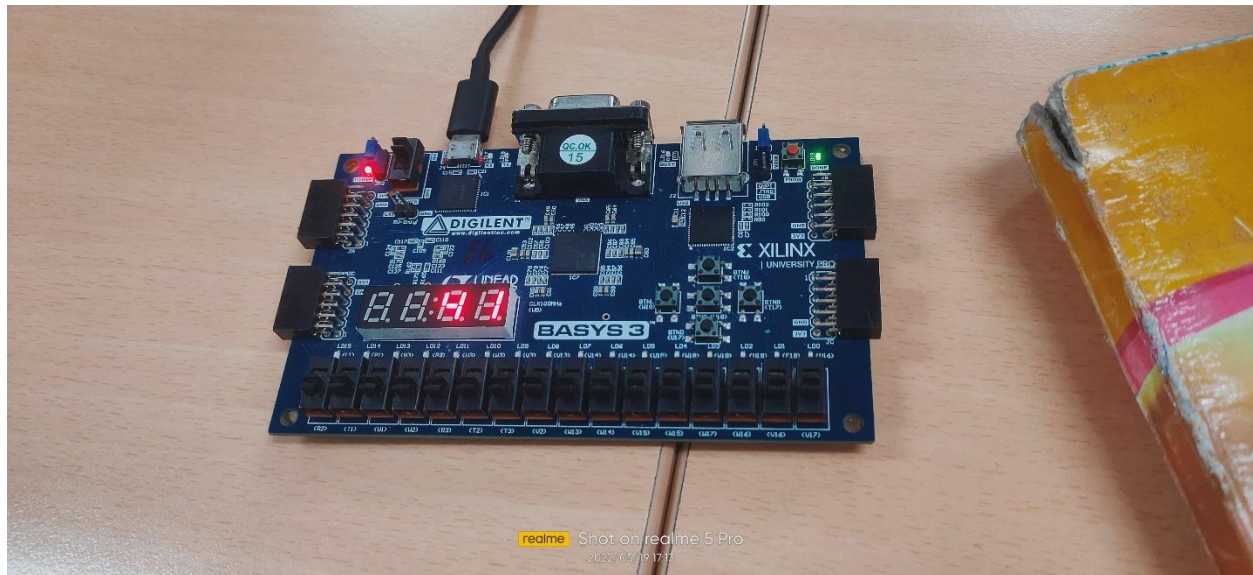
Timing Summary Report			

Power Opt Design (power_opt_design)			

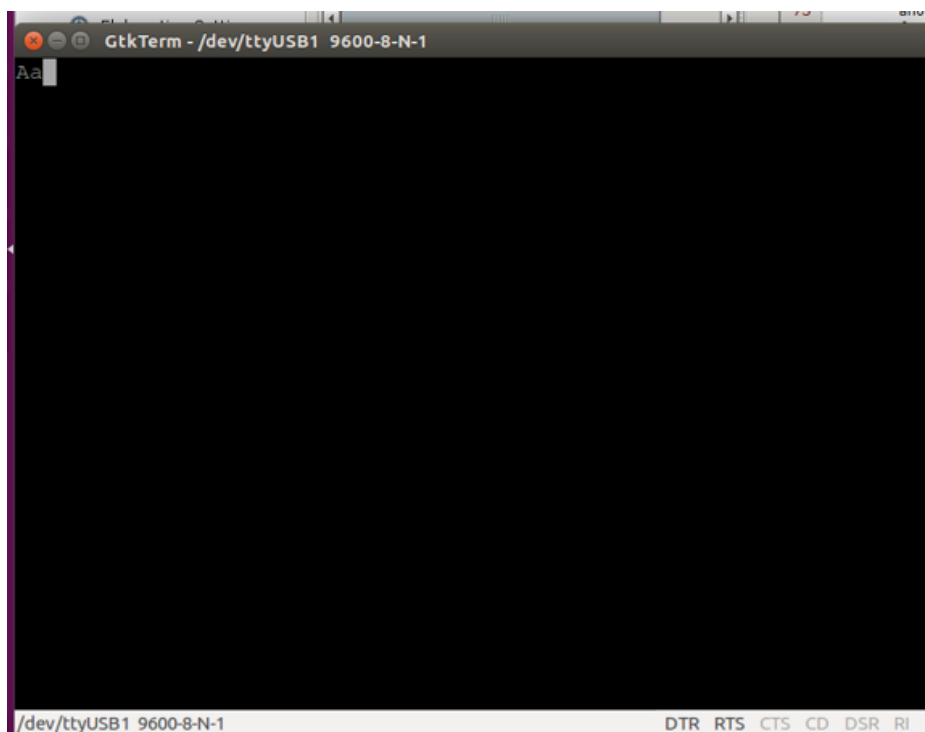
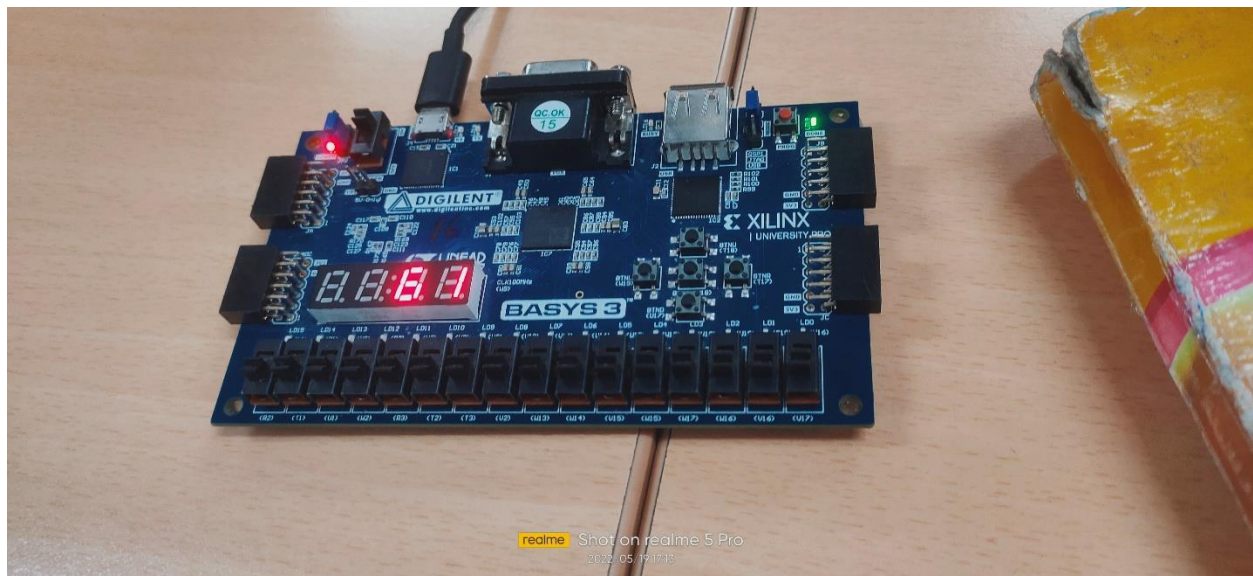
Testing on Basys3 board and gtk-
initial state-



When A,ASCII Char pressed on keyboard,then display showing hexadecimal representation-

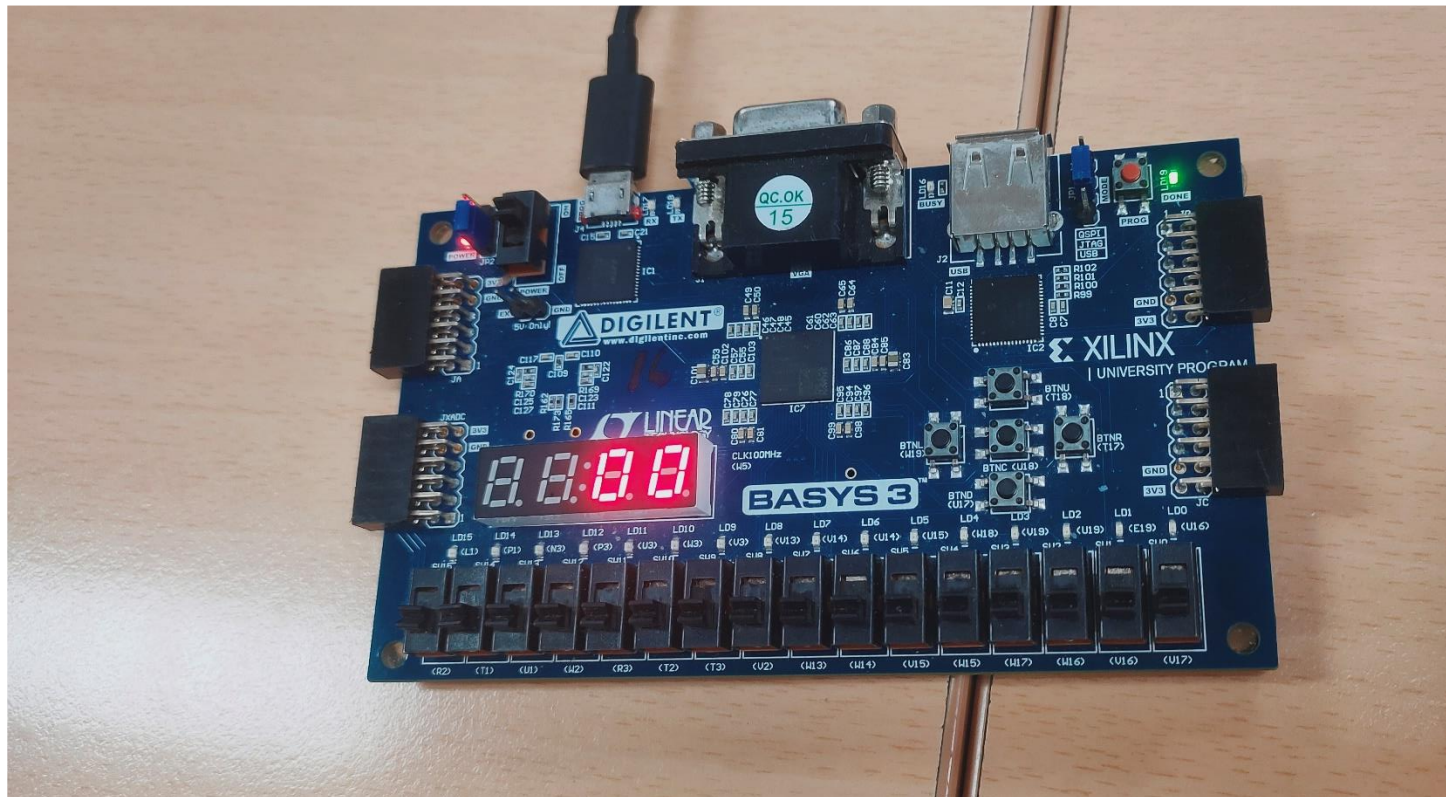


When a,ASCII Char pressed on keyboard,then display showing hexadecimal representation-

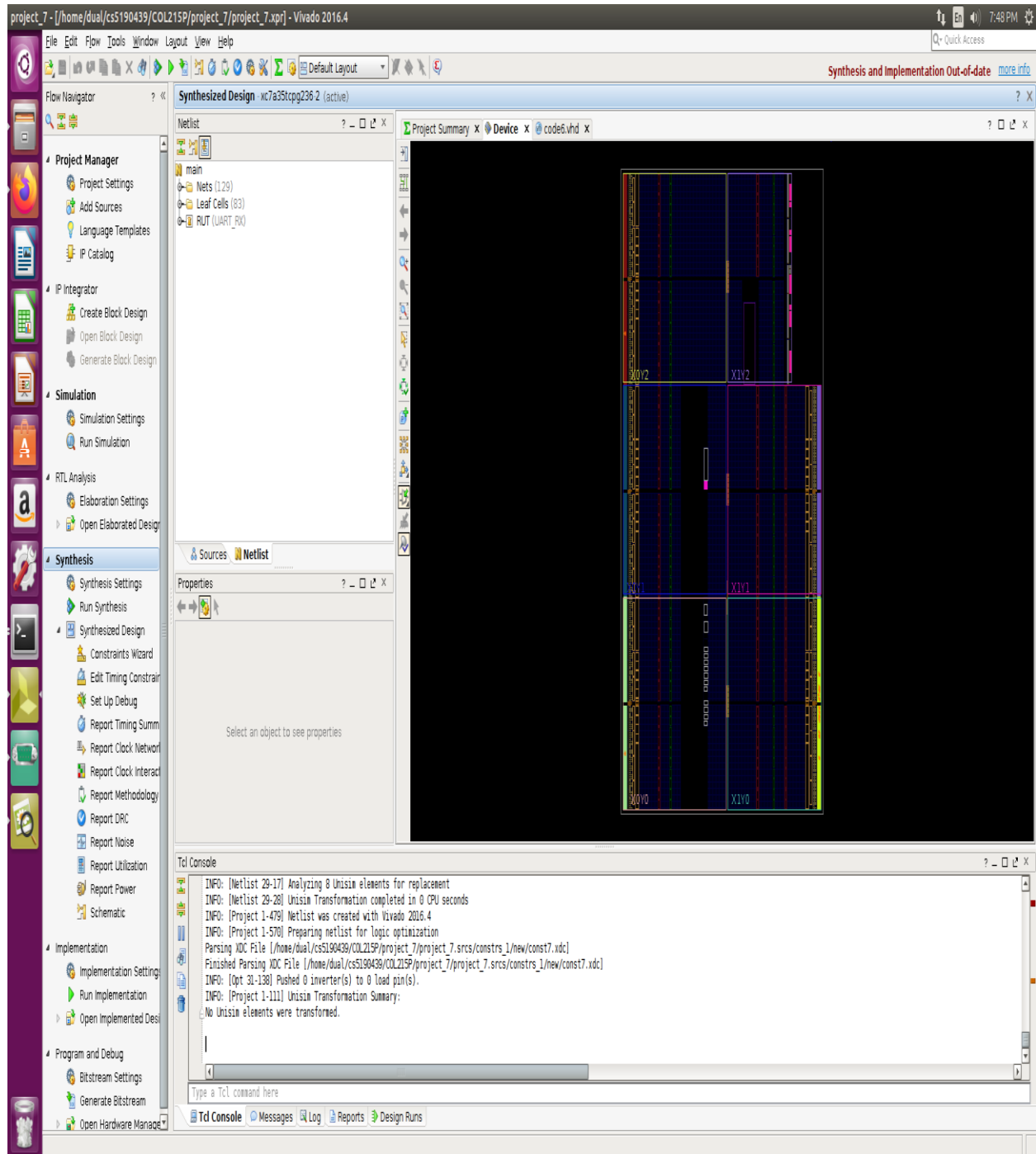


Here we tested with the help of gtk by echoing the receiver serial input .

On reset button,screen of fpga will be seen as with change to State idle-

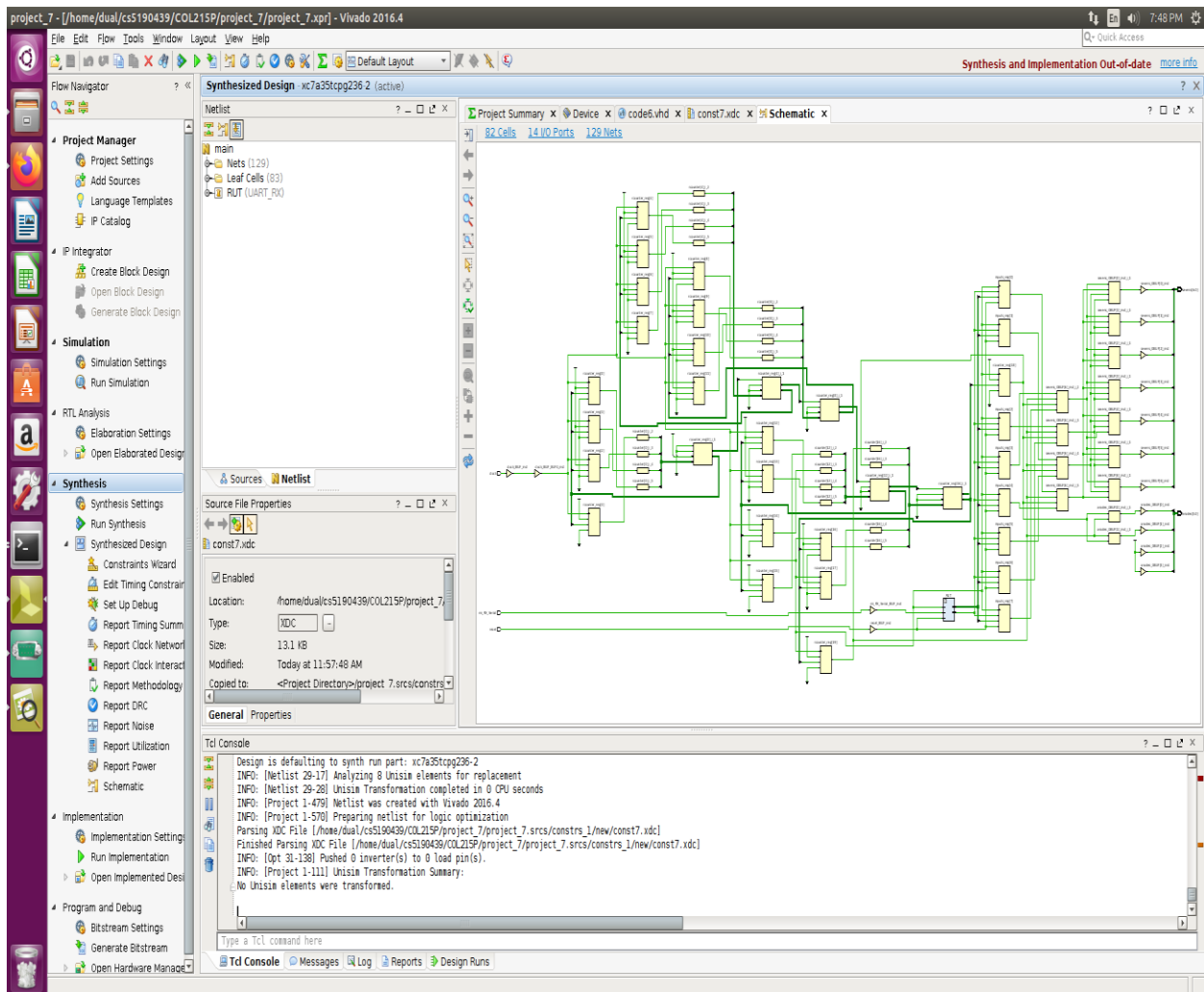


Device view-



SCHEMATIC VIEW-

Here is the circuit



Thank you!