ASSIGNMNET-7

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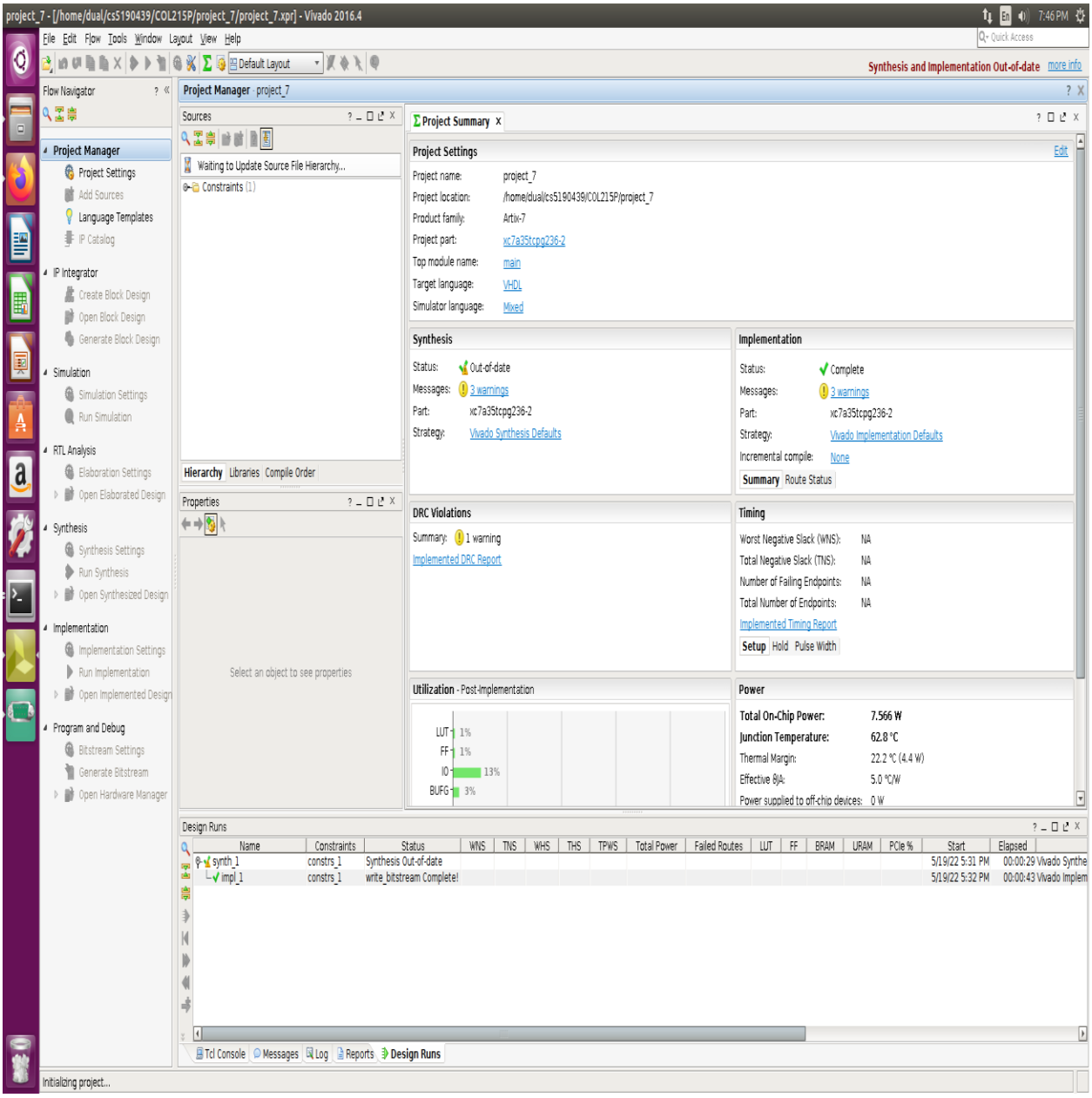
In this assignment we have learned to receive serial information without a shared clock.

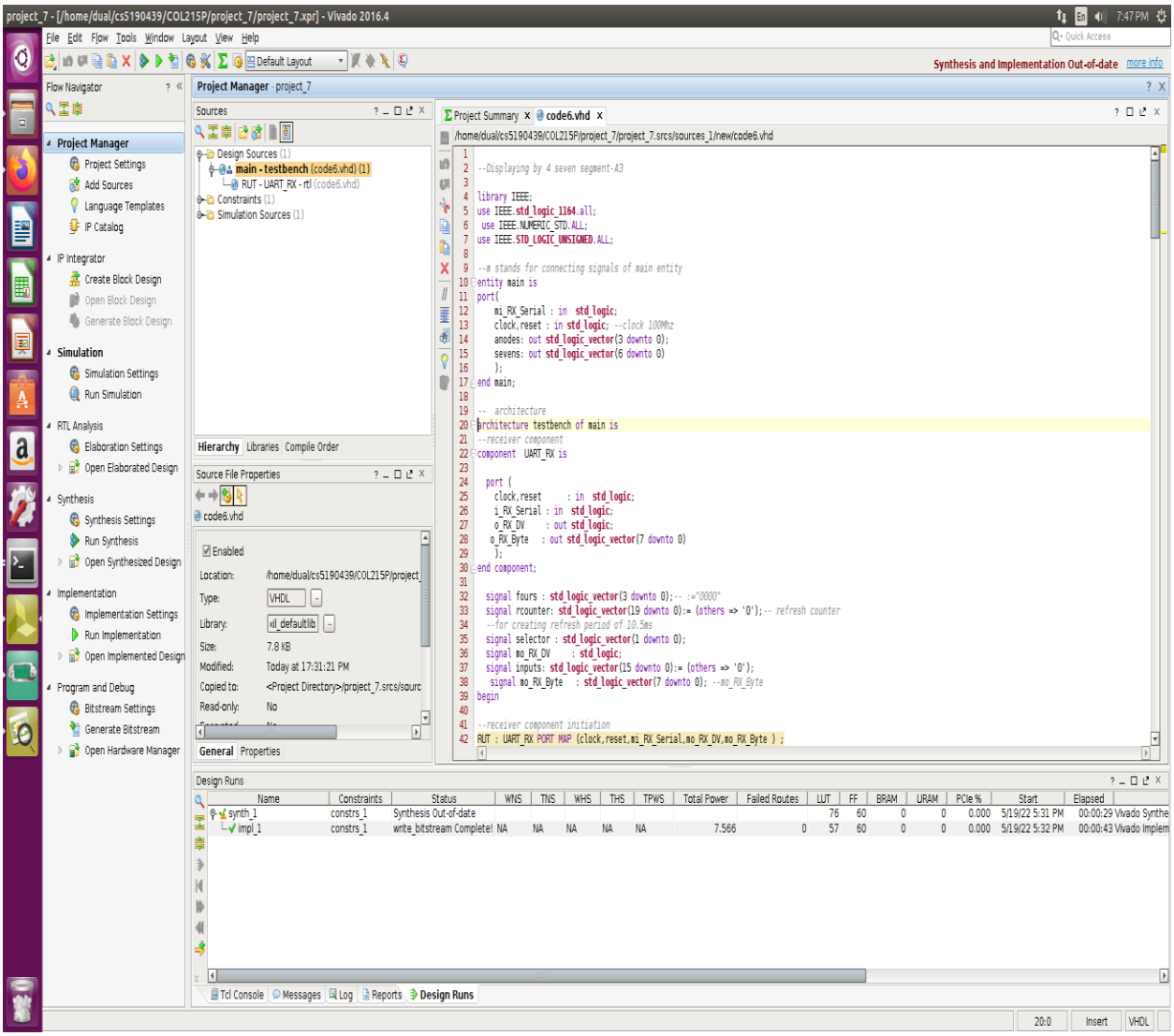
Submission folder (2019CS50439_2019CS50434) contains -

- **const7.xdc - constraint file**
- **code_7.vhd -vhdl code file**
- **main.bit - bitstream file**
- **A7_report.pdf- report file**

New project7 on Vivado-



VHDL code on Vivado -



The code is also provided in the submission file

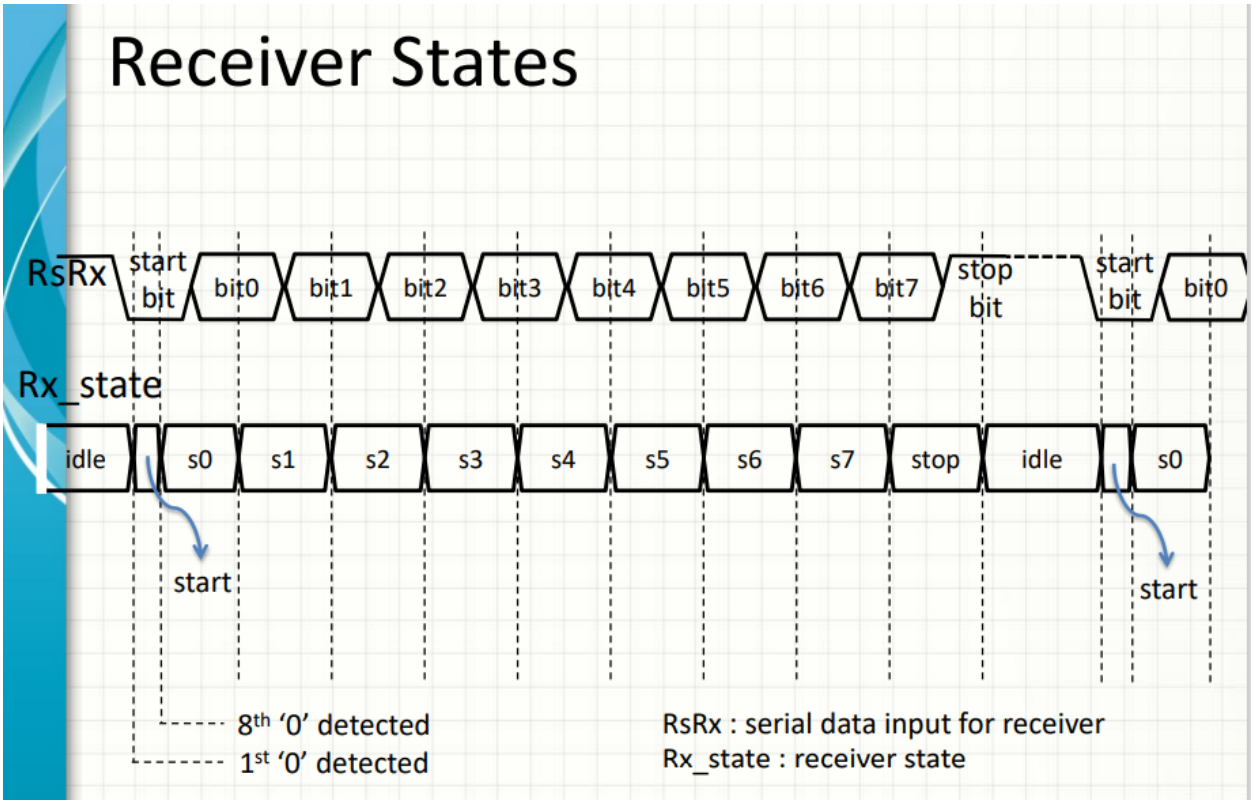
DESCRIPTION

Here we assumed normal indexing of segments of seven segment display(B-2,etc)

Design decision

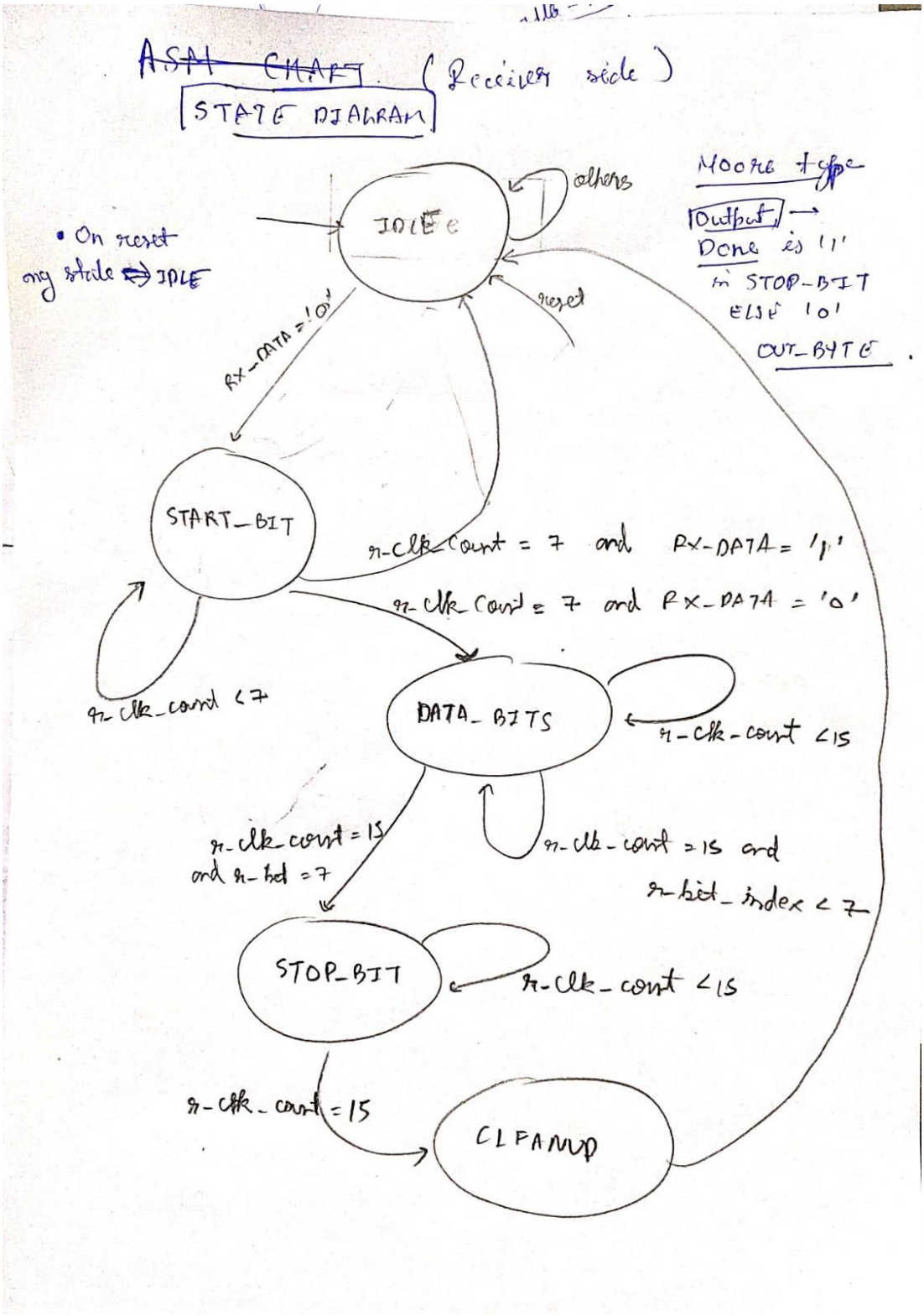
Designed asynchronous serial receiver with baud rate = 9600, 8 data bits, no parity bits and 1 stop bit.
Made a provision for resetting the FSM to idle state by a push button(display “00”),

Receiver component have serial input and parallel byte output,which we are storing to display on seven segment display.
For others Simply followed states idea learned from lectures(below image)-



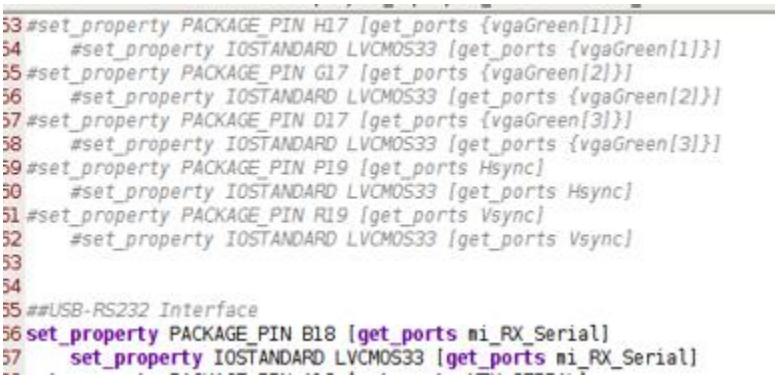
Here in state diagram ,we can find how these total 5 states related (IDLE,START_BIT,DATA_BITS,STOP_BIT,CLEANUP)-

STATE DIAGRAM



Constraint file

Matched receiver serial input port only in addition to previous A3 ports of displaying 7 segment display

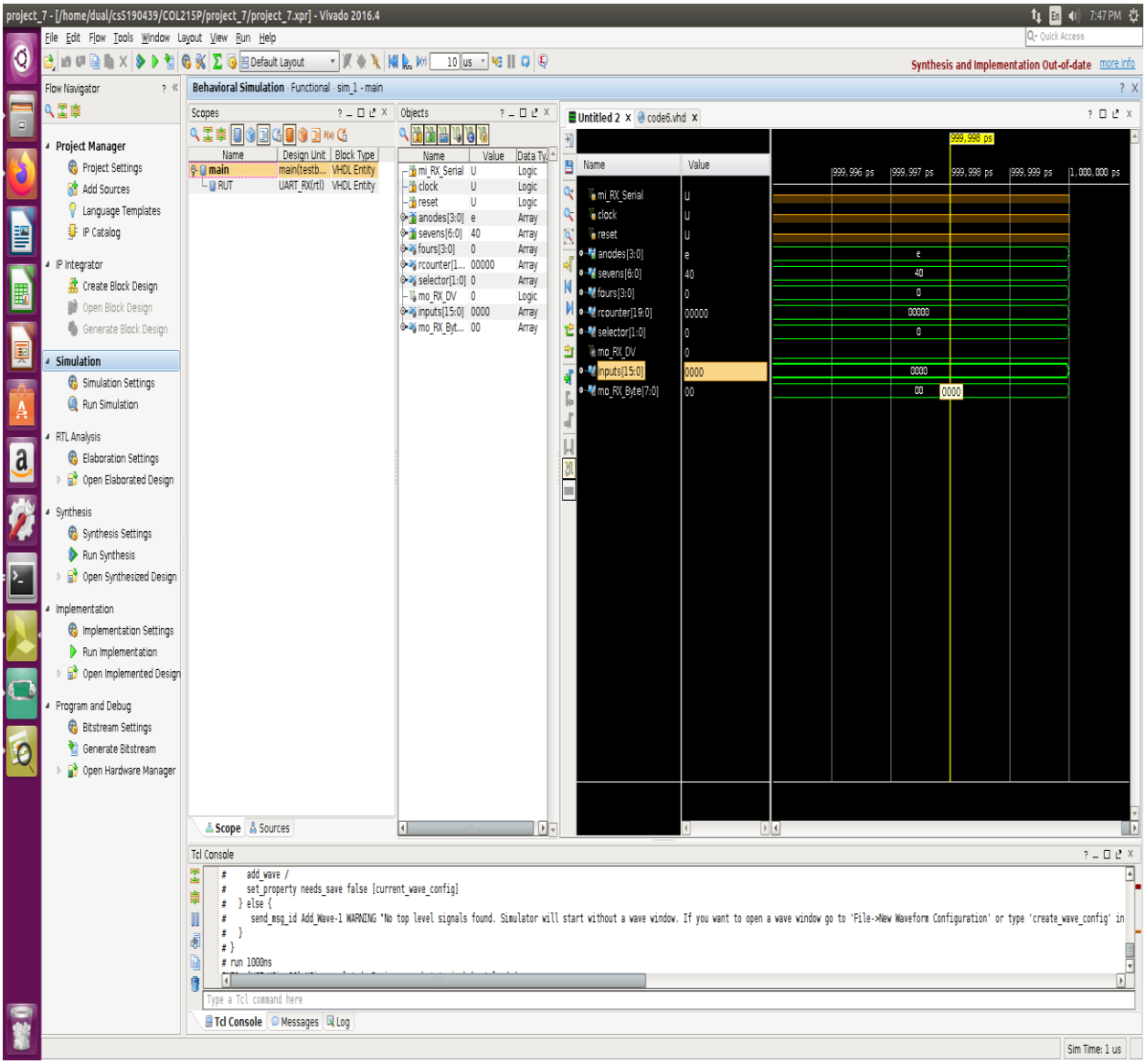


```
#set_property PACKAGE_PIN H17 [get_ports {vgaGreen[1]}]
    #set_property IOSTANDARD LVCMOS33 [get_ports {vgaGreen[1]}]
#set_property PACKAGE_PIN G17 [get_ports {vgaGreen[2]}]
    #set_property IOSTANDARD LVCMOS33 [get_ports {vgaGreen[2]}]
#set_property PACKAGE_PIN D17 [get_ports {vgaGreen[3]}]
    #set_property IOSTANDARD LVCMOS33 [get_ports {vgaGreen[3]}]
#set_property PACKAGE_PIN P19 [get_ports Hsync]
    #set_property IOSTANDARD LVCMOS33 [get_ports Hsync]
#set_property PACKAGE_PIN R19 [get_ports Vsync]
    #set_property IOSTANDARD LVCMOS33 [get_ports Vsync]


##USB-RS232 Interface
set_property PACKAGE_PIN B18 [get_ports mi_RX_Serial]
    set_property IOSTANDARD LVCMOS33 [get_ports mi_RX_Serial]
```

Simulation on vivado

For simulation tried to use fasterb clock 10ps type and reduced counter maximum values.

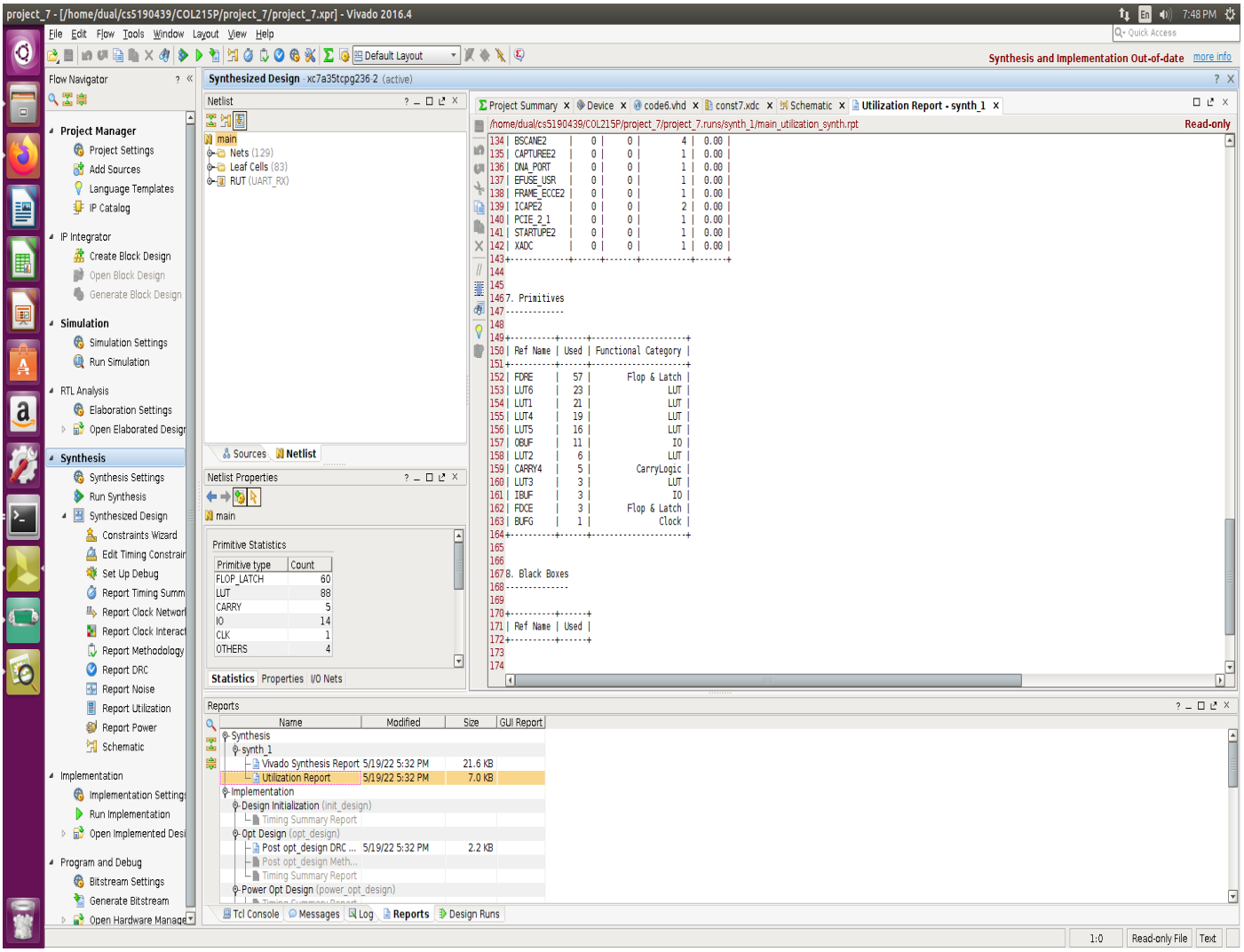


More about simulation is shown in Assignment 8 with receiver and transmitter both side and their connection there .

But also not able to simulate well as Vivado crashes unfortunately.

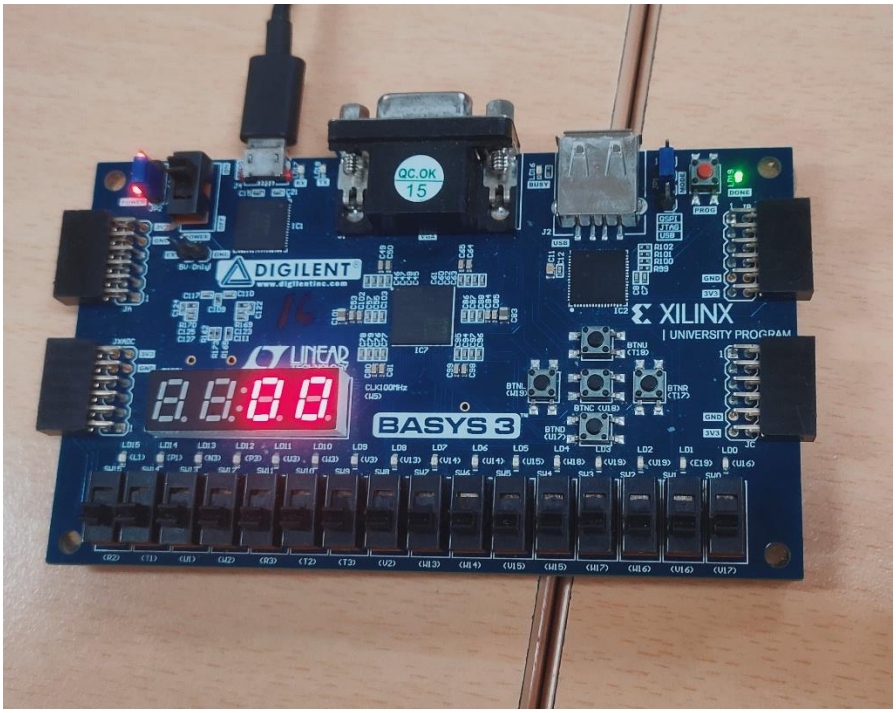
After doing above steps or till simulation work,then for implementing design on basys board, we first synthesized design, ran the implementation ,then generated Bitstream and finally opened the hardware manager to program device.

Resources utilization-

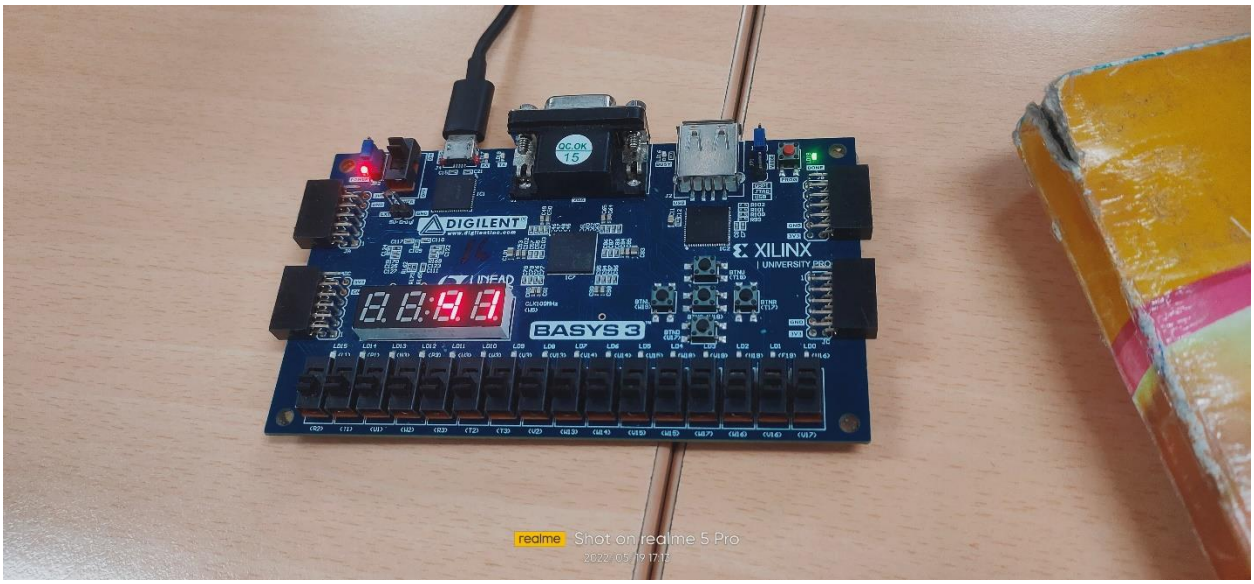


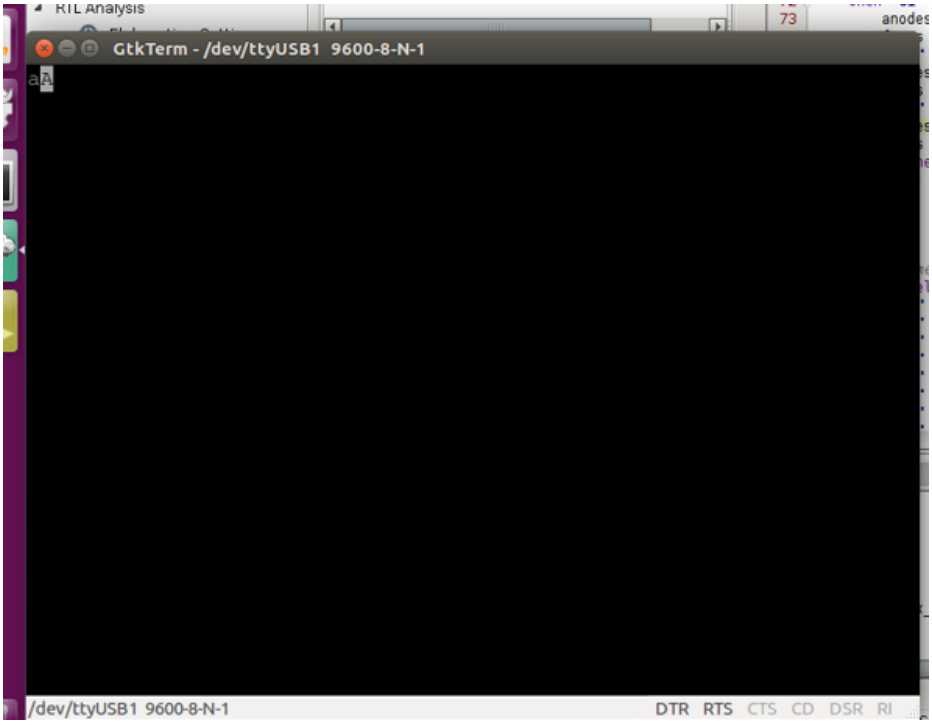
Testing on Basys3 board and gtk-

initial state-

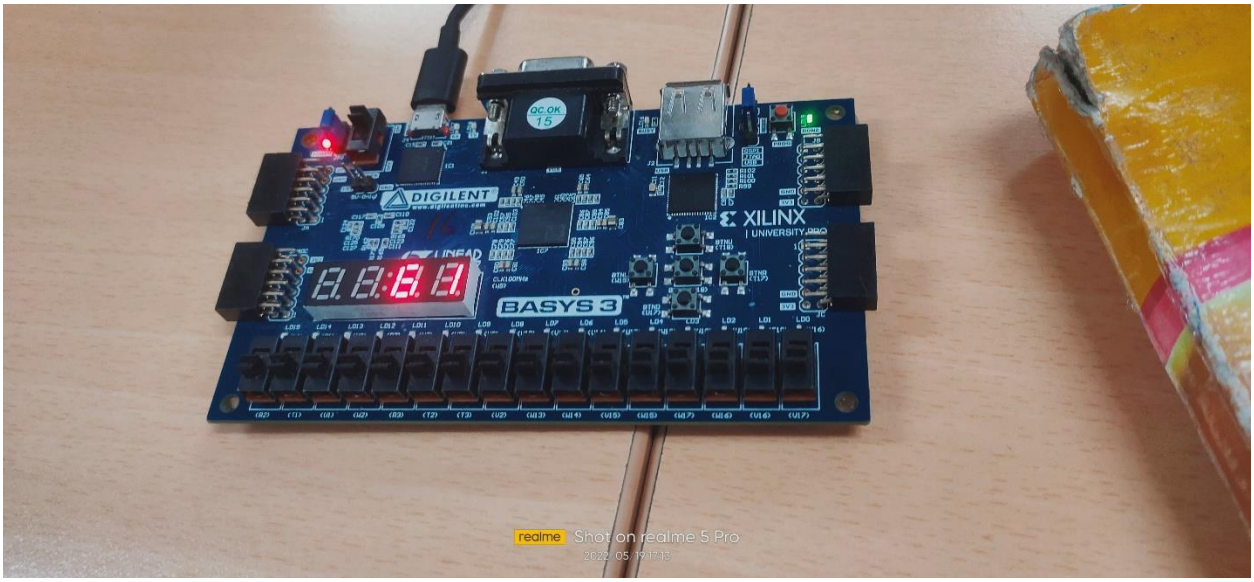


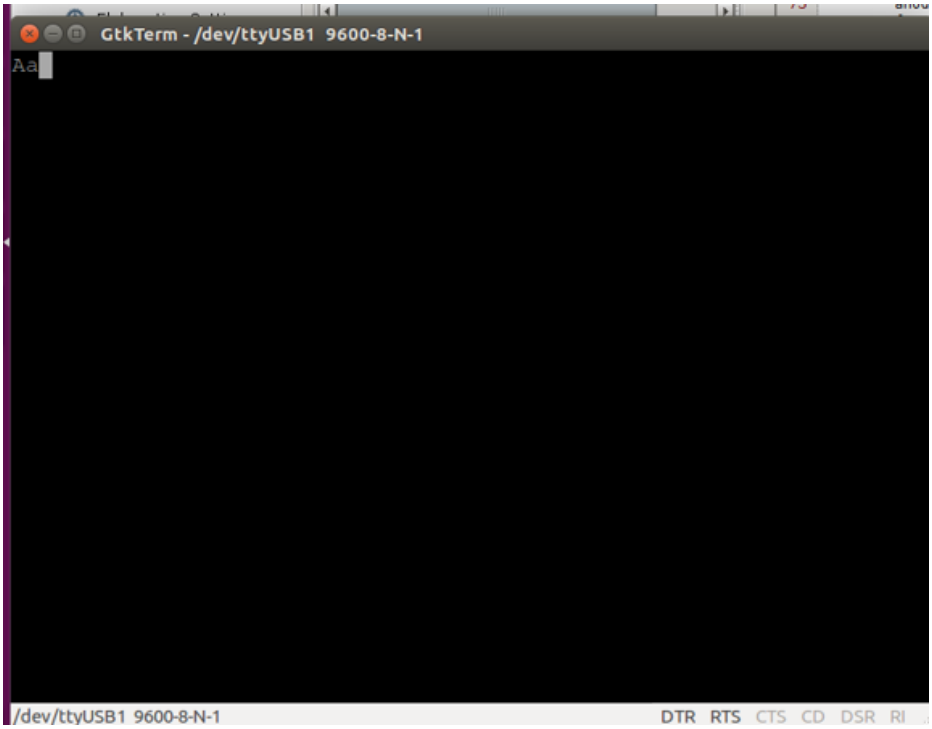
When A,ASCII Char pressed on keyboard,then display showing hexadecimal representation-





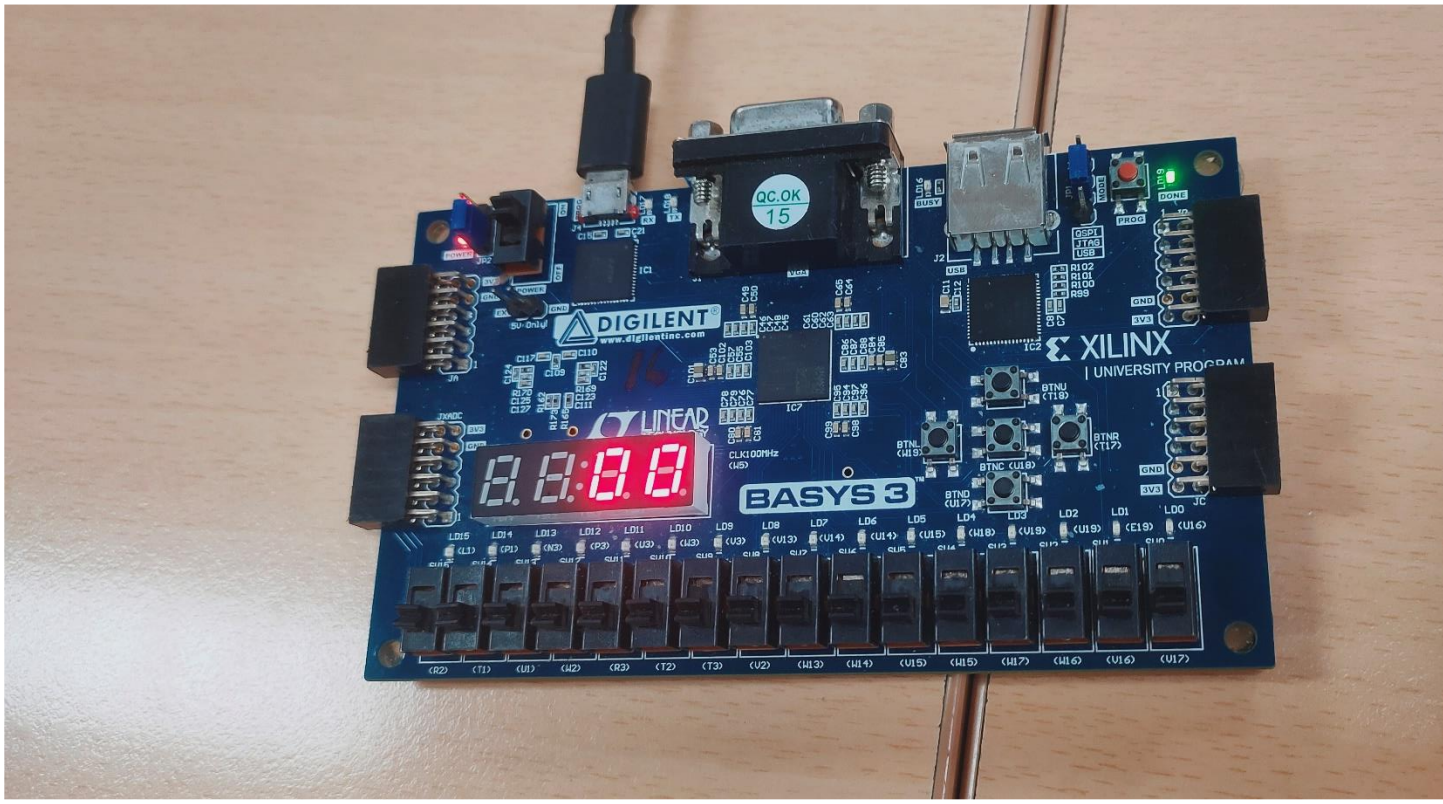
When a,ASCII Char pressed on keyboard,then display showing hexadecimal representation-



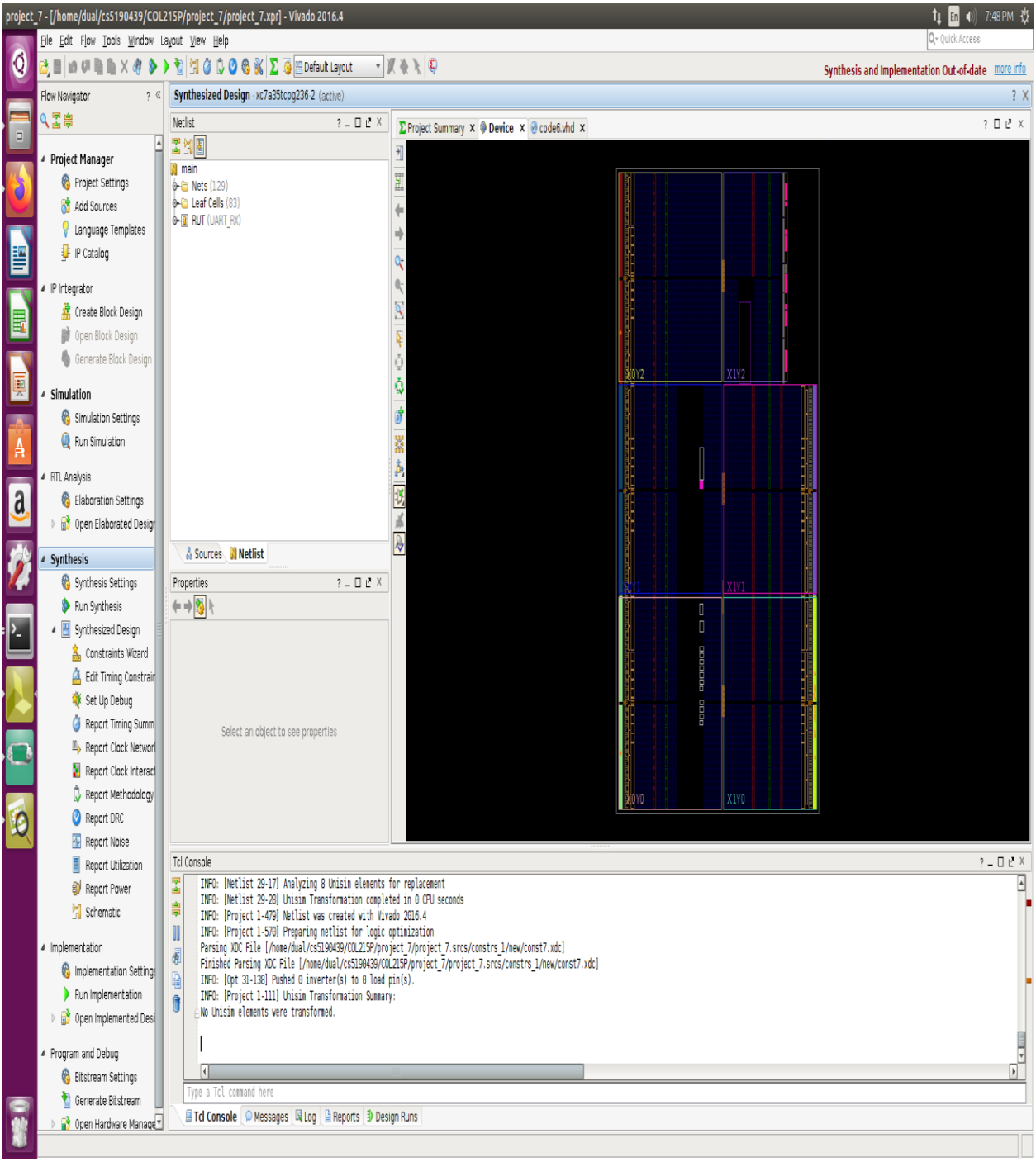


Here we tested with the help of gtk by echoing the receiver serial input .

On reset button,screen of fpga will be seen as with change to State idle-

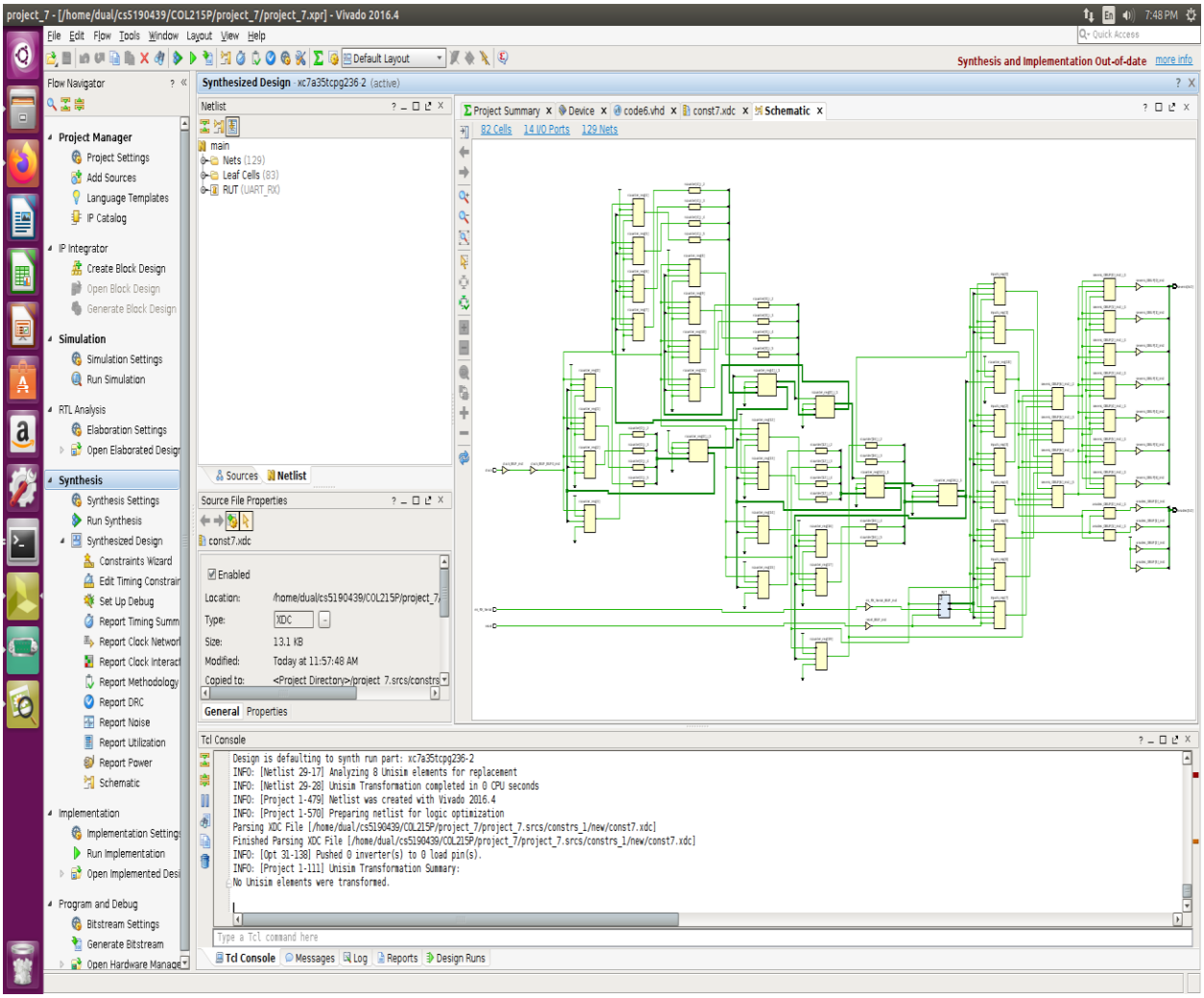


Device view-


project_7 - [/home/dual/cs5190439/COL215P/project_7/project_7.xpr] - Vivado 2016.4
File Edit Flow Tools Window Layout View Help
Default Layout
Synthesis and Implementation Out-of-date more info
Flow Navigator
Project Manager
Project Settings
Add Sources
Language Templates
IP Catalog
IP Integrator
Create Block Design
Open Block Design
Generate Block Design
Simulation
Simulation Settings
Run Simulation
RTL Analysis
Elaboration Settings
Open Elaborated Design
Synthesis
Synthesis Settings
Run Synthesis
Synthesized Design
Constraints Wizard
Edit Timing Constrain
Set Up Debug
Report Timing Summ
Report Clock Networ
Report Clock Interact
Report Methodology
Report DRC
Report Noise
Report Utilization
Report Power
Schematic
Implementation
Implementation Setting
Run Implementation
Open Implemented Desi
Program and Debug
Bitstream Settings
Generate Bitstream
Open Hardware Manage
Synthesized Design - xc7a35tcpg236-2 (active)
Netlist
main
Nets (129)
Leaf Cells (83)
RUT (UART_RX)
Sources
Netlist
Properties
Select an object to see properties
Project Summary
Device
code6.vhd
X0Y2
X1Y2
X0Y1
X1Y1
X0Y0
X1Y0
Tcl Console
INFO: [Netlist 29-17] Analyzing 8 Unisim elements for replacement
INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
INFO: [Project 1-479] Netlist was created with Vivado 2016.4
INFO: [Project 1-570] Preparing netlist for logic optimization
Parsing XDC File [/home/dual/cs5190439/COL215P/project_7/project_7.srcs/constrs_1/new/const7.xdc]
Finished Parsing XDC File [/home/dual/cs5190439/COL215P/project_7/project_7.srcs/constrs_1/new/const7.xdc]
INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
INFO: [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.
Type a Tcl command here
Tcl Console
Messages
Log
Reports
Design Runs

SCHEMETIC VIEW-

Here is the circuit



Thank you!