

ASSIGNMENT-8

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In this assignment we have learned to send serial information without a shared clock. Also designed asynchronous serial transmitter to create a loop with the receiver developed in the previous assignment

Submission folder (2019CS50439_2019CS50434) contains -

Const8.xdc - constraint file

code_8.vhd -vhdl code file

main.bit - bitstream file

A8_report.pdf- report file

New project8 on Vivado-

The screenshot displays the Vivado 2016.4 IDE interface for a new project named 'project_8'. The top menu bar includes File, Edit, Flow, Tools, Window, Layout, and Help. The status bar at the top right shows the time as 7:42 PM and the state 'write_bitstream Complete'.

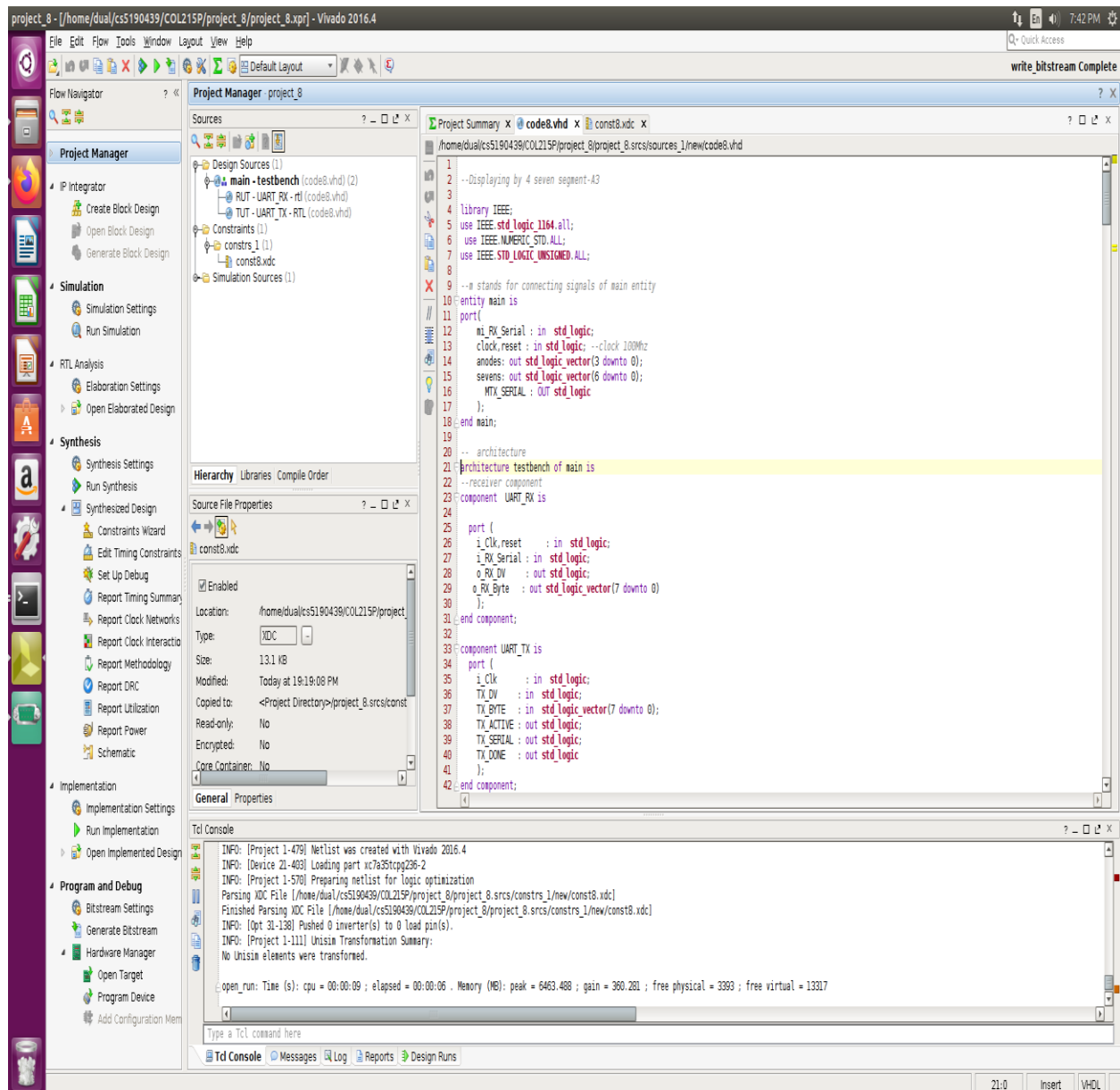
The left sidebar contains the Project Navigator with the following sections:

- Project Manager**
 - Create Block Design
 - Open Block Design
 - Generate Block Design
- Simulation**
 - Simulation Settings
 - Run Simulation
- RTL Analysis**
 - Elaboration Settings
 - Open Elaborated Design
- Synthesis**
 - Synthesis Settings
 - Run Synthesis
 - Synthesized Design
 - Constraints Wizard
 - Edit Timing Constraints
 - Set Up Debug
 - Report Timing Summary
 - Report Clock Networks
 - Report Clock Interaction
 - Report Methodology
 - Report DRC
 - Report Utilization
 - Report Power
 - Schematic
- Implementation**
 - Implementation Settings
 - Run Implementation
 - Open Implemented Design
- Program and Debug**
 - Bitstream Settings
 - Generate Bitstream
 - Hardware Manager
 - Open Target
 - Program Device
 - Add Configuration Memory

The main workspace is divided into several panes:

- Project Manager**: Shows the project hierarchy with Design Sources (main - testbench, RUT - UART_RX - rtl, TUT - UART_TX - rtl), Constraints (constrs_1), and Simulation Sources.
- Source File Properties**: Displays properties for the 'const8.xdc' file, including Location, Type (XDC), Size (13.1 KB), and Modified date.
- Project Summary**: Provides an overview of the project, including Project location, Product family (Artix-7), Project part (xc7a35tqpg236-2), Top module name (main), Target language (VHDL), and Simulator language (Mixed).
- Synthesis**: Shows the synthesis status as 'Complete' with 3 warnings. The strategy used is 'Vivado Synthesis Defaults'.
- Implementation**: Shows the implementation status as 'Complete' with 3 warnings. The strategy used is 'Vivado Implementation Defaults'.
- DRC Violations**: Shows a summary of 1 warning and a link to the 'Implemented DRC Report'.
- Timing**: Displays timing metrics such as Worst Negative Slack (WNS), Total Negative Slack (TNS), Number of Failing Endpoints, and Total Number of Endpoints. It also includes a link to the 'Implemented Timing Report'.
- Power**: Shows power metrics including Total On-Chip Power (8.085 W), Junction Temperature (65.4 °C), Thermal Margin (19.6 °C (3.9 W)), Effective θ_{JA} (5.0 °C/W), Power supplied to off-chip devices (0 W), and Confidence level (Low). It includes a link to the 'Implemented Power Report'.
- Utilization - Post-implementation**: A bar chart showing the utilization of various resources: LUT (1%), FF (1%), IO (1.4%), and BUFG (6%).
- Tcl Console**: Displays the Tcl commands and their outputs, including information about the Netlist creation, device loading, and the final open_run results.

VHDL code on Vivado -



The code is also provided in the submission file

DESCRIPTION

Here we assumed normal indexing of segments of seven segment display(B-2,etc)

Design decision

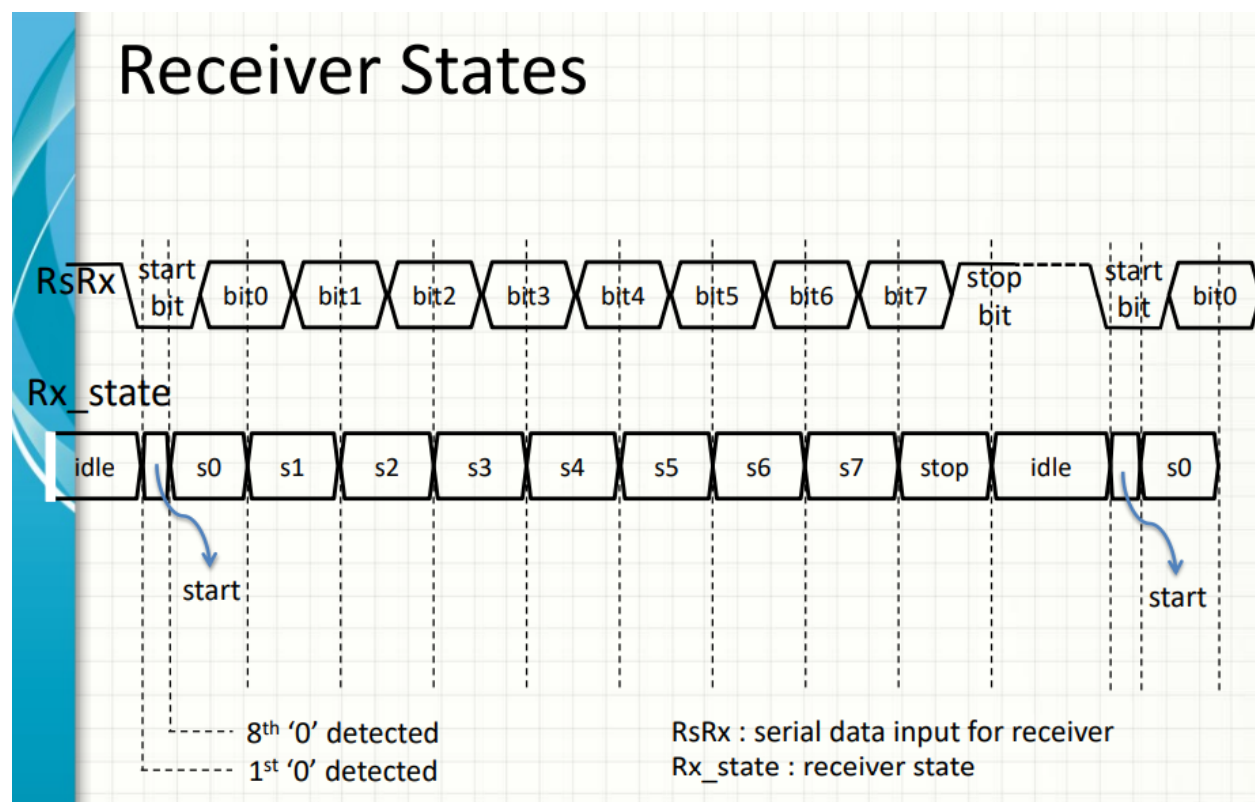
Designed asynchronous serial receiver/transmitter with baud rate = 9600, 8 data bits, no parity bits and 1 stop bit.

Made a provision for resetting the FSM to idle state by a push button(display "00"),

Receiver-

Receiver component have serial input and parallel byte output,which we are storing to display on seven segment display.

For others Simply followed states idea learned from lectures(below image)-

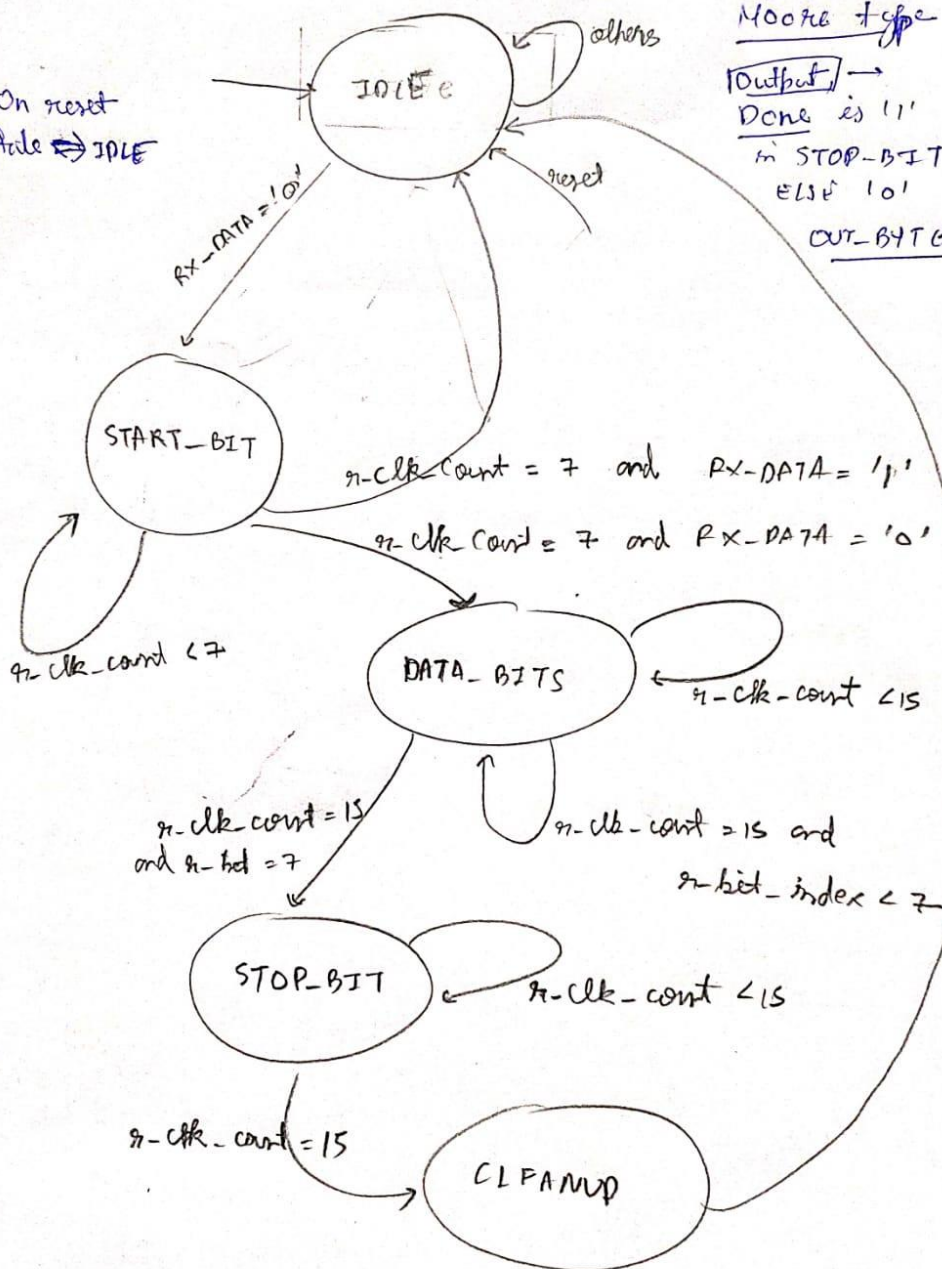


Here in state diagram ,we can find how these total 5 states related (IDLE,START_BIT,DATA_BITS,STOP_BIT,CLEANUP)-

STATE DIAGRAM-Receiver

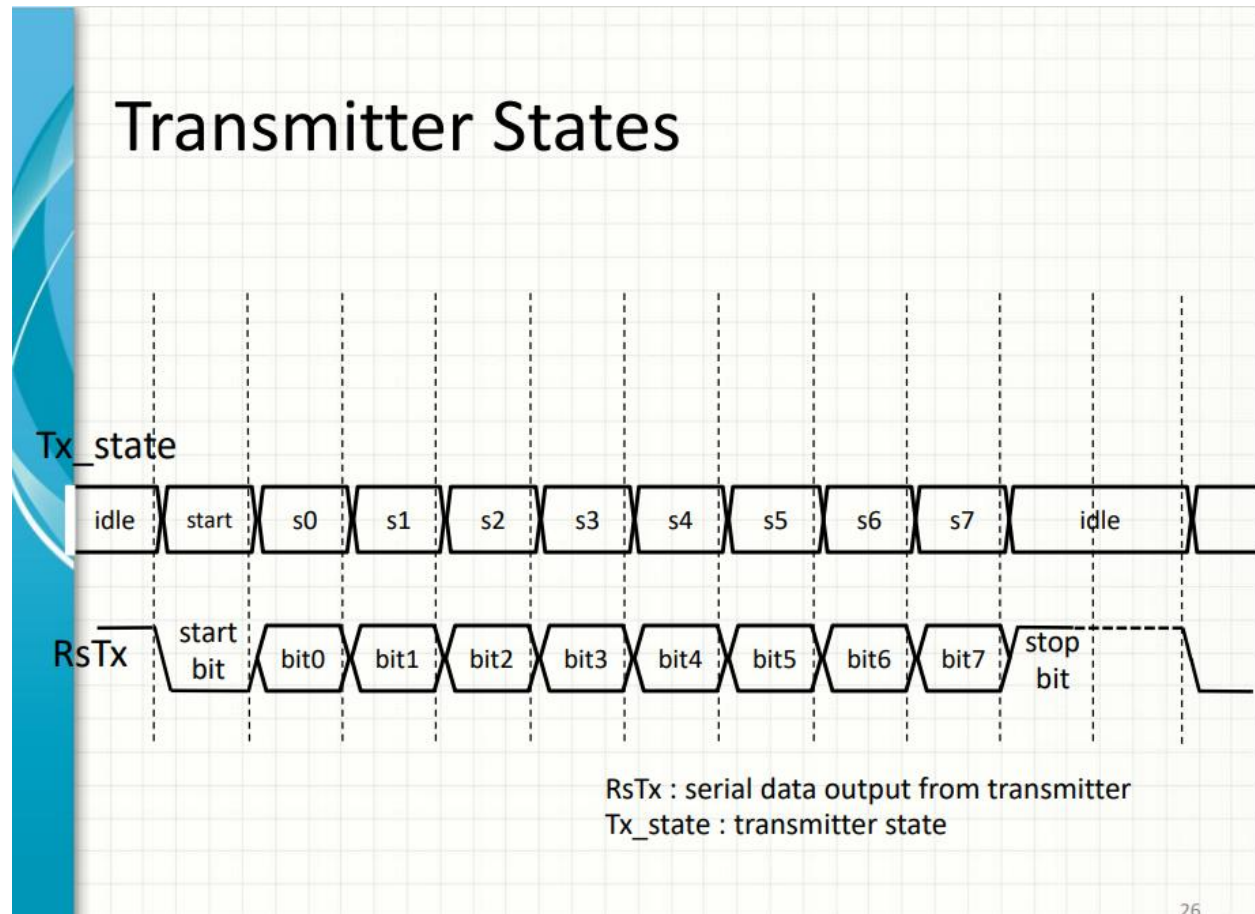
~~ASM CHART~~ (Receiver side)
STATE DIAGRAM

• On reset
my state \Rightarrow IDLE



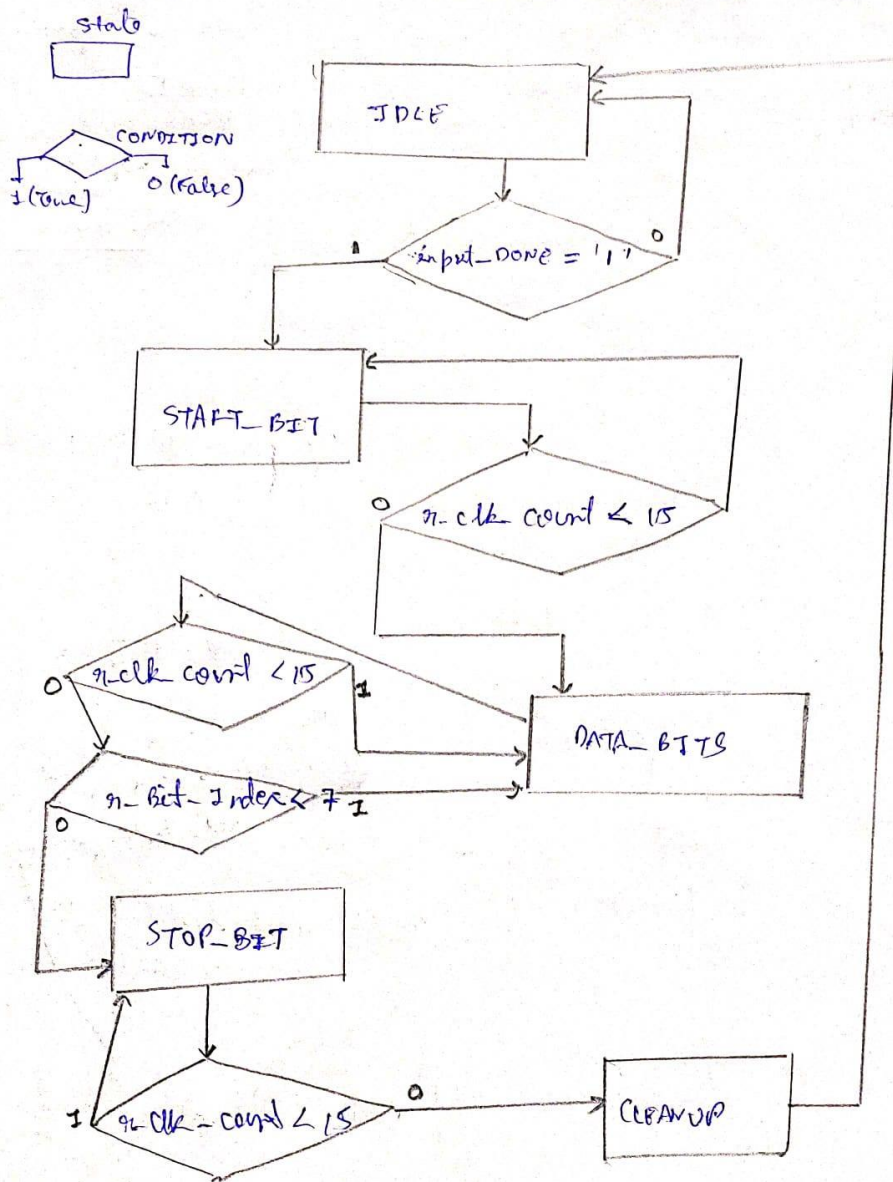
Transmitter-

Transmitter component also have similar 5 states with tstate type and related as- (IDLE,START_BIT,DATA_BITS,STOP_BIT,CLEANUP).



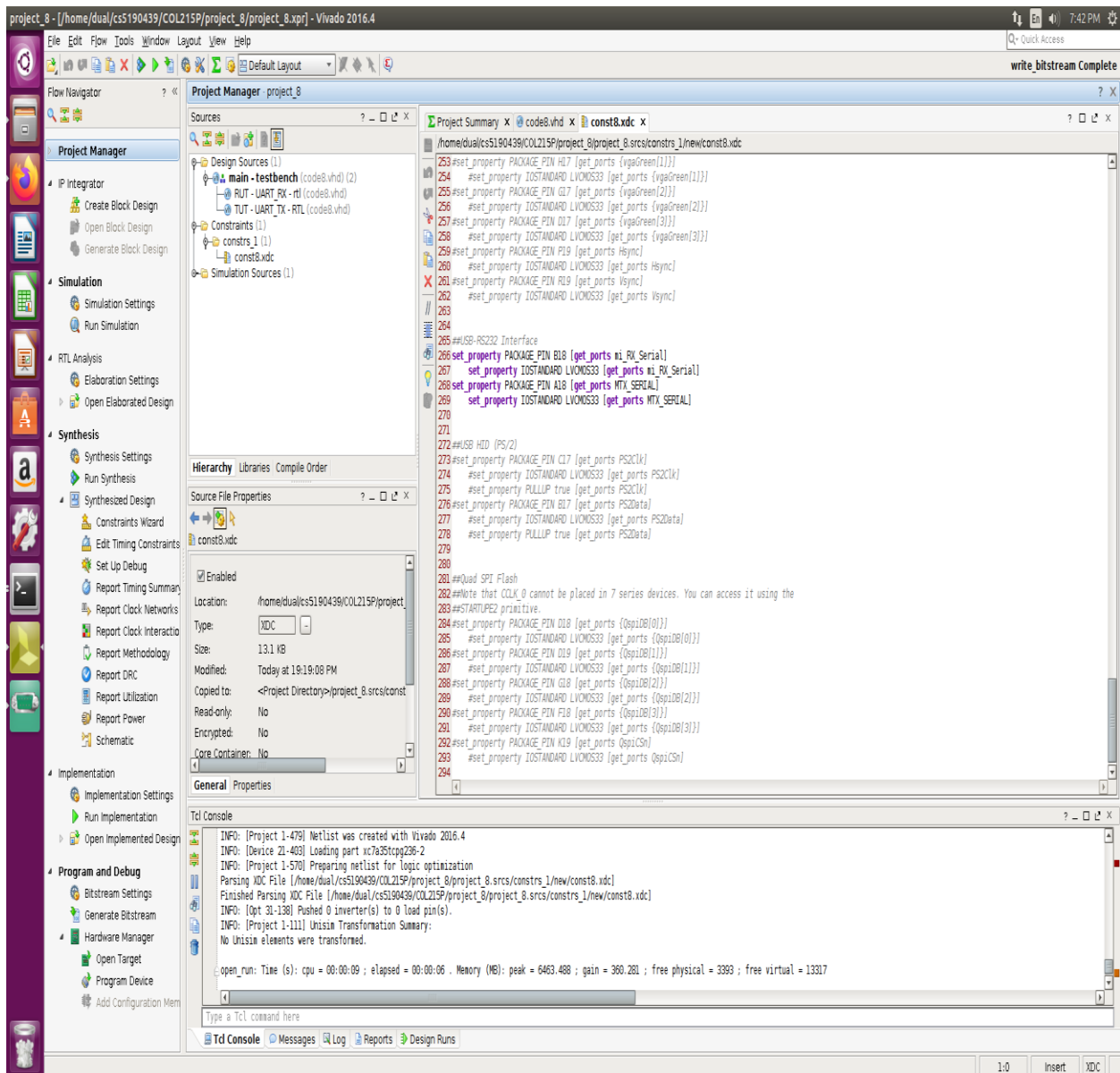
STATE DIAGRAM/ASM CHART-Transmitter

ASM CHART (Transmitter side)



Constraint file

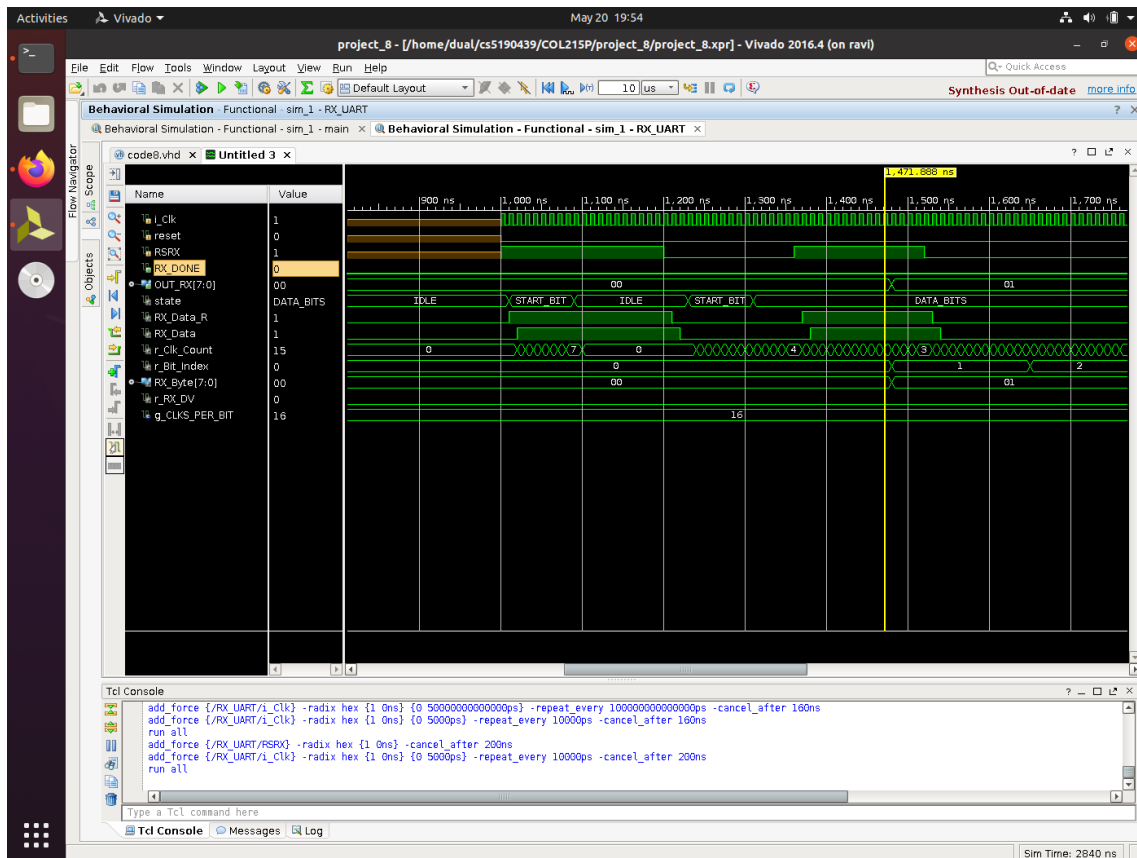
Matched receiver serial input port and transmitter serial output port in addition to previous A3 ports of displaying 7 segment display

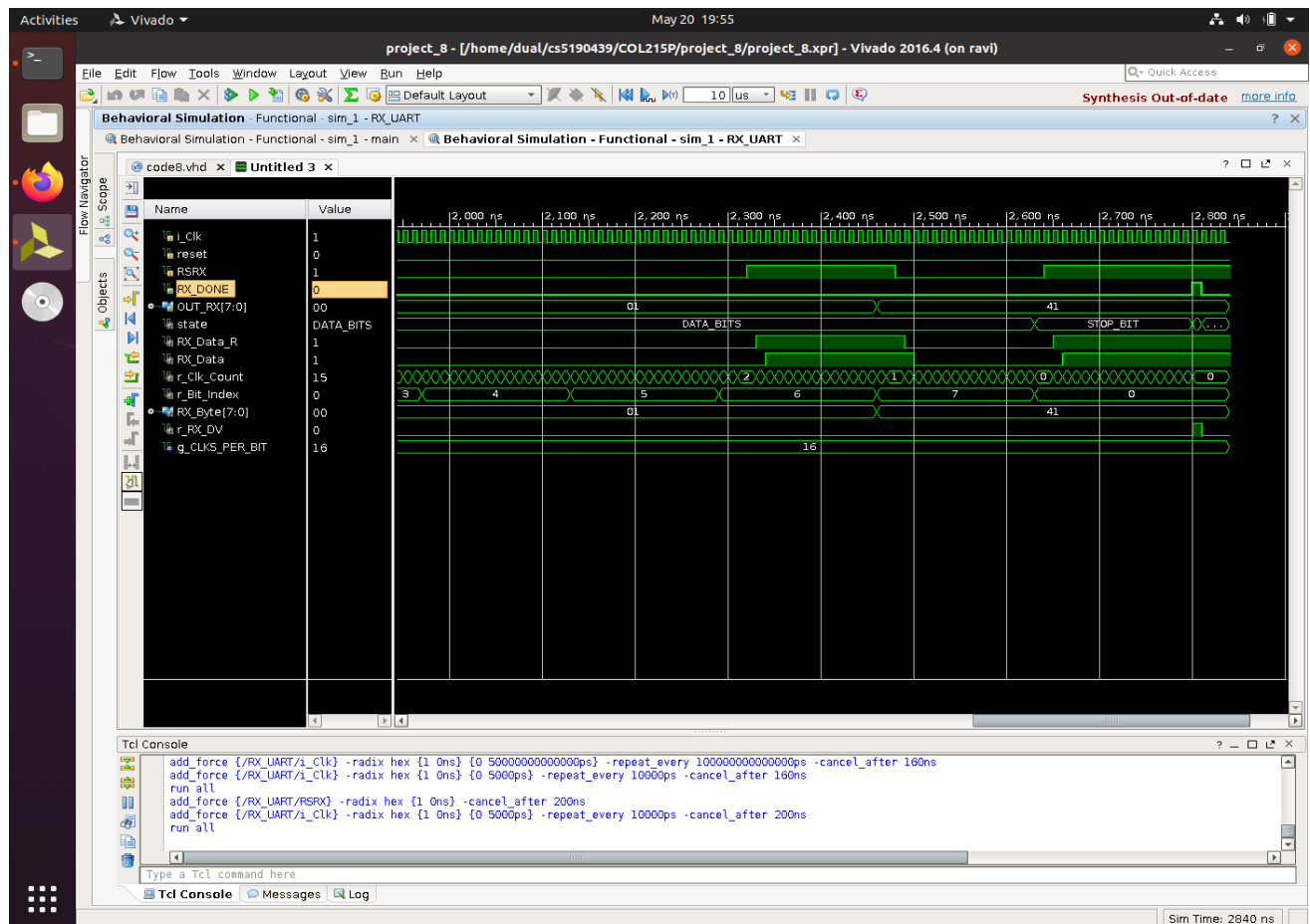


Simulation on vivado

For simulation tried to use one clock of $16 \times$ baud rate for single "A" character

Here wave generated can be found similar to theoretical conceptual diagram told above.





Similarly simulation of transmitter component also have wave similar to theoretical told image above in description.

After doing above steps or till simulation work, then for implementing design on basys board, we first synthesized design, ran the implementation, then generated Bitstream and finally opened the hardware manager to program device.

Resources utilization-

The screenshot displays the Vivado 2016.4 IDE interface. The top menu bar includes File, Edit, Flow, Tools, Window, Layout, and Help. The left sidebar contains a Project Manager and a Synthesis section with options like Synthesis Settings, Run Synthesis, and Synthesized Design. The main workspace is divided into several panes:

- Netlist**: Shows a list of components including Nets (162), Leaf Cells (115), RUT (UART_RX), and TUT (UART_TX).
- Statistics**: Displays a table of primitive statistics.
- Utilization Report - synth_1**: Shows a detailed breakdown of resource usage.
- Tcl Console**: Displays the output of the synthesis process.

Primitive Statistics Table:

Primitive type	Count
FLOP LATCH	79
LUT	106
CARRY	5
IO	15
CLK	2
OTHERS	6

Utilization Report - synth_1 Table:

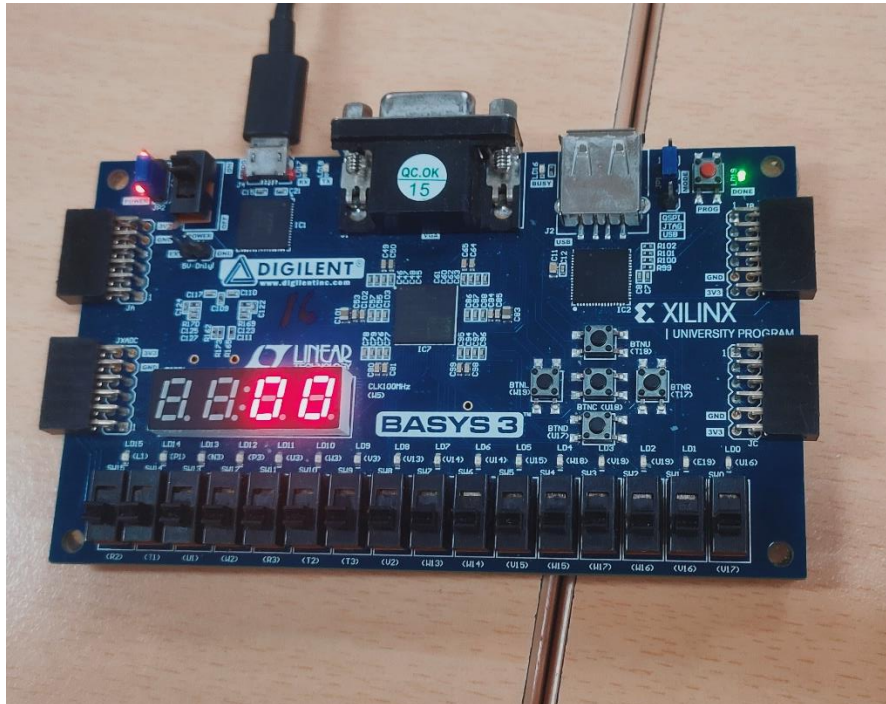
Ref Name	Used	Functional	Category		
139	ICAPE2	0	0	2	0.00
140	PCIE_2_1	0	0	1	0.00
141	STARTUP2	0	0	1	0.00
142	XADC	0	0	1	0.00
143					
144					
145					
146	7. Primitives				
147					
148					
149					
150	Ref Name	Used	Functional	Category	
151					
152	FLOP	76		Flop & Latch	
153	LUT6	29		LUT	
154	LUT4	25		LUT	
155	LUT1	22		LUT	
156	LUT5	19		LUT	
157	IOBUF	12		IO	
158	LUT2	6		LUT	
159	LUT3	5		LUT	
160	CARRY4	5		CarryLogic	
161	IOBUF	3		IO	
162	FDCE	3		Flop & Latch	
163	BUFG	2		Clock	
164					
165					
166					
167	8. Black Boxes				
168					
169					
170					
171	Ref Name	Used			
172					
173					
174					
175	9. Instantiated Netlists				
176					
177					
178					
179	Ref Name	Used			

Tcl Console Output:

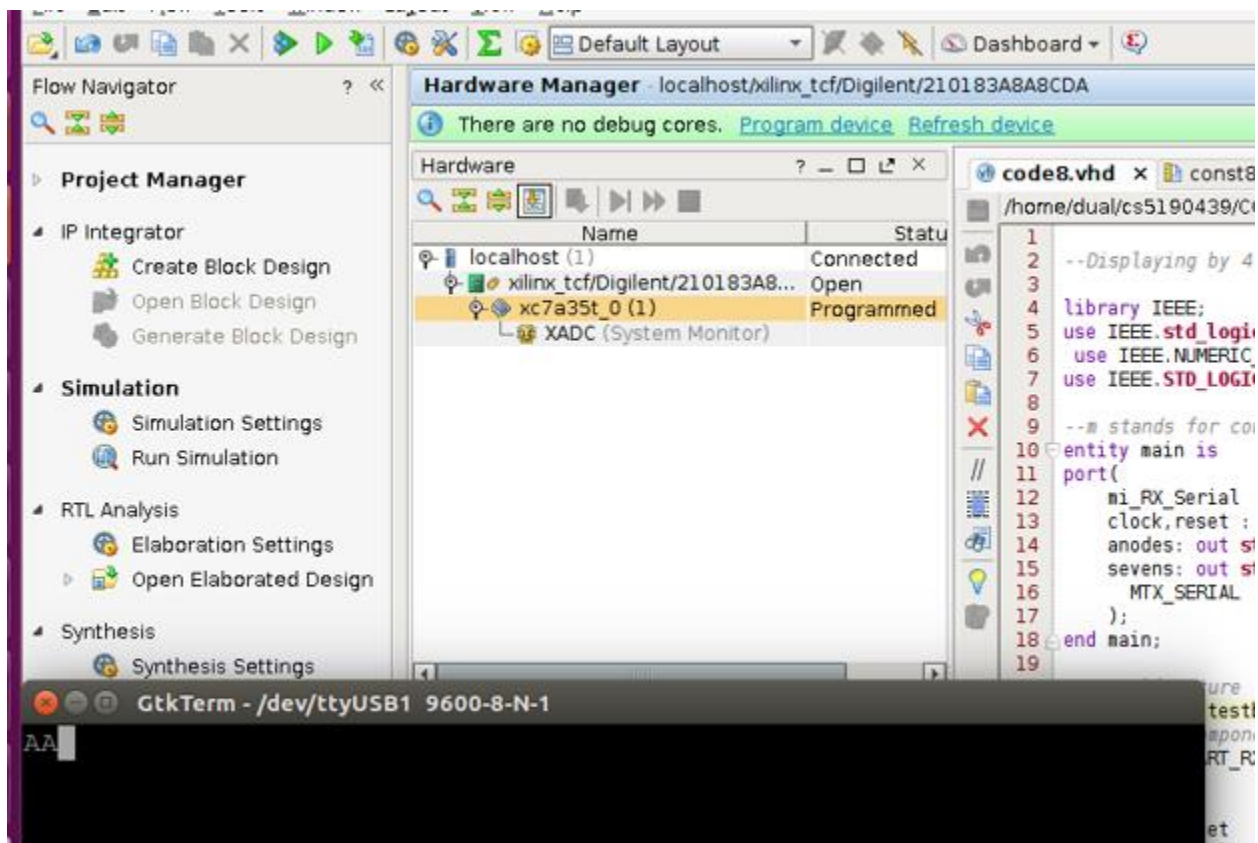
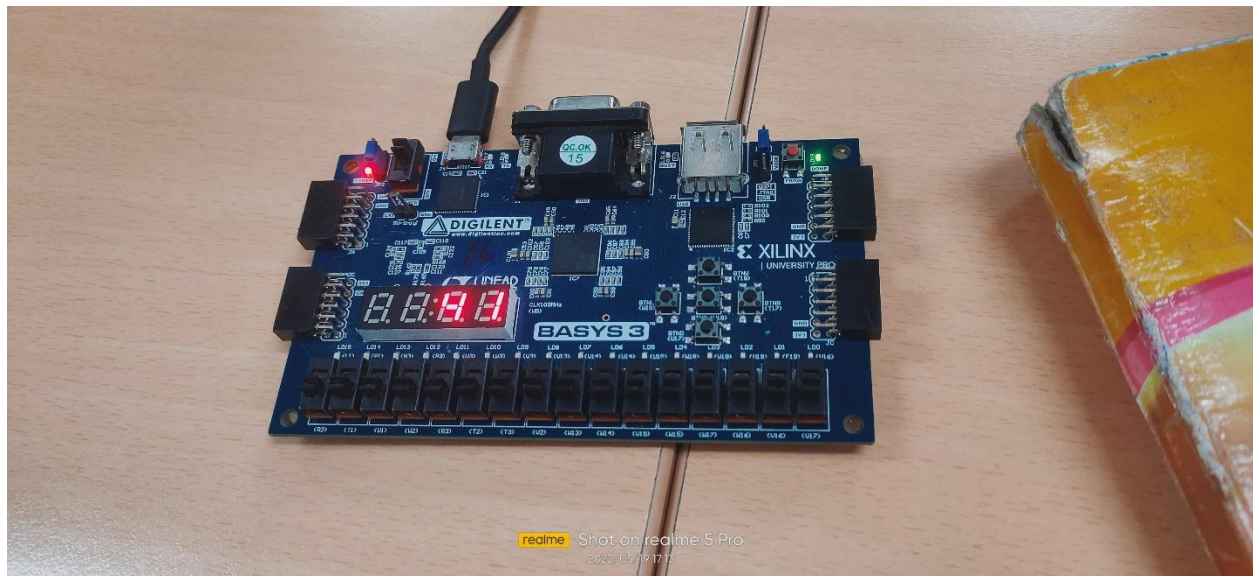
```
INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
INFO: [Project 1-479] Netlist was created with Vivado 2016.4
INFO: [Device ZU-403] Loading part xc7a35tccpg236-2
INFO: [Project 1-570] Preparing netlist for logic optimization
Parsing XDC File [/home/dual/cs5190439/COL215P/project_8/srcs/constrs_1/new/const8.xdc]
Finished Parsing XDC File [/home/dual/cs5190439/COL215P/project_8/srcs/constrs_1/new/const8.xdc]
INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
INFO: [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.

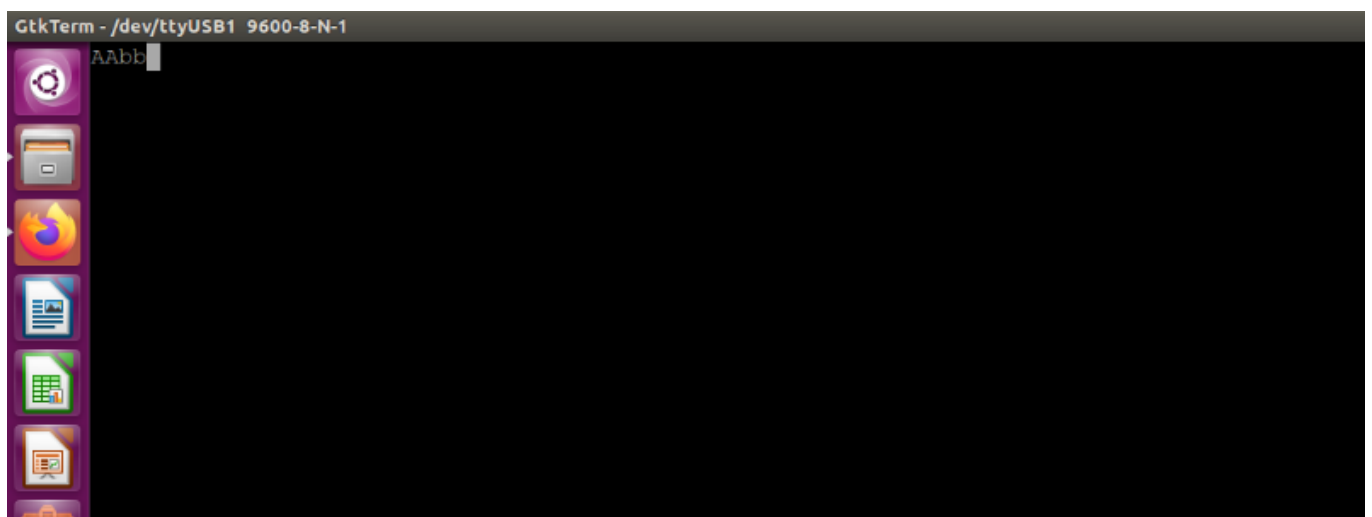
open_run: Time (s): cpu = 00:00:09 ; elapsed = 00:00:06 ; Memory (MB): peak = 6463.488 ; gain = 360.281 ; free physical = 3393 ; free virtual = 13317
```

Testing on Basys3 board and gtk-
initial state-

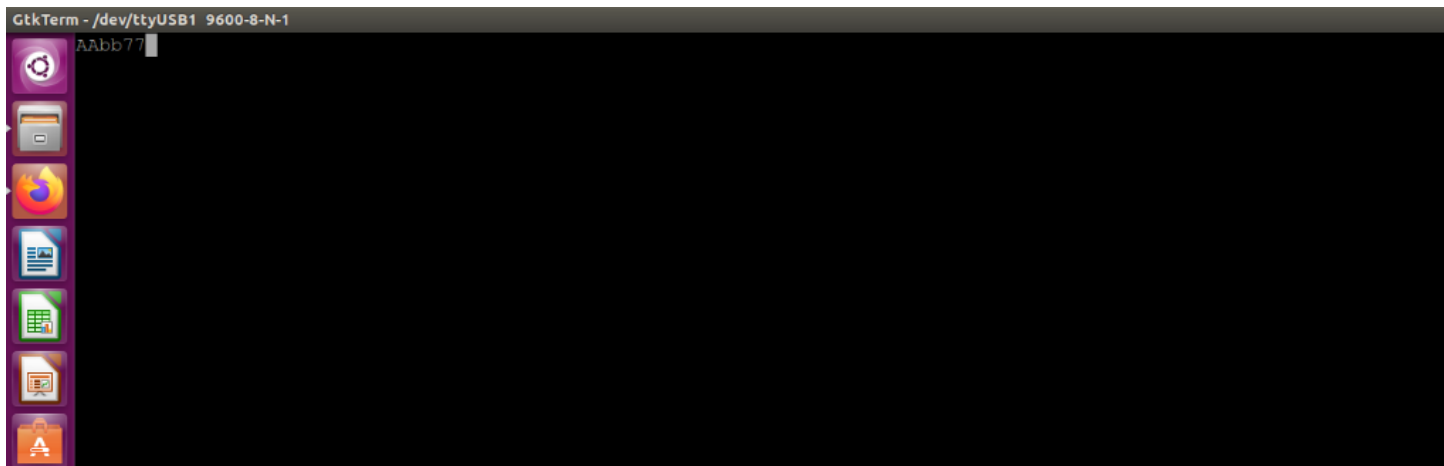
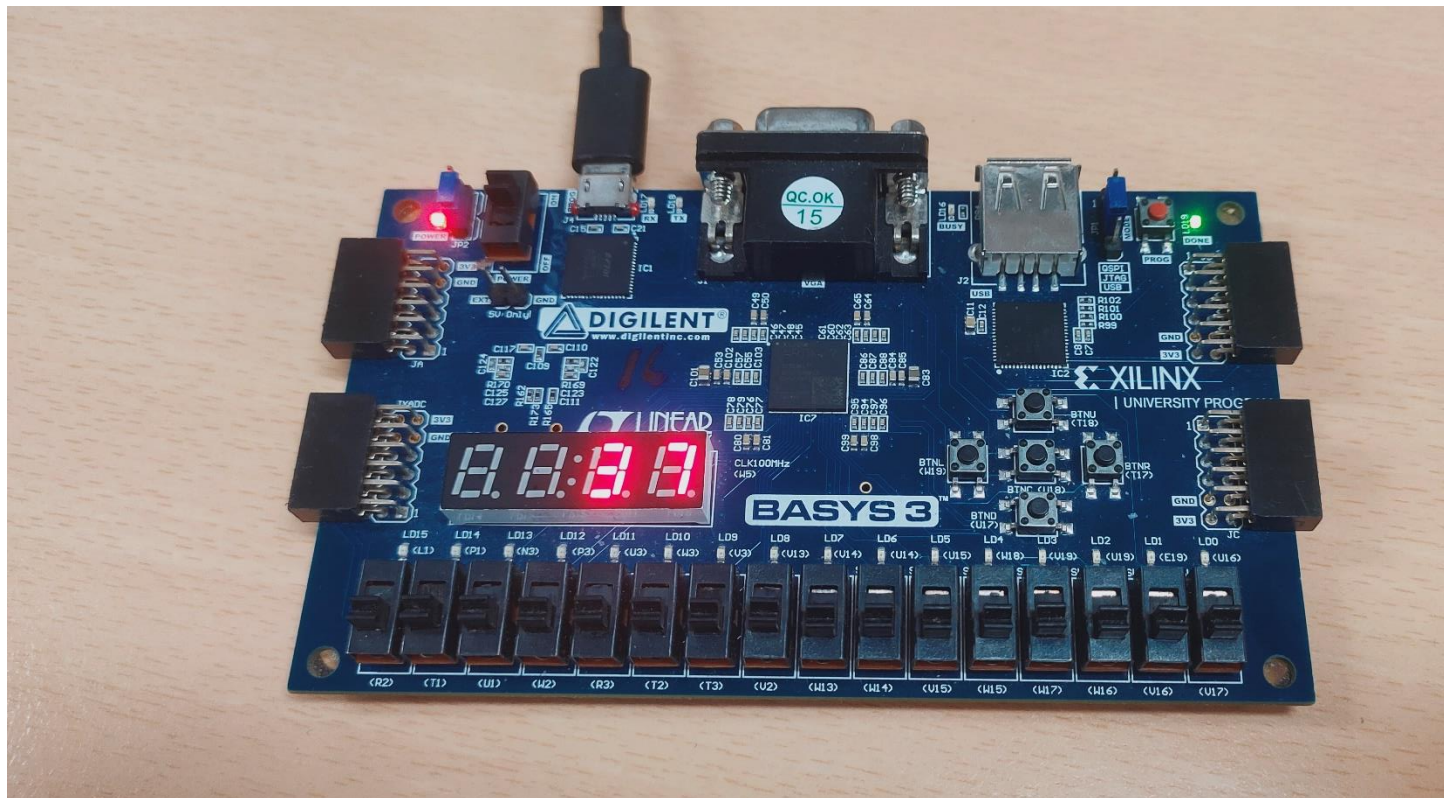


When A,ASCII Char pressed on keyboard,then display showing hexadecimal representation-



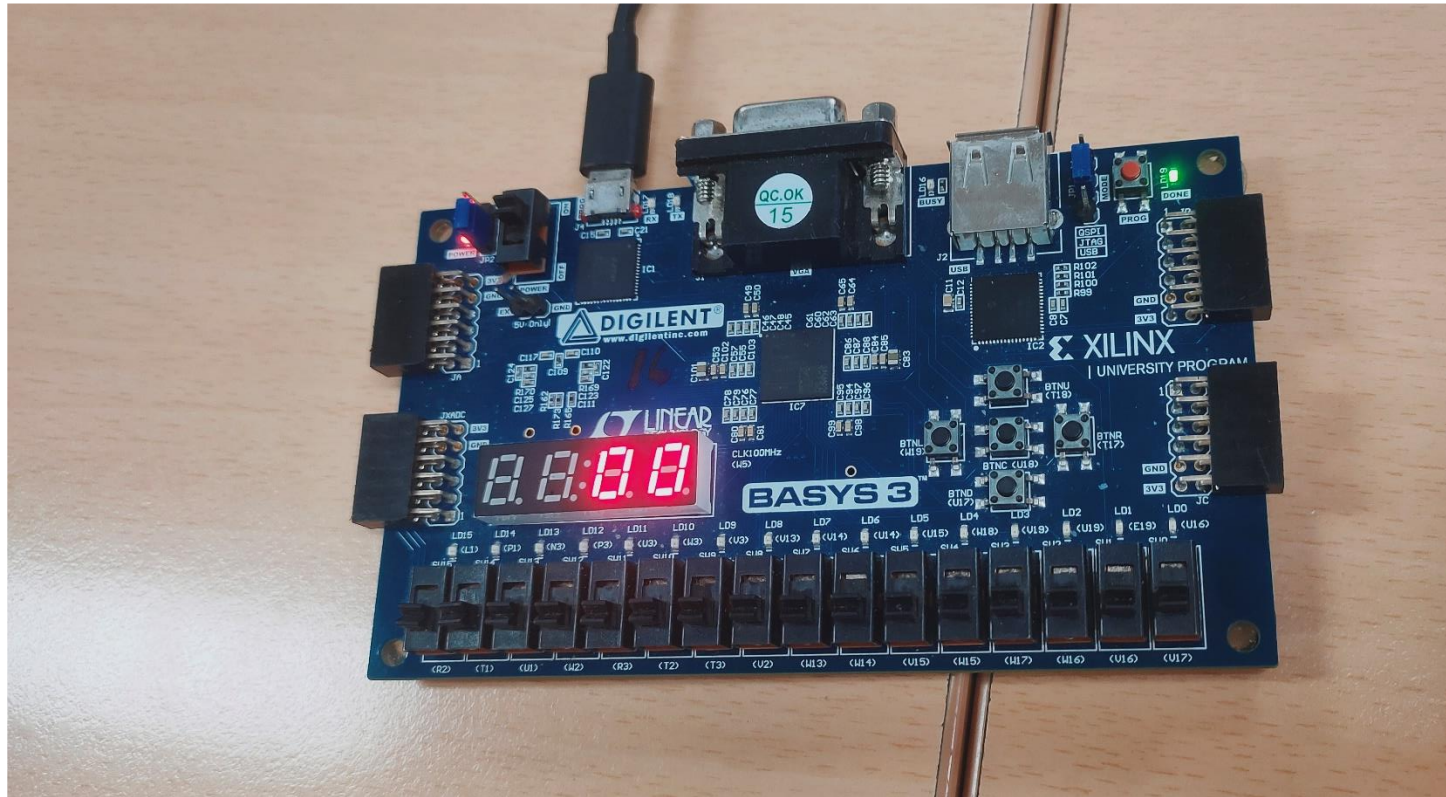


When 7,ASCII Char pressed on keyboard,then display showing hexadecimal representation-

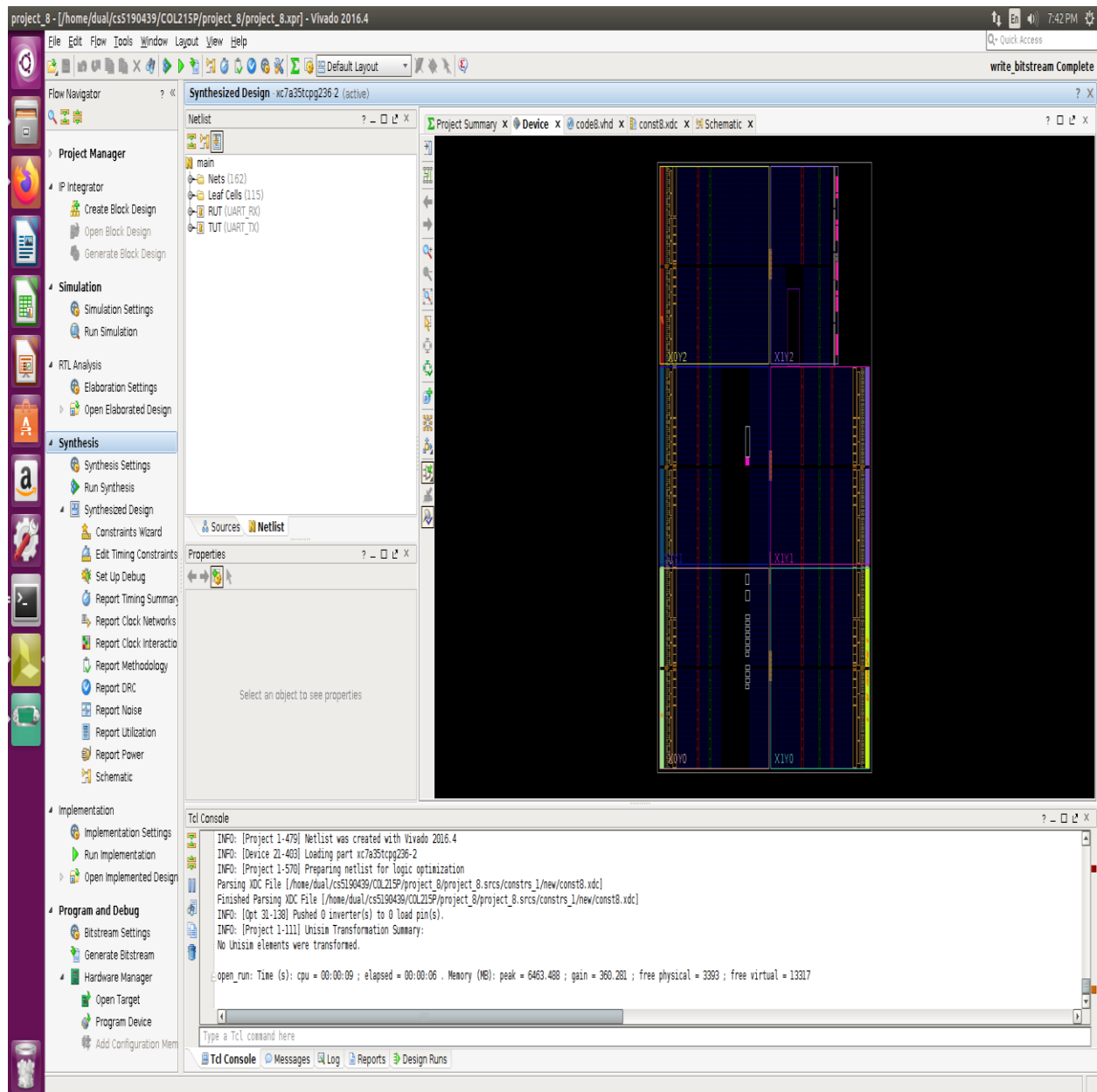


Here we tested with the help of gtk by echoing the receiver serial input .

On reset button,screen of fpga will be seen as with change to State idle-

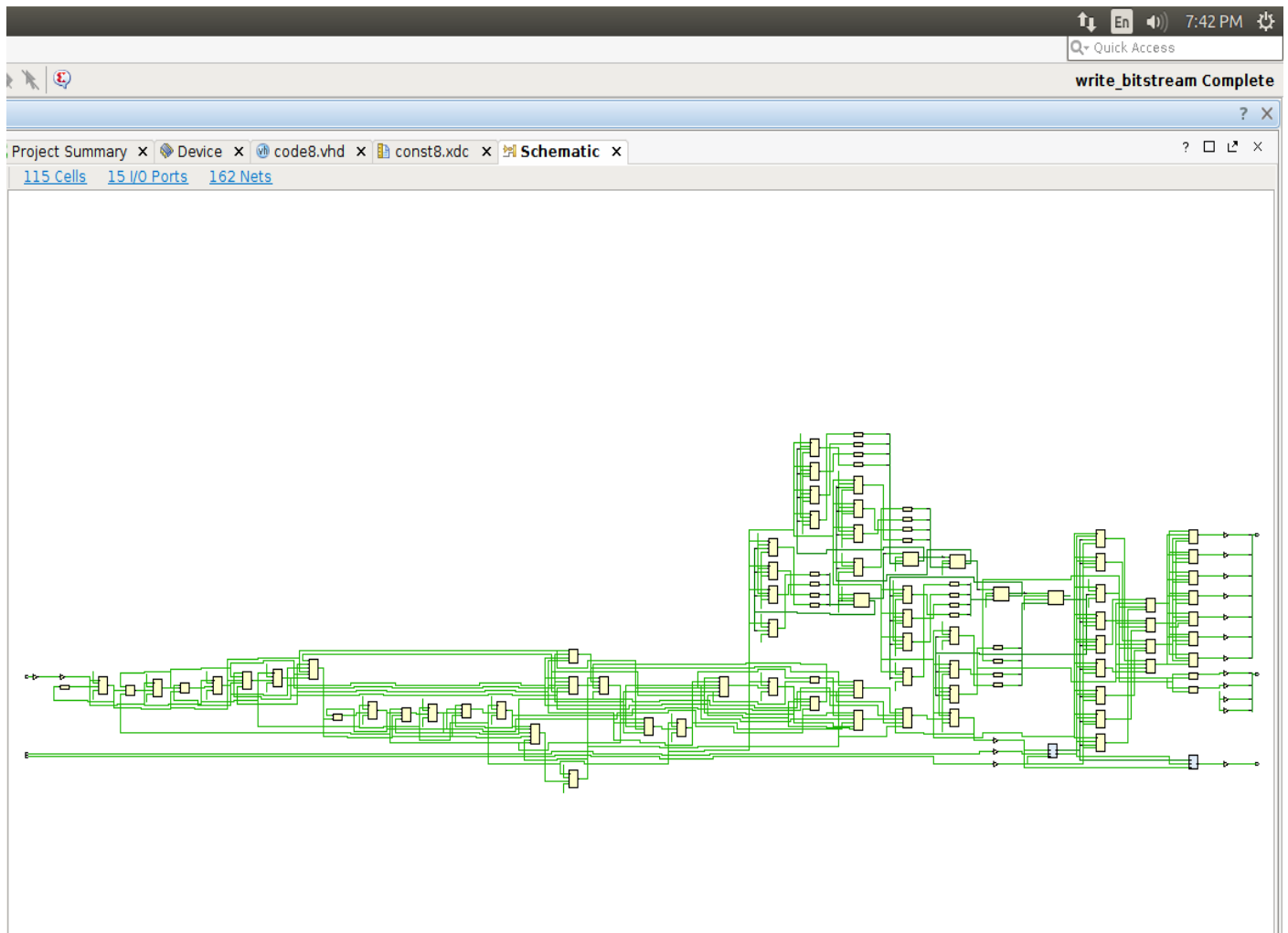


Device view-



SCHEMATIC VIEW-

Here is the circuit



Thank you!