ASSIGNMNET-3

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In this assignment we learned and designed to display multiple decimal/hexadecimal digits using 7- segment displays. Here we designed general module of quadruple seven segment display.

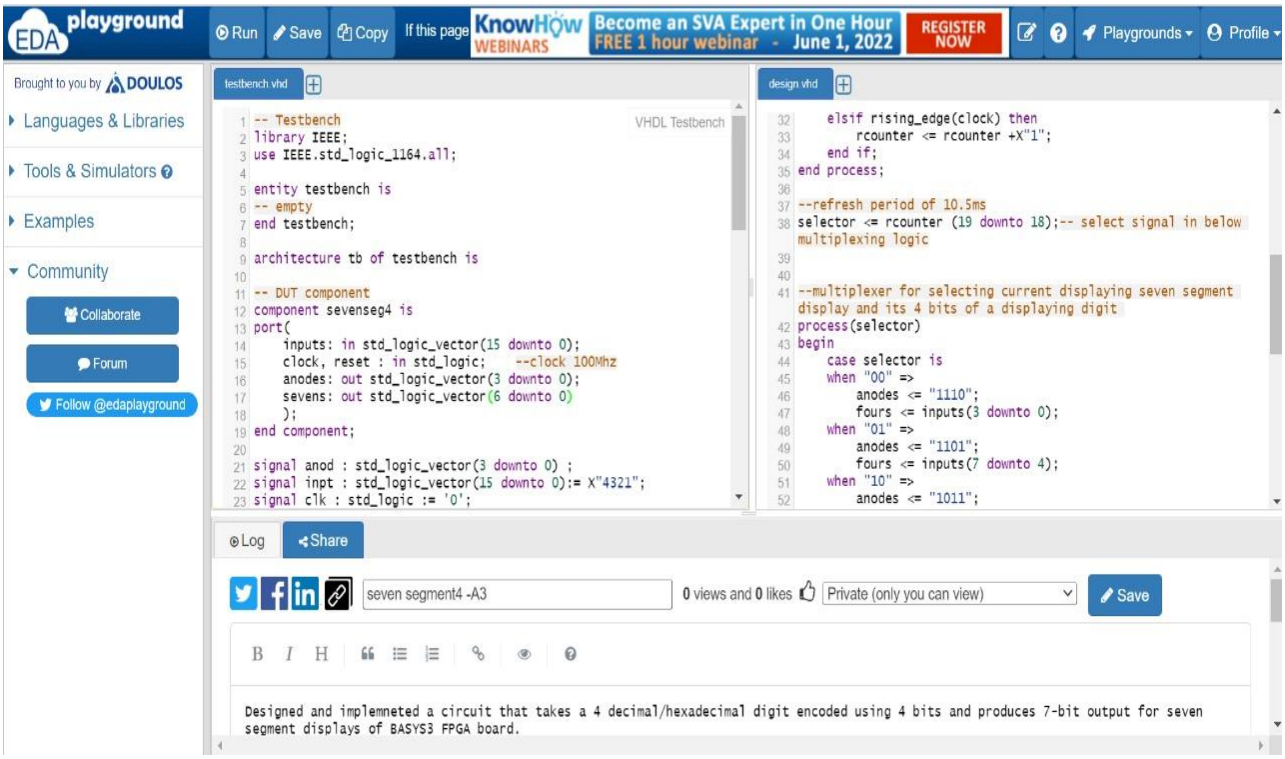
Submission folder (2019CS50439_2019CS50434) contains -

- **project3.xdc - constraint file**
- **project3_a2.vhd -vhdl code file**
- **sevenseg.bit - bitstream file**
- **A3_report.pdf- report file**

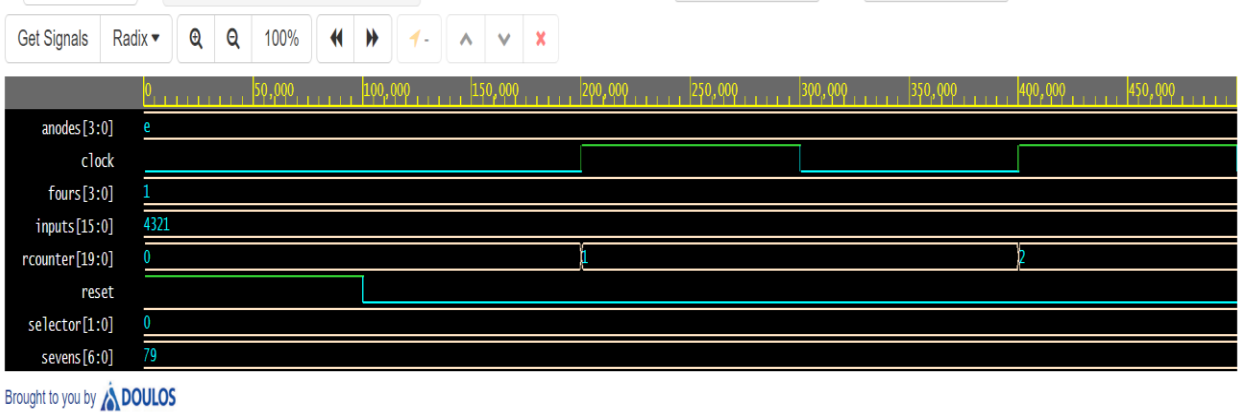
Some details of main steps involved in Assignment3 and related lab work are in next pages -

For Assignment3, we first designed and simulated on Edaplaground before lab-

EDA PLAYGROUND Code and simulation-

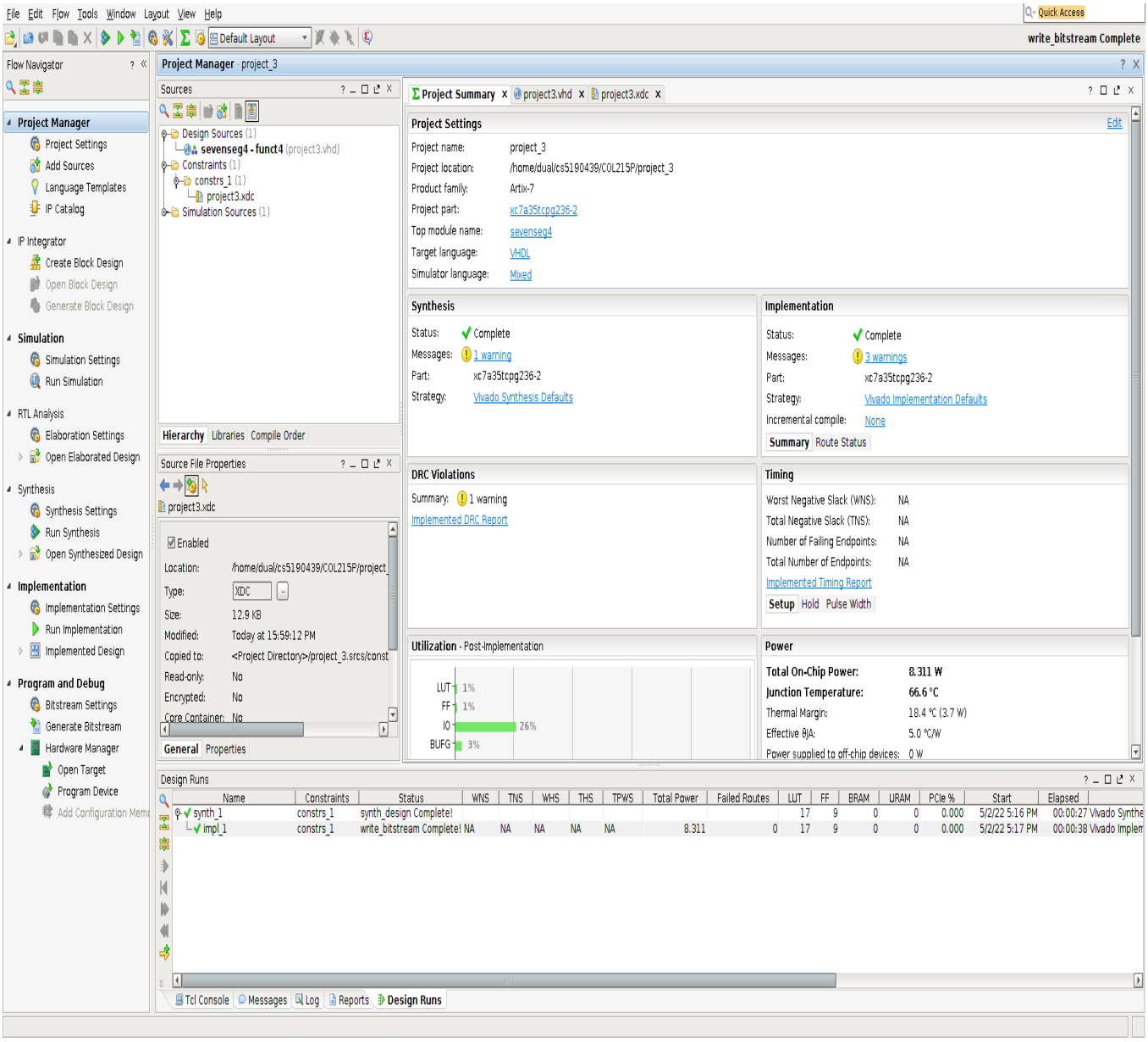


EDA PLAYGROUND EPWAVE

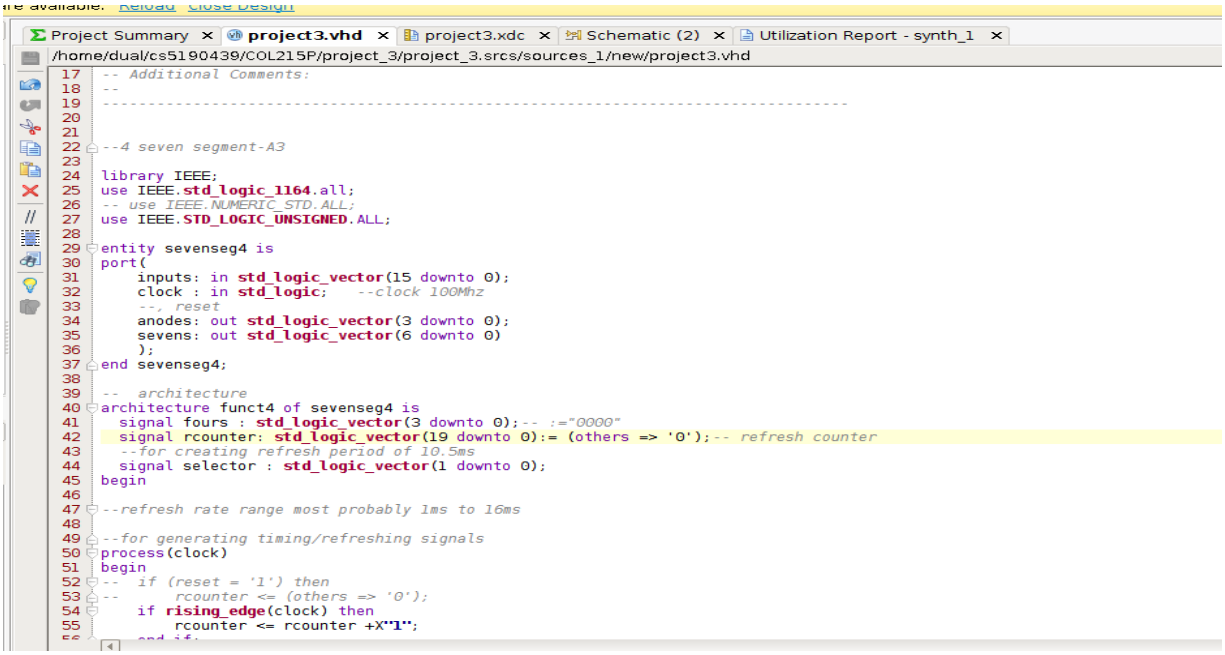


In EDAPLAYGROUND ,simulated designed code for Assignment-2,for it created separate testbench and then tested for different values of fourt signal

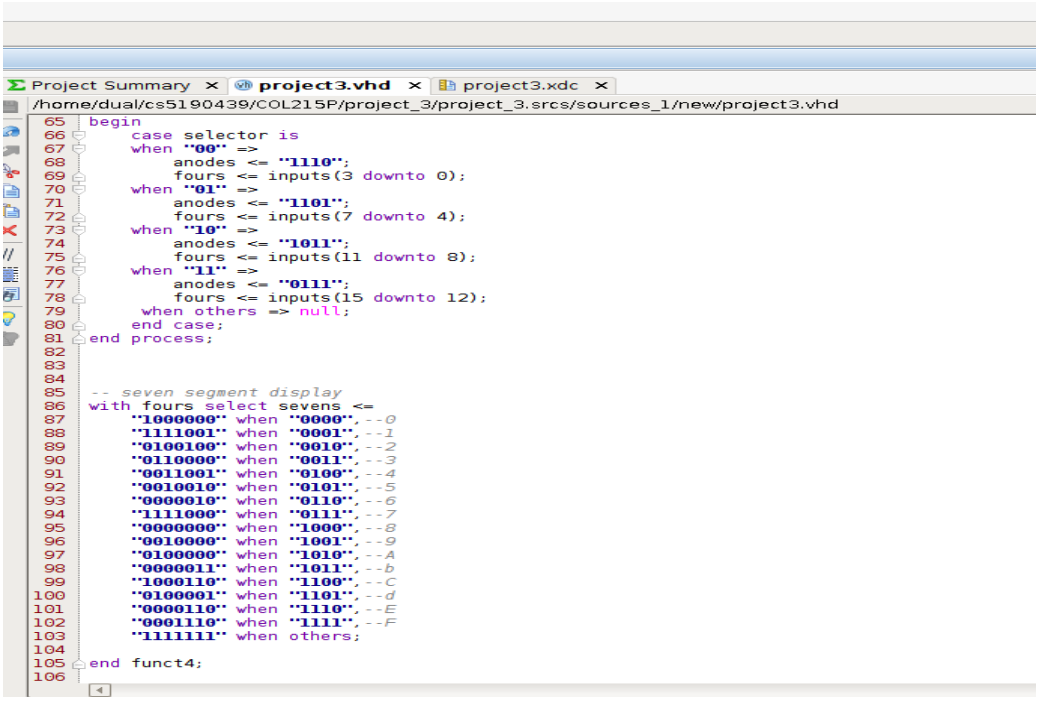
New project2 on Vivado-



VHDL code on Vivado -




```
17  -- Additional Comments:
18  --
19  ----------------------------------------------------------------------------------
20
21
22  --4 seven segment-A3
23
24  library IEEE;
25  use IEEE.std_logic_1164.all;
26  -- use IEEE.NUMERIC_STD.ALL;
27  use IEEE.STD_LOGIC_UNSIGNED.ALL;
28
29  entity sevenseg4 is
30  port(
31      inputs: in std_logic_vector(15 downto 0);
32      clock : in std_logic;    --clock 100Mhz
33      --, reset
34      anodes: out std_logic_vector(3 downto 0);
35      sevens: out std_logic_vector(6 downto 0)
36      );
37  end sevenseg4;
38
39  --  architecture
40  architecture funct4 of sevenseg4 is
41    signal fours : std_logic_vector(3 downto 0);-- :="0000"
42    signal rcounter: std_logic_vector(19 downto 0):= (others => '0');-- refresh counter
43    --for creating refresh period of 10.5ms
44    signal selector : std_logic_vector(1 downto 0);
45  begin
46
47  --refresh rate range most probably 1ms to 16ms
48
49  --for generating timing/refreshing signals
50  process(clock)
51  begin
52  --  if (reset = '1') then
53  --      rcounter <= (others => '0');
54      if rising_edge(clock) then
55          rcounter <= rcounter +X"1";
```




```
65  begin
66      case selector is
67      when "00" =>
68          anodes <= "1110";
69          fours <= inputs(3 downto 0);
70      when "01" =>
71          anodes <= "1101";
72          fours <= inputs(7 downto 4);
73      when "10" =>
74          anodes <= "1011";
75          fours <= inputs(11 downto 8);
76      when "11" =>
77          anodes <= "0111";
78          fours <= inputs(15 downto 12);
79       when others => null;
80      end case;
81  end process;
82
83
84
85  -- seven segment display
86  with fours select sevens <=
87      "1000000" when "0000",--0
88      "1111001" when "0001",--1
89      "0100100" when "0010",--2
90      "0110000" when "0011",--3
91      "0011001" when "0100",--4
92      "0010010" when "0101",--5
93      "0000010" when "0110",--6
94      "1111000" when "0111",--7
95      "0000000" when "1000",--8
96      "0010000" when "1001",--9
97      "0100000" when "1010",--A
98      "0000011" when "1011",--b
99      "1000110" when "1100",--C
100     "0100001" when "1101",--d
101     "0000110" when "1110",--E
102     "0001110" when "1111",--F
103     "1111111" when others;
104
105 end funct4;
106
```

The code is also provided in the submission file

DESCRIPTION

Here we assumed normal indexing of segments of seven segment display(B-2,etc)

Here the code takes 16 bit input through the switches for the 4 LEDs (4 bits for each) and displays the respected digit.

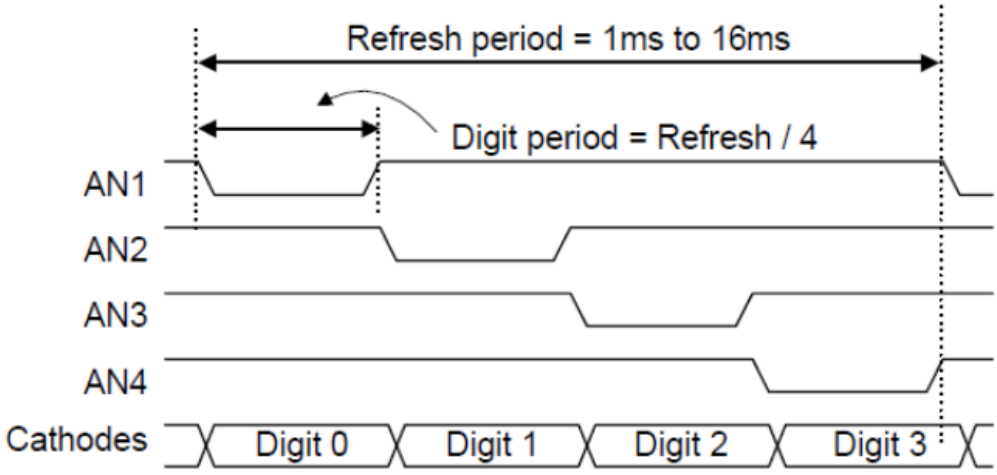
The refresh rate (the rate when every LED is switched to) is around 10ms.

Refreshing LEDs at this frequency gives us the perception that all LEDs are on at the same time,as this frequency around 95Hz (10.5 ms refresh period used in submitted code) which is greater than persistence vision of frequency - 25 Hz

Our eyes are able to percept proper displays for the refresh rate range of around 1ms – 16ms.

But at last we have also tested thoroughly to determine refresh rate range in our setup,found fine display refresh rate range, 0.01ms -20.9 ms.

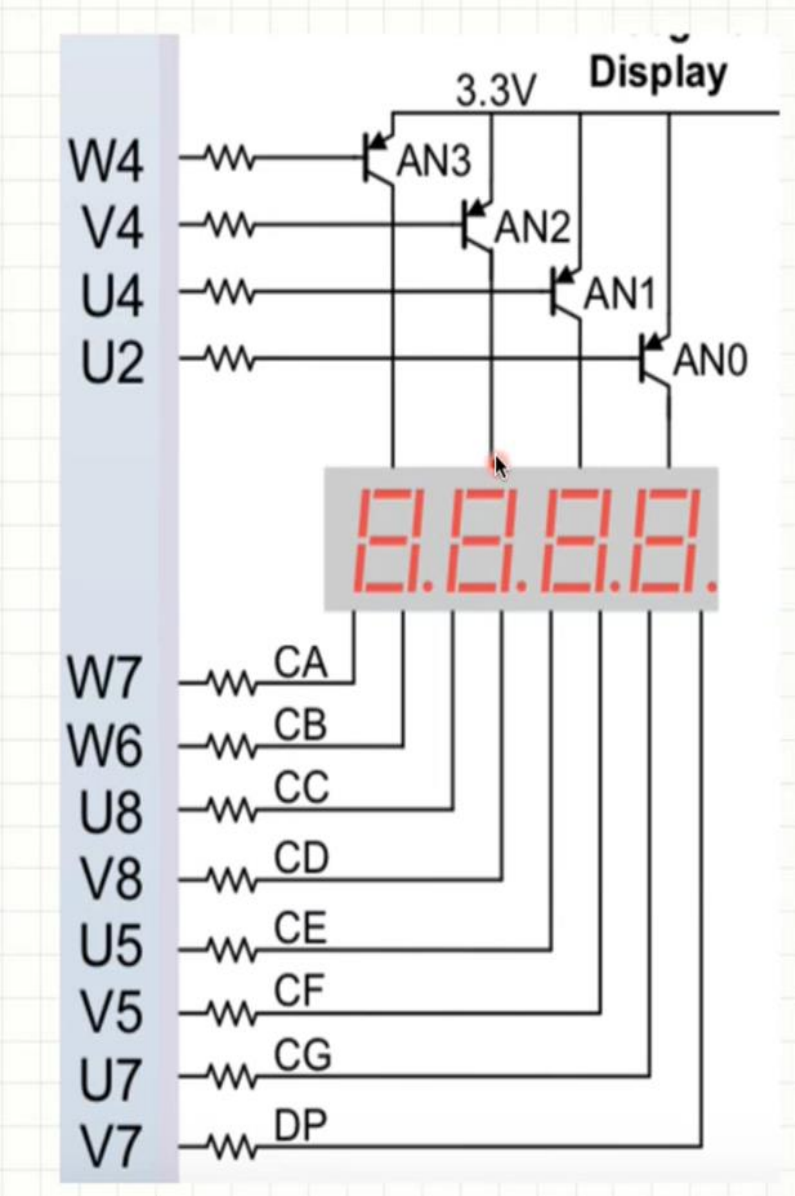
Below is timing diagram for refreshing the 4-digit seven-segment display on Basys 3 FPGA-



Seven-segment display timing diagram

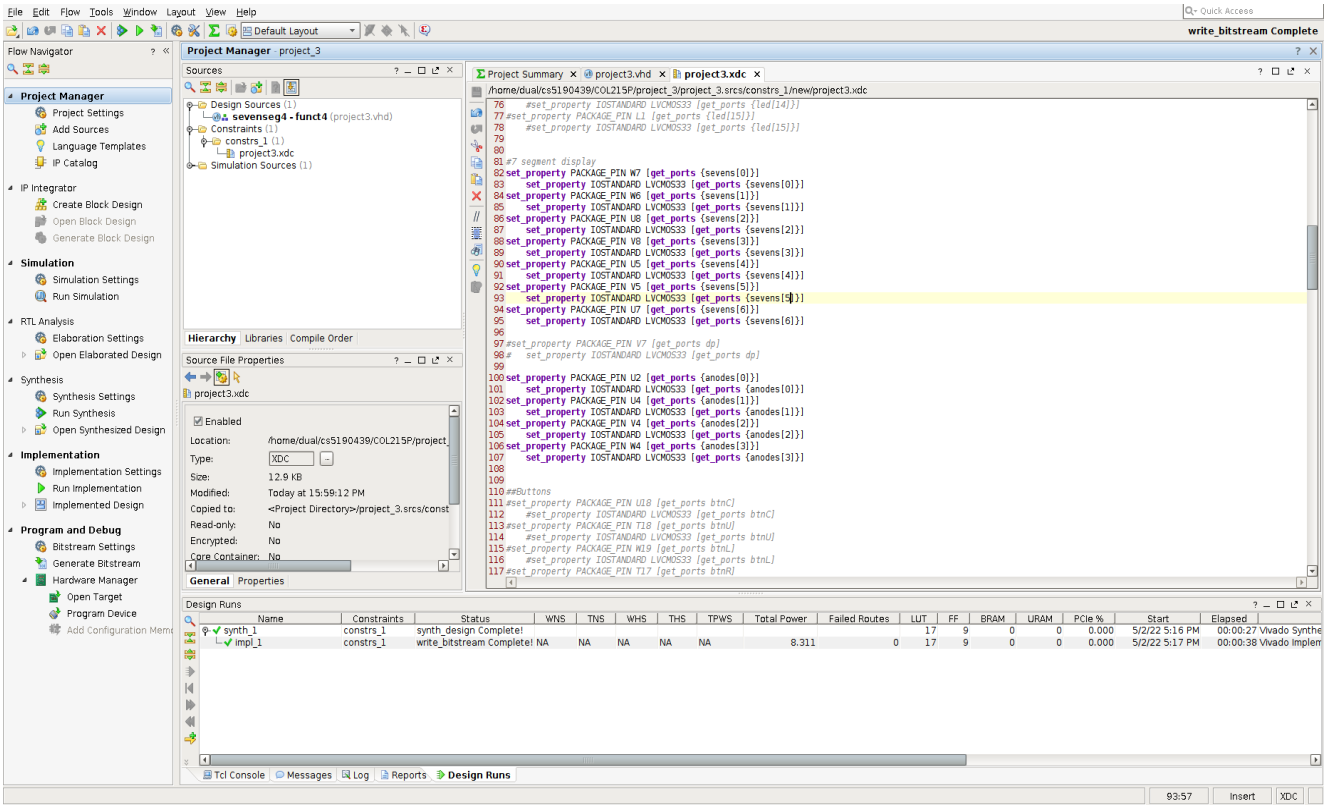
We are able to display 4 digits ,by activating one of anode ,and putting corresponding seven segment cathode values,then switching at refresh period/4

For it ,in our code we take counter of length 20,for refresh period of 10.5 ms and for above selecting logic ,took 2 msb bits of counter vector.

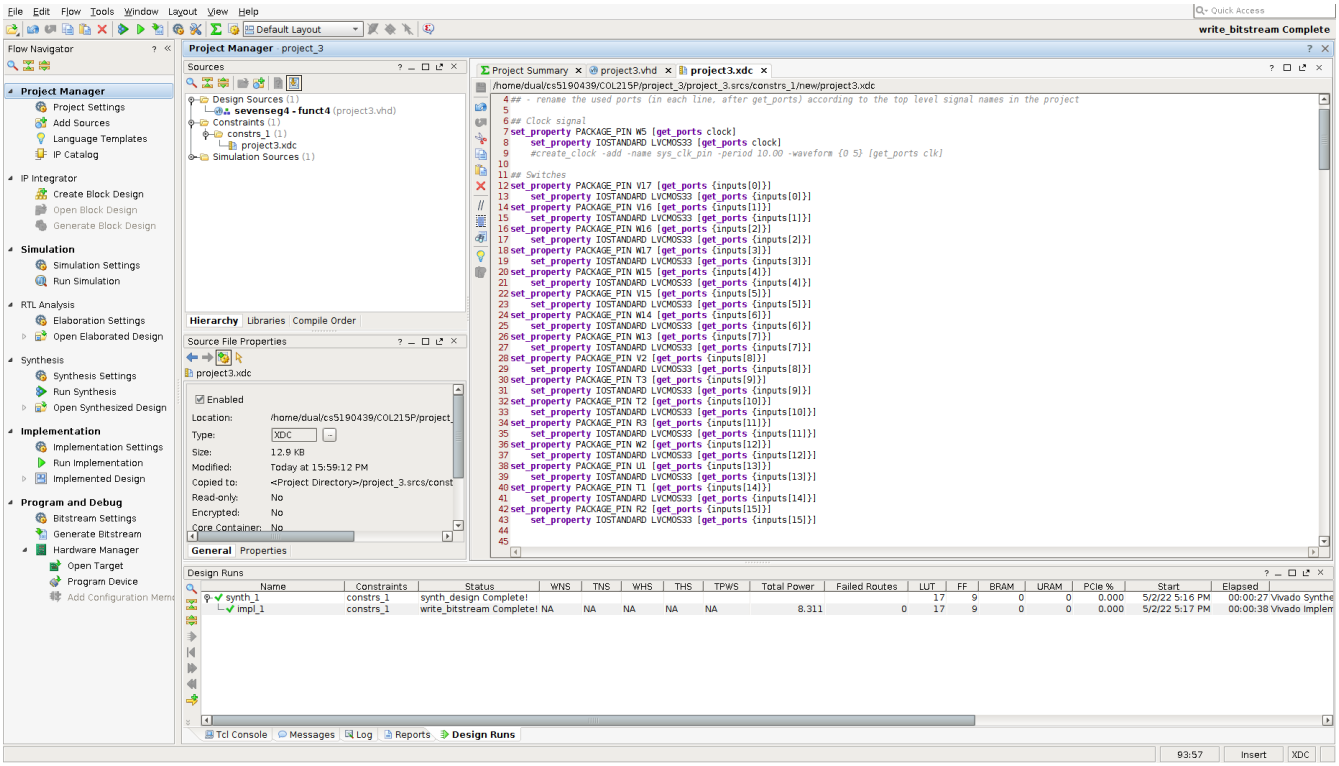


Constraint file

Anodes and cathodes matching-

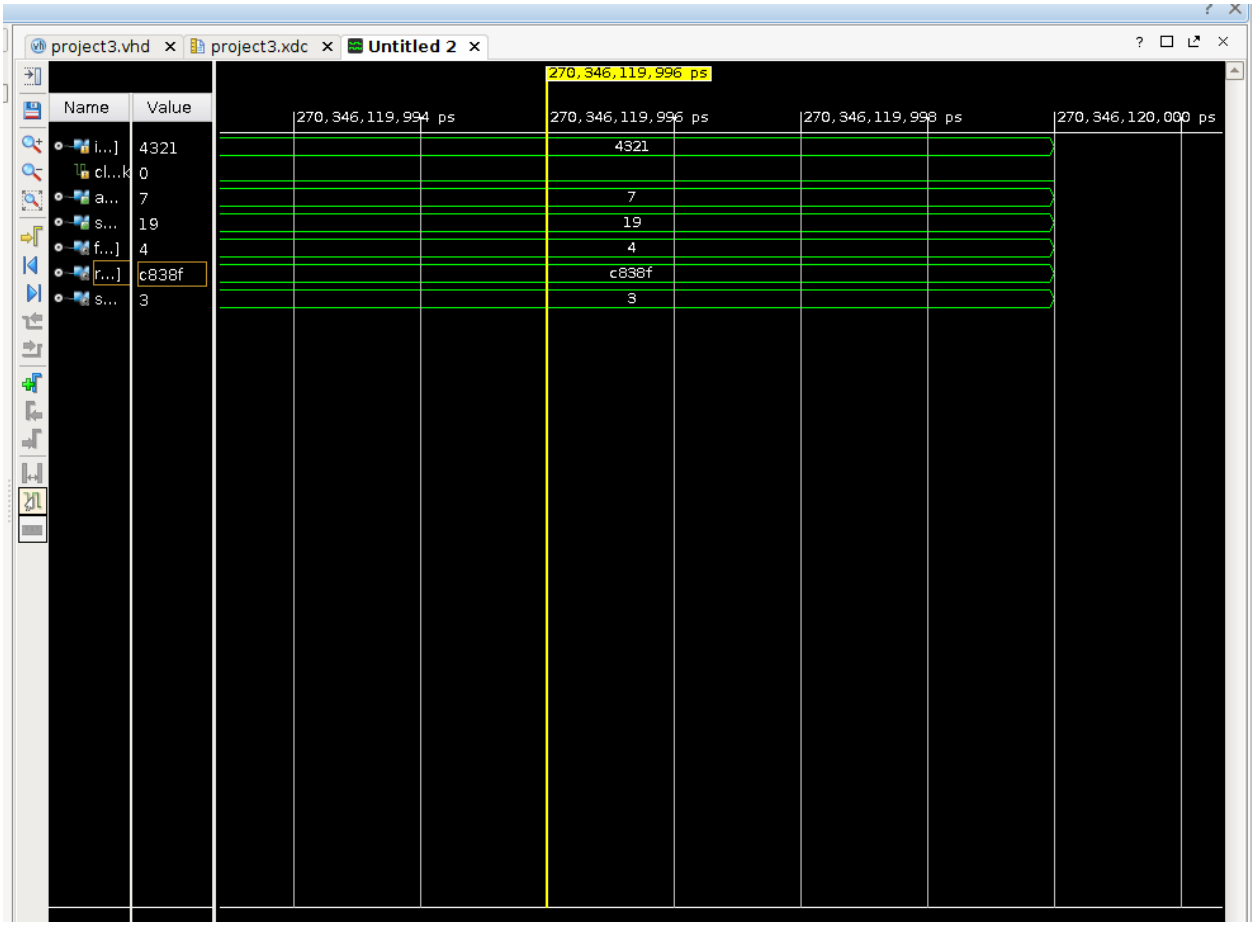


Used 16 switches to give decimal/hexadecimal input to BASYS 3 board-



Simulation of design on Vivado-

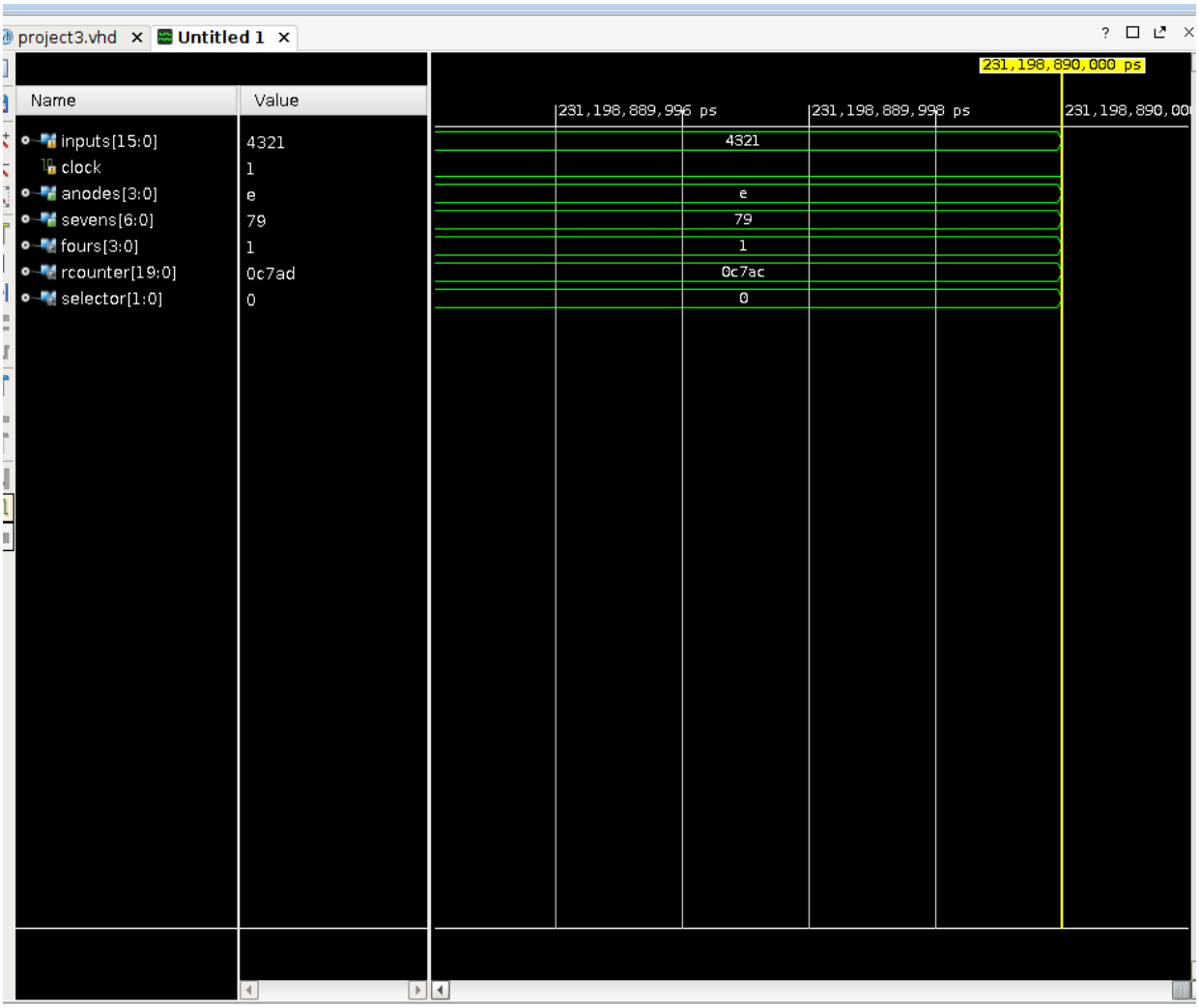
Simulated our design by changing values of signal inputs (below simulated WAVE results)-

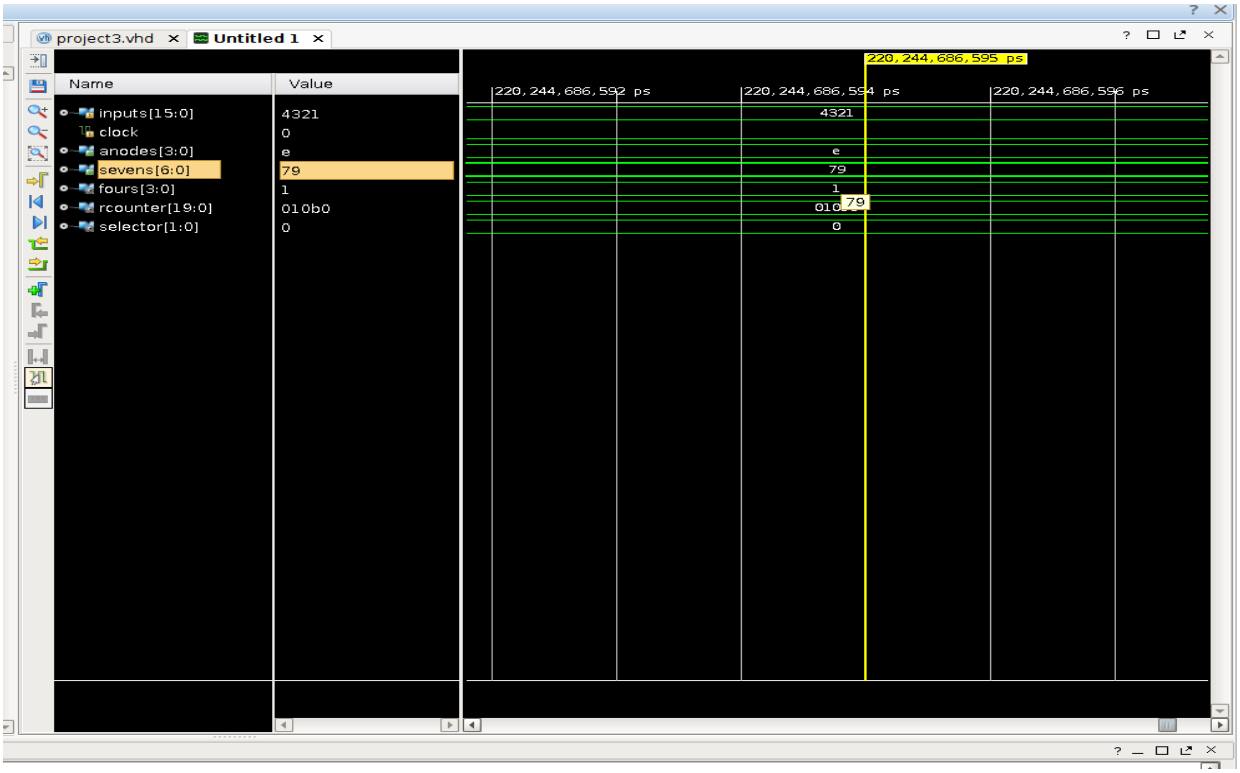


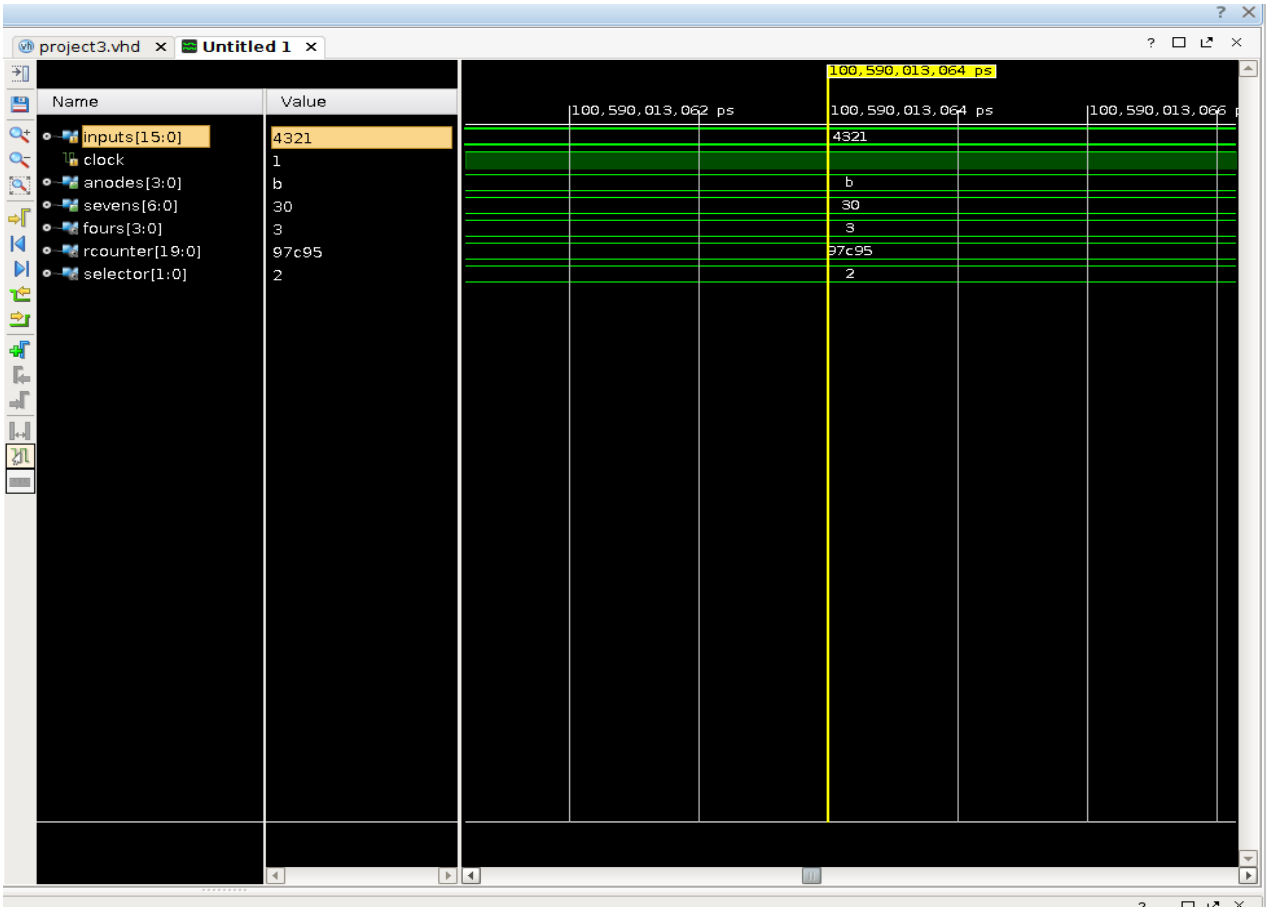
Let understand simulation example ,here in above ,inputs =X”4321”

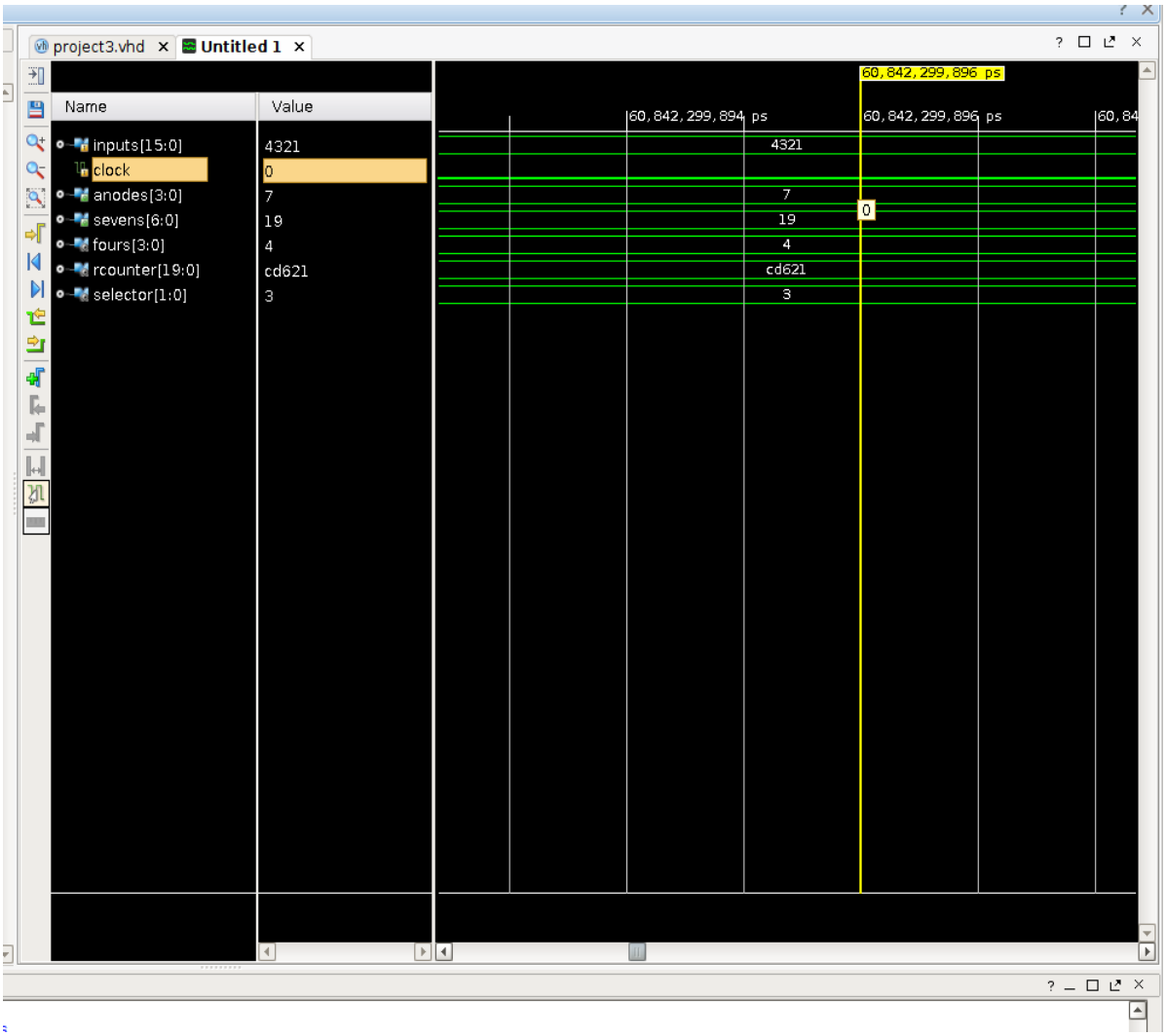
Anodes=”0111” and fours =x”4” as value of rcounter =X”C838F” which help in choosing these value as selector =”11”

Similarly below examples can be understood in this way.


project3.vhd
Untitled 1
Name
Value
inputs[15:0]
4321
clock
1
anodes[3:0]
e
sevens[6:0]
79
fours[3:0]
1
rcounter[19:0]
0c7ad
selector[1:0]
0
231,198,890,000 ps
231,198,889,996 ps
231,198,889,998 ps
231,198,890,00
4321
e
79
1
0c7ac
0


project3.vhd
Untitled 1
Name
Value
inputs[15:0]
clock
anodes[3:0]
sevens[6:0]
fours[3:0]
rcounter[19:0]
selector[1:0]
4321
0
e
79
1
010b0
0
220,244,686,595 ps
220,244,686,592 ps
220,244,686,594 ps
220,244,686,596 ps


project3.vhd
Untitled 1
Name
Value
inputs[15:0]
clock
anodes[3:0]
sevens[6:0]
fours[3:0]
rcounter[19:0]
selector[1:0]
4321
1
b
30
3
97c95
2
100,590,013,064 ps
100,590,013,062 ps
100,590,013,064 ps

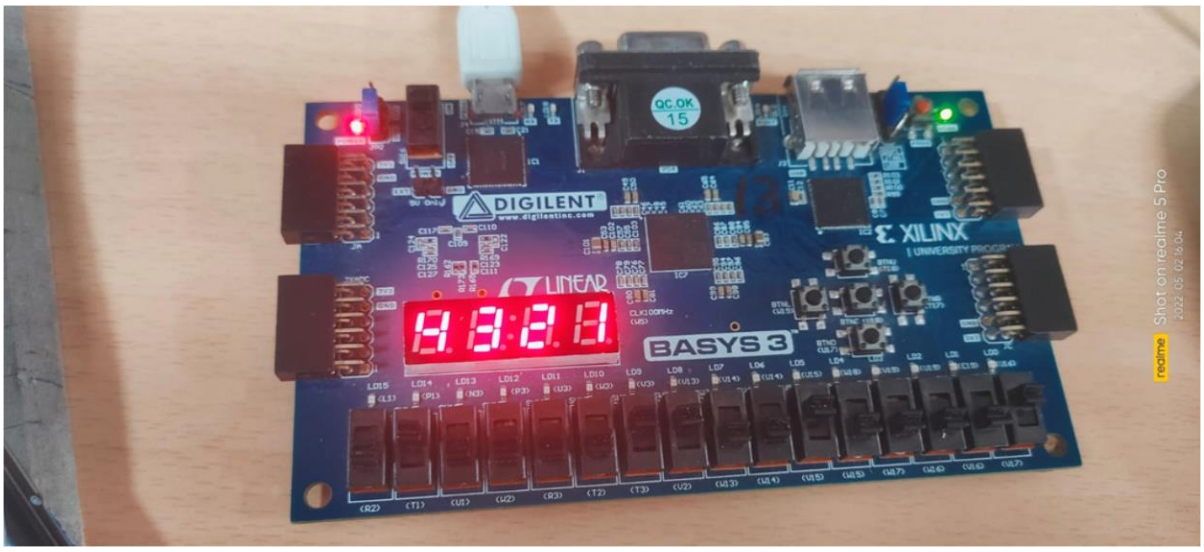


These simulation pics are taken by snapshots at different interval while running clock

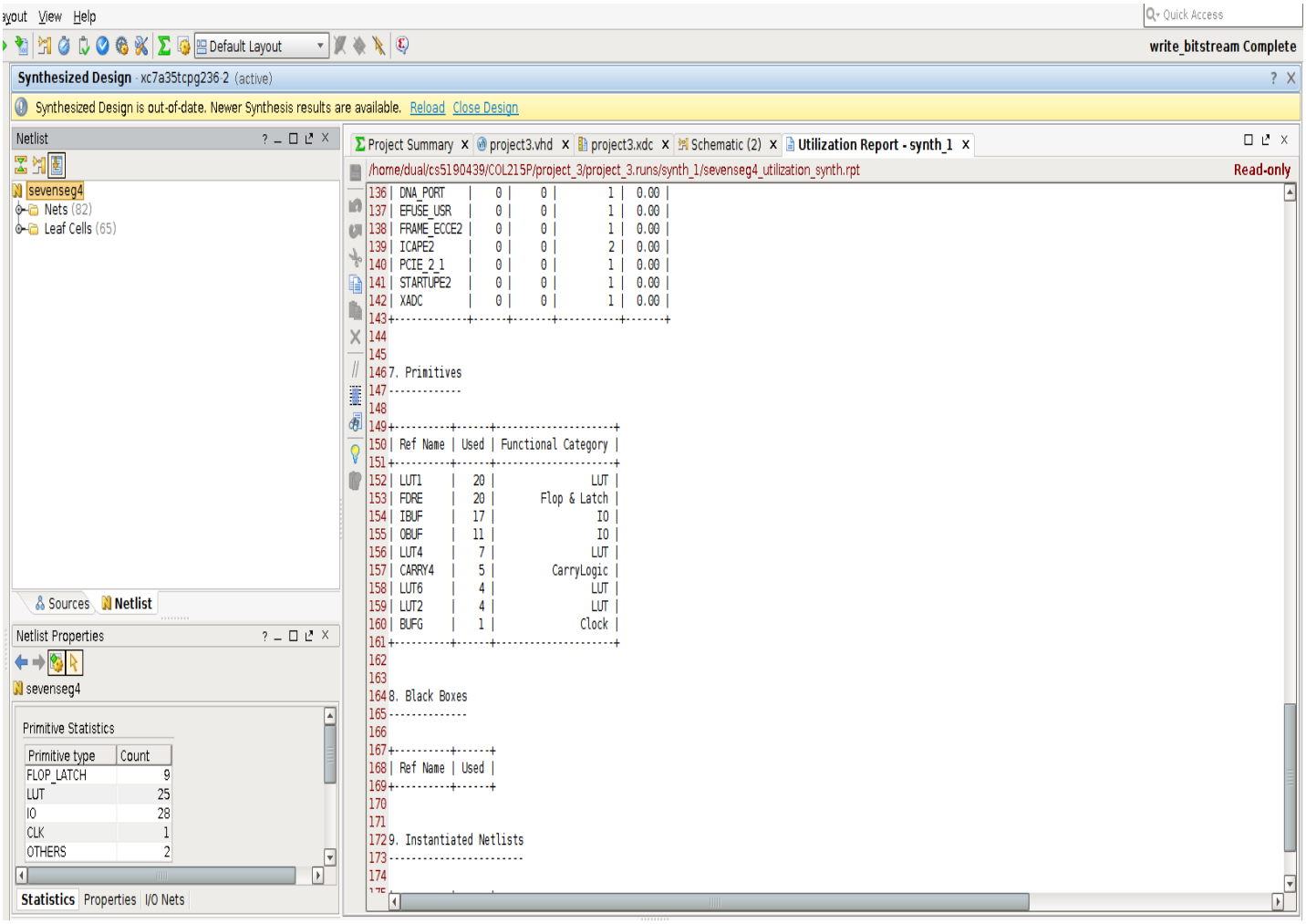
After doing above steps or till simulation work,then for implementing design on basys board, we first synthesized design, ran the implementation ,then generated Bitstream and finally opened the hardware manager to program device.

Testing on FPGA, Basys 3 board –

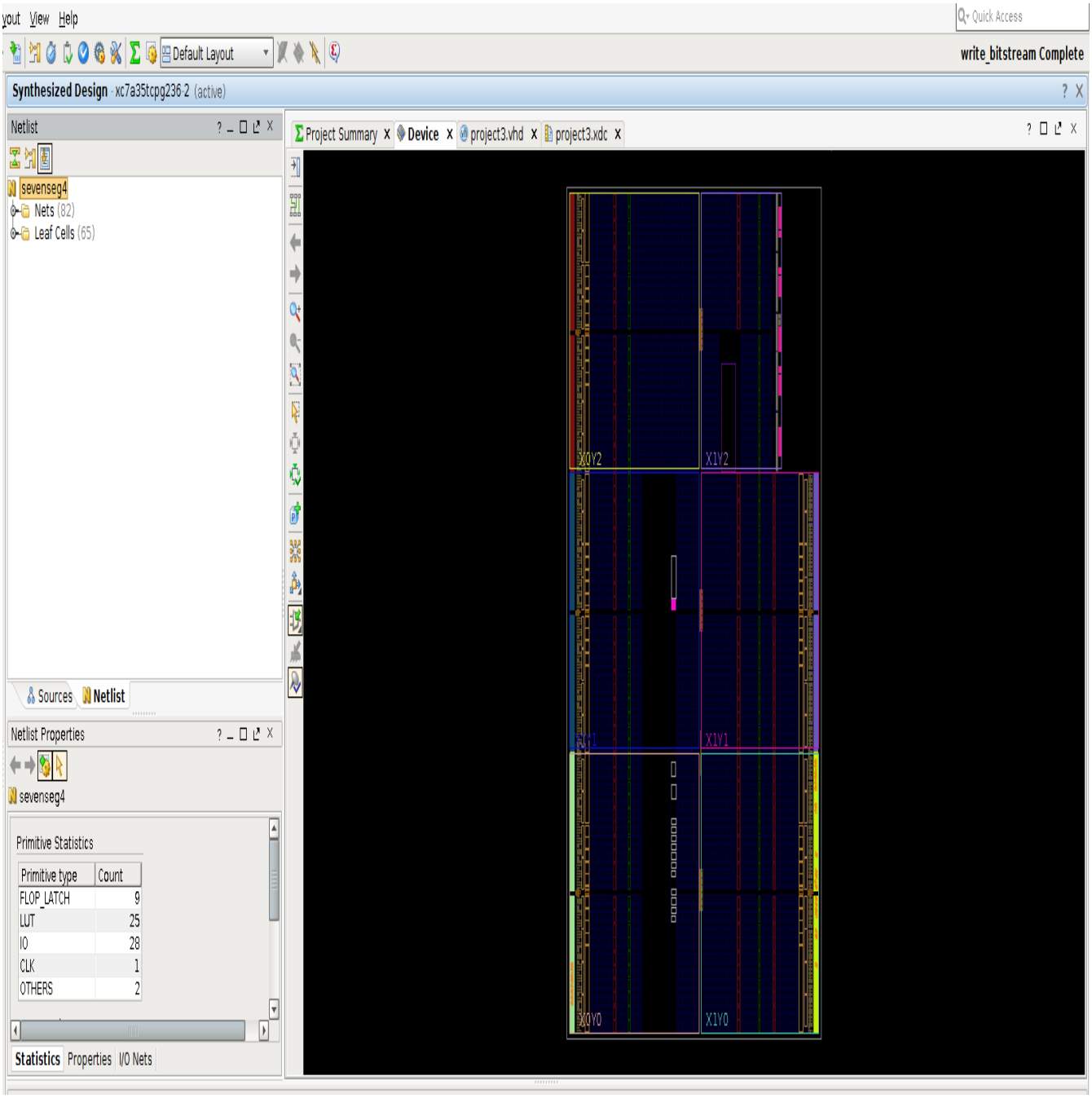
We have displayed the pattern 4321 by giving the input 0100001100100001



Resources utilization-

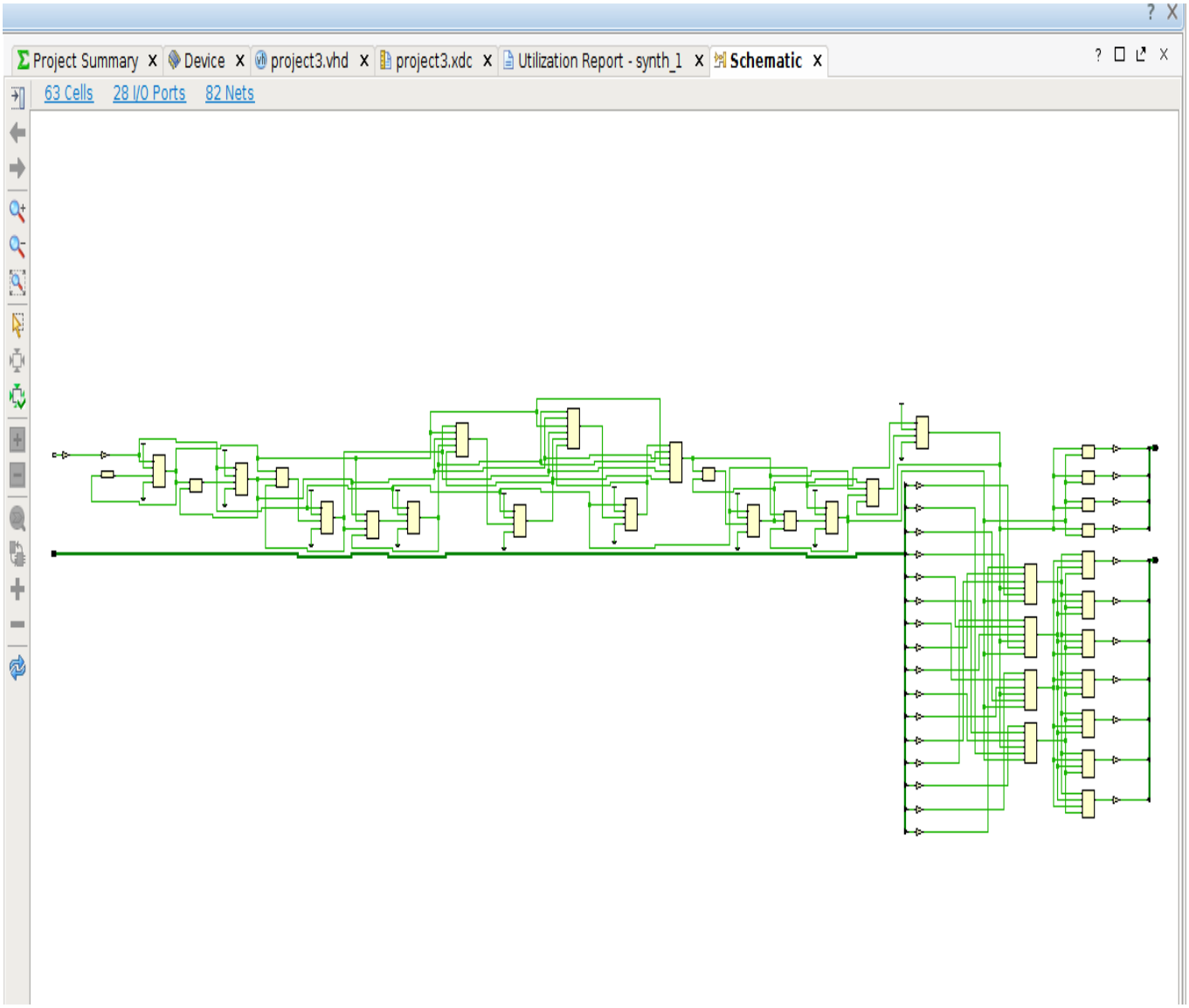


Device view-


Default Layout
write_bitstream Complete
Synthesized Design - xc7a35tcpg236-2 (active)
Netlist
sevenseg4
Nets (82)
Leaf Cells (65)
Project Summary
Device
project3.vhd
project3.xdc
X0Y2
X1Y2
X0Y1
X1Y1
X0Y0
X1Y0
Sources
Netlist
Netlist Properties
sevenseg4
Primitive Statistics
Primitive type
Count
FLOP_LATCH 9
LUT 25
IO 28
CLK 1
OTHERS 2
Statistics
Properties
I/O Nets

SCHEMETIC VIEW-

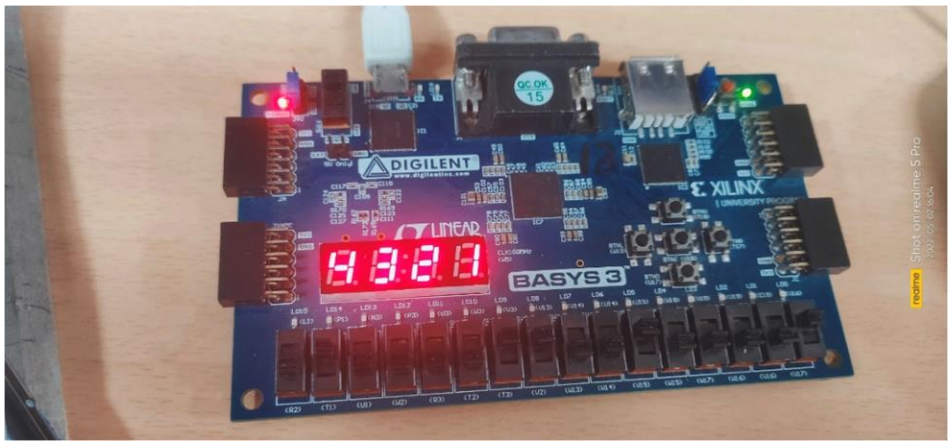
Here is the circuit for 4digit seven segment multiple display ,refresh period-10.5ms.



Below is time taking hardwork for finding refresh rate range by testing on board-

For below procedure,images decription is above and its image below…

For refresh period of 10.5 sec,Rcounter size is 20 bit(Submitted code)-



Below is generalization of attempt for calculating refresh rate range,let—

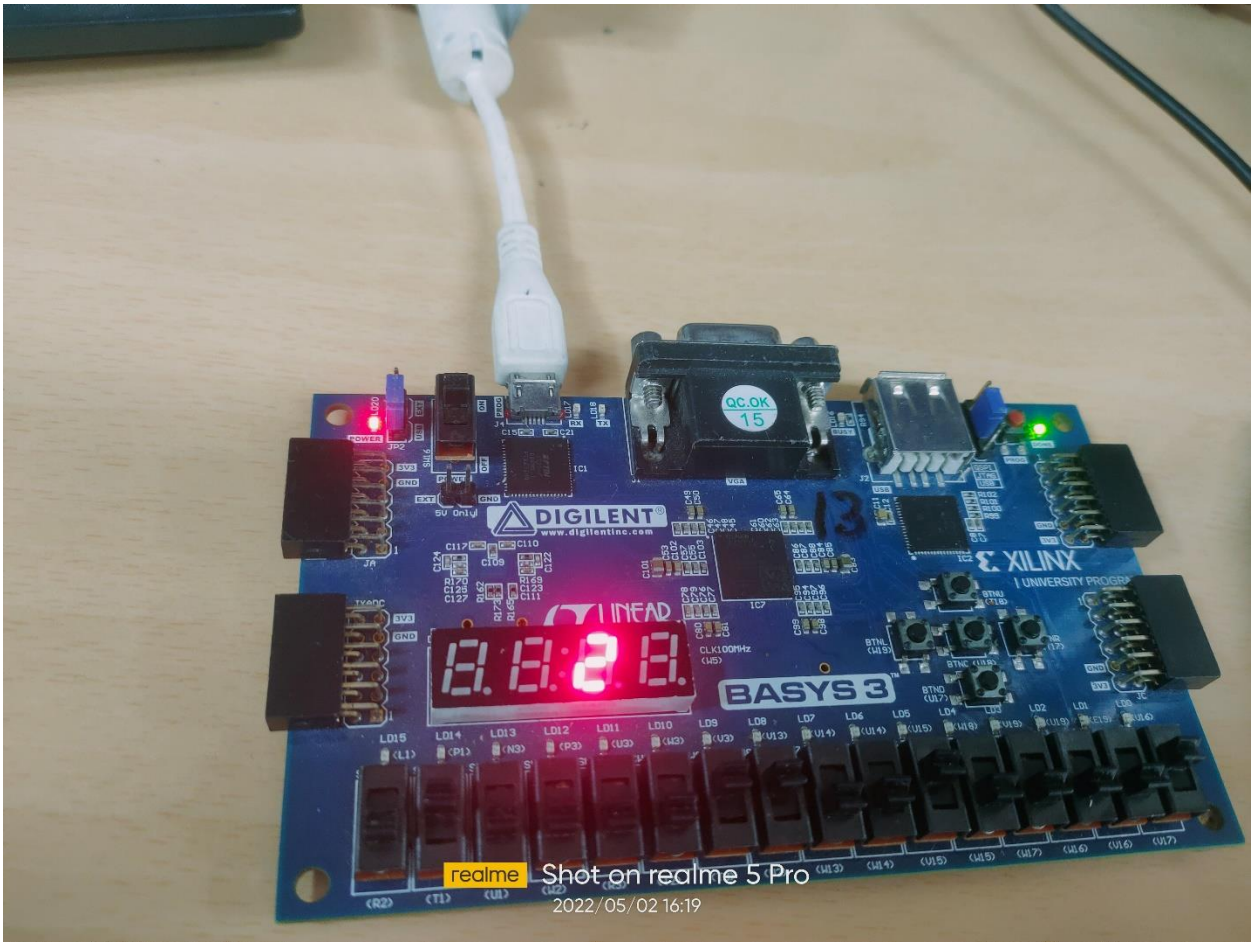
rcounter length – nbits

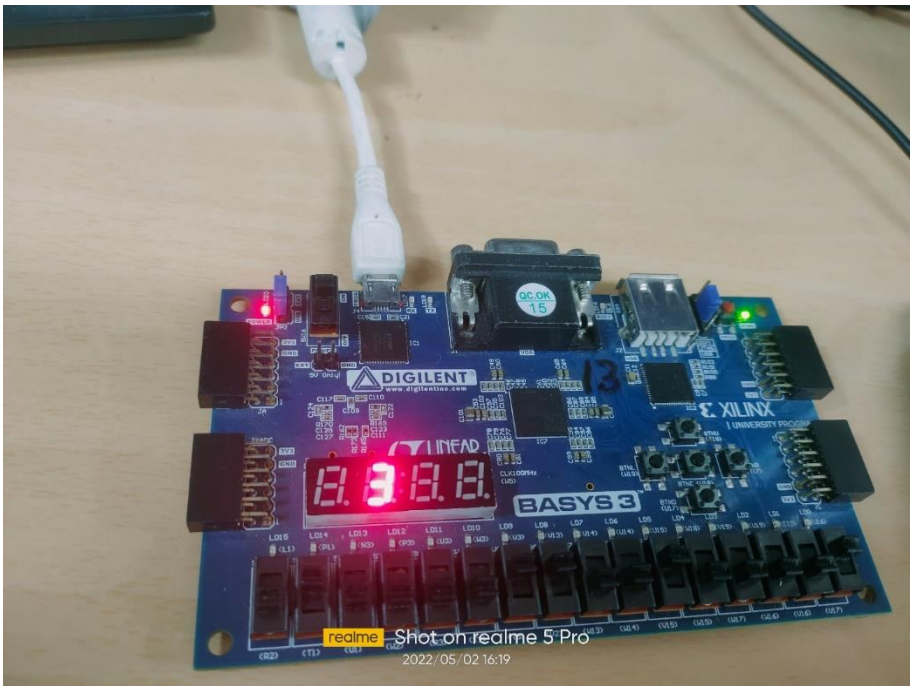
refresh period = 2^n /10^8 sec(as clock 100 Mhz)

So we found, refresh rate range for fine display- 0.01ms -20.9 ms

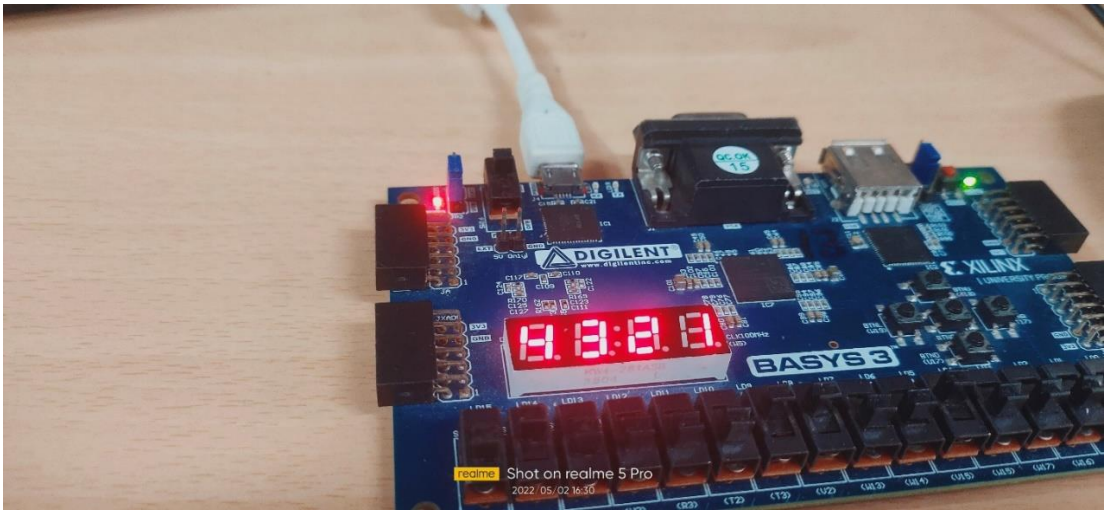
Below,rcounter length -26…

Changes seeing by eye..like rotating

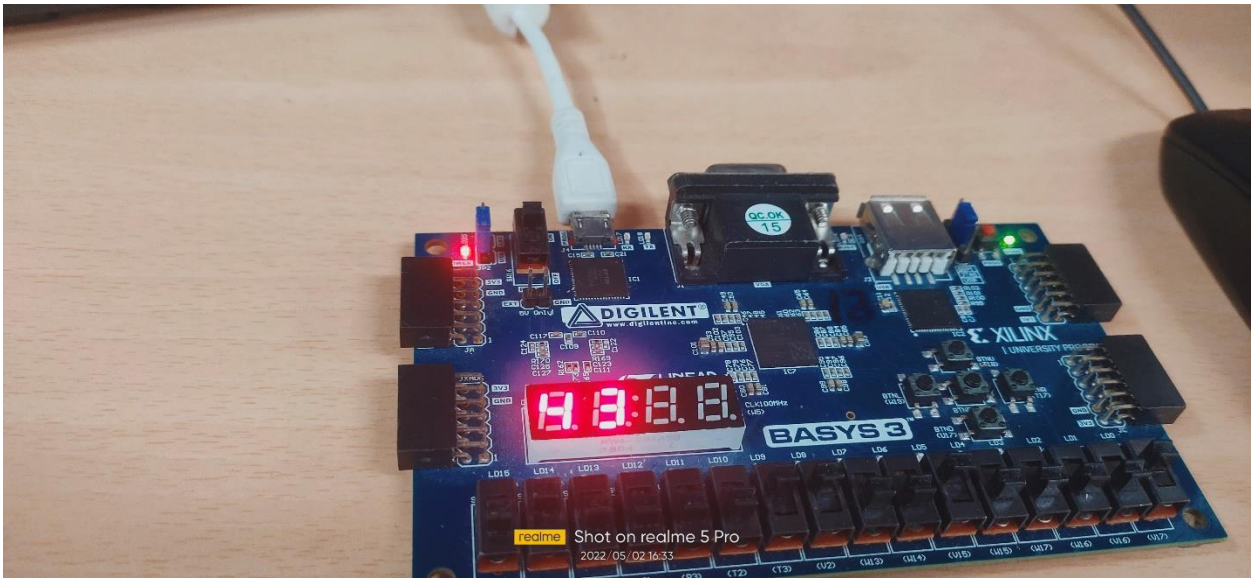


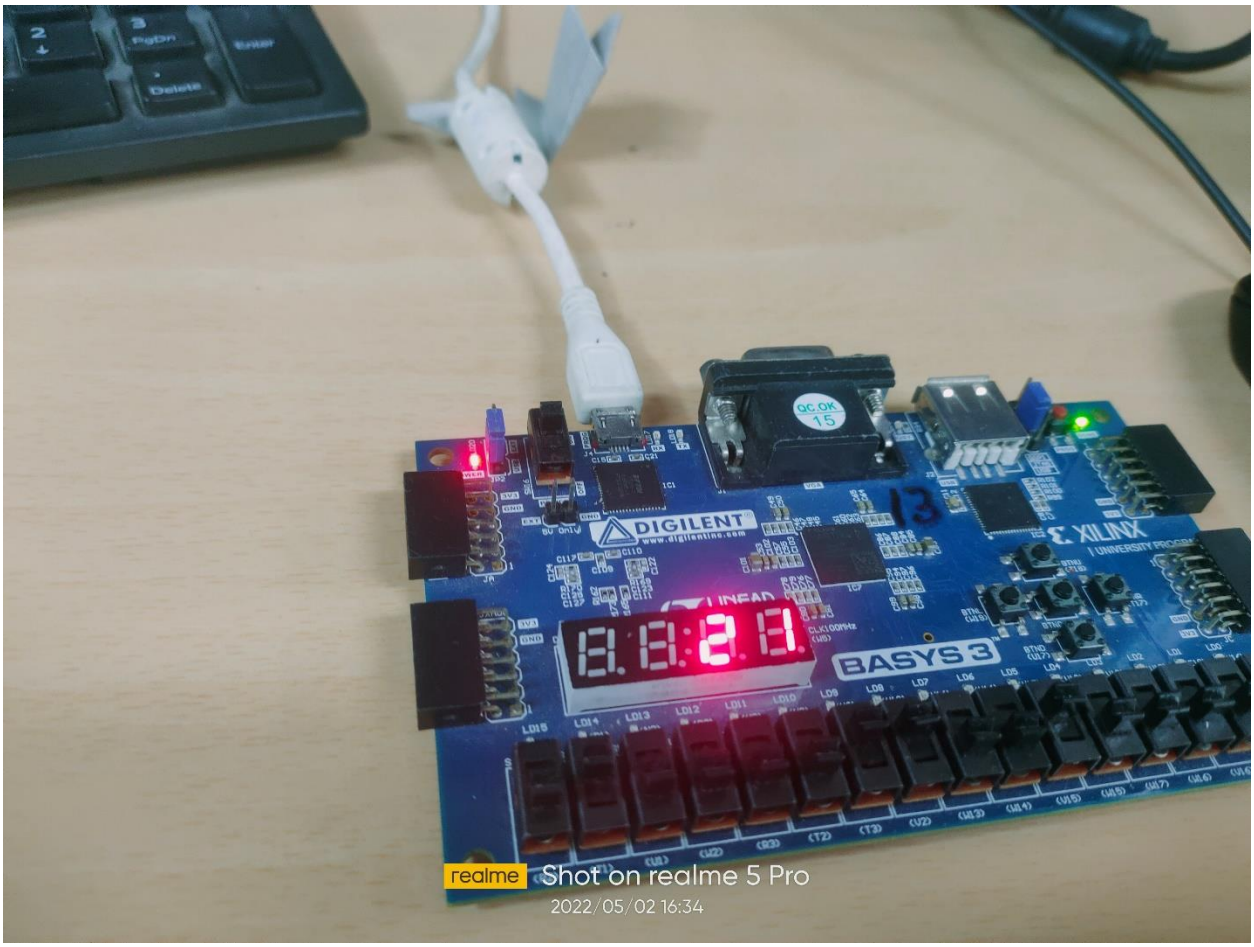


Rcounter length – 21 **(max period limit)**

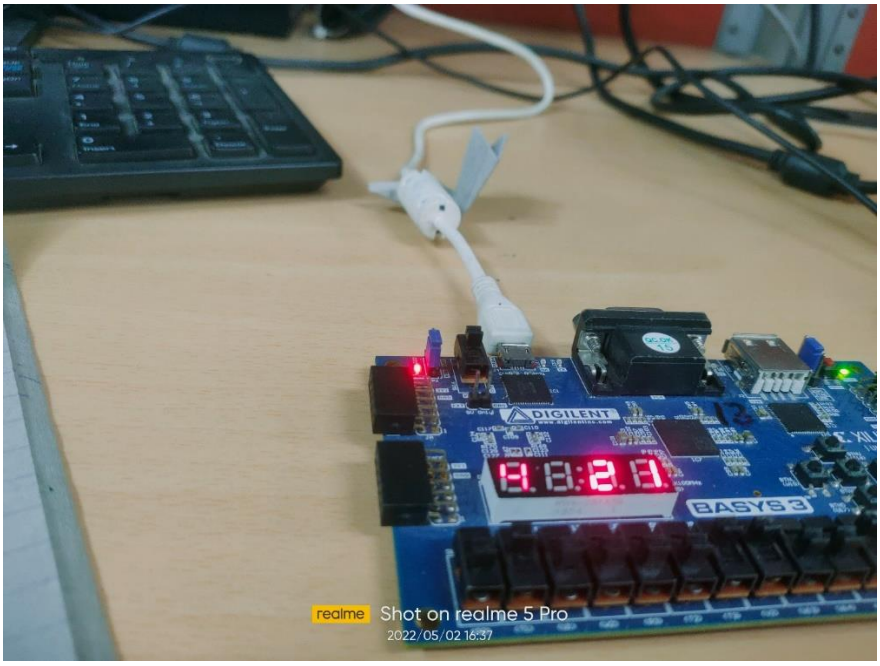


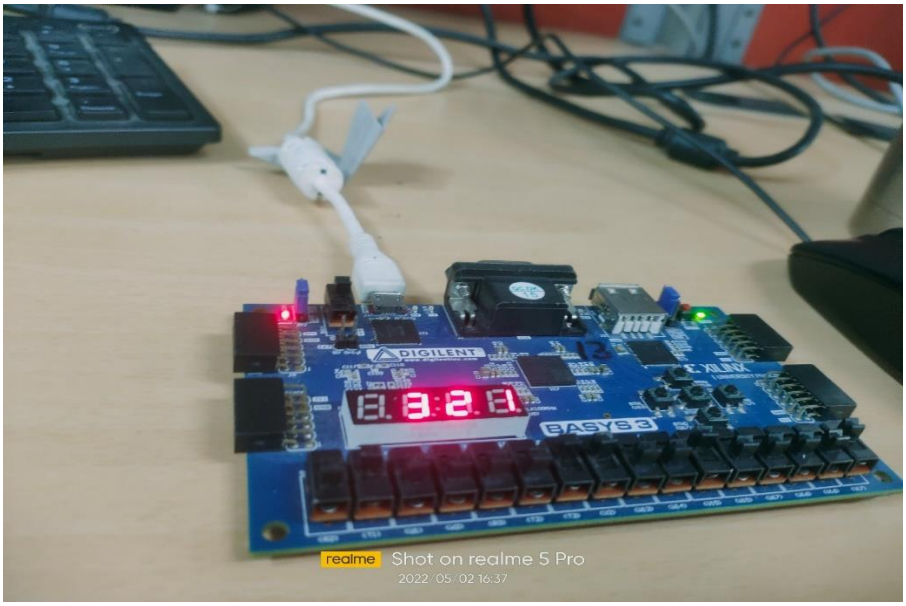
Rcounter length – 23



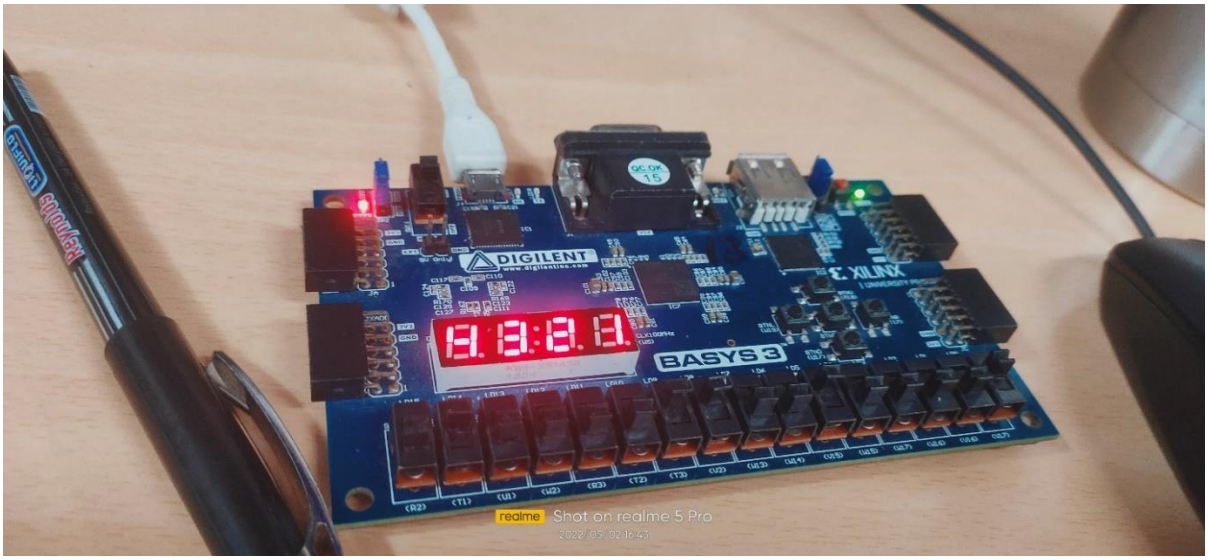


Rcounter length – 22

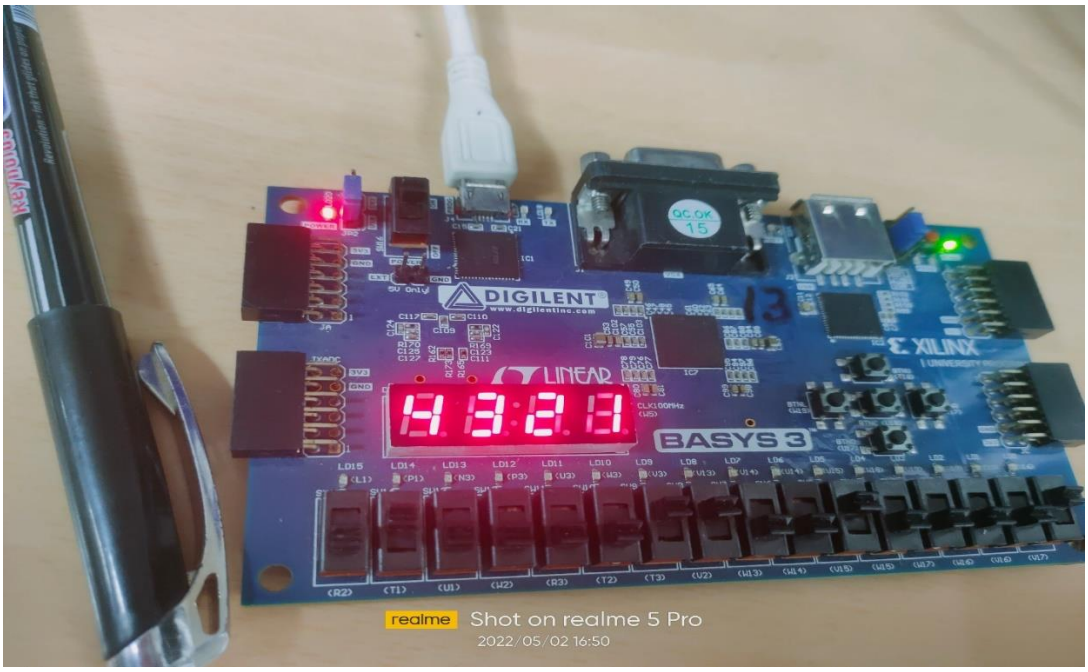


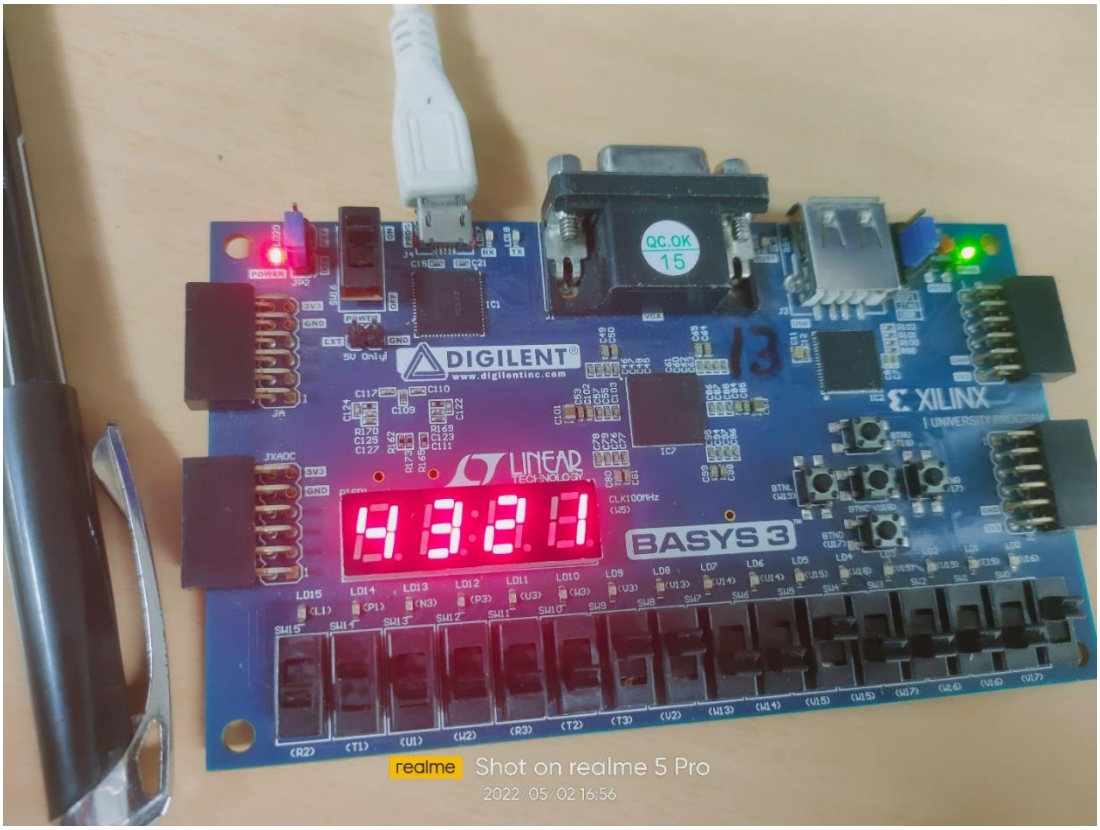


Rcounter length – 16

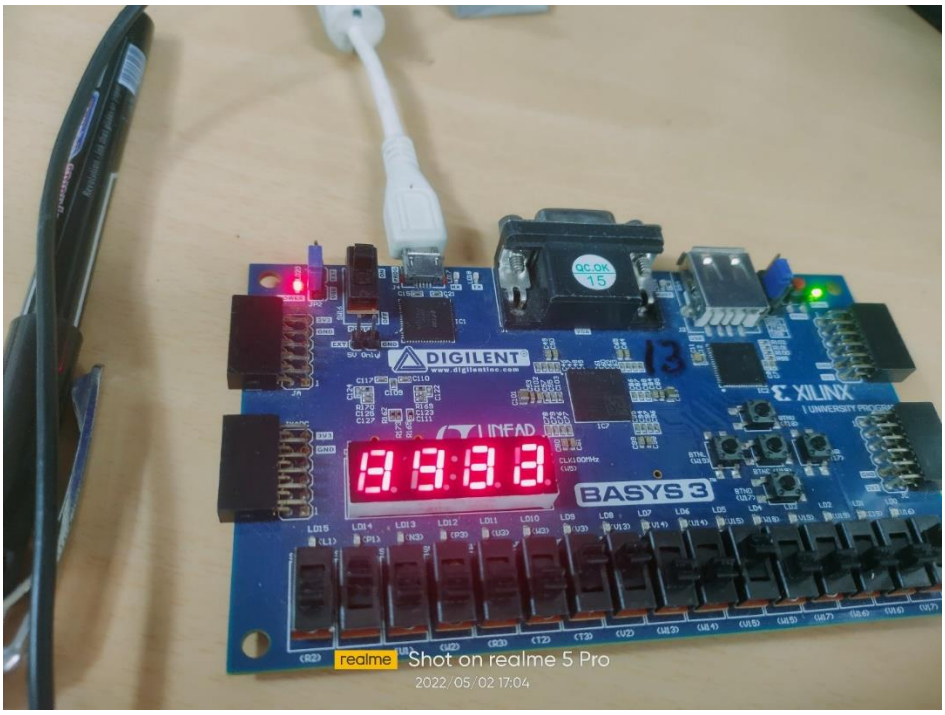


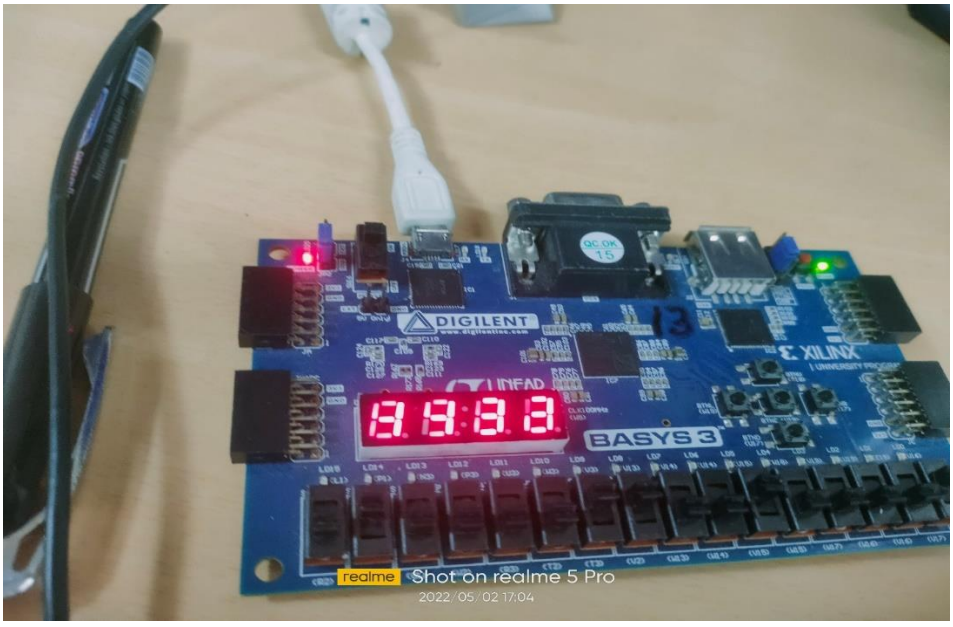
Rcounter length – 10(min limit)-Anshul Sir verified



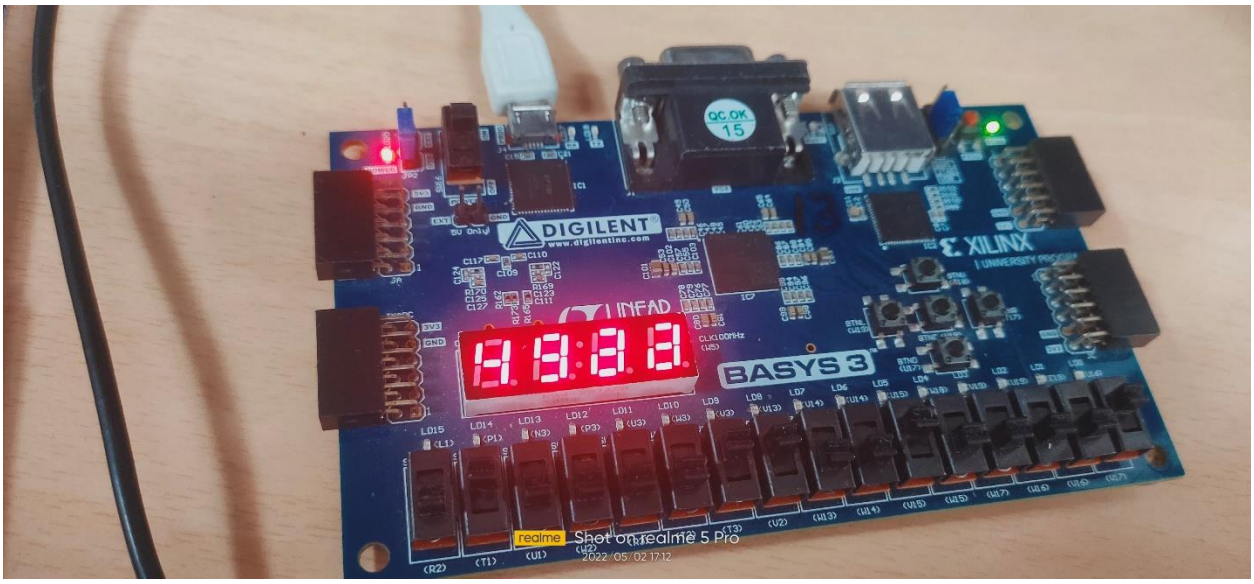


Rcounter length – 4

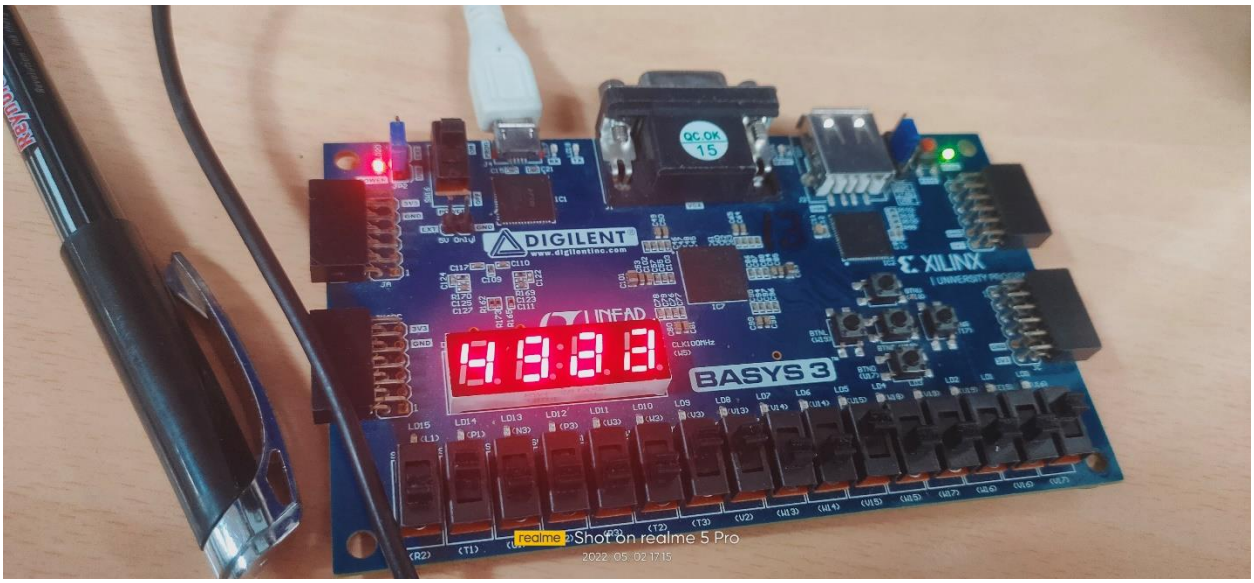




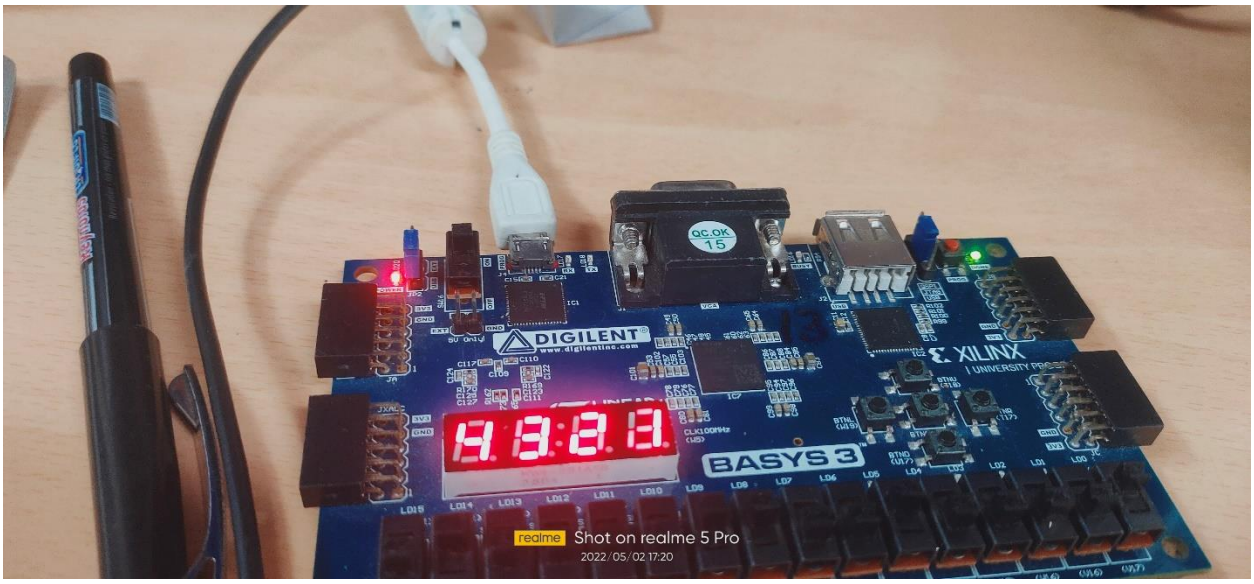
Rcounter length – 6



Rcounter length – 8



Rcounter length –9



Report became long due to adding this range part (but Anshul sir adviced us to do this method).

Thank you!