

ASSIGNMENT-3

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In this assignment we learned and designed to display multiple decimal/hexadecimal digits using 7-segment displays. Here we designed general module of quadruple seven segment display.

Submission folder (2019CS50439_2019CS50434) contains -

project3.xdc - constraint file

project3_a2.vhd -vhdl code file

sevensseg.bit - bitstream file

A3_report.pdf- report file

Some details of main steps involved in Assignment3 and related lab work are in next pages -

For Assignment3, we first designed and simulated on EDA Playground before lab-

EDA PLAYGROUND Code and simulation-

EDA playground

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testbench.vhd

```

1  -- Testbench
2  library IEEE;
3  use IEEE.std_logic_1164.all;
4
5  entity testbench is
6  -- empty
7  end testbench;
8
9  architecture tb of testbench is
10
11  -- DUT component
12  component sevenseg4 is
13  port(
14    inputs: in std_logic_vector(15 downto 0);
15    clock, reset : in std_logic; --clock 100Mhz
16    anodes: out std_logic_vector(3 downto 0);
17    sevens: out std_logic_vector(6 downto 0)
18  );
19  end component;
20
21  signal anod : std_logic_vector(3 downto 0);
22  signal inpt : std_logic_vector(15 downto 0) := X"4321";
23  signal clk : std_logic := '0';

```

design.vhd

```

32  elsif rising_edge(clock) then
33    rcounter <= rcounter + X"1";
34  end if;
35  end process;
36
37  --refresh period of 10.5ms
38  selector <= rcounter (19 downto 18);-- select signal in below
39  multiplexing logic
40
41  --multiplexer for selecting current displaying seven segment
42  display and its 4 bits of a displaying digit
43  process(selector)
44  begin
45    case selector is
46      when "00" =>
47        anodes <= "1110";
48        fours <= inputs(3 downto 0);
49      when "01" =>
50        anodes <= "1101";
51        fours <= inputs(7 downto 4);
52      when "10" =>
53        anodes <= "1011";

```

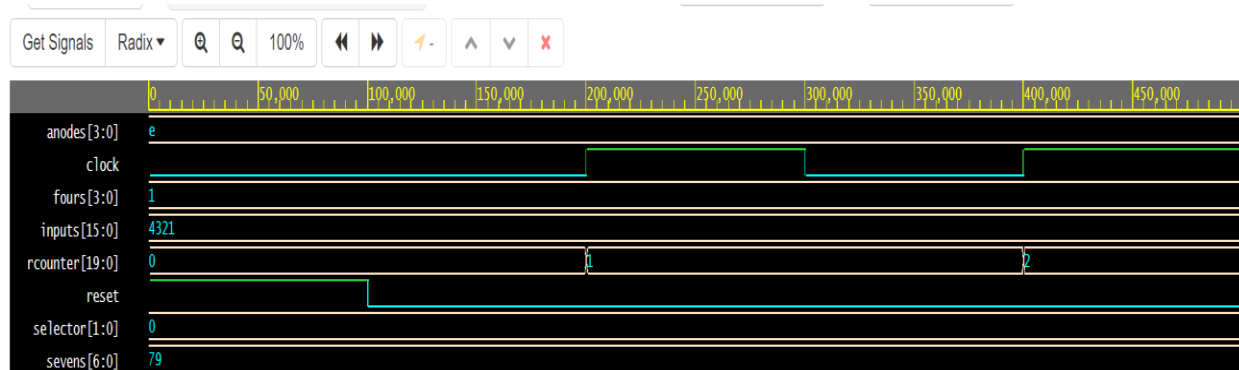
Log Share

seven segment4 -A3 0 views and 0 likes Private (only you can view) Save

B I H

Designed and implemented a circuit that takes a 4 decimal/hexadecimal digit encoded using 4 bits and produces 7-bit output for seven segment displays of BASYS3 FPGA board.

EDA PLAYGROUND EPWAVE



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In EDAPLAYGROUND ,simulated designed code for Assignment-2,for it created separate testbench and then tested for different values of four signal

New project2 on Vivado-

File Edit Flow Tools Window Layout View Help

write_bitstream Complete

Flow Navigator

Project Manager

Project Settings

Add Sources

Language Templates

IP Catalog

IP Integrator

Create Block Design

Open Block Design

Generate Block Design

Simulation

Simulation Settings

Run Simulation

RTL Analysis

Elaboration Settings

Open Elaborated Design

Synthesis

Synthesis Settings

Run Synthesis

Open Synthesized Design

Implementation

Implementation Settings

Run Implementation

Implemented Design

Program and Debug

Bitstream Settings

Generate Bitstream

Hardware Manager

Open Target

Program Device

Add Configuration Memory

Project Manager - project_3

Sources

Design Sources (1)

sevensseg4 - funct4 (project3.vhd)

Constraints (1)

constrs_1 (1)

project3.xdc

Simulation Sources (1)

Hierarchy

Libraries

Compile Order

Source File Properties

project3.xdc

Enabled

Location: /home/dual/cs5190439/COL215P/project3

Type: XDC

Size: 12.9 KB

Modified: Today at 15:59:12 PM

Copied to: <Project Directory>/project_3.srcs/constrs_1

Read-only: No

Encrypted: No

Core Container: No

General

Properties

Project Summary

Project Settings

Project name: project_3

Project location: /home/dual/cs5190439/COL215P/project_3

Product family: Artix-7

Project part: xc7a35tcbg236-2

Top module name: sevensseg4

Target language: VHDL

Simulator language: Mixed

Synthesis

Status: Complete

Messages: 1 warning

Part: xc7a35tcbg236-2

Strategy: Vivado Synthesis Defaults

Implementation

Status: Complete

Messages: 3 warnings

Part: xc7a35tcbg236-2

Strategy: Vivado Implementation Defaults

Incremental compile: None

Summary Route Status

DRC Violations

Summary: 1 warning

Implemented DRC Report

Timing

Worst Negative Slack (WNS): NA

Total Negative Slack (TNS): NA

Number of Failing Endpoints: NA

Total Number of Endpoints: NA

Implemented Timing Report

Setup Hold Pulse Width

Utilization - Post-Implementation

LUT 1%

FF 1%

IO 26%

BUFG 3%

Power

Total On-Chip Power: 8.311 W

Junction Temperature: 66.6 °C

Thermal Margin: 18.4 °C (3.7 W)

Effective θJA: 5.0 °C/W

Power supplied to off-chip devices: 0 W

Design Runs

	Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAM	URAM	PCIE %	Start	Elapsed	
synth_1	synth_1	constrs_1	synth_design Complete!	NA	NA	NA	NA	NA	8.311	0	17	9	0	0	0.000	5/2/22 5:16 PM	00:00:27	Vivado Synthesis
impl_1	impl_1	constrs_1	write_bitstream Complete!	NA	NA	NA	NA	NA	8.311	0	17	9	0	0	0.000	5/2/22 5:17 PM	00:00:38	Vivado Implementation

Tcl Console

Messages

Log

Reports

Design Runs

VHDL code on Vivado -

```
Project Summary x project3.vhd x project3.xdc x Schematic (2) x Utilization Report - synth_1 x
/home/dual/cs5190439/COL215P/project_3/project_3.srcs/sources_1/new/project3.vhd

17 -- Additional Comments:
18 --
19 -----
20
21
22 --4 seven segment-A3
23
24 library IEEE;
25 use IEEE.std_logic_1164.all;
26 -- use IEEE.NUMERIC_STD.ALL;
27 use IEEE.STD_LOGIC_UNSIGNED.ALL;
28
29 entity sevenseg4 is
30 port(
31     inputs: in std_logic_vector(15 downto 0);
32     clock : in std_logic;    --clock 100Mhz
33     --, reset
34     anodes: out std_logic_vector(3 downto 0);
35     sevens: out std_logic_vector(6 downto 0)
36 );
37 end sevenseg4;
38
39 -- architecture
40 architecture funct4 of sevenseg4 is
41     signal fours : std_logic_vector(3 downto 0); -- := "0000"
42     signal rcounter: std_logic_vector(19 downto 0) := (others => '0'); -- refresh counter
43     --for creating refresh period of 10.5ms
44     signal selector : std_logic_vector(1 downto 0);
45     begin
46
47     --refresh rate range most probably 1ms to 16ms
48
49     --for generating timing/refreshing signals
50     process(clock)
51     begin
52     -- if (reset = '1') then
53     --     rcounter <= (others => '0');
54     if rising_edge(clock) then
55         rcounter <= rcounter + X"1";
56     end if;
57 end process;
```

```
Project Summary x project3.vhd x project3.xdc x
/home/dual/cs5190439/COL215P/project_3/project_3.srcs/sources_1/new/project3.vhd

65 begin
66     case selector is
67     when "00" =>
68         anodes <= "1110";
69         fours <= inputs(3 downto 0);
70     when "01" =>
71         anodes <= "1101";
72         fours <= inputs(7 downto 4);
73     when "10" =>
74         anodes <= "1011";
75         fours <= inputs(11 downto 8);
76     when "11" =>
77         anodes <= "0111";
78         fours <= inputs(15 downto 12);
79     when others => null;
80     end case;
81 end process;
82
83
84
85 -- seven segment display
86 with fours select sevens <=
87     "1000000" when "0000", --0
88     "1111001" when "0001", --1
89     "0100100" when "0010", --2
90     "0110000" when "0011", --3
91     "0011001" when "0100", --4
92     "0010010" when "0101", --5
93     "0000010" when "0110", --6
94     "1111000" when "0111", --7
95     "0000000" when "1000", --8
96     "0010000" when "1001", --9
97     "0100000" when "1010", --A
98     "0000011" when "1011", --b
99     "1000110" when "1100", --C
100    "0100001" when "1101", --d
101    "0000110" when "1110", --E
102    "0001110" when "1111", --F
103    "1111111" when others;
104
105 end funct4;
106
```

The code is also provided in the submission file

DESCRIPTION

Here we assumed normal indexing of segments of seven segment display(B-2,etc)

Here the code takes 16 bit input through the switches for the 4 LEDs (4 bits for each) and displays the respected digit.

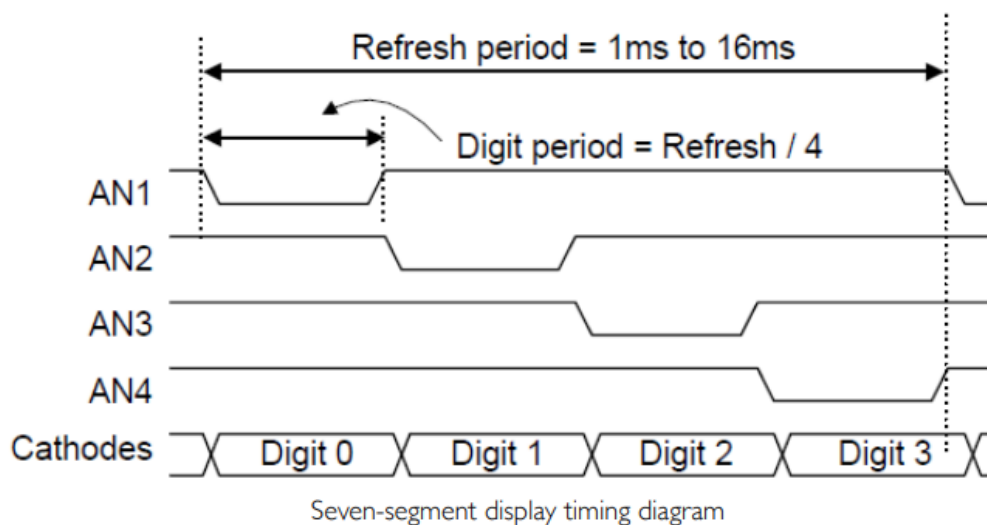
The refresh rate (the rate when every LED is switched to) is around 10ms.

Refreshing LEDs at this frequency gives us the perception that all LEDs are on at the same time,as this frequency around 95Hz (10.5 ms refresh period used in submitted code) which is greater than persistence vision of frequency - 25 Hz

Our eyes are able to percept proper displays for the refresh rate range of around 1ms – 16ms.

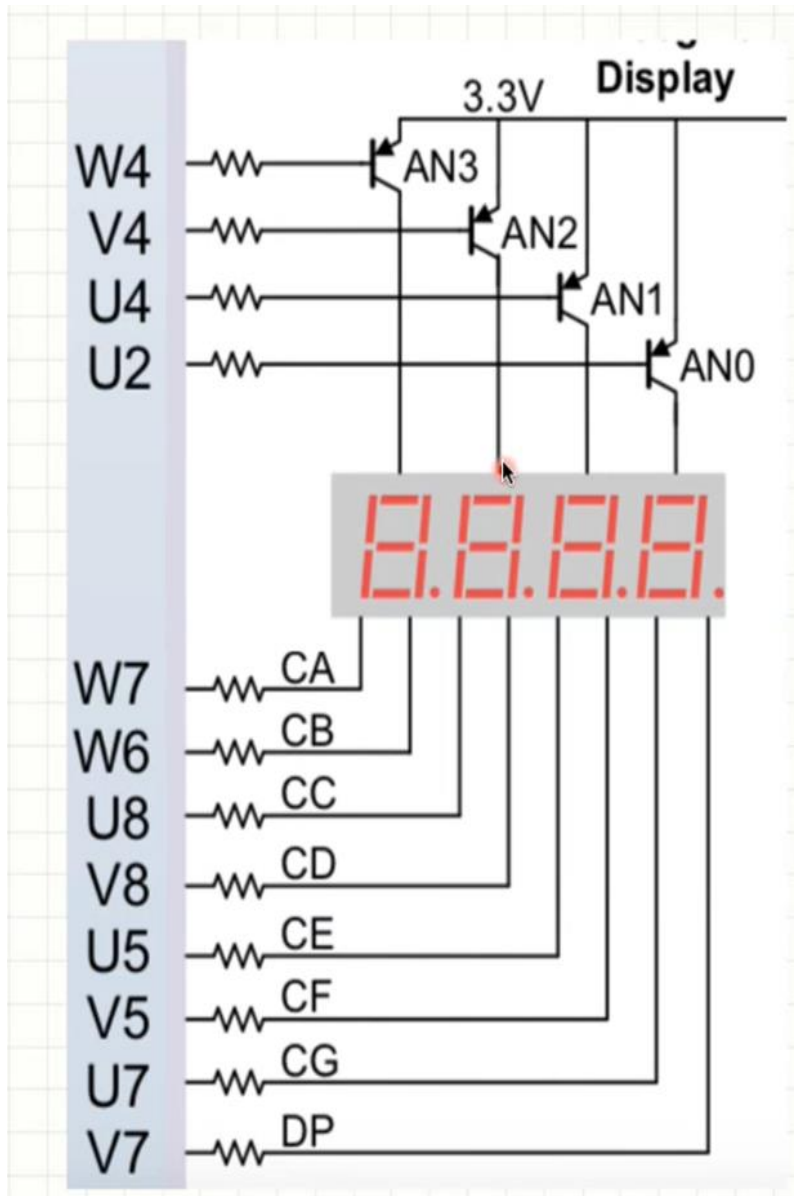
But at last we have also tested thoroughly to determine refresh rate range in our setup,found fine display refresh rate range, 0.01ms -20.9 ms.

Below is timing diagram for refreshing the 4-digit seven-segment display on Basys 3 FPGA-



We are able to display 4 digits ,by activating one of anode ,and putting corresponding seven segment cathode values,then switching at refresh period/4

For it ,in our code we take counter of length 20,for refresh period of 10.5 ms and for above selecting logic ,took 2 msb bits of counter vector.



Constraint file

Anodes and cathodes matching-

The screenshot displays the Xilinx Vivado IDE interface for a project named 'project_3'. The left sidebar contains the Project Manager, which shows the project's structure. The central Sources window displays the 'project3.xdc' file, which contains constraints for the design. The bottom Design Runs window shows the results of the synthesis and implementation processes.

Design Runs Table:

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAM	URAM	PCIE %	Start	Elapsed
synth_1	constrs_1	synth_design Complete	NA	NA	NA	NA	NA	8.311	0	17	9	0	0	0.000	5/2/22 5:16 PM	00:00:27 Vivado Synthe
impl_1	constrs_1	write_bitstream Complete	NA	NA	NA	NA	NA	8.311	0	17	9	0	0	0.000	5/2/22 5:17 PM	00:00:38 Vivado Implem

Used 16 switches to give decimal/hexadecimal input to BASYS 3 board-

The screenshot displays the Xilinx Vivado IDE interface for a project named "project_3". The left sidebar shows the Project Manager with sections for Design Sources, Constraints, Simulation Sources, IP Integrator, RTL Analysis, Synthesis, Implementation, and Program and Debug. The main workspace is divided into several panels:

- Sources:** Shows the project hierarchy with Design Sources (1), Constraints (1), and Simulation Sources (1).
- Hierarchy:** Displays the source file properties for "project3.xdc", including location, size, modified date, and read-only status.
- Design Runs:** A table showing the status of various design runs.

The Design Runs table is as follows:

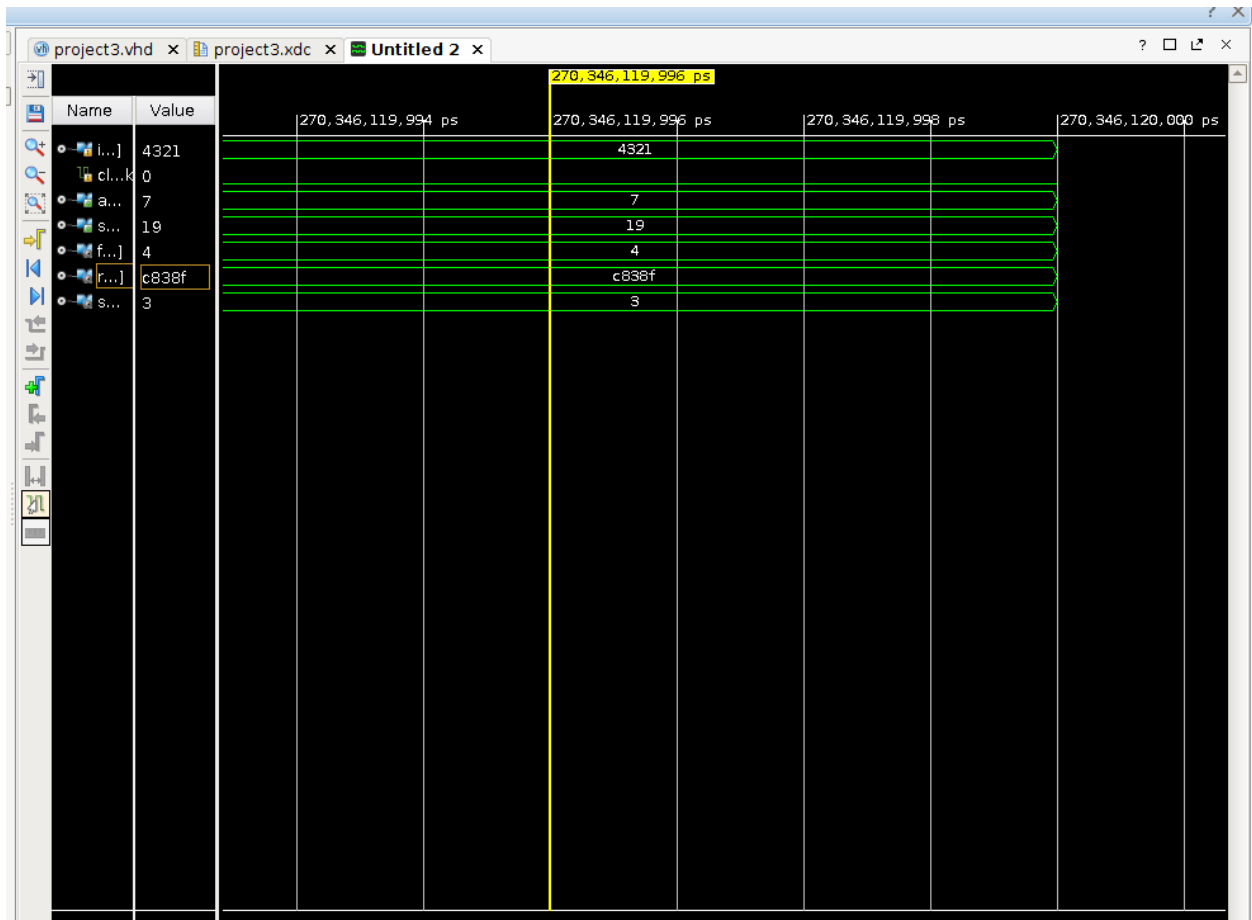
Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAM	URAM	PCle%	Start	Elapsed
synth_1	constrs_1	synth_design Complete!														
impl_1	constrs_1	write_bitstream Complete!	NA	NA	NA	NA	NA	8.311	0	17	9	0	0	0.000	5/2/22 5:16 PM	00:00:27 Vivado Synthe

The right pane shows the "project3.xdc" file content, which includes constraints for the clock signal and 16 switches. The constraints are defined as follows:

```
4## - rename the used ports (in each line, after get_ports) according to the top level signal names in the project
5
6## Clock signal
7set_property PACKAGE_PIN W5 [get_ports clock]
8set_property IOSTANDARD LVCMOS33 [get_ports clock]
9create_clock -add -name sys_clk_pin -period 10.00 -waveform {0 5} [get_ports clk]
10
11## Switches
12set_property PACKAGE_PIN V17 [get_ports {inputs[0]}]
13set_property IOSTANDARD LVCMOS33 [get_ports {inputs[0]}]
14set_property PACKAGE_PIN V16 [get_ports {inputs[1]}]
15set_property IOSTANDARD LVCMOS33 [get_ports {inputs[1]}]
16set_property PACKAGE_PIN W16 [get_ports {inputs[2]}]
17set_property IOSTANDARD LVCMOS33 [get_ports {inputs[2]}]
18set_property PACKAGE_PIN W17 [get_ports {inputs[3]}]
19set_property IOSTANDARD LVCMOS33 [get_ports {inputs[3]}]
20set_property PACKAGE_PIN W15 [get_ports {inputs[4]}]
21set_property IOSTANDARD LVCMOS33 [get_ports {inputs[4]}]
22set_property PACKAGE_PIN V15 [get_ports {inputs[5]}]
23set_property IOSTANDARD LVCMOS33 [get_ports {inputs[5]}]
24set_property PACKAGE_PIN W14 [get_ports {inputs[6]}]
25set_property IOSTANDARD LVCMOS33 [get_ports {inputs[6]}]
26set_property PACKAGE_PIN W13 [get_ports {inputs[7]}]
27set_property IOSTANDARD LVCMOS33 [get_ports {inputs[7]}]
28set_property PACKAGE_PIN V2 [get_ports {inputs[8]}]
29set_property IOSTANDARD LVCMOS33 [get_ports {inputs[8]}]
30set_property PACKAGE_PIN T3 [get_ports {inputs[9]}]
31set_property IOSTANDARD LVCMOS33 [get_ports {inputs[9]}]
32set_property PACKAGE_PIN T2 [get_ports {inputs[10]}]
33set_property IOSTANDARD LVCMOS33 [get_ports {inputs[10]}]
34set_property PACKAGE_PIN R3 [get_ports {inputs[11]}]
35set_property IOSTANDARD LVCMOS33 [get_ports {inputs[11]}]
36set_property PACKAGE_PIN W0 [get_ports {inputs[12]}]
37set_property IOSTANDARD LVCMOS33 [get_ports {inputs[12]}]
38set_property PACKAGE_PIN U1 [get_ports {inputs[13]}]
39set_property IOSTANDARD LVCMOS33 [get_ports {inputs[13]}]
40set_property PACKAGE_PIN T1 [get_ports {inputs[14]}]
41set_property IOSTANDARD LVCMOS33 [get_ports {inputs[14]}]
42set_property PACKAGE_PIN R2 [get_ports {inputs[15]}]
43set_property IOSTANDARD LVCMOS33 [get_ports {inputs[15]}]
44
45
```


Simulation of design on Vivado-

Simulated our design by changing values of signal inputs (below simulated WAVE results)-

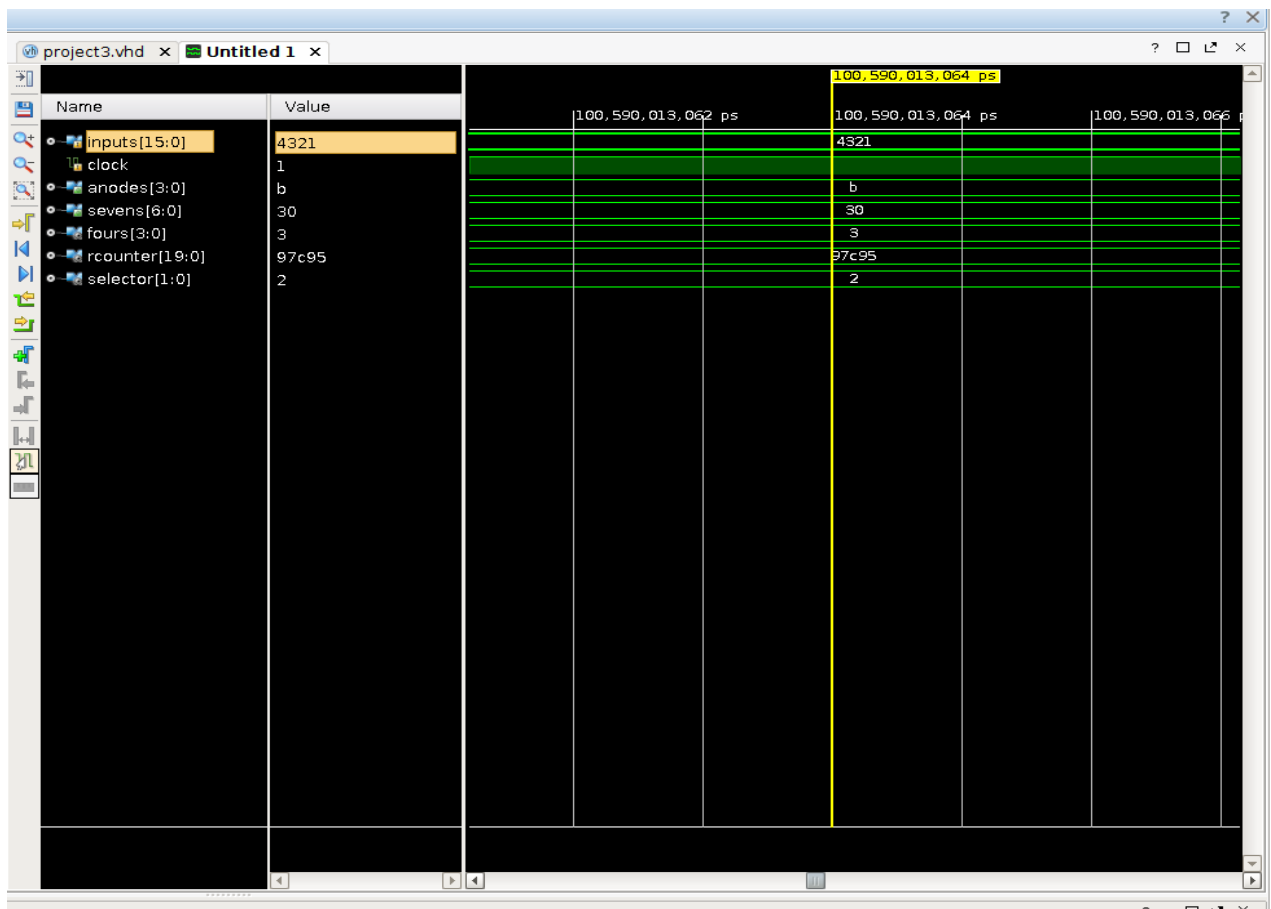
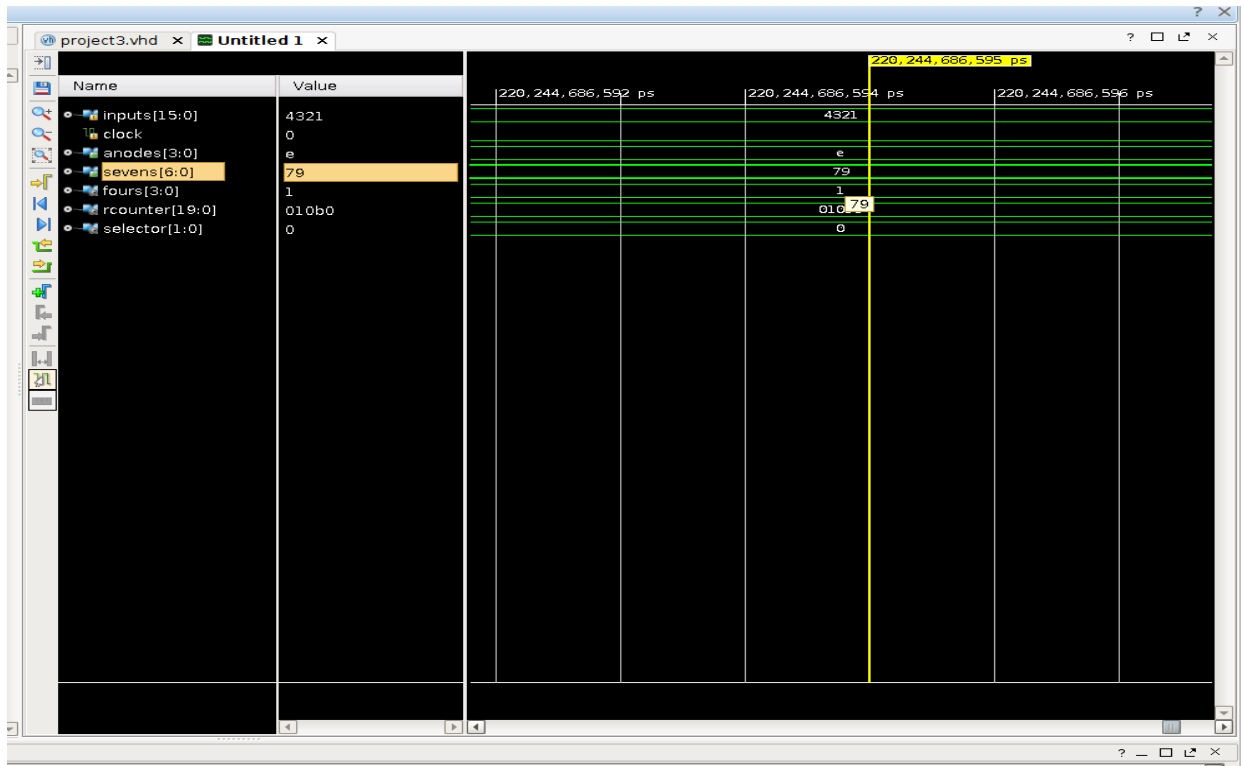


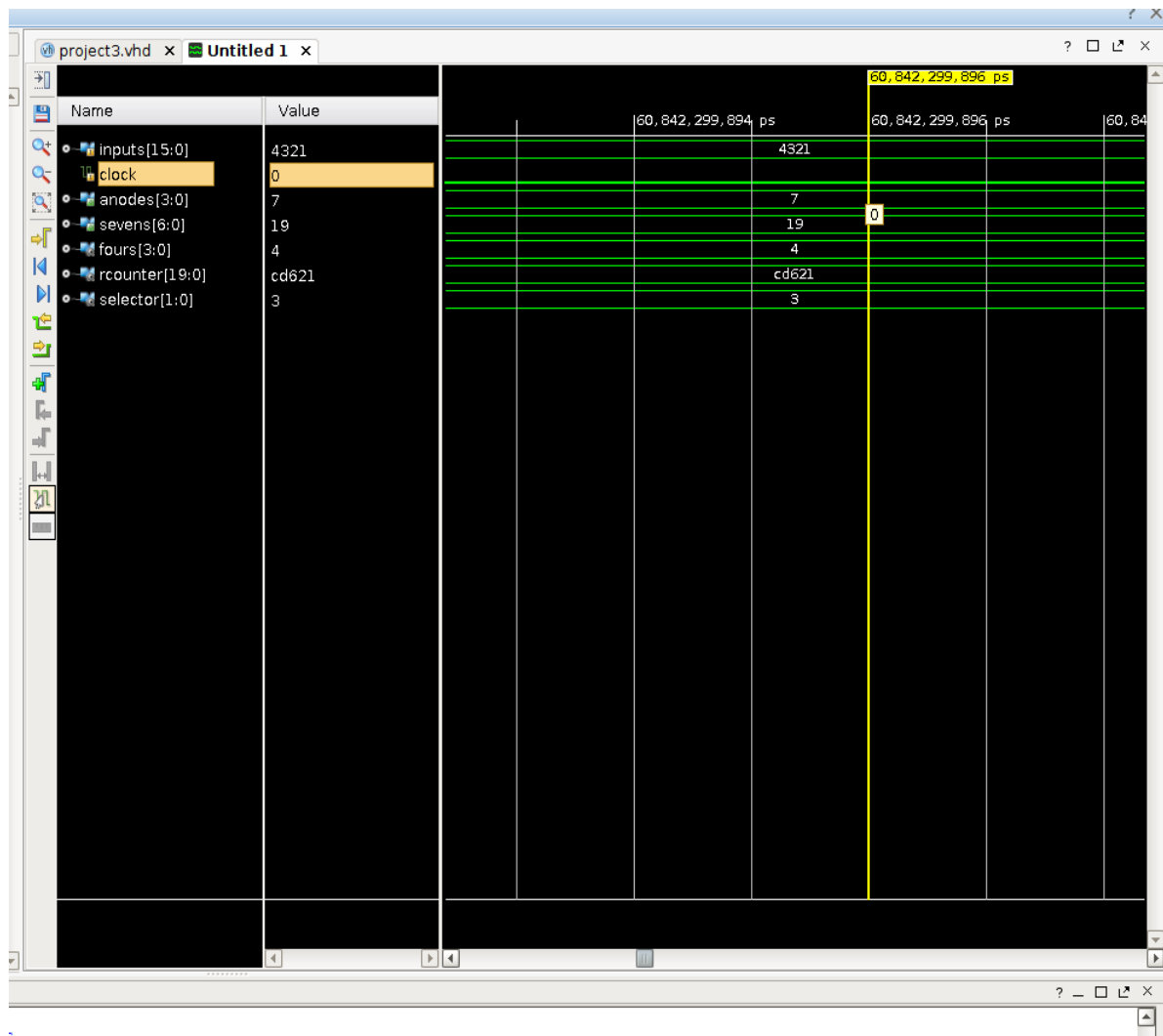
Let understand simulation example ,here in above ,inputs =X"4321"

Anodes="0111" and fours =x"4" as value of rcounter =X"C838F" which help in choosing these value as selector ="11"

Similarly below examples can be understood in this way.





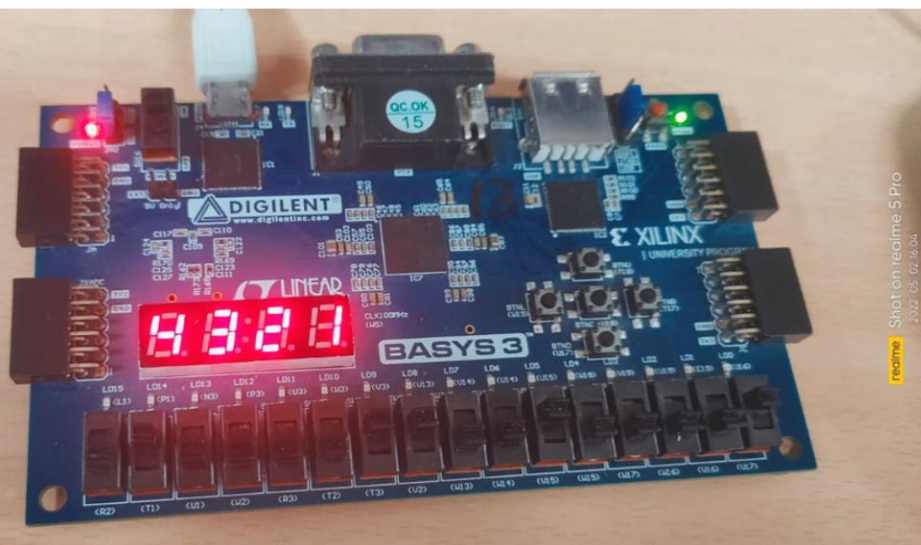


These simulation pics are taken by snapshots at different interval while running clock

After doing above steps or till simulation work, then for implementing design on basys board, we first synthesized design, ran the implementation, then generated Bitstream and finally opened the hardware manager to program device.

Testing on FPGA, Basys 3 board –

We have displayed the pattern 4321 by giving the input 0100001100100001



Resources utilization-

LayoutViewHelp

Quick Access

write_bitstream Complete

Synthesized Designxc7a35tcbg236.2 (active)

Synthesized Design is out-of-date. Newer Synthesis results are available. ReloadClose Design

Netlist

sevensseg4

Nets (82)

Leaf Cells (65)

Sources

Netlist

Netlist Properties

sevensseg4

Primitive Statistics

Primitive type	Count
FLOP_LATCH	9
LUT	25
IO	28
CLK	1
OTHERS	2

Statistics

Properties

I/O Nets

Project Summaryproject3.vhdproject3.xdcSchematic (2)Utilization Report - synth_1

/home/dual/cs5190439/COL215P/project_3/project_3.runs/synth_1/sevensseg4_utilization_synth.rptRead-only

136	DNA_PORT	0	0	1	0.00
137	EFUSE_USR	0	0	1	0.00
138	FRAME_ECCE2	0	0	1	0.00
139	ICAPE2	0	0	2	0.00
140	PCIE_2_1	0	0	1	0.00
141	STARTUPE2	0	0	1	0.00
142	XADC	0	0	1	0.00
143					
144					
145					
146	7. Primitives				
147					
148					
149					
150	Ref Name	Used	Functional Category		
151					
152	LUT1	20	LUT		
153	FORE	20	Flop & Latch		
154	IBUF	17	IO		
155	OBUF	11	IO		
156	LUT4	7	LUT		
157	CARRY4	5	CarryLogic		
158	LUT6	4	LUT		
159	LUT2	4	LUT		
160	BUFG	1	Clock		
161					
162					
163					
164	8. Black Boxes				
165					
166					
167					
168	Ref Name	Used			
169					
170					
171					
172	9. Instantiated Netlists				
173					
174					
175					

Device view-

File View Help Quick Access

write_bitstream Complete

Synthesized Design - xc7a35tcbg236 2 (active)

Project Summary x Device x project3.vhd x project3.xdc x

Netlist

- sevensseg4
- Nets (82)
- Leaf Cells (65)

Sources Netlist

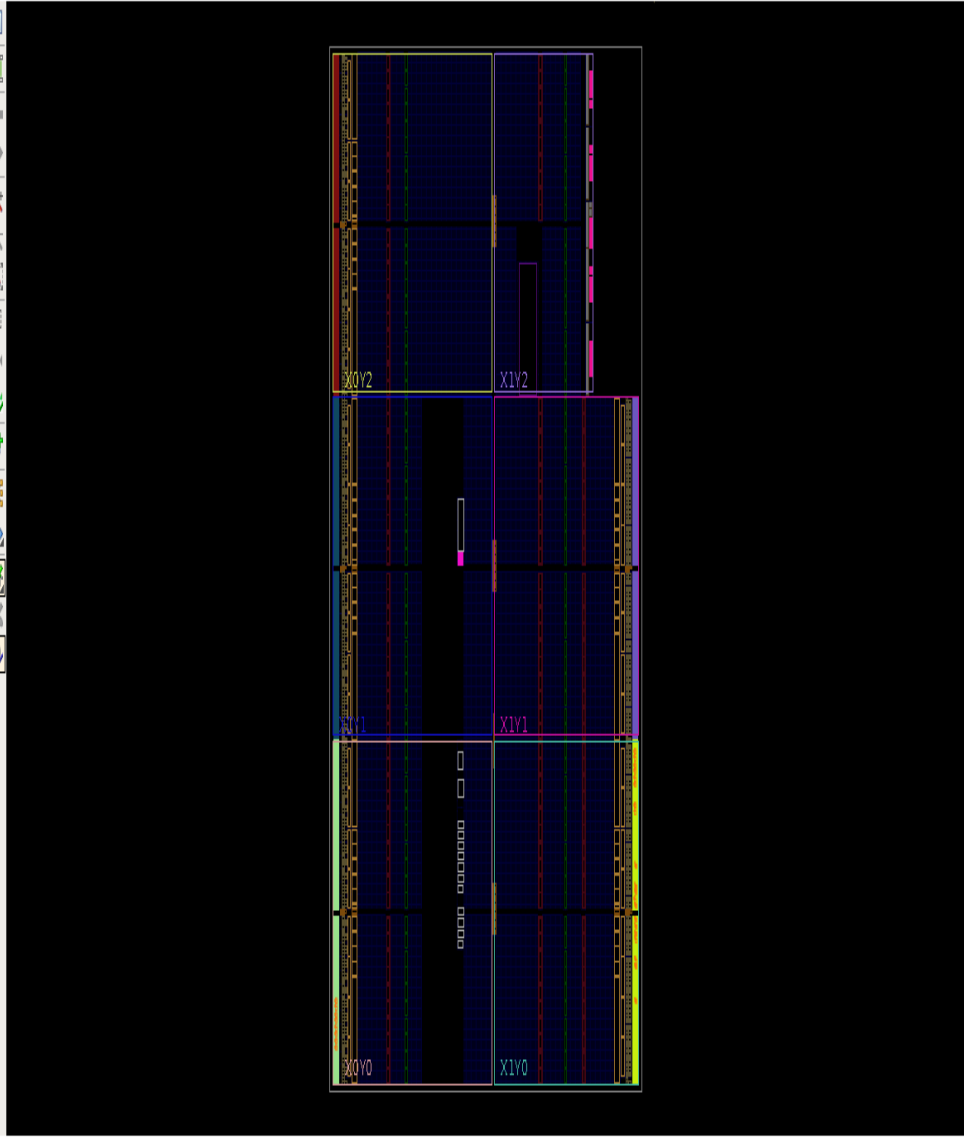
Netlist Properties

sevensseg4

Primitive Statistics

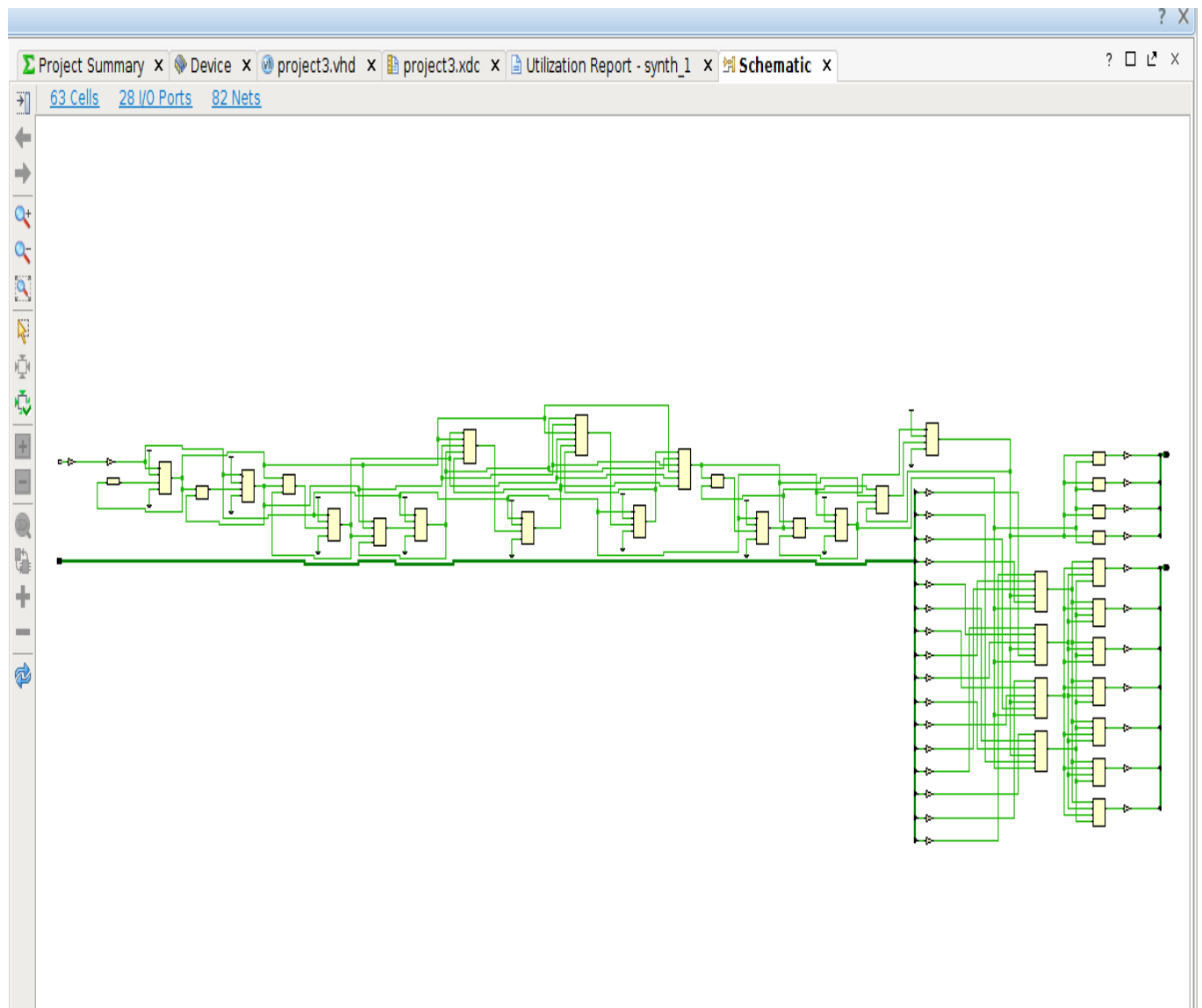
Primitive type	Count
FLOP_LATCH	9
LUT	25
IO	28
CLK	1
OTHERS	2

Statistics Properties I/O Nets



SCHEMETIC VIEW-

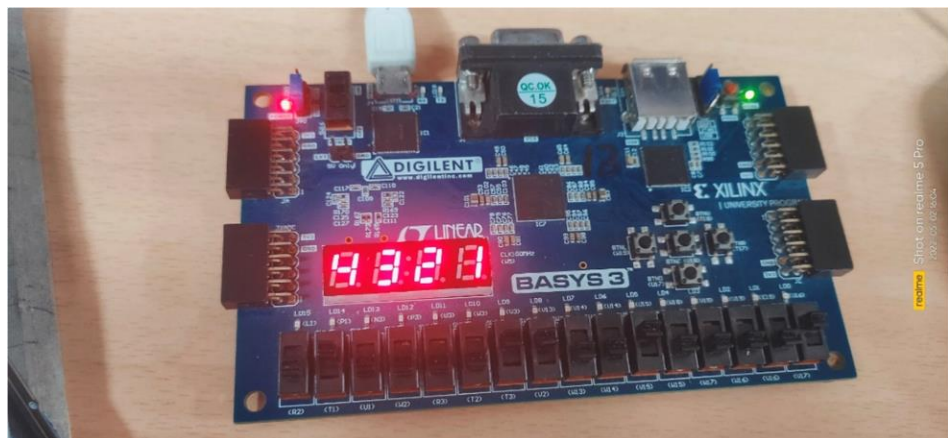
Here is the circuit for 4digit seven segment multiple display ,refresh period-10.5ms.



Below is time taking hardwork for finding refresh rate range by testing on board-

For below procedure,images decription is above and its image below...

For refresh period of 10.5 sec,Rcounter size is 20 bit(Submitted code)-



Below is generalization of attempt for calculating refresh rate range, let—

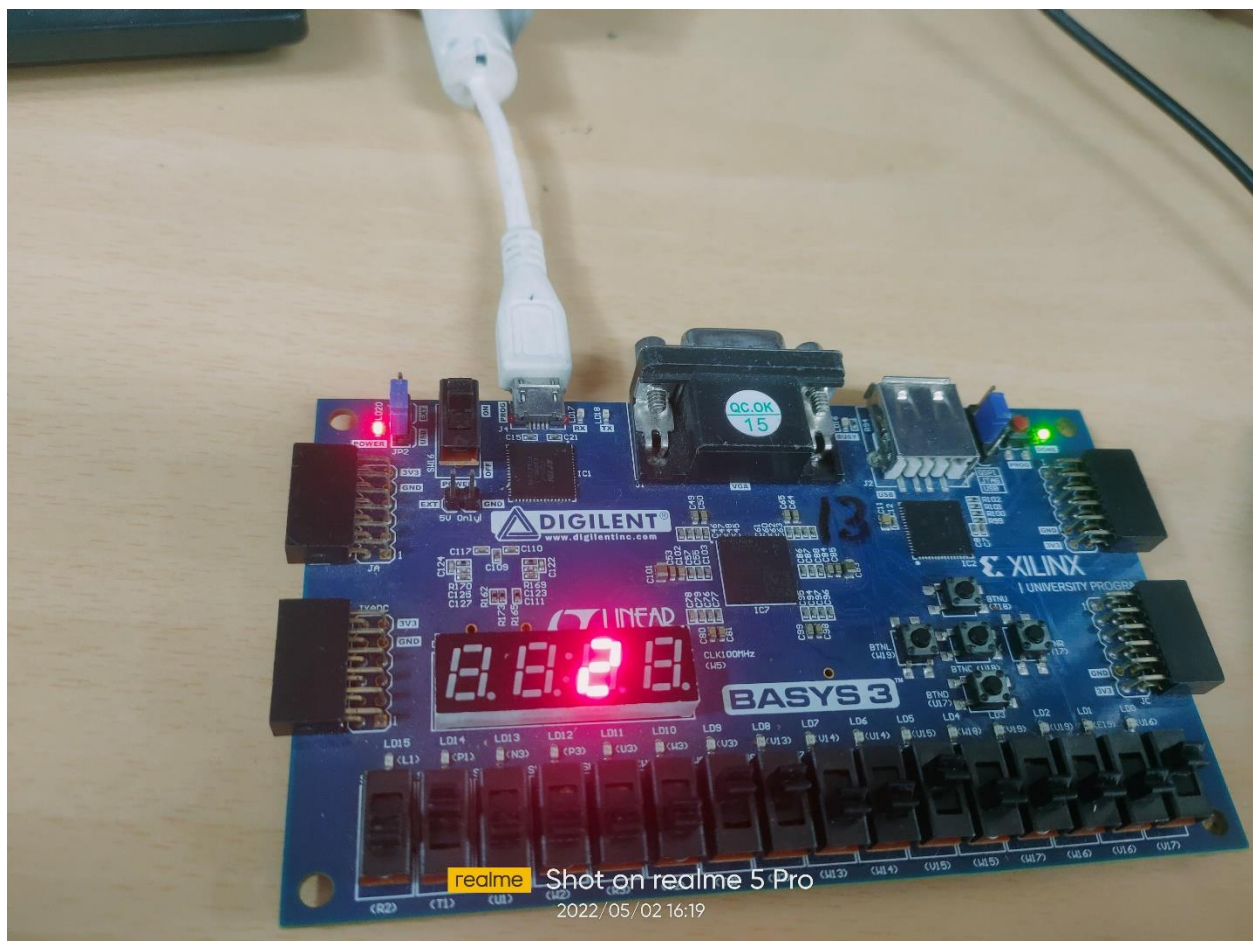
rcounter length – nbits

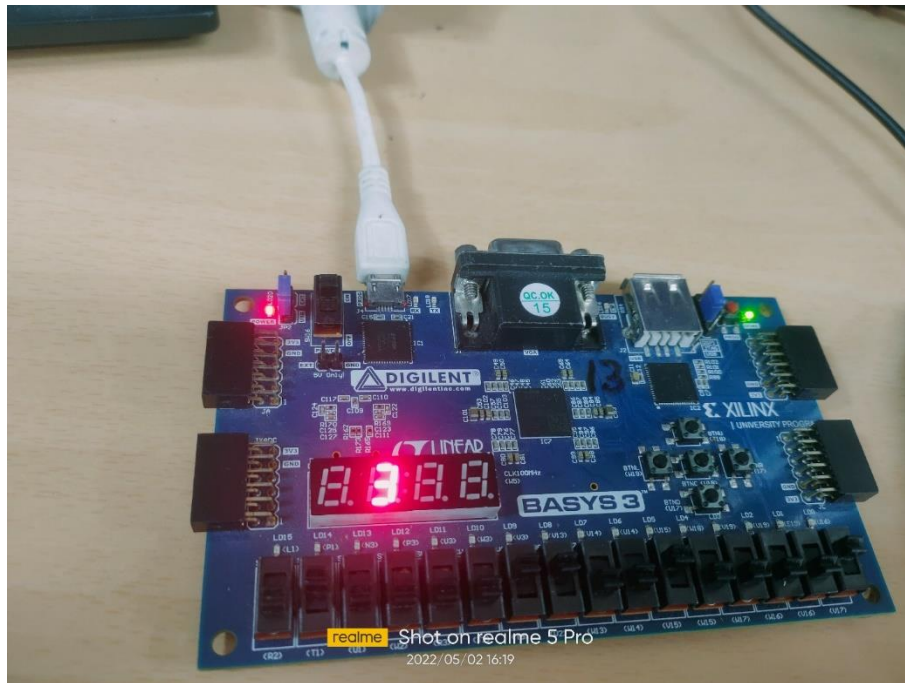
refresh period = $2^n / 10^8$ sec (as clock 100 Mhz)

So we found, refresh rate range for fine display- 0.01ms -20.9 ms

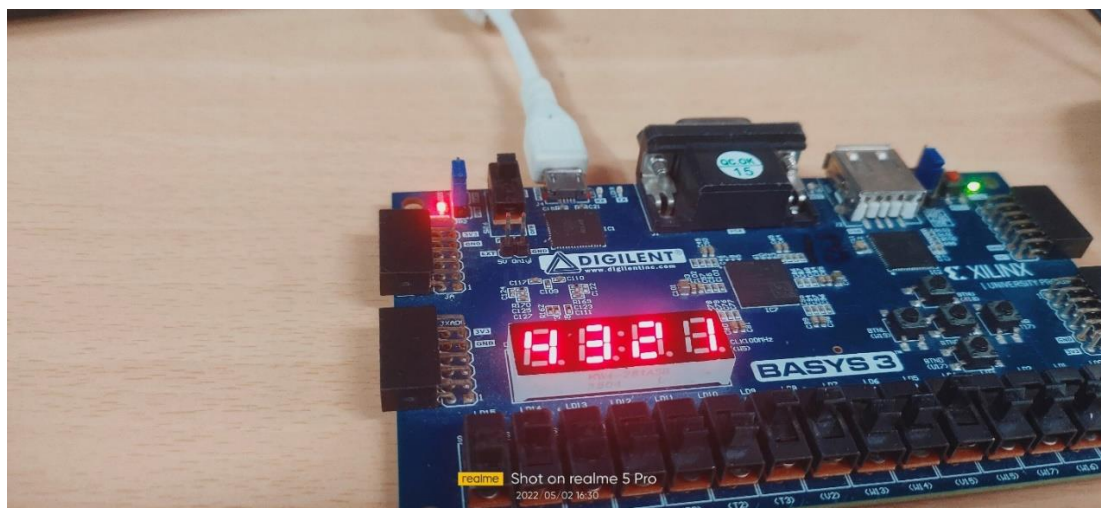
Below, rcounter length -26...

Changes seeing by eye..like rotating

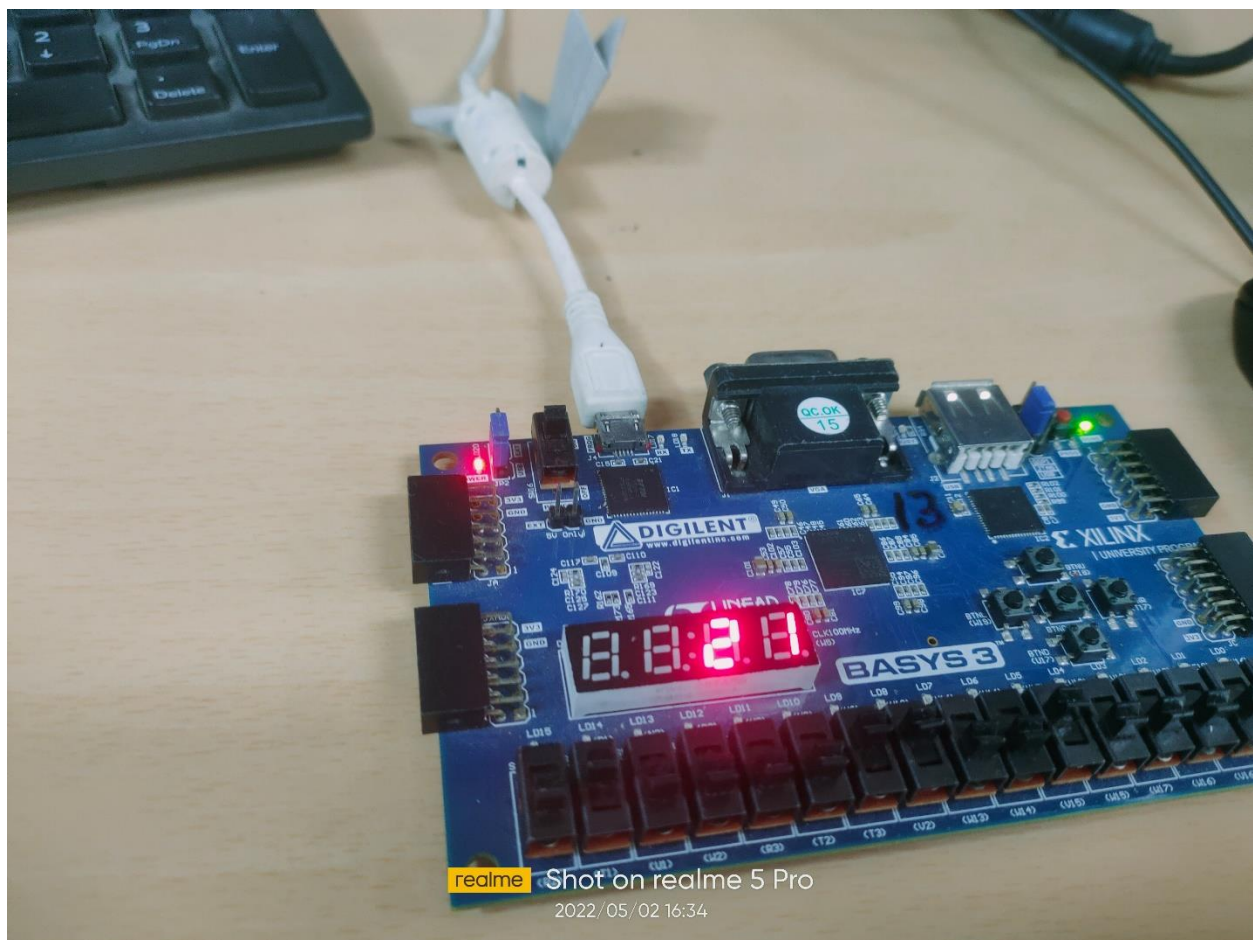
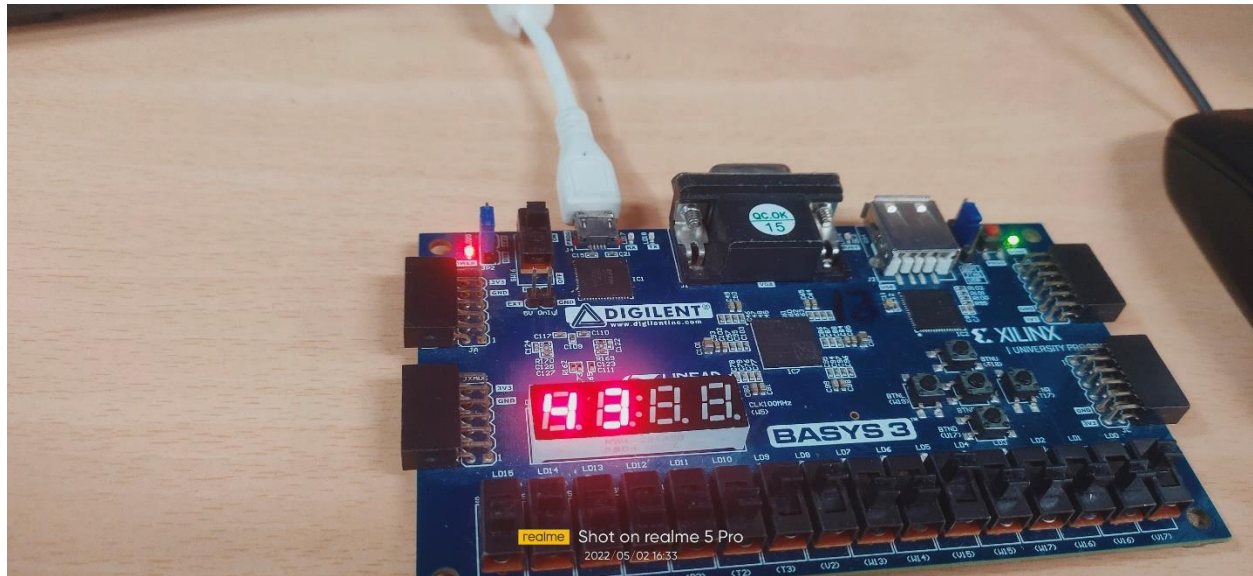




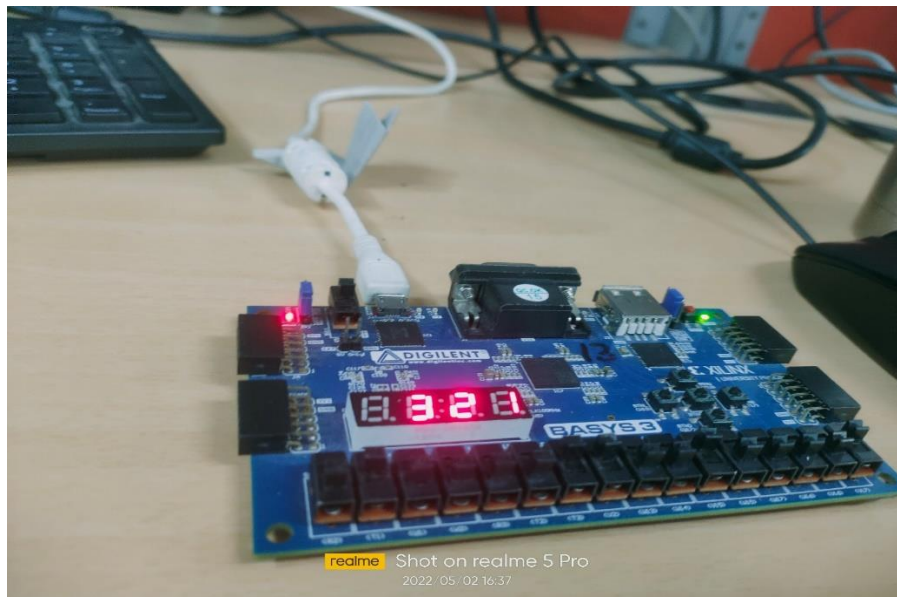
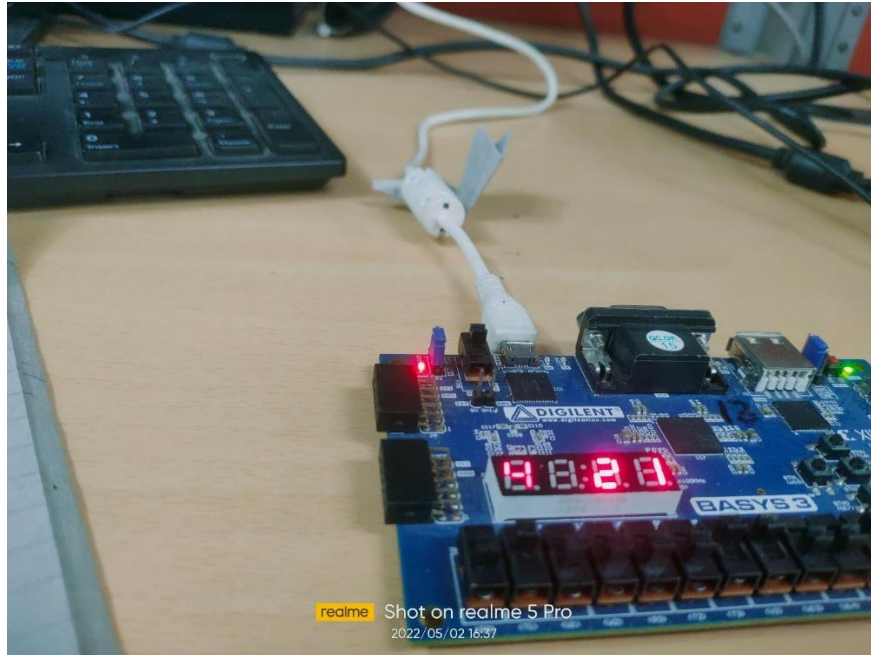
Rcounter length – 21 (max period limit)



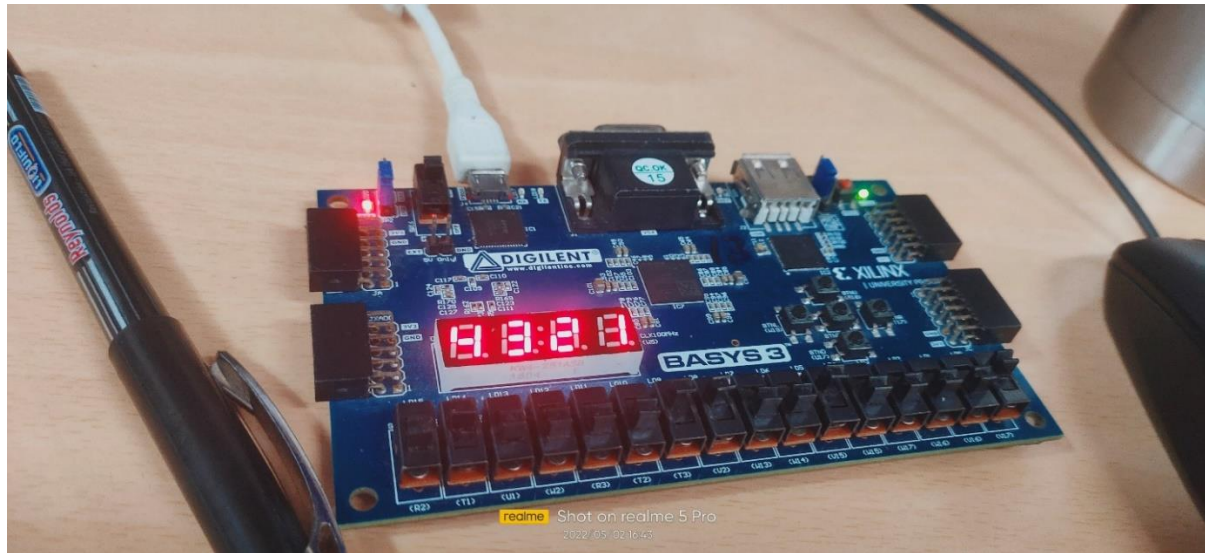
Rcounter length – 23



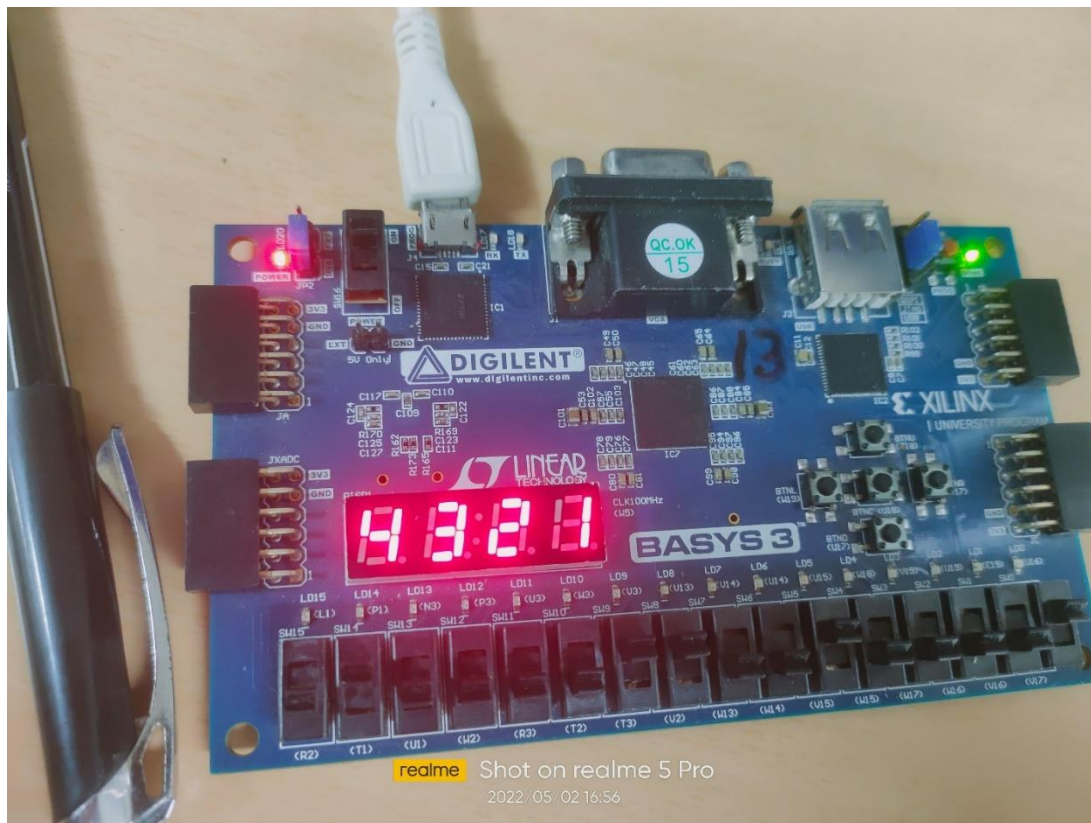
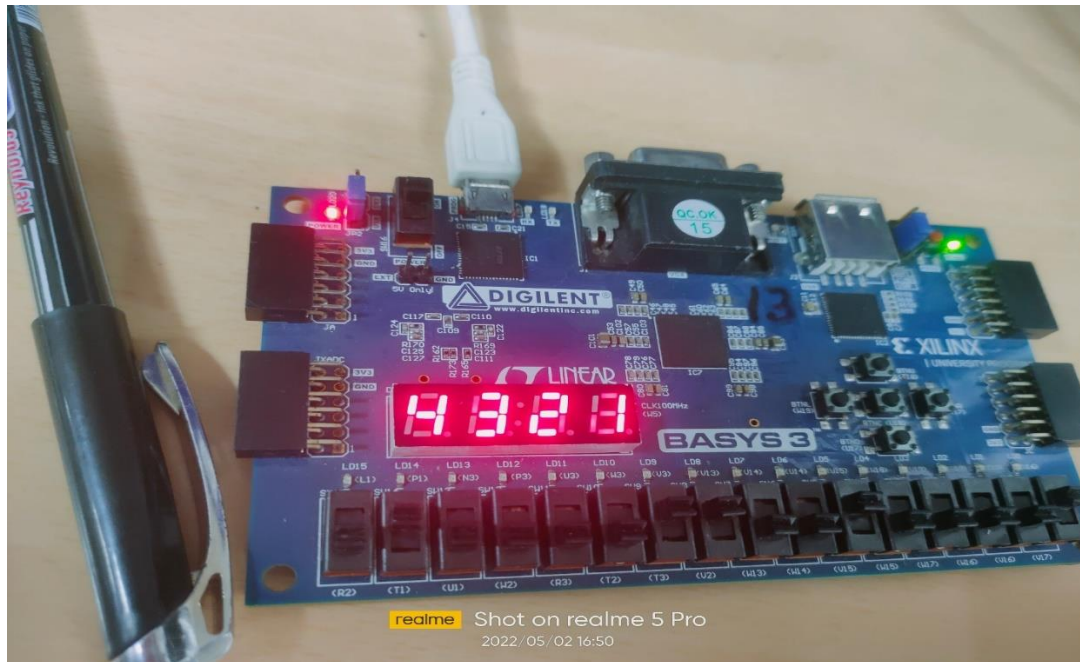
Rcounter length – 22



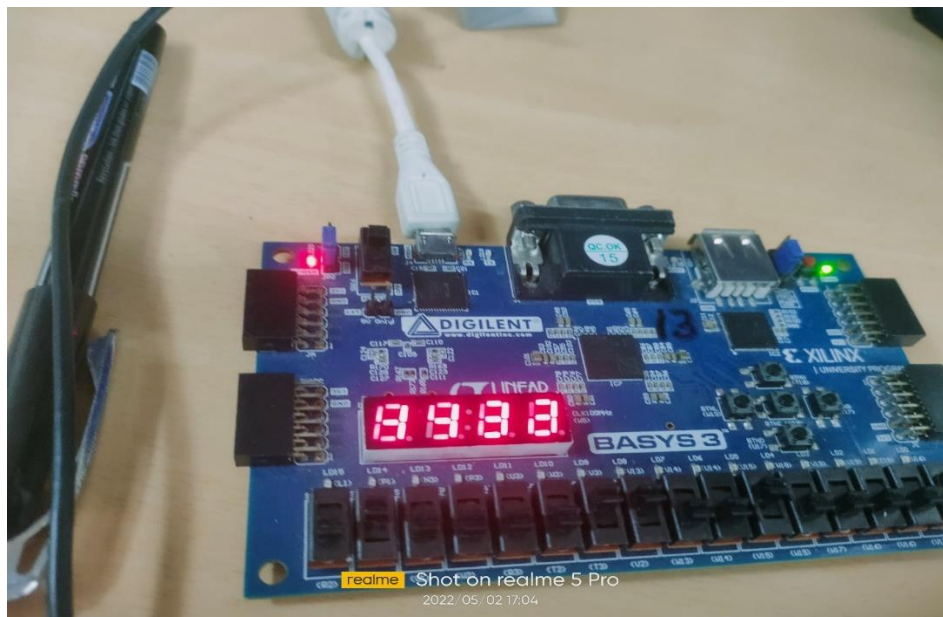
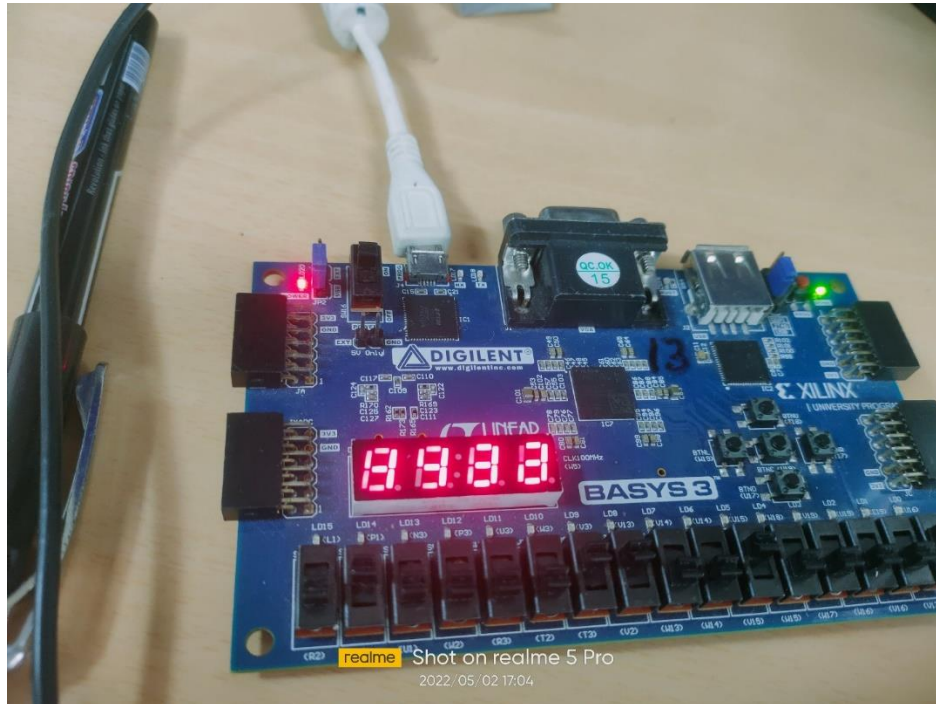
Rcounter length – 16



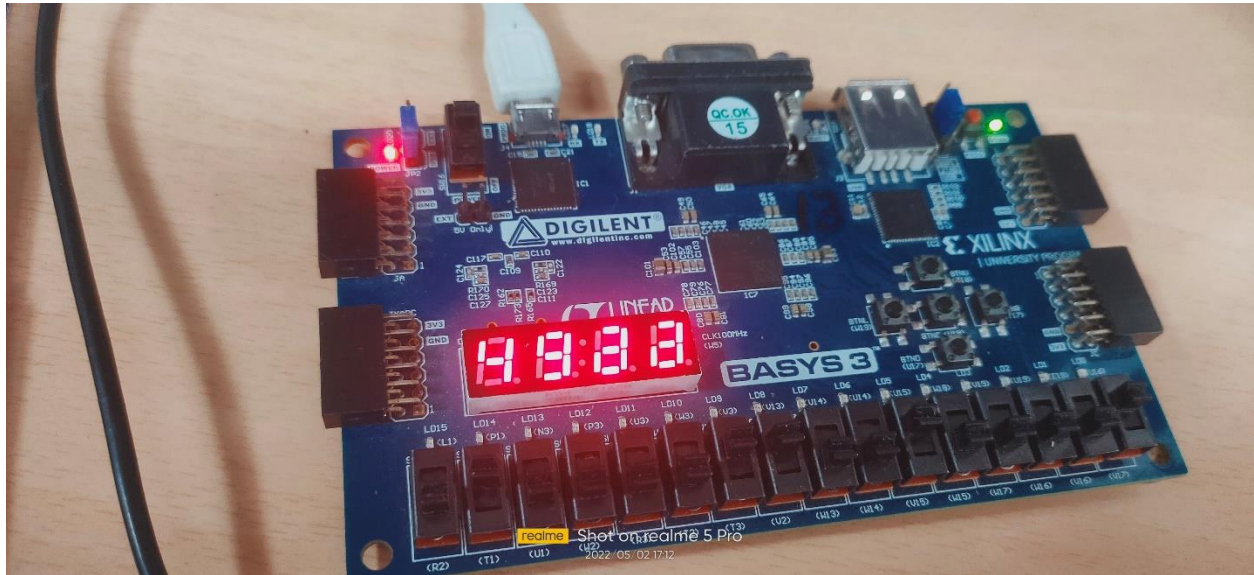
Rcounter length – 10(min limit)-Anshul Sir verified



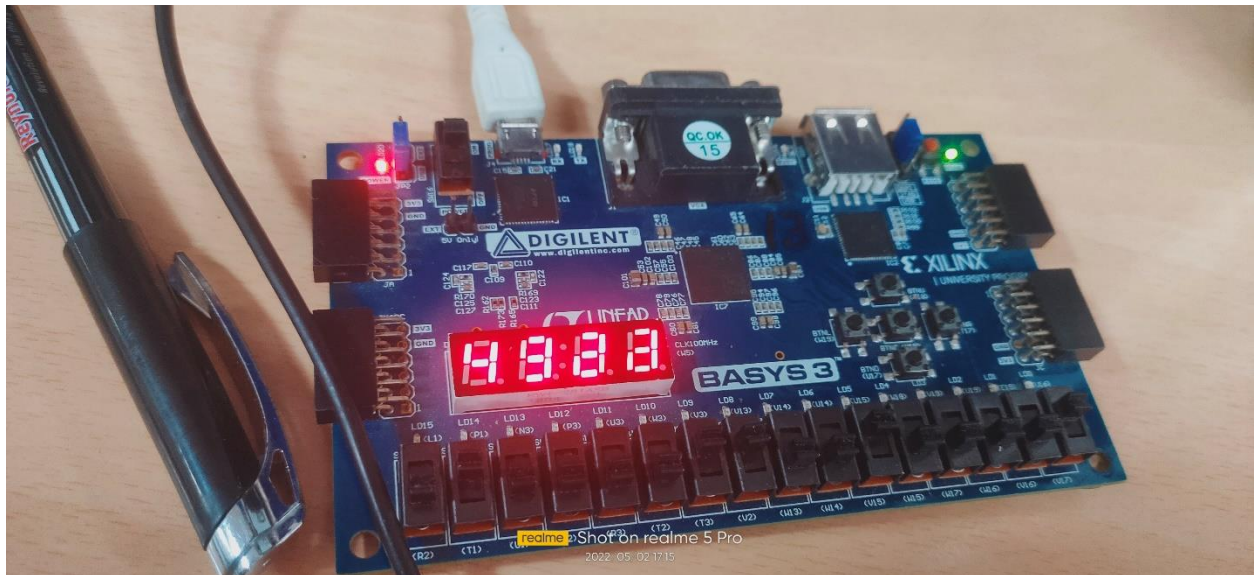
Rcounter length – 4



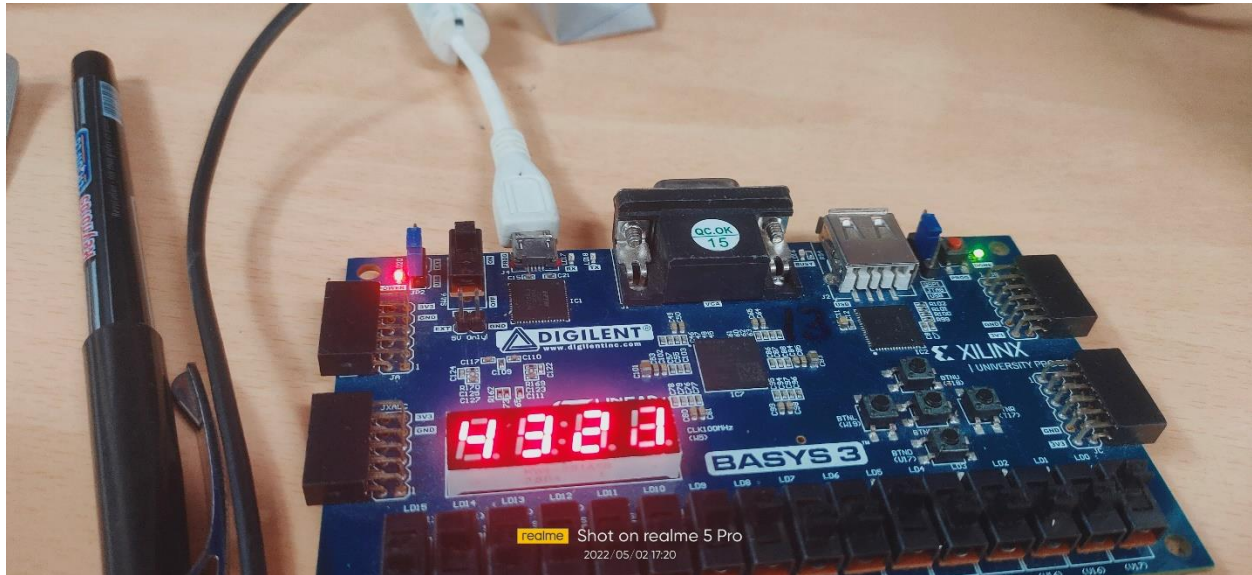
Rcounter length – 6



Rcounter length – 8



Rcounter length –9



Report became long due to adding this range part (but Anshul sir adviced us to do this method).

Thank you!