

ASSIGNMENT-6

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In this assignment we designed a stopwatch and implement it on BASYS 3 board, using 7-segment display already implemented module in A3 and push buttons.

Submission folder (2019CS50439_2019CS50434) contains -

project6.xdc - constraint file

a6.vhd -vhdl code file

stopwatch.bit - bitstream file

A6_report.pdf- report file

EDA PLAYGROUND Code and simulation-

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testbench.vhd

```
17 -- Additional Comments:
18 --
19 -----
20 -----
21
22 --4 seven segment-A3
23
24 library IEEE;
25 use IEEE.std_logic_1164.all;
26 use IEEE.NUMERIC_STD.ALL;
27 use IEEE.STD_LOGIC_UNSIGNED.ALL;
28
29 entity sevenseg4 is
30 port(
31   inputs: in std_logic_vector(15 downto 0);
32   clock : in std_logic;  --clock 100Mhz
33   --, reset
34   anodes: out std_logic_vector(3 downto 0);
35   sevens: out std_logic_vector(6 downto 0)
36 );
37 end sevenseg4;
38
39 -- architecture
40 architecture funct4 of sevenseg4 is
41   signal fours : std_logic_vector(3 downto 0);-- := "0000"
42   signal rcouter: std_logic_vector(19 downto 0) := (others =>
```

design.vhd

```
34 --A6
35
36 library IEEE;
37 use IEEE.std_logic_1164.all;
38 use IEEE.NUMERIC_STD.ALL;
39 --use IEEE.STD_LOGIC_UNSIGNED.ALL
40
41 entity stopwatch is
42 port(
43   clock, reset : in std_logic;  --clock 100Mhz
44   anodes: out std_logic_vector(3 downto 0);
45   sevens: out std_logic_vector(6 downto 0);
46   button1: in std_logic;
47   button2: in std_logic
48 );
49 end stopwatch;
50
51 -- architecture
52 architecture beh of stopwatch is
53   signal fours : std_logic_vector(3 downto 0);-- := "0000"
54   signal rcouter: unsigned(19 downto 0) := (others => '0');--
55   refresh counter
56   --for creating refresh period of 10.5ms
57   -- signal drive: std_logic := '0';
58   signal selector : unsigned(1 downto 0);
59   signal count : integer range 0 to 10000000;
60   signal state : std_logic_vector(1 downto 0) := "00"--start
```

👤 Log

🔗 Share

🐦 f in 🔗

A6

1 views and 0 likes

👤 Public (anyone with the link can view)

📄 Save

New project6 on Vivado-

project_6 - [/home/dual/cs5190439/COL215P/project_6/project_6.xpr] - Vivado 2016.4

File Edit Flow Tools Window Layout View Help

write_bitstream Complete

Flow Navigator

- Project Manager
 - Project Settings
 - Add Sources
 - Language Templates
 - IP Catalog
- IP Integrator
 - Create Block Design
 - Open Block Design
 - Generate Block Design
- Simulation
 - Simulation Settings
 - Run Simulation
- RTL Analysis
 - Elaboration Settings
 - Open Elaborated Design
- Synthesis
 - Synthesis Settings
 - Run Synthesis
 - Open Synthesized Design
- Implementation
 - Implementation Settings
 - Run Implementation
 - Open Implemented Design
- Program and Debug
 - Bitstream Settings
 - Generate Bitstream
 - Hardware Manager
 - Open Target
 - Program Device
 - Add Configuration Mem

Project Manager - project_6

Sources

- Design Sources (1)
 - stopwatch - beh (project6.vhd) (1)
- Constraints (1)
 - constrs_1 (1)
 - project3.xdc
- Simulation Sources (1)

Project Settings

Project name: project_6

Project location: /home/dual/cs5190439/COL215P/project_6

Product family: Artix-7

Project part: xc7a35tcpq236-2

Top module name: stopwatch

Target language: VHDL

Simulator language: Mixed

Synthesis

Status: Complete

Messages: 1 warning

Part: xc7a35tcpq236-2

Strategy: Vivado Synthesis Defaults

Implementation

Status: Complete

Messages: 3 warnings

Part: xc7a35tcpq236-2

Strategy: Vivado Implementation Defaults

Incremental compile: None

Summary Route Status

DRC Violations

Summary: 1 warning

Implemented DRC Report

Timing

Worst Negative Slack (WNS): NA

Total Negative Slack (TNS): NA

Number of Failing Endpoints: NA

Total Number of Endpoints: NA

Implemented Timing Report

Setup Hold Pulse Width

Power

Total On-Chip Power: 10.307 W

Junction Temperature: 76.5 °C

Thermal Margin: 8.5 °C (1.7 W)

Effective Rja: 5.0 °C/W

Power supplied to off-chip devices: 0 W

Utilization - Post-Implementation

Category	Value
LUT	1%
FF	1%
IO	14%
BUFG	3%

Hierarchy Libraries Compile Order

Source File Properties

project3.xdc

Enabled

Location: /home/dual/cs5190439/COL215P/project_6

Type: XDC

Size: 13.2 KB

Modified: Today at 16:58:04 PM

Copied to: <Project Directory>/project_6/srcs/const

Read-only: No

Encrypted: No

Core Container: No

General Properties

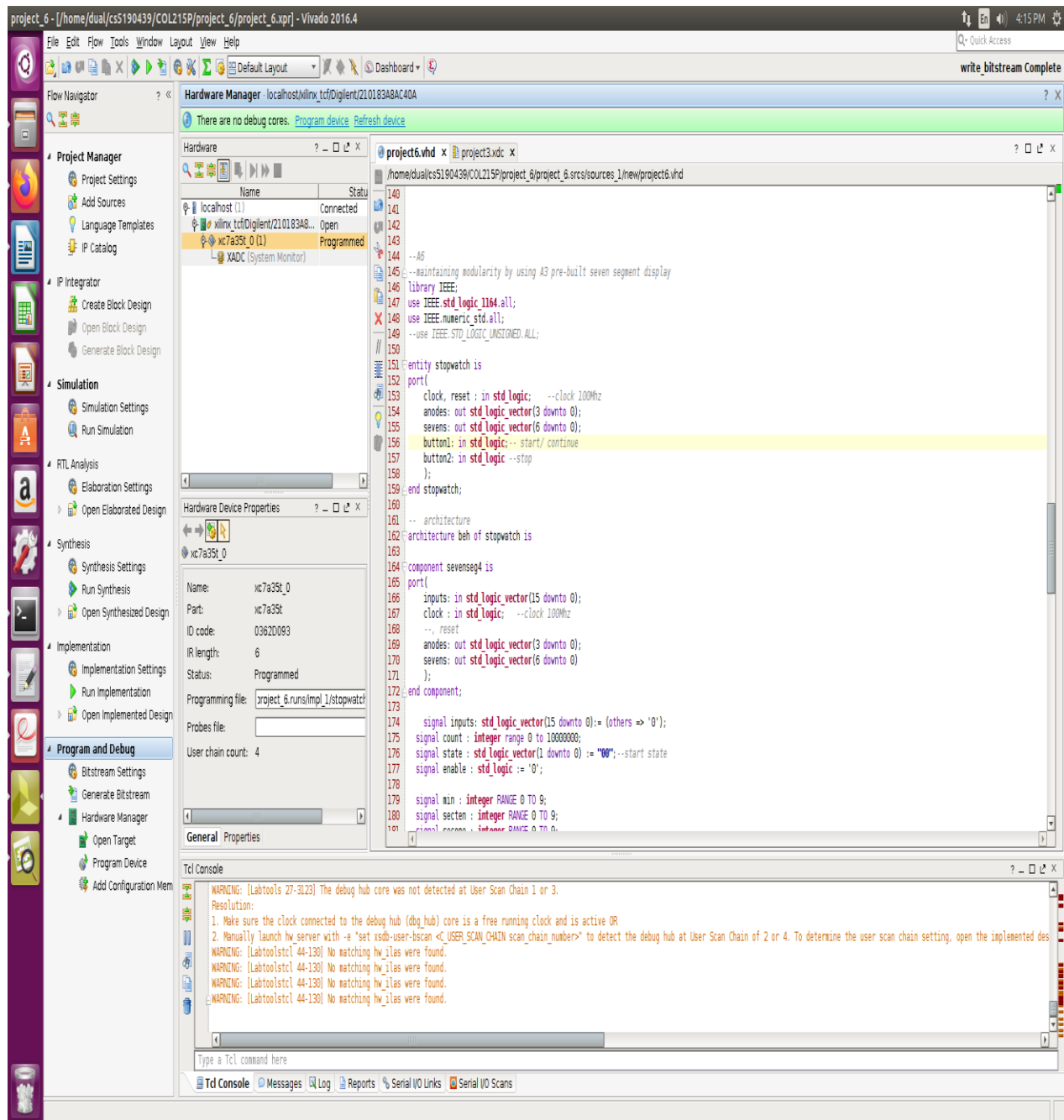
Tcl Console

```
refresh_hw_device [lindex [get_hw_devices xc7a35t_0] 0]
INFO: [Labtools 27-1434] Device xc7a35t (JTAG device index = 0) is programmed with a design that has no supported debug core(s) in it.
WARNING: [Labtools 27-3123] The debug hub core was not detected at User Scan Chain 1 or 3.
Resolution:
1. Make sure the clock connected to the debug hub (dbg_hub) core is a free running clock and is active OR
2. Manually launch hw server with -e "set xsdb-user-bscan <C_USER_SCAN_CHAIN scan_chain_number>" to detect the debug hub at User Scan Chain of 2 or 4. To determine the user scan chain setting, open the implemented des
WARNING: [Labtools 44-130] No matching hw_1las were found.
WARNING: [Labtools 44-130] No matching hw_1las were found.
WARNING: [Labtools 44-130] No matching hw_1las were found.
WARNING: [Labtools 44-130] No matching hw_1las were found.
```

Type a Tcl command here

Tcl Console Messages Log Reports Design Runs

VHDL code on Vivado -



The code is also provided in the submission file

DESCRIPTION

Here we assumed normal indexing of segments of seven segment display(B-2,etc)

What we have done is take a counter that increments every clock rising edge and after $10^7 - 1$ increments it increases the value of first LED (one-tenth of a second) then after 10 such increments the second LED is increased by one (one second), then after ten such seconds the third LED is increased by one (tens digit seconds) then after 6 such increases the fourth LED is increased by one (the minute one).

All the LEDs are reseted back to zero when they reach their limit (as per given in the assignment requirement). All of them are also reseted when reset button is pushed.

timing for refreshing the 4-digit seven-segment display on Basys 3 FPGA is same as A3,used same 4 digits sement display module-

Design decision

There is three button for implementation.

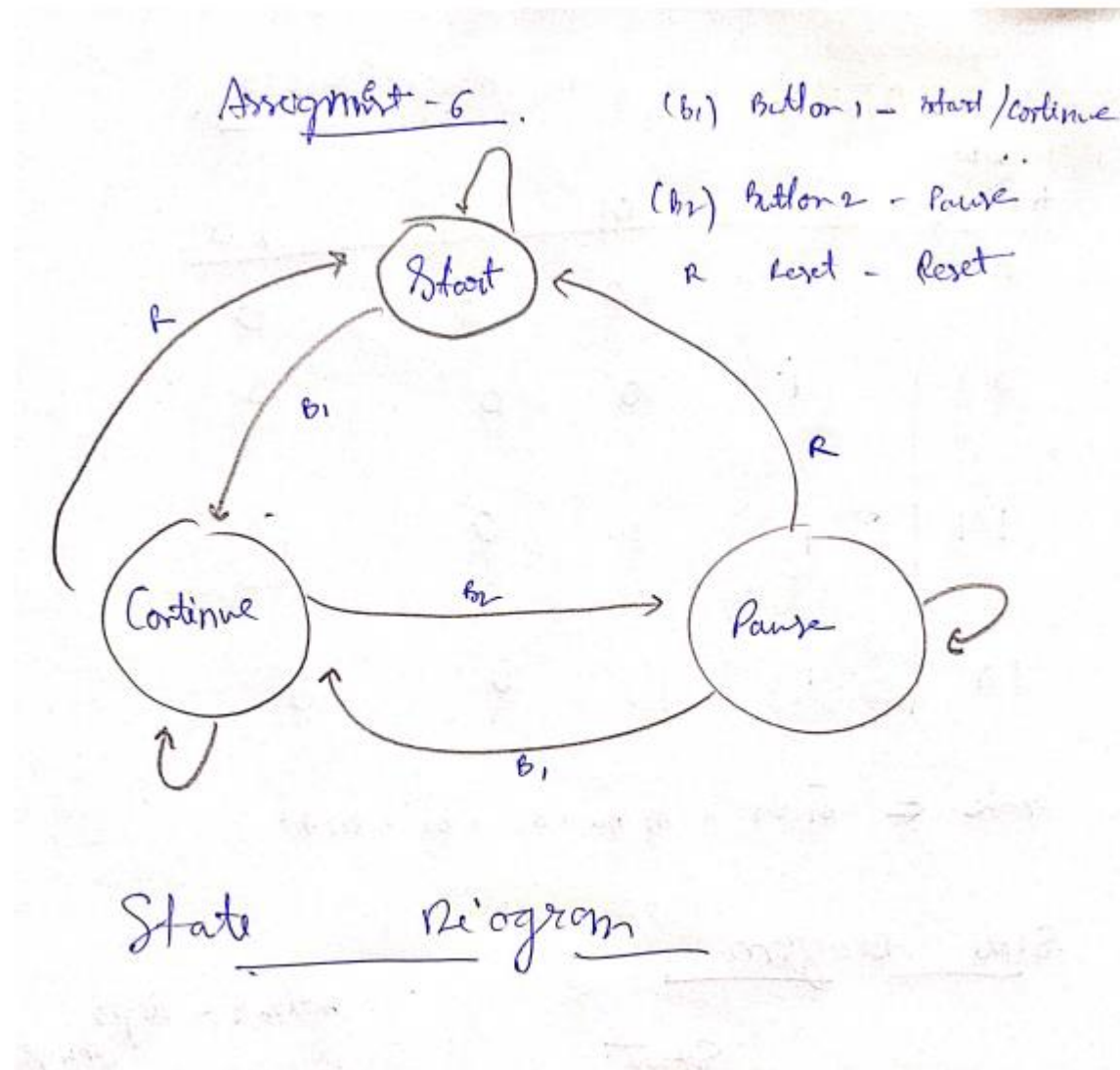
There are three states – START(on also reset),CONTINUE(on button1),PAUSE (on button2).

Start is from uniform 0000 digits.

When button1 pressed ,then stopwatch get start or continue on display.

When button2 pressed ,then pause the stopwatch

STATE DIAGRAM



Constraint file

Anodes and cathodes matching-

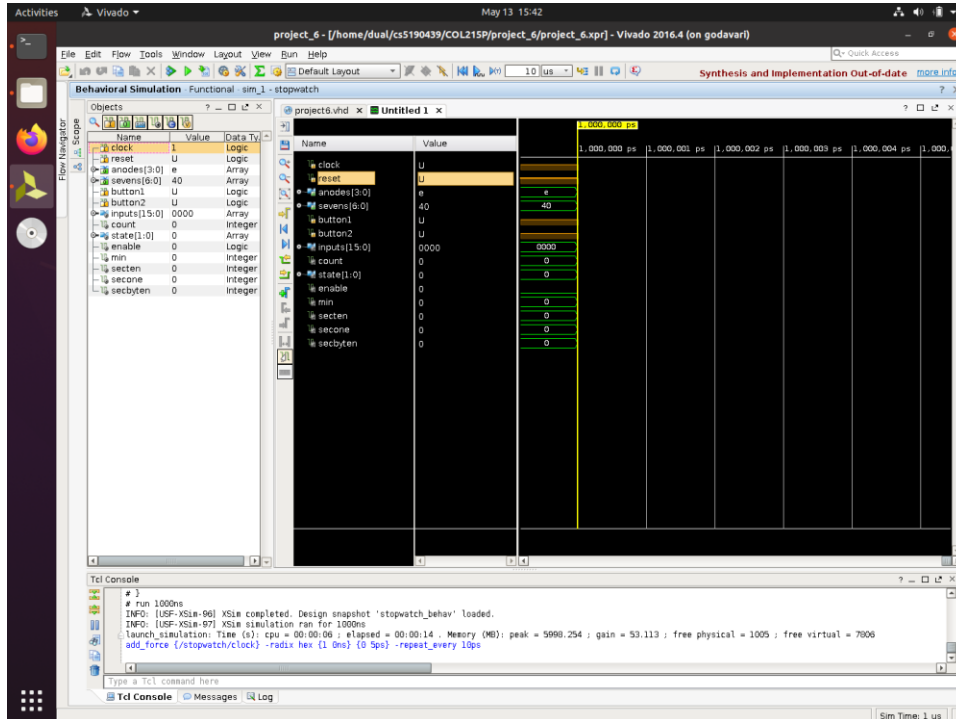
The screenshot displays the Vivado 2016.4 IDE interface. The top menu bar includes File, Edit, Flow, Tools, Window, Layout, View, and Help. The main workspace is divided into several panes:

- Flow Navigator:** Shows the project flow from Project Manager to Program and Debug.
- Hardware Manager:** Displays the hardware configuration for the device. It shows a table with columns for Name, Connected, and Status. The device is identified as xc7a35t_0 (1) and is in the 'Programmed' state.
- Project Manager:** Shows the project settings, including the project name 'project_6' and the target device 'xc7a35t_0 (1)'.
- Hardware Device Properties:** Provides detailed information about the device, including Name (xc7a35t_0), Part (xc7a35t), ID code (03620093), IR length (6), Status (Programmed), Programming file (project_6.runs/impl_1/stopwatch), and Probes file.
- Tcl Console:** Displays the output of the Tcl commands. It shows a warning message: "WARNING: [Labtools 27-3123] The debug hub core was not detected at User Scan Chain 1 or 3." and a resolution step: "1. Make sure the clock connected to the debug hub (dbg_hub) core is a free running clock and is active OR".

The bottom status bar indicates the current time as 10:27 and the active file as 'XDC'.

Simulation on vivado

For simulation tried to use faster clock 10ps type and reduced counter maximum values.



But also not able to simulate large time on stopwatch as Vivado crashes unfortunately.

After doing above steps or till simulation work, then for implementing design on basys board, we first synthesized design, ran the implementation, then generated Bitstream and finally opened the hardware manager to program device.

Resources utilization-

The screenshot displays the Vivado 2016.4 IDE interface for a project named 'project_6'. The 'Synthesized Design' tab is active, showing the 'stopwatch' netlist. The 'Netlist' pane on the left lists the components: Nets (170), Leaf Cells (122), and UUT (sevensg4). The 'Primitive Statistics' table provides a breakdown of the design's components:

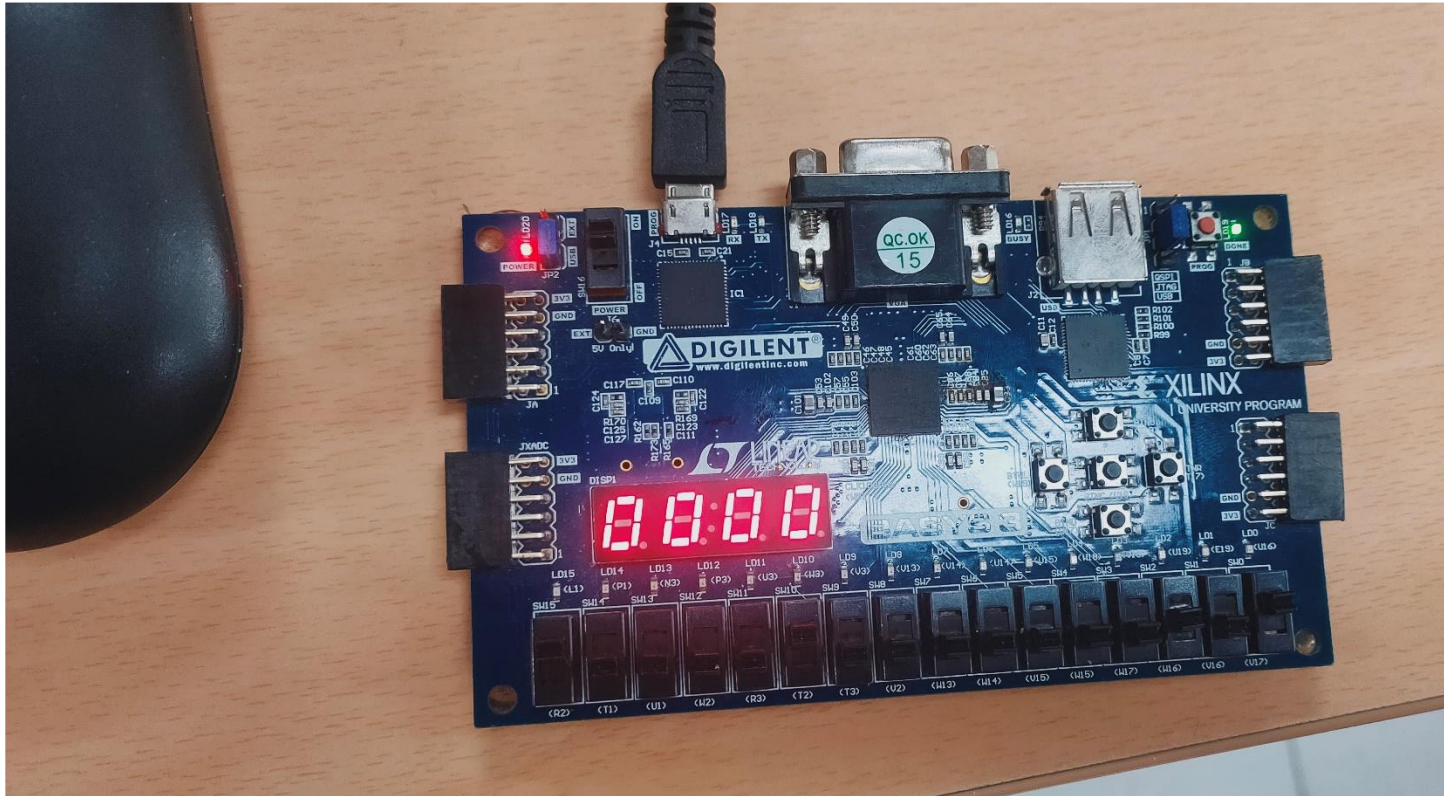
Primitive Type	Count
FLOP_LATCH	62
LUT	91
CARRY	11
IO	15
CLK	1
OTHERS	4

The 'Reports' pane at the bottom shows a list of generated reports, including the 'Utilization Report' which is highlighted. The 'Utilization Report - synth_1' is open, displaying a table of resource utilization for various components:

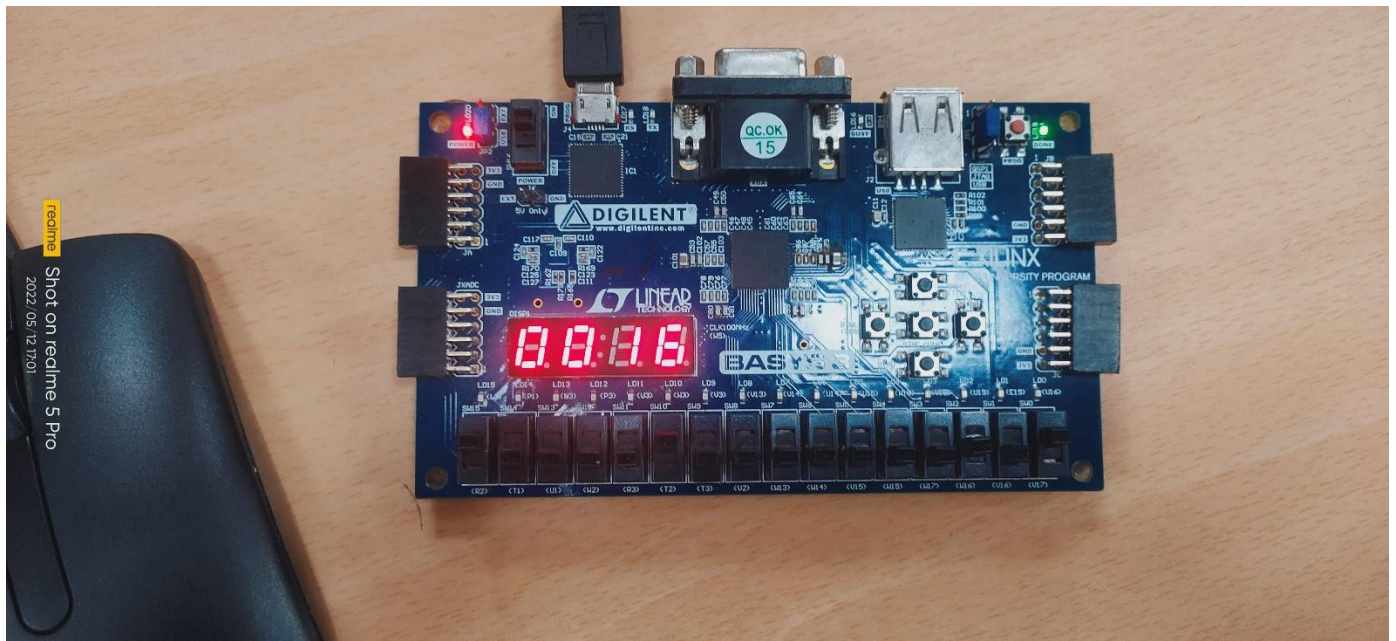
Ref Name	Used	Functional Category
136 DMA_PORT	0	0
137 EPFUSE_USR	0	1
138 FRAME_ECODE2	0	1
139 ICAPE2	0	2
140 PCIE_2_1	0	1
141 STARTUPE2	0	1
142 XADC	0	1
143		
144		
145		
146 Primitives		
147		
148		
149		
150 Ref Name Used Functional Category		
151		
152 FLOP	62	Flop & Latch
153 LUT2	30	LUT
154 LUT1	24	LUT
155 LUT4	21	LUT
156 OBUF	11	IO
157 CARRY4	11	CarryLogic
158 LUT6	10	LUT
159 LUT3	5	LUT
160 IBUF	4	IO
161 LUT5	1	LUT
162 BUF6	1	Clock
163		
164		
165		
166 Black Boxes		
167		
168		
169		
170 Ref Name Used		
171		
172		
173		
174 Instantiated Netlists		
175		
176		

Testing on Basys3 board-

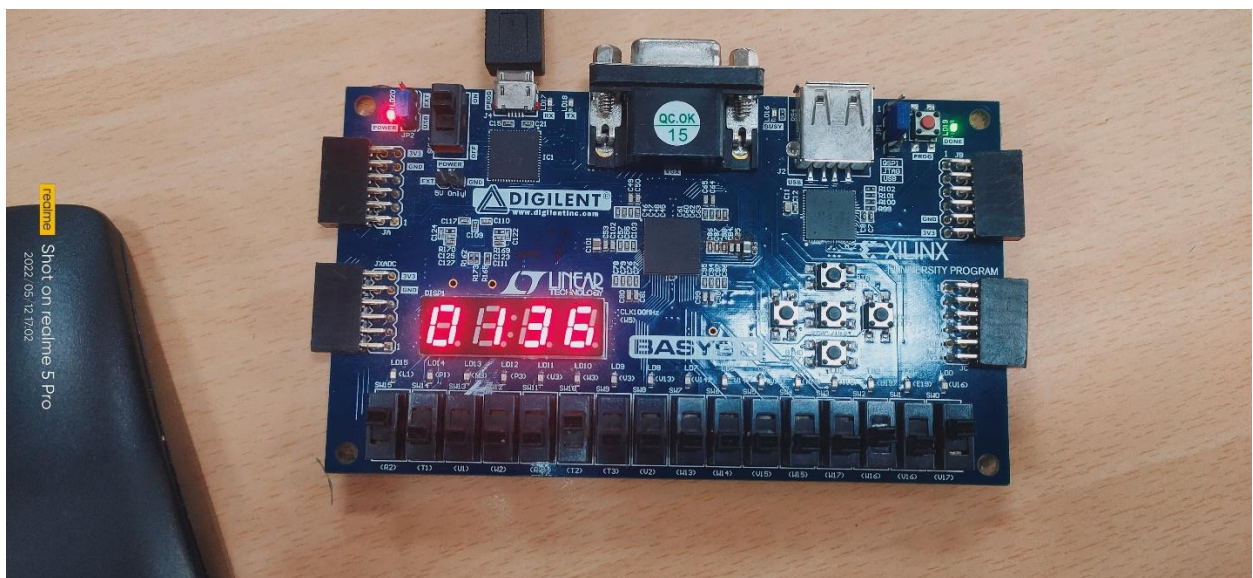
Start state-



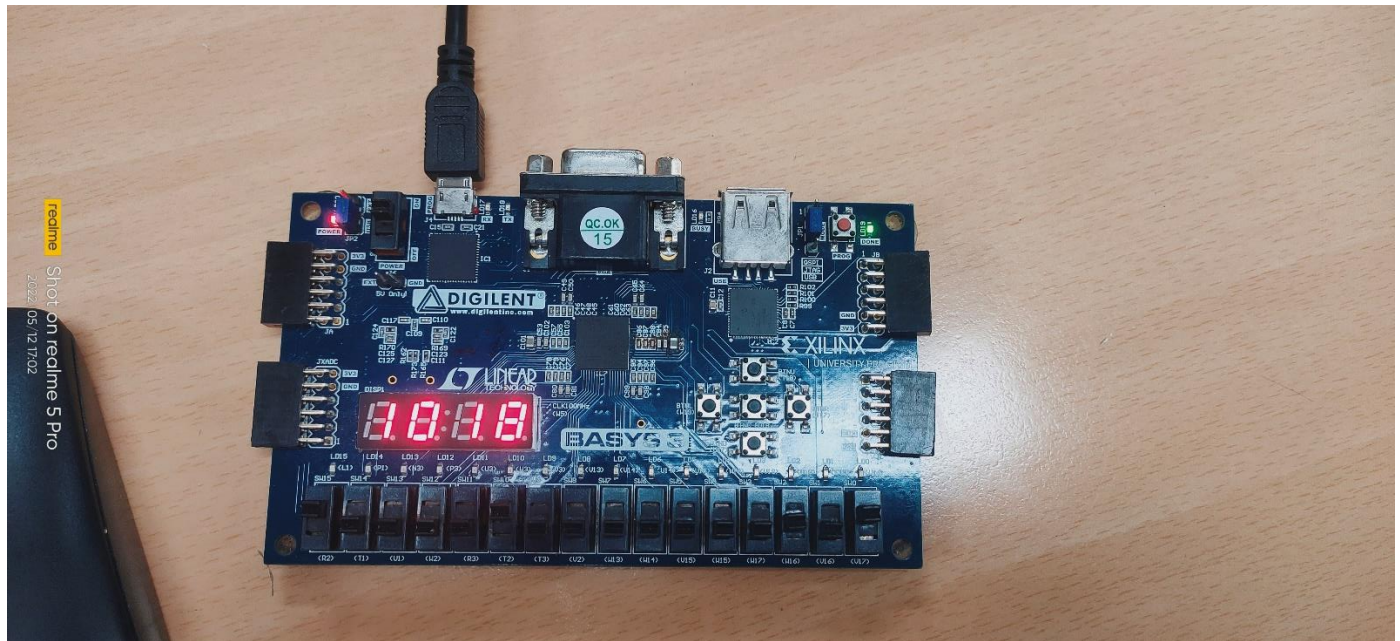
Tenth of sec and ones position of sec-



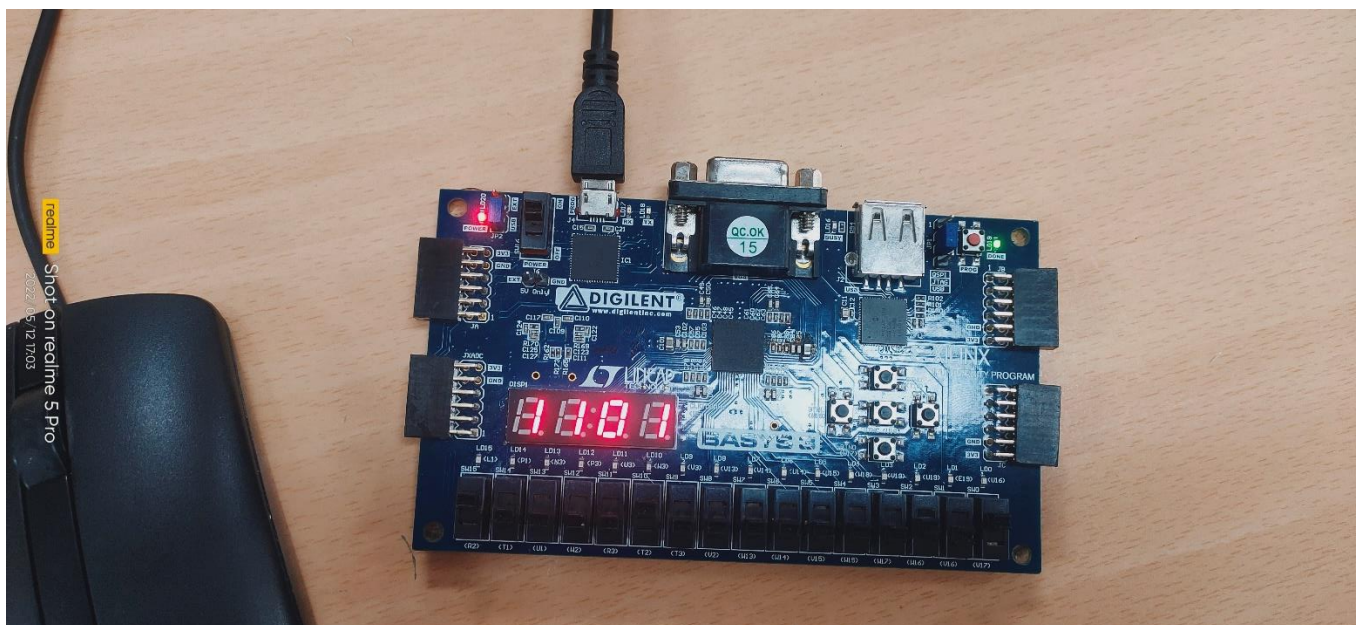
10th position of sec-

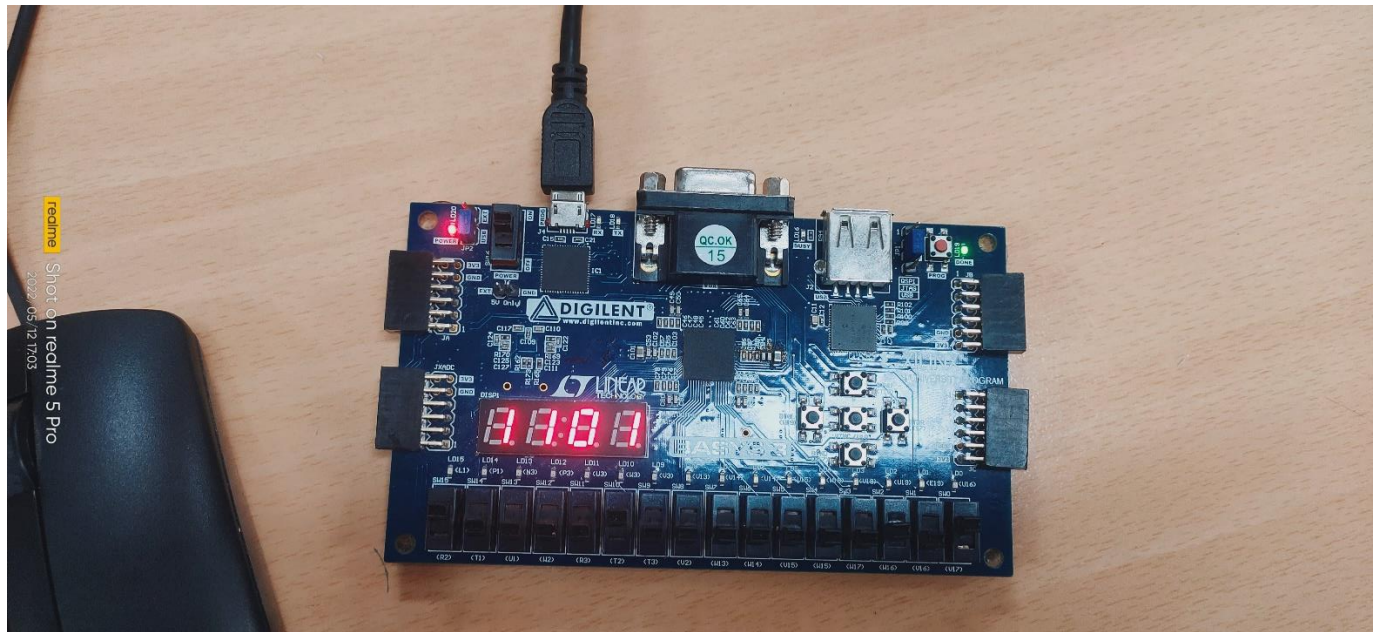


Minutes position-

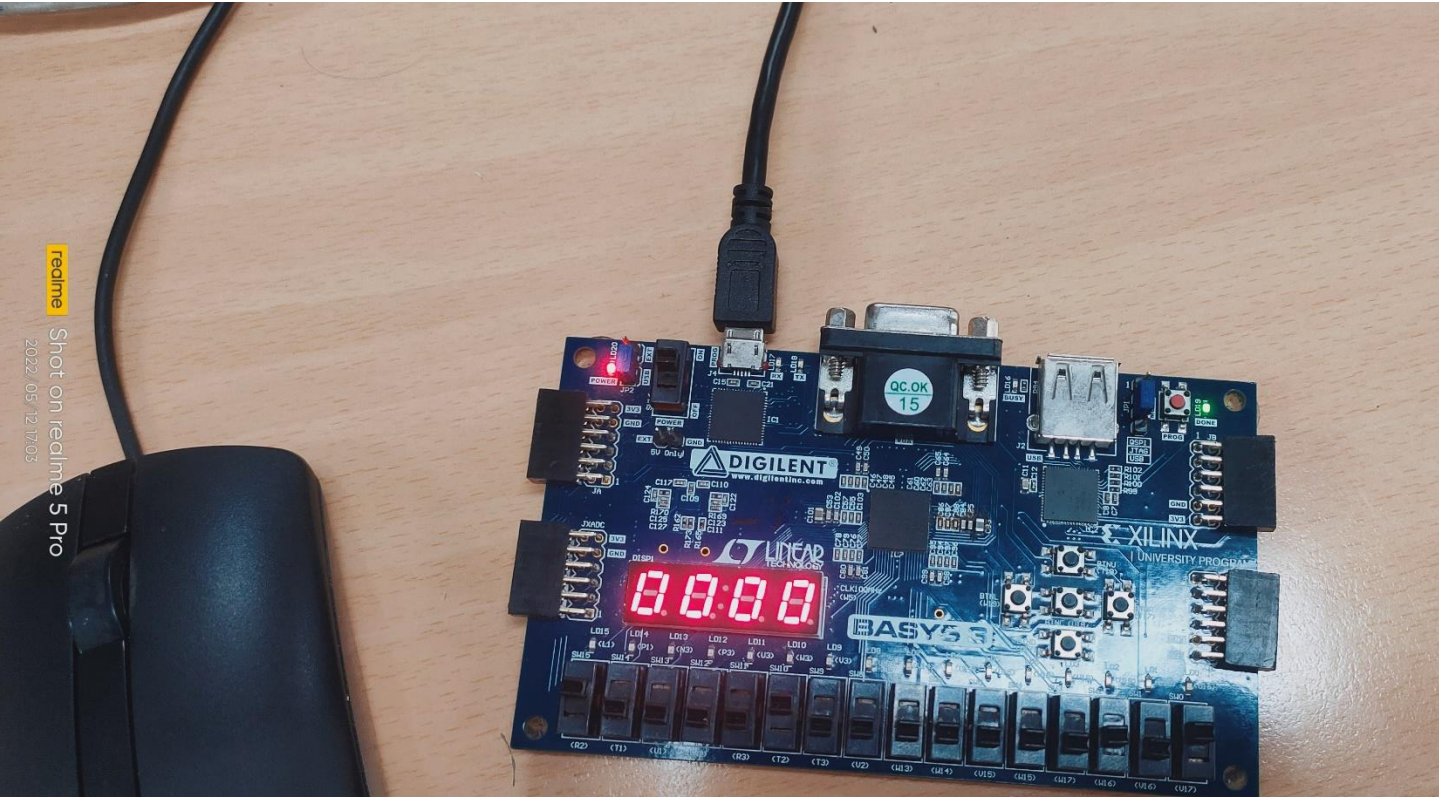


Use of pause button





Use of reset button-

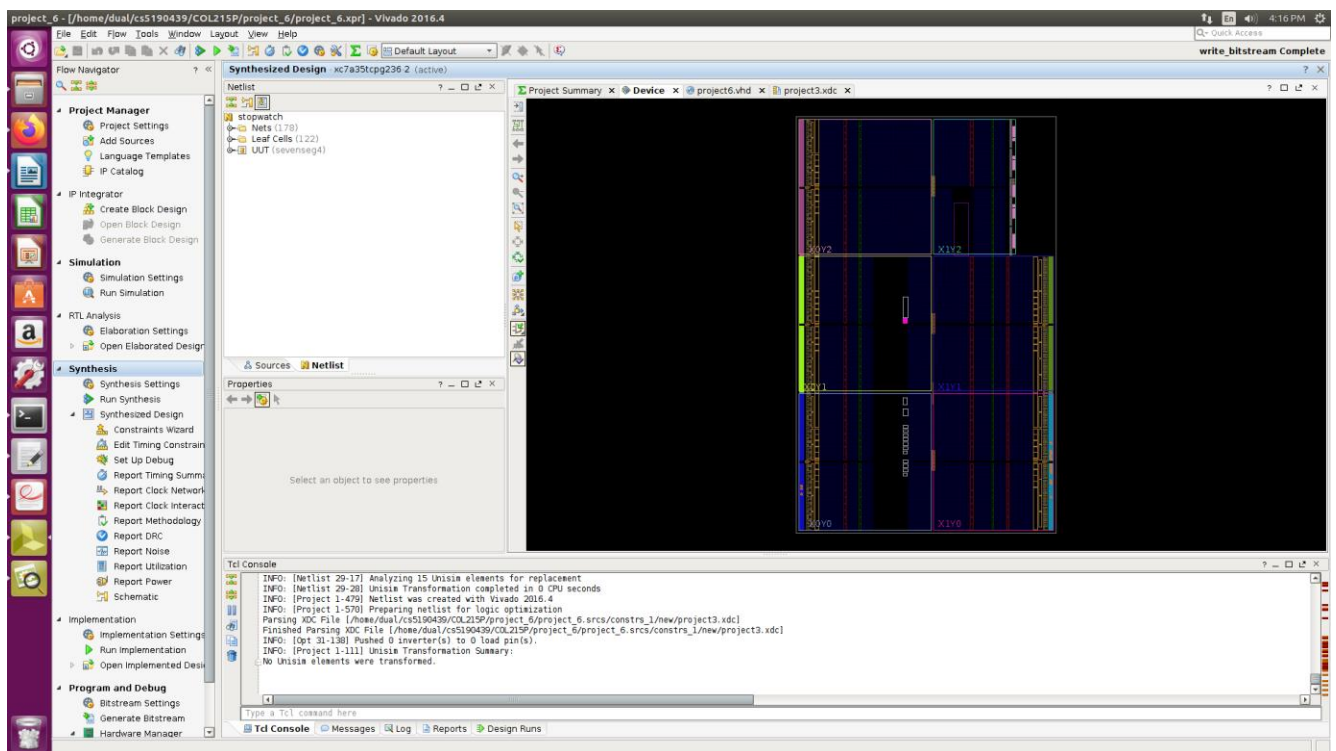


redmi

Shot on redmi 5 Pro

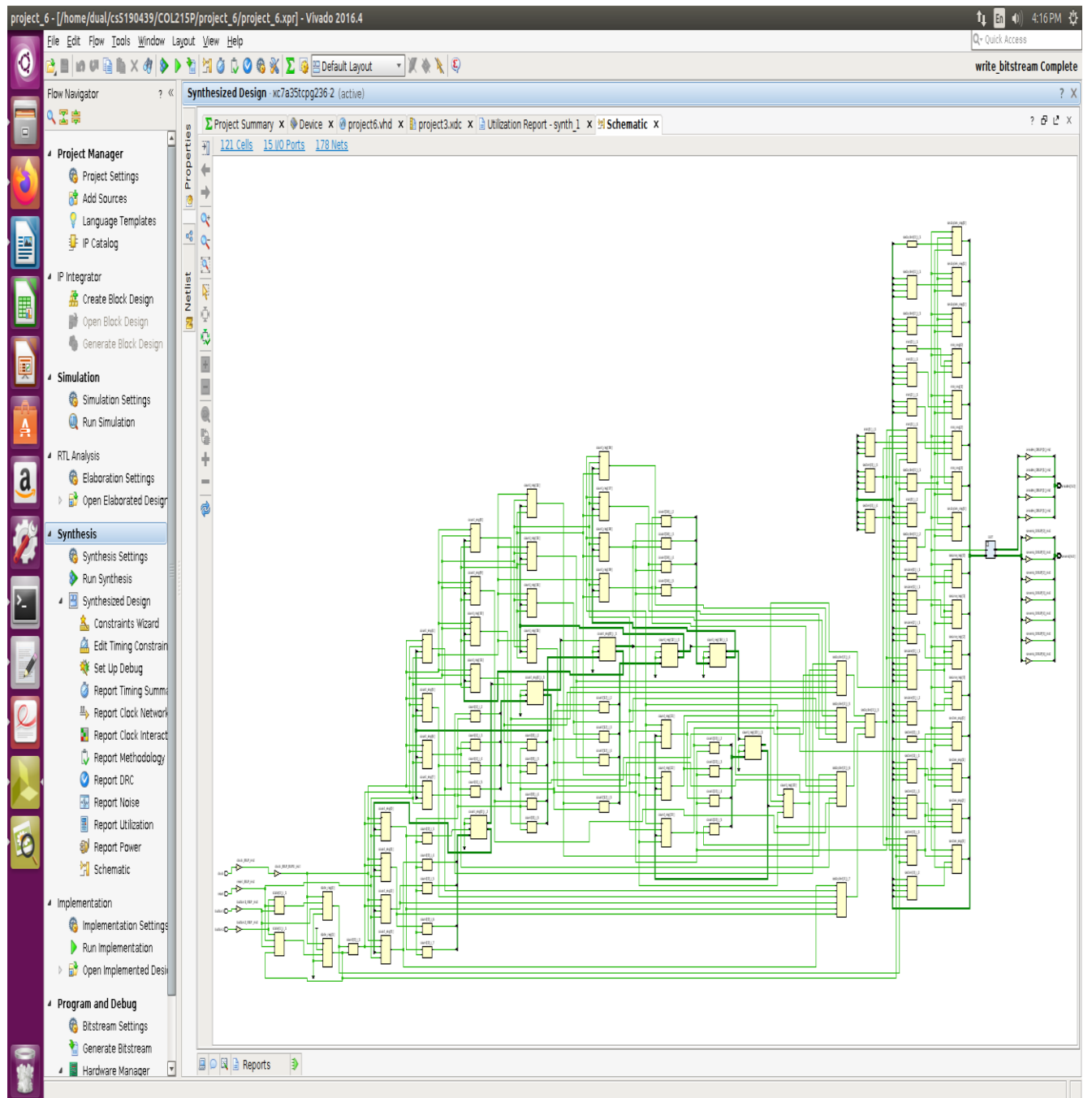
2022/05/12 17:03

Device view-



SCHEMATIC VIEW-

Here is the circuit



Thank you!