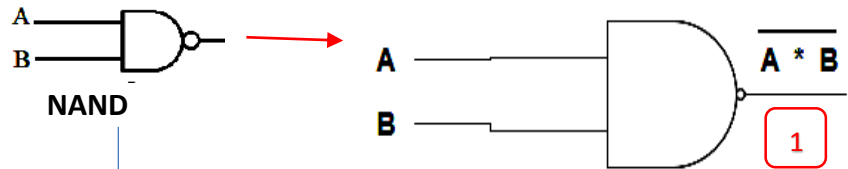
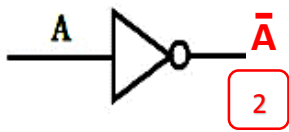


***AUDIO MATERIAL***  
***-CS-UNIT-3-***  
***Introduction to Boolean Algebra.***  
***Part 3***

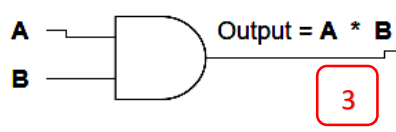
1. Implementation given function only using NAND gates.



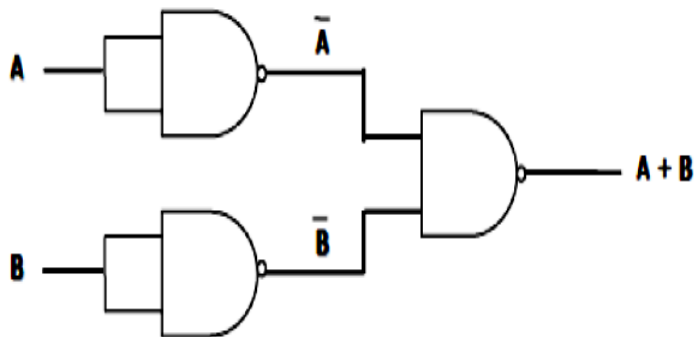
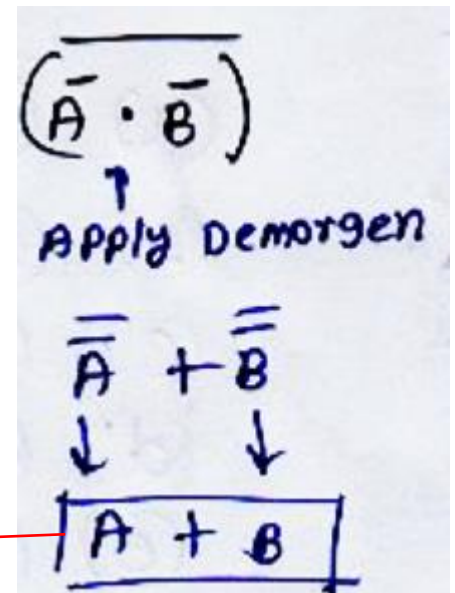
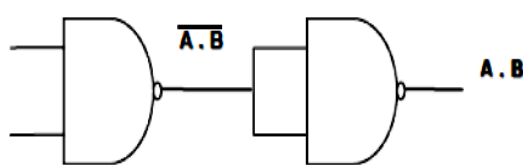
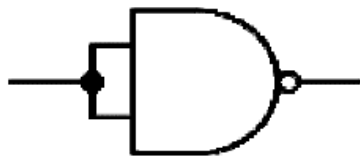
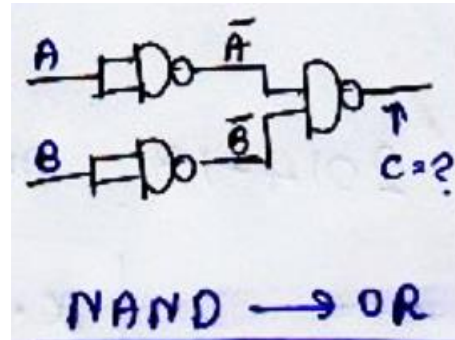
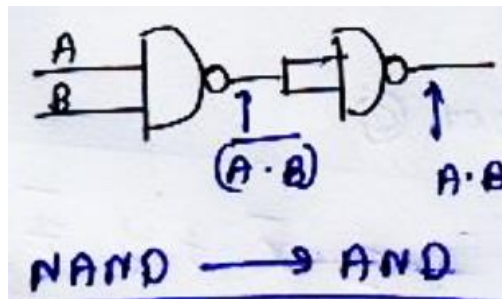
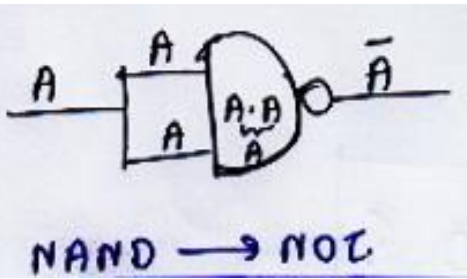
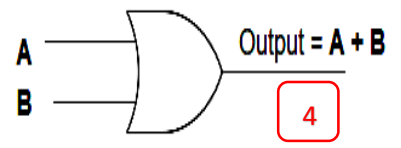
NOT



AND

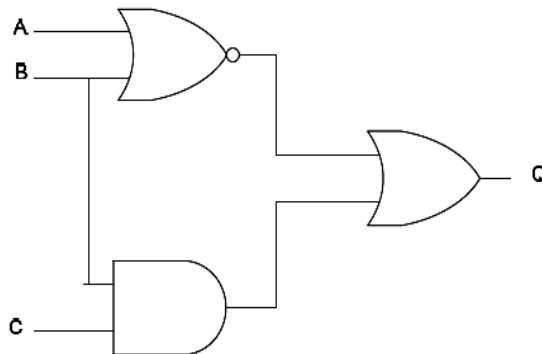


OR



2011-15

- 15) How many NAND gates are required if each of the gates in the following logic circuit is to be replaced directly by a combination of NAND gates only?



(a) 6.

(b) 7.

(c) 8.

(d) 9.

(e) 10.

2011-15

OR + NOT → NOR

↑ AND

↑ OR.

Required All gates → 9

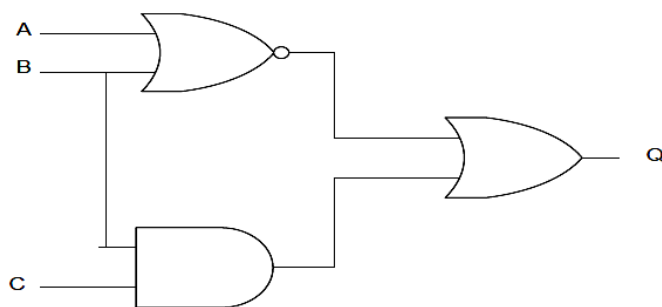
After the Reducing,  
↓ 8

Answer (d)

replace the circuit using NAND gates.

2015-15

- 15) How many NAND gates are required for the following logic circuit, if it is to be implemented only using NAND gates?



(a) 3

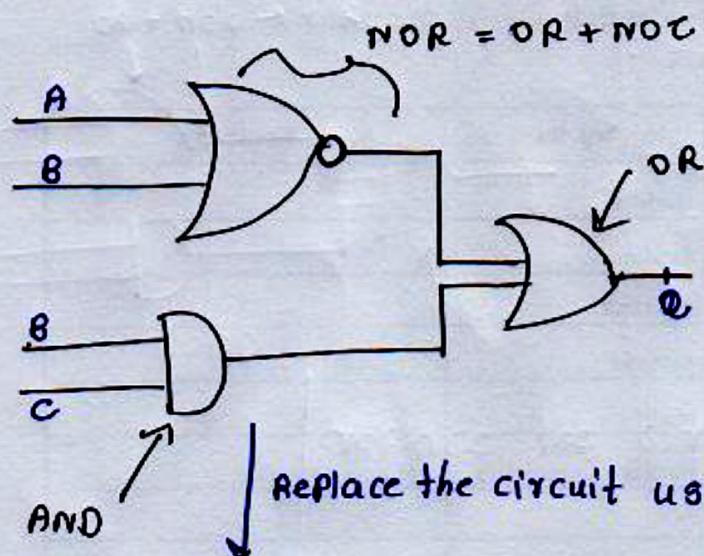
(b) 4

(c) 5

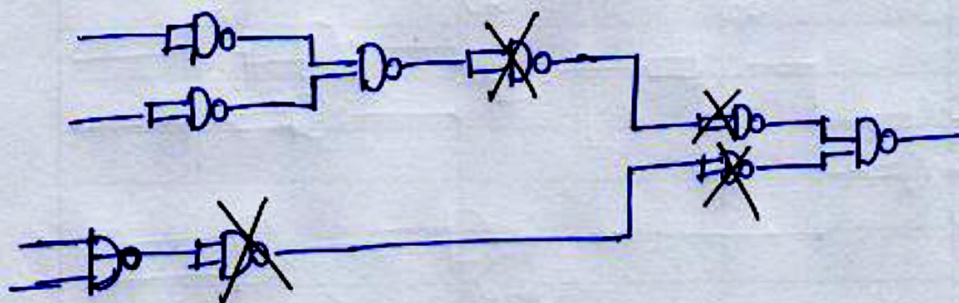
(d) 6

(e) 9

[2015-15]



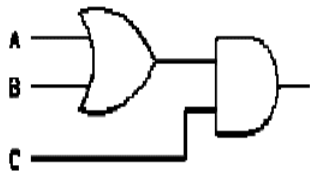
Replace the circuit using NAND gates.

Required all gates  $\rightarrow 9$ After the Reducing  $\rightarrow 5$ 

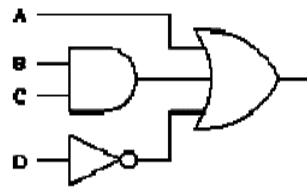
Answer @@



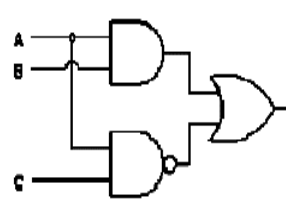
## 2. Check answers with diagram,



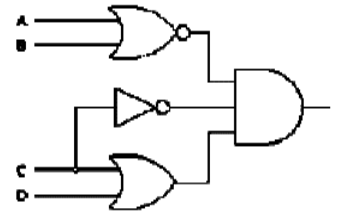
$$X = (A + B)C$$



$$X = A + (B.C) + \bar{D}$$



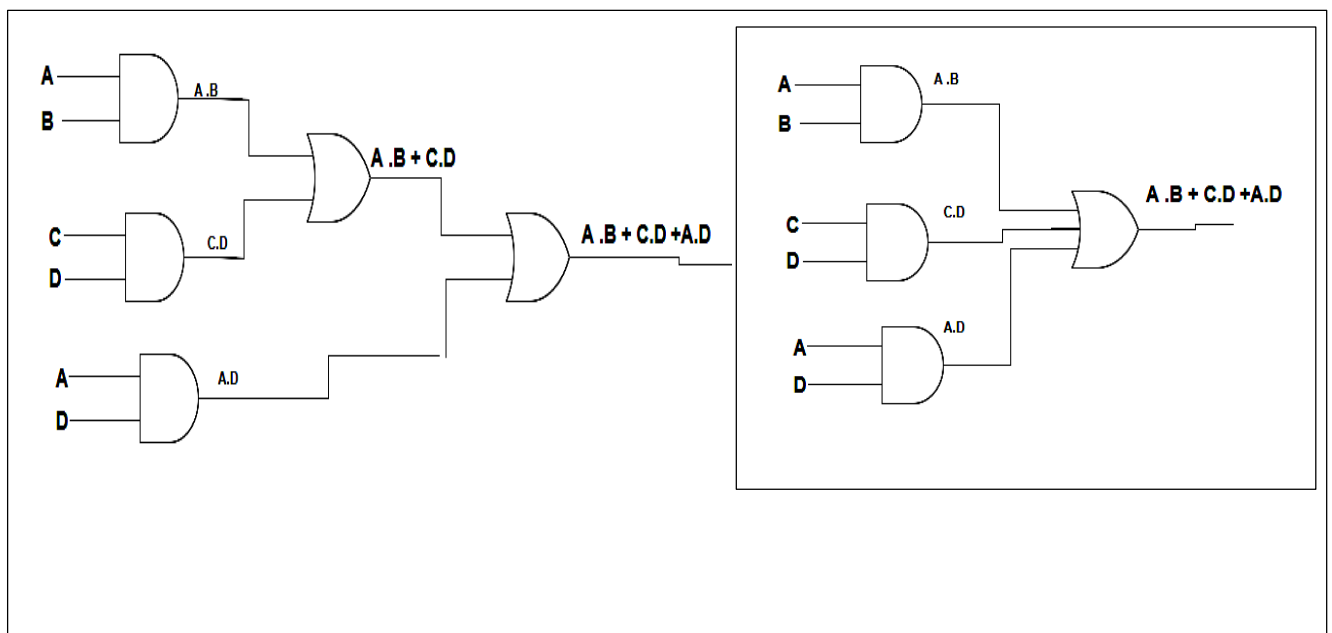
$$X = (A.B) + (\overline{A.C})$$



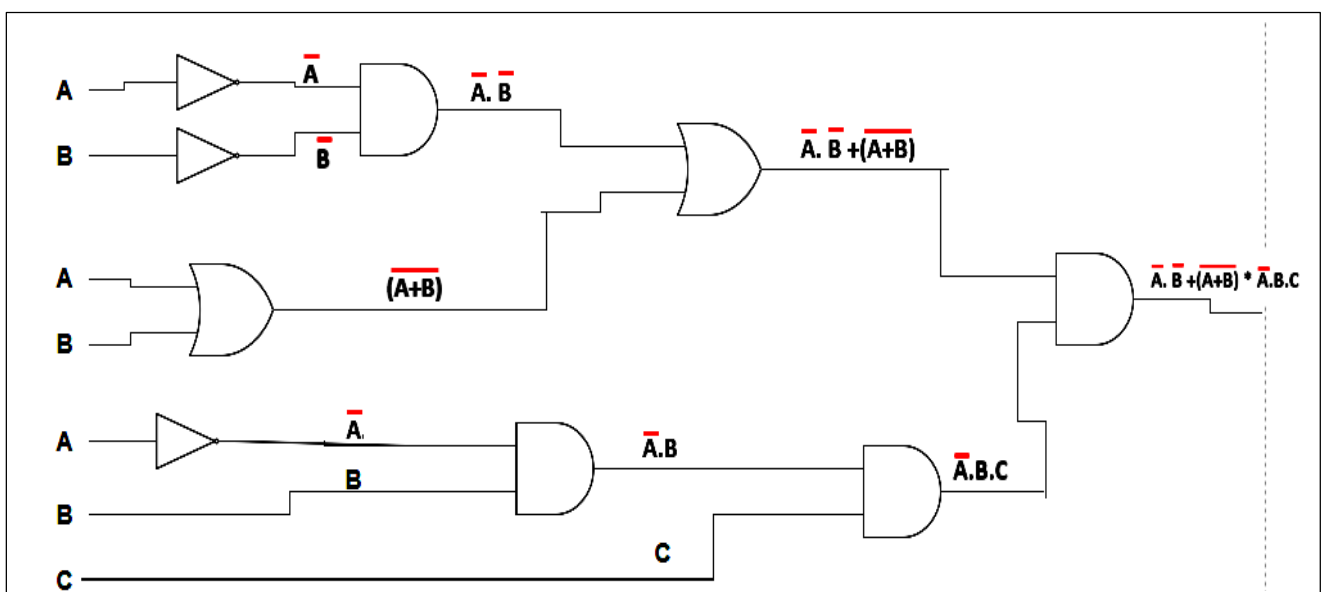
$$X = (\overline{A + B}).(C + D).\bar{C}$$

## 3. Drawing Logic Gate System (Circuit) According to Equation.

### a. $AB + CD + AD$



### b. $\bar{A}.\bar{B} + (\overline{A+B}) * \bar{A}.B.C$



c.  $\overline{A.B.C} + (A+BC) * A.B$

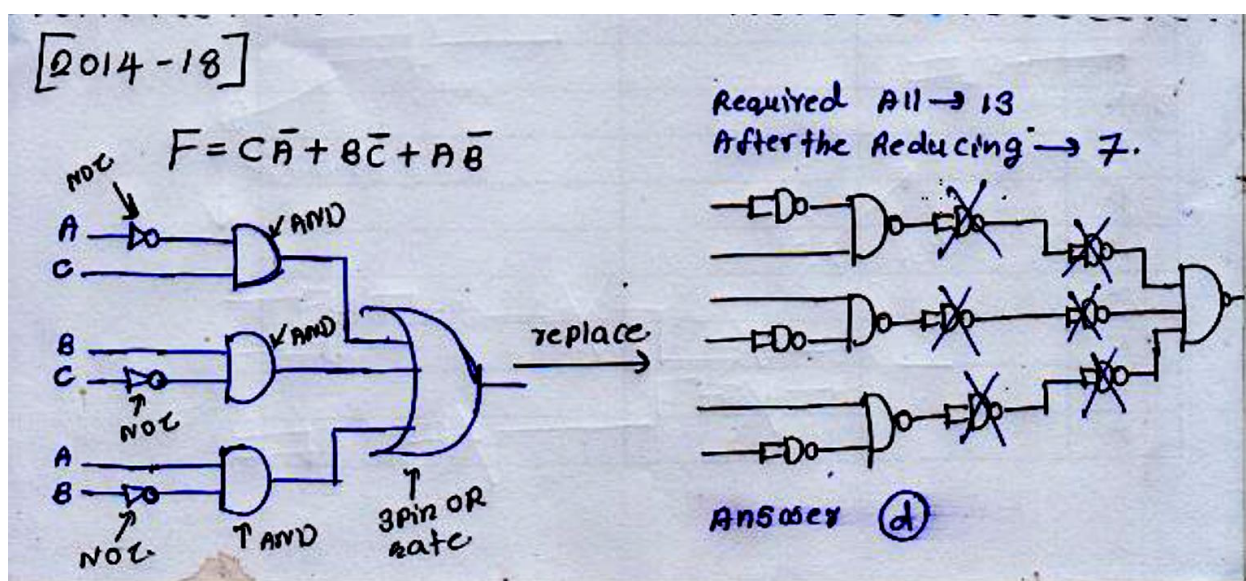


2014-18

- 18) How many NAND gates are required for the logic function F, if it is to be implemented using NAND gates only?

$$F = C\bar{A} + B\bar{C} + A\bar{B}$$

- |       |       |       |
|-------|-------|-------|
| (a) 4 | (b) 5 | (c) 6 |
| (d) 7 | (e) 8 |       |



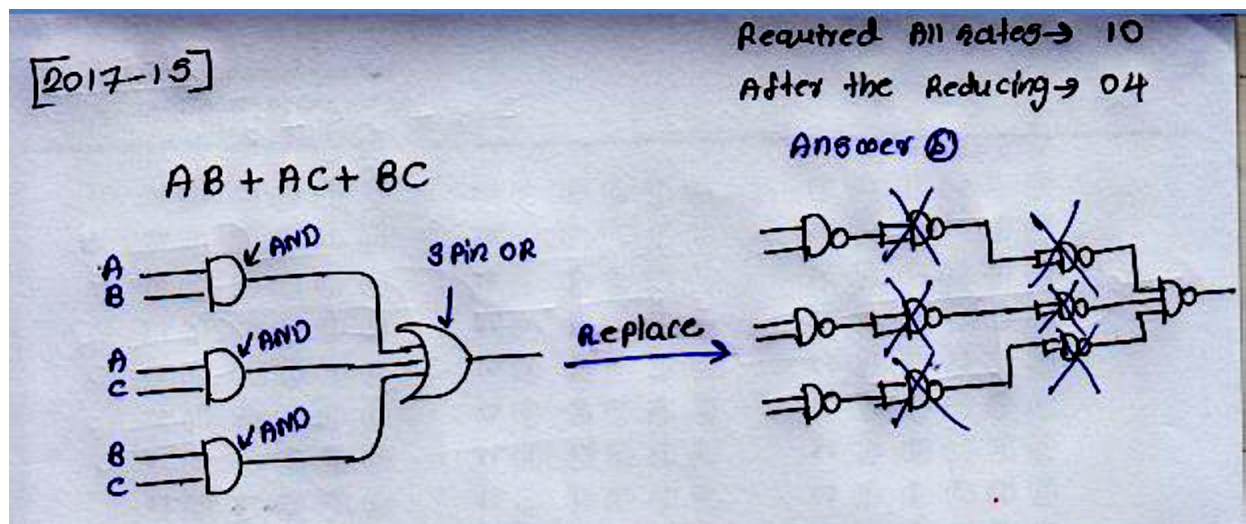
2017-15

- 15) Consider the following Boolean function

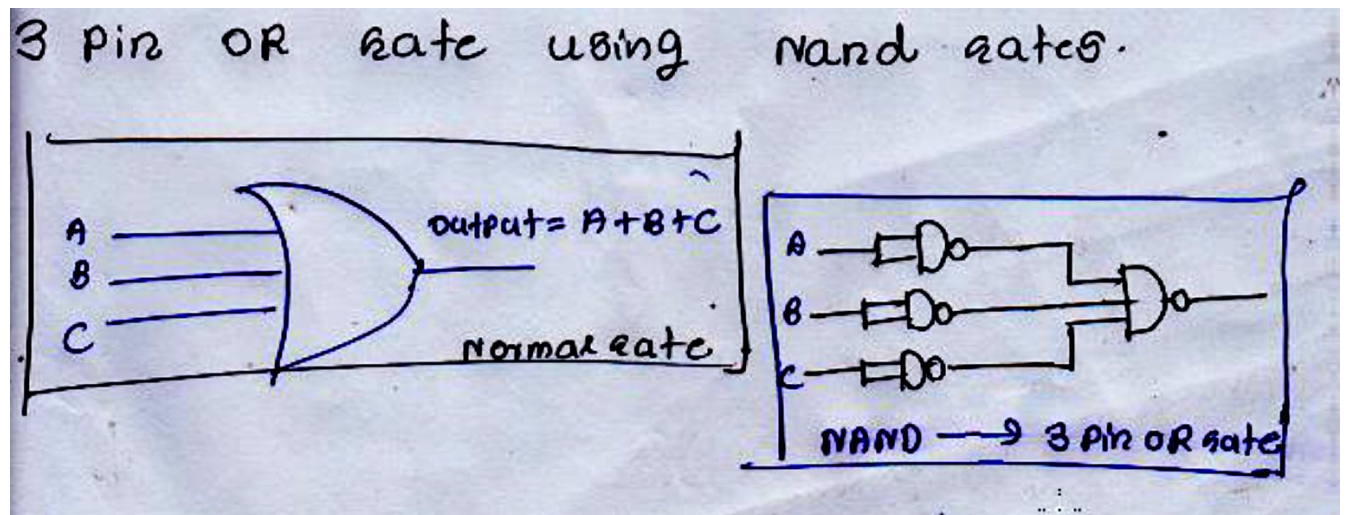
$$F(A, B, C) = (A.B) + (A.C) + (B.C)$$

How many NAND gates are required for the above Boolean function, if it is to be implemented only using NAND gates?

- |       |       |       |
|-------|-------|-------|
| (a) 3 | (b) 4 | (c) 5 |
| (d) 6 | (e) 7 |       |



NOTE:-



NEXT TUTE  $\rightarrow$  KMAP.