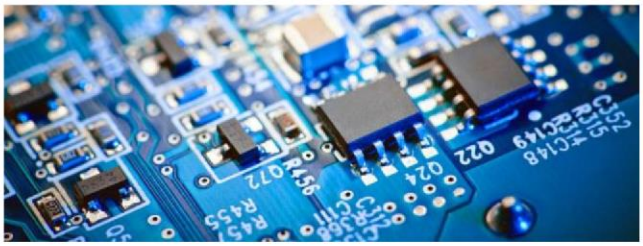
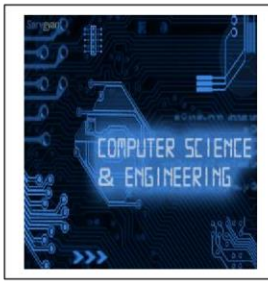
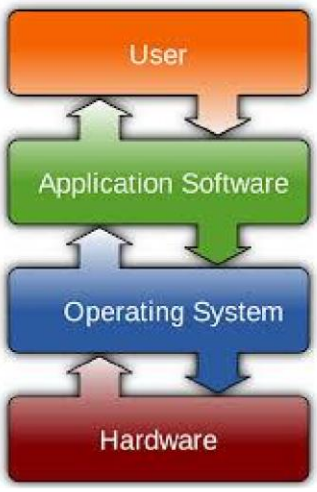
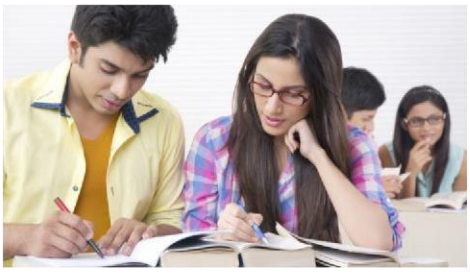
COMPUTER SYSTEM -I-Processor Architecture.

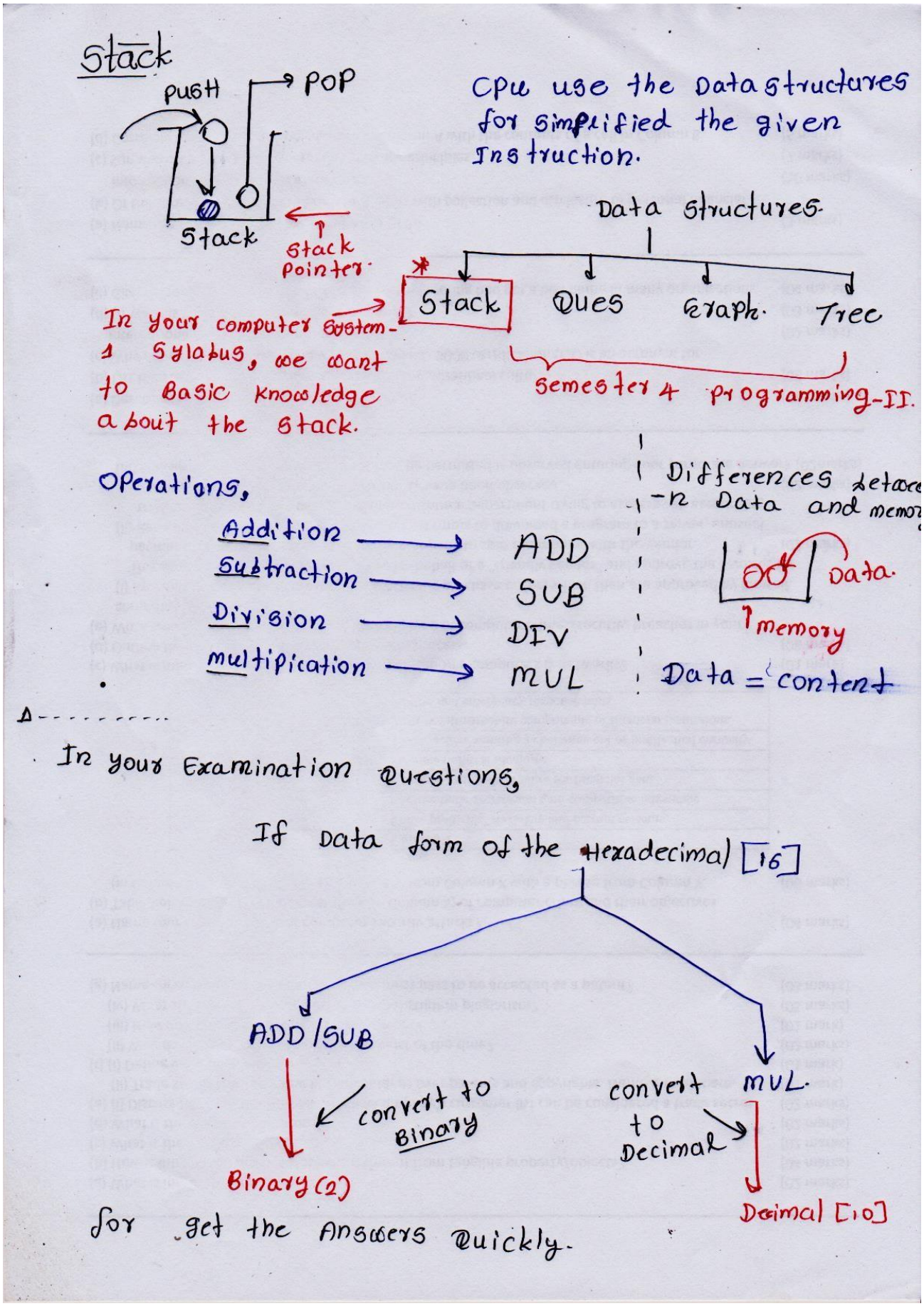






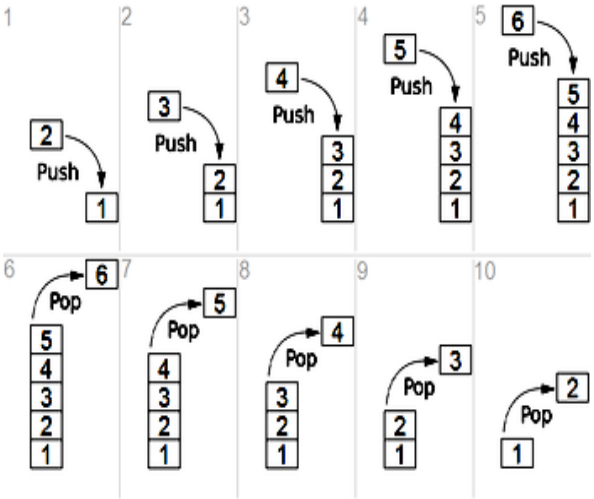


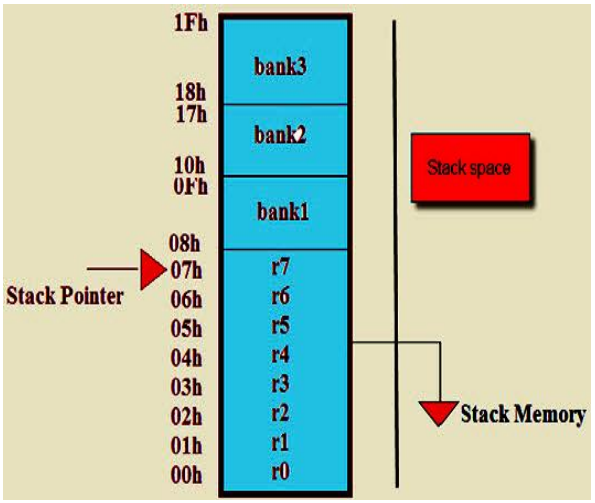
Stack base questions.

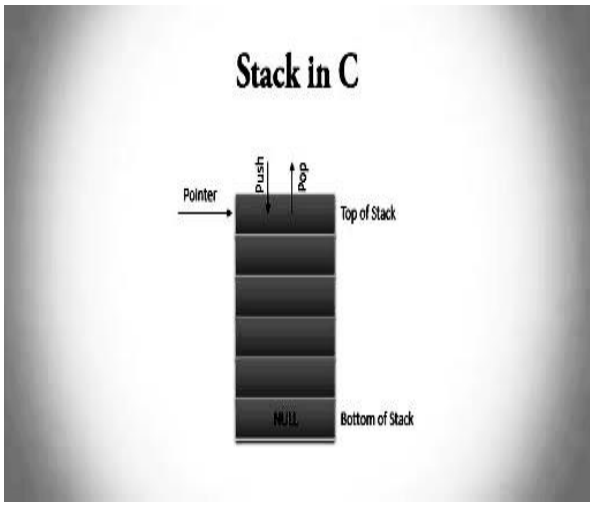


❖ Stack pointer

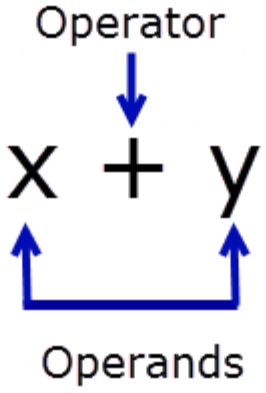
A stack pointer is a small register that stores the address of the last program request in a stack. A stack is a specialized buffer which stores data from the top down. As new requests come in, they "push down" the older ones. The most recently entered request always resides at the top of the stack, and the program always takes requests from the top.







❖ Operator vs Operands.



2010-19

19) A stack-based processor executes the following set of machine instructions sequentially.

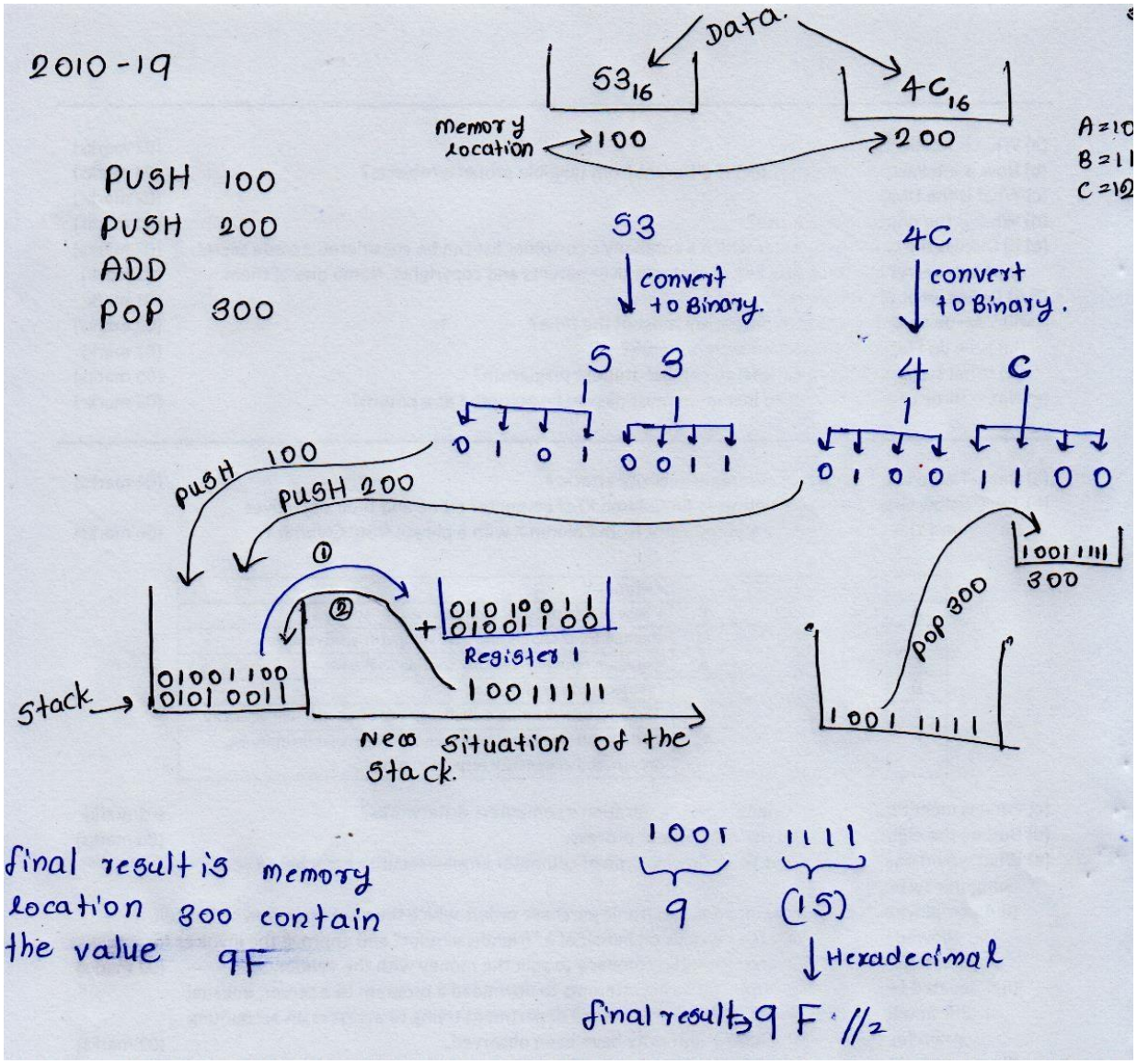
```
PUSH 100
PUSH 200
ADD
POP  300
```

Assuming that

(i) memory location 100 contains the value 53 (Hex) and memory location 200 contains the value 4C (Hex),
(ii) the stack is byte organised and the stack pointer is at 00FF, and that
(iii) all PUSH and POP instructions have a memory operand,

Which of the following could the final result be?

(a)	Memory location 300 contains the value 9F
(b)	Memory location 00FD contains the value 9F
(c)	Memory location 00FF contains a value 100
(d)	Memory location 00FE contains a value 200
(e)	Memory location 00FD contains a value 300



. **2011-21**

21) A stack-based processor executes the following set of machine instructions sequentially.

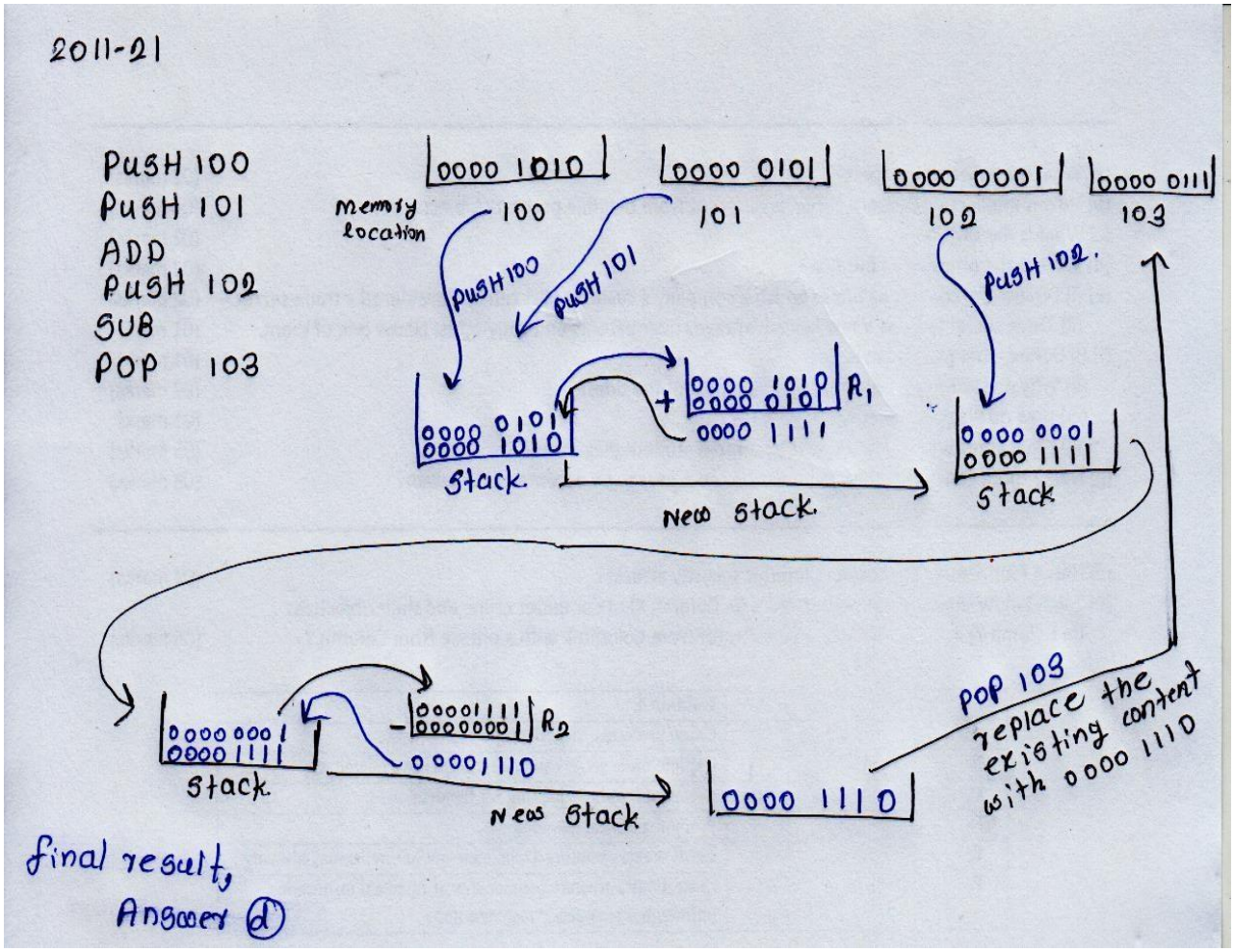
```
PUSH    100
PUSH    101
ADD
PUSH    102
SUB
POP     103
```

Assuming that:

I. Variables 0000 1010, 0000 0101, 0000 0001 and 0000 0111 are stored at memory locations 100, 101, 102 and 103 respectively,
II. The stack is byte organized and stack pointer is at 00H, and
III. All PUSH and POP instructions have a memory operand,

which of the following could be the final result?

(a) Memory location 01H contains the value 0000 0111.
(b) Memory location 02H contains the value 103.
(c) Memory location 00H contains the value 103.
(d) Memory location 103 contains the value 0000 1110.
(e) Memory location 103 contains the value 0000 0111.



2015-20

20) A stack-based architecture processor executes the following set of machine instructions sequentially.

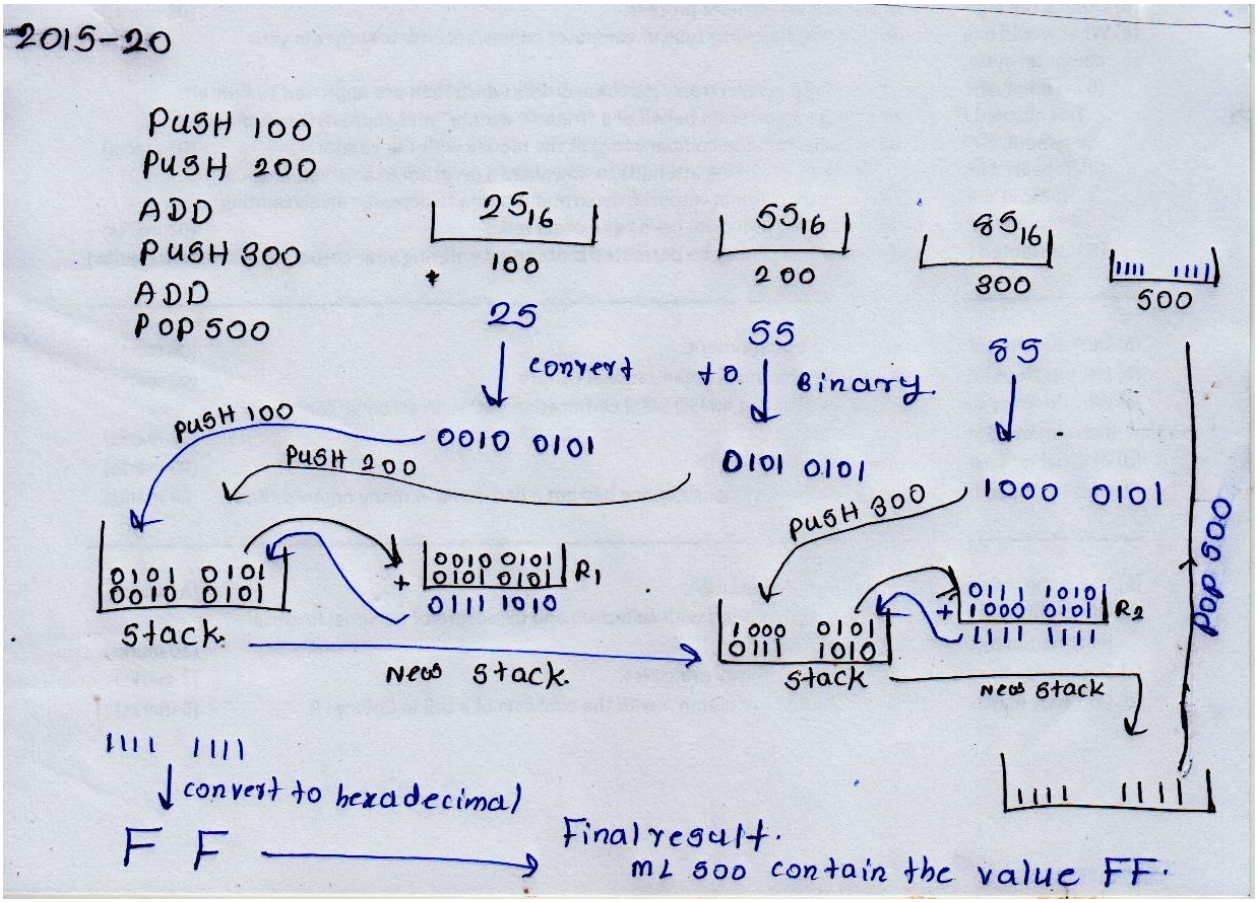
```
PUSH 100
PUSH 200
ADD
PUSH 300
ADD
POP  500
```

Assume that

- *Memory locations 100, 200 and 300 contains the values25, 55 and 85 respectively in hexadecimals.*
- *The stack is byte organized and the stack pointer is at 00FD, and that*
- *All PUSH and POP instructions have a memory operand.*

Which of the following could the final result be?

(a) Memory location 300 contains the value 4A
(b)Memory location 500 contains the value FF
(c)Memory location 00FD contains a value 100
(d)Memory location 00FE contains a value 200
(e)Memory location 00FF contains a value 300



2016-21

21) A stack-based architecture processor executes the following set of machine instructions sequentially.

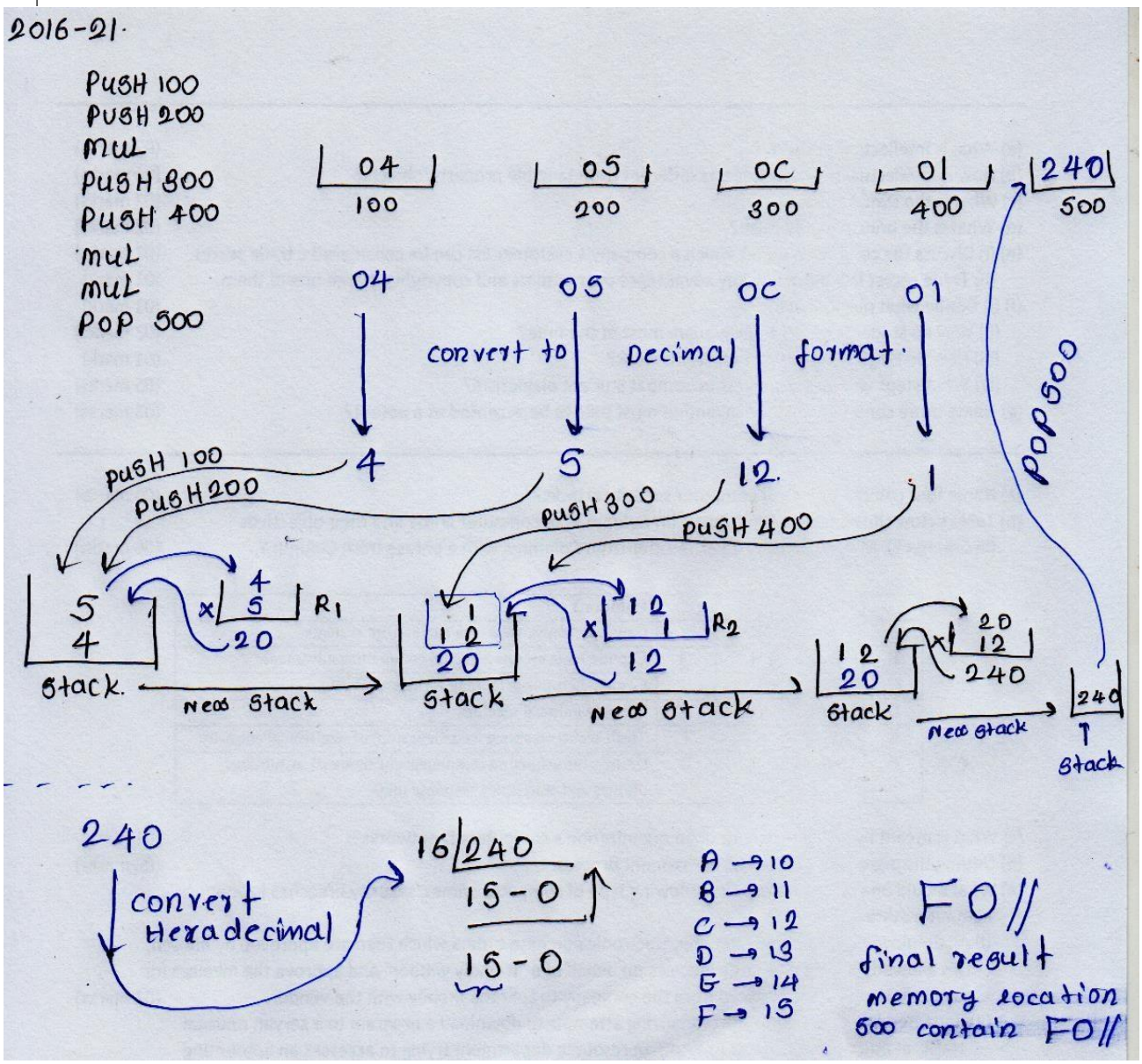
```
PUSH 100
PUSH 200
MUL
PUSH 300
PUSH 400
MUL
MUL
POP  500
```

Assume that

- *Memory locations 100, 200, 300 and 400 contain the values 04, 05, 0C and 01 respectively in hexadecimals.*
- *The stack is byte organized, the stack pointer is at 00FD and*
- *A PUSH and POP instructions have a memory operand.*

Which of the following could the final result be?

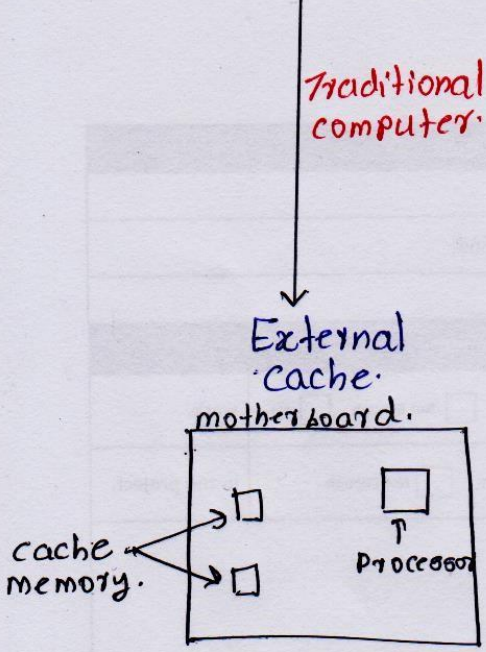
(a) Memory location 500 contains the value 0F
(b) Memory location 500 contains the value FF
(c) Memory location 500 contains the value F0
(d) Memory location 500 contains the value 14
(e) Memory location 500 contains the value 0C

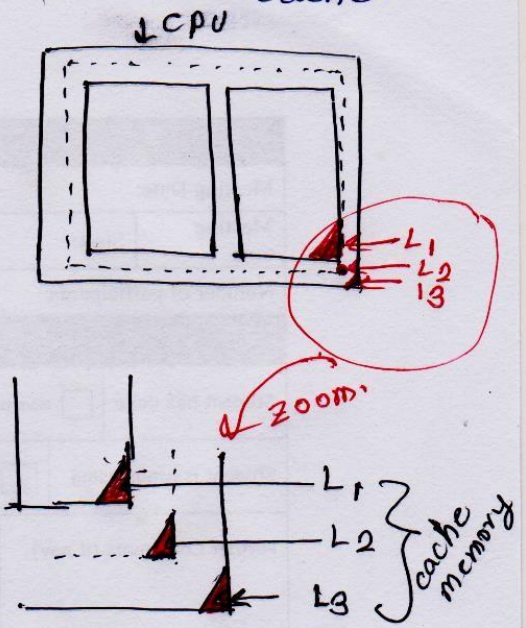


Cache Memory.

A cache memory, → modern day computers → Internal cache.

Traditional computer.





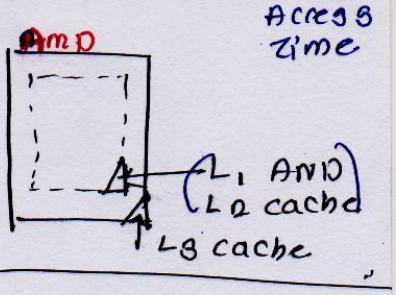
(I) capacity $L_1 < L_2 < L_3$ ← always true

(II) Accessing time,

Registers < cache memory < RAM

$L_1 < L_2 < L_3$ → always not true

- some AMD processors, L_1 access time = L_2 access time



(III) unit price,

cache > RAM > Hard disk.

(IV) L_1 cache memory → on chip

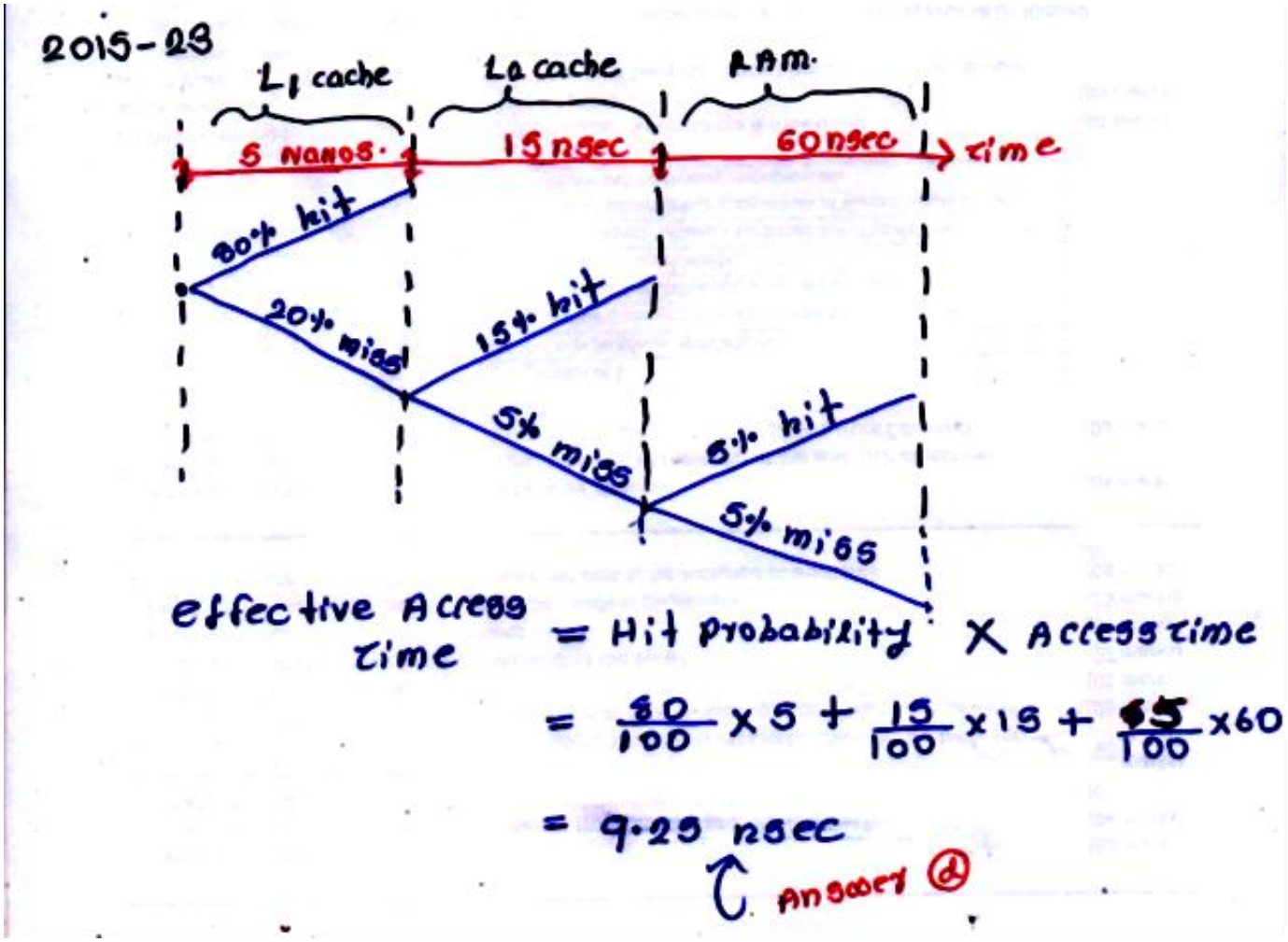
L_2 cahe memory, L_3 cache memory } off chip.

(V) → we define a cache miss to be caused by a reference to an item that is not resident in cache memory.

2015-23

23) A computer has a two-level cache. Suppose that 80% of the memory references hit on the first level cache, 15% on the second level cache, and 5% miss. The access times are 5 nano seconds (nsec) for the first level cache, 15 nsec for the second level and 60 nsecfor the main memory reference respectively. What is the effective access time?

(a) 2.25 nsec	(b) 5.25 nsec	(c) 6.25 nsec
(d) 9.25 nsec	(e) 10.75 nsec	



Addressing modes.

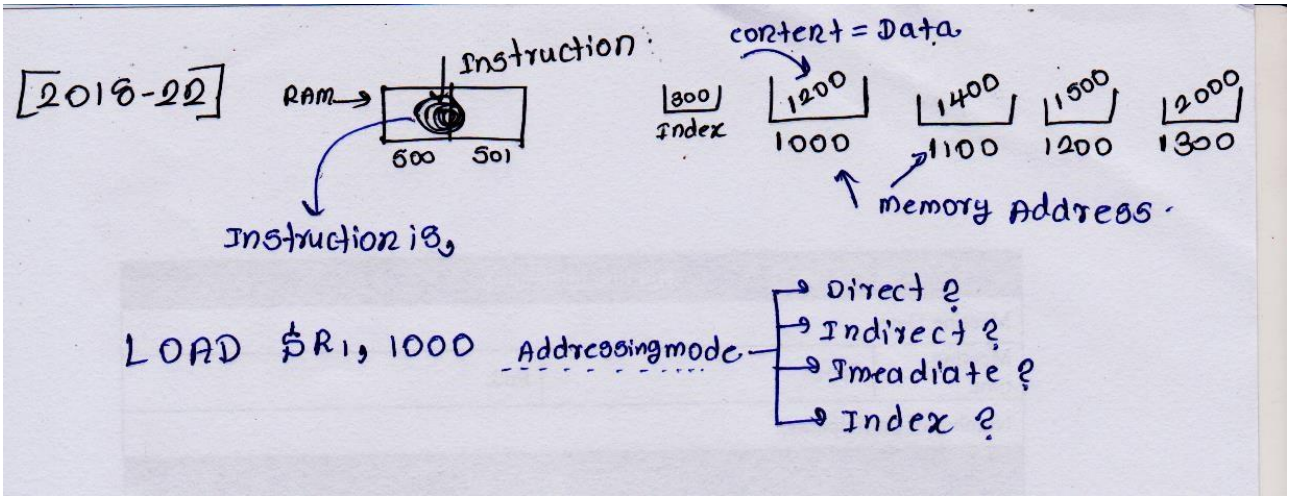
Instruction is made by,

An Instruction = OP code + Memory Address + Register Address +Addressing modes + etc..

2018-22

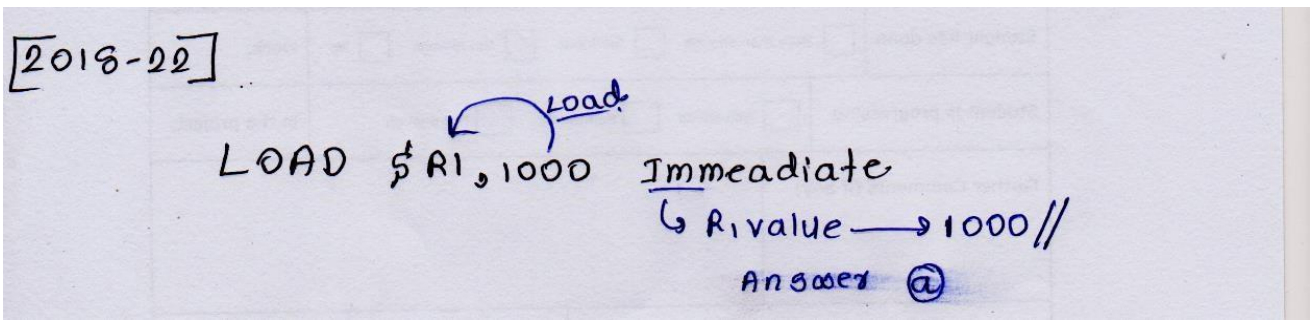
Questions 22, 23, 24 and 25 are based on the following:

A two-word instruction is stored in memory at address 500 and 501.The instruction is **LOAD $R1, 1000**. The contents of memory addresses 1000, 1100, 1200 and 1300 are 1200, 1400, 1500 and 2000 respectively. The content of indexed (base) register is 300.



22) What is the value loaded into register $R1 after the execution of the instruction, if the addressing mode is Immediate?

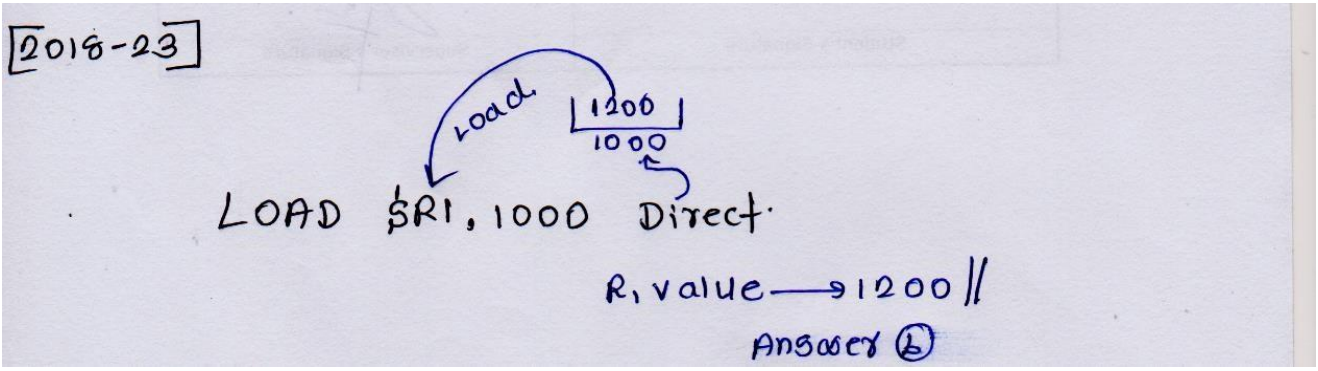
(a) 1000	(b) 1200	(c) 1400
(d) 1500	(e) 2000	



2018-23

23) What is the value loaded into register $R1 after the execution of the instruction, if the addressing mode is Direct?

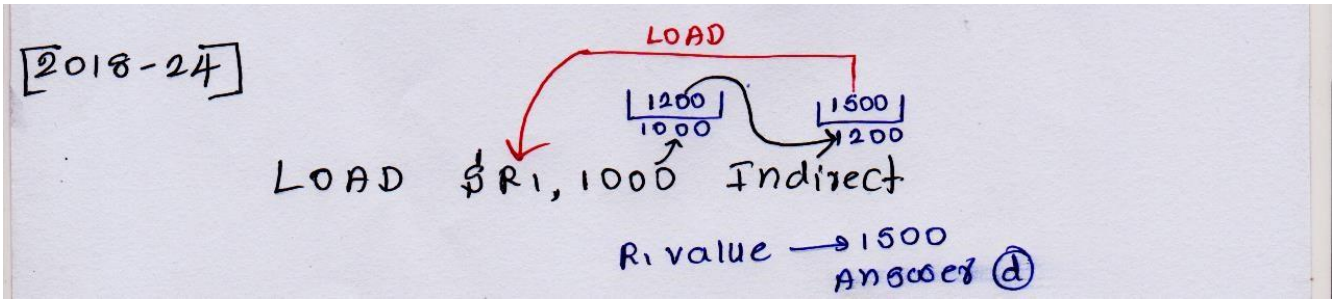
(a) 1000	(b) 1200	(c) 1400
(d) 1500	(e) 2000	



2018-24

24) What is the value loaded into register $R1 after the execution of the instruction, if the addressing mode is Indirect?

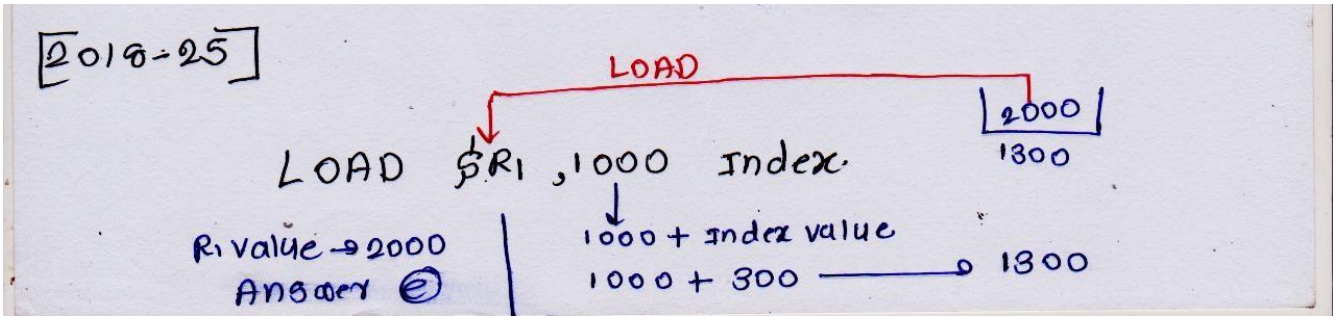
(a) 1000	(b) 1200	(c) 1400
(d) 1500	(e) 2000	



2018-25

25) What is the value loaded into register $R1 after the execution of the instruction, if the addressing mode is Indexed (Base)?

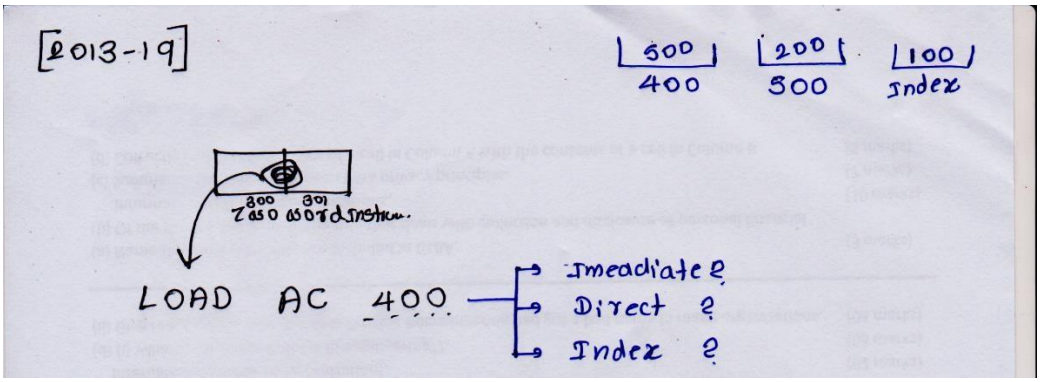
(a) 1000	(b) 1200	(c) 1400
(d) 1500	(e) 2000	



2013-19

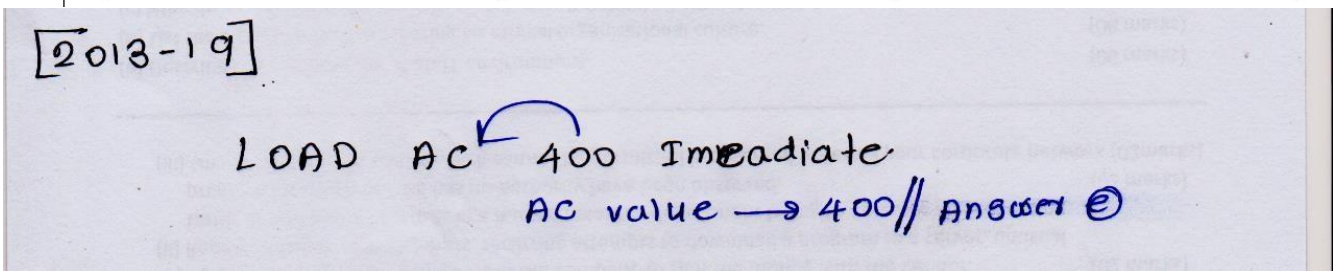
Questions 19, 20 and 21 based on the following:

A two- word instruction is stored in memory at addresses 300 and 301 respectively. The instruction is "load to AC (Accumulator)". The first word of the instruction specifies the operation code and address mode, and the second word specifies the operand part. The operand has the value 400. The content of memory addresses 400 and 500 are 500 and 200 respectively. The content of index register R is 100



19) What is the value loaded to the AC after the execution of the instruction, if the addressing mode is Immediate?

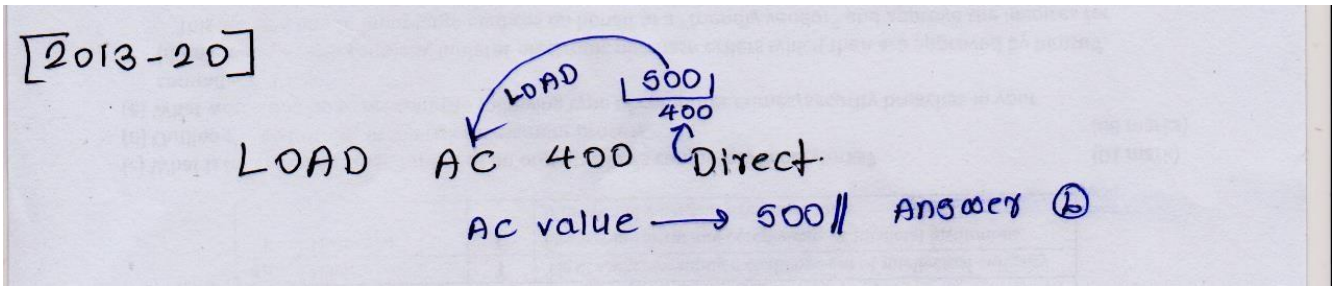
(a) 300	(b) 500	(c) 200
(d) 100	(e) 400	



2013-20

20) What is the value loaded to the AC after the execution of the instruction, if the addressing mode is Direct?

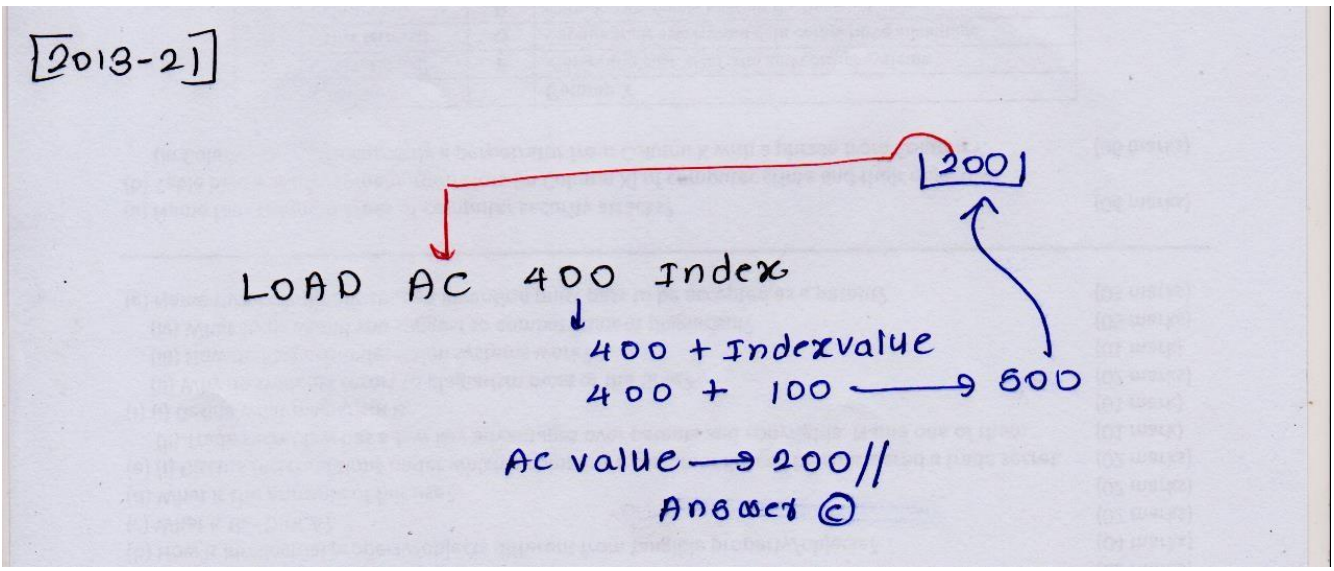
(a) 300	(b) 500	(c) 200
(d) 100	(e) 400	



2013-21

21) What is the value loaded to the AC after the execution of the instruction, if the addressing mode is Indexed?

(a) 300	(b) 500	(c) 200
(d) 100	(e) 400	



2015-19

19) On a certain machine with a single register (accumulator), the following memory locations contain the data values as indicated. For the machine instructions given, when executed, which one or more of following statement(s) are true?

Memory location	Content
0020	40
0030	50
0040	60

(i) 'LOAD IMMEDIATE' 20 will make the register value 40
(ii) 'L OAD DIRECT' 30 will make the register value 50
(iii) 'LOAD INDIRECT' 20 will make the register value 60
(iv) 'LOAD DIRECT' 30 will make the register value 30

(a) Only (ii)
(b) Only (ii) and (iv)
(c) Only (i) and (iv)
(d) Only (ii) and (iii)
(e) Only (ii), (iii) and (iv)