# STM32F745xx
# STM32F746xx

## ARM®-based Cortex®-M7 32b MCU+FPU, 462DMIPS, up to 1MB Flash/320+16+ 4KB RAM, USB OTG HS/FS, ethernet, 18 TIMs, 3 ADCs, 25 com itf, cam & LCD

**Datasheet - production data**

## Features

- Includes ST state-of-the-art patented technology
- Core: Arm® 32-bit Cortex®-M7 CPU with FPU, adaptive real-time accelerator (ART Accelerator™) and L1-cache: 4-Kbyte data cache and 4-Kbyte instruction cache, allowing 0-wait state execution from embedded flash memory and external memories, frequency up to 216 MHz, MPU, 462 DMIPS/2.14 DMIPS/MHz (Dhrystone 2.1), and DSP instructions.
- Memories
  - Up to 1 Mbyte of flash memory
  - 1024 bytes of OTP memory
  - SRAM: 320 Kbytes (including 64 Kbytes of data TCM RAM for critical real-time data) + 16 Kbytes of instruction TCM RAM (for critical real-time routines) + 4 Kbytes of backup SRAM (available in the lowest power modes)
  - Flexible external memory controller with up to 32-bit data bus: SRAM, PSRAM, SDRAM/LPSDR SDRAM, NOR/NAND memories
- Dual mode Quad-SPI
- LCD parallel interface, 8080/6800 modes
- LCD-TFT controller up to XGA resolution with dedicated Chrom-ART Accelerator™ for enhanced graphic content creation (DMA2D)
- Clock, reset and supply management
  - 1.7 V to 3.6 V application supply and I/Os
  - POR, PDR, PVD and BOR
  - Dedicated USB power
  - 4-to-26 MHz crystal oscillator
  - Internal 16 MHz factory-trimmed RC (1% accuracy)
  - 32 kHz oscillator for RTC with calibration
  - Internal 32 kHz RC with calibration
- Low-power
  - Sleep, Stop and Standby modes
  - $V_{BAT}$ supply for RTC, 32×32-bit backup registers + 4 Kbytes of backup SRAM
- 3×12-bit, 2.4 MSPS ADC: up to 24 channels and 7.2 MSPS in triple interleaved mode
- 2×12-bit D/A converters
- Up to 18 timers: up to thirteen 16-bit (1x low-power 16-bit timer available in Stop mode) and two 32-bit timers, each with up to 4 IC/OC/PWM or pulse counter and quadrature (incremental) encoder input. All 15 timers running up to 216 MHz. 2x watchdogs, SysTick timer

LQFP100 (14x14 mm)
LQFP144 (20x20 mm)
LQFP176 (24x24 mm)
LQFP208 (28x28 mm)

UFBGA176 (10x10 mm)
TFBGA216 (13x13 mm)
TFBGA100 (8x8 mm)

WLCSP143
(4.5x5.8 mm)

- General-purpose DMA: 16-stream DMA controller with FIFOs and burst support
- Debug mode
  - SWD & JTAG interfaces
  - Cortex®-M7 Trace Macrocell™
- Up to 168 I/O ports with interrupt capability
  - Up to 164 fast I/Os up to 108 MHz
  - Up to 166 5 V-tolerant I/Os
- Up to 25 communication interfaces
  - Up to 4× $I^2C$ interfaces (SMBus/PMBus)
  - Up to 4x USARTs/4 UARTs (27 Mbit/s, ISO7816 interface, LIN, IrDA, modem control)
  - Up to 6 SPIs (up to 50 Mbit/s), 3x with muxed simplex $I^2S$ for audio class accuracy via internal audio PLL or external clock
  - 2 x SAIs (serial audio interface)
  - 2 × CANs (2.0B active) and SDMMC interface
  - SPDIFRX interface
  - HDMI-CEC
- Advanced connectivity
  - USB 2.0 full-speed device/host/OTG controller with on-chip PHY
  - USB 2.0 high-speed/full-speed device/host/OTG controller with dedicated DMA, on-chip full-speed PHY and ULPI
  - 10/100 Ethernet MAC with dedicated DMA: supports IEEE 1588v2 hardware, MII/RMII
- 8- to 14-bit parallel camera interface up to 54 Mbyte/s
- True random number generator
- CRC calculation unit
- RTC: subsecond accuracy, hardware calendar
- 96-bit unique ID

**Table 1. Device summary**

| Reference | Part number |
|---|---|
| STM32F745xx | STM32F745IE, STM32F745VE, STM32F745VG, STM32F745ZE, STM32F745ZG, STM32F745IG |
| STM32F746xx | STM32F746BE, STM32F746BG, STM32F746IE, STM32F746IG, STM32F746NE, STM32F746NG, STM32F746VE, STM32F746VG, STM32F746ZE, STM32F746ZG |

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# 1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32F750x8 microcontrollers.

This document should be ready in conjunction with the *STM32F75xxx and STM32F74xxx advanced Arm®-based 32-bit MCUs* reference manual (RM0385). The reference manual is available from the STMicroelectronics website *www.st.com.*

For information on the Arm®[a] Cortex®-M7 core, refer to the Cortex®-M7 technical reference manual available from the http://www.arm.com website.

For information on the device errata with respect to the datasheet and reference manual, refer to the STM32xxx errata sheet (ES334), available on the STMicroelectronics website www.st.com.

a. Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

# 2 Description

The STM32F745xx and STM32F746xx devices are based on the high-performance Arm® Cortex®-M7 32-bit RISC core operating at up to 216 MHz frequency. The Cortex®-M7 core features a single floating point unit (SFPU) precision which supports all Arm® single-precision data-processing instructions and data types. It also implements a full set of DSP instructions and a memory protection unit (MPU) which enhances the application security.

The STM32F745xx and STM32F746xx devices incorporate high-speed embedded memories with a flash memory up to 1 Mbytes, 320 Kbytes of SRAM (including 64 Kbytes of Data TCM RAM for critical real-time data), 16 Kbytes of instruction TCM RAM (for critical real-time routines), 4 Kbytes of backup SRAM available in the lowest power modes, and an extensive range of enhanced I/Os and peripherals connected to two APB buses, two AHB buses, a 32-bit multi-AHB bus matrix and a multi layer AXI interconnect supporting internal and external memories access.

All the devices offer three 12-bit ADCs, two DACs, a low-power RTC, thirteen general-purpose 16-bit timers including two PWM timers for motor control and one low-power timer available in Stop mode, two general-purpose 32-bit timers, a true random number generator (RNG). They also feature standard and advanced communication interfaces.

- Up to four $I^2Cs$
- Six SPIs, three $I^2Ss$ in duplex mode. To achieve the audio class accuracy, the $I^2S$ peripherals can be clocked via a dedicated internal audio PLL or via an external clock to allow synchronization.
- Four USARTs plus four UARTs
- An USB OTG full-speed and a USB OTG high-speed with full-speed capability (with the ULPI),
- Two CANs
- Two SAI serial audio interfaces
- An SDMMC host interface
- Ethernet and camera interfaces
- LCD-TFT display controller
- Chrom-ART Accelerator™
- SPDIFRX interface
- HDMI-CEC

Advanced peripherals include an SDMMC interface, a flexible memory control (FMC) interface, a Quad-SPI flash memory interface, a camera interface for CMOS sensors.

The STM32F745xx and STM32F746xx devices operate in the –40 to +105 °C temperature range from a 1.7 to 3.6 V power supply. A dedicated supply input for USB (OTG_FS and OTG_HS) is available on all the packages except LQFP100 for a greater power supply choice.

The supply voltage can drop to 1.7 V with the use of an external power supply supervisor. A comprehensive set of power-saving mode allows the design of low-power applications.

The STM32F745xx and STM32F746xx devices offer devices in 8 packages ranging from 100 pins to 216 pins. The set of included peripherals changes with the device chosen.

These features make the STM32F745xx and STM32F746xx microcontrollers suitable for a wide range of applications.

- Motor drive and application control,
- Medical equipment,
- Industrial applications: PLC, inverters, circuit breakers,
- Printers, and scanners,
- Alarm systems, video intercom, and HVAC,
- Home audio appliances,
- Mobile applications, Internet of Things,
- Wearable devices: smartwatches.

## 2.1 Full compatibility throughout the family

**Table 2. STM32F745xx and STM32F746xx features and peripheral counts**

| Peripherals | | STM32F745Vx | | STM32F746Vx | | STM32F745Zx | | STM32F746Zx | | STM32F745Ix | | STM32F746Ix | | STM32F745Bx | | STM32F746Bx | | STM32F745Nx | | STM32F746Nx | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Flash memory in Kbytes | | 512 | 1024 | 512 | 1024 | 512 | 1024 | 512 | 1024 | 512 | 1024 | 512 | 1024 | 512 | 1024 | 512 | 1024 | 512 | 1024 | 512 | 1024 |
| SRAM in Kbytes | System | 320(240+16+64) | | | | | | | | | | | | | | | | | | | |
| | Instruction | 16 | | | | | | | | | | | | | | | | | | | |
| | Backup | 4 | | | | | | | | | | | | | | | | | | | |
| FMC memory controller | | Yes[1] | | | | | | | | | | | | | | | | | | | |
| Ethernet | | Yes | | | | | | | | | | | | | | | | | | | |
| Timers | General-purpose | 10 | | | | | | | | | | | | | | | | | | | |
| | Advanced-control | 2 | | | | | | | | | | | | | | | | | | | |
| | Basic | 2 | | | | | | | | | | | | | | | | | | | |
| | Low-power | 1 | | | | | | | | | | | | | | | | | | | |
| Random number generator | | Yes | | | | | | | | | | | | | | | | | | | |
| Communication interfaces | SPI / I$^2$S | 4/3 (simplex)[2] | | | | 6/3 (simplex)[2] | | | | | | | | | | | | | | | |
| | I$^2$C | 4 | | | | | | | | | | | | | | | | | | | |
| | USART/ UART | 4/4 | | | | | | | | | | | | | | | | | | | |
| | USB OTG FS | Yes | | | | | | | | | | | | | | | | | | | |
| | USB OTG HS | Yes | | | | | | | | | | | | | | | | | | | |
| | CAN | 2 | | | | | | | | | | | | | | | | | | | |
| | SAI | 2 | | | | | | | | | | | | | | | | | | | |
| | SPDIFRX | 4 inputs | | | | | | | | | | | | | | | | | | | |
| | SDMMC | Yes | | | | | | | | | | | | | | | | | | | |
| Camera interface | | Yes | | | | | | | | | | | | | | | | | | | |
| LCD-TFT | | No | | Yes | | No | | Yes | | No | | Yes | | No | | Yes | | No | | Yes | |
| Chrom-ART Accelerator™ (DMA2D) | | Yes | | | | | | | | | | | | | | | | | | | |

**Table 2. STM32F745xx and STM32F746xx features and peripheral counts (continued)**

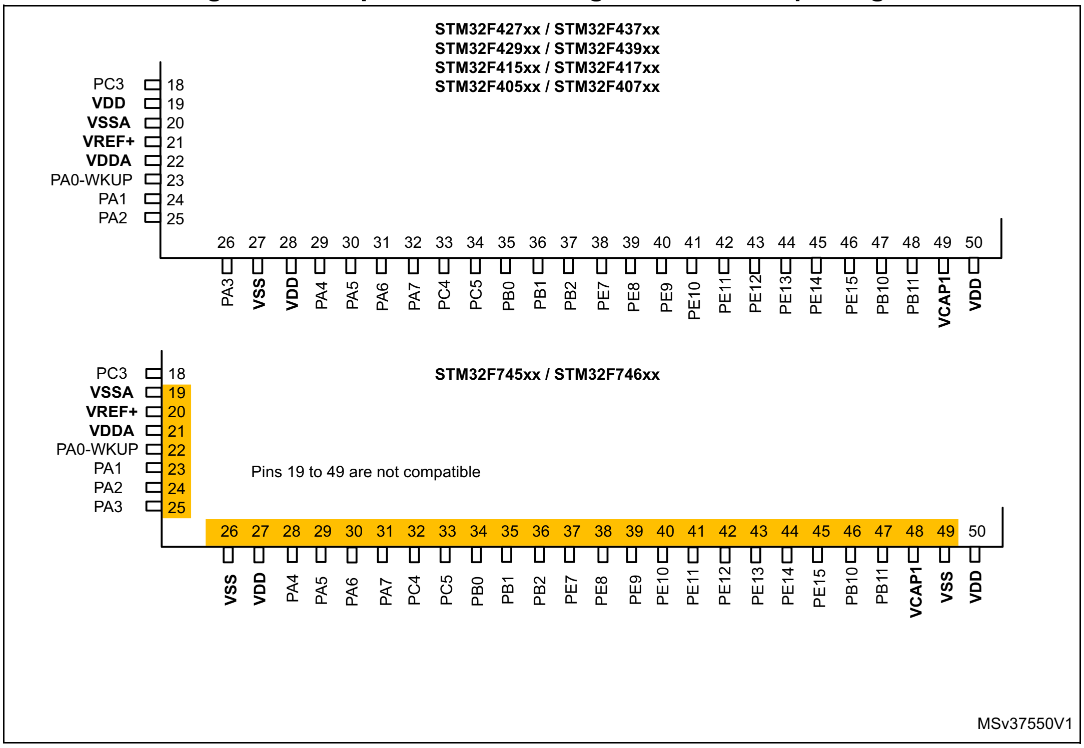
| Peripherals | STM32F745Vx | STM32F746Vx | STM32F745Zx | STM32F746Zx | STM32F745Ix | STM32F746Ix | STM32F745Bx | STM32F746Bx | STM32F745Nx | STM32F746Nx |
|---|---|---|---|---|---|---|---|---|---|---|
| GPIOs | 82 | | 114 | | 140 | | 168 | | | |
| 12-bit ADC | 3 | | | | | | | | | |
| Number of channels | 16 | | 24 | | | | | | | |
| 12-bit DAC<br>Number of channels | Yes<br>2 | | | | | | | | | |
| Maximum CPU frequency | 216 MHz(3) | | | | | | | | | |
| Operating voltage | 1.7 to 3.6 V(4) | | | | | | | | | |
| Operating temperatures | Ambient temperatures: –40 to +85 °C /–40 to +105 °C(5) | | | | | | | | | |
| | Junction temperature: –40 to + 125 °C | | | | | | | | | |
| Package | LQFP100<br>TFBGA100 | | WLCSP143<br>LQFP144 | | UFBGA176<br>LQFP176 | | LQFP208 | | TFBGA216 | |

1. For the LQFP100 package, only FMC Bank1 is available. Bank1 can only support a multiplexed NOR/PSRAM memory using the NE1 Chip Select.
2. The SPI1, SPI2 and SPI3 interfaces give the flexibility to work in an exclusive way in either the SPI mode or the I2S audio mode.
3. 216 MHz maximum frequency for -40°C to + 85°C ambient temperature range (200 MHz maximum frequency for -40°C to + 105°C ambient temperature range).
4. VDD/VDDA minimum value of 1.7 V is obtained when the internal reset is OFF (refer to *Section 3.17.2: Internal reset OFF*).
5. Not available for WLCSP packages.

The STM32F745xx and STM32F746xx devices are fully pin-to-pin, compatible with the STM32F4xxxx devices, allowing the user to try different peripherals, and reaching higher performances (higher frequency) for a greater degree of freedom during the development cycle.

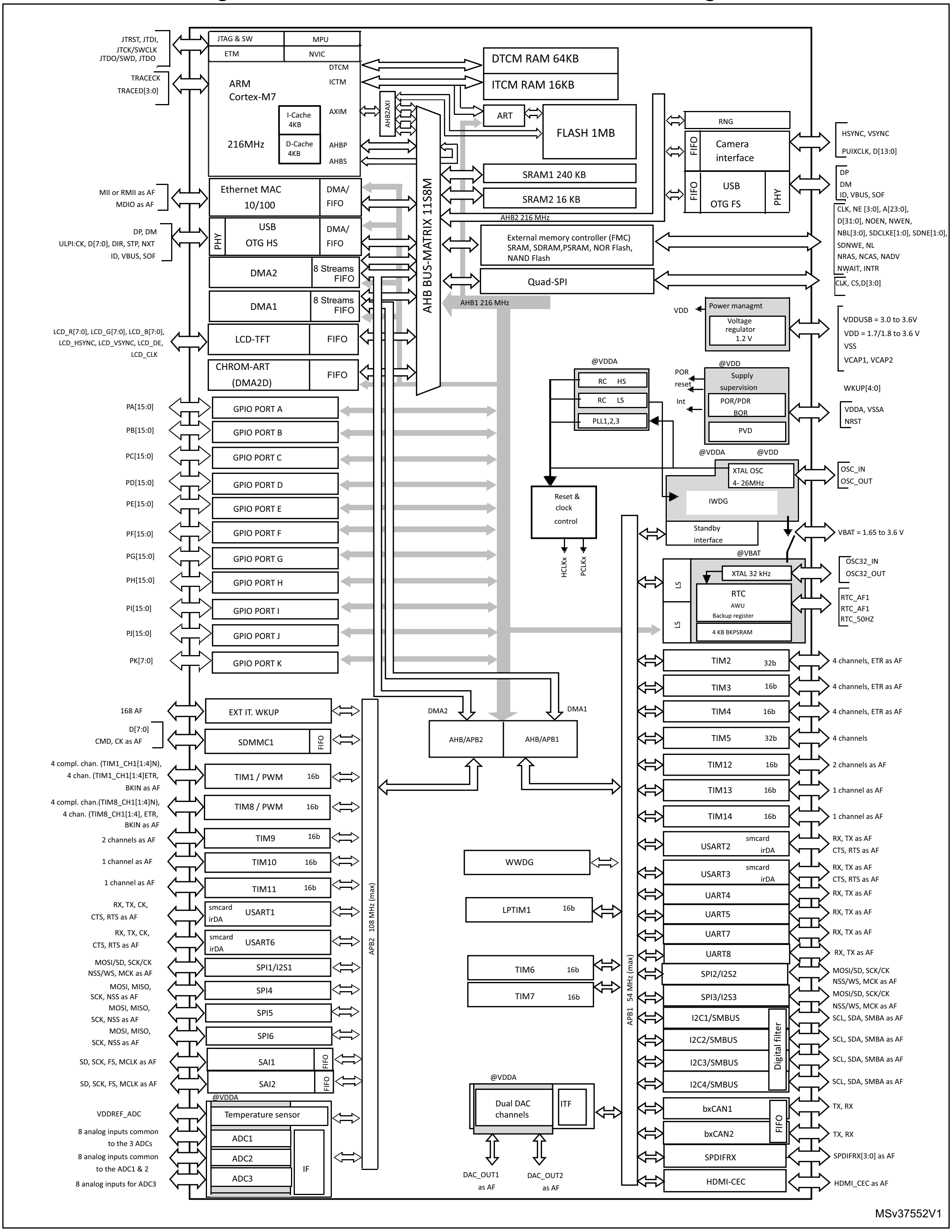
*Figure 1* give compatible board designs between the STM32F4xx families.

**Figure 1. Compatible board design for LQFP100 package**




The STM32F745xx and STM32F746xx LQFP144, LQFP176, LQFP208, TFBGA216, UFBGA176, WLCSP143 packages are fully pin to pin compatible with STM32F4xxxx devices.

**Figure 2. STM32F745xx and STM32F746xx block diagram**




1. The timers connected to APB2 are clocked from TIMxCLK up to 216 MHz, while the timers connected to APB1 are clocked from TIMxCLK either up to 108 MHz or 216 MHz depending on TIMPRE bit configuration in the RCC_DCKCFGR register.

# 3 Functional overview

## 3.1 Arm® Cortex®-M7 with FPU

The Arm® Cortex®-M7 with FPU processor is the latest generation of Arm processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and a low-power consumption, while delivering an outstanding computational performance and low interrupt latency.

The Cortex®-M7 processor is a highly efficient high-performance featuring:

- Six-stage dual-issue pipeline
- Dynamic branch prediction
- Harvard caches (4 Kbytes of I-cache and 4 Kbytes of D-cache)
- 64-bit AXI4 interface
- 64-bit ITCM interface
- 2x32-bit DTCM interfaces

The processor supports the following memory interfaces:

- Tightly Coupled Memory (TCM) interface.
- Harvard instruction and data caches and AXI master (AXIM) interface.
- Dedicated low-latency AHB-Lite peripheral (AHBP) interface.

The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution.

Its single precision FPU (floating point unit) speeds up the software development by using metalanguage development tools, while avoiding saturation.

*Figure 2* shows the general block diagram of the STM32F745xx and STM32F746xx devices.

*Note: Cortex®-M7 with FPU core is binary compatible with the Cortex®-M4 core.*

## 3.2 Memory protection unit

The memory protection unit (MPU) is used to manage the CPU accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task. This memory area is organized into up to 8 protected areas that can in turn be divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

## 3.3 Embedded flash memory

The STM32F745xx and STM32F746xx devices embed a flash memory of up to 1 Mbyte available for storing programs and data.

## 3.4 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a configurable generator polynomial value and size.

Among other applications, CRC-based techniques are used to verify the data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a mean of verifying the flash memory integrity. The CRC calculation unit helps to compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

## 3.5 Embedded SRAM

All the devices features:

- System SRAM up to 320 Kbytes:
  - SRAM1 on AHB bus Matrix: 240 Kbytes
  - SRAM2 on AHB bus Matrix: 16 Kbytes
  - DTCM-RAM on TCM interface (Tighly Coupled Memory interface): 64 Kbytes for critical real-time data.
- Instruction RAM (ITCM-RAM) 16 Kbytes:
  - It is mapped on TCM interface and reserved only for CPU Execution/Instruction useful for critical real-time routines.

The Data TCM RAM is accessible by the GP-DMAs and peripherals DMAs through specific AHB slave of the CPU.The TCM RAM instruction is reserved only for CPU. It is accessed at CPU clock speed with 0-wait states.

- 4 Kbytes of backup SRAM

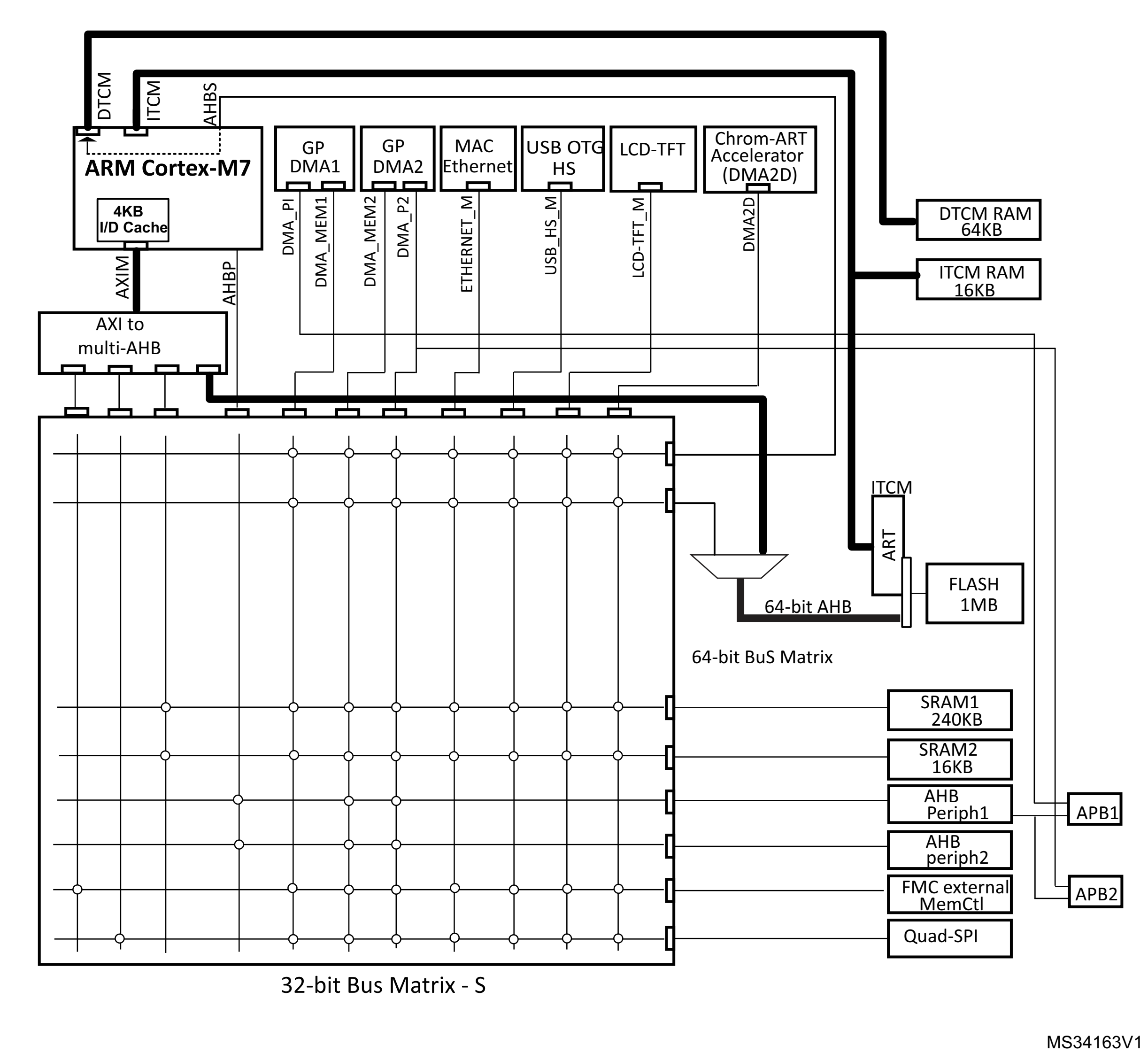
  This area is accessible only from the CPU. Its content is protected against possible unwanted write accesses, and is retained in Standby or $V_{BAT}$ mode.

## 3.6 AXI-AHB bus matrix

The STM32F745xx and STM32F746xx system architecture is based on 2 sub-systems:

- An AXI to multi AHB bridge converting AXI4 protocol to AHB-Lite protocol:
  - 3x AXI to 32-bit AHB bridges connected to AHB bus matrix
  - 1x AXI to 64-bit AHB bridge connected to the embedded flash
- A multi-AHB Bus-Matrix:
  - The 32-bit multi-AHB bus matrix interconnects all the masters (CPU, DMAs, Ethernet, USB HS, LCD-TFT, and DMA2D) and the slaves (flash memory, RAM, FMC, Quad-SPI, AHB and APB peripherals) and ensures a seamless and an efficient operation even when several high-speed peripherals work simultaneously.

**Figure 3. STM32F745xx and STM32F746xx AXI-AHB bus matrix architecture**




1. The above figure has large wires for 64-bits bus and thin wires for 32-bits bus.

## 3.7 DMA controller (DMA)

The devices feature two general-purpose dual-port DMAs (DMA1 and DMA2) with 8 streams each. They are able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. They feature dedicated FIFOs for APB/AHB peripherals, support burst transfer and are designed to provide the maximum peripheral bandwidth (AHB/APB).

The two DMA controllers support circular buffer management, so that no specific code is needed when the controller reaches the end of the buffer. The two DMA controllers also have a double buffering feature, which automates the use and switching of two memory buffers without requiring any special code.

Each stream is connected to dedicated hardware DMA requests, with support for software trigger on each stream. Configuration is made by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals:

- SPI and $I^2S$
- $I^2C$
- USART
- General-purpose, basic and advanced-control timers TIMx
- DAC
- SDMMC
- Camera interface (DCMI)
- ADC
- SAI
- SPDIFRX
- Quad-SPI
- HDMI-CEC

## 3.8 Flexible memory controller (FMC)

The Flexible memory controller (FMC) includes three memory controllers:

- The NOR/PSRAM memory controller
- The NAND/memory controller
- The Synchronous DRAM (SDRAM/Mobile LPSDR SDRAM) controller

The main features of the FMC controller are the following:

- Interface with static-memory mapped devices including:
  - Static random access memory (SRAM)
  - NOR flash memory/OneNAND flash memory
  - PSRAM (4 memory banks)
  - NAND flash memory with ECC hardware to check up to 8 Kbytes of data
- Interface with synchronous DRAM (SDRAM/Mobile LPSDR SDRAM) memories
- 8-,16-,32-bit data bus width
- Independent Chip Select control for each memory bank
- Independent configuration for each memory bank
- Write FIFO
- Read FIFO for SDRAM controller
- The Maximum FMC_CLK/FMC_SDCLK frequency for synchronous accesses is HCLK/2.

### LCD parallel interface

The FMC can be configured to interface seamlessly with most graphic LCD controllers. It supports the Intel 8080 and Motorola 6800 modes, and is flexible enough to adapt to specific LCD interfaces. This LCD parallel interface capability makes it easy to build cost-effective graphic applications using LCD modules with embedded controllers or high performance solutions using external controllers with dedicated acceleration.

## 3.9 Quad-SPI memory interface (QUADSPI)

All devices embed a Quad-SPI memory interface, which is a specialized communication interface targetting Single, Dual or Quad-SPI flash memories. It can work in:

- Direct mode through registers.
- External flash status register polling mode.
- Memory mapped mode.

Up to 256 Mbytes external flash are memory mapped, supporting 8, 16 and 32-bit access. Code execution is supported.

The opcode and the frame format are fully programmable. Communication can be either in Single Data Rate or Dual Data Rate.

## 3.10 LCD-TFT controller

The LCD-TFT display controller provides a 24-bit parallel digital RGB (Red, Green, Blue) and delivers all signals to interface directly to a broad range of LCD and TFT panels up to XGA (1024x768) resolution with the following features:

- 2 displays layers with dedicated FIFO (64x32-bit)
- Color Look-Up table (CLUT) up to 256 colors (256x24-bit) per layer
- Up to 8 Input color formats selectable per layer
- Flexible blending between two layers using alpha value (per pixel or constant)
- Flexible programmable parameters for each layer
- Color keying (transparency color)
- Up to 4 programmable interrupt events.

## 3.11 Chrom-ART Accelerator™ (DMA2D)

The Chrom-Art Accelerator™ (DMA2D) is a graphic accelerator which offers advanced bit blitting, row data copy and pixel format conversion. It supports the following functions:

- Rectangle filling with a fixed color
- Rectangle copy
- Rectangle copy with pixel format conversion
- Rectangle composition with blending and pixel format conversion.

Various image format coding are supported, from indirect 4bpp color mode up to 32bpp direct color. It embeds dedicated memory to store color lookup tables.

An interrupt can be generated when an operation is complete or at a programmed watermark.

All the operations are fully automatized and are running independently from the CPU or the DMAs.

## 3.12 Nested vectored interrupt controller (NVIC)

The devices embed a nested vectored interrupt controller able to manage 16 priority levels, and handle up to 97 maskable interrupt channels plus the 16 interrupt lines of the Cortex®-M7 with FPU core.

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Allows early processing of interrupts
- Processing of late arriving, higher-priority interrupts
- Support tail chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimum interrupt latency.

## 3.13 External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 24 edge-detector lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 168 GPIOs can be connected to the 16 external interrupt lines.

## 3.14 Clocks and startup

On reset the 16 MHz internal HSI RC oscillator is selected as the default CPU clock. The 16 MHz internal RC oscillator is factory-trimmed to offer 1% accuracy. The application can then select as system clock either the RC oscillator or an external 4-26 MHz clock source. This clock can be monitored for failure. If a failure is detected, the system automatically switches back to the internal RC oscillator and a software interrupt is generated (if enabled). This clock source is input to a PLL thus allowing to increase the frequency up to 216 MHz. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example if an indirectly used external oscillator fails).

Several prescalers allow the configuration of the two AHB buses, the high-speed APB (APB2) and the low-speed APB (APB1) domains. The maximum frequency of the two AHB buses is 216 MHz while the maximum frequency of the high-speed APB domains is 108 MHz. The maximum allowed frequency of the low-speed APB domain is 54 MHz.

The devices embed two dedicated PLL (PLLI2S and PLLSAI) which allow to achieve audio class performance. In this case, the I$^2$S and SAI master clock can generate all standard sampling frequencies from 8 kHz to 192 kHz.

## 3.15 Boot modes

At startup, the boot memory space is selected by the BOOT pin and BOOT_ADDx option bytes, allowing to program any boot memory address from 0x0000 0000 to 0x3FFF FFFF which includes:

- All flash address space mapped on ITCM or AXIM interface
- All RAM address space: ITCM, DTCM RAMs and SRAMs mapped on AXIM interface
- The System memory bootloader

The boot loader is located in system memory. It is used to reprogram the flash memory through a serial interface.

## 3.16 Power supply schemes

- $V_{BAT}$ = 1.65 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when $V_{DD}$ is not present.
- $V_{DD}$ = 1.7 to 3.6 Vexternal power supply for I/Os and the internal regulator (when enabled), provided externally through $V_{DD}$ pins.
- $V_{SSA}$, $V_{DDA}$ = 1.7 to 3.6 V: external analog power supplies for ADC, DAC, reset blocks, RCs and PLL. $V_{DDA}$ and $V_{SSA}$ must be connected to $V_{DD}$ and $V_{SS}$, respectively.

*Note: $V_{DD}/V_{DDA}$ minimum value of 1.7 V is obtained when the internal reset is OFF (refer to Section 3.17.2: Internal reset OFF). Refer to Table 3: Voltage regulator configuration mode versus device operating mode to identify the packages supporting this option.*

- $V_{DDUSB}$ can be connected either to $V_{DD}$ or an external independent power supply (3.0 to 3.6V) for USB transceivers (refer to *Figure 4* and *Figure 5*). For example, when device is powered at 1.8V, an independent power supply 3.3V can be connected to $V_{DDUSB}$. When the $V_{DDUSB}$ is connected to a separated power supply, it is independent from $V_{DD}$ or $V_{DDA}$ but it must be the last supply to be provided and the first to disappear. The following conditions $V_{DDUSB}$ must be respected:
  – During power-on phase ($V_{DD} < V_{DD\_MIN}$), $V_{DDUSB}$ should be always lower than $V_{DD}$
  – During power-down phase ($V_{DD} < V_{DD\_MIN}$), $V_{DDUSB}$ should be always lower than $V_{DD}$
  – $V_{DDSUB}$ rising and falling time rate specifications must be respected (see *Table 21* and *Table 22*)
  – In operating mode phase, $V_{DDUSB}$ could be lower or higher than $V_{DD:}$
    - If USB (USB OTG_HS/OTG_FS) is used, the associated GPIOs powered by $V_{DDUSB}$ are operating between $V_{DDUSB\_MIN}$ and $V_{DDUSB\_MAX}$.
    - The $V_{DDUSB}$ supply both USB transceiver (USB OTG_HS and USB OTG_FS). If only one USB transceiver is used in the application, the GPIOs associated to the other USB transceiver are still supplied by $V_{DDUSB}$.
    - If USB (USB OTG_HS/OTG_FS) is not used, the associated GPIOs powered by $V_{DDUSB}$ are operating between $V_{DD\_MIN}$ and $V_{DD\_MAX}$.

Figure 4. $V_{DDUSB}$ connected to $V_{DD}$ power supply

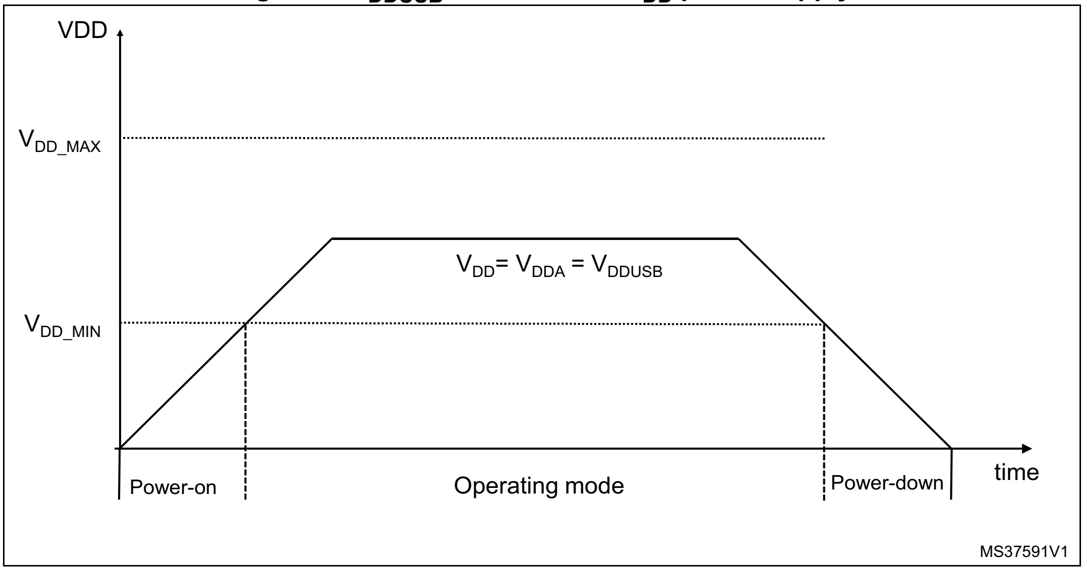
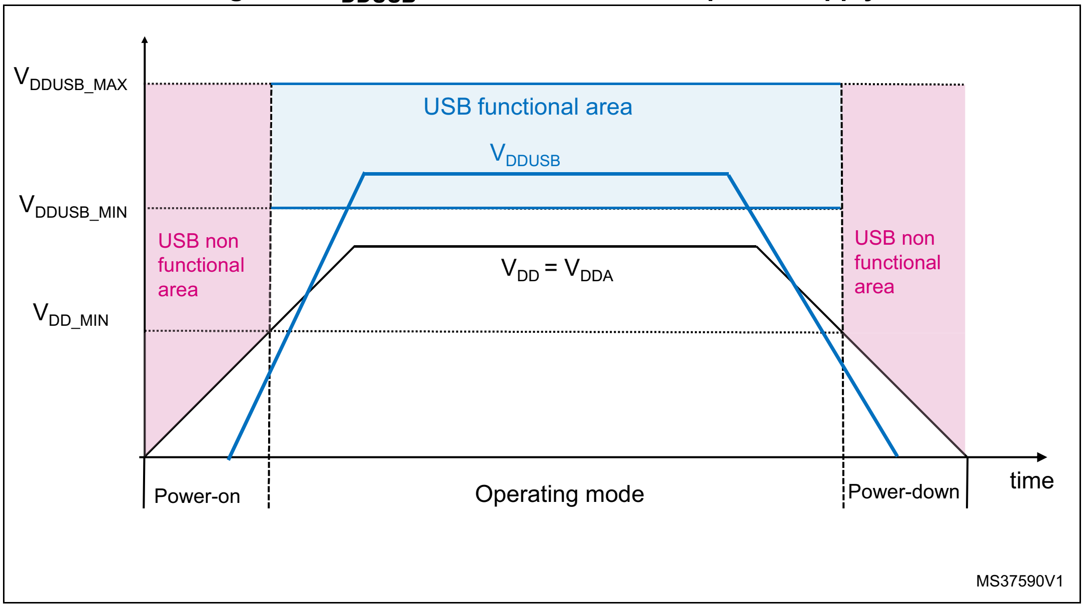



Figure 5. $V_{DDUSB}$ connected to external power supply




## 3.17 Power supply supervisor

### 3.17.1 Internal reset ON

On packages embedding the PDR_ON pin, the power supply supervisor is enabled by holding PDR_ON high. On the other packages, the power supply supervisor is always enabled.

The device has an integrated power-on reset (POR)/ power-down reset (PDR) circuitry coupled with a Brownout reset (BOR) circuitry. At power-on, POR/PDR is always active and ensures proper operation starting from 1.8 V. After the 1.8 V POR threshold level is reached, the option byte loading process starts, either to confirm or modify default BOR thresholds, or to disable BOR permanently. Three BOR thresholds are available through option bytes. The device remains in reset mode when $V_{DD}$ is below a specified threshold, $V_{POR/PDR}$ or $V_{BOR}$, without the need for an external reset circuit.

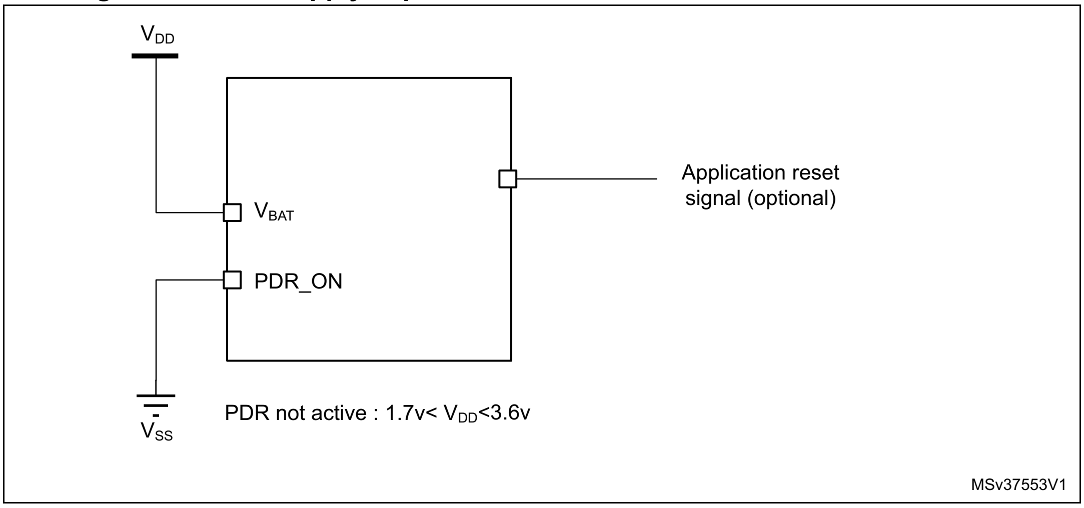
The device also features an embedded programmable voltage detector (PVD) that monitors the $V_{DD}/V_{DDA}$ power supply and compares it to the $V_{PVD}$ threshold. An interrupt can be generated when $V_{DD}/V_{DDA}$ drops below the $V_{PVD}$ threshold and/or when $V_{DD}/V_{DDA}$ is higher than the $V_{PVD}$ threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

### 3.17.2 Internal reset OFF

This feature is available only on packages featuring the PDR_ON pin. The internal power-on reset (POR) / power-down reset (PDR) circuitry is disabled through the PDR_ON pin.

An external power supply supervisor should monitor $V_{DD}$ and should maintain the device in reset mode as long as $V_{DD}$ is below a specified threshold. PDR_ON should be connected to $V_{SS}$. Refer to *Figure 6: Power supply supervisor interconnection with internal reset OFF*.

**Figure 6. Power supply supervisor interconnection with internal reset OFF**




The $V_{DD}$ specified threshold, below which the device must be maintained under reset, is 1.7 V (see *Figure 7*).

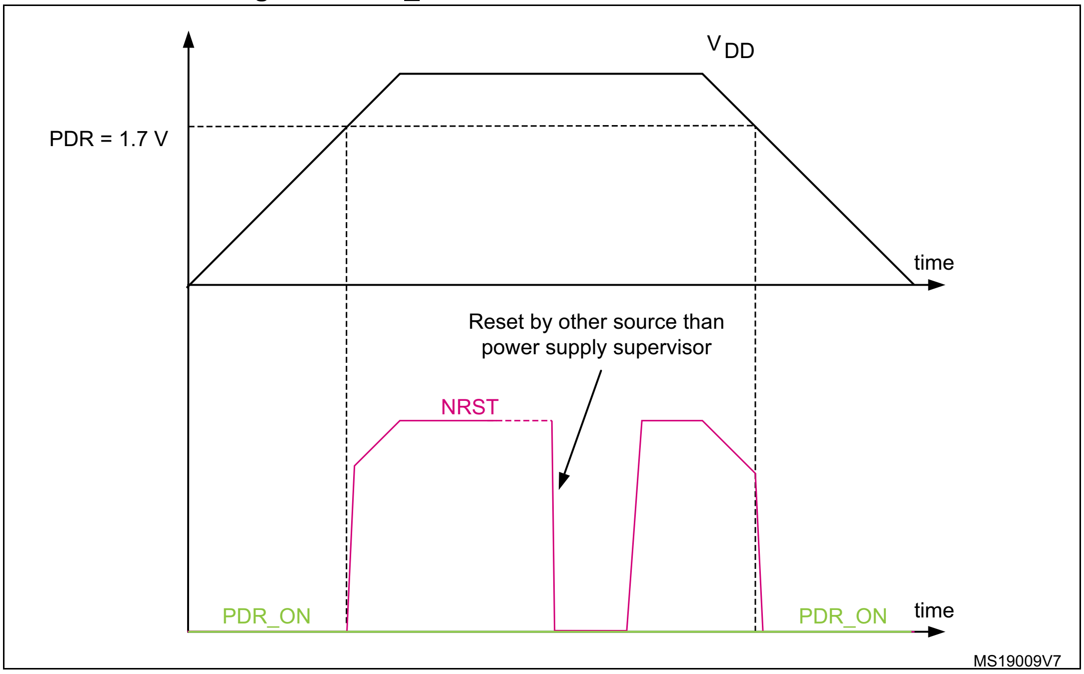
A comprehensive set of power-saving mode allows to design low-power applications.

When the internal reset is OFF, the following integrated features are no more supported:

- The integrated power-on reset (POR) / power-down reset (PDR) circuitry is disabled
- The brownout reset (BOR) circuitry must be disabled
- The embedded programmable voltage detector (PVD) is disabled
- $V_{BAT}$ functionality is no more available and $V_{BAT}$ pin should be connected to $V_{DD}$.

All the packages, except for the LQFP100, allow to disable the internal reset through the PDR_ON signal when connected to $V_{SS}$.

Figure 7. PDR_ON control with internal reset OFF




## 3.18 Voltage regulator

The regulator has four operating modes:

- Regulator ON
  - Main regulator mode (MR)
  - Low-power regulator (LPR)
  - Power-down
- Regulator OFF

### 3.18.1 Regulator ON

On packages embedding the BYPASS_REG pin, the regulator is enabled by holding BYPASS_REG low. On all other packages, the regulator is always enabled.

There are three power modes configured by software when the regulator is ON:

- MR mode used in Run/sleep modes or in Stop modes
  - In Run/Sleep mode

    The MR mode is used either in the normal mode (default mode) or the over-drive mode (enabled by software). Different voltages scaling are provided to reach the best compromise between the maximum frequency and dynamic power consumption. The over-drive mode allows operating at a higher frequency than the normal mode for a given voltage scaling.

  – In Stop modes

    The MR can be configured in two ways during Stop mode:

    MR operates in normal mode (default mode of MR in Stop mode)

    MR operates in under-drive mode (reduced leakage mode).

- LPR is used in the Stop modes:

  The LP regulator mode is configured by software when entering Stop mode.

  Like the MR mode, the LPR can be configured in two ways during Stop mode:

  – LPR operates in normal mode (default mode when LPR is ON)

  – LPR operates in under-drive mode (reduced leakage mode).

- Power-down is used in Standby mode.

  The Power-down mode is activated only when entering in Standby mode. The regulator output is in high impedance and the kernel circuitry is powered down, inducing zero consumption. The contents of the registers and SRAM are lost.

Refer to *Table 3* for a summary of voltage regulator modes versus device operating modes.

Two external ceramic capacitors should be connected on $V_{CAP\_1}$ and $V_{CAP\_2}$ pin.

All packages have the regulator ON feature.

**Table 3. Voltage regulator configuration mode versus device operating mode(1)**

| Voltage regulator configuration | Run mode | Sleep mode | Stop mode | Standby mode |
|---|---|---|---|---|
| Normal mode | MR | MR | MR or LPR | - |
| Over-drive mode(2) | MR | MR | - | - |
| Under-drive mode | - | - | MR or LPR | - |
| Power-down mode | - | - | - | Yes |

1. ‘-’ means that the corresponding configuration is not available.
2. The over-drive mode is not available when $V_{DD}$ = 1.7 to 2.1 V.

## 3.18.2 Regulator OFF

This feature is available only on packages featuring the BYPASS_REG pin. The regulator is disabled by holding BYPASS_REG high. The regulator OFF mode allows to supply externally a $V_{12}$ voltage source through $V_{CAP\_1}$ and $V_{CAP\_2}$ pins.

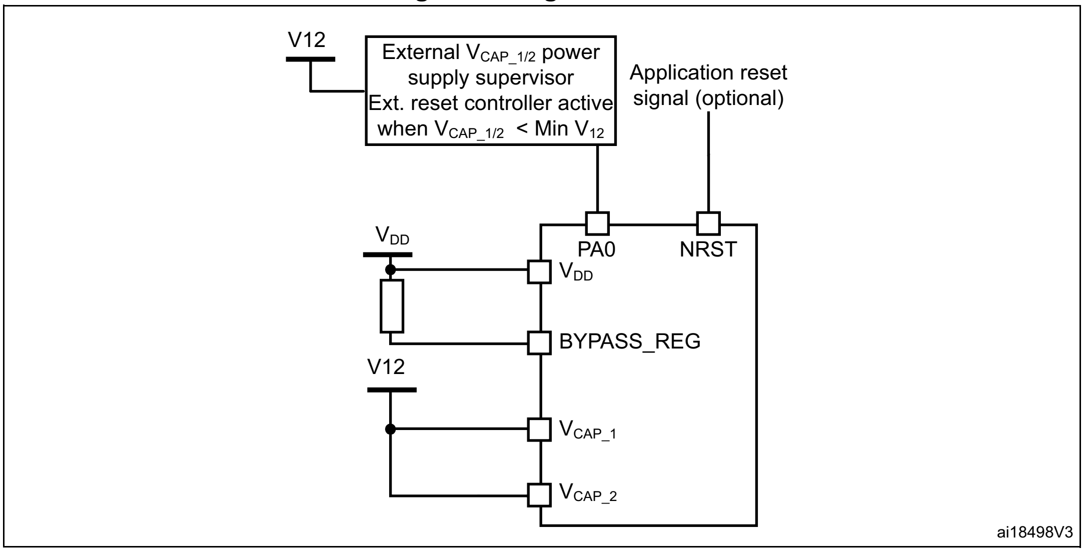
Since the internal voltage scaling is not managed internally, the external voltage value must be aligned with the targeted maximum frequency.The two 2.2 µF ceramic capacitors should be replaced by two 100 nF decoupling capacitors.

When the regulator is OFF, there is no more internal monitoring on $V_{12}$. An external power supply supervisor should be used to monitor the $V_{12}$ of the logic power domain. PA0 pin should be used for this purpose, and act as power-on reset on $V_{12}$ power domain.

In regulator OFF mode, the following features are no more supported:

- PA0 cannot be used as a GPIO pin since it allows to reset a part of the $V_{12}$ logic power domain which is not reset by the NRST pin.
- As long as PA0 is kept low, the debug mode cannot be used under power-on reset. As a consequence, PA0 and NRST pins must be managed separately if the debug connection under reset or pre-reset is required.
- The over-drive and under-drive modes are not available.
- The Standby mode is not available.

**Figure 8. Regulator OFF**

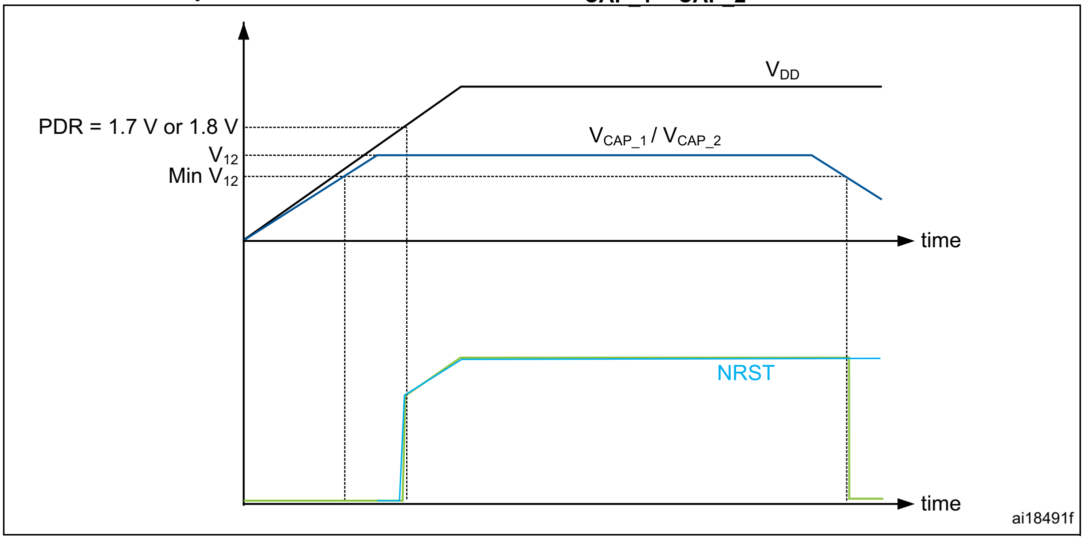



The following conditions must be respected:

- $V_{DD}$ should always be higher than $V_{CAP\_1}$ and $V_{CAP\_2}$ to avoid current injection between power domains.
- If the time for $V_{CAP\_1}$ and $V_{CAP\_2}$ to reach $V_{12}$ minimum value is faster than the time for $V_{DD}$ to reach 1.7 V, then PA0 should be kept low to cover both conditions: until $V_{CAP\_1}$ and $V_{CAP\_2}$ reach $V_{12}$ minimum value and until $V_{DD}$ reaches 1.7 V (see *Figure 9*).
- Otherwise, if the time for $V_{CAP\_1}$ and $V_{CAP\_2}$ to reach $V_{12}$ minimum value is slower than the time for $V_{DD}$ to reach 1.7 V, then PA0 could be asserted low externally (see *Figure 10*).
- If $V_{CAP\_1}$ and $V_{CAP\_2}$ go below $V_{12}$ minimum value and $V_{DD}$ is higher than 1.7 V, then a reset must be asserted on PA0 pin.

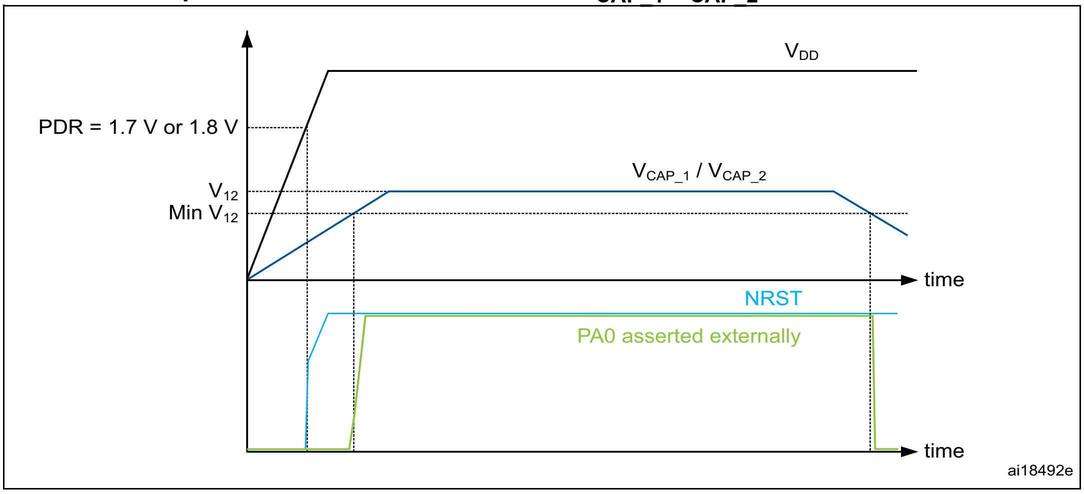
*Note: The minimum value of $V_{12}$ depends on the maximum frequency targeted in the application.*

**Figure 9. Startup in regulator OFF: slow $V_{DD}$ slope - power-down reset risen after $V_{CAP\_1}$/$V_{CAP\_2}$ stabilization**




1. This figure is valid whatever the internal reset mode (ON or OFF).

**Figure 10. Startup in regulator OFF mode: fast $V_{DD}$ slope - power-down reset risen before $V_{CAP\_1}$/$V_{CAP\_2}$ stabilization**




1. This figure is valid whatever the internal reset mode (ON or OFF).

### 3.18.3 Regulator ON/OFF and internal reset ON/OFF availability

**Table 4. Regulator ON/OFF and internal reset ON/OFF availability**

<table>
<tr><th>Package</th><th>Regulator ON</th><th>Regulator OFF</th><th>Internal reset ON</th><th>Internal reset OFF</th></tr>
<tr><td>LQFP100</td><td rowspan="2">Yes</td><td rowspan="2">No</td><td>Yes</td><td>No</td></tr>
<tr><td>LQFP144,<br>LQFP208</td><td rowspan="2">Yes<br>PDR_ON set to $V_{DD}$</td><td rowspan="2">Yes<br>PDR_ON set to VSS</td></tr>
<tr><td>TFBGA100,<br>LQFP176,<br>WLCSP143,<br>UFBGA176,<br>TFBGA216</td><td>Yes<br>BYPASS_REG set to $V_{SS}$</td><td>Yes<br>BYPASS_REG set to $V_{DD}$</td></tr>
</table>

## 3.19 Real-time clock (RTC), backup SRAM and backup registers

The RTC is an independent BCD timer/counter. It supports the following features:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format.
- Automatic correction for 28, 29 (leap year), 30, and 31 days of the month.
- Two programmable alarms.
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a master clock.
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision.
- Digital calibration circuit with 0.95 ppm resolution, to compensate for quartz crystal inaccuracy.
- Three anti-tamper detection pins with programmable filter.
- Timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event, or by a switch to $V_{BAT}$ mode.
- 17-bit auto-reload wake-up timer (WUT) for periodic events with programmable resolution and period.

The RTC and the 32 backup registers are supplied through a switch that takes power either from the $V_{DD}$ supply when present or from the $V_{BAT}$ pin.

The backup registers are 32-bit registers used to store 128 bytes of user application data when VDD power is not present. They are not reset by a system or power reset, or when the device wakes up from Standby mode.

The RTC clock sources can be:

- A 32.768 kHz external crystal (LSE)
- An external resonator or oscillator(LSE)
- The internal low-power RC oscillator (LSI, with typical frequency of 32 kHz)
- The high-speed external clock (HSE) divided by 32.

The RTC is functional in $V_{BAT}$ mode and in all low-power modes when it is clocked by the LSE. When clocked by the LSI, the RTC is not functional in $V_{BAT}$ mode, but is functional in all low-power modes.

All RTC events (Alarm, Wake-Up Timer, Timestamp or Tamper) can generate an interrupt and wake-up the device from the low-power modes.

## 3.20 Low-power modes

The devices support three low-power modes to achieve the best compromise between low-power consumption, short startup time and available wake-up sources:

- **Sleep mode**

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Stop mode**

  The Stop mode achieves the lowest power consumption while retaining the contents of SRAM and registers. All clocks in the 1.2 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled.

  The voltage regulator can be put either in main regulator mode (MR) or in low-power mode (LPR). Both modes can be configured as follows (see *Table 5: Voltage regulator modes in Stop mode*):

  – Normal mode (default mode when MR or LPR is enabled)

  – Under-drive mode.

  The device can be woken up from the Stop mode by any of the EXTI line (the EXTI line source can be one of the 16 external lines, the PVD output, the RTC alarm / wake-up / tamper / time stamp events, the USB OTG FS/HS wake-up or the Ethernet wake-up and LPTIM1 asynchronous interrupt).

**Table 5. Voltage regulator modes in Stop mode**

| Voltage regulator configuration | Main regulator (MR) | Low-power regulator (LPR) |
|---|---|---|
| Normal mode | MR ON | LPR ON |
| Under-drive mode | MR in under-drive mode | LPR in under-drive mode |

- **Standby mode**

  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.2 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, the SRAM and register contents are lost except for registers in the backup domain and the backup SRAM when selected.

  The device exits the Standby mode when an external reset (NRST pin), an IWDG reset, a rising or falling edge on one of the 6 WKUP pins (PA0, PA2, PC1, PC13, PI8, PI11), or an RTC alarm / wake-up / tamper /time stamp event occurs.

  The Standby mode is not supported when the embedded voltage regulator is bypassed and the 1.2 V domain is controlled by an external power.

## 3.21 $V_{BAT}$ operation

The $V_{BAT}$ pin allows to power the device $V_{BAT}$ domain from an external battery, an external supercapacitor, or from $V_{DD}$ when no external battery and an external supercapacitor are present.

$V_{BAT}$ operation is activated when $V_{DD}$ is not present.

The $V_{BAT}$ pin supplies the RTC, the backup registers and the backup SRAM.

*Note: When the microcontroller is supplied from $V_{BAT}$, external interrupts and RTC alarm/events do not exit it from $V_{BAT}$ operation.*

*When PDR_ON pin is connected to $V_{SS}$ (Internal Reset OFF), the $V_{BAT}$ functionality is no more available and $V_{BAT}$ pin should be connected to VDD.*

## 3.22 Timers and watchdogs

The devices include two advanced-control timers, eight general-purpose timers, two basic timers and two watchdog timers.

All timer counters can be frozen in debug mode.

*Table 6* compares the features of the advanced-control, general-purpose and basic timers.

**Table 6. Timer feature comparison**

| Timer type | Timer | Counter resolution | Counter type | Prescaler factor | DMA request generation | Capture/ compare channels | Complementary output | Max interface clock (MHz) | Max timer clock (MHz)(1) |
|---|---|---|---|---|---|---|---|---|---|
| Advanced-control | TIM1, TIM8 | 16-bit | Up, Down, Up/down | Any integer between 1 and 65536 | Yes | 4 | Yes | 108 | 216 |
| General purpose | TIM2, TIM5 | 32-bit | Up, Down, Up/down | Any integer between 1 and 65536 | Yes | 4 | No | 54 | 108/216 |
| | TIM3, TIM4 | 16-bit | Up, Down, Up/down | Any integer between 1 and 65536 | Yes | 4 | No | 54 | 108/216 |
| | TIM9 | 16-bit | Up | Any integer between 1 and 65536 | No | 2 | No | 108 | 216 |
| | TIM10, TIM11 | 16-bit | Up | Any integer between 1 and 65536 | No | 1 | No | 108 | 216 |
| | TIM12 | 16-bit | Up | Any integer between 1 and 65536 | No | 2 | No | 54 | 108/216 |
| | TIM13, TIM14 | 16-bit | Up | Any integer between 1 and 65536 | No | 1 | No | 54 | 108/216 |
| Basic | TIM6, TIM7 | 16-bit | Up | Any integer between 1 and 65536 | Yes | 0 | No | 54 | 108/216 |

1. The maximum timer clock is either 108 or 216 MHz depending on TIMPRE bit configuration in the RCC_DCKCFGR register.

### 3.22.1 Advanced-control timers (TIM1, TIM8)

The advanced-control timers (TIM1, TIM8) can be seen as three-phase PWM generators multiplexed on 6 channels. They have complementary PWM outputs with programmable inserted dead times. They can also be considered as complete general-purpose timers. Their 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge- or center-aligned modes)
- One-pulse mode output

If configured as standard 16-bit timers, they have the same features as the general-purpose TIMx timers. If configured as 16-bit PWM generators, they have full modulation capability (0-100%).

The advanced-control timer can work together with the TIMx timers via the Timer Link feature for synchronization or event chaining.

TIM1 and TIM8 support independent DMA request generation.

### 3.22.2 General-purpose timers (TIMx)

There are ten synchronizable general-purpose timers embedded in the STM32F74xxx devices (see *Table 6* for differences).

- **TIM2, TIM3, TIM4, TIM5**

  The STM32F74xxx include 4 full-featured general-purpose timers: TIM2, TIM5, TIM3, and TIM4.The TIM2 and TIM5 timers are based on a 32-bit auto-reload up/downcounter and a 16-bit prescaler. The TIM3 and TIM4 timers are based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. They all feature 4 independent channels for input capture/output compare, PWM or one-pulse mode output. This gives up to 16 input capture/output compare/PWMs on the largest packages.

  The TIM2, TIM3, TIM4, TIM5 general-purpose timers can work together, or with the other general-purpose timers and the advanced-control timers TIM1 and TIM8 via the Timer Link feature for synchronization or event chaining.

  Any of these general-purpose timers can be used to generate PWM outputs.

  TIM2, TIM3, TIM4, TIM5 all have independent DMA request generation. They are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 4 hall-effect sensors.

- **TIM9, TIM10, TIM11, TIM12, TIM13, and TIM14**

  These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler. TIM10, TIM11, TIM13, and TIM14 feature one independent channel, whereas TIM9 and TIM12 have two independent channels for input capture/output compare, PWM or one-pulse mode output. They can be synchronized with the TIM2, TIM3, TIM4, TIM5 full-featured general-purpose timers. They can also be used as simple time bases.

### 3.22.3 Basic timers TIM6 and TIM7

These timers are mainly used for DAC trigger and waveform generation. They can also be used as a generic 16-bit time base.

TIM6 and TIM7 support independent DMA request generation.

### 3.22.4 Low-power timer (LPTIM1)

The low-power timer has an independent clock and is running also in Stop mode if it is clocked by LSE, LSI or an external clock. It is able to wake-up the devices from Stop mode.

This low-power timer supports the following features:

- 16-bit up counter with 16-bit autoreload register
- 16-bit compare register
- Configurable output: pulse, PWM
- Continuous / one-shot mode
- Selectable software / hardware input trigger
- Selectable clock source:
- Internal clock source: LSE, LSI, HSI or APB clock
- External clock source over LPTIM input (working even with no internal clock source running, used by the Pulse Counter Application)
- Programmable digital glitch filter
- Encoder mode

### 3.22.5 Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 32 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management. It is hardware- or software-configurable through the option bytes.

### 3.22.6 Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

### 3.22.7 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard downcounter. It features:

- A 24-bit downcounter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source.

## 3.23 Inter-integrated circuit interface ($I^2C$)

The devices embed four I2C. Refer to *Table 7: I2C implementation* for the features implementation.

The $I^2C$ bus interface handles communication between the microcontroller and the serial $I^2C$ bus. It controls all $I^2C$ bus-specific sequencing, protocol, arbitration and timing.

The I2C peripheral supports:

- $I^2C$-bus specification and user manual rev. 5 compatibility:
  - Target and controller modes, multicontroller capability
  - Standard-mode (Sm), with a bitrate up to 100 kbit/s
  - Fast-mode (Fm), with a bitrate up to 400 kbit/s
  - 7-bit and 10-bit addressing mode, multiple 7-bit target addresses
  - Programmable setup and hold times
  - Optional clock stretching
- System Management Bus (SMBus) specification rev 2.0 compatibility:
  - Hardware PEC (Packet Error Checking) generation and verification with ACK control
  - Address resolution protocol (ARP) support
  - SMBus alert
- Power System Management Protocol (PMBus™) specification rev 1.1 compatibility
- Independent clock: a choice of independent clock sources allowing the I2C communication speed to be independent from the PCLK reprogramming.
- Programmable analog and digital noise filters
- 1-byte buffer with DMA capability

**Table 7. I2C implementation**

| I2C features(1) | I2C1 | I2C2 | I2C3 | I2C4 |
|---|---|---|---|---|
| Standard-mode (up to 100 kbit/s) | X | X | X | X |
| Fast-mode (up to 400 kbit/s) | X | X | X | X |
| Programmable analog and digital noise filters | X | X | X | X |
| SMBus/PMBus hardware support | X | X | X | X |
| Independent clock | X | X | X | X |

1. X: supported

## 3.24 Universal synchronous/asynchronous receiver transmitters (USART)

The devices embed USART. Refer to *Table 8: USART implementation* for the features implementation.

The universal synchronous asynchronous receiver transmitter (USART) offers a flexible means of full-duplex data exchange with external equipment requiring an industry standard NRZ asynchronous serial data format.

The USART peripheral supports:

- Full-duplex asynchronous communications
- Configurable oversampling method by 16 or 8 to give flexibility between speed and clock tolerance
- Dual clock domain allowing convenient baud rate programming independent from the PCLK reprogramming
- A common programmable transmit and receive baud rate of up to 27 Mbit/s when USART clock source is system clock frequency (Max is 216 MHz) and oversampling by 8 is used.
- Auto baud rate detection
- Programmable data word length (7 or 8 or 9 bits) word length
- Programmable data order with MSB-first or LSB-first shifting
- Programmable parity (odd, even, no parity)
- Configurable stop bits (1 or 1.5 or 2 stop bits)
- Synchronous mode and clock output for synchronous communications
- Single-wire half-duplex communications
- Separate signal polarity control for transmission and reception
- Swappable Tx/Rx pin configuration
- Hardware flow control for modem and RS-485 transceiver
- Multiprocessor communications
- LIN master synchronous break send capability and LIN slave break detection capability
- IrDA SIR encoder decoder supporting 3/16 bit duration for normal mode
- Smartcard mode ( T=0 and T=1 asynchronous protocols for Smartcards as defined in the ISO/IEC 7816-3 standard )
- Support for Modbus communication

The table below summarizes the implementation of all U(S)ARTs instances

**Table 8. USART implementation**

| features(1) | USART1/2/3/6 | UART4/5/7/8 |
|---|---|---|
| Data Length | 7, 8 and 9 bits | |
| Hardware flow control for modem | X | X |
| Continuous communication using DMA | X | X |
| Multiprocessor communication | X | X |
| Synchronous mode | X | - |

Table 8. USART implementation (continued)

| features[1] | USART1/2/3/6 | UART4/5/7/8 |
|---|---|---|
| Smartcard mode | X | - |
| Single-wire half-duplex communication | X | X |
| IrDA SIR ENDEC block | X | X |
| LIN mode | X | X |
| Dual clock domain | X | X |
| Receiver timeout interrupt | X | X |
| Modbus communication | X | X |
| Auto baud rate detection | X | X |
| Driver Enable | X | X |

1. X: supported.

## 3.25 Serial peripheral interface (SPI)/inter-integrated sound interfaces (I2S)

The devices feature up to six SPIs in slave and master modes in full-duplex and simplex communication modes. SPI1, SPI4, SPI5, and SPI6 can communicate at up to 54 Mbits/s, SPI2 and SPI3 can communicate at up to 27 Mbit/s. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable from 4 to 16 bits. The SPI interfaces support NSS pulse mode, TI mode and Hardware CRC calculation. All SPIs can be served by the DMA controller.

Three standard $I^2S$ interfaces (multiplexed with SPI1, SPI2 and SPI3) are available. They can be operated in master or slave mode, in simplex communication modes, and can be configured to operate with a 16-/32-bit resolution as an input or output channel. Audio sampling frequencies from 8 kHz up to 192 kHz are supported. When either or both of the $I^2S$ interfaces is/are configured in master mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling frequency.

All I2Sx can be served by the DMA controller.

## 3.26 Serial audio interface (SAI)

The devices embed two serial audio interfaces.

The serial audio interface is based on two independent audio subblocks which can operate as transmitter or receiver with their FIFO. Many audio protocols are supported by each block: I2S standards, LSB or MSB-justified, PCM/DSP, TDM, AC’97 and SPDIF output, supporting audio sampling frequencies from 8 kHz up to 192 kHz. Both subblocks can be

configured in master or in slave mode.

In master mode, the master clock can be output to the external DAC/CODEC at 256 times of the sampling frequency.

The two sub-blocks can be configured in synchronous mode when full-duplex mode is required.

SAI1 and SAI2 can be served by the DMA controller

## 3.27 SPDIFRX Receiver Interface (SPDIFRX)

The SPDIFRX peripheral, is designed to receive an S/PDIF flow compliant with IEC-60958 and IEC-61937. These standards support simple stereo streams up to high sample rate, and compressed multi-channel surround sound, such as those defined by Dolby or DTS (up to 5.1).

The main features of the SPDIFRX are the following:

- Up to 4 inputs available
- Automatic symbol rate detection
- Maximum symbol rate: 12.288 MHz
- Stereo stream from 32 to 192 kHz supported
- Supports Audio IEC-60958 and IEC-61937, consumer applications
- Parity bit management
- Communication using DMA for audio samples
- Communication using DMA for control and user channel information
- Interrupt capabilities

The SPDIFRX receiver provides all the necessary features to detect the symbol rate, and decode the incoming data stream. The user can select the wanted SPDIF input, and when a valid signal will be available, the SPDIFRX will re-sample the incoming signal, decode the manchester stream, recognize frames, sub-frames and blocks elements. It delivers to the CPU decoded data, and associated status flags.

The SPDIFRX also offers a signal named spdif_frame_sync, which toggles at the S/PDIF sub-frame rate that will be used to compute the exact sample rate for clock drift algorithms.

## 3.28 Audio PLL (PLLI2S)

The devices feature an additional dedicated PLL for audio I$^2$S and SAI applications. It allows to achieve error-free I$^2$S sampling clock accuracy without compromising on the CPU performance, while using USB peripherals.

The PLLI2S configuration can be modified to manage an I$^2$S/SAI sample rate change without disabling the main PLL (PLL) used for CPU, USB and Ethernet interfaces.

The audio PLL can be programmed with very low error to obtain sampling rates ranging from 8 KHz to 192 KHz.

In addition to the audio PLL, a master clock input pin can be used to synchronize the I$^2$S/SAI flow with an external PLL (or Codec output).

## 3.29 Audio and LCD PLL(PLLSAI)

An additional PLL dedicated to audio and LCD-TFT is used for SAI1 peripheral in case the PLLI2S is programmed to achieve another audio sampling frequency (49.152 MHz or 11.2896 MHz) and the audio application requires both sampling frequencies simultaneously.

The PLLSAI is also used to generate the LCD-TFT clock.

## 3.30 SD/SDIO/MMC card host interface (SDMMC)

An SDMMC host interface is available, that supports MultiMediaCard System Specification Version 4.2 in three different databus modes: 1-bit (default), 4-bit and 8-bit.

The interface allows data transfer at up to 50 MHz, and is compliant with the SD Memory card specification version 2.0.

The SDMMC card specification version 2.0 is also supported with two different databus modes: 1-bit (default) and 4-bit.

The current version supports only one SD/SDMMC/MMC4.2 card at any one time and a stack of MMC4.1 or previous.

The SDMMC can be served by the DMA controller

## 3.31 Ethernet MAC interface with dedicated DMA and IEEE 1588 support

The devices provide an IEEE-802.3-2002-compliant media access controller (MAC) for ethernet LAN communications through an industry-standard medium-independent interface (MII) or a reduced medium-independent interface (RMII). The microcontroller requires an external physical interface device (PHY) to connect to the physical LAN bus (twisted-pair, fiber, etc.). The PHY is connected to the device MII port using 17 signals for MII or 9 signals for RMII, and can be clocked using the 25 MHz (MII) from the microcontroller.

The devices include the following features:

- Support of 10 and 100 Mbit/s rates
- Dedicated DMA controller allowing high-speed transfers between the dedicated SRAM and the descriptors
- Tagged MAC frame support (VLAN support)
- Half-duplex (CSMA/CD) and full-duplex operation
- MAC control sublayer (control frames) support
- 32-bit CRC generation and removal
- Several address filtering modes for physical and multicast address (multicast and group addresses)
- 32-bit status code for each transmitted or received frame
- Internal FIFOs to buffer transmit and receive frames. The transmit FIFO and the receive FIFO are both 2 Kbytes.
- Supports hardware PTP (precision time protocol) in accordance with IEEE 1588 2008 (PTP V2) with the time stamp comparator connected to the TIM2 input
- Triggers interrupt when system time becomes greater than target time

## 3.32 Controller area network (bxCAN)

The two CANs are compliant with the 2.0A and B (active) specifications with a bitrate up to 1 Mbit/s. They can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. Each CAN has three transmit mailboxes, two receive FIFOS with 3 stages and 28 shared scalable filter banks (all of them can be used even if one CAN is used). 256 bytes of SRAM are allocated for each CAN.

## 3.33 Universal serial bus on-the-go full-speed (OTG_FS)

The devices embed an USB OTG full-speed device/host/OTG peripheral with integrated transceivers. The USB OTG FS peripheral is compliant with the USB 2.0 specification and with the OTG 2.0 specification. It has software-configurable endpoint setting and supports suspend/resume. The USB OTG controller requires a dedicated 48 MHz clock that is generated by a PLL connected to the HSE oscillator.

The major features are:

- Combined Rx and Tx FIFO size of 1.28 Kbytes with dynamic FIFO sizing
- Support of the session request protocol (SRP) and host negotiation protocol (HNP)
- 1 bidirectional control endpoint + 5 IN endpoints + 5 OUT endpoints
- 12 host channels with periodic OUT support
- Software configurable to OTG1.3 and OTG2.0 modes of operation
- USB 2.0 LPM (Link Power Management) support
- Internal FS OTG PHY support
- HNP/SNP/IP inside (no need for any external resistor)

For OTG/Host modes, a power switch is needed in case bus-powered devices are connected

## 3.34 Universal serial bus on-the-go high-speed (OTG_HS)

The devices embed a USB OTG high-speed (up to 480 Mb/s) device/host/OTG peripheral. The USB OTG HS supports both full-speed and high-speed operations. It integrates the transceivers for full-speed operation (12 MB/s) and features a UTMI low-pin interface (ULPI) for high-speed operation (480 MB/s). When using the USB OTG HS in HS mode, an external PHY device connected to the ULPI is required.

The USB OTG HS peripheral is compliant with the USB 2.0 specification and with the OTG 2.0 specification. It has software-configurable endpoint setting and supports suspend/resume. The USB OTG controller requires a dedicated 48 MHz clock that is generated by a PLL connected to the HSE oscillator.

The major features are:

- Combined Rx and Tx FIFO size of 4 Kbytes with dynamic FIFO sizing
- Support of the session request protocol (SRP) and host negotiation protocol (HNP)
- 8 bidirectional endpoints
- 16 host channels with periodic OUT support
- Software configurable to OTG1.3 and OTG2.0 modes of operation
- USB 2.0 LPM (Link Power Management) support
- Internal FS OTG PHY support
- External HS or HS OTG operation supporting ULPI in SDR mode. The OTG PHY is connected to the microcontroller ULPI port through 12 signals. It can be clocked using the 60 MHz output.
- Internal USB DMA
- HNP/SNP/IP inside (no need for any external resistor)
- for OTG/Host modes, a power switch is needed in case bus-powered devices are connected

## 3.35 High-definition multimedia interface (HDMI) - consumer electronics control (CEC)

The devices embed a HDMI-CEC controller that provides hardware support for the Consumer Electronics Control (CEC) protocol (Supplement 1 to the HDMI standard).

This protocol provides high-level control functions between all audiovisual products in an environment. It is specified to operate at low speeds with minimum processing and memory overhead. It has a clock domain independent from the CPU clock, allowing the HDMI-CEC controller to wake-up the MCU from Stop mode on data reception.

## 3.36 Digital camera interface (DCMI)

The devices embed a camera interface that can connect with camera modules and CMOS sensors through an 8-bit to 14-bit parallel interface, to receive video data. The camera interface can sustain a data transfer rate up to 54 Mbyte/s at 54 MHz. It features:

- Programmable polarity for the input pixel clock and synchronization signals
- Parallel data communication can be 8-, 10-, 12- or 14-bit
- Supports 8-bit progressive video monochrome or raw bayer format, YCbCr 4:2:2 progressive video, RGB 565 progressive video or compressed data (like JPEG)
- Supports continuous mode or snapshot (a single frame) mode
- Capability to automatically crop the image

## 3.37 True Random number generator (RNG)

The RNG is a true random number generator that provides full entropy outputs to the application as 32-bit samples. It is composed of a live entropy source (analog) and an internal conditioning component.

All devices embed an RNG that delivers 32-bit random numbers generated by an integrated analog circuit.

## 3.38 General-purpose input/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain, with or without pull-up or pull-down), as input (floating, with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high-current-capable and have speed selection to better manage internal noise, power consumption and electromagnetic emission.

The I/O configuration can be locked if needed by following a specific sequence in order to avoid spurious writing to the I/Os registers.

Fast I/O handling allowing maximum I/O toggling up to 108 MHz.

## 3.39 Analog-to-digital converters (ADCs)

Three 12-bit analog-to-digital converters are embedded and each ADC shares up to 16 external channels, performing conversions in the single-shot or scan mode. In scan mode, automatic conversion is performed on a selected group of analog inputs.

Additional logic functions embedded in the ADC interface allow:

- Simultaneous sample and hold
- Interleaved sample and hold

The ADC can be served by the DMA controller. An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

To synchronize A/D conversion and timers, the ADCs could be triggered by any of TIM1, TIM2, TIM3, TIM4, TIM5, or TIM8 timer.

## 3.40 Temperature sensor

The temperature sensor has to generate a voltage that varies linearly with temperature. The conversion range is between 1.7 V and 3.6 V. The temperature sensor is internally connected to the same input channel as $V_{BAT}$, ADC1_IN18, which is used to convert the sensor output voltage into a digital value. When the temperature sensor and $V_{BAT}$ conversion are enabled at the same time, only $V_{BAT}$ conversion is performed.

As the offset of the temperature sensor varies from chip to chip due to process variation, the internal temperature sensor is mainly suitable for applications that detect temperature changes instead of absolute temperatures. If an accurate temperature reading is needed, then an external temperature sensor part should be used.

## 3.41 Digital-to-analog converter (DAC)

The two 12-bit buffered DAC channels can be used to convert two digital signals into two analog voltage signal outputs.

This dual digital Interface supports the following features:

- two DAC converters: one for each output channel
- 8-bit or 12-bit monotonic output
- left or right data alignment in 12-bit mode
- synchronized update capability
- noise-wave generation
- triangular-wave generation
- dual DAC channel independent or simultaneous conversions
- DMA capability for each channel
- external triggers for conversion
- input voltage reference $V_{REF+}$

Eight DAC trigger inputs are used in the device. The DAC channels are triggered through the timer update outputs that are also connected to different DMA streams.

## 3.42 Serial wire JTAG debug port (SWJ-DP)

The Arm SWJ-DP interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

Debug is performed using 2 pins only instead of 5 required by the JTAG (JTAG pins could be re-use as GPIO with alternate function): the JTAG TMS and TCK pins are shared with SWDIO and SWCLK, respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

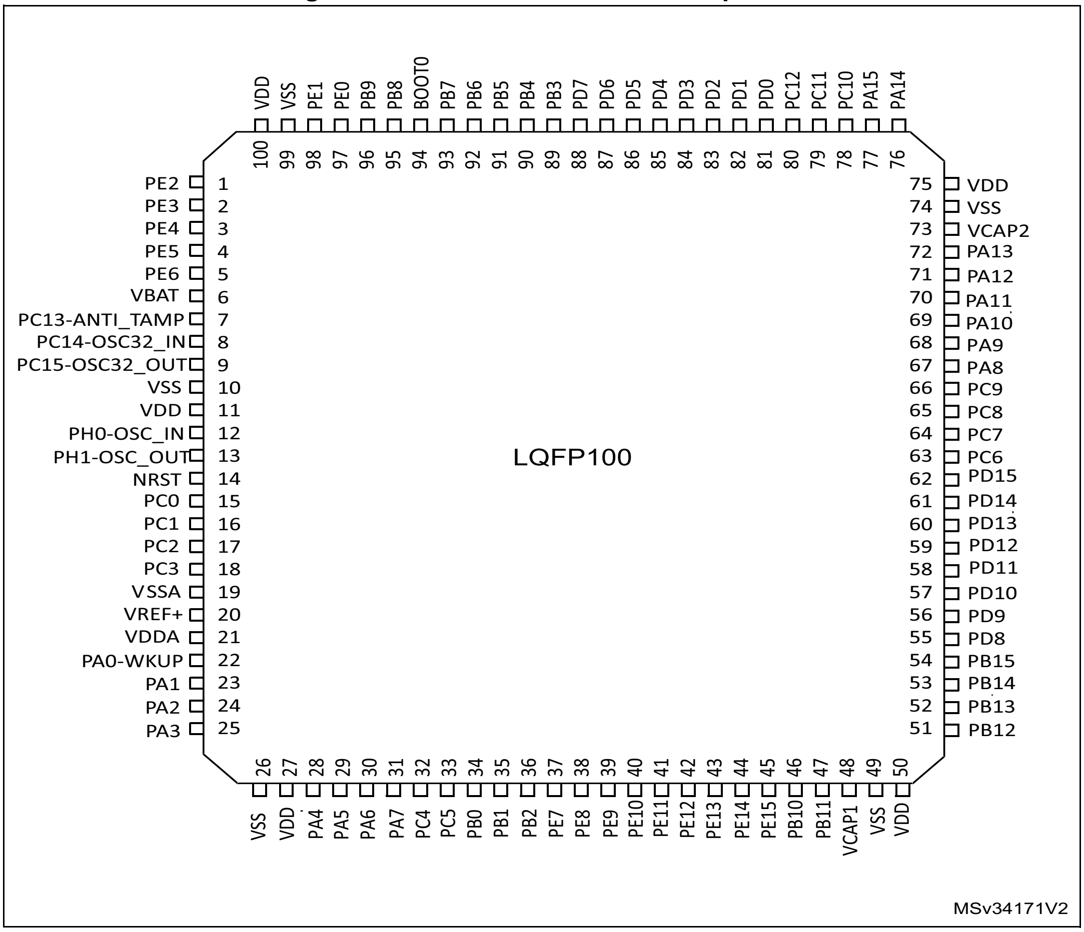
## 3.43 Embedded Trace Macrocell™

The Arm Embedded Trace Macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32F74xxx through a small number of ETM pins to an external hardware trace port analyzer (TPA) device. The TPA is connected to a host computer using USB, Ethernet, or any other high-speed channel. Real-time instruction and data flow activity can be recorded and then formatted for display on the host computer that runs the debugger software. TPA hardware is commercially available from common development tool vendors.

The Embedded Trace Macrocell operates with third party debugger software tools.

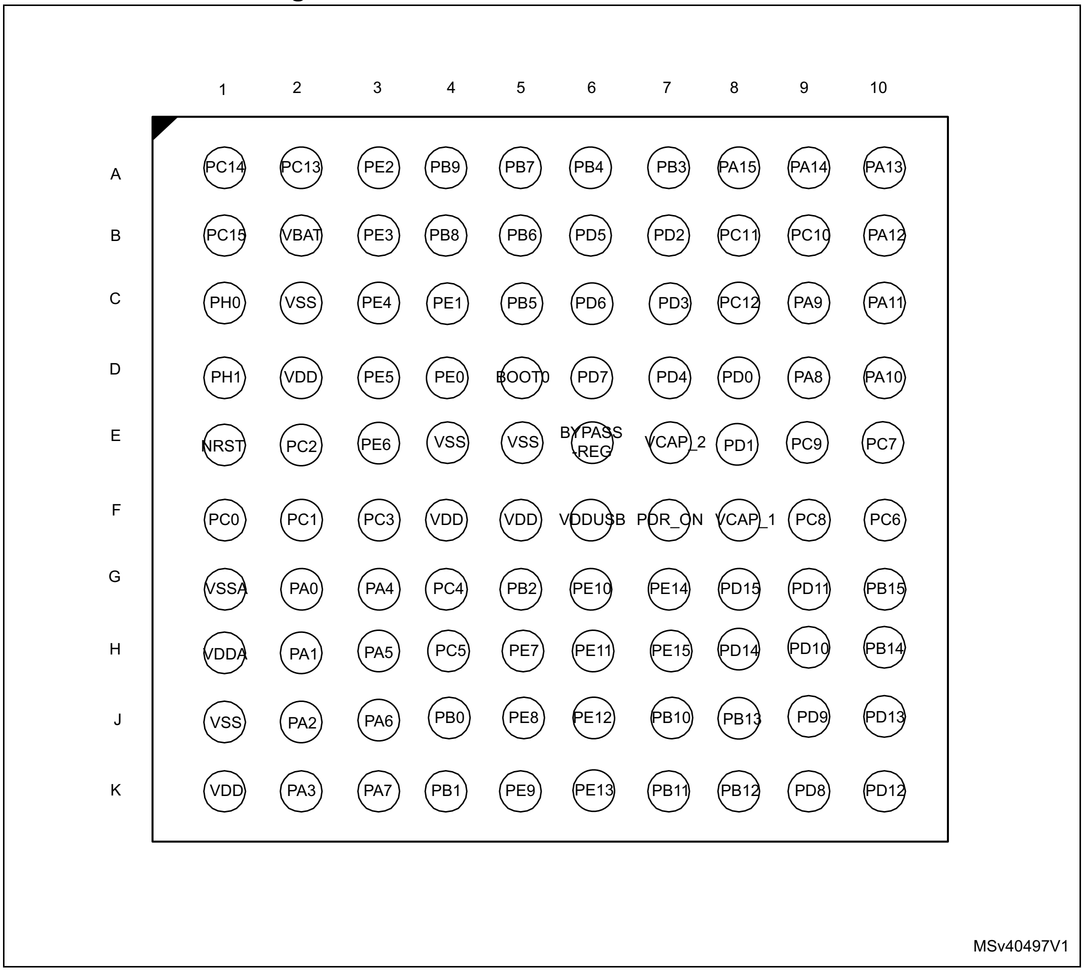
# 4 Pinouts and pin description

**Figure 11. STM32F74xVx LQFP100 pinout**




2. The above figure shows the package top view.

**Figure 12. STM32F74xVx TFBGA100 ballout**




1. The above figure shows the package top view.

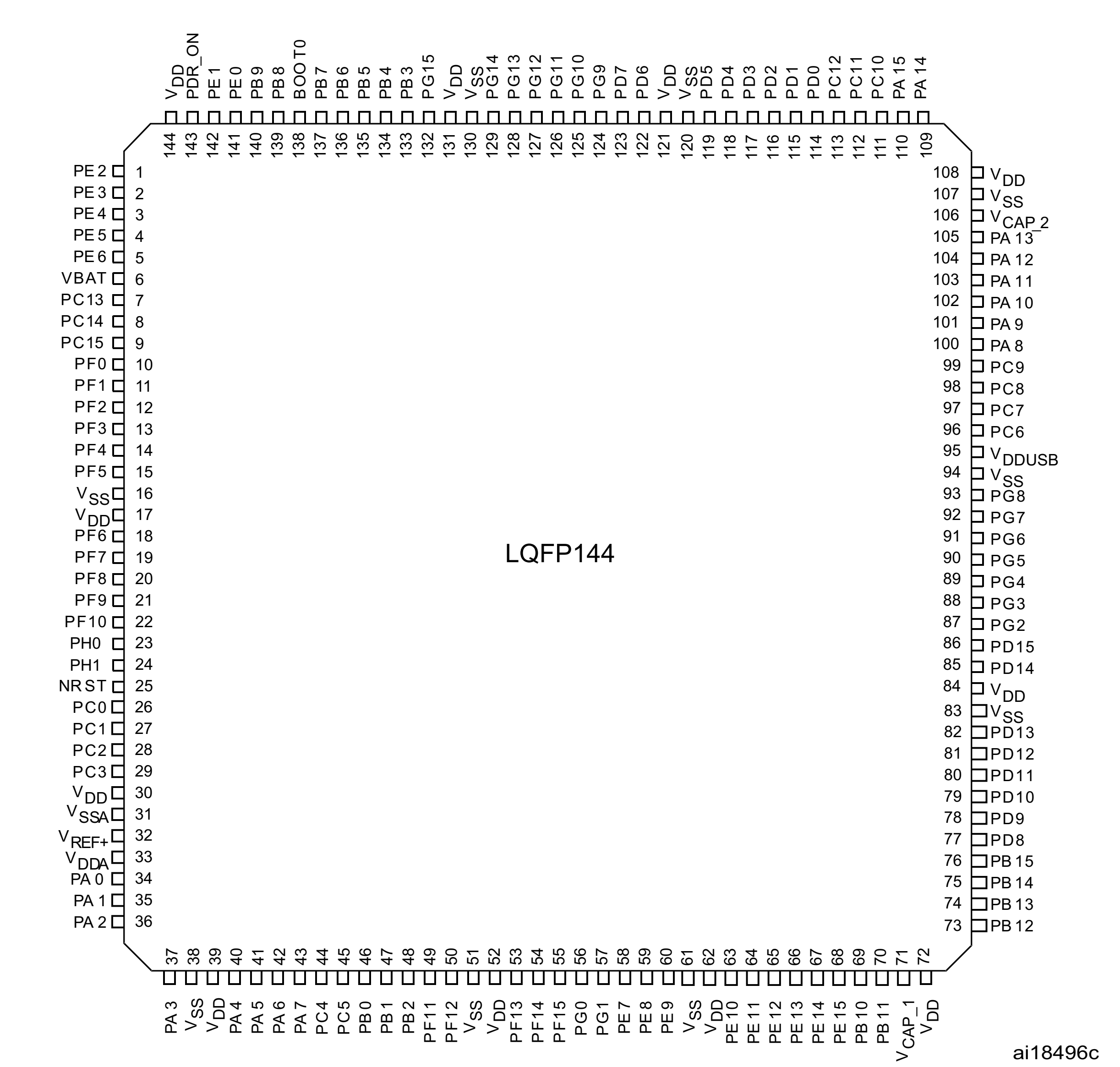
**Figure 13. STM32F74xZx WLCSP143 ballout**

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| A | VDD | PC10 | PD2 | PD5 | PD7 | PG12 | PG15 | PB6 | PB8 | PE1 | PDR_ON |
| B | PA14 | PC11 | PD0 | PD3 | PD4 | PG11 | PB3 | PB7 | PB9 | PE0 | PE4 |
| C | VDD | PA15 | PC12 | PD1 | VDD | PG10 | PB4 | PB5 | BOOT0 | PE3 | VBAT |
| D | VCAP_2 | VSS | PA13 | PA11 | PA10 | PG13 | VDD | PE2 | PE5 | PC13 | PC14 |
| E | PA12 | PA9 | PC9 | PC8 | PG9 | VDD | VSS | PE6 | PF1 | VDD | PC15 |
| F | PA8 | PC6 | PC7 | PD6 | VSS | PG14 | PF7 | PF5 | PF4 | PF2 | PF0 |
| G | VDDUSB | PG8 | PG3 | PG6 | PG4 | PG5 | VDD | PF9 | PF10 | PF6 | PF3 |
| H | PG7 | VSS | VSS | PD10 | PD13 | PD12 | VSS | PC0 | NRST | PH1 | PF8 |
| J | PG2 | PD14 | PB15 | PE10 | VDD | VDD | VDD | VDD | PC3 | PC2 | PH0 |
| K | PD15 | PD11 | PB14 | PE11 | PG1 | PF13 | PB1 | PA1 | PA0 | VSSA | PC1 |
| L | VDD | PD8 | PE15 | PE12 | PE7 | PF14 | PB2 | PA7 | PA2 | VDDA | VREF+ |
| M | PD9 | PB12 | PB10 | PE14 | PE8 | PF15 | PF11 | PC4 | PA5 | PA4 | PA3 |
| N | PB13 | VCAP_1 | PB11 | PE13 | PE9 | PG0 | PF12 | PB0 | PC5 | PA6 | BYPASS_REG |

MSv40499V1

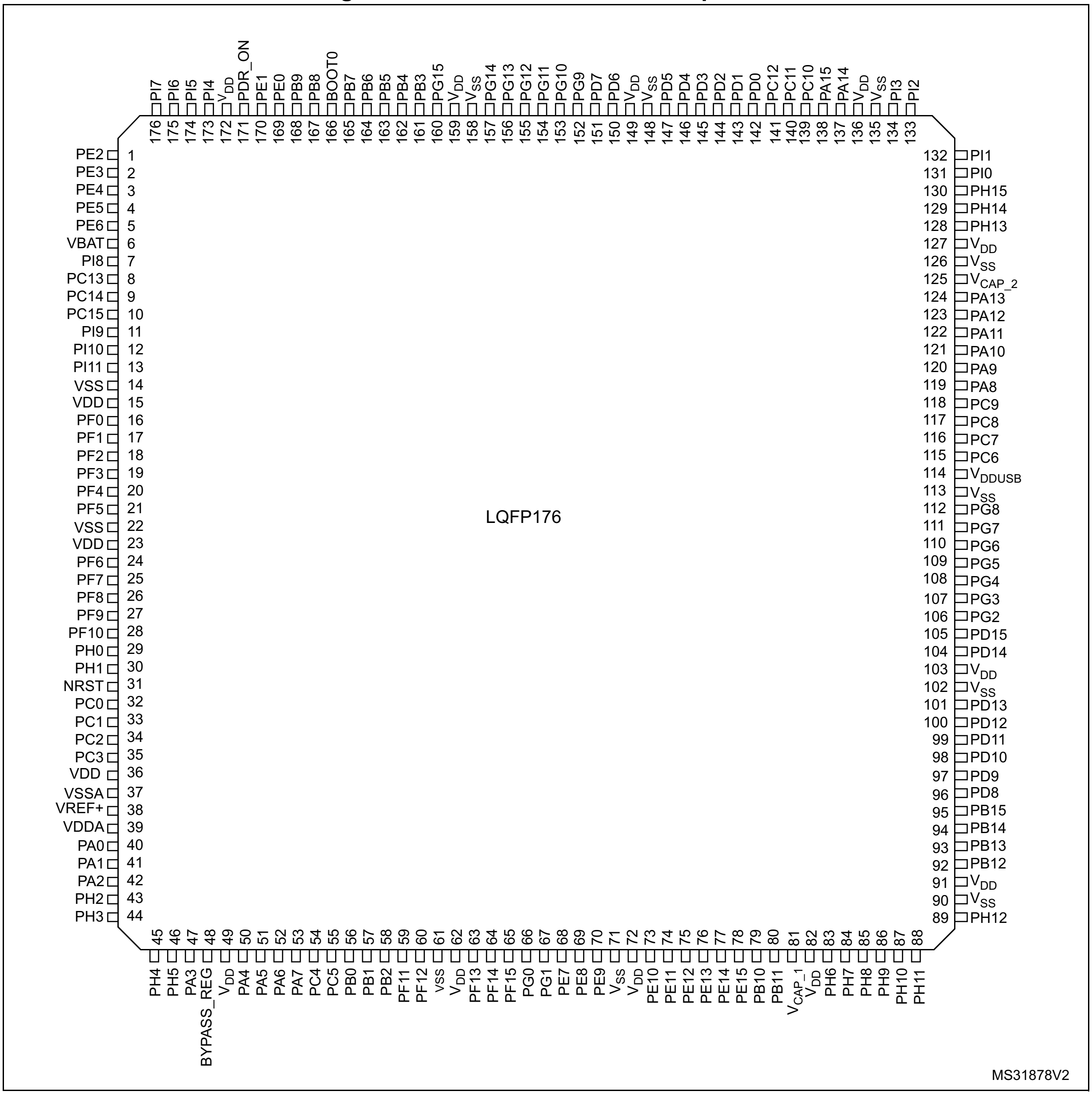
1. The above figure shows the package top view.

**Figure 14. STM32F74xZx LQFP144 pinout**



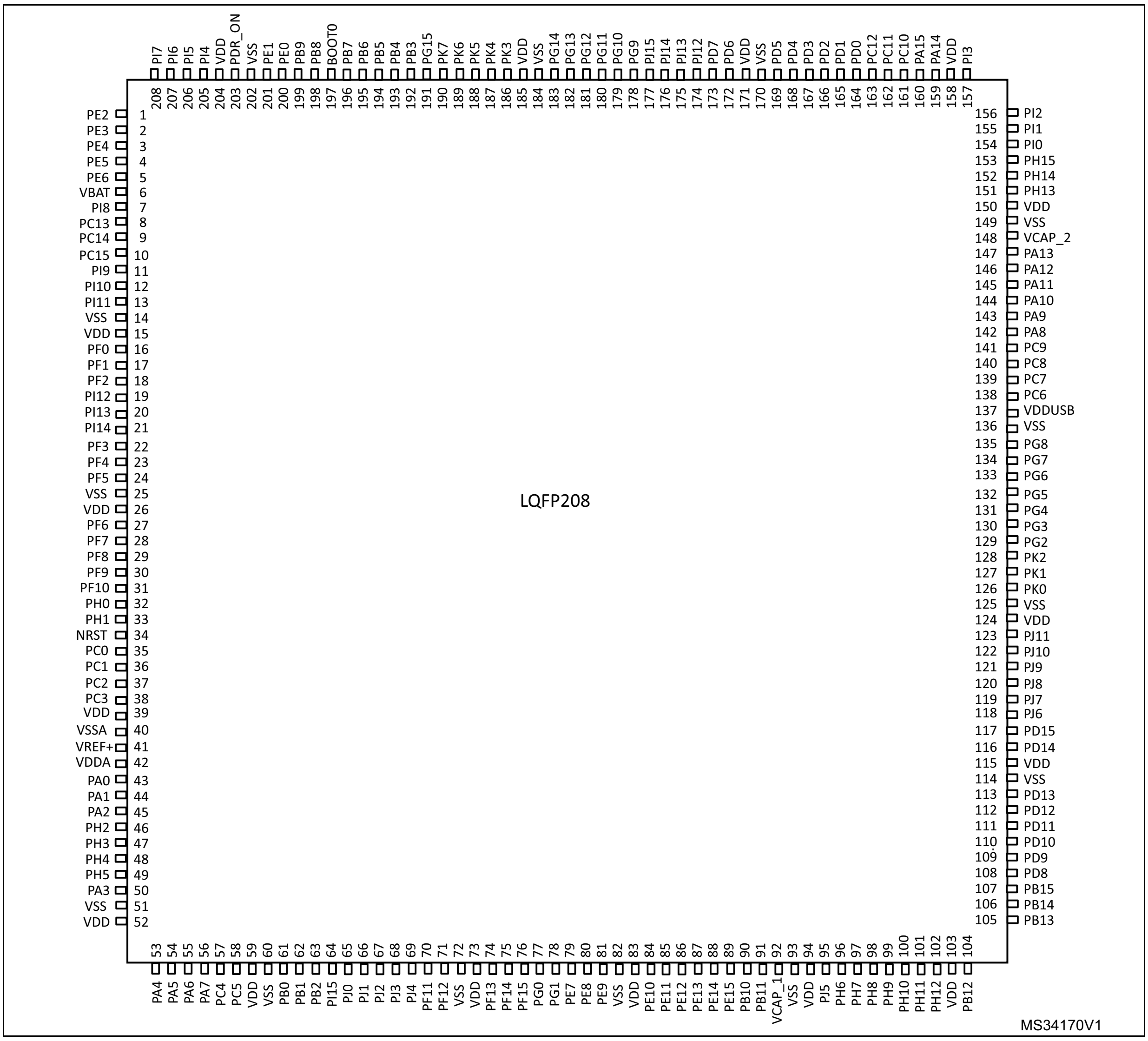

1. The above figure shows the package top view.

**Figure 15. STM32F74xIx LQFP176 pinout**



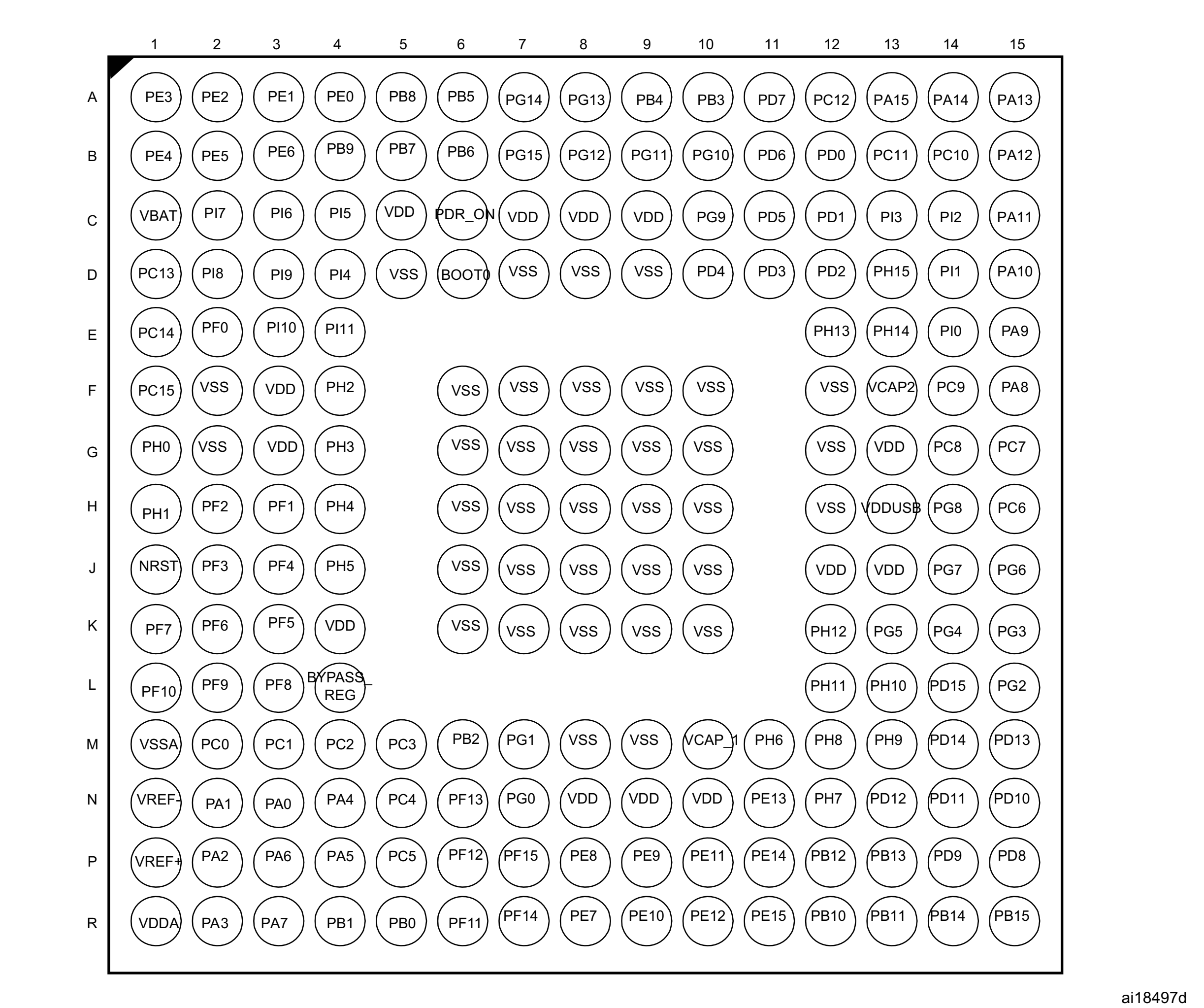

1. The above figure shows the package top view.

**Figure 16. STM32F74xBx LQFP208 pinout**



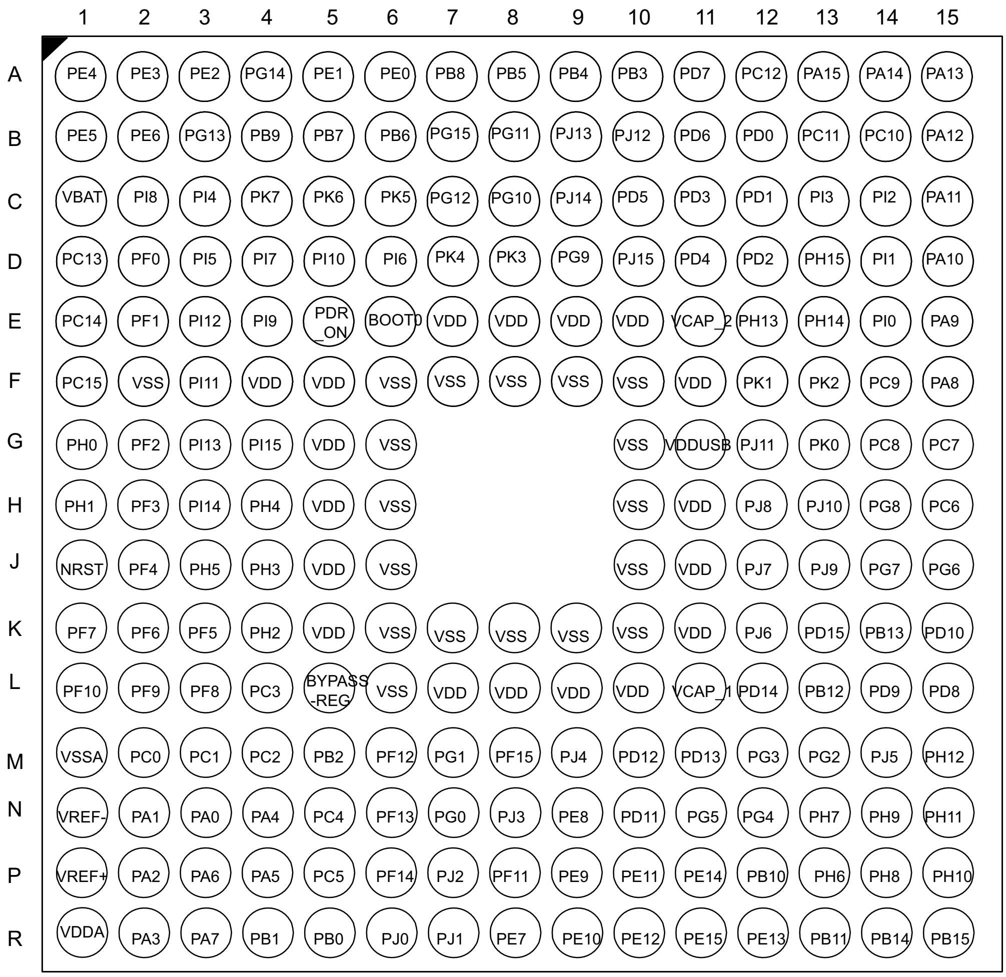

1. The above figure shows the package top view.

**Figure 17. STM32F74xIx UFBGA176 ballout**




1. The above figure shows the package top view.

**Figure 18. STM32F74xNx TFBGA216 ballout**




1. The above figure shows the package top view.

**Table 9. Legend/abbreviations used in the pinout table**

| Name | Abbreviation | Definition |
|---|---|---|
| Pin name | Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name | |
| Pin type | S | Supply pin |
| | I | Input only pin |
| | I/O | Input / output pin |
| I/O structure | FT | 5 V tolerant I/O |
| | TTa | 3.3 V tolerant I/O directly connected to ADC |
| | B | Dedicated BOOT pin |
| | RST | Bidirectional reset pin with weak pull-up resistor |
| Notes | Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset | |
| Alternate functions | Functions selected through GPIOx_AFR registers | |
| Additional functions | Functions directly selected/enabled through peripheral registers | |

**Table 10. STM32F745xx and STM32F746xx pin and ball definition**

| Pin Number | | | | | | | | Pin name (function after reset)(1) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LQFP100 | TFBGA100 | WLCSP143 | LQFP144 | UFBGA176 | LQFP176 | LQFP208 | TFBGA216 | | | | | | |
| 1 | A3 | D8 | 1 | A2 | 1 | 1 | A3 | PE2 | I/O | FT | - | TRACECLK, SPI4_SCK, SAI1_MCLK_A, QUADSPI_BK1_IO2, ETH_MII_TXD3, FMC_A23, EVENTOUT | - |
| 2 | B3 | C10 | 2 | A1 | 2 | 2 | A2 | PE3 | I/O | FT | - | TRACED0, SAI1_SD_B, FMC_A19, EVENTOUT | - |
| 3 | C3 | B11 | 3 | B1 | 3 | 3 | A1 | PE4 | I/O | FT | - | TRACED1, SPI4_NSS, SAI1_FS_A, FMC_A20, DCMI_D4, LCD_B0, EVENTOUT | - |

Table 10. STM32F745xx and STM32F746xx pin and ball definition (continued)

| Pin Number | | | | | | | | Pin name (function after reset)(1) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LQFP100 | TFBGA100 | WLCSP143 | LQFP144 | UFBGA176 | LQFP176 | LQFP208 | TFBGA216 | | | | | | |
| 4 | D3 | D9 | 4 | B2 | 4 | 4 | B1 | PE5 | I/O | FT | - | TRACED2, TIM9_CH1, SPI4_MISO, SAI1_SCK_A, FMC_A21, DCMI_D6, LCD_G0, EVENTOUT | - |
| 5 | E3 | E8 | 5 | B3 | 5 | 5 | B2 | PE6 | I/O | FT | - | TRACED3, TIM1_BKIN2, TIM9_CH2, SPI4_MOSI, SAI1_SD_A, SAI2_MCK_B, FMC_A22, DCMI_D7, LCD_G1, EVENTOUT | - |
| - | - | - | - | - | - | - | G6 | VSS | S | - | - | - | - |
| - | - | - | - | - | - | - | F5 | VDD | S | - | - | - | - |
| 6 | B2 | C11 | 6 | C1 | 6 | 6 | C1 | VBAT | S | - | - | - | - |
| - | - | - | - | D2 | 7 | 7 | C2 | PI8 | I/O | FT | (2)(3) | EVENTOUT | RTC_TAMP2/ RTC_TS,WKUP5 |
| 7 | A2 | D10 | 7 | D1 | 8 | 8 | D1 | PC13 | I/O | FT | (2)(3) | EVENTOUT | RTC_TAMP1/ RTC_TS/RTC_OUT,WKUP4 |
| 8 | A1 | D11 | 8 | E1 | 9 | 9 | E1 | PC14-OSC32_IN(PC14) | I/O | FT | (2)(3) | EVENTOUT | OSC32_IN |
| 9 | B1 | E11 | 9 | F1 | 10 | 10 | F1 | PC15-OSC32_OUT(PC15) | I/O | FT | (2)(3) | EVENTOUT | OSC32_OUT |
| - | - | - | - | - | - | - | G5 | VDD | S | - | - | - | - |
| - | - | - | - | D3 | 11 | 11 | E4 | PI9 | I/O | FT | - | CAN1_RX, FMC_D30, LCD_VSYNC, EVENTOUT | - |
| - | - | - | - | E3 | 12 | 12 | D5 | PI10 | I/O | FT | - | ETH_MII_RX_ER, FMC_D31, LCD_HSYNC, EVENTOUT | - |

Table 10. STM32F745xx and STM32F746xx pin and ball definition (continued)

| Pin Number | | | | | | | | Pin name (function after reset)(1) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LQFP100 | TFBGA100 | WLCSP143 | LQFP144 | UFBGA176 | LQFP176 | LQFP208 | TFBGA216 | | | | | | |
| - | - | - | - | E4 | 13 | 13 | F3 | PI11 | I/O | FT | - | OTG_HS_ULPI_DIR, EVENTOUT | WKUP6 |
| - | - | E7 | - | F2 | 14 | 14 | F2 | VSS | S | - | - | - | - |
| - | - | E10 | - | F3 | 15 | 15 | F4 | VDD | S | - | - | - | - |
| - | - | F11 | 10 | E2 | 16 | 16 | D2 | PF0 | I/O | FT | - | I2C2_SDA, FMC_A0, EVENTOUT | - |
| - | - | E9 | 11 | H3 | 17 | 17 | E2 | PF1 | I/O | FT | - | I2C2_SCL, FMC_A1, EVENTOUT | - |
| - | - | F10 | 12 | H2 | 18 | 18 | G2 | PF2 | I/O | FT | - | I2C2_SMBA, FMC_A2, EVENTOUT | - |
| - | - | - | - | - | - | 19 | E3 | PI12 | I/O | FT | - | LCD_HSYNC, EVENTOUT | - |
| - | - | - | - | - | - | 20 | G3 | PI13 | I/O | FT | - | LCD_VSYNC, EVENTOUT | - |
| - | - | - | - | - | - | 21 | H3 | PI14 | I/O | FT | - | LCD_CLK, EVENTOUT | - |
| - | - | G11 | 13 | J2 | 19 | 22 | H2 | PF3 | I/O | FT | - | FMC_A3, EVENTOUT | ADC3_IN9 |
| - | - | F9 | 14 | J3 | 20 | 23 | J2 | PF4 | I/O | FT | - | FMC_A4, EVENTOUT | ADC3_IN14 |
| - | - | F8 | 15 | K3 | 21 | 24 | K3 | PF5 | I/O | FT | - | FMC_A5, EVENTOUT | ADC3_IN15 |
| 10 | C2 | H7 | 16 | G2 | 22 | 25 | H6 | VSS | S | - | - | - | - |
| 11 | D2 | - | 17 | G3 | 23 | 26 | H5 | VDD | S | - | - | - | - |
| - | - | G10 | 18 | K2 | 24 | 27 | K2 | PF6 | I/O | FT | - | TIM10_CH1, SPI5_NSS, SAI1_SD_B, UART7_Rx, QUADSPI_BK1_IO3, EVENTOUT | ADC3_IN4 |
| - | - | F7 | 19 | K1 | 25 | 28 | K1 | PF7 | I/O | FT | - | TIM11_CH1, SPI5_SCK, SAI1_MCLK_B, UART7_Tx, QUADSPI_BK1_IO2, EVENTOUT | ADC3_IN5 |

Table 10. STM32F745xx and STM32F746xx pin and ball definition (continued)

| Pin Number | | | | | | | | Pin name (function after reset)[1] | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LQFP100 | TFBGA100 | WLCSP143 | LQFP144 | UFBGA176 | LQFP176 | LQFP208 | TFBGA216 | | | | | | |
| - | - | H11 | 20 | L3 | 26 | 29 | L3 | PF8 | I/O | FT | - | SPI5_MISO, SAI1_SCK_B, UART7_RTS, TIM13_CH1, QUADSPI_BK1_IO0, EVENTOUT | ADC3_IN6 |
| - | - | G8 | 21 | L2 | 27 | 30 | L2 | PF9 | I/O | FT | - | SPI5_MOSI, SAI1_FS_B, UART7_CTS, TIM14_CH1, QUADSPI_BK1_IO1, EVENTOUT | ADC3_IN7 |
| - | - | G9 | 22 | L1 | 28 | 31 | L1 | PF10 | I/O | FT | - | DCMI_D11, LCD_DE, EVENTOUT | ADC3_IN8 |
| 12 | C1 | J11 | 23 | G1 | 29 | 32 | G1 | PH0-OSC_IN(PH0) | I/O | FT | - | EVENTOUT | OSC_IN[4] |
| 13 | D1 | H10 | 24 | H1 | 30 | 33 | H1 | PH1-OSC_OUT(PH1) | I/O | FT | - | EVENTOUT | OSC_OUT[4] |
| 14 | E1 | H9 | 25 | J1 | 31 | 34 | J1 | NRST | I/O | RST | - | - | - |
| 15 | F1 | H8 | 26 | M2 | 32 | 35 | M2 | PC0 | I/O | FT | [4] | SAI2_FS_B, OTG_HS_ULPI_STP, FMC_SDNWE, LCD_R5, EVENTOUT | ADC123_IN10 |
| 16 | F2 | K11 | 27 | M3 | 33 | 36 | M3 | PC1 | I/O | FT | [4] | TRACED0, SPI2_MOSI/I2S2_SD, SAI1_SD_A, ETH_MDC, EVENTOUT | ADC123_IN11, RTC_TAMP3, WKUP3 |
| 17 | E2 | J10 | 28 | M4 | 34 | 37 | M4 | PC2 | I/O | FT | [4] | SPI2_MISO, OTG_HS_ULPI_DIR, ETH_MII_TXD2, FMC_SDNE0, EVENTOUT | ADC123_IN12 |

Table 10. STM32F745xx and STM32F746xx pin and ball definition (continued)

| Pin Number | | | | | | | | Pin name (function after reset)[(1)] | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LQFP100 | TFBGA100 | WLCSP143 | LQFP144 | UFBGA176 | LQFP176 | LQFP208 | TFBGA216 | | | | | | |
| 18 | F3 | J9 | 29 | M5 | 35 | 38 | L4 | PC3 | I/O | FT | (4) | SPI2_MOSI/I2S2_SD, OTG_HS_ULPI_NXT, ETH_MII_TX_CLK, FMC_SDCKE0, EVENTOUT | ADC123_IN13 |
| - | - | G7 | 30 | G3 | 36 | 39 | J5 | VDD | S | - | - | - | - |
| - | - | - | - | - | - | - | J6 | VSS | S | - | - | - | - |
| 19 | G1 | K10 | 31 | M1 | 37 | 40 | M1 | VSSA | S | - | - | - | - |
| - | - | - | - | N1 | - | - | N1 | VREF- | S | - | - | - | - |
| 20 | - | L11 | 32 | P1 | 38 | 41 | P1 | VREF+ | S | - | - | - | - |
| 21 | H1 | L10 | 33 | R1 | 39 | 42 | R1 | VDDA | S | - | - | - | - |
| 22 | G2 | K9 | 34 | N3 | 40 | 43 | N3 | PA0-WKUP(PA0) | I/O | FT | (5) | TIM2_CH1/TIM2_ETR, TIM5_CH1, TIM8_ETR, USART2_CTS, UART4_TX, SAI2_SD_B, ETH_MII_CRS, EVENTOUT | ADC123_IN0, WKUP1[(4)] |
| 23 | H2 | K8 | 35 | N2 | 41 | 44 | N2 | PA1 | I/O | FT | (4) | TIM2_CH2, TIM5_CH2, USART2_RTS, UART4_RX, QUADSPI_BK1_IO3, SAI2_MCK_B, ETH_MII_RX_CLK/ETH_RMII_REF_CLK, LCD_R2, EVENTOUT | ADC123_IN1 |
| 24 | J2 | L9 | 36 | P2 | 42 | 45 | P2 | PA2 | I/O | FT | (4) | TIM2_CH3, TIM5_CH3, TIM9_CH1, USART2_TX, SAI2_SCK_B, ETH_MDIO, LCD_R1, EVENTOUT | ADC123_IN2, WKUP2 |
| - | - | - | - | F4 | 43 | 46 | K4 | PH2 | I/O | FT | | LPTIM1_IN2, QUADSPI_BK2_IO0, SAI2_SCK_B, ETH_MII_CRS, FMC_SDCKE0, LCD_R0, EVENTOUT | - |

Table 10. STM32F745xx and STM32F746xx pin and ball definition (continued)

| Pin Number | | | | | | | | Pin name (function after reset)(1) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LQFP100 | TFBGA100 | WLCSP143 | LQFP144 | UFBGA176 | LQFP176 | LQFP208 | TFBGA216 | | | | | | |
| - | - | - | - | G4 | 44 | 47 | J4 | PH3 | I/O | FT | - | QUADSPI_BK2_IO1, SAI2_MCK_B, ETH_MII_COL, FMC_SDNE0, LCD_R1, EVENTOUT | - |
| - | - | - | - | H4 | 45 | 48 | H4 | PH4 | I/O | FT | - | I2C2_SCL, OTG_HS_ULPI_NXT, EVENTOUT | - |
| - | - | - | - | J4 | 46 | 49 | J3 | PH5 | I/O | FT | - | I2C2_SDA, SPI5_NSS, FMC_SDNWE, EVENTOUT | - |
| 25 | K2 | M11 | 37 | R2 | 47 | 50 | R2 | PA3 | I/O | FT | (4) | TIM2_CH4, TIM5_CH4, TIM9_CH2, USART2_RX, OTG_HS_ULPI_D0, ETH_MII_COL, LCD_B5, EVENTOUT | ADC123_IN3 |
| 26 | J1 | - | 38 | - | - | 51 | K6 | VSS | S | - | - | - | - |
| - | E6 | N11 | - | L4 | 48 | - | L5 | BYPASS_REG | I | FT | - | - | - |
| 27 | K1 | J8 | 39 | K4 | 49 | 52 | K5 | VDD | S | - | - | - | - |
| 28 | G3 | M10 | 40 | N4 | 50 | 53 | N4 | PA4 | I/O | TTa | (4) | SPI1_NSS/I2S1_WS, SPI3_NSS/I2S3_WS, USART2_CK, OTG_HS_SOF, DCMI_HSYNC, LCD_VSYNC, EVENTOUT | ADC12_IN4, DAC_OUT1 |
| 29 | H3 | M9 | 41 | P4 | 51 | 54 | P4 | PA5 | I/O | TTa | (4) | TIM2_CH1/TIM2_ETR, TIM8_CH1N, SPI1_SCK/I2S1_CK, OTG_HS_ULPI_CK, LCD_R4, EVENTOUT | ADC12_IN5, DAC_OUT2 |
| 30 | J3 | N10 | 42 | P3 | 52 | 55 | P3 | PA6 | I/O | FT | (4) | TIM1_BKIN, TIM3_CH1, TIM8_BKIN, SPI1_MISO, TIM13_CH1, DCMI_PIXCLK, LCD_G2, EVENTOUT | ADC12_IN6 |

**Table 10. STM32F745xx and STM32F746xx pin and ball definition (continued)**

| Pin Number | | | | | | | | Pin name (function after reset)(1) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LQFP100 | TFBGA100 | WLCSP143 | LQFP144 | UFBGA176 | LQFP176 | LQFP208 | TFBGA216 | | | | | | |
| 31 | K3 | L8 | 43 | R3 | 53 | 56 | R3 | PA7 | I/O | FT | (4) | TIM1_CH1N, TIM3_CH2, TIM8_CH1N, SPI1_MOSI/I2S1_SD, TIM14_CH1, ETH_MII_RX_DV/ETH_RMII_CRS_DV, FMC_SDNWE, EVENTOUT | ADC12_IN7 |
| 32 | G4 | M8 | 44 | N5 | 54 | 57 | N5 | PC4 | I/O | FT | (4) | I2S1_MCK, SPDIFRX_IN2, ETH_MII_RXD0/ETH_RMII_RXD0, FMC_SDNE0, EVENTOUT | ADC12_IN14 |
| 33 | H4 | N9 | 45 | P5 | 55 | 58 | P5 | PC5 | I/O | FT | (4) | SPDIFRX_IN3, ETH_MII_RXD1/ETH_RMII_RXD1, FMC_SDCKE0, EVENTOUT | ADC12_IN15 |
| - | - | J7 | - | - | - | 59 | L7 | VDD | S | - | - | - | - |
| - | - | - | - | - | - | 60 | L6 | VSS | S | - | - | - | - |
| 34 | J4 | N8 | 46 | R5 | 56 | 61 | R5 | PB0 | I/O | FT | (4) | TIM1_CH2N, TIM3_CH3, TIM8_CH2N, UART4_CTS, LCD_R3, OTG_HS_ULPI_D1, ETH_MII_RXD2, EVENTOUT | ADC12_IN8 |
| 35 | K4 | K7 | 47 | R4 | 57 | 62 | R4 | PB1 | I/O | FT | (4) | TIM1_CH3N, TIM3_CH4, TIM8_CH3N, LCD_R6, OTG_HS_ULPI_D2, ETH_MII_RXD3, EVENTOUT | ADC12_IN9 |
| 36 | G5 | L7 | 48 | M6 | 58 | 63 | M5 | PB2 | I/O | FT | - | SAI1_SD_A, SPI3_MOSI/I2S3_SD, QUADSPI_CLK, EVENTOUT | - |
| - | - | - | - | - | - | 64 | G4 | PI15 | I/O | FT | - | LCD_R0, EVENTOUT | - |
| - | - | - | - | - | - | 65 | R6 | PJ0 | I/O | FT | - | LCD_R1, EVENTOUT | - |
| - | - | - | - | - | - | 66 | R7 | PJ1 | I/O | FT | - | LCD_R2, EVENTOUT | - |

Table 10. STM32F745xx and STM32F746xx pin and ball definition (continued)

| Pin Number | | | | | | | | Pin name (function after reset)[1] | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LQFP100 | TFBGA100 | WLCSP143 | LQFP144 | UFBGA176 | LQFP176 | LQFP208 | TFBGA216 | | | | | | |
| - | - | - | - | - | - | 67 | P7 | PJ2 | I/O | FT | - | LCD_R3, EVENTOUT | - |
| - | - | - | - | - | - | 68 | N8 | PJ3 | I/O | FT | - | LCD_R4, EVENTOUT | - |
| - | - | - | - | - | - | 69 | M9 | PJ4 | I/O | FT | - | LCD_R5, EVENTOUT | - |
| - | - | M7 | 49 | R6 | 59 | 70 | P8 | PF11 | I/O | FT | - | SPI5_MOSI, SAI2_SD_B, FMC_SDNRAS, DCMI_D12, EVENTOUT | - |
| - | - | N7 | 50 | P6 | 60 | 71 | M6 | PF12 | I/O | FT | - | FMC_A6, EVENTOUT | - |
| - | - | - | 51 | M8 | 61 | 72 | K7 | VSS | S | - | - | - | - |
| - | - | - | 52 | N8 | 62 | 73 | L8 | VDD | S | - | - | - | - |
| - | - | K6 | 53 | N6 | 63 | 74 | N6 | PF13 | I/O | FT | - | I2C4_SMBA, FMC_A7, EVENTOUT | - |
| - | - | L6 | 54 | R7 | 64 | 75 | P6 | PF14 | I/O | FT | - | I2C4_SCL, FMC_A8, EVENTOUT | - |
| - | - | M6 | 55 | P7 | 65 | 76 | M8 | PF15 | I/O | FT | - | I2C4_SDA, FMC_A9, EVENTOUT | - |
| - | - | N6 | 56 | N7 | 66 | 77 | N7 | PG0 | I/O | FT | - | FMC_A10, EVENTOUT | - |
| - | - | K5 | 57 | M7 | 67 | 78 | M7 | PG1 | I/O | FT | - | FMC_A11, EVENTOUT | - |
| 37 | H5 | L5 | 58 | R8 | 68 | 79 | R8 | PE7 | I/O | FT | - | TIM1_ETR, UART7_Rx, QUADSPI_BK2_IO0, FMC_D4, EVENTOUT | - |
| 38 | J5 | M5 | 59 | P8 | 69 | 80 | N9 | PE8 | I/O | FT | - | TIM1_CH1N, UART7_Tx, QUADSPI_BK2_IO1, FMC_D5, EVENTOUT | - |
| 39 | K5 | N5 | 60 | P9 | 70 | 81 | P9 | PE9 | I/O | FT | - | TIM1_CH1, UART7_RTS, QUADSPI_BK2_IO2, FMC_D6, EVENTOUT | - |
| - | - | H3 | 61 | M9 | 71 | 82 | K8 | VSS | S | - | - | - | - |
| - | - | J5 | 62 | N9 | 72 | 83 | L9 | VDD | S | - | - | - | - |
| 40 | G6 | J4 | 63 | R9 | 73 | 84 | R9 | PE10 | I/O | FT | - | TIM1_CH2N, UART7_CTS, QUADSPI_BK2_IO3, FMC_D7, EVENTOUT | - |

**Table 10. STM32F745xx and STM32F746xx pin and ball definition (continued)**

| Pin Number | | | | | | | | Pin name (function after reset)[(1)] | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LQFP100 | TFBGA100 | WLCSP143 | LQFP144 | UFBGA176 | LQFP176 | LQFP208 | TFBGA216 | | | | | | |
| 41 | H6 | K4 | 64 | P10 | 74 | 85 | P10 | PE11 | I/O | FT | - | TIM1_CH2, SPI4_NSS, SAI2_SD_B, FMC_D8, LCD_G3, EVENTOUT | - |
| 42 | J6 | L4 | 65 | R10 | 75 | 86 | R10 | PE12 | I/O | FT | - | TIM1_CH3N, SPI4_SCK, SAI2_SCK_B, FMC_D9, LCD_B4, EVENTOUT | - |
| 43 | K6 | N4 | 66 | N11 | 76 | 87 | R12 | PE13 | I/O | FT | - | TIM1_CH3, SPI4_MISO, SAI2_FS_B, FMC_D10, LCD_DE, EVENTOUT | - |
| 44 | G7 | M4 | 67 | P11 | 77 | 88 | P11 | PE14 | I/O | FT | - | TIM1_CH4, SPI4_MOSI, SAI2_MCK_B, FMC_D11, LCD_CLK, EVENTOUT | - |
| 45 | H7 | L3 | 68 | R11 | 78 | 89 | R11 | PE15 | I/O | FT | - | TIM1_BKIN, FMC_D12, LCD_R7, EVENTOUT | - |
| 46 | J7 | M3 | 69 | R12 | 79 | 90 | P12 | PB10 | I/O | FT | - | TIM2_CH3, I2C2_SCL, SPI2_SCK/I2S2_CK, USART3_TX, OTG_HS_ULPI_D3, ETH_MII_RX_ER, LCD_G4, EVENTOUT | - |
| 47 | K7 | N3 | 70 | R13 | 80 | 91 | R13 | PB11 | I/O | FT | - | TIM2_CH4, I2C2_SDA, USART3_RX, OTG_HS_ULPI_D4, ETH_MII_TX_EN/ETH_RMII_TX_EN, LCD_G5, EVENTOUT | - |
| 48 | F8 | N2 | 71 | M10 | 81 | 92 | L11 | VCAP_1 | S | - | - | - | - |
| 49 | - | H2 | - | - | - | 93 | K9 | VSS | S | - | - | - | - |
| 50 | - | J6 | 72 | N10 | 82 | 94 | L10 | VDD | S | - | - | - | - |
| - | - | - | - | - | - | 95 | M14 | PJ5 | I/O | FT | - | LCD_R6, EVENTOUT | - |
| - | - | - | - | M11 | 83 | 96 | P13 | PH6 | I/O | FT | - | I2C2_SMBA, SPI5_SCK, TIM12_CH1, ETH_MII_RXD2, FMC_SDNE1, DCMI_D8, EVENTOUT | - |

Table 10. STM32F745xx and STM32F746xx pin and ball definition (continued)

| Pin Number | | | | | | | | Pin name (function after reset)[(1)] | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LQFP100 | TFBGA100 | WLCSP143 | LQFP144 | UFBGA176 | LQFP176 | LQFP208 | TFBGA216 | | | | | | |
| - | - | - | - | N12 | 84 | 97 | N13 | PH7 | I/O | FT | - | I2C3_SCL, SPI5_MISO, ETH_MII_RXD3, FMC_SDCKE1, DCMI_D9, EVENTOUT | - |
| - | - | - | - | M12 | 85 | 98 | P14 | PH8 | I/O | FT | - | I2C3_SDA, FMC_D16, DCMI_HSYNC, LCD_R2, EVENTOUT | - |
| - | - | - | - | M13 | 86 | 99 | N14 | PH9 | I/O | FT | - | I2C3_SMBA, TIM12_CH2, FMC_D17, DCMI_D0, LCD_R3, EVENTOUT | - |
| - | - | - | - | L13 | 87 | 100 | P15 | PH10 | I/O | FT | - | TIM5_CH1, I2C4_SMBA, FMC_D18, DCMI_D1, LCD_R4, EVENTOUT | - |
| - | - | - | - | L12 | 88 | 101 | N15 | PH11 | I/O | FT | - | TIM5_CH2, I2C4_SCL, FMC_D19, DCMI_D2, LCD_R5, EVENTOUT | - |
| - | - | - | - | K12 | 89 | 102 | M15 | PH12 | I/O | FT | - | TIM5_CH3, I2C4_SDA, FMC_D20, DCMI_D3, LCD_R6, EVENTOUT | - |
| - | - | - | - | H12 | 90 | - | K10 | VSS | S | - | - | - | - |
| - | - | - | - | J12 | 91 | 103 | K11 | VDD | S | - | - | - | - |
| 51 | K8 | M2 | 73 | P12 | 92 | 104 | L13 | PB12 | I/O | FT | - | TIM1_BKIN, I2C2_SMBA, SPI2_NSS/I2S2_WS, USART3_CK, CAN2_RX, OTG_HS_ULPI_D5, ETH_MII_TXD0/ETH_RMII_TXD0, OTG_HS_ID, EVENTOUT | - |
| 52 | J8 | N1 | 74 | P13 | 93 | 105 | K14 | PB13 | I/O | FT | - | TIM1_CH1N, SPI2_SCK/I2S2_CK, USART3_CTS, CAN2_TX, OTG_HS_ULPI_D6, ETH_MII_TXD1/ETH_RMII_TXD1, EVENTOUT | OTG_HS_VBUS |

**Table 10. STM32F745xx and STM32F746xx pin and ball definition (continued)**

| Pin Number | | | | | | | | Pin name (function after reset)(1) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LQFP100 | TFBGA100 | WLCSP143 | LQFP144 | UFBGA176 | LQFP176 | LQFP208 | TFBGA216 | | | | | | |
| 53 | H10 | K3 | 75 | R14 | 94 | 106 | R14 | PB14 | I/O | FT | - | TIM1_CH2N, TIM8_CH2N, SPI2_MISO, USART3_RTS, TIM12_CH1, OTG_HS_DM, EVENTOUT | - |
| 54 | G10 | J3 | 76 | R15 | 95 | 107 | R15 | PB15 | I/O | FT | - | RTC_REFIN, TIM1_CH3N, TIM8_CH3N, SPI2_MOSI/I2S2_SD, TIM12_CH2, OTG_HS_DP, EVENTOUT | - |
| 55 | K9 | L2 | 77 | P15 | 96 | 108 | L15 | PD8 | I/O | FT | - | USART3_TX, SPDIFRX_IN11, FMC_D13, EVENTOUT | - |
| 56 | J9 | M1 | 78 | P14 | 97 | 109 | L14 | PD9 | I/O | FT | - | USART3_RX, FMC_D14, EVENTOUT | - |
| 57 | H9 | H4 | 79 | N15 | 98 | 110 | K15 | PD10 | I/O | FT | - | USART3_CK, FMC_D15, LCD_B3, EVENTOUT | - |
| 58 | G9 | K2 | 80 | N14 | 99 | 111 | N10 | PD11 | I/O | FT | - | I2C4_SMBA, USART3_CTS, QUADSPI_BK1_IO0, SAI2_SD_A, FMC_A16/FMC_CLE, EVENTOUT | - |
| 59 | K10 | H6 | 81 | N13 | 100 | 112 | M10 | PD12 | I/O | FT | - | TIM4_CH1, LPTIM1_IN1, I2C4_SCL, USART3_RTS, QUADSPI_BK1_IO1, SAI2_FS_A, FMC_A17/FMC_ALE, EVENTOUT | - |
| 60 | J10 | H5 | 82 | M15 | 101 | 113 | M11 | PD13 | I/O | FT | - | TIM4_CH2, LPTIM1_OUT, I2C4_SDA, QUADSPI_BK1_IO3, SAI2_SCK_A, FMC_A18, EVENTOUT | - |

Table 10. STM32F745xx and STM32F746xx pin and ball definition (continued)

| Pin Number | | | | | | | | Pin name (function after reset)(1) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LQFP100 | TFBGA100 | WLCSP143 | LQFP144 | UFBGA176 | LQFP176 | LQFP208 | TFBGA216 | | | | | | |
| - | - | - | 83 | - | 102 | 114 | J10 | VSS | S | - | - | - | - |
| - | - | L1 | 84 | J13 | 103 | 115 | J11 | VDD | S | - | - | - | - |
| 61 | H8 | J2 | 85 | M14 | 104 | 116 | L12 | PD14 | I/O | FT | - | TIM4_CH3, UART8_CTS, FMC_D0, EVENTOUT | - |
| 62 | G8 | K1 | 86 | L14 | 105 | 117 | K13 | PD15 | I/O | FT | - | TIM4_CH4, UART8_RTS, FMC_D1, EVENTOUT | - |
| - | - | - | - | - | - | 118 | K12 | PJ6 | I/O | FT | - | LCD_R7, EVENTOUT | - |
| - | - | - | - | - | - | 119 | J12 | PJ7 | I/O | FT | - | LCD_G0, EVENTOUT | - |
| - | - | - | - | - | - | 120 | H12 | PJ8 | I/O | FT | - | LCD_G1, EVENTOUT | - |
| - | - | - | - | - | - | 121 | J13 | PJ9 | I/O | FT | - | LCD_G2, EVENTOUT | - |
| - | - | - | - | - | - | 122 | H13 | PJ10 | I/O | FT | - | LCD_G3, EVENTOUT | - |
| - | - | - | - | - | - | 123 | G12 | PJ11 | I/O | FT | - | LCD_G4, EVENTOUT | - |
| - | - | - | - | - | - | 124 | H11 | VDD | S | - | - | - | - |
| - | - | - | - | - | - | 125 | H10 | VSS | S | - | - | - | - |
| - | - | - | - | - | - | 126 | G13 | PK0 | I/O | FT | - | LCD_G5, EVENTOUT | - |
| - | - | - | - | - | - | 127 | F12 | PK1 | I/O | FT | - | LCD_G6, EVENTOUT | - |
| - | - | - | - | - | - | 128 | F13 | PK2 | I/O | FT | - | LCD_G7, EVENTOUT | - |
| - | - | J1 | 87 | L15 | 106 | 129 | M13 | PG2 | I/O | FT | - | FMC_A12, EVENTOUT | - |
| - | - | G3 | 88 | K15 | 107 | 130 | M12 | PG3 | I/O | FT | - | FMC_A13, EVENTOUT | - |
| - | - | G5 | 89 | K14 | 108 | 131 | N12 | PG4 | I/O | FT | - | FMC_A14/FMC_BA0, EVENTOUT | - |
| - | - | G6 | 90 | K13 | 109 | 132 | N11 | PG5 | I/O | FT | - | FMC_A15/FMC_BA1, EVENTOUT | - |
| - | - | G4 | 91 | J15 | 110 | 133 | J15 | PG6 | I/O | FT | - | DCMI_D12, LCD_R7, EVENTOUT | - |
| - | - | H1 | 92 | J14 | 111 | 134 | J14 | PG7 | I/O | FT | - | USART6_CK, FMC_INT, DCMI_D13, LCD_CLK, EVENTOUT | - |

**Table 10. STM32F745xx and STM32F746xx pin and ball definition (continued)**

| Pin Number | | | | | | | | Pin name (function after reset)[1] | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LQFP100 | TFBGA100 | WLCSP143 | LQFP144 | UFBGA176 | LQFP176 | LQFP208 | TFBGA216 | | | | | | |
| - | - | G2 | 93 | H14 | 112 | 135 | H14 | PG8 | I/O | FT | - | SPI6_NSS, SPDIFRX_IN2, USART6_RTS, ETH_PPS_OUT, FMC_SDCLK, EVENTOUT | - |
| - | - | D2 | 94 | G12 | 113 | 136 | G10 | VSS | S | - | - | - | - |
| - | F6 | G1 | 95 | H13 | 114 | 137 | G11 | VDDUSB | S | - | - | - | - |
| 63 | F10 | F2 | 96 | H15 | 115 | 138 | H15 | PC6 | I/O | FT | - | TIM3_CH1, TIM8_CH1, I2S2_MCK, USART6_TX, SDMMC1_D6, DCMI_D0, LCD_HSYNC, EVENTOUT | - |
| 64 | E10 | F3 | 97 | G15 | 116 | 139 | G15 | PC7 | I/O | FT | - | TIM3_CH2, TIM8_CH2, I2S3_MCK, USART6_RX, SDMMC1_D7, DCMI_D1, LCD_G6, EVENTOUT | - |
| 65 | F9 | E4 | 98 | G14 | 117 | 140 | G14 | PC8 | I/O | FT | - | TRACED1, TIM3_CH3, TIM8_CH3, UART5_RTS, USART6_CK, SDMMC1_D0, DCMI_D2, EVENTOUT | - |
| 66 | E9 | E3 | 99 | F14 | 118 | 141 | F14 | PC9 | I/O | FT | - | MCO2, TIM3_CH4, TIM8_CH4, I2C3_SDA, I2S_CKIN, UART5_CTS, QUADSPI_BK1_IO0, SDMMC1_D1, DCMI_D3, EVENTOUT | - |
| 67 | D9 | F1 | 100 | F15 | 119 | 142 | F15 | PA8 | I/O | FT | - | MCO1, TIM1_CH1, TIM8_BKIN2, I2C3_SCL, USART1_CK, OTG_FS_SOF, LCD_R6, EVENTOUT | - |
| 68 | C9 | E2 | 101 | E15 | 120 | 143 | E15 | PA9 | I/O | FT | - | TIM1_CH2, I2C3_SMBA, SPI2_SCK/I2S2_CK, USART1_TX, DCMI_D0, EVENTOUT | OTG_FS_VBUS |

**Table 10. STM32F745xx and STM32F746xx pin and ball definition (continued)**

| Pin Number | | | | | | | | Pin name (function after reset)(1) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LQFP100 | TFBGA100 | WLCSP143 | LQFP144 | UFBGA176 | LQFP176 | LQFP208 | TFBGA216 | | | | | | |
| 69 | D10 | D5 | 102 | D15 | 121 | 144 | D15 | PA10 | I/O | FT | - | TIM1_CH3, USART1_RX, OTG_FS_ID, DCMI_D1, EVENTOUT | - |
| 70 | C10 | D4 | 103 | C15 | 122 | 145 | C15 | PA11 | I/O | FT | - | TIM1_CH4, USART1_CTS, CAN1_RX, OTG_FS_DM, LCD_R4, EVENTOUT | - |
| 71 | B10 | E1 | 104 | B15 | 123 | 146 | B15 | PA12 | I/O | FT | - | TIM1_ETR, USART1_RTS, SAI2_FS_B, CAN1_TX, OTG_FS_DP, LCD_R5, EVENTOUT | - |
| 72 | A10 | D3 | 105 | A15 | 124 | 147 | A15 | PA13(JTMS-SWDIO) | I/O | FT | - | JTMS-SWDIO, EVENTOUT | - |
| 73 | E7 | D1 | 106 | F13 | 125 | 148 | E11 | VCAP_2 | S | - | - | - | - |
| 74 | E5 | D2 | 107 | F12 | 126 | 149 | F10 | VSS | S | - | - | - | - |
| 75 | F5 | C1 | 108 | G13 | 127 | 150 | F11 | VDD | S | - | - | - | - |
| - | - | - | - | E12 | 128 | 151 | E12 | PH13 | I/O | FT | - | TIM8_CH1N, CAN1_TX, FMC_D21, LCD_G2, EVENTOUT | - |
| - | - | - | - | E13 | 129 | 152 | E13 | PH14 | I/O | FT | - | TIM8_CH2N, FMC_D22, DCMI_D4, LCD_G3, EVENTOUT | - |
| - | - | - | - | D13 | 130 | 153 | D13 | PH15 | I/O | FT | - | TIM8_CH3N, FMC_D23, DCMI_D11, LCD_G4, EVENTOUT | - |
| - | - | - | - | E14 | 131 | 154 | E14 | PI0 | I/O | FT | - | TIM5_CH4, SPI2_NSS/I2S2_WS, FMC_D24, DCMI_D13, LCD_G5, EVENTOUT | - |
| - | - | - | - | D14 | 132 | 155 | D14 | PI1 | I/O | FT | - | TIM8_BKIN2, SPI2_SCK/I2S2_CK, FMC_D25, DCMI_D8, LCD_G6, EVENTOUT | - |

**Table 10. STM32F745xx and STM32F746xx pin and ball definition (continued)**

| Pin Number | | | | | | | | Pin name (function after reset)(1) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LQFP100 | TFBGA100 | WLCSP143 | LQFP144 | UFBGA176 | LQFP176 | LQFP208 | TFBGA216 | | | | | | |
| - | - | - | - | C14 | 133 | 156 | C14 | PI2 | I/O | FT | - | TIM8_CH4, SPI2_MISO, FMC_D26, DCMI_D9, LCD_G7, EVENTOUT | - |
| - | - | - | - | C13 | 134 | 157 | C13 | PI3 | I/O | FT | - | TIM8_ETR, SPI2_MOSI/I2S2_SD, FMC_D27, DCMI_D10, EVENTOUT | - |
| - | - | F5 | - | D9 | 135 | - | F9 | VSS | S | - | - | - | - |
| - | - | A1 | - | C9 | 136 | 158 | E10 | VDD | S | - | - | - | - |
| 76 | A9 | B1 | 109 | A14 | 137 | 159 | A14 | PA14(JTCK-SWCLK) | I/O | FT | - | JTCK-SWCLK, EVENTOUT | - |
| 77 | A8 | C2 | 110 | A13 | 138 | 160 | A13 | PA15(JTDI) | I/O | FT | - | JTDI, TIM2_CH1/TIM2_ETR, HDMI-CEC, SPI1_NSS/I2S1_WS, SPI3_NSS/I2S3_WS, UART4_RTS, EVENTOUT | - |
| 78 | B9 | A2 | 111 | B14 | 139 | 161 | B14 | PC10 | I/O | FT | - | SPI3_SCK/I2S3_CK, USART3_TX, UART4_TX, QUADSPI_BK1_IO1, SDMMC1_D2, DCMI_D8, LCD_R2, EVENTOUT | - |
| 79 | B8 | B2 | 112 | B13 | 140 | 162 | B13 | PC11 | I/O | FT | - | SPI3_MISO, USART3_RX, UART4_RX, QUADSPI_BK2_NCS, SDMMC1_D3, DCMI_D4, EVENTOUT | - |
| 80 | C8 | C3 | 113 | A12 | 141 | 163 | A12 | PC12 | I/O | FT | - | TRACED3, SPI3_MOSI/I2S3_SD, USART3_CK, UART5_TX, SDMMC1_CK, DCMI_D9, EVENTOUT | - |

Table 10. STM32F745xx and STM32F746xx pin and ball definition (continued)

| Pin Number | | | | | | | | Pin name (function after reset)(1) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LQFP100 | TFBGA100 | WLCSP143 | LQFP144 | UFBGA176 | LQFP176 | LQFP208 | TFBGA216 | | | | | | |
| 81 | D8 | B3 | 114 | B12 | 142 | 164 | B12 | PD0 | I/O | FT | - | CAN1_RX, FMC_D2, EVENTOUT | - |
| 82 | E8 | C4 | 115 | C12 | 143 | 165 | C12 | PD1 | I/O | FT | - | CAN1_TX, FMC_D3, EVENTOUT | - |
| 83 | B7 | A3 | 116 | D12 | 144 | 166 | D12 | PD2 | I/O | FT | - | TRACED2, TIM3_ETR, UART5_RX, SDMMC1_CMD, DCMI_D11, EVENTOUT | - |
| 84 | C7 | B4 | 117 | D11 | 145 | 167 | C11 | PD3 | I/O | FT | - | SPI2_SCK/I2S2_CK, USART2_CTS, FMC_CLK, DCMI_D5, LCD_G7, EVENTOUT | - |
| 85 | D7 | B5 | 118 | D10 | 146 | 168 | D11 | PD4 | I/O | FT | - | USART2_RTS, FMC_NOE, EVENTOUT | - |
| 86 | B6 | A4 | 119 | C11 | 147 | 169 | C10 | PD5 | I/O | FT | - | USART2_TX, FMC_NWE, EVENTOUT | - |
| - | - | - | 120 | D8 | 148 | 170 | F8 | VSS | S | - | - | - | - |
| - | - | C5 | 121 | C8 | 149 | 171 | E9 | VDD | S | - | - | - | - |
| 87 | C6 | F4 | 122 | B11 | 150 | 172 | B11 | PD6 | I/O | FT | - | SPI3_MOSI/I2S3_SD, SAI1_SD_A, USART2_RX, FMC_NWAIT, DCMI_D10, LCD_B2, EVENTOUT | - |
| 88 | D6 | A5 | 123 | A11 | 151 | 173 | A11 | PD7 | I/O | FT | - | USART2_CK, SPDIFRX_IN0, FMC_NE1, EVENTOUT | - |
| - | - | - | - | - | - | 174 | B10 | PJ12 | I/O | FT | - | LCD_B0, EVENTOUT | - |
| - | - | - | - | - | - | 175 | B9 | PJ13 | I/O | FT | - | LCD_B1, EVENTOUT | - |
| - | - | - | - | - | - | 176 | C9 | PJ14 | I/O | FT | - | LCD_B2, EVENTOUT | - |
| - | - | - | - | - | - | 177 | D10 | PJ15 | I/O | FT | - | LCD_B3, EVENTOUT | - |

**Table 10. STM32F745xx and STM32F746xx pin and ball definition (continued)**

| Pin Number | | | | | | | | Pin name (function after reset)(1) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LQFP100 | TFBGA100 | WLCSP143 | LQFP144 | UFBGA176 | LQFP176 | LQFP208 | TFBGA216 | | | | | | |
| - | - | E5 | 124 | C10 | 152 | 178 | D9 | PG9 | I/O | FT | - | SPDIFRX_IN3, USART6_RX, QUADSPI_BK2_IO2, SAI2_FS_B, FMC_NE2/FMC_NCE, DCMI_VSYNC, EVENTOUT | - |
| - | - | C6 | 125 | B10 | 153 | 179 | C8 | PG10 | I/O | FT | - | LCD_G3, SAI2_SD_B, FMC_NE3, DCMI_D2, LCD_B2, EVENTOUT | - |
| - | -- | B6 | 126 | B9 | 154 | 180 | B8 | PG11 | I/O | FT | - | SPDIFRX_IN0, ETH_MII_TX_EN/ETH_RMII_TX_EN, DCMI_D3, LCD_B3, EVENTOUT | - |
| - | - | A6 | 127 | B8 | 155 | 181 | C7 | PG12 | I/O | FT | - | LPTIM1_IN1, SPI6_MISO, SPDIFRX_IN1, USART6_RTS, LCD_B4, FMC_NE4, LCD_B1, EVENTOUT | - |
| - | - | D6 | 128 | A8 | 156 | 182 | B3 | PG13 | I/O | FT | - | TRACED0, LPTIM1_OUT, SPI6_SCK, USART6_CTS, ETH_MII_TXD0/ETH_RMII_TXD0, FMC_A24, LCD_R0, EVENTOUT | - |
| - | - | F6 | 129 | A7 | 157 | 183 | A4 | PG14 | I/O | FT | - | TRACED1, LPTIM1_ETR, SPI6_MOSI, USART6_TX, QUADSPI_BK2_IO3, ETH_MII_TXD1/ETH_RMII_TXD1, FMC_A25, LCD_B0, EVENTOUT | - |
| - | - | - | 130 | D7 | 158 | 184 | F7 | VSS | S | - | - | - | - |
| - | - | E6 | 131 | C7 | 159 | 185 | E8 | VDD | S | - | - | - | - |

**Table 10. STM32F745xx and STM32F746xx pin and ball definition (continued)**

| Pin Number | | | | | | | | Pin name (function after reset)(1) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LQFP100 | TFBGA100 | WLCSP143 | LQFP144 | UFBGA176 | LQFP176 | LQFP208 | TFBGA216 | | | | | | |
| - | - | - | - | - | - | 186 | D8 | PK3 | I/O | FT | - | LCD_B4, EVENTOUT | - |
| - | - | - | - | - | - | 187 | D7 | PK4 | I/O | FT | - | LCD_B5, EVENTOUT | - |
| - | - | - | - | - | - | 188 | C6 | PK5 | I/O | FT | - | LCD_B6, EVENTOUT | - |
| - | - | - | - | - | - | 189 | C5 | PK6 | I/O | FT | - | LCD_B7, EVENTOUT | - |
| - | - | - | - | - | - | 190 | C4 | PK7 | I/O | FT | - | LCD_DE, EVENTOUT | - |
| - | - | A7 | 132 | B7 | 160 | 191 | B7 | PG15 | I/O | FT | - | USART6_CTS, FMC_SDNCAS, DCMI_D13, EVENTOUT | - |
| 89 | A7 | B7 | 133 | A10 | 161 | 192 | A10 | PB3(JTDO/TRACESWO) | I/O | FT | - | JTDO/TRACESWO, TIM2_CH2, SPI1_SCK/I2S1_CK, SPI3_SCK/I2S3_CK, EVENTOUT | - |
| 90 | A6 | C7 | 134 | A9 | 162 | 193 | A9 | PB4(NJTRST) | I/O | FT | - | NJTRST, TIM3_CH1, SPI1_MISO, SPI3_MISO, SPI2_NSS/I2S2_WS, EVENTOUT | - |
| 91 | C5 | C8 | 135 | A6 | 163 | 194 | A8 | PB5 | I/O | FT | - | TIM3_CH2, I2C1_SMBA, SPI1_MOSI/I2S1_SD, SPI3_MOSI/I2S3_SD, CAN2_RX, OTG_HS_ULPI_D7, ETH_PPS_OUT, FMC_SDCKE1, DCMI_D10, EVENTOUT | - |
| 92 | B5 | A8 | 136 | B6 | 164 | 195 | B6 | PB6 | I/O | FT | - | TIM4_CH1, HDMI-CEC, I2C1_SCL, USART1_TX, CAN2_TX, QUADSPI_BK1_NCS, FMC_SDNE1, DCMI_D5, EVENTOUT | - |
| 93 | A5 | B8 | 137 | B5 | 165 | 196 | B5 | PB7 | I/O | FT | - | TIM4_CH2, I2C1_SDA, USART1_RX, FMC_NL, DCMI_VSYNC, EVENTOUT | - |
| 94 | D5 | C9 | 138 | D6 | 166 | 197 | E6 | BOOT | I | B | - | - | VPP |

**Table 10. STM32F745xx and STM32F746xx pin and ball definition (continued)**

| Pin Number | | | | | | | | Pin name (function after reset)(1) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LQFP100 | TFBGA100 | WLCSP143 | LQFP144 | UFBGA176 | LQFP176 | LQFP208 | TFBGA216 | | | | | | |
| 95 | B4 | A9 | 139 | A5 | 167 | 198 | A7 | PB8 | I/O | FT | - | TIM4_CH3, TIM10_CH1, I2C1_SCL, CAN1_RX, ETH_MII_TXD3, SDMMC1_D4, DCMI_D6, LCD_B6, EVENTOUT | - |
| 96 | A4 | B9 | 140 | B4 | 168 | 199 | B4 | PB9 | I/O | FT | - | TIM4_CH4, TIM11_CH1, I2C1_SDA, SPI2_NSS/I2S2_WS, CAN1_TX, SDMMC1_D5, DCMI_D7, LCD_B7, EVENTOUT | - |
| 97 | D4 | B10 | 141 | A4 | 169 | 200 | A6 | PE0 | I/O | FT | - | TIM4_ETR, LPTIM1_ETR, UART8_Rx, SAI2_MCK_A, FMC_NBL0, DCMI_D2, EVENTOUT | - |
| 98 | C4 | A10 | 142 | A3 | 170 | 201 | A5 | PE1 | I/O | FT | - | LPTIM1_IN2, UART8_Tx, FMC_NBL1, DCMI_D3, EVENTOUT | - |
| 99 | E4 | - | - | D5 | - | 202 | F6 | VSS | S | - | - | - | - |
| - | F7 | A11 | 143 | C6 | 171 | 203 | E5 | PDR_ON | S | - | - | - | - |
| 100 | F4 | D7 | 144 | C5 | 172 | 204 | E7 | VDD | S | - | - | - | - |
| - | - | - | - | D4 | 173 | 205 | C3 | PI4 | I/O | FT | - | TIM8_BKIN, SAI2_MCK_A, FMC_NBL2, DCMI_D5, LCD_B4, EVENTOUT | - |
| - | - | - | - | C4 | 174 | 206 | D3 | PI5 | I/O | FT | - | TIM8_CH1, SAI2_SCK_A, FMC_NBL3, DCMI_VSYNC, LCD_B5, EVENTOUT | - |

Table 10. STM32F745xx and STM32F746xx pin and ball definition (continued)

| Pin Number | | | | | | | | Pin name (function after reset)[1] | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LQFP100 | TFBGA100 | WLCSP143 | LQFP144 | UFBGA176 | LQFP176 | LQFP208 | TFBGA216 | | | | | | |
| - | - | - | - | C3 | 175 | 207 | D6 | PI6 | I/O | FT | - | TIM8_CH2, SAI2_SD_A, FMC_D28, DCMI_D6, LCD_B6, EVENTOUT | - |
| - | - | - | - | C2 | 176 | 208 | D4 | PI7 | I/O | FT | - | TIM8_CH3, SAI2_FS_A, FMC_D29, DCMI_D7, LCD_B7, EVENTOUT | - |

1. Function availability depends on the chosen device.
2. PC13, PC14, PC15 and PI8 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 and PI8 in output mode is limited:
   - The speed should not exceed 2 MHz with a maximum load of 30 pF.
   - These I/Os must not be used as a current source (e.g. to drive an LED).
3. Main function after the first backup domain power-up. Later on, it depends on the contents of the RTC registers even after reset (because these registers are not reset by the main reset). For details on how to manage these I/Os, refer to the RTC register description sections in the STM32F75xxx and STM32F74xxx reference manual.
4. FT = 5 V tolerant except when in analog mode or oscillator mode (for PC14, PC15, PH0 and PH1).
5. If the device is delivered in an WLCSP143, UFBGA176, LQFP176, TFBGA100 or TFBGA216 package, and the BYPASS_REG pin is set to VDD (Regulator OFF/internal reset ON mode), then PA0 is used as an internal Reset (active low).

*Note: For the UFBGA176 package, the balls "F6, F7, F8, F9, F10, G6, G7, G8, G9, G10, H6, H7, H8, H9, H10, J6, J7, J8, J9, J10, K6, K7, K8, K9, K10" are connected to VSS and their purpose is for heat dissipation and package mechanical stability.*

Table 11. FMC pin definition

| Pin name | NOR/PSRAM/SRAM | NOR/PSRAM Mux | NAND16 | SDRAM |
|---|---|---|---|---|
| PF0 | A0 | - | - | A0 |
| PF1 | A1 | - | - | A1 |
| PF2 | A2 | - | - | A2 |
| PF3 | A3 | - | - | A3 |
| PF4 | A4 | - | - | A4 |
| PF5 | A5 | - | - | A5 |
| PF12 | A6 | - | - | A6 |
| PF13 | A7 | - | - | A7 |
| PF14 | A8 | - | - | A8 |
| PF15 | A9 | - | - | A9 |
| PG0 | A10 | - | - | A10 |
| PG1 | A11 | - | - | A11 |
| PG2 | A12 | - | - | A12 |
| PG3 | A13 | - | - | - |
| PG4 | A14 | - | - | BA0 |
| PG5 | A15 | - | - | BA1 |
| PD11 | A16 | A16 | CLE | - |
| PD12 | A17 | A17 | ALE | - |
| PD13 | A18 | A18 | - | - |
| PE3 | A19 | A19 | - | - |
| PE4 | A20 | A20 | - | - |
| PE5 | A21 | A21 | - | - |
| PE6 | A22 | A22 | - | - |
| PE2 | A23 | A23 | - | - |
| PG13 | A24 | A24 | - | - |
| PG14 | A25 | A25 | - | - |
| PD14 | D0 | DA0 | D0 | D0 |
| PD15 | D1 | DA1 | D1 | D1 |
| PD0 | D2 | DA2 | D2 | D2 |
| PD1 | D3 | DA3 | D3 | D3 |
| PE7 | D4 | DA4 | D4 | D4 |
| PE8 | D5 | DA5 | D5 | D5 |
| PE9 | D6 | DA6 | D6 | D6 |
| PE10 | D7 | DA7 | D7 | D7 |

**Table 11. FMC pin definition (continued)**

| Pin name | NOR/PSRAM/SRAM | NOR/PSRAM Mux | NAND16 | SDRAM |
|---|---|---|---|---|
| PE11 | D8 | DA8 | D8 | D8 |
| PE12 | D9 | DA9 | D9 | D9 |
| PE13 | D10 | DA10 | D10 | D10 |
| PE14 | D11 | DA11 | D11 | D11 |
| PE15 | D12 | DA12 | D12 | D12 |
| PD8 | D13 | DA13 | D13 | D13 |
| PD9 | D14 | DA14 | D14 | D14 |
| PD10 | D15 | DA15 | D15 | D15 |
| PH8 | D16 | - | - | D16 |
| PH9 | D17 | - | - | D17 |
| PH10 | D18 | - | - | D18 |
| PH11 | D19 | - | - | D19 |
| PH12 | D20 | - | - | D20 |
| PH13 | D21 | - | - | D21 |
| PH14 | D22 | - | - | D22 |
| PH15 | D23 | - | - | D23 |
| PI0 | D24 | - | - | D24 |
| PI1 | D25 | - | - | D25 |
| PI2 | D26 | - | - | D26 |
| PI3 | D27 | - | - | D27 |
| PI6 | D28 | - | - | D28 |
| PI7 | D29 | - | - | D29 |
| PI9 | D30 | - | - | D30 |
| PI10 | D31 | - | - | D31 |
| PD7 | NE1 | NE1 | - | - |
| PG9 | NE2 | NE2 | NCE | - |
| PG10 | NE3 | NE3 | - | - |
| PG11 | - | - | - | - |
| PG12 | NE4 | NE4 | - | - |
| PD3 | CLK | CLK | - | - |
| PD4 | NOE | NOE | NOE | - |
| PD5 | NWE | NWE | NWE | - |
| PD6 | NWAIT | NWAIT | NWAIT | - |
| PB7 | NADV | NADV | - | - |

Table 11. FMC pin definition (continued)

| Pin name | NOR/PSRAM/SRAM | NOR/PSRAM Mux | NAND16 | SDRAM |
|---|---|---|---|---|
| PF6 | - | - | - | - |
| PF7 | - | - | - | - |
| PF8 | - | - | - | - |
| PF9 | - | - | - | - |
| PF10 | - | - | - | - |
| PG6 | - | - | - | - |
| PG7 | - | - | INT | - |
| PE0 | NBL0 | NBL0 | - | NBL0 |
| PE1 | NBL1 | NBL1 | - | NBL1 |
| PI4 | NBL2 | - | - | NBL2 |
| PI5 | NBL3 | - | - | NBL3 |
| PG8 | - | - | - | SDCLK |
| PC0 | - | - | - | SDNWE |
| PF11 | - | - | - | SDNRAS |
| PG15 | - | - | - | SDNCAS |
| PH2 | - | - | - | SDCKE0 |
| PH3 | - | - | - | SDNE0 |
| PH6 | - | - | - | SDNE1 |
| PH7 | - | - | - | SDCKE1 |
| PH5 | - | - | - | SDNWE |
| PC2 | - | - | - | SDNE0 |
| PC3 | - | - | - | SDCKE0 |
| PB5 | - | - | - | SDCKE1 |
| PB6 | - | - | - | SDNE1 |

**Table 12. STM32F745xx and STM32F746xx alternate function mapping**

| Port | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | SYS | TIM1/2 | TIM3/4/5 | TIM8/9/10/11/LPTIM1/CEC | I2C1/2/3/4/CEC | SPI1/2/3/4/5/6 | SPI3/SAI1 | SPI2/3/USART1/2/3/UART5/SPDIFRX | SAI2/USART6/UART4/5/7/8/SPDIFRX | CAN1/2/TIM12/13/14/QUADSPI/LCD | SAI2/QUADSPI/OTG2_HS/OTG1_FS | ETH/OTG1_FS | FMC/SDMMC1/OTG2_FS | DCMI | LCD | SYS |
| Port A | PA0 | - | TIM2_CH1/TIM2_ETR | TIM5_CH1 | TIM8_ETR | - | - | - | USART2_CTS | UART4_TX | - | SAI2_SD_B | ETH_MII_CRS | - | - | - | EVENTOUT |
| | PA1 | - | TIM2_CH2 | TIM5_CH2 | - | - | - | - | USART2_RTS | UART4_RX | QUADSPI_BK1_IO3 | SAI2_MCK_B | ETH_MII_RX_CLK/ETH_RMII_REF_CLK | - | - | LCD_R2 | EVENTOUT |
| | PA2 | - | TIM2_CH3 | TIM5_CH3 | TIM9_CH1 | - | - | - | USART2_TX | SAI2_SCK_B | - | - | ETH_MDIO | - | - | LCD_R1 | EVENTOUT |
| | PA3 | - | TIM2_CH4 | TIM5_CH4 | TIM9_CH2 | - | - | - | USART2_RX | - | - | OTG_HS_ULPI_D0 | ETH_MII_COL | - | - | LCD_B5 | EVENTOUT |
| | PA4 | - | - | - | - | - | SPI1_NSS/I2S1_WS | SPI3_NSS/I2S3_WS | USART2_CK | - | - | - | - | OTG_HS_SOF | DCMI_HSYNC | LCD_VSYNC | EVENTOUT |
| | PA5 | - | TIM2_CH1/TIM2_ETR | - | TIM8_CH1N | - | SPI1_SCK/I2S1_CK | - | - | - | - | OTG_HS_ULPI_CK | - | - | - | LCD_R4 | EVENTOUT |
| | PA6 | - | TIM1_BKIN | TIM3_CH1 | TIM8_BKIN | - | SPI1_MISO | - | - | - | TIM13_CH1 | - | - | - | DCMI_PIXCLK | LCD_G2 | EVENTOUT |
| | PA7 | - | TIM1_CH1N | TIM3_CH2 | TIM8_CH1N | - | SPI1_MOSI/I2S1_SD | - | - | - | TIM14_CH1 | - | ETH_MII_RX_DV/ETH_RMII_CRS_DV | FMC_SDNWE | - | - | EVENTOUT |
| | PA8 | MCO1 | TIM1_CH1 | - | TIM8_BKIN2 | I2C3_SCL | - | - | USART1_CK | - | - | OTG_FS_SOF | - | - | - | LCD_R6 | EVENTOUT |
| | PA9 | - | TIM1_CH2 | - | - | I2C3_SMBA | SPI2_SCK/I2S2_CK | - | USART1_TX | - | - | - | - | - | DCMI_D0 | - | EVENTOUT |
| | PA10 | - | TIM1_CH3 | - | - | - | - | - | USART1_RX | - | - | OTG_FS_ID | - | - | DCMI_D1 | - | EVENTOUT |
| | PA11 | - | TIM1_CH4 | - | - | - | - | - | USART1_CTS | - | CAN1_RX | OTG_FS_DM | - | - | - | LCD_R4 | EVENTOUT |

Table 12. STM32F745xx and STM32F746xx alternate function mapping (continued)

| Port | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | SYS | TIM1/2 | TIM3/4/5 | TIM8/9/10/11/LPTIM1/CEC | I2C1/2/3/4/CEC | SPI1/2/3/4/5/6 | SPI3/SAI1 | SPI2/3/USART1/2/3/UART5/SPDIFRX | SAI2/USART6/UART4/5/7/8/SPDIFRX | CAN1/2/TIM12/13/14/QUADSPI/LCD | SAI2/QUADSPI/OTG2_HS/OTG1_FS | ETH/OTG1_FS | FMC/SDMMC1/OTG2_FS | DCMI | LCD | SYS |
| Port A | PA12 | - | TIM1_ETR | - | - | - | - | - | USART1_RTS | SAI2_FS_B | CAN1_TX | OTG_FS_DP | - | - | - | LCD_R5 | EVENTOUT |
| | PA13 | JTMS-SWDIO | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOUT |
| | PA14 | JTCK-SWCLK | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOUT |
| | PA15 | JTDI | TIM2_CH1/TIM2_ETR | - | - | HDMI-CEC | SPI1_NSS/I2S1_WS | SPI3_NSS/I2S3_WS | - | UART4_RTS | - | - | - | - | - | - | EVENTOUT |
| Port B | PB0 | - | TIM1_CH2N | TIM3_CH3 | TIM8_CH2N | - | - | - | - | UART4_CTS | LCD_R3 | OTG_HS_ULPI_D1 | ETH_MII_RXD2 | - | - | - | EVENTOUT |
| | PB1 | - | TIM1_CH3N | TIM3_CH4 | TIM8_CH3N | - | - | - | - | - | LCD_R6 | OTG_HS_ULPI_D2 | ETH_MII_RXD3 | - | - | - | EVENTOUT |
| | PB2 | - | - | - | - | - | - | SAI1_SD_A | SPI3_MOSI/I2S3_SD | | QUADSPI_CLK | - | - | - | - | - | EVENTOUT |
| | PB3 | JTDO/TRACESWO | TIM2_CH2 | - | - | - | SPI1_SCK/I2S1_CK | SPI3_SCK/I2S3_CK | - | - | - | - | - | - | - | - | EVENTOUT |
| | PB4 | NJTRST | - | TIM3_CH1 | - | - | SPI1_MISO | SPI3_MISO | SPI2_NSS/I2S2_WS | - | - | - | - | - | - | - | EVENTOUT |
| | PB5 | - | - | TIM3_CH2 | - | I2C1_SMBA | SPI1_MOSI/I2S1_SD | SPI3_MOSI/I2S3_SD | - | - | CAN2_RX | OTG_HS_ULPI_D7 | ETH_PPS_OUT | FMC_SDCKE1 | DCMI_D10 | - | EVENTOUT |
| | PB6 | - | - | TIM4_CH1 | HDMI-CEC | I2C1_SCL | - | - | USART1_TX | - | CAN2_TX | QUADSPI_BK1_NCS | - | FMC_SDNE1 | DCMI_D5 | - | EVENTOUT |
| | PB7 | - | - | TIM4_CH2 | - | I2C1_SDA | - | - | USART1_RX | - | - | - | - | FMC_NL | DCMI_VSYNC | - | EVENTOUT |
| | PB8 | - | - | TIM4_CH3 | TIM10_CH1 | I2C1_SCL | - | - | - | - | CAN1_RX | | ETH_MII_TXD3 | SDMMC1_D4 | DCMI_D6 | LCD_B6 | EVENTOUT |

## Table 12. STM32F745xx and STM32F746xx alternate function mapping (continued)

| Port | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | SYS | TIM1/2 | TIM3/4/5 | TIM8/9/10/11/LPTIM1/CEC | I2C1/2/3/4/CEC | SPI1/2/3/4/5/6 | SPI3/SAI1 | SPI2/3/USART1/2/3/UART5/SPDIFRX | SAI2/USART6/UART4/5/7/8/SPDIFRX | CAN1/2/TIM12/13/14/QUADSPI/LCD | SAI2/QUADSPI/OTG2_HS/OTG1_FS | ETH/OTG1_FS | FMC/SDMMC1/OTG2_FS | DCMI | LCD | SYS |
| Port B | PB9 | - | - | TIM4_CH4 | TIM11_CH1 | I2C1_SDA | SPI2_NSS/I2S2_WS | - | - | - | CAN1_TX | - | - | SDMMC1_D5 | DCMI_D7 | LCD_B7 | EVENTOUT |
| | PB10 | - | TIM2_CH3 | - | - | I2C2_SCL | SPI2_SCK/I2S2_CK | - | USART3_TX | - | - | OTG_HS_ULPI_D3 | ETH_MII_RX_ER | - | - | LCD_G4 | EVENTOUT |
| | PB11 | - | TIM2_CH4 | - | - | I2C2_SDA | - | - | USART3_RX | - | - | OTG_HS_ULPI_D4 | ETH_MII_TX_EN/ETH_RMII_TX_EN | - | - | LCD_G5 | EVENTOUT |
| | PB12 | - | TIM1_BKIN | - | - | I2C2_SMBA | SPI2_NSS/I2S2_WS | - | USART3_CK | - | CAN2_RX | OTG_HS_ULPI_D5 | ETH_MII_TXD0/ETH_RMII_TXD0 | OTG_HS_ID | - | - | EVENTOUT |
| | PB13 | - | TIM1_CH1N | - | - | - | SPI2_SCK/I2S2_CK | - | USART3_CTS | - | CAN2_TX | OTG_HS_ULPI_D6 | ETH_MII_TXD1/ETH_RMII_TXD1 | - | - | - | EVENTOUT |
| | PB14 | - | TIM1_CH2N | - | TIM8_CH2N | - | SPI2_MISO | - | USART3_RTS | - | TIM12_CH1 | - | - | OTG_HS_DM | - | - | EVENTOUT |
| | PB15 | RTC_REFIN | TIM1_CH3N | - | TIM8_CH3N | - | SPI2_MOSI/I2S2_SD | - | - | - | TIM12_CH2 | - | - | OTG_HS_DP | - | - | EVENTOUT |
| Port C | PC0 | - | - | - | - | - | - | - | - | SAI2_FS_B | - | OTG_HS_ULPI_STP | - | FMC_SDNWE | - | LCD_R5 | EVENTOUT |
| | PC1 | TRACED0 | - | - | - | - | SPI2_MOSI/I2S2_SD | SAI1_SD_A | - | - | - | - | ETH_MDC | - | - | - | EVENTOUT |
| | PC2 | - | - | - | - | - | SPI2_MISO | - | - | - | - | OTG_HS_ULPI_DIR | ETH_MII_TXD2 | FMC_SDNE0 | - | - | EVENTOUT |
| | PC3 | - | - | - | - | - | SPI2_MOSI/I2S2_SD | - | - | - | - | OTG_HS_ULPI_NXT | ETH_MII_TX_CLK | FMC_SDCKE0 | - | - | EVENTOUT |

**Table 12. STM32F745xx and STM32F746xx alternate function mapping (continued)**

| Port | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | SYS | TIM1/2 | TIM3/4/5 | TIM8/9/10/11/LPTIM1/CEC | I2C1/2/3/4/CEC | SPI1/2/3/4/5/6 | SPI3/SAI1 | SPI2/3/USART1/2/3/UART5/SPDIFRX | SAI2/USART6/UART4/5/7/8/SPDIFRX | CAN1/2/TIM12/13/14/QUADSPI/LCD | SAI2/QUADSPI/OTG2_HS/OTG1_FS | ETH/OTG1_FS | FMC/SDMMC1/OTG2_FS | DCMI | LCD | SYS |
| Port C | PC4 | - | - | - | - | - | I2S1_MCK | - | - | SPDIFRX_IN2 | - | - | ETH_MII_RXD0/ETH_RMII_RXD0 | FMC_SDNE0 | - | - | EVENTOUT |
| Port C | PC5 | - | - | - | - | - | - | - | - | SPDIFRX_IN3 | - | - | ETH_MII_RXD1/ETH_RMII_RXD1 | FMC_SDCKE0 | - | - | EVENTOUT |
| Port C | PC6 | - | - | TIM3_CH1 | TIM8_CH1 | - | I2S2_MCK | - | - | USART6_TX | - | - | - | SDMMC1_D6 | DCMI_D0 | LCD_HSYNC | EVENTOUT |
| Port C | PC7 | - | - | TIM3_CH2 | TIM8_CH2 | - | - | I2S3_MCK | - | USART6_RX | - | - | - | SDMMC1_D7 | DCMI_D1 | LCD_G6 | EVENTOUT |
| Port C | PC8 | TRACED1 | - | TIM3_CH3 | TIM8_CH3 | - | - | - | UART5_RTS | USART6_CK | - | - | - | SDMMC1_D0 | DCMI_D2 | - | EVENTOUT |
| Port C | PC9 | MCO2 | - | TIM3_CH4 | TIM8_CH4 | I2C3_SDA | I2S_CKIN | - | UART5_CTS | - | QUADSPI_BK1_IO0 | - | - | SDMMC1_D1 | DCMI_D3 | - | EVENTOUT |
| Port C | PC10 | - | - | - | - | - | - | SPI3_SCK/I2S3_CK | USART3_TX | UART4_TX | QUADSPI_BK1_IO1 | - | - | SDMMC1_D2 | DCMI_D8 | LCD_R2 | EVENTOUT |
| Port C | PC11 | - | - | - | - | - | - | SPI3_MISO | USART3_RX | UART4_RX | QUADSPI_BK2_NCS | - | - | SDMMC1_D3 | DCMI_D4 | - | EVENTOUT |
| Port C | PC12 | TRACED3 | - | - | - | - | - | SPI3_MOSI/I2S3_SD | USART3_CK | UART5_TX | - | - | - | SDMMC1_CK | DCMI_D9 | - | EVENTOUT |
| Port C | PC13 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOUT |
| Port C | PC14 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOUT |
| Port C | PC15 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOUT |

**Table 12. STM32F745xx and STM32F746xx alternate function mapping (continued)**

| Port | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | SYS | TIM1/2 | TIM3/4/5 | TIM8/9/10/11/LPTIM1/CEC | I2C1/2/3/4/CEC | SPI1/2/3/4/5/6 | SPI3/SAI1 | SPI2/3/USART1/2/3/UART5/SPDIFRX | SAI2/USART6/UART4/5/7/8/SPDIFRX | CAN1/2/TIM12/13/14/QUADSPI/LCD | SAI2/QUADSPI/OTG2_HS/OTG1_FS | ETH/OTG1_FS | FMC/SDMMC1/OTG2_FS | DCMI | LCD | SYS |
| Port D | PD0 | - | - | - | - | - | - | - | - | - | CAN1_RX | - | - | FMC_D2 | - | - | EVENTOUT |
| | PD1 | - | - | - | - | - | - | - | - | - | CAN1_TX | - | - | FMC_D3 | - | - | EVENTOUT |
| | PD2 | TRACED2 | - | TIM3_ETR | - | - | - | - | - | UART5_RX | - | - | - | SDMMC1_CMD | DCMI_D11 | - | EVENTOUT |
| | PD3 | - | - | - | - | - | SPI2_SCK/I2S2_CK | - | USART2_CTS | - | - | - | - | FMC_CLK | DCMI_D5 | LCD_G7 | EVENTOUT |
| | PD4 | - | - | - | - | - | - | - | USART2_RTS | - | - | - | - | FMC_NOE | - | - | EVENTOUT |
| | PD5 | - | - | - | - | - | - | - | USART2_TX | - | - | - | - | FMC_NWE | - | - | EVENTOUT |
| | PD6 | - | - | - | - | - | SPI3_MOSI/I2S3_SD | SAI1_SD_A | USART2_RX | - | - | - | - | FMC_NWAIT | DCMI_D10 | LCD_B2 | EVENTOUT |
| | PD7 | - | - | - | - | - | - | - | USART2_CK | SPDIFRX_IN0 | - | - | - | FMC_NE1 | - | - | EVENTOUT |
| | PD8 | - | - | - | - | - | - | - | USART3_TX | SPDIFRX_IN1 | - | - | - | FMC_D13 | - | - | EVENTOUT |
| | PD9 | - | - | - | - | - | - | - | USART3_RX | - | - | - | - | FMC_D14 | - | - | EVENTOUT |
| | PD10 | - | - | - | - | - | - | - | USART3_CK | - | - | - | - | FMC_D15 | - | LCD_B3 | EVENTOUT |
| | PD11 | - | - | - | - | I2C4_SMBA | - | - | USART3_CTS | - | QUADSPI_BK1_IO0 | SAI2_SD_A | - | FMC_A16/FMC_CLE | - | - | EVENTOUT |
| | PD12 | - | - | TIM4_CH1 | LPTIM1_IN1 | I2C4_SCL | - | - | USART3_RTS | - | QUADSPI_BK1_IO1 | SAI2_FS_A | - | FMC_A17/FMC_ALE | - | - | EVENTOUT |
| | PD13 | - | - | TIM4_CH2 | LPTIM1_OUT | I2C4_SDA | - | - | - | - | QUADSPI_BK1_IO3 | SAI2_SCK_A | - | FMC_A18 | - | - | EVENTOUT |

Table 12. STM32F745xx and STM32F746xx alternate function mapping (continued)

| Port | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | SYS | TIM1/2 | TIM3/4/5 | TIM8/9/10/11/LPTIM1/CEC | I2C1/2/3/4/CEC | SPI1/2/3/4/5/6 | SPI3/SAI1 | SPI2/3/USART1/2/3/UART5/SPDIFRX | SAI2/USART6/UART4/5/7/8/SPDIFRX | CAN1/2/TIM12/13/14/QUADSPI/LCD | SAI2/QUADSPI/OTG2_HS/OTG1_FS | ETH/OTG1_FS | FMC/SDMMC1/OTG2_FS | DCMI | LCD | SYS |
| Port D | PD14 | - | - | TIM4_CH3 | - | - | - | - | - | UART8_CTS | - | - | - | FMC_D0 | - | - | EVENTOUT |
| | PD15 | - | - | TIM4_CH4 | - | - | - | - | - | UART8_RTS | - | - | - | FMC_D1 | - | - | EVENTOUT |
| Port E | PE0 | - | - | TIM4_ETR | LPTIM1_ETR | - | - | - | - | UART8_Rx | - | SAI2_MCK_A | - | FMC_NBL0 | DCMI_D2 | - | EVENTOUT |
| | PE1 | - | - | - | LPTIM1_IN2 | - | - | - | - | UART8_Tx | - | - | - | FMC_NBL1 | DCMI_D3 | - | EVENTOUT |
| | PE2 | TRACECLK | - | - | - | - | SPI4_SCK | SAI1_MCLK_A | - | - | QUADSPI_BK1_IO2 | - | ETH_MII_TXD3 | FMC_A23 | - | - | EVENTOUT |
| | PE3 | TRACED0 | - | - | - | - | - | SAI1_SD_B | - | - | - | - | - | FMC_A19 | - | - | EVENTOUT |
| | PE4 | TRACED1 | - | - | - | - | SPI4_NSS | SAI1_FS_A | - | - | - | - | - | FMC_A20 | DCMI_D4 | LCD_B0 | EVENTOUT |
| | PE5 | TRACED2 | - | - | TIM9_CH1 | - | SPI4_MISO | SAI1_SCK_A | - | - | - | - | - | FMC_A21 | DCMI_D6 | LCD_G0 | EVENTOUT |
| | PE6 | TRACED3 | TIM1_BKIN2 | - | TIM9_CH2 | - | SPI4_MOSI | SAI1_SD_A | - | - | - | SAI2_MCK_B | - | FMC_A22 | DCMI_D7 | LCD_G1 | EVENTOUT |
| | PE7 | - | TIM1_ETR | - | - | - | - | - | - | UART7_Rx | - | QUADSPI_BK2_IO0 | - | FMC_D4 | - | - | EVENTOUT |
| | PE8 | - | TIM1_CH1N | - | - | - | - | - | - | UART7_Tx | - | QUADSPI_BK2_IO1 | - | FMC_D5 | - | - | EVENTOUT |
| | PE9 | - | TIM1_CH1 | - | - | - | - | - | - | UART7_RTS | - | QUADSPI_BK2_IO2 | - | FMC_D6 | - | - | EVENTOUT |
| | PE10 | - | TIM1_CH2N | - | - | - | - | - | - | UART7_CTS | - | QUADSPI_BK2_IO3 | - | FMC_D7 | - | - | EVENTOUT |
| | PE11 | - | TIM1_CH2 | - | - | - | SPI4_NSS | - | - | - | - | SAI2_SD_B | - | FMC_D8 | - | LCD_G3 | EVENTOUT |
| | PE12 | - | TIM1_CH3N | - | - | - | SPI4_SCK | - | - | - | - | SAI2_SCK_B | - | FMC_D9 | - | LCD_B4 | EVENTOUT |
| | PE13 | - | TIM1_CH3 | - | - | - | SPI4_MISO | - | - | - | - | SAI2_FS_B | - | FMC_D10 | - | LCD_DE | EVENTOUT |

**Table 12. STM32F745xx and STM32F746xx alternate function mapping (continued)**

| Port | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | SYS | TIM1/2 | TIM3/4/5 | TIM8/9/10/11/LPTIM1/CEC | I2C1/2/3/4/CEC | SPI1/2/3/4/5/6 | SPI3/SAI1 | SPI2/3/USART1/2/3/UART5/SPDIFRX | SAI2/USART6/UART4/5/7/8/SPDIFRX | CAN1/2/TIM12/13/14/QUADSPI/LCD | SAI2/QUADSPI/OTG2_HS/OTG1_FS | ETH/OTG1_FS | FMC/SDMMC1/OTG2_FS | DCMI | LCD | SYS |
| Port E | PE14 | - | TIM1_CH4 | - | - | - | SPI4_MOSI | - | - | - | - | SAI2_MCK_B | - | FMC_D11 | - | LCD_CLK | EVENTOUT |
| | PE15 | - | TIM1_BKIN | - | - | - | - | - | - | - | - | - | - | FMC_D12 | - | LCD_R7 | EVENTOUT |
| Port F | PF0 | - | - | - | - | I2C2_SDA | - | - | - | - | - | - | - | FMC_A0 | - | - | EVENTOUT |
| | PF1 | - | - | - | - | I2C2_SCL | - | - | - | - | - | - | - | FMC_A1 | - | - | EVENTOUT |
| | PF2 | - | - | - | - | I2C2_SMBA | - | - | - | - | - | - | - | FMC_A2 | - | - | EVENTOUT |
| | PF3 | - | - | - | - | - | - | - | - | - | - | - | - | FMC_A3 | - | - | EVENTOUT |
| | PF4 | - | - | - | - | - | - | - | - | - | - | - | - | FMC_A4 | - | - | EVENTOUT |
| | PF5 | - | - | - | - | - | - | - | - | - | - | - | - | FMC_A5 | - | - | EVENTOUT |
| | PF6 | - | - | - | TIM10_CH1 | - | SPI5_NSS | SAI1_SD_B | - | UART7_Rx | QUADSPI_BK1_IO3 | - | - | - | - | - | EVENTOUT |
| | PF7 | - | - | - | TIM11_CH1 | - | SPI5_SCK | SAI1_MCLK_B | - | UART7_Tx | QUADSPI_BK1_IO2 | - | - | - | - | - | EVENTOUT |
| | PF8 | - | - | - | - | - | SPI5_MISO | SAI1_SCK_B | - | UART7_RTS | TIM13_CH1 | QUADSPI_BK1_IO0 | - | - | - | - | EVENTOUT |
| | PF9 | - | - | - | - | - | SPI5_MOSI | SAI1_FS_B | - | UART7_CTS | TIM14_CH1 | QUADSPI_BK1_IO1 | - | - | - | - | EVENTOUT |
| | PF10 | - | - | - | - | - | - | - | - | - | - | - | - | - | DCMI_D11 | LCD_DE | EVENTOUT |
| | PF11 | - | - | - | - | - | SPI5_MOSI | - | - | - | - | SAI2_SD_B | - | FMC_SDNRAS | DCMI_D12 | - | EVENTOUT |
| | PF12 | - | - | - | - | - | - | - | - | - | - | - | - | FMC_A6 | - | - | EVENTOUT |

**Table 12. STM32F745xx and STM32F746xx alternate function mapping (continued)**

| Port | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | SYS | TIM1/2 | TIM3/4/5 | TIM8/9/10/11/LPTIM1/CEC | I2C1/2/3/4/CEC | SPI1/2/3/4/5/6 | SPI3/SAI1 | SPI2/3/USART1/2/3/UART5/SPDIFRX | SAI2/USART6/UART4/5/7/8/SPDIFRX | CAN1/2/TIM12/13/14/QUADSPI/LCD | SAI2/QUADSPI/OTG2_HS/OTG1_FS | ETH/OTG1_FS | FMC/SDMMC1/OTG2_FS | DCMI | LCD | SYS |
| Port F | PF13 | - | - | - | - | I2C4_SMBA | - | - | - | - | - | - | - | FMC_A7 | - | - | EVENTOUT |
| | PF14 | - | - | - | - | I2C4_SCL | - | - | - | - | - | - | - | FMC_A8 | - | - | EVENTOUT |
| | PF15 | - | - | - | - | I2C4_SDA | - | - | - | - | - | - | - | FMC_A9 | - | - | EVENTOUT |
| Port G | PG0 | - | - | - | - | - | - | - | - | - | - | - | - | FMC_A10 | - | - | EVENTOUT |
| | PG1 | - | - | - | - | - | - | - | - | - | - | - | - | FMC_A11 | - | - | EVENTOUT |
| | PG2 | - | - | - | - | - | - | - | - | - | - | - | - | FMC_A12 | - | - | EVENTOUT |
| | PG3 | - | - | - | - | - | - | - | - | - | - | - | - | FMC_A13 | - | - | EVENTOUT |
| | PG4 | - | - | - | - | - | - | - | - | - | - | - | - | FMC_A14/FMC_BA0 | - | - | EVENTOUT |
| | PG5 | - | - | - | - | - | - | - | - | - | - | - | - | FMC_A15/FMC_BA1 | - | - | EVENTOUT |
| | PG6 | - | - | - | - | - | - | - | - | - | - | - | - | - | DCMI_D12 | LCD_R7 | EVENTOUT |
| | PG7 | - | - | - | - | - | - | - | - | USART6_CK | - | - | - | FMC_INT | DCMI_D13 | LCD_CLK | EVENTOUT |
| | PG8 | - | - | - | - | - | SPI6_NSS | - | SPDIFRX_IN2 | USART6_RTS | - | - | ETH_PPS_OUT | FMC_SDCLK | - | - | EVENTOUT |
| | PG9 | - | - | - | - | - | - | - | SPDIFRX_IN3 | USART6_RX | QUADSPI_BK2_IO2 | SAI2_FS_B | - | FMC_NE2/FMC_NCE | DCMI_VSYNC | - | EVENTOUT |
| | PG10 | - | - | - | - | - | - | - | - | - | LCD_G3 | SAI2_SD_B | - | FMC_NE3 | DCMI_D2 | LCD_B2 | EVENTOUT |

**Table 12. STM32F745xx and STM32F746xx alternate function mapping (continued)**

| Port | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | SYS | TIM1/2 | TIM3/4/5 | TIM8/9/10/11/LPTIM1/CEC | I2C1/2/3/4/CEC | SPI1/2/3/4/5/6 | SPI3/SAI1 | SPI2/3/USART1/2/3/UART5/SPDIFRX | SAI2/USART6/UART4/5/7/8/SPDIFRX | CAN1/2/TIM12/13/14/QUADSPI/LCD | SAI2/QUADSPI/OTG2_HS/OTG1_FS | ETH/OTG1_FS | FMC/SDMMC1/OTG2_FS | DCMI | LCD | SYS |
| Port G | PG11 | - | - | - | - | - | - | - | SPDIFRX_IN0 | - | - | - | ETH_MII_TX_EN/ETH_RMII_TX_EN | - | DCMI_D3 | LCD_B3 | EVENTOUT |
| | PG12 | - | - | - | LPTIM1_IN1 | - | SPI6_MISO | - | SPDIFRX_IN1 | USART6_RTS | LCD_B4 | - | - | FMC_NE4 | - | LCD_B1 | EVENTOUT |
| | PG13 | TRACED0 | - | - | LPTIM1_OUT | - | SPI6_SCK | - | - | USART6_CTS | - | - | ETH_MII_TXD0/ETH_RMII_TXD0 | FMC_A24 | - | LCD_R0 | EVENTOUT |
| | PG14 | TRACED1 | - | - | LPTIM1_ETR | - | SPI6_MOSI | - | - | USART6_TX | QUADSPI_BK2_IO3 | - | ETH_MII_TXD1/ETH_RMII_TXD1 | FMC_A25 | - | LCD_B0 | EVENTOUT |
| | PG15 | - | - | - | - | - | - | - | - | USART6_CTS | - | - | - | FMC_SDNCAS | DCMI_D13 | - | EVENTOUT |
| Port H | PH0 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOUT |
| | PH1 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOUT |
| | PH2 | - | - | - | LPTIM1_IN2 | - | - | - | - | - | QUADSPI_BK2_IO0 | SAI2_SCK_B | ETH_MII_CRS | FMC_SDCKE0 | - | LCD_R0 | EVENTOUT |
| | PH3 | - | - | - | - | - | - | - | - | - | QUADSPI_BK2_IO1 | SAI2_MCK_B | ETH_MII_COL | FMC_SDNE0 | - | LCD_R1 | EVENTOUT |
| | PH4 | - | - | - | - | I2C2_SCL | - | - | - | - | - | OTG_HS_ULPI_NXT | - | - | - | - | EVENTOUT |
| | PH5 | - | - | - | - | I2C2_SDA | SPI5_NSS | - | - | - | - | - | - | FMC_SDNWE | - | - | EVENTOUT |
| | PH6 | - | - | - | - | I2C2_SMBA | SPI5_SCK | - | - | - | TIM12_CH1 | - | ETH_MII_RXD2 | FMC_SDNE1 | DCMI_D8 | - | EVENTOUT |
| | PH7 | - | - | - | - | I2C3_SCL | SPI5_MISO | - | - | - | - | - | ETH_MII_RXD3 | FMC_SDCKE1 | DCMI_D9 | - | EVENTOUT |

**Table 12. STM32F745xx and STM32F746xx alternate function mapping (continued)**

| Port | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | SYS | TIM1/2 | TIM3/4/5 | TIM8/9/10/11/LPTIM1/CEC | I2C1/2/3/4/CEC | SPI1/2/3/4/5/6 | SPI3/SAI1 | SPI2/3/USART1/2/3/UART5/SPDIFRX | SAI2/USART6/UART4/5/7/8/SPDIFRX | CAN1/2/TIM12/13/14/QUADSPI/LCD | SAI2/QUADSPI/OTG2_HS/OTG1_FS | ETH/OTG1_FS | FMC/SDMMC1/OTG2_FS | DCMI | LCD | SYS |
| Port H | PH8 | - | - | - | - | I2C3_SDA | - | - | - | - | - | - | - | FMC_D16 | DCMI_HSYNC | LCD_R2 | EVENTOUT |
| | PH9 | - | - | - | - | I2C3_SMBA | - | - | - | - | TIM12_CH2 | - | - | FMC_D17 | DCMI_D0 | LCD_R3 | EVENTOUT |
| | PH10 | - | - | TIM5_CH1 | - | I2C4_SMBA | - | - | - | - | - | - | - | FMC_D18 | DCMI_D1 | LCD_R4 | EVENTOUT |
| | PH11 | - | - | TIM5_CH2 | - | I2C4_SCL | - | - | - | - | - | - | - | FMC_D19 | DCMI_D2 | LCD_R5 | EVENTOUT |
| | PH12 | - | - | TIM5_CH3 | - | I2C4_SDA | - | - | - | - | - | - | - | FMC_D20 | DCMI_D3 | LCD_R6 | EVENTOUT |
| | PH13 | - | - | - | TIM8_CH1N | - | - | - | - | - | CAN1_TX | - | - | FMC_D21 | - | LCD_G2 | EVENTOUT |
| | PH14 | - | - | - | TIM8_CH2N | - | - | - | - | - | - | - | - | FMC_D22 | DCMI_D4 | LCD_G3 | EVENTOUT |
| | PH15 | - | - | - | TIM8_CH3N | - | - | - | - | - | - | - | - | FMC_D23 | DCMI_D11 | LCD_G4 | EVENTOUT |
| Port I | PI0 | - | - | TIM5_CH4 | - | - | SPI2_NSS/I2S2_WS | - | - | - | - | - | - | FMC_D24 | DCMI_D13 | LCD_G5 | EVENTOUT |
| | PI1 | - | - | - | TIM8_BKIN2 | - | SPI2_SCK/I2S2_CK | - | - | - | - | - | - | FMC_D25 | DCMI_D8 | LCD_G6 | EVENTOUT |
| | PI2 | - | - | - | TIM8_CH4 | - | SPI2_MISO | - | - | - | - | - | - | FMC_D26 | DCMI_D9 | LCD_G7 | EVENTOUT |
| | PI3 | - | - | - | TIM8_ETR | - | SPI2_MOSI/I2S2_SD | - | - | - | - | - | - | FMC_D27 | DCMI_D10 | - | EVENTOUT |
| | PI4 | - | - | - | TIM8_BKIN | - | - | - | - | - | - | SAI2_MCK_A | - | FMC_NBL2 | DCMI_D5 | LCD_B4 | EVENTOUT |
| | PI5 | - | - | - | TIM8_CH1 | - | - | - | - | - | - | SAI2_SCK_A | - | FMC_NBL3 | DCMI_VSYNC | LCD_B5 | EVENTOUT |
| | PI6 | - | - | - | TIM8_CH2 | - | - | - | - | - | - | SAI2_SD_A | - | FMC_D28 | DCMI_D6 | LCD_B6 | EVENTOUT |

## Table 12. STM32F745xx and STM32F746xx alternate function mapping (continued)

| Port | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | SYS | TIM1/2 | TIM3/4/5 | TIM8/9/10/11/LPTIM1/CEC | I2C1/2/3/4/CEC | SPI1/2/3/4/5/6 | SPI3/SAI1 | SPI2/3/USART1/2/3/UART5/SPDIFRX | SAI2/USART6/UART4/5/7/8/SPDIFRX | CAN1/2/TIM12/13/14/QUADSPI/LCD | SAI2/QUADSPI/OTG2_HS/OTG1_FS | ETH/OTG1_FS | FMC/SDMMC1/OTG2_FS | DCMI | LCD | SYS |
| Port I | PI7 | - | - | - | TIM8_CH3 | - | - | - | - | - | - | SAI2_FS_A | - | FMC_D29 | DCMI_D7 | LCD_B7 | EVENTOUT |
| | PI8 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOUT |
| | PI9 | - | - | - | - | - | - | - | - | - | CAN1_RX | - | - | FMC_D30 | - | LCD_VSYNC | EVENTOUT |
| | PI10 | - | - | - | - | - | - | - | - | - | - | - | ETH_MII_RX_ER | FMC_D31 | - | LCD_HSYNC | EVENTOUT |
| | PI11 | - | - | - | - | - | - | - | - | - | - | OTG_HS_ULPI_DIR | - | - | - | - | EVENTOUT |
| | PI12 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_HSYNC | EVENTOUT |
| | PI13 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_VSYNC | EVENTOUT |
| | PI14 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_CLK | EVENTOUT |
| | PI15 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_R0 | EVENTOUT |
| Port J | PJ0 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_R1 | EVENTOUT |
| | PJ1 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_R2 | EVENTOUT |
| | PJ2 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_R3 | EVENTOUT |
| | PJ3 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_R4 | EVENTOUT |
| | PJ4 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_R5 | EVENTOUT |
| | PJ5 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_R6 | EVENTOUT |
| | PJ6 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_R7 | EVENTOUT |

Table 12. STM32F745xx and STM32F746xx alternate function mapping (continued)

| Port | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | SYS | TIM1/2 | TIM3/4/5 | TIM8/9/10/11/LPTIM1/CEC | I2C1/2/3/4/CEC | SPI1/2/3/4/5/6 | SPI3/SAI1 | SPI2/3/USART1/2/3/UART5/SPDIFRX | SAI2/USART6/UART4/5/7/8/SPDIFRX | CAN1/2/TIM12/13/14/QUADSPI/LCD | SAI2/QUADSPI/OTG2_HS/OTG1_FS | ETH/OTG1_FS | FMC/SDMMC1/OTG2_FS | DCMI | LCD | SYS |
| Port J | PJ7 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_G0 | EVENTOUT |
| | PJ8 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_G1 | EVENTOUT |
| | PJ9 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_G2 | EVENTOUT |
| | PJ10 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_G3 | EVENTOUT |
| | PJ11 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_G4 | EVENTOUT |
| | PJ12 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_B0 | EVENTOUT |
| | PJ13 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_B1 | EVENTOUT |
| | PJ14 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_B2 | EVENTOUT |
| | PJ15 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_B3 | EVENTOUT |

Table 12. STM32F745xx and STM32F746xx alternate function mapping (continued)

| Port | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | SYS | TIM1/2 | TIM3/4/5 | TIM8/9/10/11/LPTIM1/CEC | I2C1/2/3/4/CEC | SPI1/2/3/4/5/6 | SPI3/SAI1 | SPI2/3/USART1/2/3/UART5/SPDIFRX | SAI2/USART6/UART4/5/7/8/SPDIFRX | CAN1/2/TIM12/13/14/QUADSPI/LCD | SAI2/QUADSPI/OTG2_HS/OTG1_FS | ETH/OTG1_FS | FMC/SDMMC1/OTG2_FS | DCMI | LCD | SYS |
| Port K | PK0 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_G5 | EVENTOUT |
| | PK1 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_G6 | EVENTOUT |
| | PK2 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_G7 | EVENTOUT |
| | PK3 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_B4 | EVENTOUT |
| | PK4 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_B5 | EVENTOUT |
| | PK5 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_B6 | EVENTOUT |
| | PK6 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_B7 | EVENTOUT |
| | PK7 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_DE | EVENTOUT |

# 5 Memory mapping

Refer to the product line reference manual for details on the memory mapping as well as the boundary addresses for all peripherals.

The memory map is shown in *Figure 19*.

**Figure 19. Memory map**

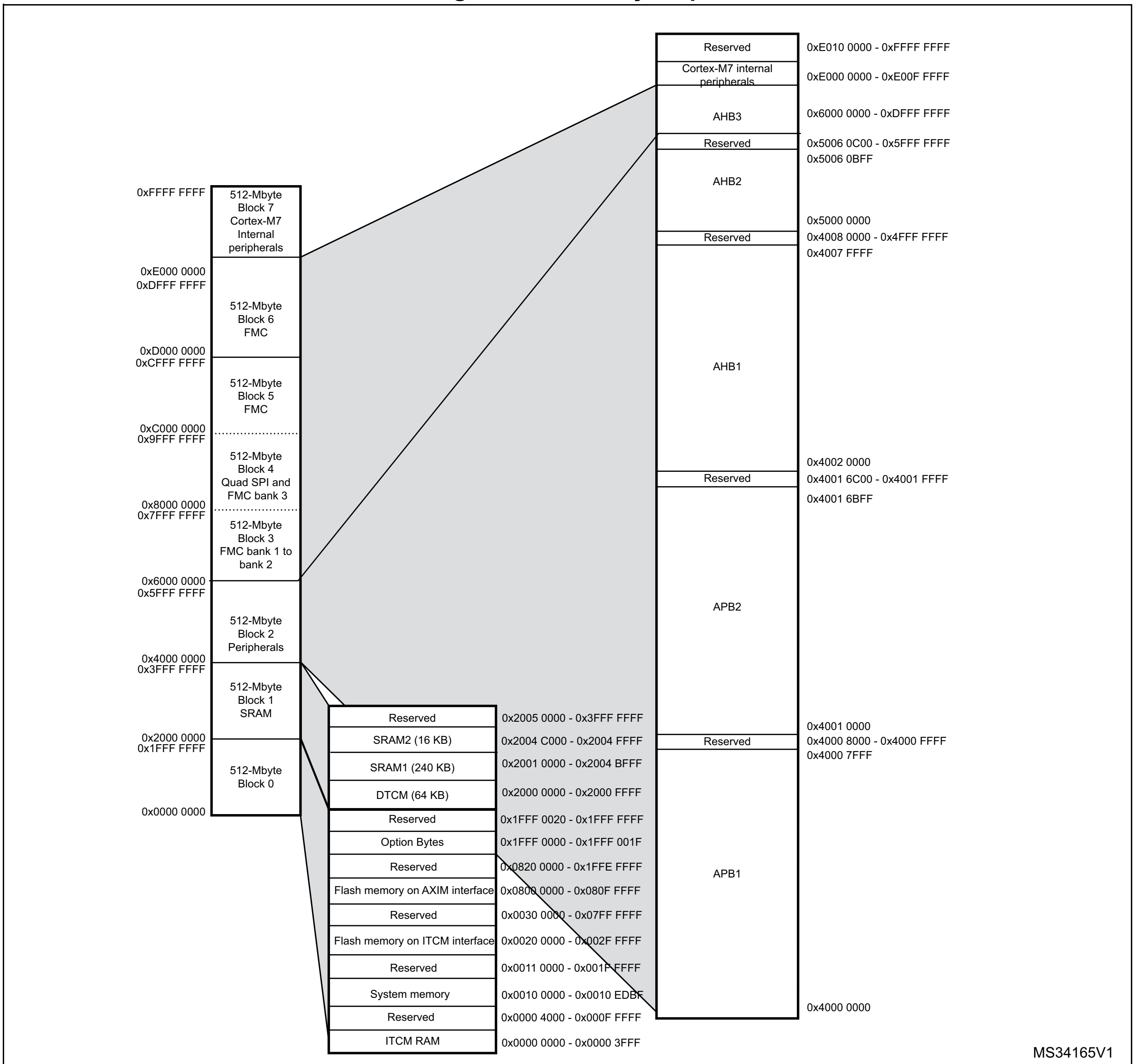


**Table 13. STM32F745xx and STM32F746xx register boundary addresses**

| Bus | Boundary address | Peripheral |
|---|---|---|
| | 0xE00F FFFF - 0xFFFF FFFF | Reserved |
| Cortex-M7 | 0xE000 0000 - 0xE00F FFFF | Cortex-M7 internal peripherals |
| AHB3 | 0xD000 0000 - 0xDFFF FFFF | FMC bank 6 |
| | 0xC000 0000 - 0xCFFF FFFF | FMC bank 5 |
| | 0xA000 1000 - 0xBFFF FFFF | Reserved |
| | 0xA000 0000- 0xA000 0FFF | FMC control register |
| | 0x9000 0000 - 0x9FFF FFFF | FMC bank 4 |
| | 0x8000 0000 - 0x8FFF FFFF | FMC bank 3 |
| | 0x7000 0000 - 0x7FFF FFFF | FMC bank 2 |
| | 0x6000 0000 - 0x6FFF FFFF | FMC bank 1 |
| | 0x5006 0C00- 0x5FFF FFFF | Reserved |
| AHB2 | 0x5006 0800 - 0X5006 0BFF | RNG |
| | 0x5005 0400 - X5006 07FF | Reserved |
| | 0x5005 0000 - 0X5005 03FF | DCMI |
| | 0x5004 0000- 0x5004 FFFF | Reserved |
| | 0x5000 0000 - 0X5003 FFFF | USB OTG FS |

**Table 13. STM32F745xx and STM32F746xx register boundary addresses (continued)**

| Bus | Boundary address | Peripheral |
|---|---|---|
| | 0x4008 0000- 0x4FFF FFFF | Reserved |
| AHB1 | 0x4004 0000 - 0x4007 FFFF | USB OTG HS |
| | 0x4002 BC00- 0x4003 FFFF | Reserved |
| | 0x4002 B000 - 0x4002 BBFF | DMA2D |
| | 0x4002 9400 - 0x4002 AFFF | Reserved |
| | 0x4002 9000 - 0x4002 93FF | ETHERNET MAC |
| | 0x4002 8C00 - 0x4002 8FFF | |
| | 0x4002 8800 - 0x4002 8BFF | |
| | 0x4002 8400 - 0x4002 87FF | |
| | 0x4002 8000 - 0x4002 83FF | |
| | 0x4002 6800 - 0x4002 7FFF | Reserved |
| | 0x4002 6400 - 0x4002 67FF | DMA2 |
| | 0x4002 6000 - 0x4002 63FF | DMA1 |
| | 0X4002 5000 - 0X4002 5FFF | Reserved |
| | 0x4002 4000 - 0x4002 4FFF | BKPSRAM |
| | 0x4002 3C00 - 0x4002 3FFF | Flash interface register |
| | 0x4002 3800 - 0x4002 3BFF | RCC |
| | 0X4002 3400 - 0X4002 37FF | Reserved |
| | 0x4002 3000 - 0x4002 33FF | CRC |
| | 0x4002 2C00 - 0x4002 2FFF | Reserved |
| | 0x4002 2800 - 0x4002 2BFF | GPIOK |
| | 0x4002 2400 - 0x4002 27FF | GPIOJ |
| | 0x4002 2000 - 0x4002 23FF | GPIOI |
| | 0x4002 1C00 - 0x4002 1FFF | GPIOH |
| | 0x4002 1800 - 0x4002 1BFF | GPIOG |
| | 0x4002 1400 - 0x4002 17FF | GPIOF |
| | 0x4002 1000 - 0x4002 13FF | GPIOE |
| | 0X4002 0C00 - 0x4002 0FFF | GPIOD |
| | 0x4002 0800 - 0x4002 0BFF | GPIOC |
| | 0x4002 0400 - 0x4002 07FF | GPIOB |
| | 0x4002 0000 - 0x4002 03FF | GPIOA |

Table 13. STM32F745xx and STM32F746xx register boundary addresses (continued)

| Bus | Boundary address | Peripheral |
|---|---|---|
| | 0x4001 6C00- 0x4001 FFFF | Reserved |
| APB2 | 0x4001 6800 - 0x4001 6BFF | LCD-TFT |
| | 0x4001 5C00 - 0x4001 67FF | Reserved |
| | 0x4001 5800 - 0x4001 5BFF | SAI1 |
| | 0x4001 5400 - 0x4001 57FF | SPI6 |
| | 0x4001 5000 - 0x4001 53FF | SPI5 |
| | 0x4001 5400 - 0x4001 57FF | SPI6 |
| | 0x4001 5000 - 0x4001 53FF | SPI5 |
| | 0x4001 4C00 - 0x4001 4FFF | Reserved |
| | 0x4001 4800 - 0x4001 4BFF | TIM11 |
| | 0x4001 4400 - 0x4001 47FF | TIM10 |
| | 0x4001 4000 - 0x4001 43FF | TIM9 |
| | 0x4001 3C00 - 0x4001 3FFF | EXTI |
| | 0x4001 3800 - 0x4001 3BFF | SYSCFG |
| | 0x4001 3400 - 0x4001 37FF | SPI4 |
| | 0x4001 3000 - 0x4001 33FF | SPI1 |
| | 0x4001 2C00 - 0x4001 2FFF | SDMMC1 |
| | 0x4001 2400 - 0x4001 2BFF | Reserved |
| | 0x4001 2000 - 0x4001 23FF | ADC1 - ADC2 - ADC3 |
| | 0x4001 1800 - 0x4001 1FFF | Reserved |
| | 0x4001 1400 - 0x4001 17FF | USART6 |
| | 0x4001 1000 - 0x4001 13FF | USART1 |
| | 0x4001 0800 - 0x4001 0FFF | Reserved |
| | 0x4001 0400 - 0x4001 07FF | TIM8 |
| | 0x4001 0000 - 0x4001 03FF | TIM1 |

Table 13. STM32F745xx and STM32F746xx register boundary addresses (continued)

| Bus | Boundary address | Peripheral |
|---|---|---|
| | 0x4000 8000- 0x4000 FFFF | Reserved |
| APB1 | 0x4000 7C00 - 0x4000 7FFF | UART8 |
| | 0x4000 7800 - 0x4000 7BFF | UART7 |
| | 0x4000 7400 - 0x4000 77FF | DAC |
| | 0x4000 7000 - 0x4000 73FF | PWR |
| | 0x4000 6C00 - 0x4000 6FFF | Reserved |
| | 0x4000 6800 - 0x4000 6BFF | CAN2 |
| | 0x4000 6400 - 0x4000 67FF | CAN1 |
| | 0x4000 6000 - 0x4000 63FF | Reserved |
| | 0x4000 5C00 - 0x4000 5FFF | I2C3 |
| | 0x4000 5800 - 0x4000 5BFF | I2C2 |
| | 0x4000 5400 - 0x4000 57FF | I2C1 |
| | 0x4000 5000 - 0x4000 53FF | UART5 |
| | 0x4000 4C00 - 0x4000 4FFF | UART4 |
| | 0x4000 4800 - 0x4000 4BFF | USART3 |
| | 0x4000 4400 - 0x4000 47FF | USART2 |
| | 0x4000 4000 - 0x4000 43FF | I2S3ext |
| | 0x4000 3C00 - 0x4000 3FFF | SPI3 / I2S3 |
| | 0x4000 3800 - 0x4000 3BFF | SPI2 / I2S2 |
| | 0x4000 3400 - 0x4000 37FF | I2S2ext |
| | 0x4000 3000 - 0x4000 33FF | IWDG |
| | 0x4000 2C00 - 0x4000 2FFF | WWDG |
| | 0x4000 2800 - 0x4000 2BFF | RTC & BKP Registers |
| | 0x4000 2400 - 0x4000 27FF | Reserved |
| | 0x4000 2000 - 0x4000 23FF | TIM14 |
| | 0x4000 1C00 - 0x4000 1FFF | TIM13 |
| | 0x4000 1800 - 0x4000 1BFF | TIM12 |
| | 0x4000 1400 - 0x4000 17FF | TIM7 |
| | 0x4000 1000 - 0x4000 13FF | TIM6 |
| | 0x4000 0C00 - 0x4000 0FFF | TIM5 |
| | 0x4000 0800 - 0x4000 0BFF | TIM4 |
| | 0x4000 0400 - 0x4000 07FF | TIM3 |
| | 0x4000 0000 - 0x4000 03FF | TIM2 |

**Table 14. STM32F745xx and STM32F746xx register boundary addresses**

| Bus | Boundary address | Peripheral |
|---|---|---|
| | 0xE00F FFFF - 0xFFFF FFFF | Reserved |
| Cortex-M7 | 0xE000 0000 - 0xE00F FFFF | Cortex-M7 internal peripherals |
| AHB3 | 0xD000 0000 - 0xDFFF FFFF | FMC bank 6 |
| | 0xC000 0000 - 0xCFFF FFFF | FMC bank 5 |
| | 0xA000 2000 - 0xBFFF FFFF | Reserved |
| | 0xA000 1000 - 0xA000 1FFF | Quad-SPI control register |
| | 0xA000 0000- 0xA000 0FFF | FMC control register |
| | 0x9000 0000 - 0x9FFF FFFF | Quad-SPI |
| | 0x8000 0000 - 0x8FFF FFFF | FMC bank 3 |
| | 0x7000 0000 - 0x7FFF FFFF | FMC bank 2 |
| | 0x6000 0000 - 0x6FFF FFFF | FMC bank 1 |
| | 0x5006 0C00- 0x5FFF FFFF | Reserved |
| AHB2 | 0x5006 0800 - 0x5006 0BFF | RNG |
| | 0x5005 0400 - 0x5006 07FF | Reserved |
| | 0x5005 0000 - 0x5005 03FF | DCMI |
| | 0x5004 0000- 0x5004 FFFF | Reserved |
| | 0x5000 0000 - 0x5003 FFFF | USB OTG FS |

**Table 14. STM32F745xx and STM32F746xx register boundary addresses (continued)**

| Bus | Boundary address | Peripheral |
|---|---|---|
| | 0x4008 0000- 0x4FFF FFFF | Reserved |
| AHB1 | 0x4004 0000 - 0x4007 FFFF | USB OTG HS |
| | 0x4002 BC00- 0x4003 FFFF | Reserved |
| | 0x4002 B000 - 0x4002 BBFF | Chrom-ART (DMA2D) |
| | 0x4002 9400 - 0x4002 AFFF | Reserved |
| | 0x4002 9000 - 0x4002 93FF | ETHERNET MAC |
| | 0x4002 8C00 - 0x4002 8FFF | |
| | 0x4002 8800 - 0x4002 8BFF | |
| | 0x4002 8400 - 0x4002 87FF | |
| | 0x4002 8000 - 0x4002 83FF | |
| | 0x4002 6800 - 0x4002 7FFF | Reserved |
| | 0x4002 6400 - 0x4002 67FF | DMA2 |
| | 0x4002 6000 - 0x4002 63FF | DMA1 |
| | 0x4002 5000 - 0X4002 5FFF | Reserved |
| | 0x4002 4000 - 0x4002 4FFF | BKPSRAM |
| | 0x4002 3C00 - 0x4002 3FFF | Flash interface register |
| | 0x4002 3800 - 0x4002 3BFF | RCC |
| | 0X4002 3400 - 0X4002 37FF | Reserved |
| | 0x4002 3000 - 0x4002 33FF | CRC |
| | 0x4002 2C00 - 0x4002 2FFF | Reserved |
| | 0x4002 2800 - 0x4002 2BFF | GPIOK |
| | 0x4002 2400 - 0x4002 27FF | GPIOJ |
| | 0x4002 2000 - 0x4002 23FF | GPIOI |
| | 0x4002 1C00 - 0x4002 1FFF | GPIOH |
| | 0x4002 1800 - 0x4002 1BFF | GPIOG |
| | 0x4002 1400 - 0x4002 17FF | GPIOF |
| | 0x4002 1000 - 0x4002 13FF | GPIOE |
| | 0X4002 0C00 - 0x4002 0FFF | GPIOD |
| | 0x4002 0800 - 0x4002 0BFF | GPIOC |
| | 0x4002 0400 - 0x4002 07FF | GPIOB |
| | 0x4002 0000 - 0x4002 03FF | GPIOA |

Table 14. STM32F745xx and STM32F746xx register boundary addresses (continued)

| Bus | Boundary address | Peripheral |
|---|---|---|
| | 0x4001 6C00- 0x4001 FFFF | Reserved |
| APB2 | 0x4001 6800 - 0x4001 6BFF | LCD-TFT |
| | 0x4001 6000 - 0x4001 67FF | Reserved |
| | 0x4001 5C00 - 0x4001 5FFF | SAI2 |
| | 0x4001 5800 - 0x4001 5BFF | SAI1 |
| | 0x4001 5400 - 0x4001 57FF | SPI6 |
| | 0x4001 5000 - 0x4001 53FF | SPI5 |
| | 0x4001 4C00 - 0x4001 4FFF | Reserved |
| | 0x4001 4800 - 0x4001 4BFF | TIM11 |
| | 0x4001 4400 - 0x4001 47FF | TIM10 |
| | 0x4001 4000 - 0x4001 43FF | TIM9 |
| | 0x4001 3C00 - 0x4001 3FFF | EXTI |
| | 0x4001 3800 - 0x4001 3BFF | SYSCFG |
| | 0x4001 3400 - 0x4001 37FF | SPI4 |
| | 0x4001 3000 - 0x4001 33FF | SPI1/I2S1 |
| | 0x4001 2C00 - 0x4001 2FFF | SDMMC |
| | 0x4001 2400 - 0x4001 2BFF | Reserved |
| | 0x4001 2000 - 0x4001 23FF | ADC1 - ADC2 - ADC3 |
| | 0x4001 1800 - 0x4001 1FFF | Reserved |
| | 0x4001 1400 - 0x4001 17FF | USART6 |
| | 0x4001 1000 - 0x4001 13FF | USART1 |
| | 0x4001 0800 - 0x4001 0FFF | Reserved |
| | 0x4001 0400 - 0x4001 07FF | TIM8 |
| | 0x4001 0000 - 0x4001 03FF | TIM1 |

Table 14. STM32F745xx and STM32F746xx register boundary addresses (continued)

| Bus | Boundary address | Peripheral |
|---|---|---|
| | 0x4000 8000- 0x4000 FFFF | Reserved |
| APB1 | 0x4000 7C00 - 0x4000 7FFF | UART8 |
| | 0x4000 7800 - 0x4000 7BFF | UART7 |
| | 0x4000 7400 - 0x4000 77FF | DAC |
| | 0x4000 7000 - 0x4000 73FF | PWR |
| | 0x4000 6C00 - 0x4000 6FFF | HDMI-CEC |
| | 0x4000 6800 - 0x4000 6BFF | CAN2 |
| | 0x4000 6400 - 0x4000 67FF | CAN1 |
| | 0x4000 6000 - 0x4000 63FF | I2C4 |
| | 0x4000 5C00 - 0x4000 5FFF | I2C3 |
| | 0x4000 5800 - 0x4000 5BFF | I2C2 |
| | 0x4000 5400 - 0x4000 57FF | I2C1 |
| | 0x4000 5000 - 0x4000 53FF | UART5 |
| | 0x4000 4C00 - 0x4000 4FFF | UART4 |
| | 0x4000 4800 - 0x4000 4BFF | USART3 |
| | 0x4000 4400 - 0x4000 47FF | USART2 |
| | 0x4000 4000 - 0x4000 43FF | SPDIFRX |
| | 0x4000 3C00 - 0x4000 3FFF | SPI3 / I2S3 |
| | 0x4000 3800 - 0x4000 3BFF | SPI2 / I2S2 |
| | 0x4000 3400 - 0x4000 37FF | Reserved |
| | 0x4000 3000 - 0x4000 33FF | IWDG |
| | 0x4000 2C00 - 0x4000 2FFF | WWDG |
| | 0x4000 2800 - 0x4000 2BFF | RTC & BKP Registers |
| | 0x4000 2400 - 0x4000 27FF | LPTIM1 |
| | 0x4000 2000 - 0x4000 23FF | TIM14 |
| | 0x4000 1C00 - 0x4000 1FFF | TIM13 |
| | 0x4000 1800 - 0x4000 1BFF | TIM12 |
| | 0x4000 1400 - 0x4000 17FF | TIM7 |
| | 0x4000 1000 - 0x4000 13FF | TIM6 |
| | 0x4000 0C00 - 0x4000 0FFF | TIM5 |
| | 0x4000 0800 - 0x4000 0BFF | TIM4 |
| | 0x4000 0400 - 0x4000 07FF | TIM3 |
| | 0x4000 0000 - 0x4000 03FF | TIM2 |

# 6 Electrical characteristics

## 6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to $V_{SS}$.

### 6.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at $T_A$ = 25 °C and $T_A$ = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3σ).

### 6.1.2 Typical values

Unless otherwise specified, typical data are based on $T_A$ = 25 °C, $V_{DD}$ = 3.3 V (for the 1.7 V ≤$V_{DD}$ ≤3.6 V voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2σ).

### 6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

### 6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 20*.

### 6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 21*.

**Figure 20. Pin loading conditions**

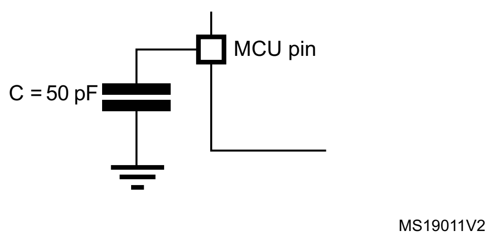
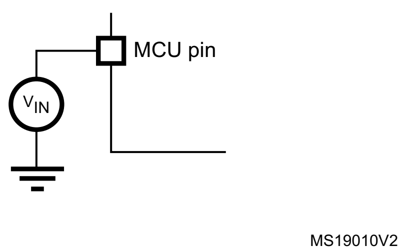
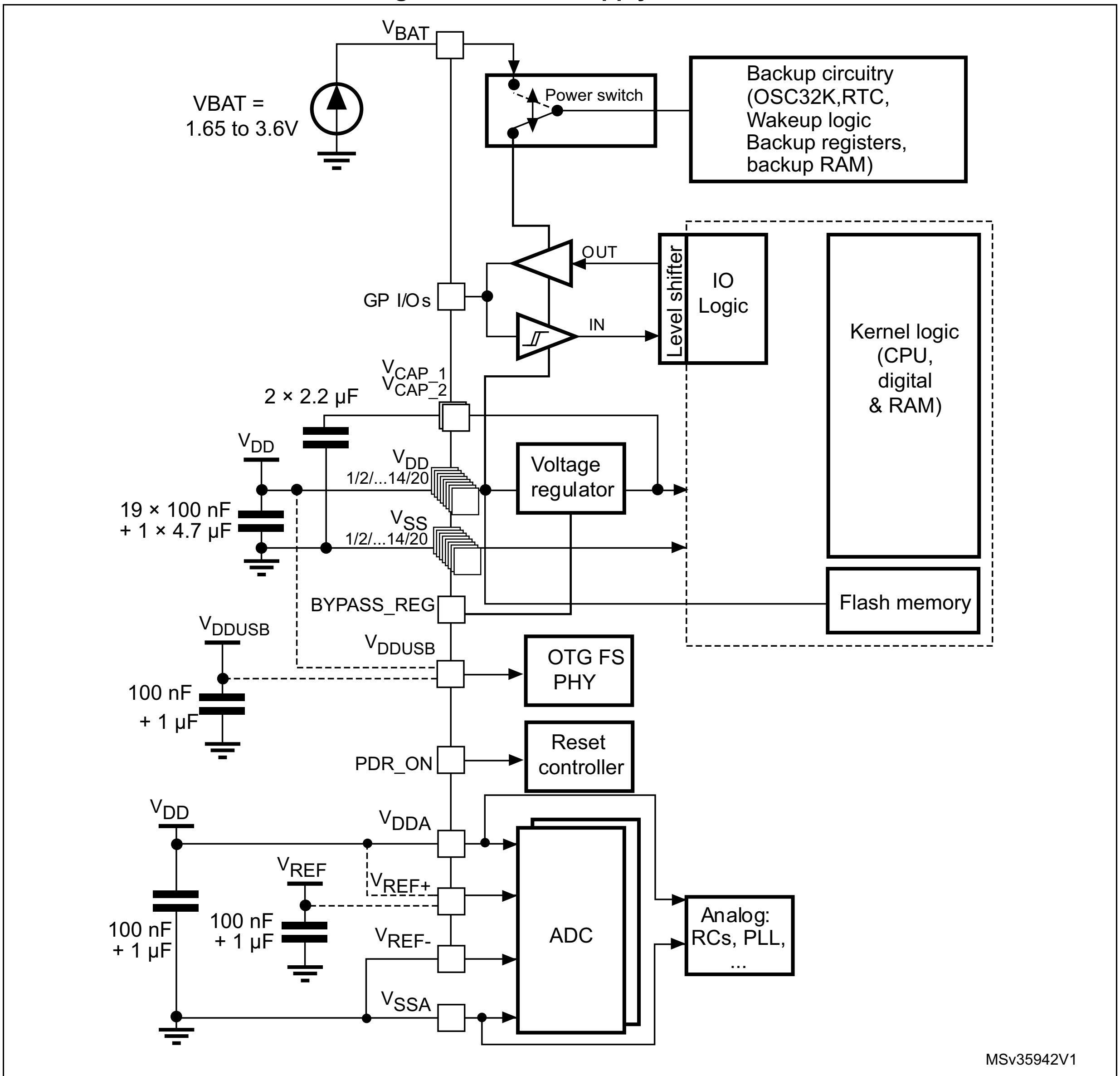



**Figure 21. Pin input voltage**



### 6.1.6 Power supply scheme

**Figure 22. Power supply scheme**

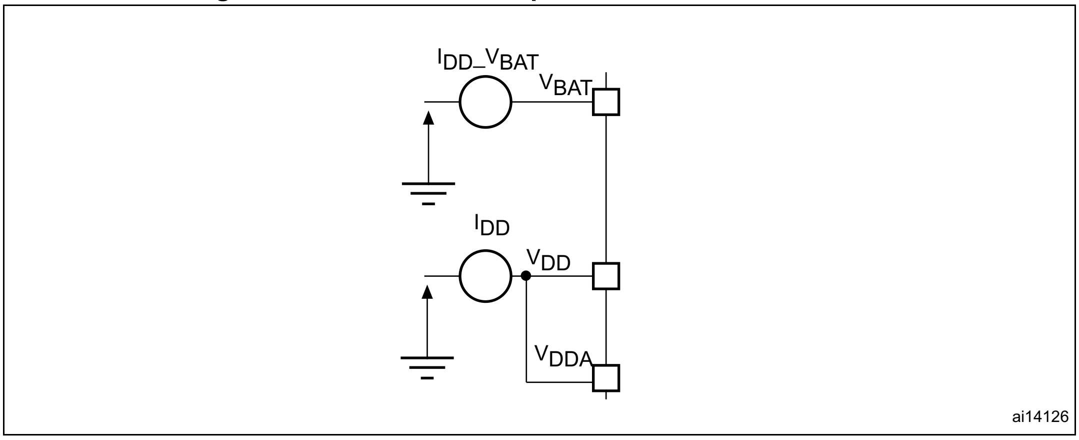



1. To connect BYPASS_REG and PDR_ON pins, refer to *Section 3.17: Power supply supervisor* and *Section 3.18: Voltage regulator*
2. The two 2.2 µF ceramic capacitors should be replaced by two 100 nF decoupling capacitors when the voltage regulator is OFF.
3. The 4.7 µF ceramic capacitor must be connected to one of the $V_{DD}$ pin.
4. $V_{DDA}$=$V_{DD}$ and $V_{SSA}$=$V_{SS}$.

**Caution:** Each power supply pair ($V_{DD}$/$V_{SS}$, $V_{DDA}$/$V_{SSA}$ ...) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure good operation of the device. It is not recommended to remove filtering capacitors to reduce PCB size or cost. This might cause incorrect operation of the device.

### 6.1.7 Current consumption measurement

**Figure 23. Current consumption measurement scheme**




## 6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 15: Voltage characteristics*, *Table 16: Current characteristics*, and *Table 17: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**Table 15. Voltage characteristics**

| Symbol | Ratings | Min | Max | Unit |
|---|---|---|---|---|
| $V_{DD}–V_{SS}$ | External main supply voltage (including $V_{DDA}$, $V_{DD,}$ $V_{BAT}$ and $V_{DDUSB}$) (1) | − 0.3 | 4.0 | V |
| $V_{IN}$ | Input voltage on FT pins(2) | $V_{SS}$ − 0.3 | $V_{DD}$+4.0 | |
| | Input voltage on TTa pins | $V_{SS}$ − 0.3 | 4.0 | |
| | Input voltage on any other pin | $V_{SS}$ − 0.3 | 4.0 | |
| | Input voltage on BOOT pin | $V_{SS}$ | 9.0 | |
| $\|\Delta V_{DDx}\|$ | Variations between different $V_{DD}$ power pins | - | 50 | mV |
| $\|V_{SSX} - V_{SS}\|$ | Variations between all the different ground pins(3) | - | 50 | |
| $V_{ESD(HBM)}$ | Electrostatic discharge voltage (human body model) | see *Section 6.3.15: Absolute maximum ratings (electrical sensitivity)* | | - |

1. All main power ($V_{DD}$, $V_{DDA}$, $V_{DDUSB}$) and ground ($V_{SS}$, $V_{SSA}$) pins must always be connected to the external power supply, in the permitted range.
2. $V_{IN}$ maximum value must always be respected. Refer to *Table 16* for the values of the maximum allowed injected current.
3. Include VREF- pin.

**Table 16. Current characteristics**

| Symbol | Ratings | Max. | Unit |
|---|---|---|---|
| $\Sigma I_{VDD}$ | Total current into sum of all $V_{DD\_x}$ power lines (source)(1) | 320 | mA |
| $\Sigma I_{VSS}$ | Total current out of sum of all $V_{SS\_x}$ ground lines (sink)(1) | − 320 | |
| $\Sigma I_{VDDUSB}$ | Total current into $V_{DDUSB}$ power line (source) | 25 | |
| $I_{VDD}$ | Maximum current into each $V_{DD\_x}$ power line (source)(1) | 100 | |
| $I_{VSS}$ | Maximum current out of each $V_{SS\_x}$ ground line (sink)(1) | − 100 | |
| $I_{IO}$ | Output current sunk by any I/O and control pin | 25 | |
| | Output current sourced by any I/Os and control pin | − 25 | |
| $\Sigma I_{IO}$ | Total output current sunk by sum of all I/O and control pins (2) | 120 | |
| | Total output current sunk by sum of all USB I/Os | 25 | |
| | Total output current sourced by sum of all I/Os and control pins(2) | − 120 | |
| $I_{INJ(PIN)}$ | Injected current on FT, FTf, RST and B pins (3) | − 5/+0 | |
| | Injected current on TTa pins(4) | ±5 | |
| $\Sigma I_{INJ(PIN)}$(4) | Total injected current (sum of all I/O and control pins)(5) | ±25 | |

1. All main power ($V_{DD}$, $V_{DDA}$) and ground ($V_{SS}$, $V_{SSA}$) pins must always be connected to the external power supply, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count LQFP packages.
3. Positive injection is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
4. A positive injection is induced by $V_{IN}$>$V_{DDA}$ while a negative injection is induced by $V_{IN}$<$V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 15: Voltage characteristics* for the values of the maximum allowed input voltage.
5. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

**Table 17. Thermal characteristics**

| Symbol | Ratings | Value | Unit |
|---|---|---|---|
| $T_{STG}$ | Storage temperature range | − 65 to +150 | °C |
| $T_J$ | Maximum junction temperature | 125 | |

## 6.3 Operating conditions

### 6.3.1 General operating conditions

**Table 18. General operating conditions**

| Symbol | Parameter | Conditions[1] | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $f_{HCLK}$ | Internal AHB clock frequency | Power Scale 3 (VOS[1:0] bits in PWR_CR register = 0x01), Regulator ON, over-drive OFF | | 0 | - | 144 | MHz |
| | | Power Scale 2 (VOS[1:0] bits in PWR_CR register = 0x10), Regulator ON | Over-drive OFF | 0 | - | 168 | |
| | | | Over-drive ON | | - | 180 | |
| | | Power Scale 1 (VOS[1:0] bits in PWR_CR register= 0x11), Regulator ON | Over-drive OFF | 0 | - | 180 | |
| | | | Over-drive ON | | - | 216[2] | |
| $f_{PCLK1}$ | Internal APB1 clock frequency | Over-drive OFF | | 0 | - | 45 | |
| | | Over-drive ON | | 0 | - | 54 | |
| $f_{PCLK2}$ | Internal APB2 clock frequency | Over-drive OFF | | 0 | - | 90 | |
| | | Over-drive ON | | 0 | - | 108 | |
| $V_{DD}$ | Standard operating voltage | - | | 1.7[3] | - | 3.6 | V |
| $V_{DDA}$[4][5] | Analog operating voltage (ADC limited to 1.2 M samples) | Must be the same potential as $V_{DD}$[6] | | 1.7[3] | - | 2.4 | |
| | Analog operating voltage (ADC limited to 2.4 M samples) | | | 2.4 | - | 3.6 | |
| $V_{DDUSB}$ | USB supply voltage (supply voltage for PA11,PA12, PB14 and PB15 pins) | USB not used | | 1.7 | 3.3 | 3.6 | |
| | | USB used | | 3.0 | - | 3.6 | |
| $V_{BAT}$ | Backup operating voltage | - | | 1.65 | - | 3.6 | |

**Table 18. General operating conditions (continued)**

| Symbol | Parameter | Conditions(1) | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{12}$ | Regulator ON: 1.2 V internal voltage on $V_{CAP\_1}/V_{CAP\_2}$ pins | Power Scale 3 ((VOS[1:0] bits in PWR_CR register = 0x01), 144 MHz HCLK max frequency | 1.08 | 1.14 | 1.20 | V |
| | | Power Scale 2 ((VOS[1:0] bits in PWR_CR register = 0x10), 168 MHz HCLK max frequency with over-drive OFF or 180 MHz with over-drive ON | 1.20 | 1.26 | 1.32 | |
| | | Power Scale 1 ((VOS[1:0] bits in PWR_CR register = 0x11), 180 MHz HCLK max frequency with over-drive OFF or 216 MHz with over-drive ON | 1.26 | 1.32 | 1.40 | |
| | Regulator OFF: 1.2 V external voltage must be supplied from external regulator on $V_{CAP\_1}/V_{CAP\_2}$ pins(7) | Max frequency 144 MHz | 1.10 | 1.14 | 1.20 | |
| | | Max frequency 168MHz | 1.20 | 1.26 | 1.32 | |
| | | Max frequency 180 MHz | 1.26 | 1.32 | 1.38 | |
| $V_{IN}$ | Input voltage on RST and FT pins(8) | $2\ V \leq V_{DD} \leq 3.6\ V$ | − 0.3 | - | 5.5 | |
| | | $V_{DD} \leq 2\ V$ | − 0.3 | - | 5.2 | |
| | Input voltage on TTa pins | - | − 0.3 | - | $V_{DDA}$+ 0.3 | |
| | Input voltage on BOOT pin | - | 0 | - | 9 | |
| $P_D$ | Power dissipation at $T_A$ = 85 °C for suffix 6 or $T_A$ = 105 °C for suffix 7(9) | LQFP100 | - | - | 465 | mW |
| | | TFBGA100 | - | - | 351 | |
| | | WLCSP143 | - | - | 641 | |
| | | LQFP144 | - | - | 500 | |
| | | LQFP176 | - | - | 526 | |
| | | UFBGA176 | - | - | 513 | |
| | | LQFP208 | - | - | 1053 | |
| | | TFBGA216 | - | - | 690 | |
| TA | Ambient temperature for 6 suffix version | Maximum power dissipation | − 40 | - | 85 | °C |
| | | Low power dissipation(10) | − 40 | - | 105 | |
| | Ambient temperature for 7 suffix version | Maximum power dissipation | − 40 | - | 105 | °C |
| | | Low power dissipation(10) | − 40 | - | 125 | |
| TJ | Junction temperature range | 6 suffix version | − 40 | - | 105 | °C |
| | | 7 suffix version | − 40 | - | 125 | |

1. The over-drive mode is not supported at the voltage ranges from 1.7 to 2.1 V.
2. 216 MHz maximum frequency for 6 suffix version (200 MHz maximum frequency for 7 suffix version).
3. $V_{DD}/V_{DDA}$ minimum value of 1.7 V is obtained with the use of an external power supply supervisor (refer to *Section 3.17.2: Internal reset OFF*).
4. When the ADC is used, refer to *Table 63: ADC characteristics*.
5. If $V_{REF+}$ pin is present, it must respect the following condition: $V_{DDA}$-$V_{REF+}$ < 1.2 V.

6. It is recommended to power $V_{DD}$ and $V_{DDA}$ from the same source. A maximum difference of 300 mV between $V_{DD}$ and $V_{DDA}$ can be tolerated during power-up and power-down operation.
7. The over-drive mode is not supported when the internal regulator is OFF.
8. To sustain a voltage higher than VDD+0.3, the internal Pull-up and Pull-Down resistors must be disabled
9. If $T_A$ is lower, higher $P_D$ values are allowed as long as $T_J$ does not exceed $T_{Jmax}$.
10. In low power dissipation state, $T_A$ can be extended to this range as long as $T_J$ does not exceed $T_{Jmax}$.

**Table 19. Limitations depending on the operating power supply range**

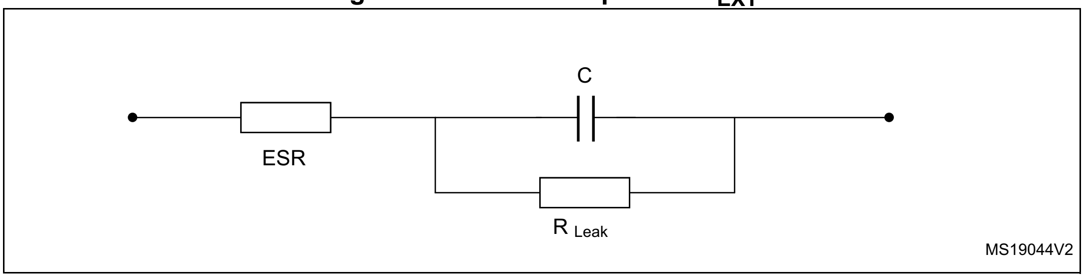
| Operating power supply range | ADC operation | Maximum flash memory access frequency with no wait states ($f_{Flashmax}$) | Maximum HCLK frequency vs flash memory wait states (1)(2) | I/O operation | Possible flash memory operations |
|---|---|---|---|---|---|
| $V_{DD}$ =1.7 to 2.1 V(3) | Conversion time up to 1.2 Msps | 20 MHz | 180 MHz with 8 wait states and over-drive OFF | No I/O compensation | 8-bit erase and program operations only |
| $V_{DD}$ = 2.1 to 2.4 V | Conversion time up to 1.2 Msps | 22 MHz | 216 MHz with 9 wait states and over-drive ON | No I/O compensation | 16-bit erase and program operations |
| $V_{DD}$ = 2.4 to 2.7 V | Conversion time up to 2.4 Msps | 24 MHz | 216 MHz with 8 wait states and over-drive ON | I/O compensation works | 16-bit erase and program operations |
| $V_{DD}$ = 2.7 to 3.6 V(4) | Conversion time up to 2.4 Msps | 30 MHz | 216 MHz with 7 wait states and over-drive ON | I/O compensation works | 32-bit erase and program operations |

1. Applicable only when the code is executed from flash memory. When the code is executed from RAM, no wait state is required.
2. Thanks to the ART accelerator on ITCM interface and L1-cache on AXI interface, the number of wait states given here does not impact the execution speed from flash memory since the ART accelerator or L1-cache allows to achieve a performance equivalent to 0-wait state program execution.
3. $V_{DD}/V_{DDA}$ minimum value of 1.7 V is obtained with the use of an external power supply supervisor (refer to *Section 3.17.2: Internal reset OFF*).
4. The voltage range for USB full speed PHYs can drop down to 2.7 V. However the electrical characteristics of D- and D+ pins will be degraded between 2.7 and 3 V.

## 6.3.2 VCAP1/VCAP2 external capacitor

Stabilization for the main regulator is achieved by connecting an external capacitor $C_{EXT}$ to the VCAP1/VCAP2 pins. $C_{EXT}$ is specified in *Table 20*.

**Figure 24. External capacitor $C_{EXT}$**




1. Legend: ESR is the equivalent series resistance.

Table 20. VCAP1/VCAP2 operating conditions[1]

| Symbol | Parameter | Conditions |
|---|---|---|
| CEXT | Capacitance of external capacitor | 2.2 µF |
| ESR | ESR of external capacitor | < 2 Ω |

1. When bypassing the voltage regulator, the two 2.2 µF $V_{CAP}$ capacitors are not required and should be replaced by two 100 nF decoupling capacitors.

### 6.3.3 Operating conditions at power-up / power-down (regulator ON)

Subject to general operating conditions for $T_A$.

Table 21. Operating conditions at power-up / power-down (regulator ON)

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{VDD}$ | $V_{DD}$ rise time rate | 20 | ∞ | µs/V |
| | $V_{DD}$ fall time rate | 20 | ∞ | |

### 6.3.4 Operating conditions at power-up / power-down (regulator OFF)

Subject to general operating conditions for $T_A$.

Table 22. Operating conditions at power-up / power-down (regulator OFF)[1]

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $t_{VDD}$ | $V_{DD}$ rise time rate | Power-up | 20 | ∞ | µs/V |
| | $V_{DD}$ fall time rate | Power-down | 20 | ∞ | |
| $t_{VCAP}$ | $V_{CAP\_1}$ and $V_{CAP\_2}$ rise time rate | Power-up | 20 | ∞ | |
| | $V_{CAP\_1}$ and $V_{CAP\_2}$ fall time rate | Power-down | 20 | ∞ | |

1. To reset the internal logic at power-down, a reset must be applied on pin PA0 when $V_{DD}$ reach below 1.08 V.

### 6.3.5 Reset and power control block characteristics

The parameters given in *Table 23* are derived from tests performed under ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 18*.

Table 23. Reset and power control block characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{PVD}$ | Programmable voltage detector level selection | PLS[2:0]=000 (rising edge) | 2.09 | 2.14 | 2.19 | V |
| | | PLS[2:0]=000 (falling edge) | 1.98 | 2.04 | 2.08 | V |
| | | PLS[2:0]=001 (rising edge) | 2.23 | 2.30 | 2.37 | V |
| | | PLS[2:0]=001 (falling edge) | 2.13 | 2.19 | 2.25 | V |
| | | PLS[2:0]=010 (rising edge) | 2.39 | 2.45 | 2.51 | V |
| | | PLS[2:0]=010 (falling edge) | 2.29 | 2.35 | 2.39 | V |
| | | PLS[2:0]=011 (rising edge) | 2.54 | 2.60 | 2.65 | V |
| | | PLS[2:0]=011 (falling edge) | 2.44 | 2.51 | 2.56 | V |
| | | PLS[2:0]=100 (rising edge) | 2.70 | 2.76 | 2.82 | V |
| | | PLS[2:0]=100 (falling edge) | 2.59 | 2.66 | 2.71 | V |
| | | PLS[2:0]=101 (rising edge) | 2.86 | 2.93 | 2.99 | V |
| | | PLS[2:0]=101 (falling edge) | 2.75 | 2.84 | 2.92 | V |
| | | PLS[2:0]=110 (rising edge) | 2.96 | 3.03 | 3.10 | V |
| | | PLS[2:0]=110 (falling edge) | 2.85 | 2.93 | 2.99 | V |
| | | PLS[2:0]=111 (rising edge) | 3.07 | 3.14 | 3.21 | V |
| | | PLS[2:0]=111 (falling edge) | 2.95 | 3.03 | 3.09 | V |
| $V_{PVDhyst}$(1) | PVD hysteresis | - | - | 100 | - | mV |
| $V_{POR/PDR}$ | Power-on/power-down reset threshold | Falling edge | 1.60 | 1.68 | 1.76 | V |
| | | Rising edge | 1.64 | 1.72 | 1.80 | V |
| $V_{PDRhyst}$(1) | PDR hysteresis | - | - | 40 | - | mV |
| $V_{BOR1}$ | Brownout level 1 threshold | Falling edge | 2.13 | 2.19 | 2.24 | V |
| | | Rising edge | 2.23 | 2.29 | 2.33 | V |
| $V_{BOR2}$ | Brownout level 2 threshold | Falling edge | 2.44 | 2.50 | 2.56 | V |
| | | Rising edge | 2.53 | 2.59 | 2.63 | V |
| $V_{BOR3}$ | Brownout level 3 threshold | Falling edge | 2.75 | 2.83 | 2.88 | V |
| | | Rising edge | 2.85 | 2.92 | 2.97 | V |
| $V_{BORhyst}$(1) | BOR hysteresis | - | - | 100 | - | mV |
| $T_{RSTTEMPO}$(1)(2) | POR reset temporization | - | 0.5 | 1.5 | 3.0 | ms |
| $I_{RUSH}$(1) | InRush current on voltage regulator power-on (POR or wake-up from Standby) | - | - | 160 | 250 | mA |
| $E_{RUSH}$(1) | InRush energy on voltage regulator power-on (POR or wake-up from Standby) | $V_{DD}$ = 1.7 V, $T_A$ = 105 °C, $I_{RUSH}$ = 171 mA for 31 µs | - | - | 5.4 | µC |

1. Guaranteed by design.
2. The reset temporization is measured from the power-on (POR reset or wake-up from $V_{BAT}$) to the instant when first instruction is read by the user application code.

### 6.3.6 Over-drive switching characteristics

When the over-drive mode switches from enabled to disabled or disabled to enabled, the system clock is stalled during the internal voltage set-up.

The over-drive switching characteristics are given in *Table 24*. They are sbject to general operating conditions for $T_A$.

**Table 24. Over-drive switching characteristics[1]**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Tod_swen | Over_drive switch enable time | HSI | - | 45 | - | µs |
| | | HSE max for 4 MHz and min for 26 MHz | 45 | - | 100 | |
| | | External HSE 50 MHz | - | 40 | - | |
| Tod_swdis | Over_drive switch disable time | HSI | - | 20 | - | |
| | | HSE max for 4 MHz and min for 26 MHz. | 20 | - | 80 | |
| | | External HSE 50 MHz | - | 15 | - | |

1. Guaranteed by design.

### 6.3.7 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The current consumption is measured as described in *Figure 23: Current consumption measurement scheme*.

All the run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to CoreMark code.

### Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at $V_{DD}$ or $V_{SS}$ (no load).
- All peripherals are disabled except if it is explicitly mentioned.
- The flash memory access time is adjusted both to $f_{HCLK}$ frequency and $V_{DD}$ range (see *Table 19: Limitations depending on the operating power supply range*).
- When the regulator is ON, the voltage scaling and over-drive mode are adjusted to $f_{HCLK}$ frequency as follows:
  - Scale 3 for $f_{HCLK} \leq 144$ MHz
  - Scale 2 for 144 MHz < $f_{HCLK} \leq 168$ MHz
  - Scale 1 for 168 MHz < $f_{HCLK} \leq 216$ MHz. The over-drive is only ON at 216 MHz.
- When the regulator is OFF, the V12 is provided externally as described in *Table 18: General operating conditions*:
- The system clock is HCLK, $f_{PCLK1} = f_{HCLK}/4$, and $f_{PCLK2} = f_{HCLK}/2$.
- External clock frequency is 25 MHz and PLL is ON when $f_{HCLK}$ is higher than 25 MHz.
- The typical current consumption values are obtained for 1.7 V ≤ $V_{DD}$ ≤ 3.6 V voltage range and for $T_A$= 25 °C unless otherwise specified.
- The maximum values are obtained for 1.7 V ≤ $V_{DD}$ ≤ 3.6 V voltage range and a maximum ambient temperature ($T_A$) unless otherwise specified.
- For the voltage range 1.7 V ≤ $V_{DD}$ ≤ 3.6 V, the maximum frequency is 180 MHz.

**Table 25. Typical and maximum current consumption in Run mode, code with data processing running from ITCM RAM, regulator ON**

| Symbol | Parameter | Conditions | $f_{HCLK}$ (MHz) | Typ | Max(1) | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | $T_A$ = 25 °C | $T_A$ = 85 °C | $T_A$ = 105 °C | |
| $I_{DD}$ | Supply current in RUN mode | All peripherals enabled(2)(3) | 216 | 178 | 208(4) | 230(4) | - | mA |
| | | | 200 | 165 | 193 | 212 | 230 | |
| | | | 180 | 147 | 171(4) | 185(4) | 198(4) | |
| | | | 168 | 130 | 152 | 164 | 177 | |
| | | | 144 | 100 | 116 | 127 | 137 | |
| | | | 60 | 44 | 52 | 63 | 73 | |
| | | | 25 | 21 | 25 | 36 | 46 | |
| | | All peripherals disabled(3) | 216 | 102 | 120(4) | 141(4) | - | |
| | | | 200 | 95 | 111 | 131 | 149 | |
| | | | 180 | 84 | 98(4) | 112(4) | 125(4) | |
| | | | 168 | 75 | 87 | 100 | 112 | |
| | | | 144 | 58 | 67 | 77 | 88 | |
| | | | 60 | 25 | 30 | 41 | 51 | |
| | | | 25 | 12 | 15 | 25 | 36 | |

1. Guaranteed by characterization results.

2. When analog peripheral blocks such as ADCs, DACs, HSE, LSE, HSI, or LSI are ON, an additional power consumption should be considered.
3. When the ADC is ON (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.73 mA per ADC for the analog part.
4. Guaranteed by test in production.

**Table 26. Typical and maximum current consumption in Run mode, code with data processing running from flash memory (ART ON except prefetch / L1-cache ON) or SRAM on AXI (L1-cache ON), regulator ON**

| Symbol | Parameter | Conditions | $f_{HCLK}$ (MHz) | Typ | Max(1) | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | $T_A$ = 25 °C | $T_A$ = 85 °C | $T_A$ = 105 °C | |
| $I_{DD}$ | Supply current in RUN mode | All peripherals enabled(2)(3) | 216 | 186 | 213 | 234 | - | mA |
| | | | 200 | 172 | 197 | 217 | 235 | |
| | | | 180 | 152 | 175 | 189 | 202 | |
| | | | 168 | 135 | 155 | 168 | 180 | |
| | | | 144 | 104 | 119 | 130 | 140 | |
| | | | 60 | 46 | 53 | 64 | 74 | |
| | | | 25 | 22 | 25 | 36 | 47 | |
| | | All peripherals disabled(3) | 216 | 108 | 124 | 146 | - | |
| | | | 200 | 100 | 115 | 135 | 154 | |
| | | | 180 | 89 | 102 | 116 | 129 | |
| | | | 168 | 79 | 90 | 103 | 115 | |
| | | | 144 | 61 | 69 | 80 | 90 | |
| | | | 60 | 27 | 31 | 42 | 52 | |
| | | | 25 | 12 | 15 | 26 | 36 | |

1. Guaranteed by characterization results.
2. When analog peripheral blocks such as ADCs, DACs, HSE, LSE, HSI, or LSI are ON, an additional power consumption should be considered.
3. When the ADC is ON (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.73 mA per ADC for the analog part.

**Table 27. Typical and maximum current consumption in Run mode, code with data processing running from flash memory or SRAM on AXI (L1-cache disabled), regulator ON**

| Symbol | Parameter | Conditions | $f_{HCLK}$ (MHz) | Typ | Max(1) | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | TA= 25 °C | TA=85 °C | TA=105 °C | |
| $I_{DD}$ | Supply current in RUN mode | All peripherals enabled(2)(3) | 216 | 181 | 210 | 233 | - | mA |
| | | | 200 | 168 | 194 | 216 | 234 | |
| | | | 180 | 153 | 176 | 192 | 206 | |
| | | | 168 | 136 | 157 | 172 | 184 | |
| | | | 144 | 109 | 125 | 137 | 148 | |
| | | | 60 | 53 | 61 | 73 | 84 | |
| | | | 25 | 26 | 30 | 41 | 52 | |
| | | All peripherals disabled(3) | 216 | 105 | 121 | 145 | - | |
| | | | 200 | 98 | 112 | 134 | 153 | |
| | | | 180 | 90 | 103 | 119 | 132 | |
| | | | 168 | 81 | 93 | 107 | 120 | |
| | | | 144 | 67 | 76 | 88 | 89 | |
| | | | 60 | 34 | 40 | 51 | 62 | |
| | | | 25 | 17 | 20 | 31 | 42 | |

1. Guaranteed by characterization results.
2. When analog peripheral blocks such as ADCs, DACs, HSE, LSE, HSI, or LSI are ON, an additional power consumption should be considered.
3. When the ADC is ON (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.73 mA per ADC for the analog part.

**Table 28. Typical and maximum current consumption in Run mode, code with data processing running from flash memory on ITCM interface (ART disabled), regulator ON**

| Symbol | Parameter | Conditions | $f_{HCLK}$ (MHz) | Typ | Max[1] | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | TA= 25 °C | TA=85 °C | TA=105 °C | |
| $I_{DD}$ | Supply current in RUN mode | All peripherals enabled[2][3] | 216 | 205 | 237 | 261 | - | mA |
| | | | 200 | 191 | 219 | 241 | 260 | |
| | | | 180 | 176 | 202 | 218 | 232 | |
| | | | 168 | 158 | 181 | 196 | 209 | |
| | | | 144 | 130 | 148 | 161 | 172 | |
| | | | 60 | 58 | 67 | 79 | 89 | |
| | | | 25 | 27 | 32 | 43 | 54 | |
| | | All peripherals disabled[3] | 216 | 130 | 149 | 173 | - | |
| | | | 200 | 121 | 138 | 160 | 179 | |
| | | | 180 | 113 | 129 | 145 | 159 | |
| | | | 168 | 102 | 116 | 131 | 144 | |
| | | | 144 | 88 | 100 | 112 | 123 | |
| | | | 60 | 40 | 45 | 57 | 68 | |
| | | | 25 | 19 | 22 | 33 | 44 | |

1. Guaranteed by characterization results.
2. When analog peripheral blocks such as ADCs, DACs, HSE, LSE, HSI, or LSI are ON, an additional power consumption should be considered.
3. When the ADC is ON (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.73 mA per ADC for the analog part.

**Table 29. Typical and maximum current consumption in Run mode, code with data processing running from flash memory (ART ON except prefetch / L1-cache ON) or SRAM on AXI (L1-cache ON), regulator OFF**

| Symbol | Parameter | Conditions | $f_{HCLK}$ (MHz) | Typ | | Max[(1)] | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | TA= 25 °C | | TA= 85 °C | | TA= 105 °C | | |
| | | | | IDD12 | IDD | IDD12 | IDD | IDD12 | IDD | IDD12 | IDD | |
| IDD12/ IDD | Supply current in RUN mode from V12 and VDD supply | All Peripherals Enabled[(2)(3)] | 180 | 151 | 1 | 174 | 2 | 190 | 2 | 204 | 2 | mA |
| | | | 168 | 135 | 1 | 156 | 2 | 170 | 2 | 182 | 2 | |
| | | | 144 | 108 | 1 | 124 | 2 | 136 | 2 | 146 | 2 | |
| | | | 60 | 52 | 1 | 60 | 2 | 71 | 2 | 82 | 2 | |
| | | | 25 | 25 | 1 | 29 | 2 | 40 | 2 | 50 | 2 | |
| | | All Peripherals Disabled[(3)] | 180 | 89 | 1 | 102 | 2 | 117 | 2 | 130 | 2 | |
| | | | 168 | 80 | 1 | 91 | 2 | 105 | 2 | 118 | 2 | |
| | | | 144 | 66 | 1 | 75 | 2 | 86 | 2 | 97 | 2 | |
| | | | 60 | 33 | 1 | 38 | 2 | 49 | 2 | 60 | 2 | |
| | | | 25 | 16 | 1 | 18 | 2 | 29 | 2 | 40 | 2 | |

1. Guaranteed by characterization results.
2. When analog peripheral blocks such as ADCs, DACs, HSE, LSE, HSI, or LSI are ON, an additional power consumption should be considered.
3. When the ADC is ON (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.73 mA per ADC for the analog part.

**Table 30. Typical and maximum current consumption in Sleep mode, regulator ON**

| Symbol | Parameter | Conditions | $f_{HCLK}$ (MHz) | Typ | Max[1] | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | $T_A$ = 25 °C | $T_A$ = 85 °C | $T_A$ = 105 °C | |
| $I_{DD}$ | Supply current in Sleep mode | All peripherals enabled[2] | 216 | 116 | 137[3] | 159[3] | - | mA |
| | | | 200 | 108 | 127 | 147 | 166 | |
| | | | 180 | 95 | 112[3] | 126[3] | 140[3] | |
| | | | 168 | 85 | 99 | 112 | 125 | |
| | | | 144 | 65 | 76 | 87 | 98 | |
| | | | 60 | 30 | 35 | 46 | 57 | |
| | | | 25 | 15 | 18 | 29 | 39 | |
| | | All peripherals disabled | 216 | 35 | 46[3] | 71[3] | - | |
| | | | 200 | 32 | 43 | 66 | 86 | |
| | | | 180 | 28 | 38[3] | 53[3] | 70[3] | |
| | | | 168 | 25 | 33 | 47 | 61 | |
| | | | 144 | 20 | 26 | 37 | 50 | |
| | | | 60 | 10 | 14 | 26 | 36 | |
| | | | 25 | 5 | 8 | 20 | 31 | |

1. Guaranteed by characterization results.
2. When analog peripheral blocks such as ADCs, DACs, HSE, LSE, HSI, or LSI are ON, an additional power consumption should be considered.
3. Guaranteed by test in production.

**Table 31. Typical and maximum current consumption in Sleep mode, regulator OFF**

| Symbol | Parameter | Conditions | $f_{HCLK}$ (MHz) | Typ | | Max[1] | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | TA= 25 °C | | TA= 85 °C | | TA= 105 °C | | |
| | | | | IDD12 | IDD | IDD12 | IDD | IDD12 | IDD | IDD12 | IDD | |
| IDD12/ IDD | Supply current in RUN mode from V12 and $V_{DD}$ supply | All Peripherals Enabled[2] | 180 | 94 | 1 | 110 | 2 | 125 | 2 | 138 | 2 | mA |
| | | | 168 | 83 | 1 | 96 | 2 | 111 | 2 | 123 | 2 | |
| | | | 144 | 64 | 1 | 74 | 2 | 85 | 2 | 96 | 2 | |
| | | | 60 | 29 | 1 | 34 | 2 | 44 | 2 | 55 | 2 | |
| | | | 25 | 14 | 1 | 16 | 2 | 27 | 2 | 37 | 2 | |
| | | All Peripherals Disabled | 180 | 27 | 1 | 36 | 2 | 51 | 2 | 68 | 2 | |
| | | | 168 | 24 | 1 | 31 | 2 | 45 | 2 | 59 | 2 | |
| | | | 144 | 18 | 1 | 24 | 2 | 35 | 2 | 48 | 2 | |
| | | | 60 | 9 | 1 | 12 | 2 | 24 | 2 | 34 | 2 | |
| | | | 25 | 4 | 1 | 6 | 2 | 18 | 2 | 29 | 2 | |

1. Guaranteed by characterization results.

2. When analog peripheral blocks such as ADCs, DACs, HSE, LSE, HSI, or LSI are ON, an additional power consumption should be considered.

**Table 32. Typical and maximum current consumptions in Stop mode**

| Symbol | Parameter | Conditions | Typ | Max[(1)] | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | $V_{DD}$ = 3.6 V | | | |
| | | | $T_A$ = 25 °C | $T_A$ = 25 °C | $T_A$ = 85 °C | $T_A$ = 105 °C | |
| $I_{DD\_STOP\_NM}$ (normal mode) | Supply current in Stop mode, main regulator in Run mode | Flash memory in Stop mode, all oscillators OFF, no IWDG | 0.45 | 2.00 | 14.00 | 22.00 | mA |
| | | Flash memory in Deep power down mode, all oscillators OFF | 0.40 | 2.00 | 14.00 | 22.00 | |
| | Supply current in Stop mode, main regulator in Low-power mode | Flash memory in Stop mode, all oscillators OFF, no IWDG | 0.32 | 1.50 | 10.00 | 18.00 | |
| | | Flash memory in Deep power down mode, all oscillators OFF, no IWDG | 0.27 | 1.50 | 10.00 | 18.00 | |
| $I_{DD\_STOP\_UDM}$ (under-drive mode) | Supply current in Stop mode, main regulator in Low voltage and under-drive modes | Regulator in Run mode, flash memory in Deep power down mode, all oscillators OFF, no IWDG | 0.15 | 0.80 | 4.00 | 7.00 | |
| | | Regulator in Low-power mode, flash memory in Deep power down mode, all oscillators OFF, no IWDG | 0.10 | 0.70 | 4.00 | 7.00 | |

1. Data based on characterization, tested in production.

**Table 33. Typical and maximum current consumptions in Standby mode**

| Symbol | Parameter | Conditions | Typ(1) | | | Max(2) | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | $T_A$ = 25 °C | | | $T_A$ = 25 °C | $T_A$ = 85 °C | $T_A$ = 105 °C | |
| | | | $V_{DD}$ = 1.7 V | $V_{DD}$= 2.4 V | $V_{DD}$ = 3.3 V | $V_{DD}$ = 3.3 V | | | |
| $I_{DD\_STBY}$ | Supply current in Standby mode | Backup SRAM OFF, RTC and LSE OFF | 1.7 | 1.9 | 2.3 | 5(3) | 15(3) | 31(3) | µA |
| | | Backup SRAM ON, RTC and LSE OFF | 2.4 | 2.6 | 3.0 | 6(3) | 20(3) | 40(3) | |
| | | Backup SRAM OFF, RTC ON and LSE in low drive mode | 2.1 | 2.4 | 2.9 | 6 | 19 | 39 | |
| | | Backup SRAM OFF, RTC ON and LSE in medium low drive mode | 2.1 | 2.4 | 2.9 | 6 | 19 | 39 | |
| | | Backup SRAM OFF, RTC ON and LSE in medium high drive mode | 2.2 | 2.5 | 3.0 | 7 | 20 | 40 | |
| | | Backup SRAM OFF, RTC ON and LSE in high drive mode | 2.3 | 2.6 | 3.1 | 7 | 20 | 42 | |
| | | Backup SRAM ON, RTC ON and LSE in low drive mode | 2.7 | 3.0 | 3.6 | 8 | 23 | 49 | |
| | | Backup SRAM ON, RTC ON and LSE in Medium low drive mode | 2.7 | 3.0 | 3.6 | 8 | 23 | 49 | |
| | | Backup SRAM ON, RTC ON and LSE in Medium high drive mode | 2.8 | 3.1 | 3.7 | 8 | 24 | 50 | |
| | | Backup SRAM ON, RTC ON and LSE in High drive mode | 2.9 | 3.2 | 3.8 | 8 | 25 | 51 | |

1. PDR is OFF for $V_{DD}$=1.7V. When the PDR is OFF (internal reset OFF), the typical current consumption is reduced by additional 1.2 µA.
2. Guaranteed by characterization results.
3. Based on characterization, tested in production.

**Table 34. Typical and maximum current consumptions in $V_{BAT}$ mode**

| Symbol | Parameter | Conditions(1) | Typ | | | Max(2) | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | $T_A$ =25 °C | | | $T_A$ =85 °C | $T_A$ =105 °C | |
| | | | $V_{BAT}$ = 1.7 V | $V_{BAT}$= 2.4 V | $V_{BAT}$= 3.3 V | $V_{BAT}$ = 3.6 V | | |
| $I_{DD\_VBAT}$ | Supply current in $V_{BAT}$ mode | Backup SRAM OFF, RTC and LSE OFF | 0.03 | 0.03 | 0.04 | 0.2 | 0.4 | µA |
| | | Backup SRAM ON, RTC and LSE OFF | 0.74 | 0.75 | 0.78 | 3.0 | 7.0 | |
| | | Backup SRAM OFF, RTC ON and LSE in low drive mode | 0.40 | 0.52 | 0.72 | 2.8 | 6.5 | |
| | | Backup SRAM OFF, RTC ON and LSE in medium low drive mode | 0.40 | 0.52 | 0.72 | 2.8 | 6.5 | |
| | | Backup SRAM OFF, RTC ON and LSE in medium high drive mode | 0.54 | 0.64 | 0.85 | 3.3 | 7.6 | |
| | | Backup SRAM OFF, RTC ON and LSE in high drive mode | 0.62 | 0.73 | 0.94 | 3.6 | 8.4 | |
| | | Backup SRAM ON, RTC ON and LSE in low drive mode | 1.06 | 1.18 | 1.41 | 5.4 | 12.7 | |
| | | Backup SRAM ON, RTC ON and LSE in Medium low drive mode | 1.16 | 1.28 | 1.51 | 5.8 | 13.6 | |
| | | Backup SRAM ON, RTC ON and LSE in Medium high drive mode | 1.18 | 1.3 | 1.54 | 5.9 | 13.8 | |
| | | Backup SRAM ON, RTC ON and LSE in High drive mode | 1.36 | 1.48 | 1.73 | 6.7 | 15.5 | |

1. Crystal used: Abracon ABS07-120-32.768 kHz-T with a $C_L$ of 6 pF for typical values.
2. Guaranteed by characterization results.

Figure 25. Typical $V_{BAT}$ current consumption (RTC ON/BKP SRAM OFF and LSE in low drive mode)

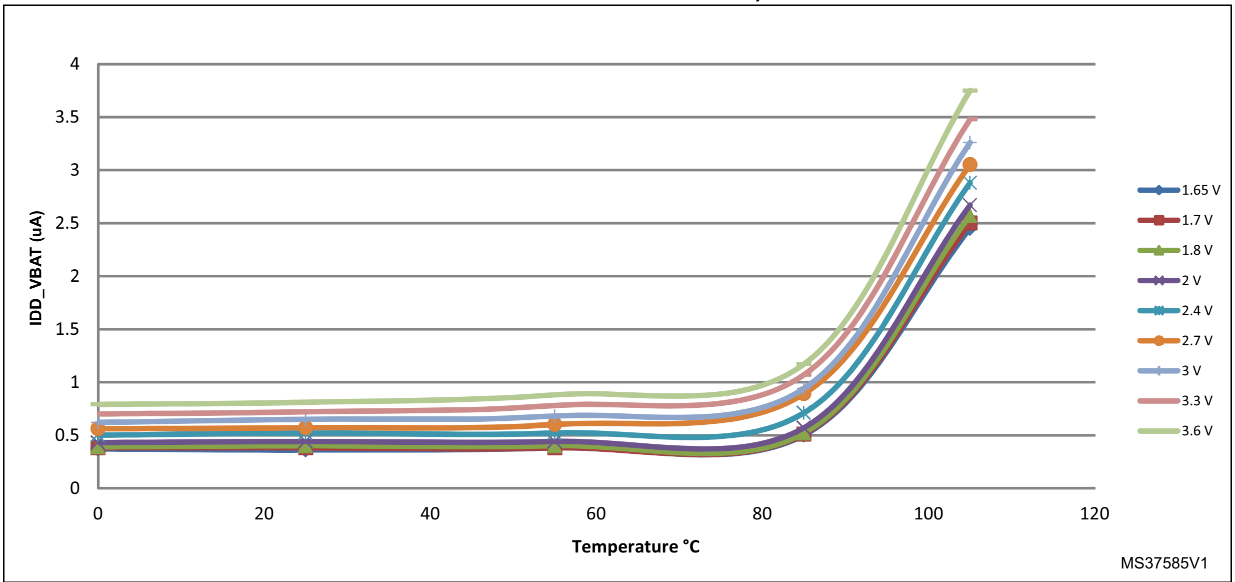



Figure 26. Typical $V_{BAT}$ current consumption (RTC ON/BKP SRAM OFF and LSE in medium low drive mode)

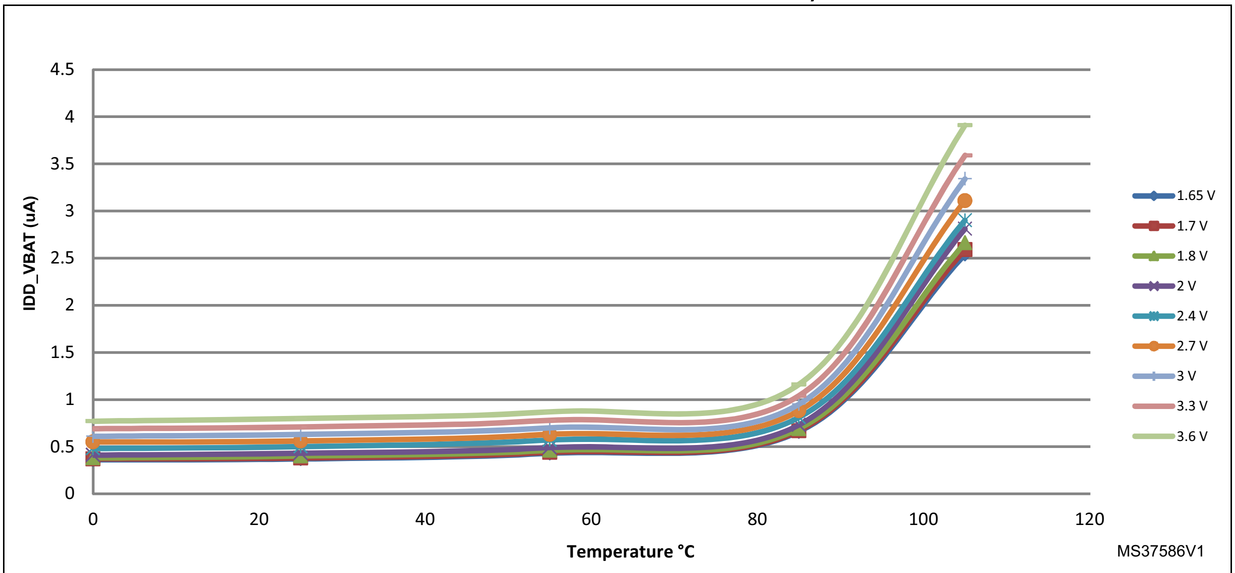


Figure 27. Typical $V_{BAT}$ current consumption (RTC ON/BKP SRAM OFF and LSE in medium high drive mode)

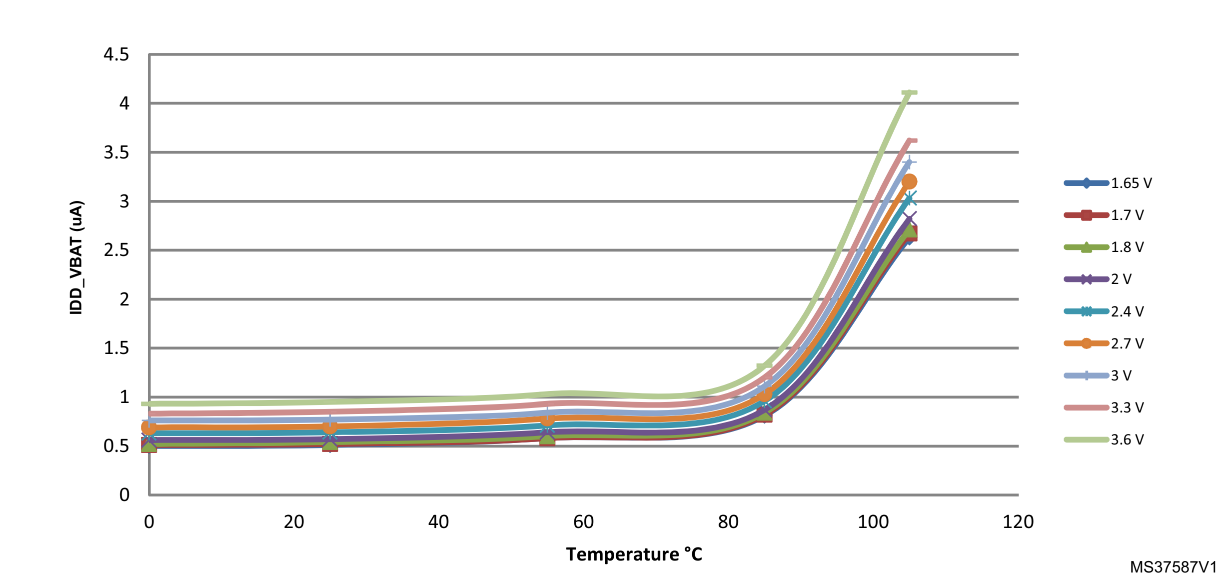



Figure 28. Typical $V_{BAT}$ current consumption (RTC ON/BKP SRAM OFF and LSE in high drive mode)

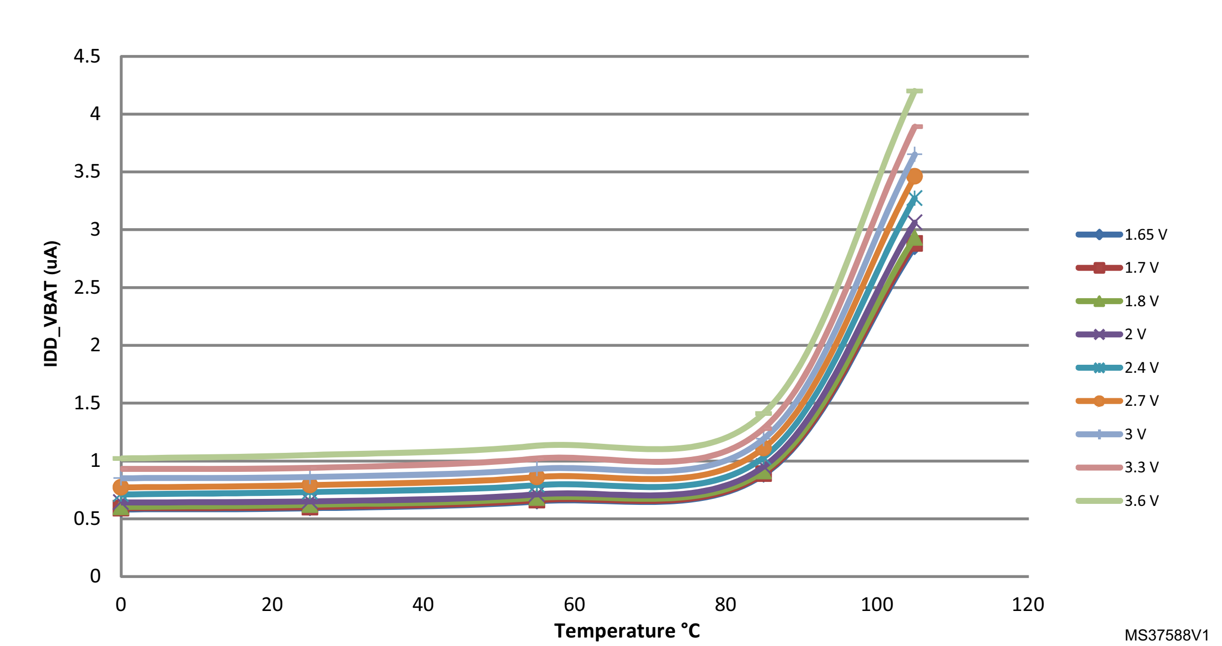
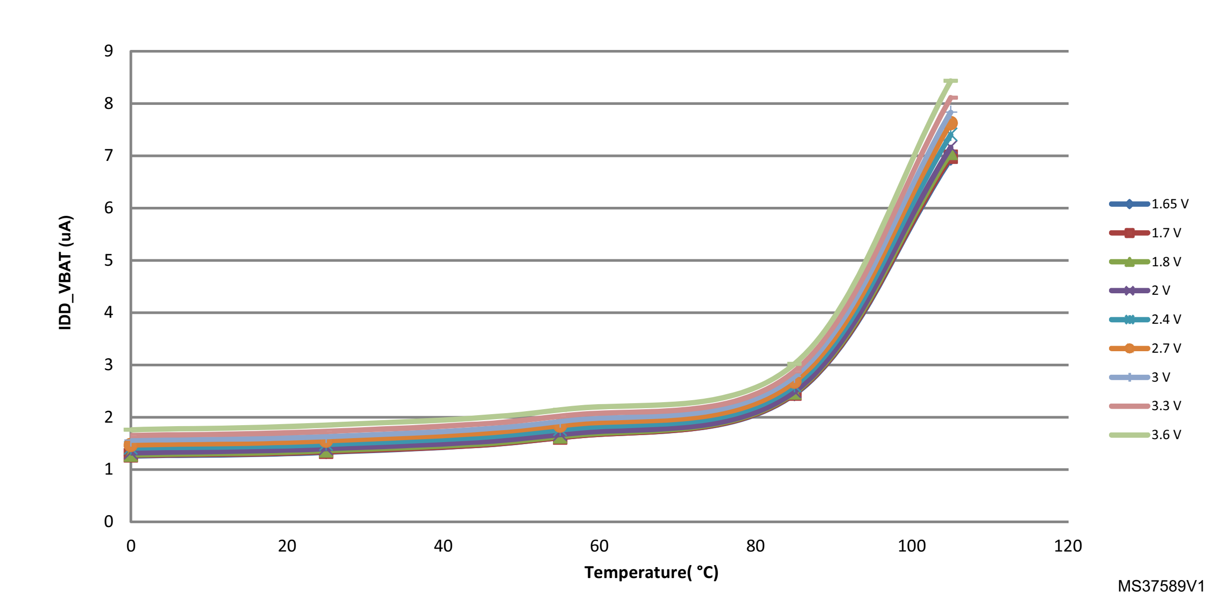


**Figure 29. Typical $V_{BAT}$ current consumption (RTC ON/BKP SRAM OFF and LSE in high medium drive mode)**




### I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

I/O static current consumption

All the I/Os used as input with pull-up or pull-down generate current consumption when the pin is externally held to the opposite level. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in *Table 57: I/O static characteristics*.

For the output pins, any internal or external pull-up or pull-down or external load must also be considered to estimate the current consumption.

Additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins which should be configured as analog inputs.

**Caution:** Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

I/O dynamic current consumption

In addition to the internal peripheral current consumption (see *Table 36: Peripheral current consumption*), the I/Os used by an application also contribute to the current consumption.

When an I/O pin switches, it uses the current from the MCU supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load connected to the pin:

$$I_{SW} = V_{DD} \times f_{SW} \times C$$

where

$I_{SW}$ is the current sunk by a switching I/O to charge/discharge the capacitive load

$V_{DD}$ is the MCU supply voltage

$f_{SW}$ is the I/O switching frequency

C is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT}$

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

**Table 35. Switching output I/O current consumption(1)**

| Symbol | Parameter | Conditions | I/O toggling frequency (fsw) MHz | Typ $V_{DD}$ = 3.3 V | Typ $V_{DD}$ = 1.8 V | Unit |
|---|---|---|---|---|---|---|
| $I_{DDIO}$ | I/O switching Current | $C_{EXT}$ = 0 pF<br>$C = C_{INT} + C_S + C_{EXT}$ | 2 | 0.1 | 0.1 | mA |
| | | | 8 | 0.4 | 0.2 | |
| | | | 25 | 1.1 | 0.7 | |
| | | | 50 | 2.4 | 1.3 | |
| | | | 60 | 3.1 | 1.6 | |
| | | | 84 | 4.3 | 2.4 | |
| | | | 90 | 4.9 | 2.6 | |
| | | | 100 | 5.4 | 2.8 | |
| | | | 108 | 5.6 | - | |
| | | $C_{EXT}$ = 10 pF<br>$C = C_{INT} + C_S + C_{EXT}$ | 2 | 0.2 | 0.1 | |
| | | | 8 | 0.6 | 0.3 | |
| | | | 25 | 1.8 | 1.1 | |
| | | | 50 | 3.1 | 2.3 | |
| | | | 60 | 4.6 | 3.4 | |
| | | | 84 | 9.7 | 3.6 | |
| | | | 90 | 10.12 | 5.2 | |
| | | | 100 | 14.92 | 5.4 | |
| | | | 108 | 18.11 | - | |

**Table 35. Switching output I/O current consumption[1] (continued)**

| Symbol | Parameter | Conditions | I/O toggling frequency (fsw) MHz | Typ $V_{DD}$ = 3.3 V | Typ $V_{DD}$ = 1.8 V | Unit |
|---|---|---|---|---|---|---|
| $I_{DDIO}$ | I/O switching Current | $C_{EXT}$ = 22 pF<br>$C = C_{INT} + C_S + C_{EXT}$ | 2 | 0.3 | 0.1 | mA |
| | | | 8 | 1.0 | 0.5 | |
| | | | 25 | 3.5 | 1.6 | |
| | | | 50 | 5.9 | 4.2 | |
| | | | 60 | 10.0 | 4.4 | |
| | | | 84 | 19.12 | 5.8 | |
| | | | 90 | 19.6 | - | |
| | | $C_{EXT}$ = 33 pF<br>$C = C_{INT} + C_S + C_{EXT}$ | 2 | 0.3 | 0.2 | |
| | | | 8 | 1.3 | 0.7 | |
| | | | 25 | 3.5 | 2.3 | |
| | | | 50 | 10.26 | 5.19 | |
| | | | 60 | 16.53 | - | |

1. CINT + $C_{S,}$ PCB board capacitance including the pad pin is estimated to15 pF.

### On-chip peripheral current consumption

The MCU is placed under the following conditions:

- At startup, all I/O pins are in analog input configuration.
- All peripherals are disabled unless otherwise mentioned.
- I/O compensation cell enabled.
- The ART/L1-cache is ON.
- Scale 1 mode selected, internal digital voltage V12 = 1.32 V.
- HCLK is the system clock. $f_{PCLK1} = f_{HCLK}/4$, and $f_{PCLK2} = f_{HCLK}/2$.
  The given value is calculated by measuring the difference of current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on
  - $f_{HCLK}$ = 216 MHz (Scale 1 + over-drive ON), $f_{HCLK}$ = 168 MHz (Scale 2), $f_{HCLK}$ = 144 MHz (Scale 3)
- Ambient operating temperature is 25 °C and $V_{DD}$=3.3 V.

**Table 36. Peripheral current consumption**

| Peripheral | | $I_{DD}$(Typ)[1] | | | Unit |
|---|---|---|---|---|---|
| | | Scale 1 | Scale 2 | Scale 3 | |
| AHB1 (up to 216 MHz) | GPIOA | 2.2 | 2.1 | 1.9 | µA/MHz |
| | GPIOB | 2.1 | 1.8 | 1.7 | |
| | GPIOC | 2.3 | 2.0 | 1.9 | |
| | GPIOD | 2.2 | 1.9 | 1.8 | |
| | GPIOE | 2.2 | 1.9 | 1.8 | |
| | GPIOF | 2.2 | 1.9 | 1.8 | |
| | GPIOG | 2.1 | 1.8 | 1.7 | |
| | GPIOH | 2.0 | 1.7 | 1.7 | |
| | GPIOI | 2.3 | 2.0 | 1.7 | |
| | GPIOJ | 2.2 | 1.9 | 1.7 | |
| | GPIOK | 2.0 | 1.7 | 1.7 | |
| | CRC | 1.0 | 0.9 | 0.8 | |
| | BKPSRAM | 0.8 | 0.7 | 0.6 | |
| | DMA1 | 2.7 x N + 5.1 | 2.6 x N + 4.7 | 2.2 x N + 4 | |
| | DMA2 | 2.2 x N + 4.9 | 2.6 x N + 4.4 | 2.2 x N + 4.1 | |
| | DMA2D | 87.1 | 82.5 | 69.6 | |
| | ETH_MAC<br>ETH_MAC_TX<br>ETH_MAC_RX<br>ETH_MAC_PTP | 42.1 | 39.7 | 34.1 | |
| | OTG_HS<br>OTG_HS+ULPI | 57.5 | 54.4 | 47.6 | |
| AHB2 (up to 216 MHz) | DCMI | 5.1 | 4.7 | 4.0 | µA/MHz |
| | RNG | 2.8 | 2.4 | 2.3 | |
| | USB_OTG_FS | 31.8 | 29.9 | 25.8 | |
| AHB3 (up to 216 MHz) | FMC | 18.9 | 17.7 | 15.2 | µA/MHz |
| | QSPI | 23.2 | 21.8 | 18.5 | |
| Bus matrix[2] | | 21.06 | 20.3 | 17.2 | µA/MHz |

**Table 36. Peripheral current consumption (continued)**

| Peripheral | | $I_{DD}$(Typ)[1] | | | Unit |
|---|---|---|---|---|---|
| | | Scale 1 | Scale 2 | Scale 3 | |
| APB1 (up to 54 MHz) | TIM2 | 19.8 | 18.7 | 16.1 | µA/MHz |
| | TIM3 | 16.6 | 15.1 | 13.6 | |
| | TIM4 | 16.2 | 15.1 | 13.3 | |
| | TIM5 | 19 | 17.8 | 15.8 | |
| | TIM6 | 3 | 2.7 | 2.5 | |
| | TIM7 | 3 | 2.7 | 2.5 | |
| | TIM12 | 12.4 | 11.3 | 10.3 | |
| | TIM13 | 6 | 5.3 | 5 | |
| | TIM14 | 6 | 5.3 | 5 | |
| | LPTIM1 | 9.4 | 8.7 | 8.1 | |
| | WWDG | 1.8 | 1.6 | 1.4 | |
| | SPI2/I2S2[3] | 3 | 2.9 | 2.8 | |
| | SPI3/I2S3[3] | 3.2 | 2.9 | 2.8 | |
| | SPDIFRX | 2.2 | 2 | 1.7 | |
| | USART2 | 12.8 | 12 | 10.8 | |
| | USART3 | 15.6 | 14.2 | 13.1 | |
| | UART4 | 11.8 | 10.7 | 9.7 | |
| | UART5 | 11.2 | 10 | 9.2 | |
| | I2C1 | 9.8 | 8.7 | 7.8 | |
| | I2C2 | 8.6 | 7.8 | 7.2 | |
| | I2C3 | 8.6 | 7.8 | 7.2 | |
| | I2C4 | 12 | 10.9 | 9.7 | |
| | CAN1 | 6.8 | 6 | 5.6 | |
| | CAN2 | 6.8 | 6 | 5.8 | |
| | CEC | 1 | 0.7 | 0.8 | |
| | PWR | 1.2 | 0.9 | 0.8 | |
| | DAC[4] | 3 | 2.7 | 2.5 | |
| | UART7 | 12.4 | 11.6 | 10 | |
| | UART8 | 10.4 | 9.3 | 8.6 | |

**Table 36. Peripheral current consumption (continued)**

| Peripheral | | $I_{DD}$(Typ)[(1)] | | | Unit |
|---|---|---|---|---|---|
| | | Scale 1 | Scale 2 | Scale 3 | |
| APB2 (up to 108 MHz) | TIM1 | 25.2 | 23.9 | 20.4 | µA/MHz |
| | TIM8 | 25.3 | 24 | 20.4 | |
| | USART1 | 10.3 | 9.8 | 8.2 | |
| | USART6 | 10.1 | 9.7 | 8.1 | |
| | ADC1[(5)] | 4.5 | 4.4 | 3.5 | |
| | ADC2[(5)] | 4.5 | 4.4 | 3.5 | |
| | ADC3[(5)] | 4.5 | 4.4 | 3.3 | |
| | SDMMC1 | 8.5 | 7.9 | 6.7 | |
| | SPI1/I2S1[(3)] | 3.1 | 3 | 2.5 | |
| | SPI4 | 3.1 | 3 | 2.5 | |
| | SYSCFG | 1.5 | 1.4 | 1 | |
| | TIM9 | 8.8 | 8.4 | 6.9 | |
| | TIM10 | 5.6 | 5.2 | 4.3 | |
| | TIM11 | 5.4 | 5.2 | 4.3 | |
| | SPI5 | 3 | 2.8 | 2.2 | |
| | SPI6 | 3 | 2.8 | 2.2 | |
| | SAI1 | 3.4 | 3.3 | 2.6 | |
| | SAI2 | 3.3 | 3.2 | 2.5 | |
| | LTDC | 56.7 | 53.8 | 45.7 | |

1. When the I/O compensation cell is ON, $I_{DD}$ typical value increases by 0.22 mA.
2. The BusMatrix is automatically active when at least one master is ON.
3. To enable an I2S peripheral, first set the I2SMOD bit and then the I2SE bit in the SPI_I2SCFGR register.
4. When the DAC is ON and EN1/2 bits are set in DAC_CR register, add an additional power consumption of 0.75 mA per DAC channel for the analog part.
5. When the ADC is ON (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.73 mA per ADC for the analog part.

### 6.3.8 Wake-up time from low-power modes

The wake-up times given in *Table 37* are measured starting from the wake-up event trigger up to the first instruction executed by the CPU:

- For Stop or Sleep modes: the wake-up event is WFE.
- WKUP (PA0) pin is used to wake-up from Standby, Stop and Sleep modes.

All timings are derived from tests performed under ambient temperature and $V_{DD}$=3.3 V.

**Table 37. Low-power mode wake-up timings**

| Symbol | Parameter | Conditions | Typ(1) | Max(1) | Unit |
|---|---|---|---|---|---|
| $t_{WUSLEEP}$(2) | Wake up from Sleep | - | 13 | 13 | CPU clock cycles |
| $t_{WUSTOP}$(2) | Wake up from Stop mode with MR/LP regulator in normal mode | Main regulator is ON | 14 | 14.9 | µs |
| | | Main regulator is ON and flash memory in Deep power down mode | 104.1 | 107.6 | |
| | | Low power regulator is ON | 21.4 | 24.2 | |
| | | Low power regulator is ON and flash memory in Deep power down mode | 111.5 | 116.5 | |
| $t_{WUSTOP}$(2) | Wake up from Stop mode with MR/LP regulator in Under-drive mode | Main regulator in under-drive mode (flash memory in Deep power-down mode) | 107.4 | 113.2 | |
| | | Low power regulator in under-drive mode (flash memory in Deep power-down mode ) | 112.7 | 120 | |
| tWUSTDBY (2) | Wake up from Standby mode | Exit Standby mode on rising edge | 308 | 313 | |
| | | Exit Standby mode on falling edge | 307 | 313 | |

1. Guaranteed by characterization results.
2. The wake-up times are measured from the wake-up event to the point in which the application code reads the first

### 6.3.9 External clock source characteristics

#### High-speed external user clock generated from an external source

In bypass mode the HSE oscillator is switched off and the input pin is a standard I/O. The external clock signal has to respect the *Table 57: I/O static characteristics*. However, the recommended clock input waveform is shown in *Figure 30*.

The characteristics given in *Table 38* result from tests performed using an high-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 18*.

**Table 38. High-speed external user clock characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{HSE\_ext}$ | External user clock source frequency(1) | - | 1 | - | 50 | MHz |
| $V_{HSEH}$ | OSC_IN input pin high level voltage | | $0.7V_{DD}$ | - | $V_{DD}$ | V |
| $V_{HSEL}$ | OSC_IN input pin low level voltage | | $V_{SS}$ | - | $0.3V_{DD}$ | |
| $t_{w(HSE)}$ $t_{w(HSE)}$ | OSC_IN high or low time(1) | | 5 | - | - | ns |
| $t_{r(HSE)}$ $t_{f(HSE)}$ | OSC_IN rise or fall time(1) | | - | - | 10 | |
| $C_{in(HSE)}$ | OSC_IN input capacitance(1) | - | - | 5 | - | pF |
| $DuCy_{(HSE)}$ | Duty cycle | - | 45 | - | 55 | % |
| $I_L$ | OSC_IN Input leakage current | $V_{SS} \leq V_{IN} \leq V_{DD}$ | - | - | ±1 | µA |

1. Guaranteed by design.

#### Low-speed external user clock generated from an external source

In bypass mode the LSE oscillator is switched off and the input pin is a standard I/O. The external clock signal has to respect the *Table 57: I/O static characteristics*. However, the recommended clock input waveform is shown in *Figure 31*.

The characteristics given in *Table 39* result from tests performed using an low-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 18*.

**Table 39. Low-speed external user clock characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{LSE\_ext}$ | User External clock source frequency(1) | - | - | 32.768 | 1000 | kHz |
| $V_{LSEH}$ | OSC32_IN input pin high level voltage | | $0.7V_{DD}$ | - | $V_{DD}$ | V |
| $V_{LSEL}$ | OSC32_IN input pin low level voltage | | $V_{SS}$ | - | $0.3V_{DD}$ | |
| $t_{w(LSE)}$ $t_{f(LSE)}$ | OSC32_IN high or low time(1) | | 450 | - | - | ns |
| $t_{r(LSE)}$ $t_{f(LSE)}$ | OSC32_IN rise or fall time(1) | | - | - | 50 | |
| $C_{in(LSE)}$ | OSC32_IN input capacitance(1) | - | - | 5 | - | pF |
| $DuCy_{(LSE)}$ | Duty cycle | - | 30 | - | 70 | % |
| $I_L$ | OSC32_IN Input leakage current | $V_{SS} \leq V_{IN} \leq V_{DD}$ | - | - | ±1 | µA |

1. Guaranteed by design.

**Figure 30. High-speed external clock source AC timing diagram**

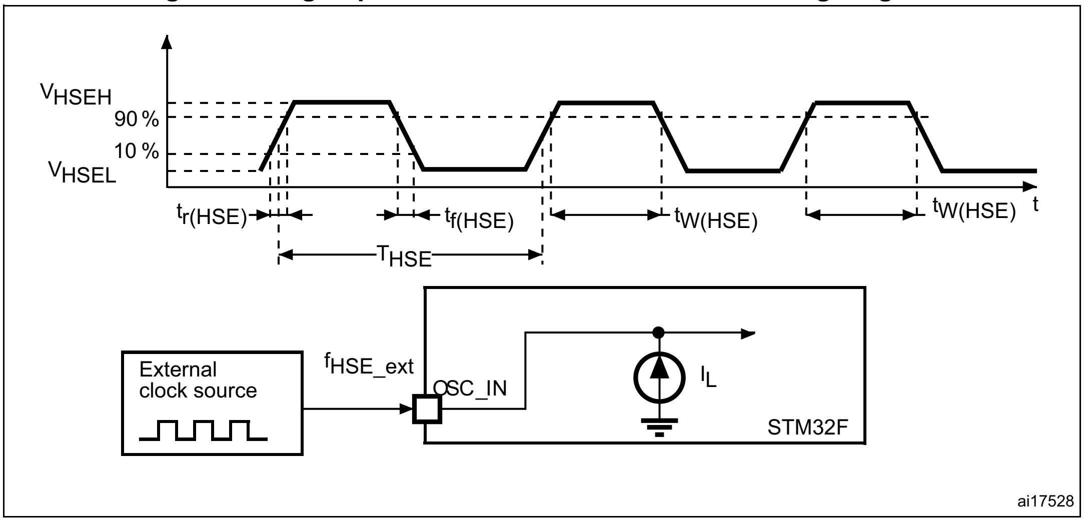
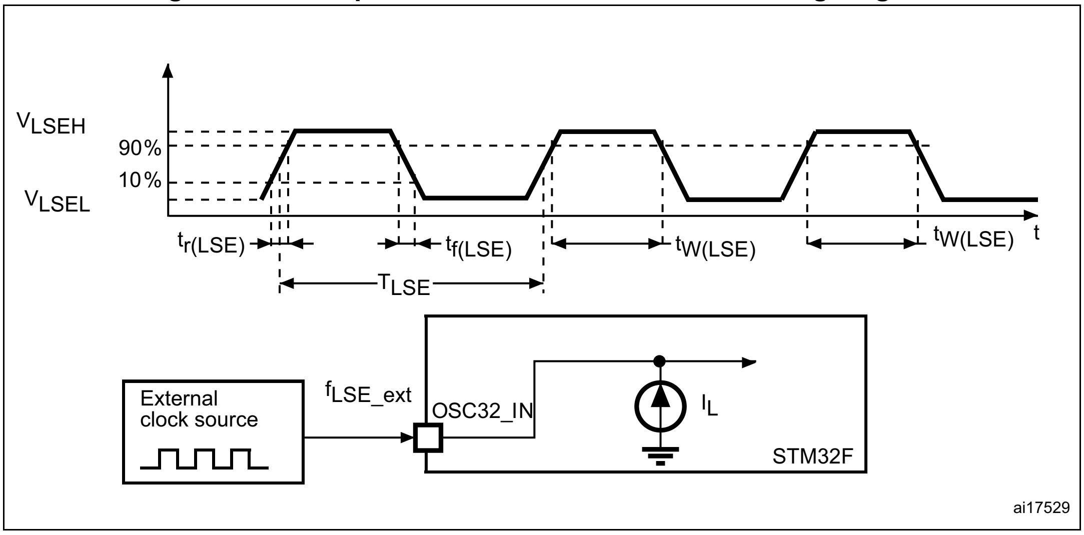


**Figure 31. Low-speed external clock source AC timing diagram**




## High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 26 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 40*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

**Table 40. HSE 4-26 MHz oscillator characteristics(1)**

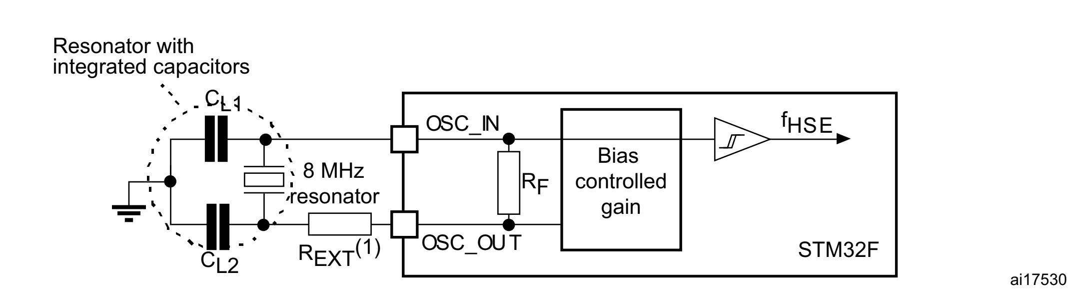
| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{OSC\_IN}$ | Oscillator frequency | - | 4 | - | 26 | MHz |
| $R_F$ | Feedback resistor | - | - | 200 | - | kΩ |
| $I_{DD}$ | HSE current consumption | $V_{DD}$=3.3 V, ESR= 30 Ω, $C_L$=5 pF@25 MHz | - | 450 | - | µA |
| | | $V_{DD}$=3.3 V, ESR= 30 Ω, $C_L$=10 pF@25 MHz | - | 530 | - | |
| $ACC_{HSE}$(2) | HSE accuracy | - | – 500 | - | 500 | ppm |
| $G_m$_crit_max | Maximum critical crystal $g_m$ | Startup | - | - | 1 | mA/V |
| $t_{SU(HSE)}$(3) | Startup time | $V_{DD}$ is stabilized | - | 2 | - | ms |

1. Guaranteed by design.
2. This parameter depends on the crystal used in the application. The minimum and maximum values must be respected to comply with USB standard specifications.
3. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is based on characterization results. It is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

For $C_{L1}$ and $C_{L2}$, it is recommended to use high-quality external ceramic capacitors designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see Figure 32). $C_{L1}$ and $C_{L2}$ are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of $C_{L1}$ and $C_{L2}$. PCB and MCU pin capacitance must be included when sizing $C_{L1}$ and $C_{L2}$.

Note: *For information on selecting the crystal, refer to the application note AN2867 “Guidelines for Oscillator Design on STM8AF/AL/S and STM32 MCUs/MPUs.” available from the ST website www.st.com.*

**Figure 32. Typical application with an 8 MHz crystal**




1. $R_{EXT}$ value depends on the crystal characteristics.

### Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in Table 41. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

**Table 41. LSE oscillator characteristics ($f_{LSE}$ = 32.768 kHz) (1)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{DD}$ | LSE current consumption | LSEDRV[1:0]=00<br>Low drive capability | - | 250 | - | nA |
| | | LSEDRV[1:0]=10<br>Medium low drive capability | - | 300 | - | |
| | | LSEDRV[1:0]=01<br>Medium high drive capability | - | 370 | - | |
| | | LSEDRV[1:0]=11<br>High drive capability | - | 480 | - | |

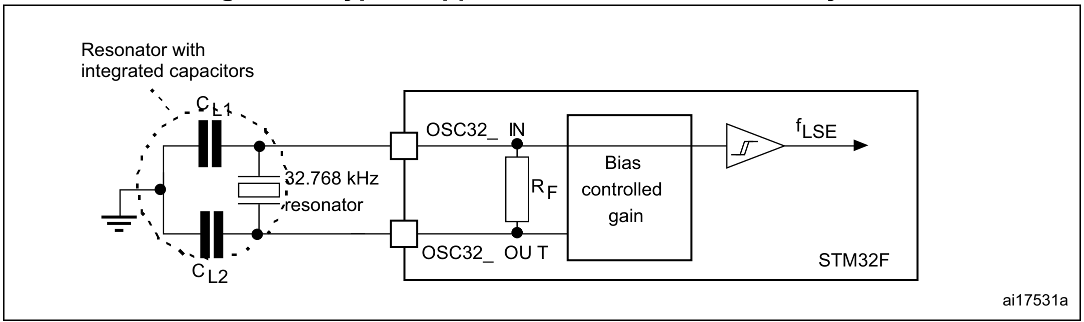
**Table 41. LSE oscillator characteristics ($f_{LSE}$ = 32.768 kHz) (1) (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $G_m$_crit_max | Maximum critical crystal $g_m$ | LSEDRV[1:0]=00<br>Low drive capability | - | - | 0.48 | µA/V |
| | | LSEDRV[1:0]=10<br>Medium low drive capability | - | - | 0.75 | |
| | | LSEDRV[1:0]=01<br>Medium high drive capability | - | - | 1.7 | |
| | | LSEDRV[1:0]=11<br>High drive capability | - | - | 2.7 | |
| $t_{SU}$(2) | start-up time | $V_{DD}$ is stabilized | - | 2 | - | s |

1. Guaranteed by design.
2. Guaranteed by characterization results. $t_{SU}$ is the start-up time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

*Note: For information on selecting the crystal, refer to the application note AN2867 "Guidelines for Oscillator Design on STM8AF/AL/S and STM32 MCUs/MPUs." available from the ST website www.st.com.*

**Figure 33. Typical application with a 32.768 kHz crystal**



## 6.3.10 Internal clock source characteristics

The parameters given in Table 42 and Table 43 are derived from tests performed under ambient temperature and $V_{DD}$ supply voltage conditions summarized in Table 18.

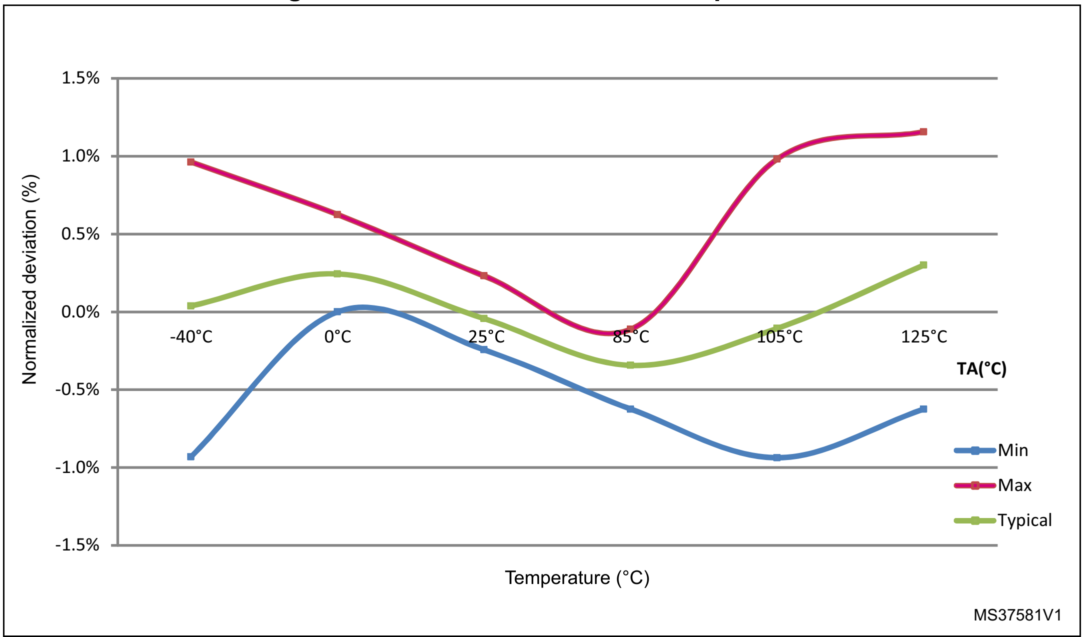
### High-speed internal (HSI) RC oscillator

Table 42. HSI oscillator characteristics [(1)]

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{HSI}$ | Frequency | - | - | 16 | - | MHz |
| $ACC_{HSI}$ | HSI user trimming step[(2)] | - | - | - | 1 | % |
| | Accuracy of the HSI oscillator | $T_A$ = –40 to 105 °C[(3)] | − 8 | - | 4.5 | % |
| | | $T_A$ = –10 to 85 °C[(3)] | − 4 | - | 4 | % |
| | | $T_A$ = 25 °C[(4)] | − 1 | - | 1 | % |
| $t_{su(HSI)}$[(2)] | HSI oscillator startup time | - | - | 2.2 | 4 | µs |
| $I_{DD(HSI)}$[(2)] | HSI oscillator power consumption | - | - | 60 | 80 | µA |

1. $V_{DD}$ = 3.3 V, PLL OFF, $T_A$ = –40 to 125 °C unless otherwise specified.
2. Guaranteed by design.
3. Guaranteed by characterization results.
4. Factory calibrated, parts not soldered.

Figure 34. HSI deviation versus temperature




1. Guaranteed by characterization results.

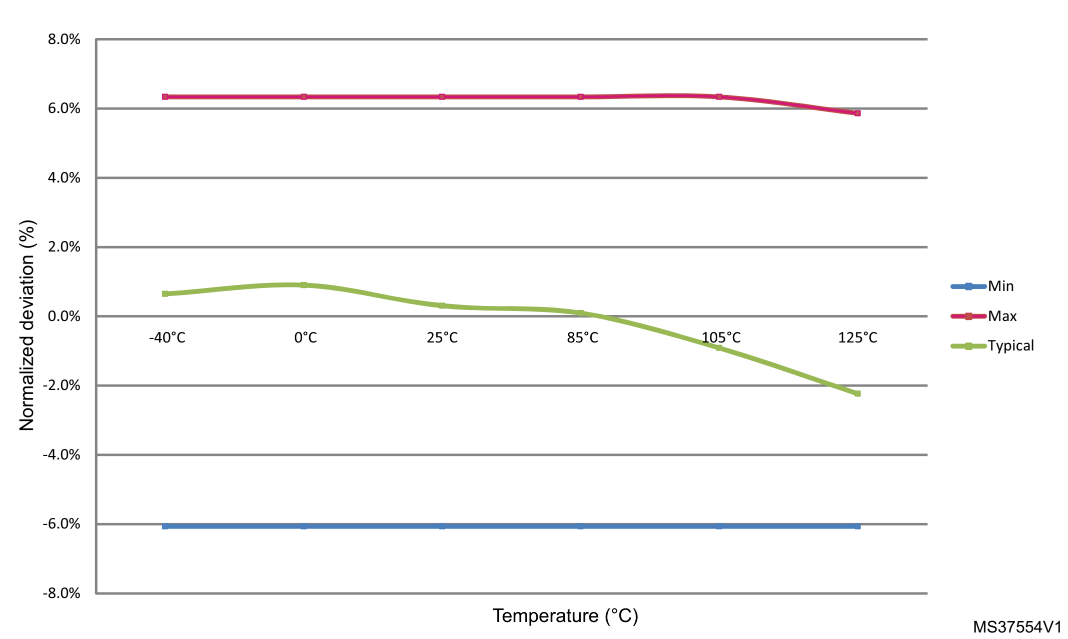
### Low-speed internal (LSI) RC oscillator

**Table 43. LSI oscillator characteristics (1)**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $f_{LSI}$ (2) | Frequency | 17 | 32 | 47 | kHz |
| $t_{su(LSI)}$ (3) | LSI oscillator startup time | - | 15 | 40 | µs |
| $I_{DD(LSI)}$ (3) | LSI oscillator power consumption | - | 0.4 | 0.6 | µA |

1. $V_{DD}$ = 3 V, $T_A$ = –40 to 105 °C unless otherwise specified.
2. Guaranteed by characterization results.
3. Guaranteed by design.

**Figure 35. LSI deviation versus temperature**




## 6.3.11 PLL characteristics

The parameters given in *Table 44* and *Table 45* are derived from tests performed under temperature and $V_{DD}$ supply voltage conditions summarized in *Table 18*.

**Table 44. Main PLL characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{PLL\_IN}$ | PLL input clock(1) | - | 0.95(2) | 1 | 2.10 | MHz |
| $f_{PLL\_OUT}$ | PLL multiplier output clock | - | 24 | - | 216 | |
| $f_{PLL48\_OUT}$ | 48 MHz PLL multiplier output clock | - | - | 48 | 75 | |
| $f_{VCO\_OUT}$ | PLL VCO output | - | 100 | - | 432 | |

**Table 44. Main PLL characteristics (continued)**

<table>
<tr><th>Symbol</th><th>Parameter</th><th colspan="2">Conditions</th><th>Min</th><th>Typ</th><th>Max</th><th>Unit</th></tr>
<tr><td rowspan="2">$t_{LOCK}$</td><td rowspan="2">PLL lock time</td><td colspan="2">VCO freq = 100 MHz</td><td>75</td><td>-</td><td>200</td><td rowspan="2">µs</td></tr>
<tr><td colspan="2">VCO freq = 432 MHz</td><td>100</td><td>-</td><td>300</td></tr>
<tr><td rowspan="7">Jitter(3)</td><td rowspan="2">Cycle-to-cycle jitter</td><td rowspan="4">System clock 216 MHz</td><td>RMS</td><td>-</td><td>25</td><td>-</td><td rowspan="7">ps</td></tr>
<tr><td>peak to peak</td><td>-</td><td>±150</td><td>-</td></tr>
<tr><td rowspan="2">Period Jitter</td><td>RMS</td><td>-</td><td>15</td><td>-</td></tr>
<tr><td>peak to peak</td><td>-</td><td>±200</td><td>-</td></tr>
<tr><td>Main clock output (MCO) for RMII Ethernet</td><td colspan="2">Cycle to cycle at 50 MHz on 1000 samples</td><td>-</td><td>32</td><td>-</td></tr>
<tr><td>Main clock output (MCO) for MII Ethernet</td><td colspan="2">Cycle to cycle at 25 MHz on 1000 samples</td><td>-</td><td>40</td><td>-</td></tr>
<tr><td>Bit Time CAN jitter</td><td colspan="2">Cycle to cycle at 1 MHz on 1000 samples</td><td>-</td><td>330</td><td>-</td></tr>
<tr><td>$I_{DD(PLL)}$(4)</td><td>PLL power consumption on $V_{DD}$</td><td colspan="2">VCO freq = 100 MHz<br>VCO freq = 432 MHz</td><td>0.15<br>0.45</td><td>-</td><td>0.40<br>0.75</td><td>mA</td></tr>
<tr><td>$I_{DDA(PLL)}$(4)</td><td>PLL power consumption on $V_{DDA}$</td><td colspan="2">VCO freq = 100 MHz<br>VCO freq = 432 MHz</td><td>0.30<br>0.55</td><td>-</td><td>0.40<br>0.85</td><td>mA</td></tr>
</table>

1. Take care of using the appropriate division factor M to obtain the specified PLL input clock values. The M factor is shared between PLL and PLLI2S.
2. Guaranteed by design.
3. The use of 2 PLLs in parallel could degraded the Jitter up to +30%.
4. Guaranteed by characterization results.

**Table 45. PLLI2S characteristics**

<table>
<tr><th>Symbol</th><th>Parameter</th><th>Conditions</th><th>Min</th><th>Typ</th><th>Max</th><th>Unit</th></tr>
<tr><td>$f_{PLLI2S\_IN}$</td><td>PLLI2S input clock(1)</td><td>-</td><td>0.95(2)</td><td>1</td><td>2.10</td><td rowspan="5">MHz</td></tr>
<tr><td>$f_{PLLI2SP\_OUT}$</td><td>PLLI2S multiplier output clock for SPDIFRX</td><td>-</td><td>-</td><td>-</td><td>216</td></tr>
<tr><td>$f_{PLLI2SQ\_OUT}$</td><td>PLLI2S multiplier output clock for SAI</td><td>-</td><td>-</td><td>-</td><td>216</td></tr>
<tr><td>$f_{PLLI2SR\_OUT}$</td><td>PLLI2S multiplier output clock for I2S</td><td>-</td><td>-</td><td>-</td><td>216</td></tr>
<tr><td>$f_{VCO\_OUT}$</td><td>PLLI2S VCO output</td><td>-</td><td>100</td><td>-</td><td>432</td></tr>
<tr><td rowspan="2">$t_{LOCK}$</td><td rowspan="2">PLLI2S lock time</td><td>VCO freq = 100 MHz</td><td>75</td><td>-</td><td>200</td><td rowspan="2">µs</td></tr>
<tr><td>VCO freq = 432 MHz</td><td>100</td><td>-</td><td>300</td></tr>
</table>

**Table 45. PLLI2S characteristics (continued)**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| Jitter[3] | Master I2S clock jitter | Cycle to cycle at 12.288 MHz on 48KHz period, N=432, R=5 | RMS | - | 90 | - | ps |
| | | | peak to peak | - | ±280 | - | |
| | | Average frequency of 12.288 MHz<br>N = 432, R = 5<br>on 1000 samples | | - | 90 | - | ps |
| | WS I2S clock jitter | Cycle to cycle at 48 KHz on 1000 samples | | - | 400 | - | ps |
| $I_{DD(PLLI2S)}$[4] | PLLI2S power consumption on $V_{DD}$ | VCO freq = 100 MHz<br>VCO freq = 432 MHz | | 0.15<br>0.45 | - | 0.40<br>0.75 | mA |
| $I_{DDA(PLLI2S)}$[4] | PLLI2S power consumption on $V_{DDA}$ | VCO freq = 100 MHz<br>VCO freq = 432 MHz | | 0.30<br>0.55 | - | 0.40<br>0.85 | mA |

1. Take care of using the appropriate division factor M to have the specified PLL input clock values.
2. Guaranteed by design.
3. Value given with main PLL running.
4. Guaranteed by characterization results.

**Table 46. PLLISAI characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{PLLSAI\_IN}$ | PLLSAI input clock[1] | - | 0.95[2] | 1 | 2.10 | MHz |
| $f_{PLLSAIP\_OUT}$ | PLLSAI multiplier output clock for 48 MHz | - | - | 48 | 75 | |
| $f_{PLLSAIQ\_OUT}$ | PLLSAI multiplier output clock for SAI | - | - | - | 216 | |
| $f_{PLLSAIR\_OUT}$ | PLLSAI multiplier output clock for LCD-TFT | - | - | - | 216 | |
| $f_{VCO\_OUT}$ | PLLSAI VCO output | - | 100 | - | 432 | |
| $t_{LOCK}$ | PLLSAI lock time | VCO freq = 100 MHz | 75 | - | 200 | µs |
| | | VCO freq = 432 MHz | 100 | - | 300 | |

**Table 46. PLLISAI characteristics (continued)**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| Jitter(3) | Master SAI clock jitter | Cycle to cycle at 12.288 MHz on 48KHz period, N=432, R=5 | RMS | - | 90 | - | ps |
| | | | peak to peak | - | ±280 | - | ps |
| | | Average frequency of 12.288 MHz N = 432, R = 5 on 1000 samples | | - | 90 | - | ps |
| | FS clock jitter | Cycle to cycle at 48 KHz on 1000 samples | | - | 400 | - | ps |
| $I_{DD(PLLSAI)}$(4) | PLLSAI power consumption on $V_{DD}$ | VCO freq = 100 MHz<br>VCO freq = 432 MHz | | 0.15<br>0.45 | - | 0.40<br>0.75 | mA |
| $I_{DDA(PLLSAI)}$(4) | PLLSAI power consumption on $V_{DDA}$ | VCO freq = 100 MHz<br>VCO freq = 432 MHz | | 0.30<br>0.55 | - | 0.40<br>0.85 | mA |

1. Take care of using the appropriate division factor M to have the specified PLL input clock values.
2. Guaranteed by design.
3. Value given with main PLL running.
4. Guaranteed by characterization results.

### 6.3.12 PLL spread spectrum clock generation (SSCG) characteristics

The spread spectrum clock generation (SSCG) feature allows to reduce electromagnetic interferences (see *Table 53: EMI characteristics*). It is available only on the main PLL.

**Table 47. SSCG parameters constraint**

| Symbol | Parameter | Min | Typ | Max(1) | Unit |
|---|---|---|---|---|---|
| $f_{Mod}$ | Modulation frequency | - | - | 10 | KHz |
| md | Peak modulation depth | 0.25 | - | 2 | % |
| MODEPER * INCSTEP | - | - | - | $2^{15} - 1$ | - |

1. Guaranteed by design.

Equation 1

The frequency modulation period (MODEPER) is given by the equation below:

$$MODEPER = round[f_{PLL\_IN} / (4 \times f_{Mod})]$$

$f_{PLL\_IN}$ and $f_{Mod}$ must be expressed in Hz.

As an example:

If $f_{PLL\_IN}$ = 1 MHz, and $f_{MOD}$ = 1 kHz, the modulation depth (MODEPER) is given by equation 1:

$$MODEPER = round[10^6 / (4 \times 10^3)] = 250$$

Equation 2

Equation 2 allows to calculate the increment step (INCSTEP):

$$\mathrm{INCSTEP} = \mathrm{round}[((2^{15} - 1) \times \mathrm{md} \times \mathrm{PLLN}) / (100 \times 5 \times \mathrm{MODEPER})]$$

$f_{VCO\_OUT}$ must be expressed in MHz.

With a modulation depth (md) = ±2 % (4 % peak to peak), and PLLN = 240 (in MHz):

$$\mathrm{INCSTEP} = \mathrm{round}[((2^{15} - 1) \times 2 \times 240) / (100 \times 5 \times 250)] = 126\mathrm{md(quantitazed)}\%$$

An amplitude quantization error may be generated because the linear modulation profile is obtained by taking the quantized values (rounded to the nearest integer) of MODPER and INCSTEP. As a result, the achieved modulation depth is quantized. The percentage quantized modulation depth is given by the following formula:

$$\mathrm{md}_{\mathrm{quantized}}\% = (\mathrm{MODEPER} \times \mathrm{INCSTEP} \times 100 \times 5) / ((2^{15} - 1) \times \mathrm{PLLN})$$

As a result:

$$\mathrm{md}_{\mathrm{quantized}}\% = (250 \times 126 \times 100 \times 5) / ((2^{15} - 1) \times 240) = 2.002\%\mathrm{(peak)}$$

*Figure 36* and *Figure 37* show the main PLL output clock waveforms in center spread and down spread modes, where:

F0 is $f_{PLL\_OUT}$ nominal.

$T_{mode}$ is the modulation period.

md is the modulation depth.

**Figure 36. PLL output clock waveforms in center spread mode**

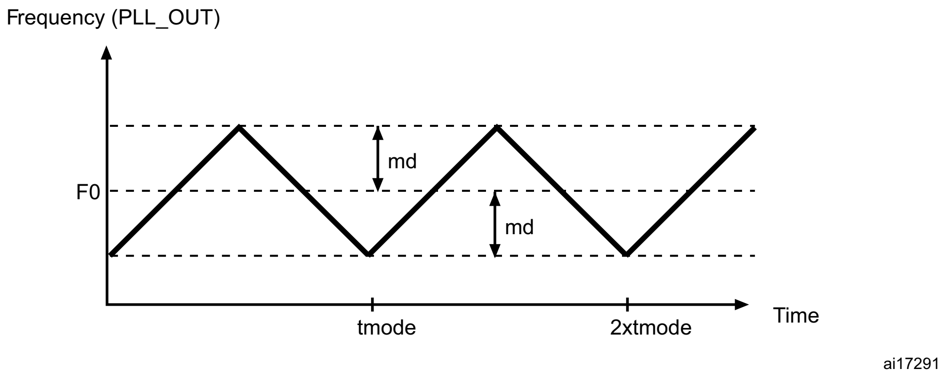
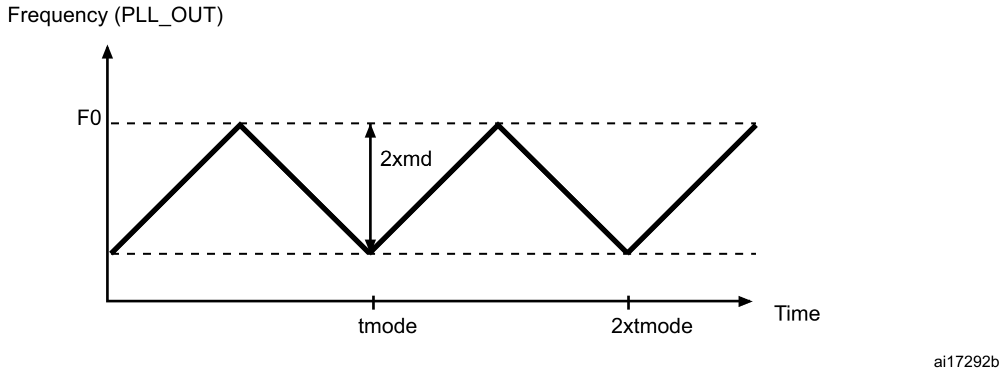


**Figure 37. PLL output clock waveforms in down spread mode**




## 6.3.13 Memory characteristics

### Flash memory

The characteristics are given at TA = –40 to 105 °C unless otherwise specified.

The devices are shipped to customers with the flash memory erased.

**Table 48. Flash memory characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{DD}$ | Supply current | Write / Erase 8-bit mode, $V_{DD}$ = 1.7 V | - | 14 | - | mA |
| | | Write / Erase 16-bit mode, $V_{DD}$ = 2.1 V | - | 17 | - | |
| | | Write / Erase 32-bit mode, $V_{DD}$ = 3.3 V | - | 24 | - | |

**Table 49. Flash memory programming**

| Symbol | Parameter | Conditions | Min(1) | Typ | Max(1) | Unit |
|---|---|---|---|---|---|---|
| $t_{prog}$ | Word programming time | Program/erase parallelism (PSIZE) = x 8/16/32 | - | 16 | 100(2) | µs |
| $t_{ERASE32KB}$ | Sector (32 KB) erase time | Program/erase parallelism (PSIZE) = x 8 | - | 400 | 800 | ms |
| | | Program/erase parallelism (PSIZE) = x 16 | - | 250 | 600 | |
| | | Program/erase parallelism (PSIZE) = x 32 | - | 200 | 500 | |
| $t_{ERASE128KB}$ | Sector (128 KB) erase time | Program/erase parallelism (PSIZE) = x 8 | - | 1100 | 2400 | ms |
| | | Program/erase parallelism (PSIZE) = x 16 | - | 800 | 1400 | |
| | | Program/erase parallelism (PSIZE) = x 32 | - | 500 | 1100 | |

Table 49. Flash memory programming (continued)

| Symbol | Parameter | Conditions | Min(1) | Typ | Max(1) | Unit |
|---|---|---|---|---|---|---|
| $t_{ERASE256KB}$ | Sector (256 KB) erase time | Program/erase parallelism (PSIZE) = x 8 | - | 2.1 | 4 | s |
| | | Program/erase parallelism (PSIZE) = x 16 | - | 1.5 | 2.6 | |
| | | Program/erase parallelism (PSIZE) = x 32 | - | 1 | 2 | |
| $t_{ME}$ | Mass erase time | Program/erase parallelism (PSIZE) = x 8 | - | 8 | 16 | s |
| | | Program/erase parallelism (PSIZE) = x 16 | - | 5.6 | 11.2 | |
| | | Program/erase parallelism (PSIZE) = x 32 | - | 4 | 8 | |
| $V_{prog}$ | Programming voltage | 32-bit program operation | 2.7 | - | 3.6 | V |
| | | 16-bit program operation | 2.1 | - | 3.6 | V |
| | | 8-bit program operation | 1.7 | - | 3.6 | V |

1. Guaranteed by characterization results.
2. The maximum programming time is measured after 100K erase operations.

Table 50. Flash memory programming with $V_{PP}$

| Symbol | Parameter | Conditions | Min(1) | Typ | Max(1) | Unit |
|---|---|---|---|---|---|---|
| $t_{prog}$ | Double word programming | $T_A$ = 0 to +40 °C<br>$V_{DD}$ = 3.3 V<br>$V_{PP}$ = 8.5 V | - | 16 | 100(2) | µs |
| $t_{ERASE32KB}$ | Sector (32 KB) erase time | | - | 180 | - | ms |
| $t_{ERASE128KB}$ | Sector (128 KB) erase time | | - | 450 | - | |
| $t_{ERASE256KB}$ | Sector (256 KB) erase time | | - | 900 | - | |
| $t_{ME}$ | Mass erase time | | - | 6.9 | - | s |
| $V_{prog}$ | Programming voltage | - | 2.7 | - | 3.6 | V |
| $V_{PP}$ | $V_{PP}$ voltage range | - | 7 | - | 9 | V |
| $I_{PP}$ | Minimum current sunk on the $V_{PP}$ pin | - | 10 | - | - | mA |
| $t_{VPP}$(3) | Cumulative time during which $V_{PP}$ is applied | - | - | - | 1 | hour |

1. Guaranteed by design.
2. The maximum programming time is measured after 100K erase operations.
3. $V_{PP}$ should only be connected during programming/erasing.

**Table 51. Flash memory endurance and data retention**

| Symbol | Parameter | Conditions | Value Min[1] | Unit |
|---|---|---|---|---|
| $N_{END}$ | Endurance | $T_A$ = –40 to +85 °C (6 suffix versions)<br>$T_A$ = –40 to +105 °C (7 suffix versions) | 10 | kcycles |
| $t_{RET}$ | Data retention | 1 kcycle[2] at $T_A$ = 85 °C | 30 | Years |
| | | 1 kcycle[2] at $T_A$ = 105 °C | 10 | |
| | | 10 kcycles[2] at $T_A$ = 55 °C | 20 | |

1. Guaranteed by characterization results.
2. Cycling performed over the whole temperature range.

### 6.3.14 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

#### Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A burst of fast transient voltage (positive and negative) is applied to $V_{DD}$ and $V_{SS}$ through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 52*. They are based on the EMS levels and classes defined in application note AN1709.

**Table 52. EMS characteristics**

| Symbol | Parameter | Conditions | Level/ Class |
|---|---|---|---|
| $V_{FESD}$ | Voltage limits to be applied on any I/O pin to induce a functional disturbance | $V_{DD}$ = 3.3 V, $T_A$ = +25 °C, $f_{HCLK}$ = 216 MHz, conforms to IEC 61000-4-2 | 2B |
| $V_{EFTB}$ | Fast transient voltage burst limits to be applied through 100 pF on $V_{DD}$ and $V_{SS}$ pins to induce a functional disturbance | $V_{DD}$ = 3.3 V, TFBGA216, $T_A$ =+25 °C, $f_{HCLK}$ = 216 MHz, conforms to IEC 61000-4-2 | 4A |

As a consequence, it is recommended to add a serial resistor (1 kΩ) located as close as possible to the MCU to the pins exposed to noise (connected to tracks longer than 50 mm on PCB).

### Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

### Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application, executing EEMBC code, is running. This emission test is compliant with SAE IEC61967-2 standard which specifies the test board and the pin loading.

**Table 53. EMI characteristics**

| Symbol | Parameter | Conditions | Monitored frequency band | Max vs. [$f_{HSE}/f_{CPU}$] | Unit |
|---|---|---|---|---|---|
| | | | | 25/200 MHz | |
| $S_{EMI}$ | Peak(1) | VDD = 3.6 V, TA = 25 °C, LQFP64 package compliant with IEC 61967-2 | 0.1 MHz to 30 MHz | 7 | dBµV |
| | | | 30 MHz to 130 MHz | -1 | |
| | | | 130 MHz to 1 GHz | 8 | |
| | | | 1 GHz to 2 GHz | 7 | |
| | Level(2) | | 0.1 MHz to 2 GHz | 2.5 | - |

1. Refer to AN1709 "EMI radiated test" chapter.
2. Refer to AN1709 "EMI level classification" chapter

## 6.3.15 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

### Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the ANSI/ESDA/JEDEC JS-001-2012 and ANSI/ESD S5.3.1-2009 standards.

**Table 54. ESD absolute maximum ratings**

| Symbol | Ratings | Conditions | Class | Maximum value(1) | Unit |
|---|---|---|---|---|---|
| $V_{ESD(HBM)}$ | Electrostatic discharge voltage (human body model) | $T_A$ = +25 °C conforming to ANSI/ESDA/JEDEC JS-001-2012 | 2 | 2000 | V |
| $V_{ESD(CDM)}$ | Electrostatic discharge voltage (charge device model) | $T_A$ = +25 °C conforming to ANSI/ESD S5.3.1-2009, LQFP100, LQFP144, LQFP176, LQFP208, WLCSP143, UFBGA176, TFBGA100 and TFBGA216 packages | C3 | 250 | |

1. Guaranteed by characterization results.

### Static latchup

Two complementary static tests are required on six parts to assess the latchup performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latchup standard.

**Table 55. Electrical sensitivities**

| Symbol | Parameter | Conditions | Class |
|---|---|---|---|
| LU | Static latch-up class | $T_A$ = +105 °C conforming to JESD78A | II level A |

## 6.3.16 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below $V_{SS}$ or above $V_{DD}$ (for standard, 3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

### Functional susceptibilty to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (>5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of –5 µA/+0 µA range), or other functional failure (for example reset, oscillator frequency deviation).

Negative induced leakage current is caused by negative injection and positive induced leakage current by positive injection.

The test results are given in Table 56.

**Table 56. I/O current injection susceptibility[1]**

<table>
<tr><th rowspan="2">Symbol</th><th rowspan="2">Description</th><th colspan="2">Functional susceptibility</th><th rowspan="2">Unit</th></tr>
<tr><th>Negative injection</th><th>Positive injection</th></tr>
<tr><td rowspan="5">$I_{INJ}$</td><td>Injected current on BOOT pin</td><td>– 0</td><td>NA</td><td rowspan="5">mA</td></tr>
<tr><td>Injected current on NRST pin</td><td>– 0</td><td>NA</td></tr>
<tr><td>Injected current on PA0, PC0 pins</td><td>– 0</td><td>NA</td></tr>
<tr><td>Injected current on any other FT pin</td><td>– 5</td><td>NA</td></tr>
<tr><td>Injected current on any other pins</td><td>– 5</td><td>+5</td></tr>
</table>

1. NA = not applicable.

*Note: It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.*

## 6.3.17 I/O port characteristics

### General input/output characteristics

Unless otherwise specified, the parameters given in Table 57: I/O static characteristics are derived from tests performed under the conditions summarized in Table 18. All I/Os are CMOS and TTL compliant.

*Note: For information on GPIO configuration, refer to the application note AN4899 “STM32 GPIO configuration for hardware settings and low-power consumption” available from the ST website www.st.com.*

**Table 57. I/O static characteristics**

<table>
<tr><th>Symbol</th><th>Parameter</th><th>Conditions</th><th>Min</th><th>Typ</th><th>Max</th><th>Unit</th></tr>
<tr><td rowspan="4">$V_{IL}$</td><td rowspan="2">FT, TTa and NRST I/O input low level voltage</td><td rowspan="2">$1.7\ V \leq V_{DD} \leq 3.6\ V$</td><td rowspan="2">-</td><td rowspan="2">-</td><td>$0.35V_{DD} - 0.04$[1]</td><td rowspan="4">V</td></tr>
<tr><td>$0.3V_{DD}$[2]</td></tr>
<tr><td rowspan="2">BOOT I/O input low level voltage</td><td>$1.75\ V \leq V_{DD} \leq 3.6\ V$, –40 °C$\leq T_A \leq$105 °C</td><td>-</td><td>-</td><td rowspan="2">$0.1V_{DD}+0.1$[1]</td></tr>
<tr><td>$1.7\ V \leq V_{DD} \leq 3.6\ V$, 0 °C$\leq T_A \leq$105 °C</td><td>-</td><td>-</td></tr>
</table>

**Table 57. I/O static characteristics (continued)**

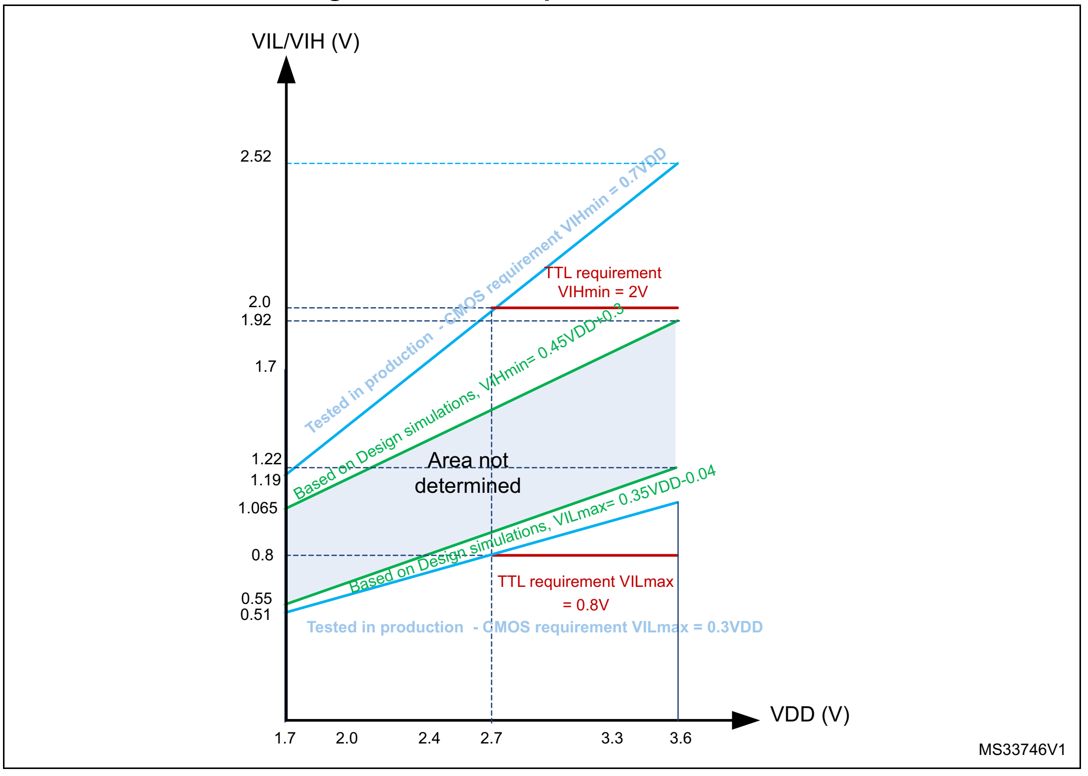
| Symbol | Parameter | | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | FT, TTa and NRST I/O input high level voltage[5] | | 1.7 V≤$V_{DD}$≤3.6 V | $0.45V_{DD}+0.3$[1] | - | - | V |
| | | | | $0.7V_{DD}$[2] | | | |
| | BOOT I/O input high level voltage | | 1.75 V≤$V_{DD}$ ≤3.6 V, –40 °C≤$T_A$ ≤105 °C | $0.17V_{DD}+0.7$[1] | - | - | |
| | | | 1.7 V≤$V_{DD}$ ≤3.6 V, 0 °C≤$T_A$ ≤105 °C | | | | |
| $V_{HYS}$ | FT, TTa and NRST I/O input hysteresis | | 1.7 V≤$V_{DD}$≤3.6 V | $10\%V_{DD}$[3] | - | - | V |
| | BOOT I/O input hysteresis | | 1.75 V≤$V_{DD}$ ≤3.6 V, –40 °C≤$T_A$ ≤105 °C | 0.1 | - | - | |
| | | | 1.7 V≤$V_{DD}$ ≤3.6 V, 0 °C≤$T_A$ ≤105 °C | | | | |
| $I_{lkg}$ | I/O input leakage current [4] | | $V_{SS}$ ≤$V_{IN}$ ≤$V_{DD}$ | - | - | ±1 | µA |
| | I/O FT input leakage current [5] | | $V_{IN}$ = 5 V | - | - | 3 | |
| $R_{PU}$ | Weak pull-up equivalent resistor[6] | All pins except for PA10/PB12 (OTG_FS_ID ,OTG_HS_ID ) | $V_{IN} = V_{SS}$ | 30 | 40 | 50 | kΩ |
| | | PA10/PB12 (OTG_FS_ID ,OTG_HS_ID ) | | 7 | 10 | 14 | |
| $R_{PD}$ | Weak pull-down equivalent resistor[7] | All pins except for PA10/PB12 (OTG_FS_ID ,OTG_HS_ID ) | $V_{IN} = V_{DD}$ | 30 | 40 | 50 | |
| | | PA10/PB12 (OTG_FS_ID ,OTG_HS_ID ) | | 7 | 10 | 14 | |
| $C_{IO}$[8] | I/O pin capacitance | | - | - | 5 | - | pF |

1. Guaranteed by design.
2. Tested in production.
3. With a minimum of 200 mV.
4. Leakage could be higher than the maximum value, if negative current is injected on adjacent pins, Refer to *Table 56: I/O current injection susceptibility*
5. To sustain a voltage higher than VDD +0.3 V, the internal pull-up/pull-down resistors must be disabled. Leakage could be higher than the maximum value, if negative current is injected on adjacent pins.Refer to *Table 56: I/O current injection susceptibility*
6. Pull-up resistors are designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimum (~10% order).

7. Pull-down resistors are designed with a true resistance in series with a switchable NMOS. This NMOS contribution to the series resistance is minimum (~10% order).
8. Hysteresis voltage between Schmitt trigger switching levels. Guaranteed by characterization results.

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements for FT I/Os is shown in *Figure 38*.

**Figure 38. FT I/O input characteristics**




## Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ±8 mA, and sink or source up to ±20 mA (with a relaxed $V_{OL}/V_{OH}$) except PC13, PC14, PC15 and PI8 which can sink or source up to ±3mA. When using the PC13 to PC15 and PI8 GPIOs in output mode, the speed should not exceed 2 MHz with a maximum load of 30 pF.

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 6.2*. In particular:

- The sum of the currents sourced by all the I/Os on $V_{DD,}$ plus the maximum Run consumption of the MCU sourced on $V_{DD,}$ cannot exceed the absolute maximum rating $\Sigma I_{VDD}$ (see *Table 16*).
- The sum of the currents sunk by all the I/Os on $V_{SS}$ plus the maximum Run consumption of the MCU sunk on $V_{SS}$ cannot exceed the absolute maximum rating $\Sigma I_{VSS}$ (see *Table 16*).

## Output voltage levels

Unless otherwise specified, the parameters given in *Table 58* are derived from tests performed under ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 18*. All I/Os are CMOS and TTL compliant.

**Table 58. Output voltage characteristics**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{OL}$(1) | Output low level voltage for an I/O pin | CMOS port(2)<br>$I_{IO}$ = +8 mA<br>$2.7\text{ V} \le V_{DD} \le 3.6\text{ V}$ | - | 0.4 | V |
| $V_{OH}$(3) | Output high level voltage for an I/O pin except PC14 | CMOS port(2)<br>$I_{IO}$ = -8 mA<br>$2.7\text{ V} \le V_{DD} \le 3.6\text{ V}$ | $V_{DD} - 0.4$ | - | |
| $V_{OH}$(3) | Output high level voltage for PC14 | CMOS port(2)<br>$I_{IO}$ = -2 mA<br>$2.7\text{ V} \le V_{DD} \le 3.6\text{ V}$ | $V_{DD} - 0.4$ | - | |
| $V_{OL}$(1) | Output low level voltage for an I/O pin | TTL port(2)<br>$I_{IO}$ =+8mA<br>$2.7\text{ V} \le V_{DD} \le 3.6\text{ V}$ | - | 0.4 | V |
| $V_{OH}$(3) | Output high level voltage for an I/O pin except PC14 | TTL port(2)<br>$I_{IO}$ =-8mA<br>$2.7\text{ V} \le V_{DD} \le 3.6\text{ V}$ | 2.4 | - | |
| $V_{OL}$(1) | Output low level voltage for an I/O pin | $I_{IO}$ = +20 mA<br>$2.7\text{ V} \le V_{DD} \le 3.6\text{ V}$ | - | 1.3(4) | V |
| $V_{OH}$(3) | Output high level voltage for an I/O pin except PC14 | $I_{IO}$ = -20 mA<br>$2.7\text{ V} \le V_{DD} \le 3.6\text{ V}$ | $V_{DD} - 1.3$(4) | - | |
| $V_{OL}$(1) | Output low level voltage for an I/O pin | $I_{IO}$ = +6 mA<br>$1.8\text{ V} \le V_{DD} \le 3.6\text{ V}$ | - | 0.4(4) | V |
| $V_{OH}$(3) | Output high level voltage for an I/O pin except PC14 | $I_{IO}$ = -6 mA<br>$1.8\text{ V} \le V_{DD} \le 3.6\text{ V}$ | $V_{DD} - 0.4$(4) | - | |
| $V_{OL}$(1) | Output low level voltage for an I/O pin | $I_{IO}$ = +4 mA<br>$1.7\text{ V} \le V_{DD} \le 3.6\text{V}$ | - | 0.4(5) | V |
| $V_{OH}$(3) | Output high level voltage for an I/O pin except PC14 | $I_{IO}$ = -4 mA<br>$1.7\text{ V} \le V_{DD} \le 3.6\text{V}$ | $V_{DD} - 0.4$(5) | - | |
| $V_{OH}$(3) | Output high level voltage for PC14 | $I_{IO}$ = -1 mA<br>$1.7\text{ V} \le V_{DD} \le 3.6\text{V}$ | $V_{DD} - 0.4$(5) | - | |

1. The $I_{IO}$ current sunk by the device must always respect the absolute maximum rating specified in *Table 16*. and the sum of $I_{IO}$ (I/O ports and control pins) must not exceed $I_{VSS}$.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. The $I_{IO}$ current sourced by the device must always respect the absolute maximum rating specified in *Table 16* and the sum of $I_{IO}$ (I/O ports and control pins) must not exceed $I_{VDD}$.
4. Based on characterization data.
5. Guaranteed by design.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 39* and *Table 59*, respectively.

Unless otherwise specified, the parameters given in *Table 59* are derived from tests performed under the ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 18*.

**Table 59. I/O AC characteristics(1)(2)**

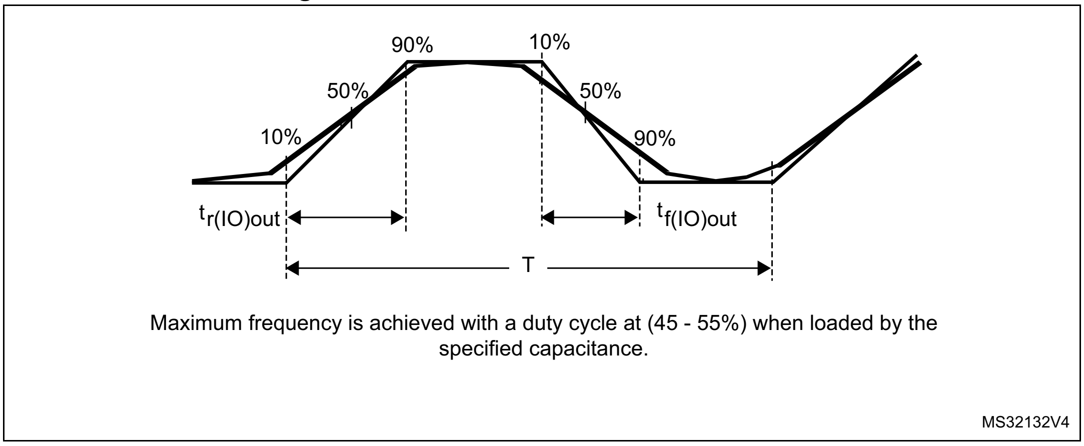
| OSPEEDRy [1:0] bit value(1) | Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| 00 | $f_{max(IO)out}$ | Maximum frequency(3) | $C_L$ = 50 pF, $V_{DD} \geq$ 2.7 V | - | - | 4 | MHz |
| | | | $C_L$ = 50 pF, $V_{DD} \geq$ 1.7 V | - | - | 2 | |
| | | | $C_L$ = 10 pF, $V_{DD} \geq$ 2.7 V | - | - | 8 | |
| | | | $C_L$ = 10 pF, $V_{DD} \geq$ 1.8 V | - | - | 4 | |
| | | | $C_L$ = 10 pF, $V_{DD} \geq$ 1.7 V | - | - | 3 | |
| | $t_{f(IO)out}$/ $t_{r(IO)out}$ | Output high to low level fall time and output low to high level rise time | $C_L$ = 50 pF, $V_{DD}$ = 1.7 V to 3.6 V | - | - | 100 | ns |
| 01 | $f_{max(IO)out}$ | Maximum frequency(3) | $C_L$ = 50 pF, $V_{DD} \geq$ 2.7 V | - | - | 25 | MHz |
| | | | $C_L$ = 50 pF, $V_{DD} \geq$ 1.8 V | - | - | 12.5 | |
| | | | $C_L$ = 50 pF, $V_{DD} \geq$ 1.7 V | - | - | 10 | |
| | | | $C_L$ = 10 pF, $V_{DD} \geq$ 2.7 V | - | - | 50 | |
| | | | $C_L$ = 10 pF, $V_{DD} \geq$ 1.8 V | - | - | 20 | |
| | | | $C_L$ = 10 pF, $V_{DD} \geq$ 1.7 V | - | - | 12.5 | |
| | $t_{f(IO)out}$/ $t_{r(IO)out}$ | Output high to low level fall time and output low to high level rise time | $C_L$ = 50 pF, $V_{DD} \geq$ 2.7 V | - | - | 10 | ns |
| | | | $C_L$ = 10 pF, $V_{DD} \geq$ 2.7 V | - | - | 6 | |
| | | | $C_L$ = 50 pF, $V_{DD} \geq$ 1.7 V | - | - | 20 | |
| | | | $C_L$ = 10 pF, $V_{DD} \geq$ 1.7 V | - | - | 10 | |
| 10 | $f_{max(IO)out}$ | Maximum frequency(3) | $C_L$ = 40 pF, $V_{DD} \geq$ 2.7 V | - | - | 50(4) | MHz |
| | | | $C_L$ = 10 pF, $V_{DD} \geq$ 2.7 V | - | - | 100(4) | |
| | | | $C_L$ = 40 pF, $V_{DD} \geq$ 1.7 V | - | - | 25 | |
| | | | $C_L$ = 10 pF, $V_{DD} \geq$ 1.8 V | - | - | 50 | |
| | | | $C_L$ = 10 pF, $V_{DD} \geq$ 1.7 V | - | - | 42.5 | |
| | $t_{f(IO)out}$/ $t_{r(IO)out}$ | Output high to low level fall time and output low to high level rise time | $C_L$ = 40 pF, $V_{DD} \geq$2.7 V | - | - | 6 | ns |
| | | | $C_L$ = 10 pF, $V_{DD} \geq$ 2.7 V | - | - | 4 | |
| | | | $C_L$ = 40 pF, $V_{DD} \geq$ 1.7 V | - | - | 10 | |
| | | | $C_L$ = 10 pF, $V_{DD} \geq$ 1.7 V | - | - | 6 | |

**Table 59. I/O AC characteristics(1)(2) (continued)**

| OSPEEDRy [1:0] bit value(1) | Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| 11 | $f_{max(IO)out}$ | Maximum frequency(3) | $C_L$ = 30 pF, $V_{DD} \geq 2.7$ V | - | - | 100(4) | MHz |
| | | | $C_L$ = 30 pF, $V_{DD} \geq 1.8$ V | - | - | 50 | |
| | | | $C_L$ = 30 pF, $V_{DD} \geq 1.7$ V | - | - | 42.5 | |
| | | | $C_L$ = 10 pF, $V_{DD} \geq 2.7$ V | - | - | 180(4) | |
| | | | $C_L$ = 10 pF, $V_{DD} \geq 1.8$ V | - | - | 100 | |
| | | | $C_L$ = 10 pF, $V_{DD} \geq 1.7$ V | - | - | 72.5 | |
| | $t_{f(IO)out}$/ $t_{r(IO)out}$ | Output high to low level fall time and output low to high level rise time | $C_L$ = 30 pF, $V_{DD} \geq 2.7$ V | - | - | 4 | ns |
| | | | $C_L$ = 30 pF, $V_{DD} \geq 1.8$ V | - | - | 6 | |
| | | | $C_L$ = 30 pF, $V_{DD} \geq 1.7$ V | - | - | 7 | |
| | | | $C_L$ = 10 pF, $V_{DD} \geq 2.7$ V | - | - | 2.5 | |
| | | | $C_L$ = 10 pF, $V_{DD} \geq 1.8$ V | - | - | 3.5 | |
| | | | $C_L$ = 10 pF, $V_{DD} \geq 1.7$ V | - | - | 4 | |
| - | tEXTIpw | Pulse width of external signals detected by the EXTI controller | - | 10 | - | - | ns |

1. Guaranteed by design.
2. The I/O speed is configured using the OSPEEDRy[1:0] bits. Refer to the STM32F75xxx and STM32F74xxx reference manual for a description of the GPIOx_SPEEDR GPIO port output speed register.
3. The maximum frequency is defined in *Figure 39*.
4. For maximum frequencies above 50 MHz and $V_{DD}$ > 2.4 V, the compensation cell should be used.

**Figure 39. I/O AC characteristics definition**



### 6.3.18 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, $R_{PU}$ (see *Table 57: I/O static characteristics*).

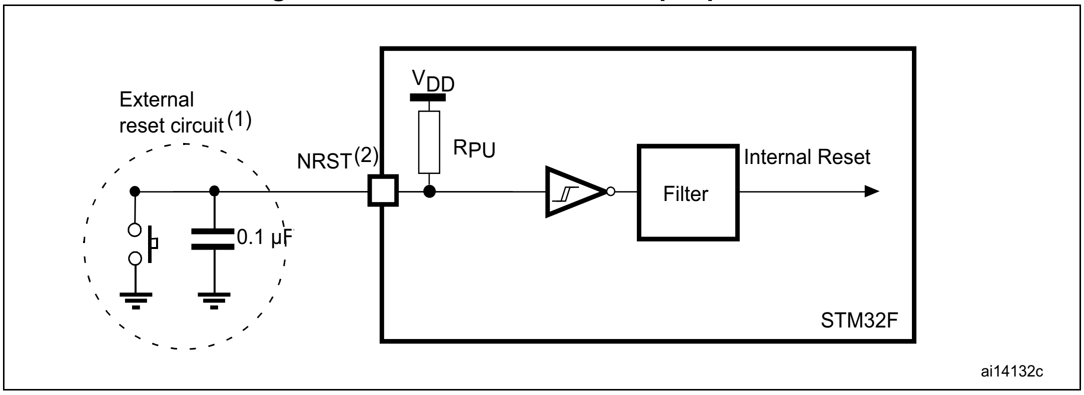
Unless otherwise specified, the parameters given in *Table 60* are derived from tests performed under the ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 18*.

**Table 60. NRST pin characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $R_{PU}$ | Weak pull-up equivalent resistor(1) | $V_{IN} = V_{SS}$ | 30 | 40 | 50 | kΩ |
| $V_{F(NRST)}$(2) | NRST Input filtered pulse | - | - | - | 100 | ns |
| $V_{NF(NRST)}$(2) | NRST Input not filtered pulse | $V_{DD}$ > 2.7 V | 300 | - | - | ns |
| $T_{NRST\_OUT}$ | Generated reset pulse duration | Internal Reset source | 20 | - | - | µs |

1. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).
2. Guaranteed by design.

**Figure 40. Recommended NRST pin protection**




1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 57*. Otherwise the reset is not taken into account by the device.

## 6.3.19 TIM timer characteristics

The parameters given in Table 61 are guaranteed by design.

Refer to Section 6.3.17: I/O port characteristics for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

**Table 61. TIMx characteristics(1)(2)**

| Symbol | Parameter | Conditions(3) | Min | Max | Unit |
|---|---|---|---|---|---|
| $t_{res(TIM)}$ | Timer resolution time | AHB/APBx prescaler=1 or 2 or 4, $f_{TIMxCLK}$ = 216 MHz | 1 | - | $t_{TIMxCLK}$ |
| | | AHB/APBx prescaler>4, $f_{TIMxCLK}$ = 108 MHz | 1 | - | $t_{TIMxCLK}$ |
| $f_{EXT}$ | Timer external clock frequency on CH1 to CH4 | $f_{TIMxCLK}$ = 216 MHz | 0 | $f_{TIMxCLK}/2$ | MHz |
| $Res_{TIM}$ | Timer resolution | | - | 16/32 | bit |
| $t_{MAX\_COUNT}$ | Maximum possible count with 32-bit counter | - | - | 65536 × 65536 | $t_{TIMxCLK}$ |

1. TIMx is used as a general term to refer to the TIM1 to TIM12 timers.
2. Guaranteed by design.
3. The maximum timer frequency on APB1 or APB2 is up to 216 MHz, by setting the TIMPRE bit in the RCC_DCKCFGR register, if APBx prescaler is 1 or 2 or 4, then TIMxCLK = HCLK, otherwise TIMxCLK = 4x PCLKx.

## 6.3.20 RTC characteristics

**Table 62. RTC characteristics**

| Symbol | Parameter | Conditions | Min | Max |
|---|---|---|---|---|
| - | $f_{PCLK1}$/RTCCLK frequency ratio | Any read/write operation from/to an RTC register | 4 | - |

## 6.3.21 12-bit ADC characteristics

Unless otherwise specified, the parameters given in Table 63 are derived from tests performed under the ambient temperature, $f_{PCLK2}$ frequency and $V_{DDA}$ supply voltage conditions summarized in Table 18.

**Table 63. ADC characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DDA}$ | Power supply | $V_{DDA} - V_{REF+} < 1.2$ V | 1.7(1) | - | 3.6 | V |
| $V_{REF+}$ | Positive reference voltage | | 1.7(1) | - | $V_{DDA}$ | V |
| $V_{REF-}$ | Negative reference voltage | - | - | 0 | - | V |

**Table 63. ADC characteristics (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{ADC}$ | ADC clock frequency | $V_{DDA}$ = 1.7(1) to 2.4 V | 0.6 | 15 | 18 | MHz |
| | | $V_{DDA}$ = 2.4 to 3.6 V | 0.6 | 30 | 36 | MHz |
| $f_{TRIG}$(2) | External trigger frequency | $f_{ADC}$ = 30 MHz, 12-bit resolution | - | - | 1764 | kHz |
| | | - | - | - | 17 | $1/f_{ADC}$ |
| $V_{AIN}$ | Conversion voltage range(3) | - | 0 ($V_{SSA}$ or $V_{REF-}$ tied to ground) | - | $V_{REF+}$ | V |
| $R_{AIN}$(2) | External input impedance | See *Equation 1* for details | - | - | 50 | kΩ |
| $R_{ADC}$(2)(4) | Sampling switch resistance | - | - | - | 6 | kΩ |
| $C_{ADC}$(2) | Internal sample and hold capacitor | - | - | 4 | 7 | pF |
| $t_{lat}$(2) | Injection trigger conversion latency | $f_{ADC}$ = 30 MHz | - | - | 0.100 | µs |
| | | | - | - | 3(5) | $1/f_{ADC}$ |
| $t_{latr}$(2) | Regular trigger conversion latency | $f_{ADC}$ = 30 MHz | - | - | 0.067 | µs |
| | | | - | - | 2(5) | $1/f_{ADC}$ |
| $t_S$(2) | Sampling time | $f_{ADC}$ = 30 MHz | 0.100 | - | 16 | µs |
| | | - | 3 | - | 480 | $1/f_{ADC}$ |
| $t_{STAB}$(2) | Power-up time | - | - | 2 | 3 | µs |
| $t_{CONV}$(2) | Total conversion time (including sampling time) | $f_{ADC}$ = 30 MHz 12-bit resolution | 0.50 | - | 16.40 | µs |
| | | $f_{ADC}$ = 30 MHz 10-bit resolution | 0.43 | - | 16.34 | µs |
| | | $f_{ADC}$ = 30 MHz 8-bit resolution | 0.37 | - | 16.27 | µs |
| | | $f_{ADC}$ = 30 MHz 6-bit resolution | 0.30 | - | 16.20 | µs |
| | | 9 to 492 ($t_S$ for sampling +n-bit resolution for successive approximation) | | | | $1/f_{ADC}$ |
| $f_S$(2) | Sampling rate ($f_{ADC}$ = 30 MHz, and $t_S$ = 3 ADC cycles) | 12-bit resolution Single ADC | - | - | 2 | Msps |
| | | 12-bit resolution Interleave Dual ADC mode | - | - | 3.75 | Msps |
| | | 12-bit resolution Interleave Triple ADC mode | - | - | 6 | Msps |

**Table 63. ADC characteristics (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{VREF+}$(2) | ADC $V_{REF}$ DC current consumption in conversion mode | - | - | 300 | 500 | µA |
| $I_{VDDA}$(2) | ADC $V_{DDA}$ DC current consumption in conversion mode | - | - | 1.6 | 1.8 | mA |

1. $V_{DDA}$ minimum value of 1.7 V is obtained with the use of an external power supply supervisor (refer to *Section 3.17.2: Internal reset OFF*).
2. Guaranteed by characterization results.
3. $V_{REF+}$ is internally connected to $V_{DDA}$ and $V_{REF-}$ is internally connected to $V_{SSA}$.
4. $R_{ADC}$ maximum value is given for $V_{DD}$=1.7 V, and minimum value for $V_{DD}$=3.3 V.
5. For external triggers, a delay of $1/f_{PCLK2}$ must be added to the latency specified in *Table 63*.

### Equation 1: $R_{AIN}$ max formula

$$R_{AIN} = \frac{(k - 0.5)}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The formula above (*Equation 1*) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. N = 12 (from 12-bit resolution) and k is the number of sampling periods defined in the ADC_SMPR1 register.

**Table 64. ADC static accuracy at $f_{ADC}$ = 18 MHz**

| Symbol | Parameter | Test conditions | Typ | Max(1) | Unit |
|---|---|---|---|---|---|
| ET | Total unadjusted error | $f_{ADC}$ =18 MHz<br>$V_{DDA}$ = 1.7 to 3.6 V<br>$V_{REF}$ = 1.7 to 3.6 V<br>$V_{DDA} - V_{REF}$ < 1.2 V | ±3 | ±4 | LSB |
| EO | Offset error | | ±2 | ±3 | |
| EG | Gain error | | ±1 | ±3 | |
| ED | Differential linearity error | | ±1 | ±2 | |
| EL | Integral linearity error | | ±2 | ±3 | |

1. Guaranteed by characterization results.

**Table 65. ADC static accuracy at $f_{ADC}$ = 30 MHz**

| Symbol | Parameter | Test conditions | Typ | Max(1) | Unit |
|---|---|---|---|---|---|
| ET | Total unadjusted error | $f_{ADC}$ = 30 MHz,<br>$R_{AIN}$ < 10 kΩ,<br>$V_{DDA}$ = 2.4 to 3.6 V,<br>$V_{REF}$ = 1.7 to 3.6 V,<br>$V_{DDA} - V_{REF}$ < 1.2 V | ±2 | ±5 | LSB |
| EO | Offset error | | ±1.5 | ±2.5 | |
| EG | Gain error | | ±1.5 | ±4 | |
| ED | Differential linearity error | | ±1 | ±2 | |
| EL | Integral linearity error | | ±1.5 | ±3 | |

1. Guaranteed by characterization results.

**Table 66. ADC static accuracy at $f_{ADC}$ = 36 MHz**

| Symbol | Parameter | Test conditions | Typ | Max[(1)] | Unit |
|---|---|---|---|---|---|
| ET | Total unadjusted error | $f_{ADC}$ =36 MHz, $V_{DDA}$ = 2.4 to 3.6 V, $V_{REF}$ = 1.7 to 3.6 V $V_{DDA} - V_{REF}$ < 1.2 V | ±4 | ±7 | LSB |
| EO | Offset error | | ±2 | ±3 | |
| EG | Gain error | | ±3 | ±6 | |
| ED | Differential linearity error | | ±2 | ±3 | |
| EL | Integral linearity error | | ±3 | ±6 | |

1. Guaranteed by characterization results.

**Table 67. ADC dynamic accuracy at $f_{ADC}$ = 18 MHz - limited test conditions[(1)]**

| Symbol | Parameter | Test conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| ENOB | Effective number of bits | $f_{ADC}$ =18 MHz $V_{DDA} = V_{REF+}$= 1.7 V Input Frequency = 20 KHz Temperature = 25 °C | 10.3 | 10.4 | - | bits |
| SINAD | Signal-to-noise and distortion ratio | | 64 | 64.2 | - | dB |
| SNR | Signal-to-noise ratio | | 64 | 65 | - | |
| THD | Total harmonic distortion | | − 67 | − 72 | - | |

1. Guaranteed by characterization results.

**Table 68. ADC dynamic accuracy at $f_{ADC}$ = 36 MHz - limited test conditions[(1)]**

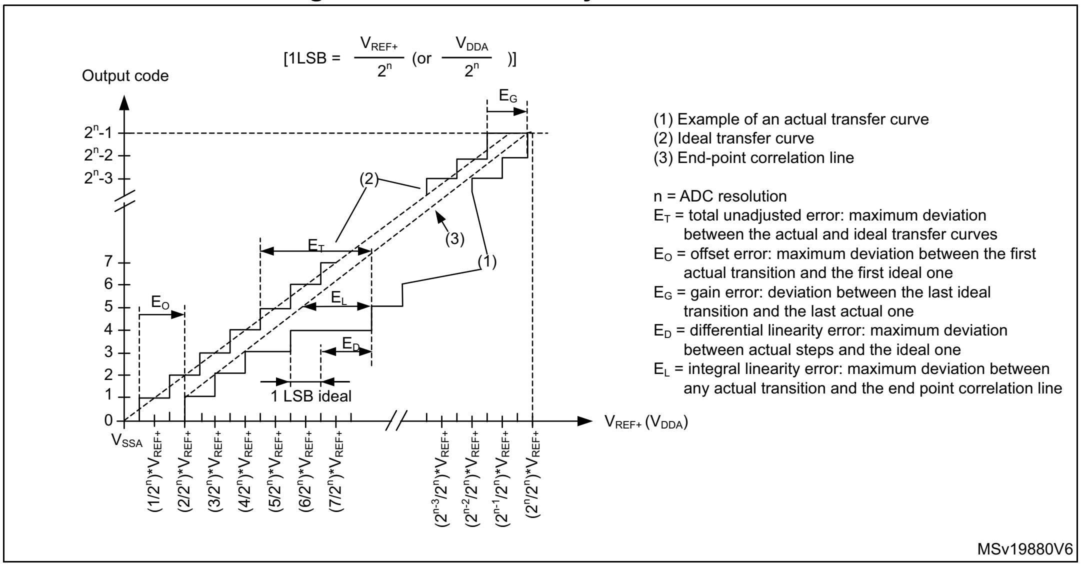
| Symbol | Parameter | Test conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| ENOB | Effective number of bits | $f_{ADC}$ =36 MHz $V_{DDA} = V_{REF+}$ = 3.3 V Input Frequency = 20 KHz Temperature = 25 °C | 10.6 | 10.8 | - | bits |
| SINAD | Signal-to noise and distortion ratio | | 66 | 67 | - | dB |
| SNR | Signal-to noise ratio | | 64 | 68 | - | |
| THD | Total harmonic distortion | | − 70 | − 72 | - | |

1. Guaranteed by characterization results.

Note: ADC accuracy vs. negative injection current: injecting a negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.

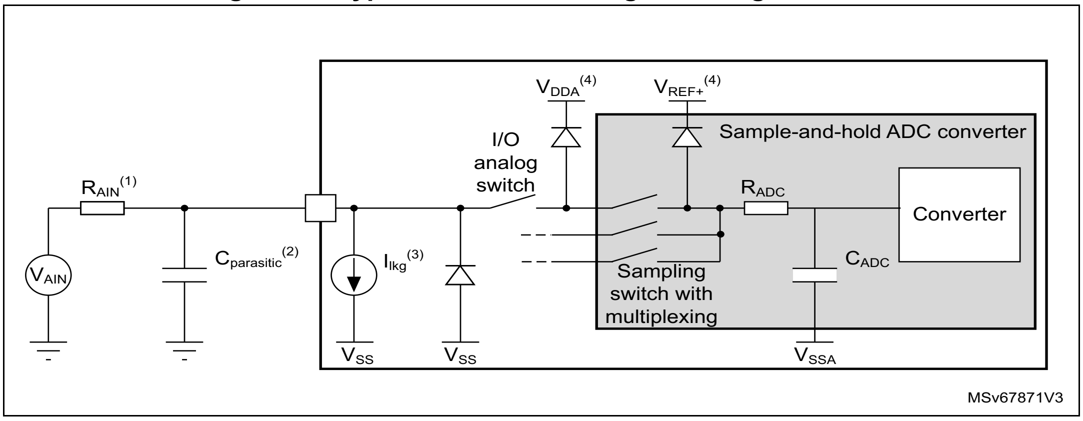
Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 6.3.17* does not affect the ADC accuracy.

**Figure 41. ADC accuracy characteristics**




1. See also *Table 65*.
2. Example of an actual transfer curve.
3. Ideal transfer curve.
4. End point correlation line.
5. $E_T$ = Total Unadjusted Error: maximum deviation between the actual and the ideal transfer curves.
   EO = Offset Error: deviation between the first actual transition and the first ideal one.
   EG = Gain Error: deviation between the last ideal transition and the last actual one.
   ED = Differential Linearity Error: maximum deviation between actual steps and the ideal one.
   EL = Integral Linearity Error: maximum deviation between any actual transition and the end point correlation line.

**Figure 42. Typical connection diagram using the ADC**

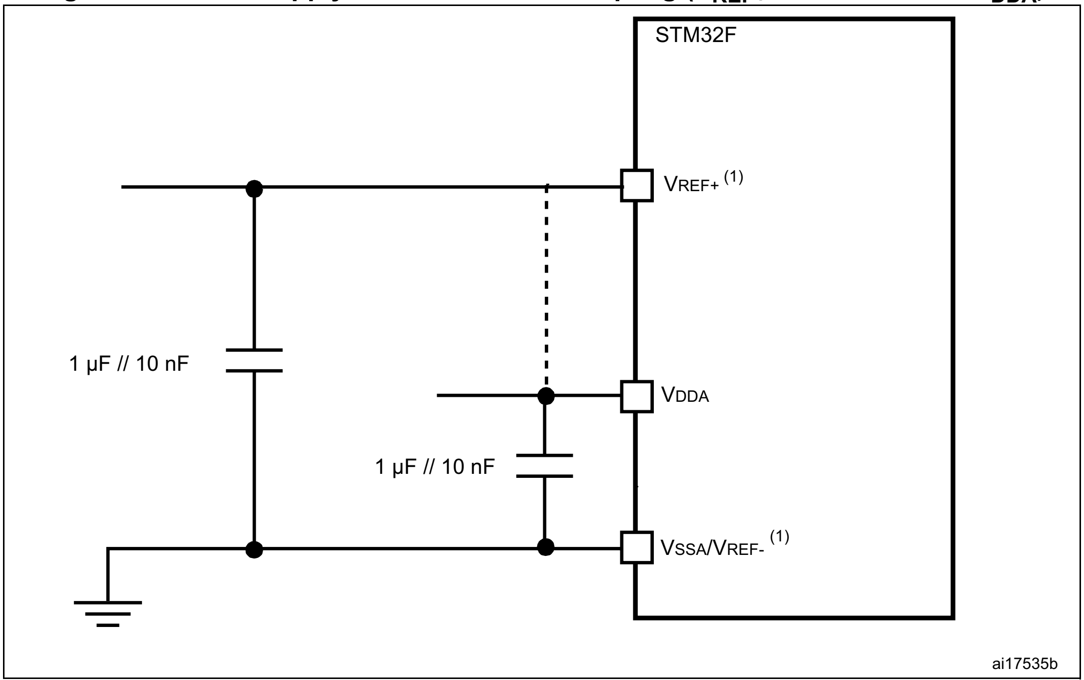



1. Refer to *Table 63* for the values of $R_{AIN}$, $R_{ADC}$ and $C_{ADC}$.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 5 pF). A high $C_{parasitic}$ value downgrades conversion accuracy. To remedy this, $f_{ADC}$ should be reduced.
3. Refer to *Table 57: I/O static characteristics* for the value of $I_{lkg}$.
4. Refer to *Figure 22: Power supply scheme*.

### General PCB design guidelines

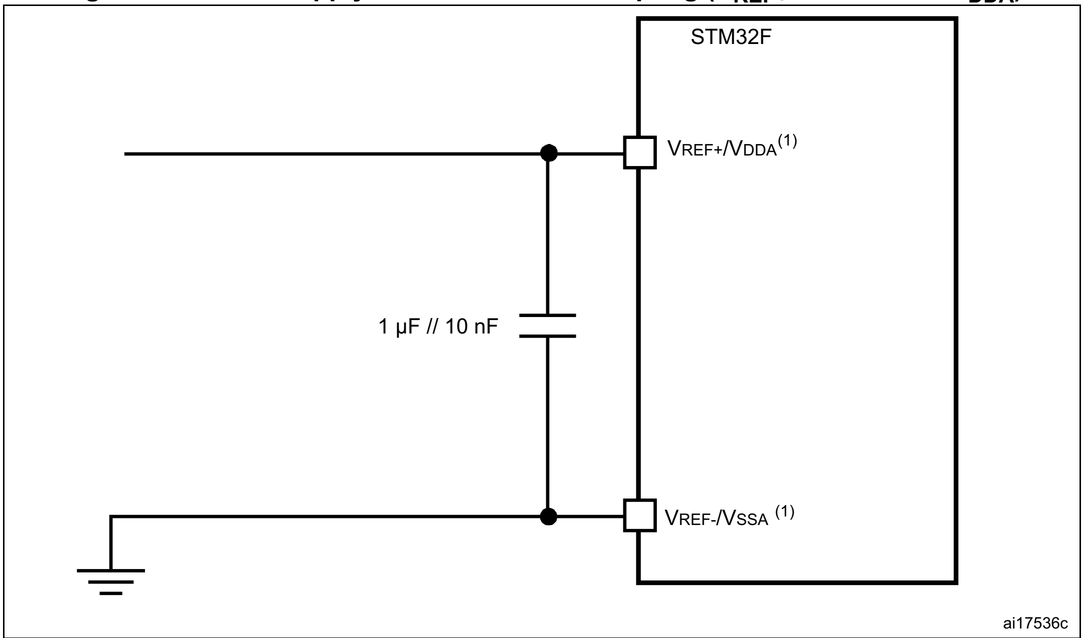
Power supply decoupling should be performed as shown in *Figure 43* or *Figure 44*, depending on whether $V_{REF+}$ is connected to $V_{DDA}$ or not. The 10 nF capacitors should be ceramic (good quality). They should be placed them as close as possible to the chip.

**Figure 43. Power supply and reference decoupling ($V_{REF+}$ not connected to $V_{DDA}$)**




1. $V_{REF+}$ input is available on all the packages except TFBGA100 whereas the $V_{REF-}$ is available only on UFBGA176 and TFBGA216. When $V_{REF-}$ is not available, it is internally connected to $V_{DDA}$ and $V_{SSA}$.

**Figure 44. Power supply and reference decoupling ($V_{REF+}$ connected to $V_{DDA}$)**




1. $V_{REF+}$ input is available on all the packages except TFBGA100, whereas the $V_{REF-}$ is available only on UFBGA176 and TFBGA216. When $V_{REF-}$ is not available, it is internally connected to $V_{DDA}$ and $V_{SSA}$.

## 6.3.22 Temperature sensor characteristics

**Table 69. Temperature sensor characteristics**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_L$(1) | $V_{SENSE}$ linearity with temperature | - | ±1 | ±2 | °C |
| Avg_Slope(1) | Average slope | - | 2.5 | - | mV/°C |
| $V_{25}$(1) | Voltage at 25 °C | - | 0.76 | - | V |
| $t_{START}$(2) | Startup time | - | 6 | 10 | µs |
| $T_{S\_temp}$(2) | ADC sampling time when reading the temperature (1 °C accuracy) | 10 | - | - | µs |

1. Guaranteed by characterization results.
2. Guaranteed by design.

**Table 70. Temperature sensor calibration values**

| Symbol | Parameter | Memory address |
|---|---|---|
| TS_CAL1 | TS ADC raw data acquired at temperature of 30 °C, $V_{DDA}$= 3.3 V | 0x1FF0 F44C - 0x1FF0 F44D |
| TS_CAL2 | TS ADC raw data acquired at temperature of 110 °C, $V_{DDA}$= 3.3 V | 0x1FF0 F44E - 0x1FF0 F44F |

## 6.3.23 $V_{BAT}$ monitoring characteristics

**Table 71. $V_{BAT}$ monitoring characteristics**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| R | Resistor bridge for $V_{BAT}$ | - | 50 | - | KΩ |
| Q | Ratio on $V_{BAT}$ measurement | - | 4 | - | - |
| Er(1) | Error on Q | –1 | - | +1 | % |
| $T_{S\_vbat}$(2)(2) | ADC sampling time when reading the $V_{BAT}$ 1 mV accuracy | 5 | - | - | µs |

1. Guaranteed by design.
2. Shortest sampling time can be determined in the application by multiple iterations.

## 6.3.24 Reference voltage

The parameters given in *Table 72* are derived from tests performed under ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 18*.

**Table 72. internal reference voltage**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{REFINT}$ | Internal reference voltage | –40 °C < $T_A$ < +105 °C | 1.18 | 1.21 | 1.24 | V |
| $T_{S\_vrefint}$(1) | ADC sampling time when reading the internal reference voltage | - | 10 | - | - | µs |
| $V_{RERINT\_s}$(2) | Internal reference voltage spread over the temperature range | $V_{DD}$ = 3V ± 10mV | - | 3 | 5 | mV |

**Table 72. internal reference voltage (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $T_{Coeff}$(2) | Temperature coefficient | - | - | 30 | 50 | ppm/°C |
| $t_{START}$(2) | Startup time | - | - | 6 | 10 | µs |

1. Shortest sampling time can be determined in the application by multiple iterations.
2. Guaranteed by design.

**Table 73. Internal reference voltage calibration values**

| Symbol | Parameter | Memory address |
|---|---|---|
| $V_{REFIN\_CAL}$ | Raw data acquired at temperature of 30 °C $V_{DDA}$ = 3.3 V | 0x1FF0 F44A - 0x1FF0 F44B |

## 6.3.25 DAC electrical characteristics

**Table 74. DAC characteristics**

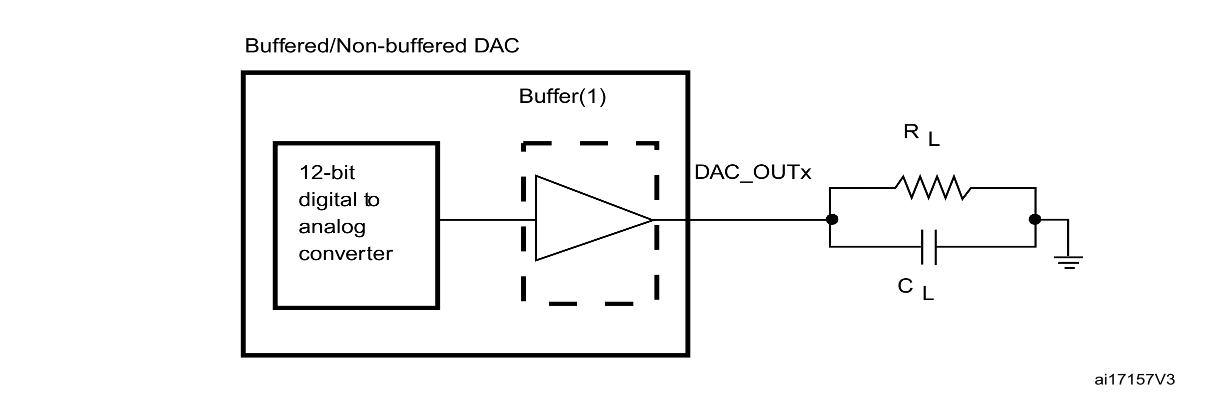
| Symbol | Parameter | Min | Typ | Max | Unit | Comments |
|---|---|---|---|---|---|---|
| $V_{DDA}$ | Analog supply voltage | 1.7(1) | - | 3.6 | V | - |
| $V_{REF+}$ | Reference supply voltage | 1.7(1) | - | 3.6 | V | $V_{REF+} \leq V_{DDA}$ |
| $V_{SSA}$ | Ground | 0 | - | 0 | V | - |
| $R_{LOAD}$(2) | Resistive load with buffer ON | 5 | - | - | kΩ | - |
| $R_O$(2) | Impedance output with buffer OFF | - | - | 15 | kΩ | When the buffer is OFF, the Minimum resistive load between DAC_OUT and $V_{SS}$ to have a 1% accuracy is 1.5 MΩ |
| $C_{LOAD}$(2) | Capacitive load | - | - | 50 | pF | Maximum capacitive load at DAC_OUT pin (when the buffer is ON). |
| DAC_OUT min(2) | Lower DAC_OUT voltage with buffer ON | 0.2 | - | - | V | It gives the maximum output excursion of the DAC.<br>It corresponds to 12-bit input code (0x0E0) to (0xF1C) at $V_{REF+}$ = 3.6 V and (0x1C7) to (0xE38) at $V_{REF+}$ = 1.7 V |
| DAC_OUT max(2) | Higher DAC_OUT voltage with buffer ON | - | - | $V_{DDA}$ – 0.2 | V | |
| DAC_OUT min(2) | Lower DAC_OUT voltage with buffer OFF | - | 0.5 | - | mV | It gives the maximum output excursion of the DAC. |
| DAC_OUT max(2) | Higher DAC_OUT voltage with buffer OFF | - | - | $V_{REF+}$ – 1LSB | V | |
| $I_{VREF+}$(4) | DAC DC $V_{REF}$ current consumption in quiescent mode (Standby mode) | - | 170 | 240 | µA | With no load, worst code (0x800) at $V_{REF+}$ = 3.6 V in terms of DC consumption on the inputs |
| | | - | 50 | 75 | | With no load, worst code (0xF1C) at $V_{REF+}$ = 3.6 V in terms of DC consumption on the inputs |

**Table 74. DAC characteristics (continued)**

| Symbol | Parameter | Min | Typ | Max | Unit | Comments |
|---|---|---|---|---|---|---|
| $I_{DDA}$(4) | DAC DC $V_{DDA}$ current consumption in quiescent mode(3) | - | 280 | 380 | µA | With no load, middle code (0x800) on the inputs |
| | | - | 475 | 625 | µA | With no load, worst code (0xF1C) at $V_{REF+}$ = 3.6 V in terms of DC consumption on the inputs |
| DNL(4) | Differential non linearity Difference between two consecutive code-1LSB) | - | - | ±0.5 | LSB | Given for the DAC in 10-bit configuration. |
| | | - | - | ±2 | LSB | Given for the DAC in 12-bit configuration. |
| INL(4) | Integral non linearity (difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 1023) | - | - | ±1 | LSB | Given for the DAC in 10-bit configuration. |
| | | - | - | ±4 | LSB | Given for the DAC in 12-bit configuration. |
| Offset(4) | Offset error (difference between measured value at Code (0x800) and the ideal value = $V_{REF+}/2$) | - | - | ±10 | mV | Given for the DAC in 12-bit configuration |
| | | - | - | ±3 | LSB | Given for the DAC in 10-bit at $V_{REF+}$ = 3.6 V |
| | | - | - | ±12 | LSB | Given for the DAC in 12-bit at $V_{REF+}$ = 3.6 V |
| Gain error(4) | Gain error | - | - | ±0.5 | % | Given for the DAC in 12-bit configuration |
| $t_{SETTLING}$(4) | Settling time (full scale: for a 10-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value ±4LSB | - | 3 | 6 | µs | $C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ |
| THD(4) | Total Harmonic Distortion Buffer ON | - | - | - | dB | $C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ |
| Update rate(2) | Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1LSB) | - | - | 1 | MS/s | $C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ |
| $t_{WAKEUP}$(4) | Wake-up time from off state (Setting the ENx bit in the DAC Control register) | - | 6.5 | 10 | µs | $C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ input code between lowest and highest possible ones. |
| PSRR+ (2) | Power supply rejection ratio (to $V_{DDA}$) (static DC measurement) | - | –67 | –40 | dB | No $R_{LOAD}$, $C_{LOAD}$ = 50 pF |

1. $V_{DDA}$ minimum value of 1.7 V is obtained with the use of an external power supply supervisor (refer to *Section 3.17.2: Internal reset OFF*).
2. Guaranteed by design.
3. The quiescent mode corresponds to a state where the DAC maintains a stable output level to ensure that no dynamic consumption occurs.
4. Guaranteed by characterization results.

**Figure 45. 12-bit buffered /non-buffered DAC**




1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

## 6.3.26 Communications interfaces

### I$^2$C interface characteristics

The I$^2$C interface meets the timings requirements of the I$^2$C-bus specification and user manual rev. 03 for:

- Standard-mode (Sm): with a bit rate up to 100 kbit/s
- Fast-mode (Fm): with a bit rate up to 400 kbit/s.
- Fast-mode Plus (Fm+): with a bit rate up to 1Mbit/s.

The I$^2$C timings requirements are guaranteed by design when the I2C peripheral is properly configured (refer to RM0385 reference manual) and when the I2CCLK frequency is greater than the minimum shown in the table below:

**Table 75. Minimum I2CCLK frequency in all I2C modes**

| Symbol | Parameter | Condition | | Min | Unit |
|---|---|---|---|---|---|
| f(I2CCLK) | I2CCLK frequency | Standard-mode | | 2 | MHz |
| | | Fast-mode | Analog Filter ON DNF=0 | 10 | |
| | | | Analog Filter OFF DNF=1 | 9 | |
| | | Fast-mode Plus | Analog Filter ON DNF=0 | 22.5 | |
| | | | Analog Filter OFF DNF=1 | 16 | |

The SDA and SCL I/O requirements are met with the following restrictions: the SDA and SCL I/O pins are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and $V_{DD}$ is disabled, but is still present.

The 20mA output drive requirement in Fast-mode Plus is not supported. This limits the maximum load Cload supported in Fm+, which is given by these formulas:

- $Tr(SDA/SCL)=0.8473xR_pxC_{load}$
- $R_p(min)= (VDD-V_{OL}(max))/I_{OL}(max)$

Where Rp is the I2C lines pull-up. Refer to *Section 6.3.17: I/O port characteristics* for the I2C I/Os characteristics.

All $I^2C$ SDA and SCL I/Os embed an analog filter. Refer to the table below for the analog filter characteristics:

**Table 76. I2C analog filter characteristics[(1)]**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{AF}$ | Maximum pulse width of spikes that are suppressed by the analog filter | 50[(2)] | 150[(3)] | ns |

1. Guaranteed by characterization results.
2. Spikes with widths below $t_{AF(min)}$ are filtered.
3. Spikes with widths above $t_{AF(max)}$ are not filtered

## SPI interface characteristics

Unless otherwise specified, the parameters given in *Table 77* for the SPI interface are derived from tests performed under the ambient temperature, $f_{PCLKx}$ frequency and $V_{DD}$ supply voltage conditions summarized in *Table 18*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$

Refer to *Section 6.3.17: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI).

**Table 77. SPI dynamic characteristics(1)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{SCK}$<br>$1/t_{c(SCK)}$ | SPI clock frequency | Master mode<br>SPI1,4,5,6<br>2.7≤VDD≤3.6 | - | - | 54(2) | MHz |
| | | Master mode<br>SPI1,4,5,6<br>1.71≤VDD≤3.6 | | | 27 | |
| | | Master transmitter mode<br>SPI1,4,5,6<br>1.71≤VDD≤3.6 | | | 54 | |
| | | Slave receiver mode<br>SPI1,4,5,6<br>1.71≤VDD≤3.6 | | | 54 | |
| | | Slave mode transmitter/full duplex<br>SPI1,4,5,6<br>2.7≤VDD≤3.6 | | | 50(3) | |
| | | Slave mode transmitter/full duplex<br>SPI1,4,5,6<br>1.71≤VDD≤3.6 | | | 38(3) | |
| | | Master & Slave mode<br>SPI2,3<br>1.71≤VDD≤3.6 | | | 27 | |
| tsu(NSS) | NSS setup time | Slave mode, SPI presc = 2 | 4*Tpclk | - | - | ns |
| th(NSS) | NSS hold time | Slave mode, SPI presc = 2 | 2*Tpclk | - | - | |
| tw(SCKH)<br>tw(SCKL) | SCK high and low time | Master mode | Tpclk-2 | Tpclk | Tpclk+2 | |

**Table 77. SPI dynamic characteristics(1) (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| tsu(MI) | Data input setup time | Master mode | 5.5 | - | - | ns |
| tsu(SI) | | Slave mode | 4 | - | - | |
| th(MI) | Data input hold time | Master mode | 4 | - | - | |
| th(SI) | | Slave mode | 2 | - | - | |
| ta(SO) | Data output access time | Slave mode | 7 | - | 21 | |
| tdis(SO) | Data output disable time | Slave mode | 5 | - | 12 | |
| tv(SO) | Data output valid time | Slave mode 2.7≤VDD≤3.6V | - | 6.5 | 10 | |
| | | Slave mode 1.71≤VDD≤3.6V | - | 6.5 | 13 | |
| tv(MO) | | Master mode | - | 2 | 4 | |
| th(SO) | Data output hold time | Slave mode 1.71≤VDD≤3.6V | 5.5 | - | - | |
| th(MO) | | Master mode | 0 | - | - | |

1. Guaranteed by characterization results.
2. Excepting SPI1 with SCK IO pin mapped on PA5. In this configuration, Maximum achievable frequency is 40MHz.
3. Maximum Frequency of Slave Transmitter is determined by sum of Tv(SO) and Tsu(MI) intervals which has to fit into SCK level phase preceding the SCK sampling edge.This value can be achieved when it communicates with a Master having Tsu(MI)=0 while signal Duty(SCK)=50%.

**Figure 46. SPI timing diagram - slave mode and CPHA = 0**

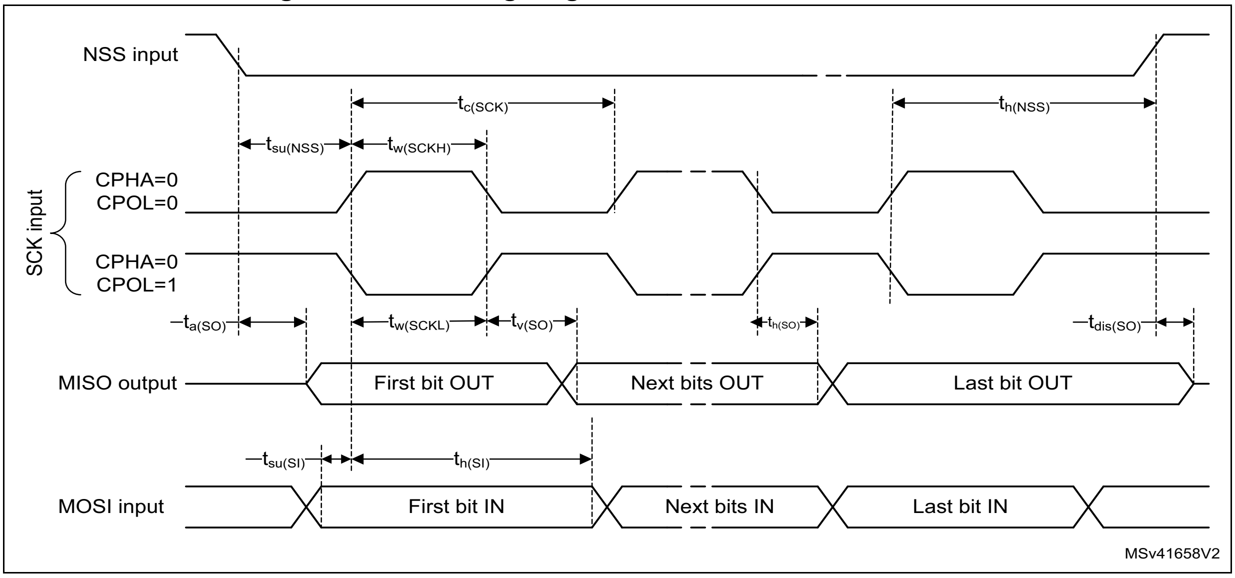


Figure 47. SPI timing diagram - slave mode and CPHA = 1

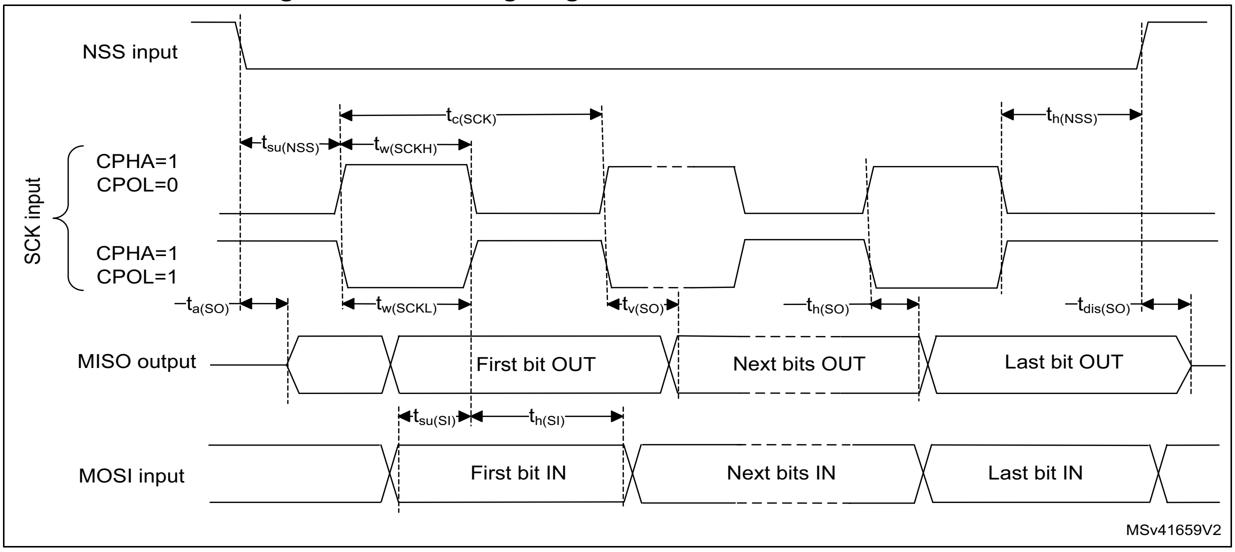
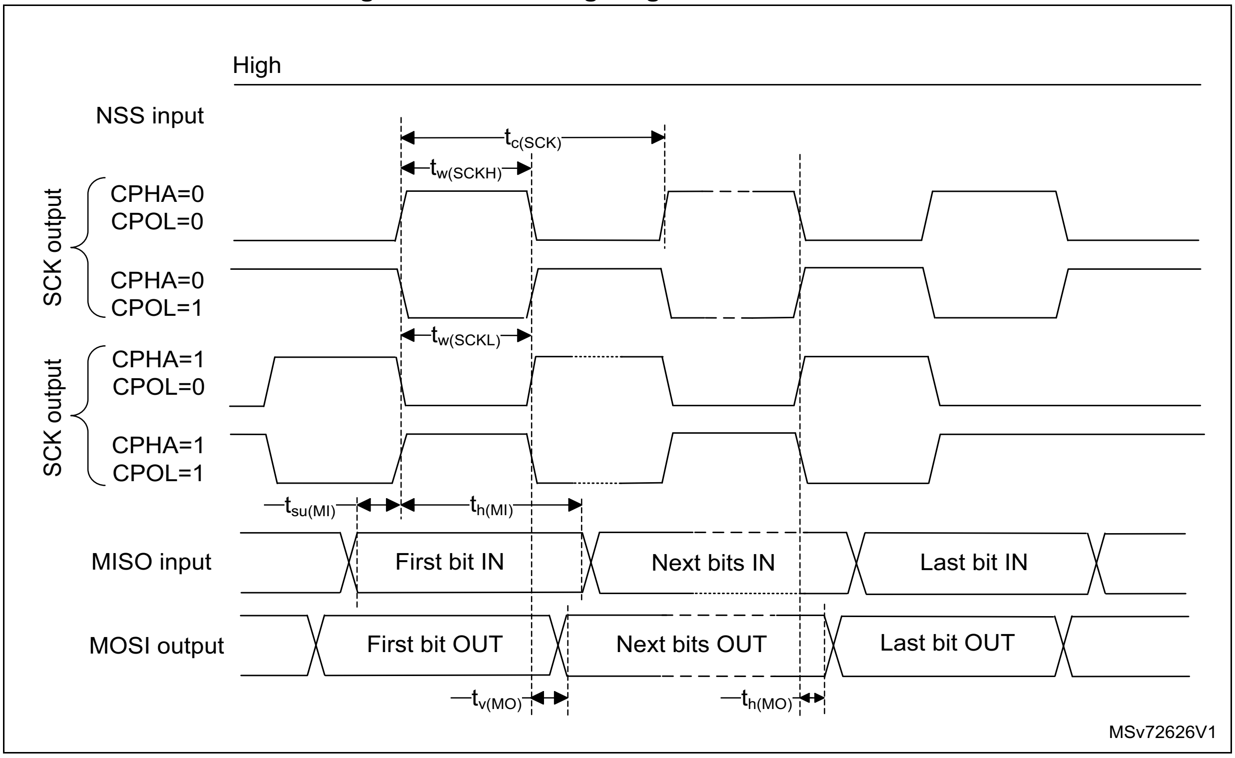



Figure 48. SPI timing diagram - master mode




## $I^2S$ interface characteristics

Unless otherwise specified, the parameters given in *Table 78* for the $I^2S$ interface are derived from tests performed under the ambient temperature, $f_{PCLKx}$ frequency and $V_{DD}$ supply voltage conditions summarized in *Table 18*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$

Refer to *Section 6.3.17: I/O port characteristics* for more details on the input/output alternate function characteristics (CK, SD, WS).

**Table 78. $I^2S$ dynamic characteristics[1]**

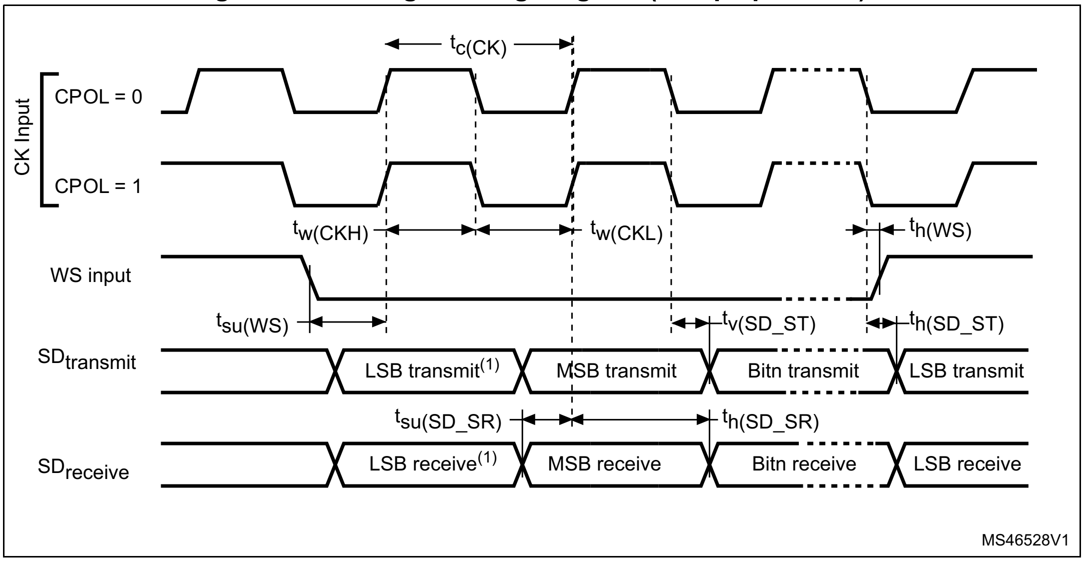
| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $f_{MCK}$ | I2S Main clock output | - | 256x8K | 256xFs[2] | MHz |
| $f_{CK}$ | I2S clock frequency | Master data: 32 bits | - | 64xFs | MHz |
| | | Slave data: 32 bits | - | 64xFs | |
| $D_{CK}$ | I2S clock frequency duty cycle | Slave receiver | 30 | 70 | % |
| $t_{v(WS)}$ | WS valid time | Master mode | - | 5 | ns |
| $t_{h(WS)}$ | WS hold time | Master mode | 0 | - | |
| $t_{su(WS)}$ | WS setup time | Slave mode | 5 | - | ns |
| | | Slave mode<br>PCM short pulse mode[3] | 3 | - | |
| $t_{h(WS)}$ | WS hold time | Slave mode | 0 | - | |
| | | Slave mode<br>PCM short pulse mode[3] | 2 | - | |
| $t_{su(SD\_MR)}$ | Data input setup time | Master receiver | 5 | - | |
| $t_{su(SD\_SR)}$ | | Slave receiver | 1 | - | |
| $t_{h(SD\_MR)}$ | Data input hold time | Master receiver | 5 | - | |
| $t_{h(SD\_SR)}$ | | Slave receiver | 1.5 | - | |
| $t_{v(SD\_ST)}$ | Data output valid time | Slave transmitter (after enable edge) | - | 16 | |
| $t_{v(SD\_MT)}$ | | Master transmitter (after enable edge) | - | 3.5 | |
| $t_{h(SD\_ST)}$ | Data output hold time | Slave transmitter (after enable edge) | 5 | - | |
| $t_{h(SD\_MT)}$ | | Master transmitter (after enable edge) | 0 | - | |

1. Guaranteed by characterization results.
2. The maximum value of 256xFs is 45 MHz (APB1 maximum frequency).
3. Measurement done with respect to I2S_CK rising edge.

*Note: Refer to RM0385 reference manual I2S section for more details on the sampling frequency ($F_S$).*

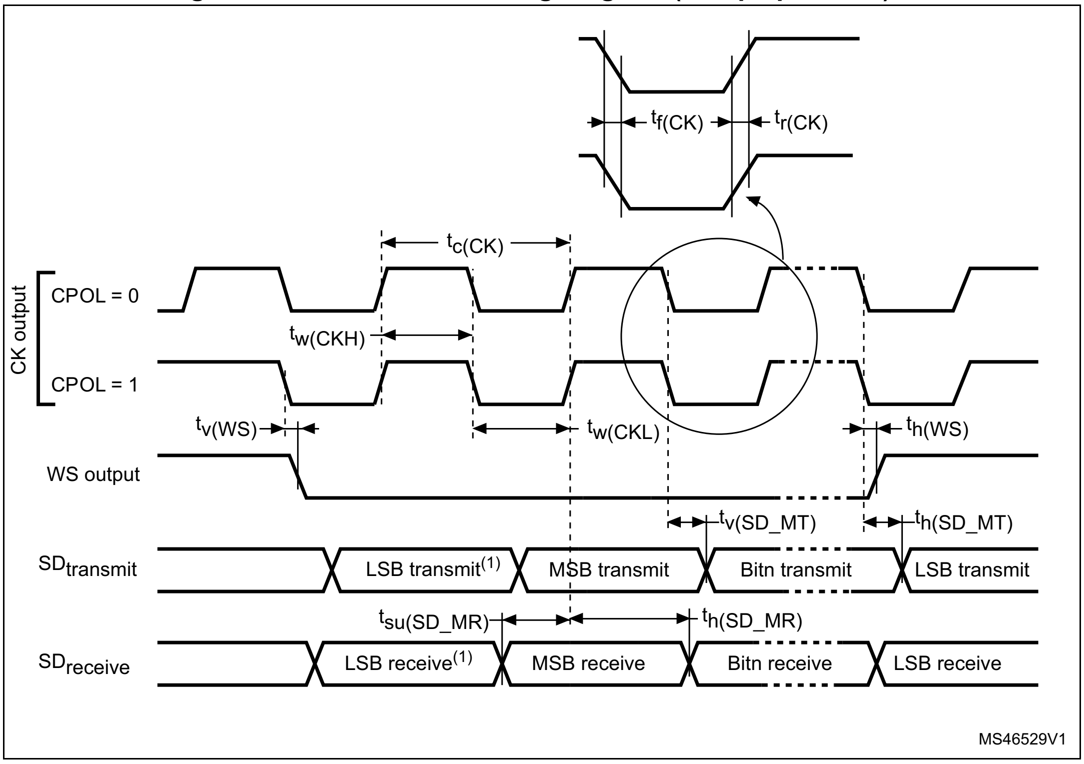
*$f_{MCK}$, $f_{CK}$, and $D_{CK}$ values reflect only the digital peripheral behavior. The values of these parameters might be slightly impacted by the source clock precision. $D_{CK}$ depends mainly on the value of ODD bit. The digital contribution leads to a minimum value of (I2SDIV/(2*I2SDIV+ODD) and a maximum value of (I2SDIV+ODD)/(2*I2SDIV+ODD). $F_S$ maximum value is supported for each mode/condition.*

**Figure 49. I²S target timing diagram (Philips protocol)[(1)]**




1. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

**Figure 50. I²S controller timing diagram (Philips protocol)[(1)]**




1. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

### SAI characteristics

Unless otherwise specified, the parameters given in *Table 79* for SAI are derived from tests performed under the ambient temperature, $f_{PCLKx}$ frequency and VDD supply voltage conditions summarized in *Table 18*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C=30 pF
- Measurement points are performed at CMOS levels: $0.5V_{DD}$

Refer to *Section 6.3.17: I/O port characteristics* for more details on the input/output alternate function characteristics (SCK,SD,WS).

**Table 79. SAI characteristics[1]**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $f_{MCKL}$ | SAI Main clock output | - | 256 x 8K | 256xFs[2] | MHz |
| $F_{SCK}$ | SAI clock frequency | Master data: 32 bits | - | 128xFs | MHz |
| | | Slave data: 32 bits | - | 128xFs | |
| $D_{SCK}$ | SAI clock frequency duty cycle | Slave receiver | 30 | 70 | % |
| $t_{v(FS)}$ | FS valid time | Master mode | 8 | 22 | ns |
| $t_{su(FS)}$ | FS setup time | Slave mode | 2 | - | |
| $t_{h(FS)}$ | FS hold time | Master mode | 8 | - | |
| | | Slave mode | 0 | - | |
| $t_{su(SD\_MR)}$ | Data input setup time | Master receiver | 5 | - | |
| $t_{su(SD\_SR)}$ | | Slave receiver | 3 | - | |
| $t_{h(SD\_MR)}$ | Data input hold time | Master receiver | 0 | - | |
| $t_{h(SD\_SR)}$ | | Slave receiver | 6 | - | |
| $t_{v(SD\_ST)}$ $t_{h(SD\_ST)}$ | Data output valid time | Slave transmitter (after enable edge) | - | 15 | |
| $t_{v(SD\_MT)}$ | | Master transmitter (after enable edge) | - | 20 | |
| $t_{h(SD\_MT)}$ | Data output hold time | Master transmitter (after enable edge) | 7 | - | |

1. Guaranteed by characterization results.
2. 256xFs maximum corresponds to 45 MHz (APB2 xaximum frequency)

**Figure 51. SAI master timing waveforms**

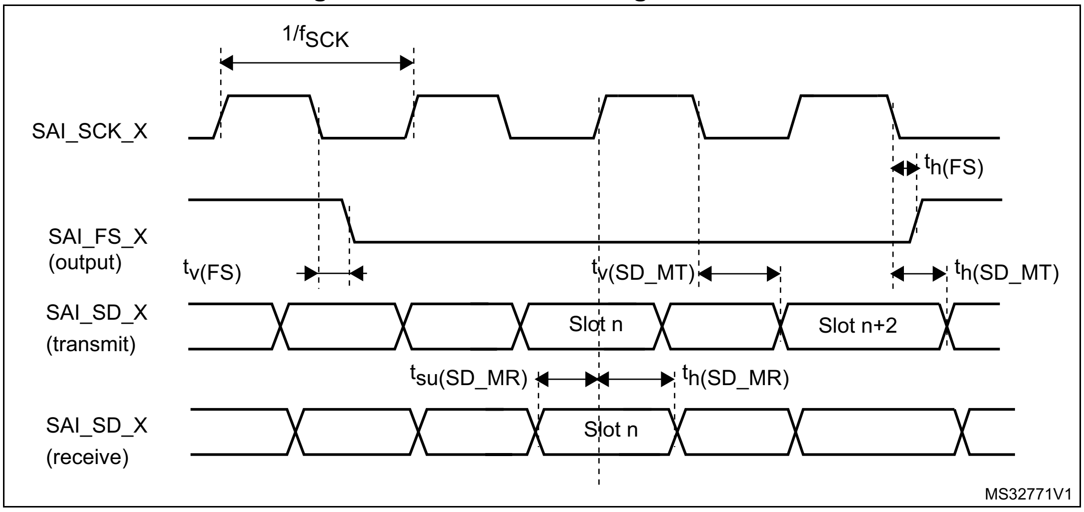
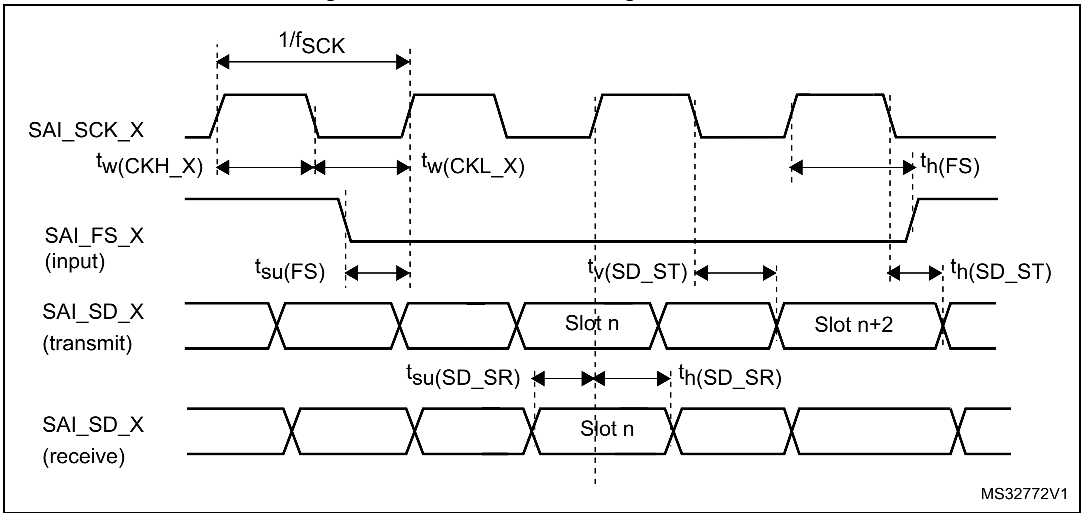



**Figure 52. SAI slave timing waveforms**



### USB OTG full speed (FS) characteristics

This interface is present in both the USB OTG HS and USB OTG FS controllers.

**Table 80. USB OTG full speed startup time**

| Symbol | Parameter | Max | Unit |
|---|---|---|---|
| $t_{STARTUP}$(1) | USB OTG full speed transceiver startup time | 1 | µs |

1. Guaranteed by design.

**Table 81. USB OTG full speed DC electrical characteristics**

<table>
<tr><th colspan="2">Symbol</th><th>Parameter</th><th>Conditions</th><th>Min.(1)</th><th>Typ.</th><th>Max.(1)</th><th>Unit</th></tr>
<tr><td rowspan="4">Input levels</td><td>$V_{DDUSB}$</td><td>USB OTG full speed transceiver operating voltage</td><td>-</td><td>3.0(2)</td><td>-</td><td>3.6</td><td>V</td></tr>
<tr><td>$V_{DI}$(3)</td><td>Differential input sensitivity</td><td>I(USB_FS_DP/DM, USB_HS_DP/DM)</td><td>0.2</td><td>-</td><td>-</td><td rowspan="3">V</td></tr>
<tr><td>$V_{CM}$(3)</td><td>Differential common mode range</td><td>Includes $V_{DI}$ range</td><td>0.8</td><td>-</td><td>2.5</td></tr>
<tr><td>$V_{SE}$(3)</td><td>Single ended receiver threshold</td><td>-</td><td>1.3</td><td>-</td><td>2.0</td></tr>
<tr><td rowspan="2">Output levels</td><td>$V_{OL}$</td><td>Static output level low</td><td>$R_L$ of 1.5 kΩ to 3.6 V(4)</td><td>-</td><td>-</td><td>0.3</td><td rowspan="2">V</td></tr>
<tr><td>$V_{OH}$</td><td>Static output level high</td><td>$R_L$ of 15 kΩ to $V_{SS}$(4)</td><td>2.8</td><td>-</td><td>3.6</td></tr>
<tr><td colspan="2" rowspan="2">$R_{PD}$</td><td>PA11, PA12, PB14, PB15 (USB_FS_DP/DM, USB_HS_DP/DM)</td><td rowspan="2">$V_{IN} = V_{DD}$</td><td>17</td><td>21</td><td>24</td><td rowspan="4">kΩ</td></tr>
<tr><td>PA9, PB13 (OTG_FS_VBUS, OTG_HS_VBUS)</td><td>0.65</td><td>1.1</td><td>2.0</td></tr>
<tr><td colspan="2" rowspan="2">$R_{PU}$</td><td>PA12, PB15 (USB_FS_DP, USB_HS_DP)</td><td>$V_{IN} = V_{SS}$</td><td>1.5</td><td>1.8</td><td>2.1</td></tr>
<tr><td>PA9, PB13 (OTG_FS_VBUS, OTG_HS_VBUS)</td><td>$V_{IN} = V_{SS}$</td><td>0.25</td><td>0.37</td><td>0.55</td></tr>
</table>

1. All the voltages are measured from the local ground potential.
2. The USB OTG full speed transceiver functionality is ensured down to 2.7 V but not the full USB full speed electrical characteristics which are degraded in the 2.7-to-3.0 V $V_{DDUSB}$ voltage range.
3. Guaranteed by design.
4. $R_L$ is the load connected on the USB OTG full speed drivers.

*Note: When VBUS sensing feature is enabled, PA9 and PB13 should be left at their default state (floating input), not as alternate function. A typical 200 µA current consumption of the sensing block (current to voltage conversion to determine the different sessions) can be observed on PA9 and PB13 when the feature is enabled.*

Figure 53. USB OTG full speed timings: definition of data signal rise and fall time

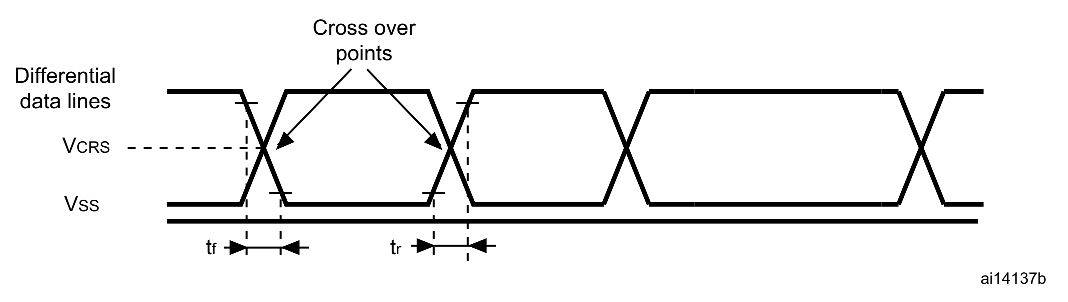



Table 82. USB OTG full speed electrical characteristics(1)

| Driver characteristics | | | | | |
|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Max** | **Unit** |
| $t_r$ | Rise time(2) | $C_L$ = 50 pF | 4 | 20 | ns |
| $t_f$ | Fall time(2) | $C_L$ = 50 pF | 4 | 20 | ns |
| $t_{rfm}$ | Rise/ fall time matching | $t_r/t_f$ | 90 | 110 | % |
| $V_{CRS}$ | Output signal crossover voltage | - | 1.3 | 2.0 | V |
| $Z_{DRV}$ | Output driver impedance(3) | Driving high or low | 28 | 44 | Ω |

1. Guaranteed by design.
2. Measured from 10% to 90% of the data signal. For more detailed informations, please refer to USB Specification - Chapter 7 (version 2.0).
3. No external termination series resistors are required on DP (D+) and DM (D-) pins since the matching impedance is included in the embedded driver.

## USB high speed (HS) characteristics

Unless otherwise specified, the parameters given in *Table 85* for ULPI are derived from tests performed under the ambient temperature, $f_{HCLK}$ frequency summarized in *Table 84* and $V_{DD}$ supply voltage conditions summarized in *Table 83*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11, unless otherwise specified
- Capacitive load C = 20 pF, unless otherwise specified
- Measurement points are done at CMOS levels: $0.5V_{DD}$.

Refer to *Section 6.3.17: I/O port characteristics* for more details on the input/output characteristics.

Table 83. USB HS DC electrical characteristics

| Symbol | | Parameter | Min.(1) | Max.(1) | Unit |
|---|---|---|---|---|---|
| **Input level** | $V_{DD}$ | USB OTG HS operating voltage | 1.7 | 3.6 | V |

1. All the voltages are measured from the local ground potential.

**Table 84. USB HS clock timing parameters(1)**

| Symbol | Parameter | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| - | $f_{HCLK}$ value to guarantee proper operation of USB HS interface | | 30 | - | - | MHz |
| $F_{START\_8BIT}$ | Frequency (first transition) | 8-bit ±10% | 54 | 60 | 66 | MHz |
| $F_{STEADY}$ | Frequency (steady state) ±500 ppm | | 59.97 | 60 | 60.03 | MHz |
| $D_{START\_8BIT}$ | Duty cycle (first transition) | 8-bit ±10% | 40 | 50 | 60 | % |
| $D_{STEADY}$ | Duty cycle (steady state) ±500 ppm | | 49.975 | 50 | 50.025 | % |
| $t_{STEADY}$ | Time to reach the steady state frequency and duty cycle after the first transition | | - | - | 1.4 | ms |
| $t_{START\_DEV}$ | Clock startup time after the de-assertion of SuspendM | Peripheral | - | - | 5.6 | ms |
| $t_{START\_HOST}$ | | Host | - | - | - | |
| $t_{PREP}$ | PHY preparation time after the first transition of the input clock | | - | - | - | µs |

1. Guaranteed by design.

**Figure 54. ULPI timing diagram**

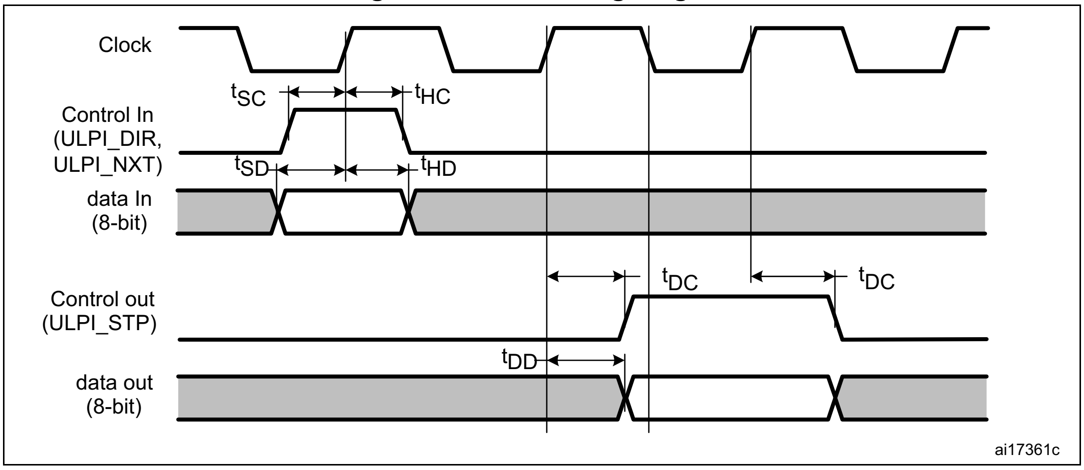


**Table 85. Dynamic characteristics: USB ULPI[(1)]**

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{SC}$ | Control in (ULPI_DIR, ULPI_NXT) setup time | - | 3 | - | - | ns |
| $t_{HC}$ | Control in (ULPI_DIR, ULPI_NXT) hold time | - | 1 | - | - | |
| $t_{SD}$ | Data in setup time | - | 1.5 | - | - | |
| $t_{HD}$ | Data in hold time | - | 0.5 | - | - | |
| $t_{DC}/t_{DD}$ | Data/control output delay | 2.7 V < $V_{DD}$ < 3.6 V, $C_L$ = 20 pF and OSPEEDRy[1:0] = 11 | - | 5.5 | 9 | |
| | | - | - | 5.5 | 11.5 | |
| | | 1.7 V < $V_{DD}$ < 3.6 V, $C_L$ = 15 pF and OSPEEDRy[1:0] = 11 | - | | | |

1. Guaranteed by characterization results.

### Ethernet characteristics

Unless otherwise specified, the parameters given in *Table 86*, *Table 87* and *Table 88* for SMI, RMII and MII are derived from tests performed under the ambient temperature, $f_{HCLK}$ frequency summarized in *Table 18* and $V_{DD}$ supply voltage conditions summarized in *Table 86*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 20 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$.

Refer to *Section 6.3.17: I/O port characteristics* for more details on the input/output characteristics.

*Table 86* gives the list of Ethernet MAC signals for the SMI (station management interface) and *Figure 55* shows the corresponding timing diagram.

**Figure 55. Ethernet SMI timing diagram**

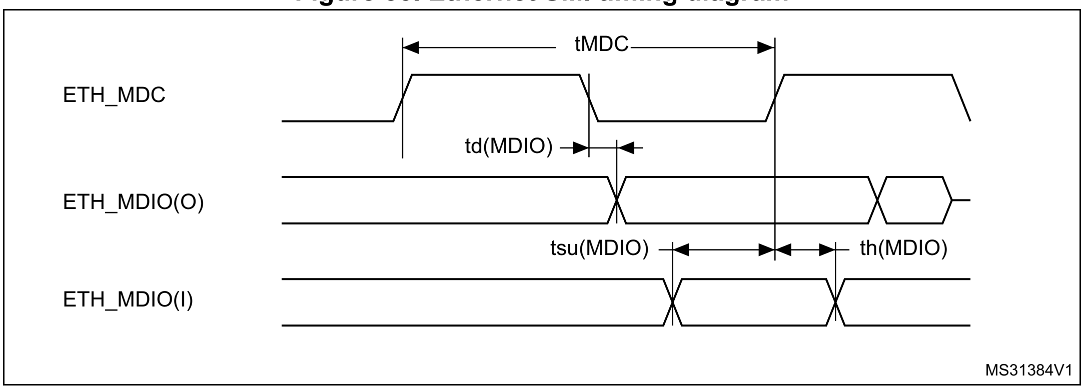


**Table 86. Dynamics characteristics: Ethernet MAC signals for SMI[(1)]**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{MDC}$ | MDC cycle time(2.38 MHz) | 400 | 400 | 403 | ns |
| $T_{d(MDIO)}$ | Write data valid time | 10 | 10.5 | 12.5 | |
| $t_{su(MDIO)}$ | Read data setup time | 12.5 | - | - | |
| $t_{h(MDIO)}$ | Read data hold time | 0 | - | - | |

1. Guaranteed by characterization results.

*Table 87* gives the list of Ethernet MAC signals for the RMII and *Figure 56* shows the corresponding timing diagram.

**Figure 56. Ethernet RMII timing diagram**

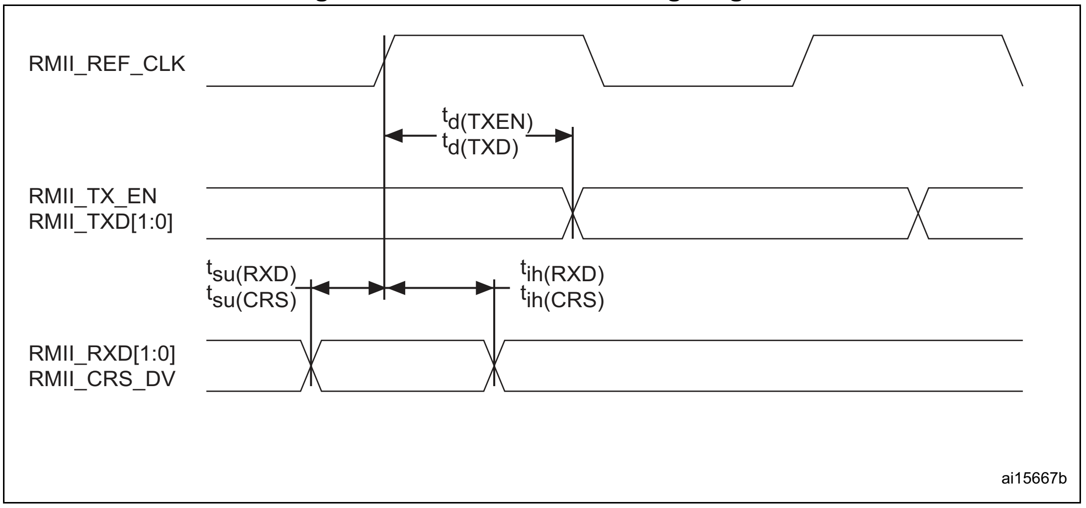



**Table 87. Dynamics characteristics: Ethernet MAC signals for RMII[(1)]**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{su(RXD)}$ | Receive data setup time | 1 | - | - | ns |
| $t_{ih(RXD)}$ | Receive data hold time | 1.5 | - | - | |
| $t_{su(CRS)}$ | Carrier sense setup time | 1 | - | - | |
| $t_{ih(CRS)}$ | Carrier sense hold time | 1 | - | - | |
| $t_{d(TXEN)}$ | Transmit enable valid delay time | 5 | 6 | 10.5 | |
| $t_{d(TXD)}$ | Transmit data valid delay time | 5 | 6 | 12 | |

1. Guaranteed by characterization results.

Table 88 gives the list of Ethernet MAC signals for MII and Figure 56 shows the corresponding timing diagram.

**Figure 57. Ethernet MII timing diagram**

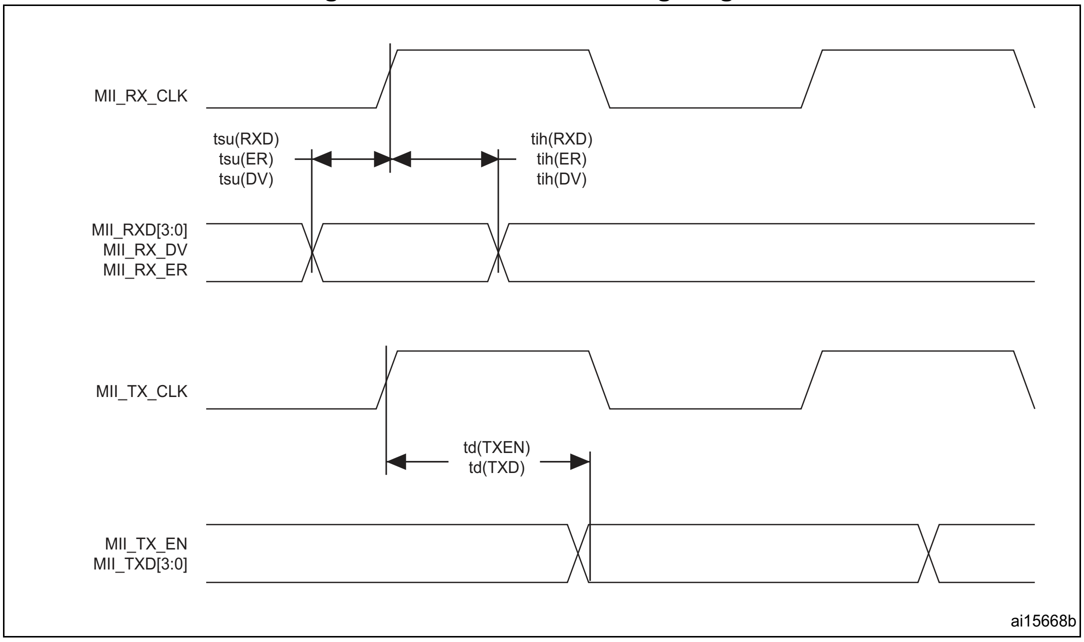



**Table 88. Dynamics characteristics: Ethernet MAC signals for MII(1)**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{su(RXD)}$ | Receive data setup time | 3 | - | - | ns |
| $t_{ih(RXD)}$ | Receive data hold time | 1.5 | - | - | |
| $t_{su(DV)}$ | Data valid setup time | 0 | - | - | |
| $t_{ih(DV)}$ | Data valid hold time | 1.5 | - | - | |
| $t_{su(ER)}$ | Error setup time | 1.5 | - | - | |
| $t_{ih(ER)}$ | Error hold time | 0.5 | - | - | |
| $t_{d(TXEN)}$ | Transmit enable valid delay time | 6.5 | 7 | 13.5 | |
| $t_{d(TXD)}$ | Transmit data valid delay time | 6.5 | 7 | 13.5 | |

1. Guaranteed by characterization results.

## CAN (controller area network) interface

Refer to Section 6.3.17: I/O port characteristics for more details on the input/output alternate function characteristics (CANx_TX and CANx_RX).

### 6.3.27 FMC characteristics

Unless otherwise specified, the parameters given in *Table 89* to *Table 102* for the FMC interface are derived from tests performed under the ambient temperature, $f_{HCLK}$ frequency and $V_{DD}$ supply voltage conditions summarized in *Table 18*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Measurement points are done at CMOS levels: $0.5V_{DD}$

Refer to *Section 6.3.17: I/O port characteristics* for more details on the input/output characteristics.

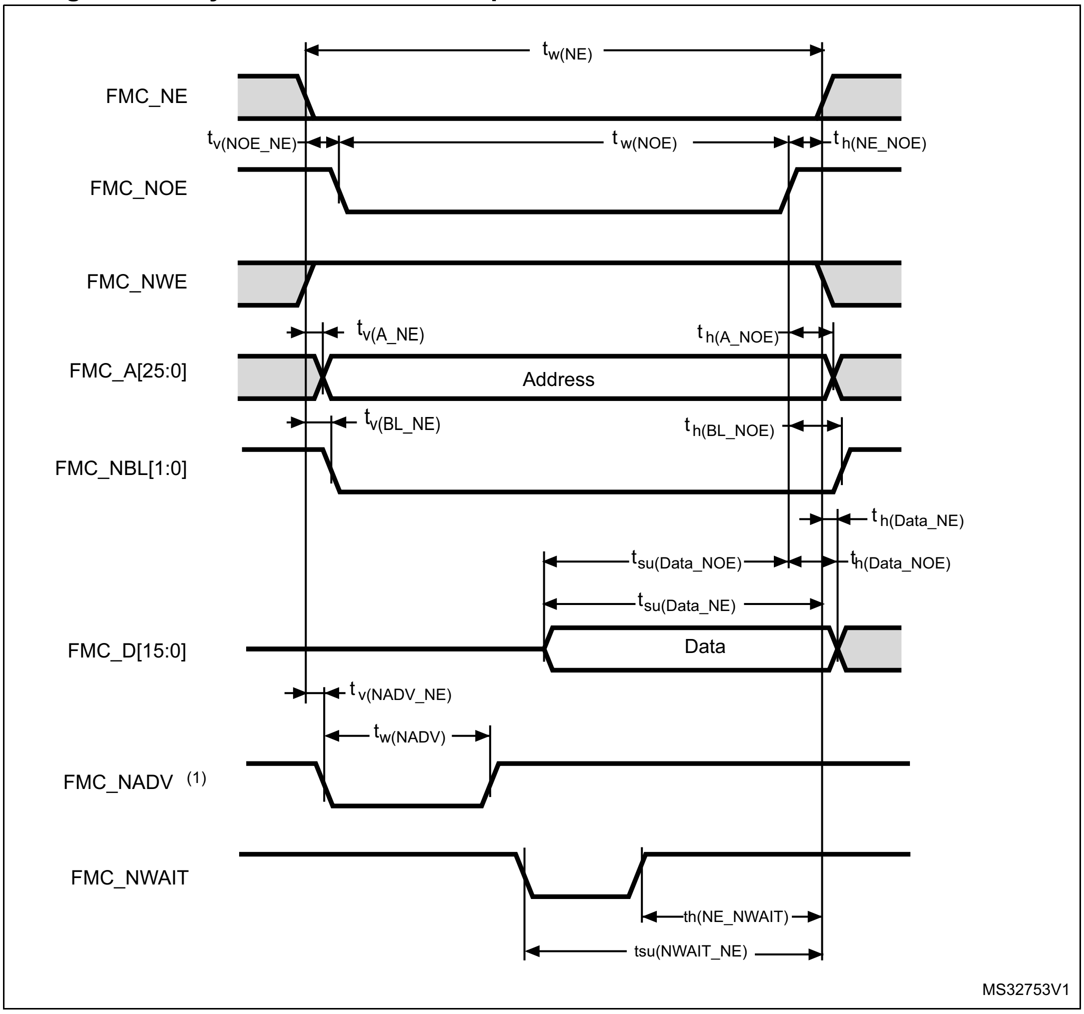
#### Asynchronous waveforms and timings

*Figure 58* through *Figure 61* represent asynchronous waveforms and *Table 89* through *Table 96* provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- AddressSetupTime = 0x1
- AddressHoldTime = 0x1
- DataSetupTime = 0x1 (except for asynchronous NWAIT mode , DataSetupTime = 0x5)
- BusTurnAroundDuration = 0x0
- Capcitive load CL = 30 pF

In all timing tables, the $T_{HCLK}$ is the HCLK clock period

**Figure 58. Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms**




1. Mode 2/B, C and D only. In Mode 1, FMC_NADV is not used.

Table 89. Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings(1)

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(NE)}$ | FMC_NE low time | $2T_{HCLK} - 0.5$ | $2\ T_{HCLK}+1.5$ | ns |
| $t_{v(NOE\_NE)}$ | FMC_NEx low to FMC_NOE low | 0 | 1 | |
| $t_{w(NOE)}$ | FMC_NOE low time | $2T_{HCLK} - 1$ | $2T_{HCLK} + 1$ | |
| $t_{h(NE\_NOE)}$ | FMC_NOE high to FMC_NE high hold time | 0 | - | |
| $t_{v(A\_NE)}$ | FMC_NEx low to FMC_A valid | - | 0.5 | |
| $t_{h(A\_NOE)}$ | Address hold time after FMC_NOE high | 0 | - | |
| $t_{v(BL\_NE)}$ | FMC_NEx low to FMC_BL valid | - | 0.5 | |
| $t_{h(BL\_NOE)}$ | FMC_BL hold time after FMC_NOE high | 0 | - | |
| $t_{su(Data\_NE)}$ | Data to FMC_NEx high setup time | $T_{HCLK} - 2$ | - | |
| $t_{su(Data\_NOE)}$ | Data to FMC_NOEx high setup time | $T_{HCLK} -2$ | - | |
| $t_{h(Data\_NOE)}$ | Data hold time after FMC_NOE high | 0 | - | |
| $t_{h(Data\_NE)}$ | Data hold time after FMC_NEx high | 0 | - | |
| $t_{v(NADV\_NE)}$ | FMC_NEx low to FMC_NADV low | - | 0 | |
| $t_{w(NADV)}$ | FMC_NADV low time | - | $T_{HCLK} +1$ | |

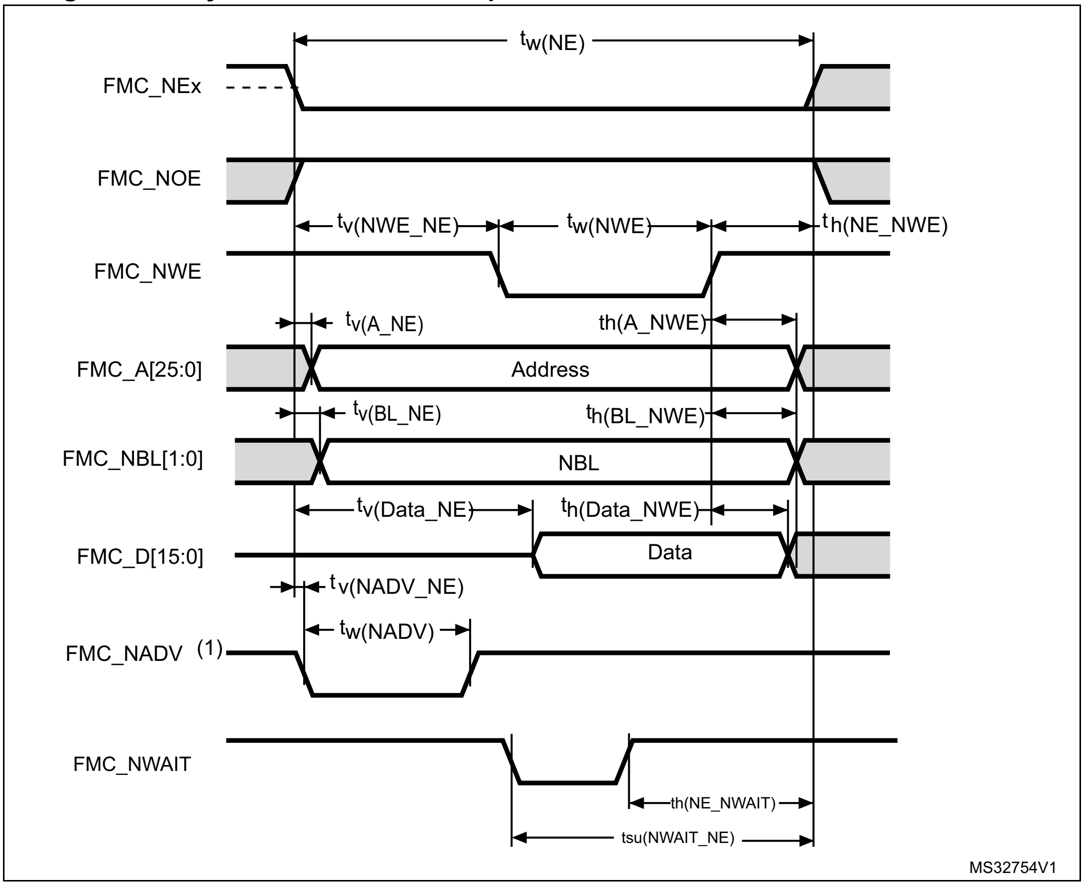
1. $C_L$ = 30 pF.

Table 90. Asynchronous non-multiplexed SRAM/PSRAM/NOR read - NWAIT timings(1)

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(NE)}$ | FMC_NE low time | $7T_{HCLK} - 1$ | $7T_{HCLK}$ | ns |
| $t_{w(NOE)}$ | FMC_NWE low time | $5T_{HCLK} - 1$ | $5T_{HCLK} + 1$ | |
| $t_{w(NWAIT)}$ | FMC_NWAIT low time | $T_{HCLK} - 0.5$ | | |
| $t_{su(NWAIT\_NE)}$ | FMC_NWAIT valid before FMC_NEx high | $5T_{HCLK} + 1.5$ | - | |
| $t_{h(NE\_NWAIT)}$ | FMC_NEx hold time after FMC_NWAIT invalid | $4T_{HCLK}+1$ | - | |

1. Guaranteed by characterization results.

Figure 59. Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms




1. Mode 2/B, C and D only. In Mode 1, FMC_NADV is not used.

Table 91. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings[1]

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(NE)}$ | FMC_NE low time | $3T_{HCLK}-0.5$ | $3T_{HCLK}+1.5$ | ns |
| $t_{v(NWE\_NE)}$ | FMC_NEx low to FMC_NWE low | $T_{HCLK}-0.5$ | $T_{HCLK}+1$ | |
| $t_{w(NWE)}$ | FMC_NWE low time | $T_{HCLK}-0.5$ | $T_{HCLK}+1$ | |
| $t_{h(NE\_NWE)}$ | FMC_NWE high to FMC_NE high hold time | $T_{HCLK}-0.5$ | - | |
| $t_{v(A\_NE)}$ | FMC_NEx low to FMC_A valid | - | 0 | |
| $t_{h(A\_NWE)}$ | Address hold time after FMC_NWE high | $T_{HCLK}-0.5$ | - | |
| $t_{v(BL\_NE)}$ | FMC_NEx low to FMC_BL valid | - | 0 | |
| $t_{h(BL\_NWE)}$ | FMC_BL hold time after FMC_NWE high | $T_{HCLK}-0.5$ | - | |
| $t_{v(Data\_NE)}$ | Data to FMC_NEx low to Data valid | - | $T_{HCLK}+3$ | |
| $t_{h(Data\_NWE)}$ | Data hold time after FMC_NWE high | $T_{HCLK}+0.5$ | - | |
| $t_{v(NADV\_NE)}$ | FMC_NEx low to FMC_NADV low | - | 0 | |
| $t_{w(NADV)}$ | FMC_NADV low time | - | $T_{HCLK}+0.5$ | |

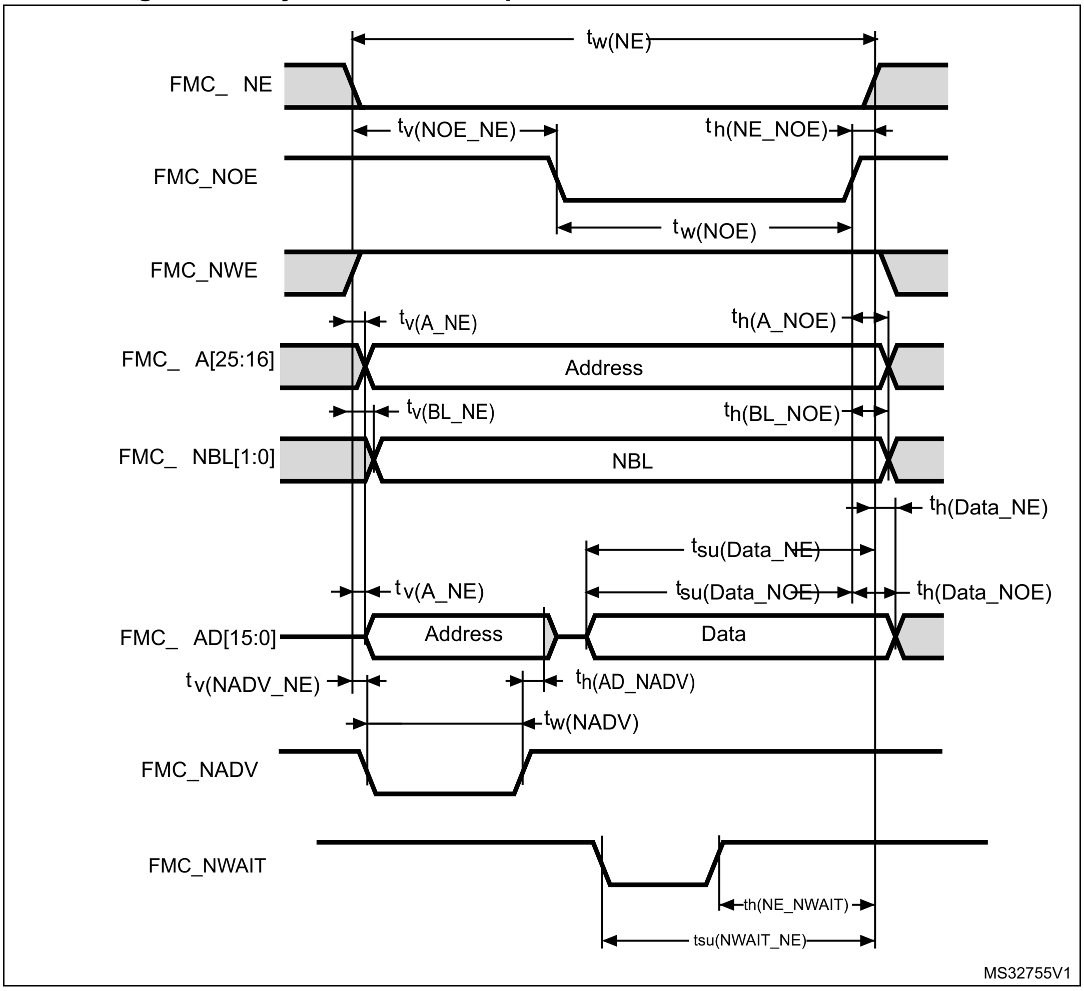
1. Guaranteed by characterization results.

**Table 92. Asynchronous non-multiplexed SRAM/PSRAM/NOR write - NWAIT timings(1)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(NE)}$ | FMC_NE low time | $8T_{HCLK}-0.5$ | $8T_{HCLK}+1.5$ | ns |
| $t_{w(NWE)}$ | FMC_NWE low time | $6T_{HCLK}-0.5$ | $6T_{HCLK}+1$ | |
| $t_{su(NWAIT\_NE)}$ | FMC_NWAIT valid before FMC_NEx high | $6T_{HCLK}-1$ | - | |
| $t_{h(NE\_NWAIT)}$ | FMC_NEx hold time after FMC_NWAIT invalid | $4T_{HCLK}+2$ | - | |

1. Guaranteed by characterization results.

**Figure 60. Asynchronous multiplexed PSRAM/NOR read waveforms**



### Table 93. Asynchronous multiplexed PSRAM/NOR read timings(1)

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(NE)}$ | FMC_NE low time | $3T_{HCLK}-0.5$ | $3T_{HCLK}+1.5$ | ns |
| $t_{v(NOE\_NE)}$ | FMC_NEx low to FMC_NOE low | $2T_{HCLK}-1$ | $2T_{HCLK}+0.5$ | |
| $t_{tw(NOE)}$ | FMC_NOE low time | $T_{HCLK}-0.5$ | $T_{HCLK}+0.5$ | |
| $t_{h(NE\_NOE)}$ | FMC_NOE high to FMC_NE high hold time | 0 | - | |
| $t_{v(A\_NE)}$ | FMC_NEx low to FMC_A valid | - | 0.5 | |
| $t_{v(NADV\_NE)}$ | FMC_NEx low to FMC_NADV low | 0 | 0.5 | |
| $t_{w(NADV)}$ | FMC_NADV low time | $T_{HCLK}-0.5$ | $T_{HCLK}+1.5$ | |
| $t_{h(AD\_NADV)}$ | FMC_AD(address) valid hold time after FMC_NADV high) | 0 | - | |
| $t_{h(A\_NOE)}$ | Address hold time after FMC_NOE high | $T_{HCLK}-0.5$ | - | |
| $t_{h(BL\_NOE)}$ | FMC_BL time after FMC_NOE high | 0 | - | |
| $t_{v(BL\_NE)}$ | FMC_NEx low to FMC_BL valid | - | 0.5 | |
| $t_{su(Data\_NE)}$ | Data to FMC_NEx high setup time | $T_{HCLK}-2$ | - | |
| $t_{su(Data\_NOE)}$ | Data to FMC_NOE high setup time | $T_{HCLK}-2$ | - | |
| $t_{h(Data\_NE)}$ | Data hold time after FMC_NEx high | 0 | - | |
| $t_{h(Data\_NOE)}$ | Data hold time after FMC_NOE high | 0 | - | |

1. Guaranteed by characterization results.

### Table 94. Asynchronous multiplexed PSRAM/NOR read-NWAIT timings(1)

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(NE)}$ | FMC_NE low time | $8T_{HCLK}-1$ | $8T_{HCLK}+2$ | ns |
| $t_{w(NOE)}$ | FMC_NWE low time | $5T_{HCLK}-1$ | $5T_{HCLK}+1$ | |
| $t_{su(NWAIT\_NE)}$ | FMC_NWAIT valid before FMC_NEx high | $5T_{HCLK}+1.5$ | - | |
| $t_{h(NE\_NWAIT)}$ | FMC_NEx hold time after FMC_NWAIT invalid | $4T_{HCLK}+1$ | - | |

1. Guaranteed by characterization results.

**Figure 61. Asynchronous multiplexed PSRAM/NOR write waveforms**

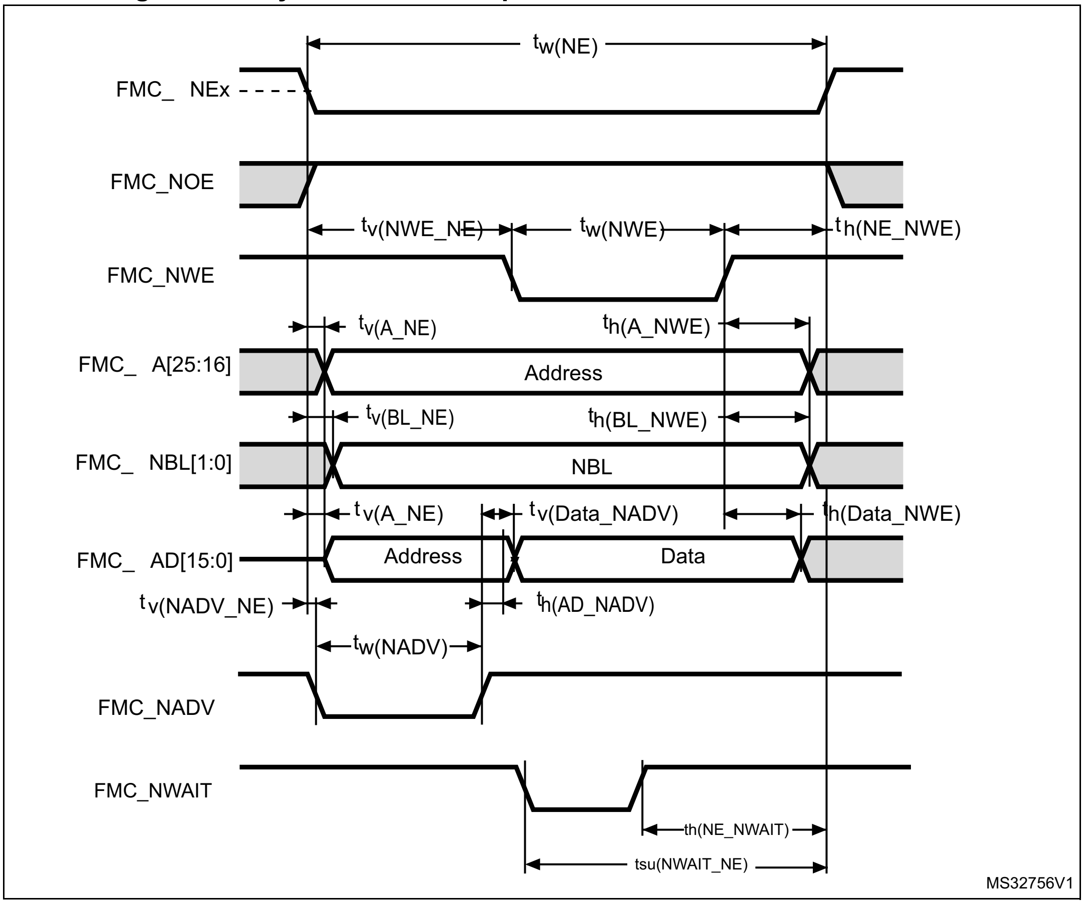



**Table 95. Asynchronous multiplexed PSRAM/NOR write timings(1)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(NE)}$ | FMC_NE low time | $4T_{HCLK}-0.5$ | $4T_{HCLK}+1.5$ | ns |
| $t_{v(NWE\_NE)}$ | FMC_NEx low to FMC_NWE low | $T_{HCLK}-1$ | $T_{HCLK}+0.5$ | |
| $t_{w(NWE)}$ | FMC_NWE low time | $2T_{HCLK}-0.5$ | $2T_{HCLK}+0.5$ | |
| $t_{h(NE\_NWE)}$ | FMC_NWE high to FMC_NE high hold time | $T_{HCLK}$ | - | |
| $t_{v(A\_NE)}$ | FMC_NEx low to FMC_A valid | - | 0 | |
| $t_{v(NADV\_NE)}$ | FMC_NEx low to FMC_NADV low | 0 | 0.5 | |
| $t_{w(NADV)}$ | FMC_NADV low time | $T_{HCLK}-0.5$ | $T_{HCLK}+ 1.5$ | |
| $t_{h(AD\_NADV)}$ | FMC_AD(adress) valid hold time after FMC_NADV high) | $T_{HCLK}-2$ | - | |
| $t_{h(A\_NWE)}$ | Address hold time after FMC_NWE high | $T_{HCLK}$ | - | |
| $t_{h(BL\_NWE)}$ | FMC_BL hold time after FMC_NWE high | $T_{HCLK}-2$ | - | |
| $t_{v(BL\_NE)}$ | FMC_NEx low to FMC_BL valid | - | 0 | |
| $t_{v(Data\_NADV)}$ | FMC_NADV high to Data valid | - | $T_{HCLK}+2$ | |
| $t_{h(Data\_NWE)}$ | Data hold time after FMC_NWE high | $T_{HCLK}+0.5$ | - | |

1. Guaranteed by characterization results.

**Table 96. Asynchronous multiplexed PSRAM/NOR write-NWAIT timings(1)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(NE)}$ | FMC_NE low time | $9T_{HCLK}$ | $9T_{HCLK}+1.5$ | ns |
| $t_{w(NWE)}$ | FMC_NWE low time | $7T_{HCLK}-0.5$ | $7T_{HCLK}+0.5$ | |
| $t_{su(NWAIT\_NE)}$ | FMC_NWAIT valid before FMC_NEx high | $6T_{HCLK}+2$ | - | |
| $t_{h(NE\_NWAIT)}$ | FMC_NEx hold time after FMC_NWAIT invalid | $4T_{HCLK}-1$ | - | |

1. Guaranteed by characterization results.

### Synchronous waveforms and timings

*Figure 62* through *Figure 65* represent synchronous waveforms and *Table 97* through *Table 100* provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- BurstAccessMode = FMC_BurstAccessMode_Enable;
- MemoryType = FMC_MemoryType_CRAM;
- WriteBurst = FMC_WriteBurst_Enable;
- CLKDivision = 1;
- DataLatency = 1 for NOR flash; DataLatency = 0 for PSRAM
- CL = 30 pF on data and address lines. CL = 10 pF on FMC_CLK unless otherwise specified.

In all timing tables, the $T_{HCLK}$ is the HCLK clock period.

– For 2.7 V≤$V_{DD}$≤3.6 V, maximum FMC_CLK = 108 MHz at CL=20 pF or 90 MHz at CL=30 pF (on FMC_CLK).

– For 1.71 V≤$V_{DD}$<2.7 V, maximum FMC_CLK = 70 MHz at CL=10 pF (on FMC_CLK).

**Figure 62. Synchronous multiplexed NOR/PSRAM read timings**

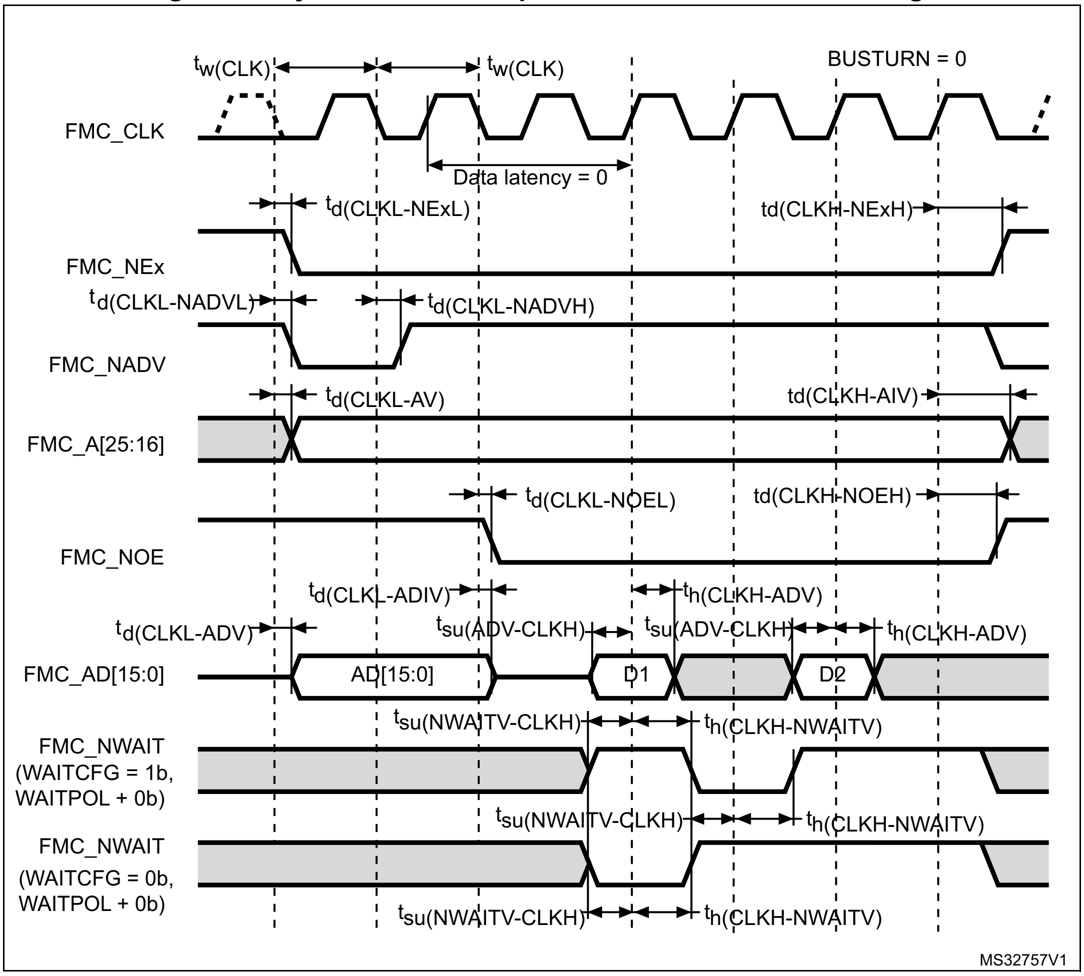


Table 97. Synchronous multiplexed NOR/PSRAM read timings[1]

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(CLK)}$ | FMC_CLK period | $2T_{HCLK}-0.5$ | - | ns |
| $t_{d(CLKL-NExL)}$ | FMC_CLK low to FMC_NEx low (x=0..2) | - | 2 | |
| $t_{d(CLKH\_NExH)}$ | FMC_CLK high to FMC_NEx high (x= 0…2) | $T_{HCLK}+0.5$ | - | |
| $t_{d(CLKL-NADVL)}$ | FMC_CLK low to FMC_NADV low | - | 1.5 | |
| $t_{d(CLKL-NADVH)}$ | FMC_CLK low to FMC_NADV high | 0 | - | |
| $t_{d(CLKL-AV)}$ | FMC_CLK low to FMC_Ax valid (x=16…25) | - | 2 | |
| $t_{d(CLKH-AIV)}$ | FMC_CLK high to FMC_Ax invalid (x=16…25) | $T_{HCLK}$ | - | |
| $t_{d(CLKL-NOEL)}$ | FMC_CLK low to FMC_NOE low | - | 2 | |
| $t_{d(CLKH-NOEH)}$ | FMC_CLK high to FMC_NOE high | $T_{HCLK}-0.5$ | - | |
| $t_{d(CLKL-ADV)}$ | FMC_CLK low to FMC_AD[15:0] valid | - | 3 | |
| $t_{d(CLKL-ADIV)}$ | FMC_CLK low to FMC_AD[15:0] invalid | 0 | - | |
| $t_{su(ADV-CLKH)}$ | FMC_A/D[15:0] valid data before FMC_CLK high | 1.5 | - | |
| $t_{h(CLKH-ADV)}$ | FMC_A/D[15:0] valid data after FMC_CLK high | 1 | - | |
| $t_{su(NWAIT-CLKH)}$ | FMC_NWAIT valid before FMC_CLK high | 2 | - | |
| $t_{h(CLKH-NWAIT)}$ | FMC_NWAIT valid after FMC_CLK high | 3.5 | - | |

1. Guaranteed by characterization results.

**Figure 63. Synchronous multiplexed PSRAM write timings**

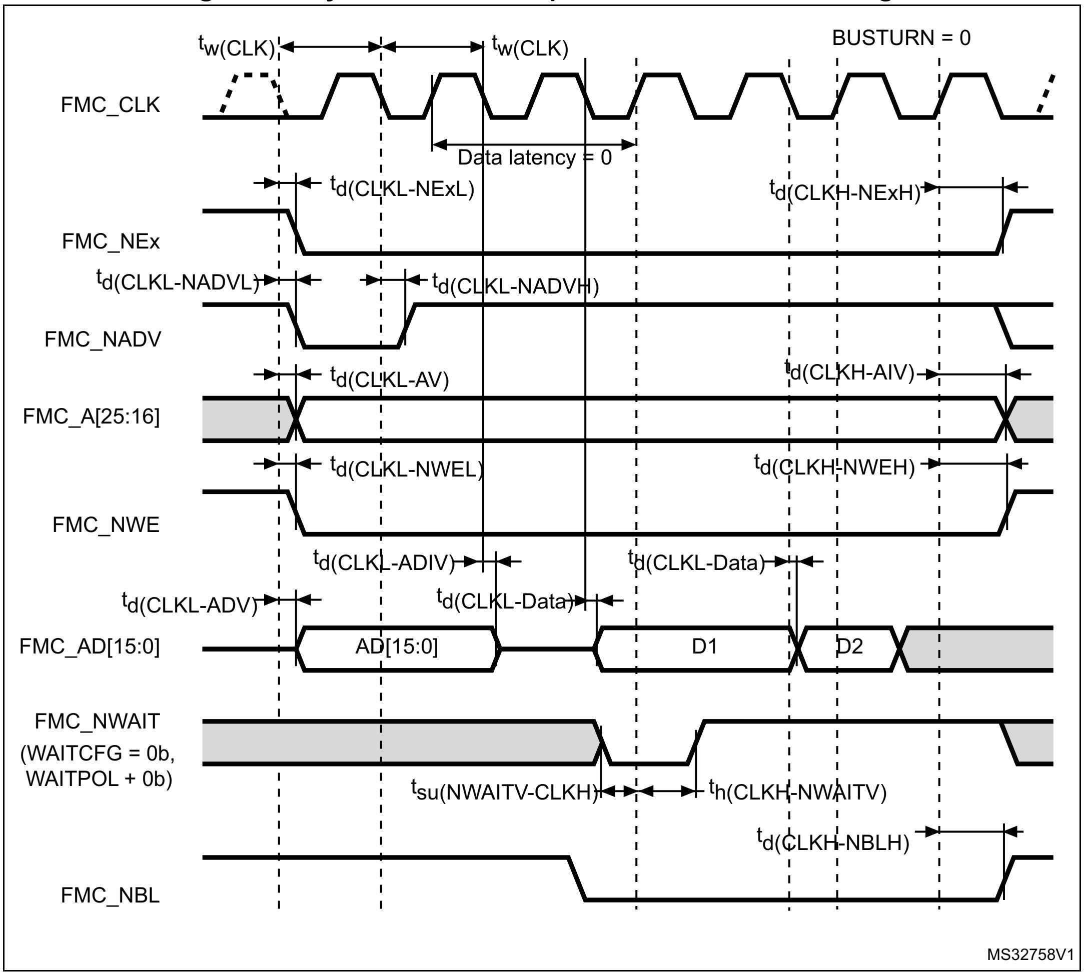


Table 98. Synchronous multiplexed PSRAM write timings(1)

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(CLK)}$ | FMC_CLK period | $2T_{HCLK}-0.5$ | - | ns |
| $t_{d(CLKL-NExL)}$ | FMC_CLK low to FMC_NEx low (x=0..2) | - | 1.5 | |
| $t_{d(CLKH-NExH)}$ | FMC_CLK high to FMC_NEx high (x= 0…2) | $T_{HCLK}+0.5$ | - | |
| $t_{d(CLKL-NADVL)}$ | FMC_CLK low to FMC_NADV low | - | 1.5 | |
| $t_{d(CLKL-NADVH)}$ | FMC_CLK low to FMC_NADV high | 0 | - | |
| $t_{d(CLKL-AV)}$ | FMC_CLK low to FMC_Ax valid (x=16…25) | - | 2 | |
| $t_{d(CLKH-AIV)}$ | FMC_CLK high to FMC_Ax invalid (x=16…25) | $T_{HCLK}$ | - | |
| $t_{d(CLKL-NWEL)}$ | FMC_CLK low to FMC_NWE low | - | 1.5 | |
| $t_{(CLKH-NWEH)}$ | FMC_CLK high to FMC_NWE high | $T_{HCLK}-0.5$ | - | |
| $t_{d(CLKL-ADV)}$ | FMC_CLK low to FMC_AD[15:0] valid | - | 3 | |
| $t_{d(CLKL-ADIV)}$ | FMC_CLK low to FMC_AD[15:0] invalid | 0 | - | |
| $t_{d(CLKL-DATA)}$ | FMC_A/D[15:0] valid data after FMC_CLK low | - | 3.5 | |
| $t_{d(CLKL-NBLL)}$ | FMC_CLK low to FMC_NBL low | 1 | - | |
| $t_{d(CLKH-NBLH)}$ | FMC_CLK high to FMC_NBL high | $T_{HCLK}+0.5$ | - | |
| $t_{su(NWAIT-CLKH)}$ | FMC_NWAIT valid before FMC_CLK high | 2 | - | |
| $t_{h(CLKH-NWAIT)}$ | FMC_NWAIT valid after FMC_CLK high | 3.5 | - | |

1. Guaranteed by characterization results.

**Figure 64. Synchronous non-multiplexed NOR/PSRAM read timings**

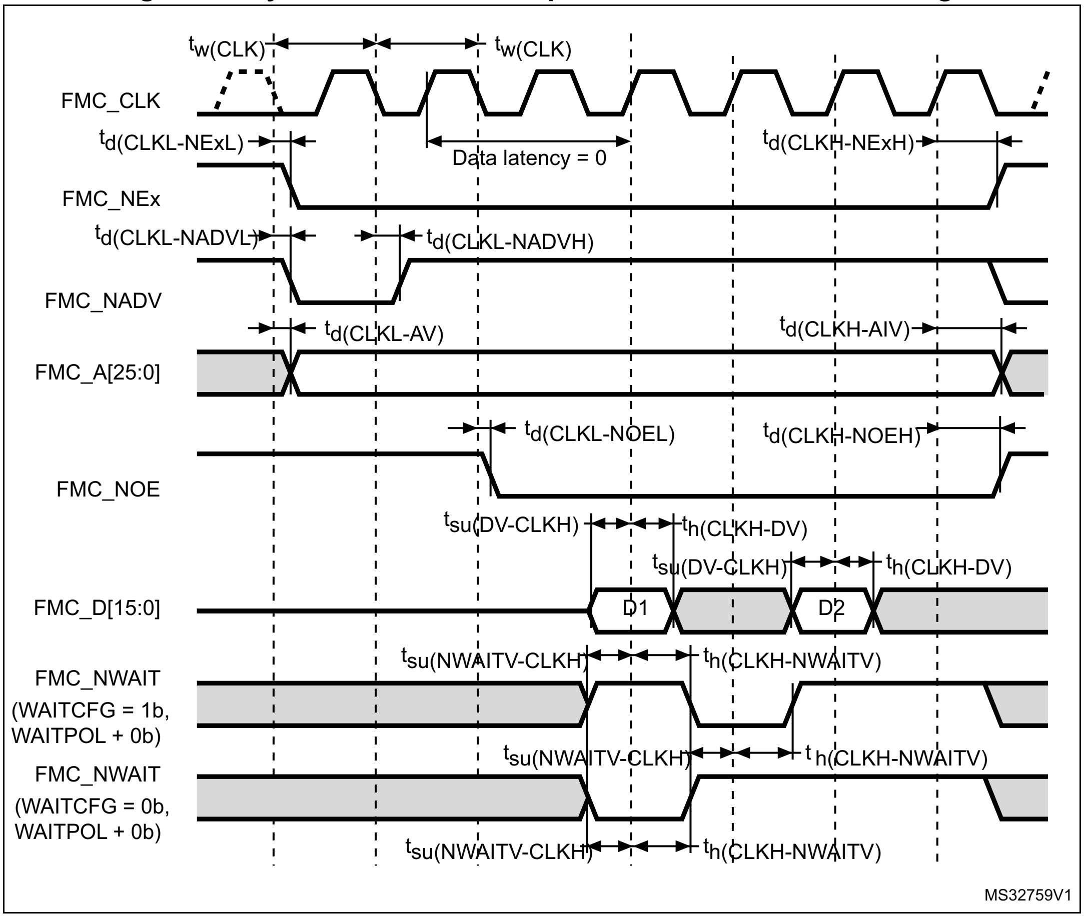



**Table 99. Synchronous non-multiplexed NOR/PSRAM read timings(1)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(CLK)}$ | FMC_CLK period | $2T_{HCLK}-1$ | - | ns |
| $t_{(CLKL-NExL)}$ | FMC_CLK low to FMC_NEx low (x=0..2) | - | 2.5 | |
| $t_{d(CLKH-NExH)}$ | FMC_CLK high to FMC_NEx high (x= 0…2) | $T_{HCLK}+0.5$ | - | |
| $t_{d(CLKL-NADVL)}$ | FMC_CLK low to FMC_NADV low | - | 0 | |
| $t_{d(CLKL-NADVH)}$ | FMC_CLK low to FMC_NADV high | 0 | - | |
| $t_{d(CLKL-AV)}$ | FMC_CLK low to FMC_Ax valid (x=16…25) | - | 2.5 | |
| $t_{d(CLKH-AIV)}$ | FMC_CLK high to FMC_Ax invalid (x=16…25) | $T_{HCLK}$ | - | |
| $t_{d(CLKL-NOEL)}$ | FMC_CLK low to FMC_NOE low | - | 2 | |
| $t_{d(CLKH-NOEH)}$ | FMC_CLK high to FMC_NOE high | $T_{HCLK}+0.5$ | - | |
| $t_{su(DV-CLKH)}$ | FMC_D[15:0] valid data before FMC_CLK high | 1.5 | - | |
| $t_{h(CLKH-DV)}$ | FMC_D[15:0] valid data after FMC_CLK high | 1 | - | |
| $t_{(NWAIT-CLKH)}$ | FMC_NWAIT valid before FMC_CLK high | 2 | - | |
| $t_{h(CLKH-NWAIT)}$ | FMC_NWAIT valid after FMC_CLK high | 3.5 | - | |

1. Guaranteed by characterization results.

**Figure 65. Synchronous non-multiplexed PSRAM write timings**

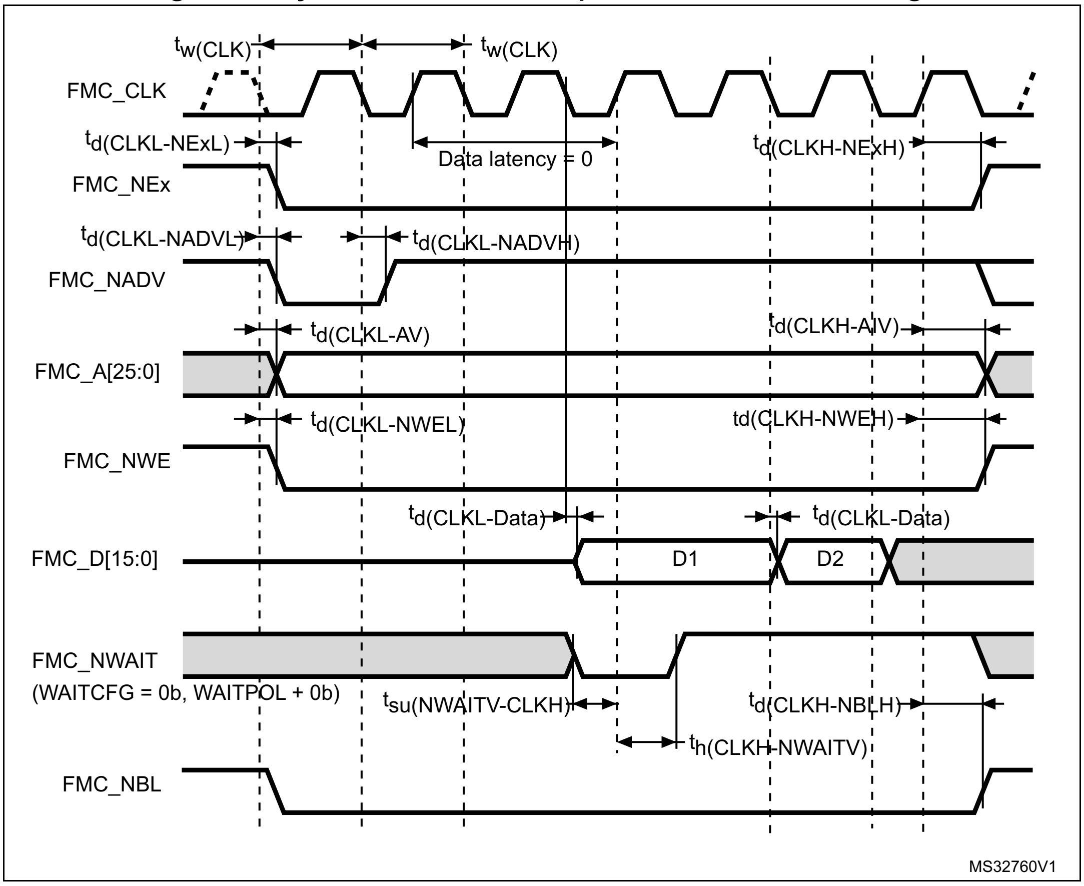


**Table 100. Synchronous non-multiplexed PSRAM write timings**(1)

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{(CLK)}$ | FMC_CLK period | $2T_{HCLK}-1$ | - | ns |
| $t_{d(CLKL\text{-}NExL)}$ | FMC_CLK low to FMC_NEx low (x=0..2) | - | 2.5 | |
| $t_{(CLKH\text{-}NExH)}$ | FMC_CLK high to FMC_NEx high (x= 0…2) | $T_{HCLK}+0.5$ | - | |
| $t_{d(CLKL\text{-}NADVL)}$ | FMC_CLK low to FMC_NADV low | - | 1.5 | |
| $t_{d(CLKL\text{-}NADVH)}$ | FMC_CLK low to FMC_NADV high | 0 | - | |
| $t_{d(CLKL\text{-}AV)}$ | FMC_CLK low to FMC_Ax valid (x=16…25) | - | 2.5 | |
| $t_{d(CLKH\text{-}AIV)}$ | FMC_CLK high to FMC_Ax invalid (x=16…25) | 0 | - | |
| $t_{d(CLKL\text{-}NWEL)}$ | FMC_CLK low to FMC_NWE low | - | 1.5 | |
| $t_{d(CLKH\text{-}NWEH)}$ | FMC_CLK high to FMC_NWE high | $T_{HCLK}+1$ | - | |
| $t_{d(CLKL\text{-}Data)}$ | FMC_D[15:0] valid data after FMC_CLK low | - | 3 | |
| $t_{d(CLKL\text{-}NBLL)}$ | FMC_CLK low to FMC_NBL low | 1.5 | - | |
| $t_{d(CLKH\text{-}NBLH)}$ | FMC_CLK high to FMC_NBL high | $T_{HCLK}+0.5$ | - | |
| $t_{su(NWAIT\text{-}CLKH)}$ | FMC_NWAIT valid before FMC_CLK high | 2 | - | |
| $t_{h(CLKH\text{-}NWAIT)}$ | FMC_NWAIT valid after FMC_CLK high | 3.5 | - | |

1. Guaranteed by characterization results.

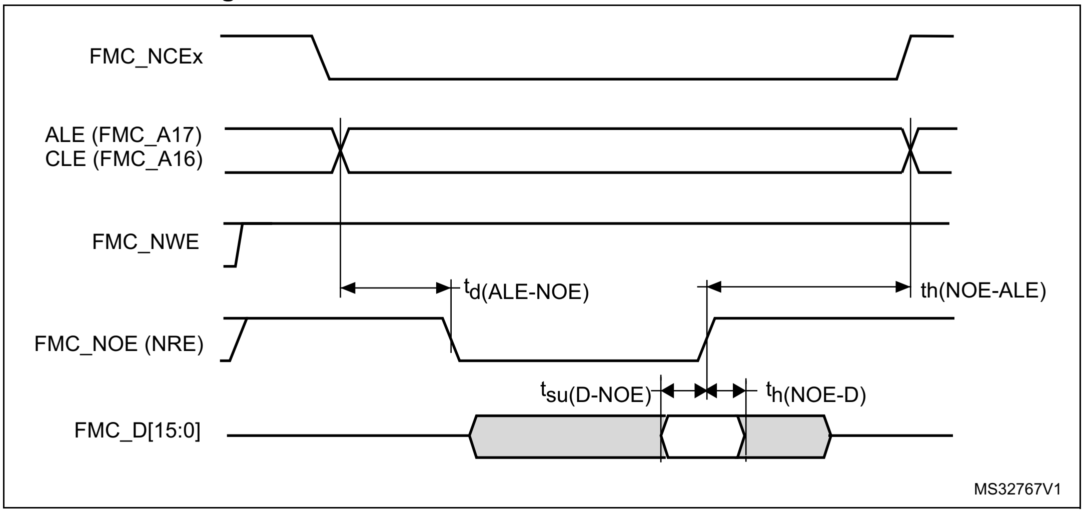
### NAND controller waveforms and timings

*Figure 66* through *Figure 69* represent synchronous waveforms, and *Table 101* and *Table 102* provide the corresponding timings. The results shown in this table are obtained with the following FMC configuration:

- COM.FMC_SetupTime = 0x01;
- COM.FMC_WaitSetupTime = 0x03;
- COM.FMC_HoldSetupTime = 0x02;
- COM.FMC_HiZSetupTime = 0x01;
- ATT.FMC_SetupTime = 0x01;
- ATT.FMC_WaitSetupTime = 0x03;
- ATT.FMC_HoldSetupTime = 0x02;
- ATT.FMC_HiZSetupTime = 0x01;
- Bank = FMC_Bank_NAND;
- MemoryDataWidth = FMC_MemoryDataWidth_16b;
- ECC = FMC_ECC_Enable;
- ECCPageSize = FMC_ECCPageSize_512Bytes;
- TCLRSetupTime = 0;
- TARSetupTime = 0.

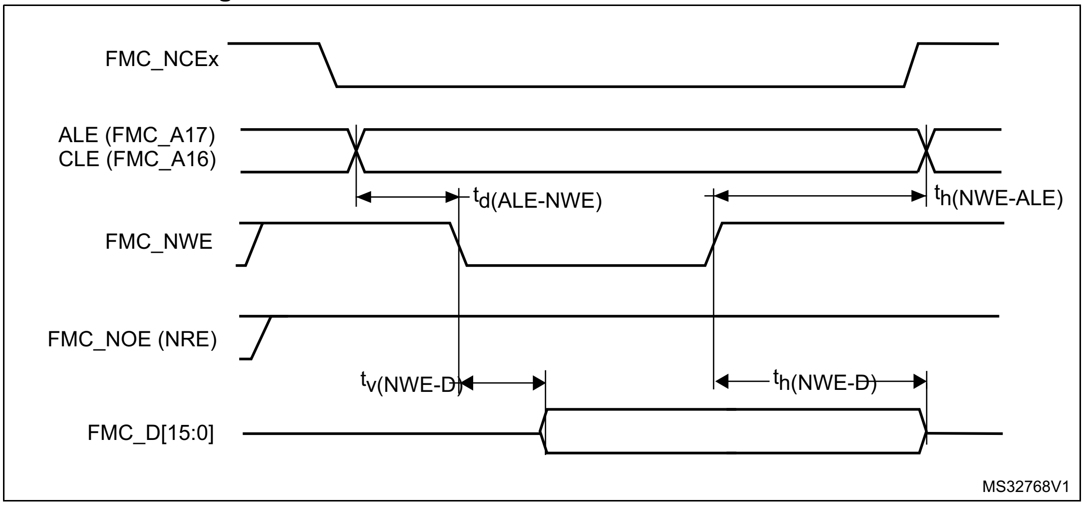
In all timing tables, the $T_{HCLK}$ is the HCLK clock period.

Figure 66. NAND controller waveforms for read access




1. y = 7 or 15 depending on the NAND flash memory interface

Figure 67. NAND controller waveforms for write access




1. y = 7 or 15 depending on the NAND flash memory interface.

Figure 68. NAND controller waveforms for common memory read access

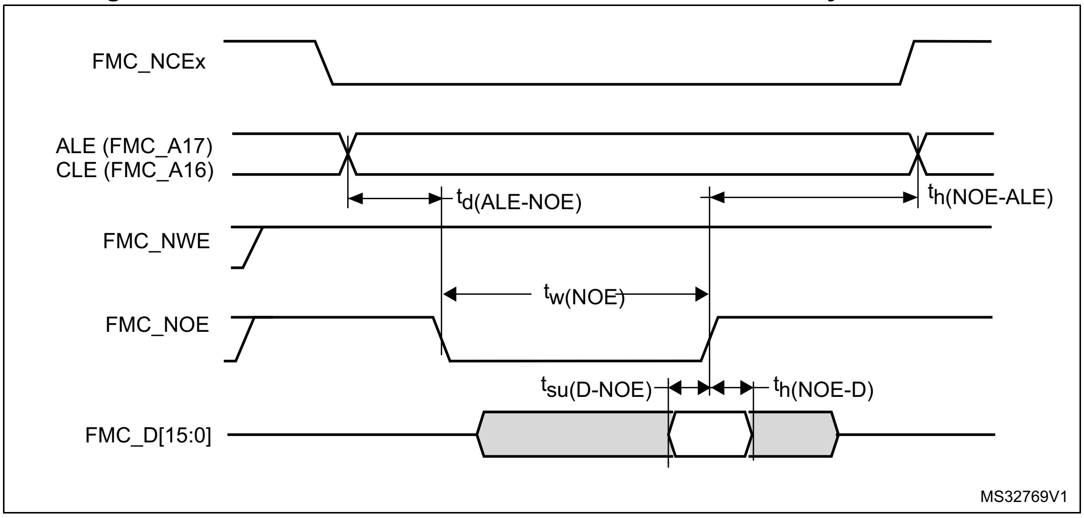



Figure 69. NAND controller waveforms for common memory write access

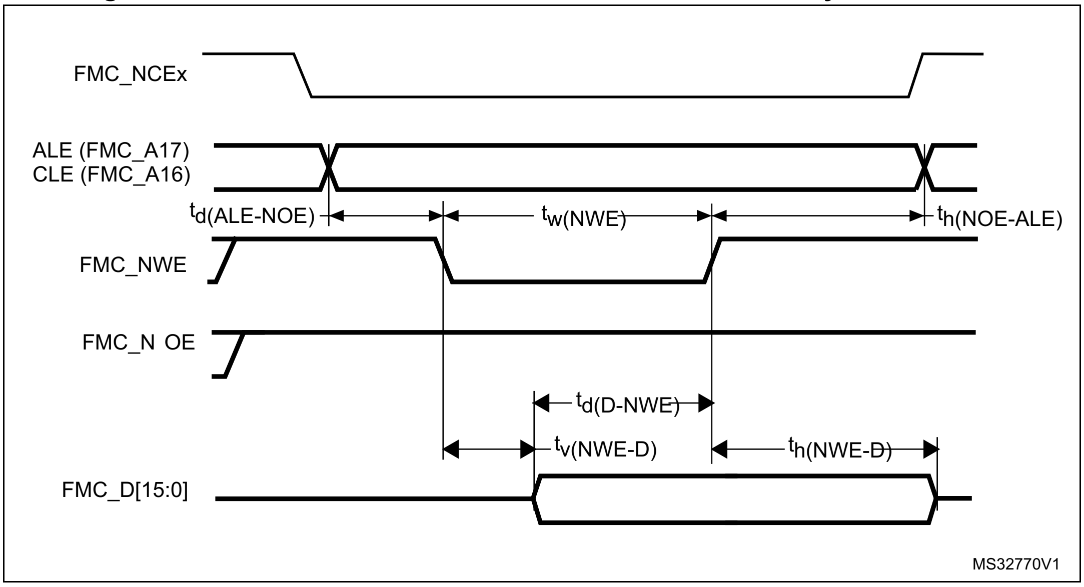



Table 101. Switching characteristics for NAND flash read cycles(1)

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(N0E)}$ | FMC_NOE low width | $4T_{HCLK}-0.5$ | $4T_{HCLK}$ | ns |
| $t_{su(D-NOE)}$ | FMC_D[15-0] valid data before FMC_NOE high | 13 | - | |
| $t_{h(NOE-D)}$ | FMC_D[15-0] valid data after FMC_NOE high | 3 | - | |
| $t_{d(ALE-NOE)}$ | FMC_ALE valid before FMC_NOE low | - | $3T_{HCLK}-0.5$ | |
| $t_{h(NOE-ALE)}$ | FMC_NWE high to FMC_ALE invalid | $3T_{HCLK}-2$ | - | |

1. Guaranteed by characterization results.

**Table 102. Switching characteristics for NAND flash write cycles[1]**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(NWE)}$ | FMC_NWE low width | $4T_{HCLK}-0.5$ | $4T_{HCLK}$ | ns |
| $t_{v(NWE-D)}$ | FMC_NWE low to FMC_D[15-0] valid | 0 | - | |
| $t_{h(NWE-D)}$ | FMC_NWE high to FMC_D[15-0] invalid | $3T_{HCLK}-1$ | - | |
| $t_{d(D-NWE)}$ | FMC_D[15-0] valid before FMC_NWE high | $5T_{HCLK}-3$ | - | |
| $t_{d(ALE-NWE)}$ | FMC_ALE valid before FMC_NWE low | - | $3T_{HCLK}-0.5$ | |
| $t_{h(NWE-ALE)}$ | FMC_NWE high to FMC_ALE invalid | $3T_{HCLK}-2$ | - | |

1. Guaranteed by characterization results.

### SDRAM waveforms and timings

- CL = 30 pF on data and address lines. CL = 10 pF on FMC_SDCLK unless otherwise specified.

In all timing tables, the $T_{HCLK}$ is the HCLK clock period.

- For 3.0 V≤$V_{DD}$≤3.6 V, maximum FMC_SDCLK= 100 MHz at CL=20 pF (on FMC_SDCLK).
- For 2.7 V≤$V_{DD}$≤3.6 V, maximum FMC_SDCLK = 90 MHz at CL=30 pF (on FMC_SDCLK).
- For 1.71 V≤$V_{DD}$<1.9 V, maximum FMC_SDCLK = 70 MHz at CL=10 pF (on FMC_SDCLK).

**Figure 70. SDRAM read access waveforms (CL = 1)**

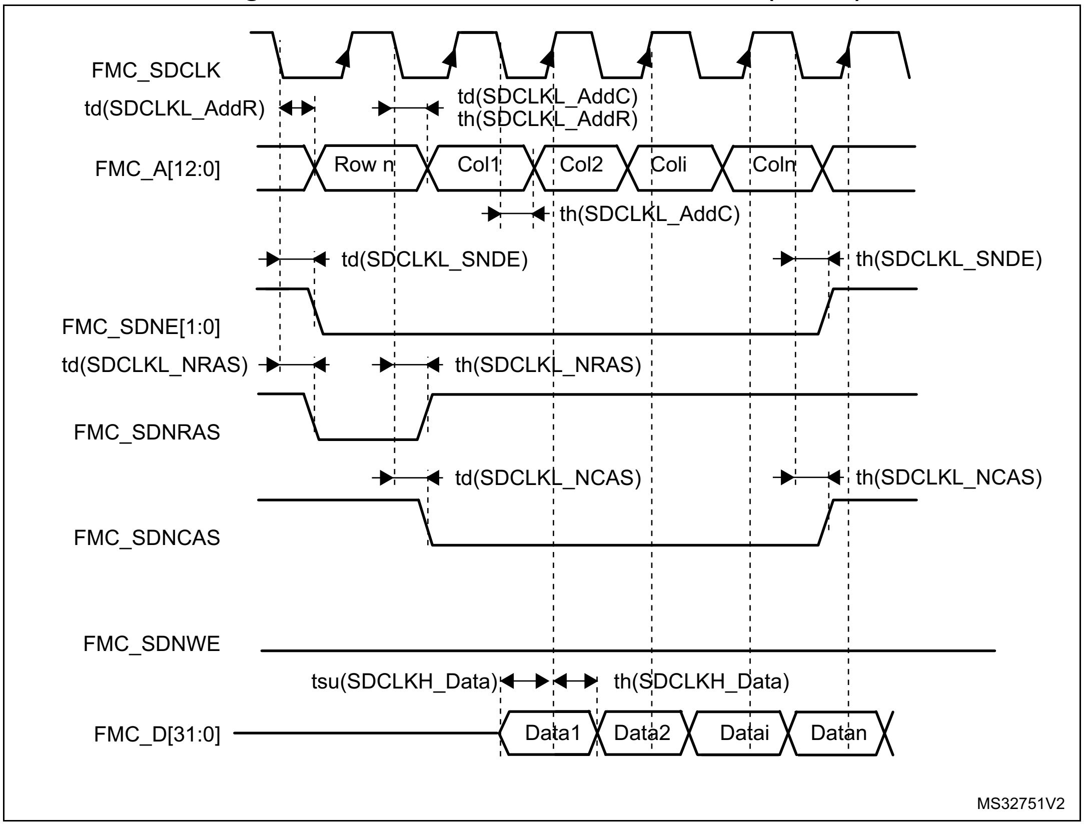


Table 103. SDRAM read timings[1]

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(SDCLK)}$ | FMC_SDCLK period | $2T_{HCLK}-0.5$ | $2T_{HCLK}+0.5$ | ns |
| $t_{su(SDCLKH\_Data)}$ | Data input setup time | 3.5 | - | |
| $t_{h(SDCLKH\_Data)}$ | Data input hold time | 1.5 | - | |
| $t_{d(SDCLKL\_Add)}$ | Address valid time | - | 4 | |
| $t_{d(SDCLKL- SDNE)}$ | Chip select valid time | - | 0.5 | |
| $t_{h(SDCLKL\_SDNE)}$ | Chip select hold time | 0 | - | |
| $t_{d(SDCLKL\_SDNRAS)}$ | SDNRAS valid time | - | 0.5 | |
| $t_{h(SDCLKL\_SDNRAS)}$ | SDNRAS hold time | 0 | - | |
| $t_{d(SDCLKL\_SDNCAS)}$ | SDNCAS valid time | - | 0.5 | |
| $t_{h(SDCLKL\_SDNCAS)}$ | SDNCAS hold time | 0 | - | |

1. Guaranteed by characterization results.

Table 104. LPSDR SDRAM read timings[1]

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{W(SDCLK)}$ | FMC_SDCLK period | $2T_{HCLK}-0.5$ | $2T_{HCLK}+0.5$ | ns |
| $t_{su(SDCLKH\_Data)}$ | Data input setup time | 3 | - | |
| $t_{h(SDCLKH\_Data)}$ | Data input hold time | 1.5 | - | |
| $t_{d(SDCLKL\_Add)}$ | Address valid time | - | 3.5 | |
| $t_{d(SDCLKL\_SDNE)}$ | Chip select valid time | - | 0.5 | |
| $t_{h(SDCLKL\_SDNE)}$ | Chip select hold time | 0 | - | |
| $t_{d(SDCLKL\_SDNRAS}$ | SDNRAS valid time | - | 0.5 | |
| $t_{h(SDCLKL\_SDNRAS)}$ | SDNRAS hold time | 0 | - | |
| $t_{d(SDCLKL\_SDNCAS)}$ | SDNCAS valid time | - | 0.5 | |
| $t_{h(SDCLKL\_SDNCAS)}$ | SDNCAS hold time | 0 | - | |

1. Guaranteed by characterization results.

Figure 71. SDRAM write access waveforms

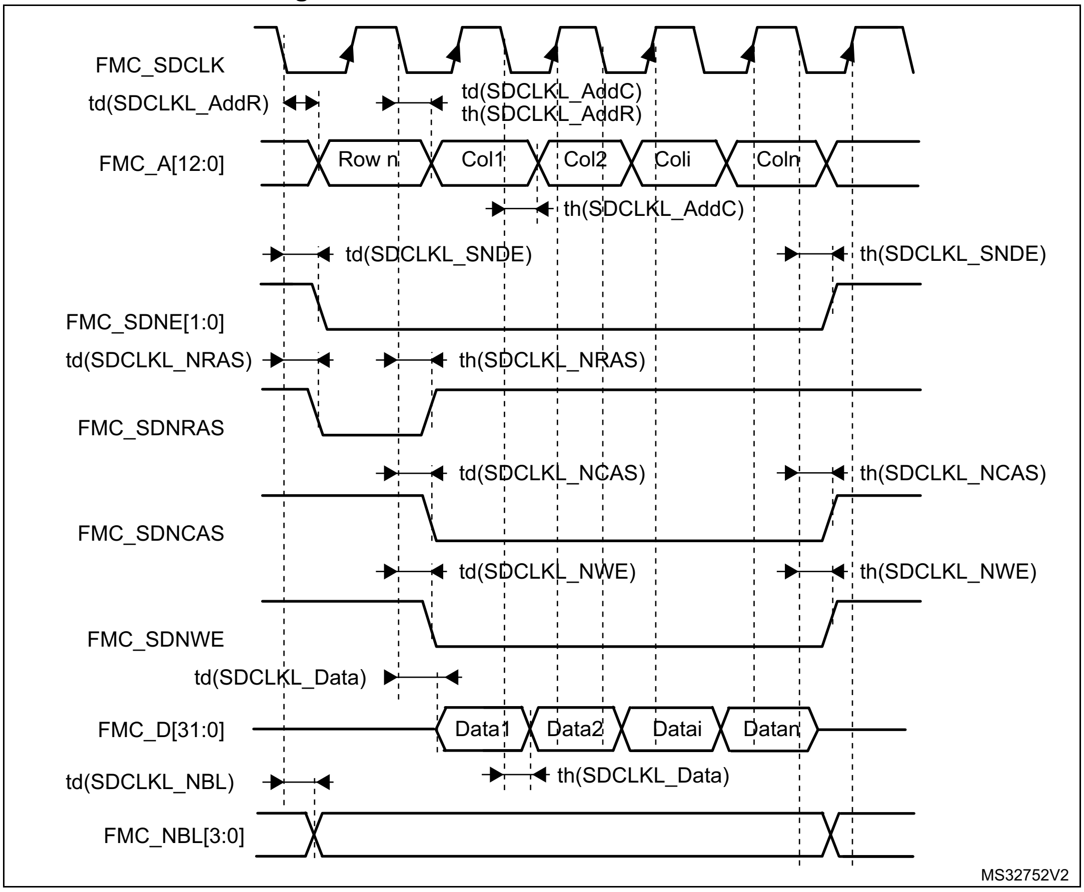



Table 105. SDRAM write timings[(1)]

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(SDCLK)}$ | FMC_SDCLK period | $2T_{HCLK}-0.5$ | $2T_{HCLK}+0.5$ | ns |
| $t_{d(SDCLKL\_Data)}$ | Data output valid time | - | 2 | |
| $t_{h(SDCLKL\_Data)}$ | Data output hold time | 0.5 | - | |
| $t_{d(SDCLKL\_Add)}$ | Address valid time | - | 4 | |
| $t_{d(SDCLKL\_SDNWE)}$ | SDNWE valid time | - | 0.5 | |
| $t_{h(SDCLKL\_SDNWE)}$ | SDNWE hold time | 0 | - | |
| $t_{d(SDCLKL\_SDNE)}$ | Chip select valid time | - | 0.5 | |
| $t_{h(SDCLKL-\_SDNE)}$ | Chip select hold time | 0 | - | |
| $t_{d(SDCLKL\_SDNRAS)}$ | SDNRAS valid time | - | 0.5 | |
| $t_{h(SDCLKL\_SDNRAS)}$ | SDNRAS hold time | 0 | - | |
| $t_{d(SDCLKL\_SDNCAS)}$ | SDNCAS valid time | - | 0.5 | |
| $t_{d(SDCLKL\_SDNCAS)}$ | SDNCAS hold time | 0 | - | |

1. Guaranteed by characterization results.

**Table 106. LPSDR SDRAM write timings[1]**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(SDCLK)}$ | FMC_SDCLK period | $2T_{HCLK}-0.5$ | $2T_{HCLK}+0.5$ | ns |
| $t_{d(SDCLKL\_Data)}$ | Data output valid time | - | 4 | |
| $t_{h(SDCLKL\_Data)}$ | Data output hold time | 0 | - | |
| $t_{d(SDCLKL\_Add)}$ | Address valid time | - | 3.5 | |
| $t_{d(SDCLKL-SDNWE)}$ | SDNWE valid time | - | 0.5 | |
| $t_{h(SDCLKL-SDNWE)}$ | SDNWE hold time | 0 | - | |
| $t_{d(SDCLKL-SDNE)}$ | Chip select valid time | - | 0.5 | |
| $t_{h(SDCLKL-SDNE)}$ | Chip select hold time | 0 | - | |
| $t_{d(SDCLKL-SDNRAS)}$ | SDNRAS valid time | - | 0.5 | |
| $t_{h(SDCLKL-SDNRAS)}$ | SDNRAS hold time | 0 | - | |
| $t_{d(SDCLKL-SDNCAS)}$ | SDNCAS valid time | - | 0.5 | |
| $t_{d(SDCLKL-SDNCAS)}$ | SDNCAS hold time | 0 | - | |

1. Guaranteed by characterization results.

## 6.3.28 Quad-SPI interface characteristics

Unless otherwise specified, the parameters given in *Table 107* and *Table 108* for Quad-SPI are derived from tests performed under the ambient temperature, $f_{AHB}$ frequency and $V_{DD}$ supply voltage conditions summarized in *Table 18: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 20 pF
- Measurement points are done at CMOS levels: $0.5 \times V_{DD}$

Refer to *Section 6.3.17: I/O port characteristics* for more details on the input/output alternate function characteristics.

**Table 107. Quad-SPI characteristics in SDR mode[1]**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Fck1/t(CK) | Quad-SPI clock frequency | $2.7\ V \leq V_{DD} < 3.6\ V$ CL=20 pF | - | - | 108 | MHz |
| | | $1.71\ V < V_{DD} < 3.6\ V$ CL=15 pF | - | - | 100 | |

**Table 107. Quad-SPI characteristics (continued)in SDR mode[1] (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| tw(CKH) | Quad-SPI clock high and low time | - | t(CK)/2 -1 | - | t(CK)/2 | ns |
| tw(CKL) | | | t(CK)/2 | - | t(CK)/2+1 | |
| ts(IN) | Data input setup time | - | 1 | - | - | |
| th(IN) | Data input hold time | | 3 | - | - | |
| tv(OUT) | Data output valid time | 2.7 V<$V_{DD}$<3.6 V | - | 1.5 | 3 | |
| | | 1.71 V<$V_{DD}$<3.6 V | - | 1.5 | 4 | |
| th(OUT) | Data output hold time | - | 0 | - | - | |

1. Guaranteed by characterization results.

**Table 108. Quad-SPI characteristics in DDR mode[1]**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Fck1/t(CK) | Quad-SPI clock frequency | 2.7 V<$V_{DD}$<3.6 V CL=20 pF | - | - | 80 | MHz |
| | | 1.8 V<$V_{DD}$<3.6 V CL=15 pF | - | - | 80 | |
| | | 1.71 V<$V_{DD}$<3.6 V CL=10 pF | - | - | 80 | |
| tw(CKH) | Quad-SPI clock high and low time | - | t(CK)/2 -1 | - | t(CK)/2 | ns |
| tw(CKL) | | | t(CK)/2 | - | t(CK)/2+ 1 | |
| ts(IN), tsf(IN) | Data input setup time | 2.7 V<$V_{DD}$<3.6 V | 1.5 | - | - | |
| | | 1.71 V<$V_{DD}$<2 V | 0.75 | - | - | |
| thr(IN), thf(IN) | Data input hold time | 2.7 V<$V_{DD}$<3.6 V | 3.5 | - | - | |
| | | 1.71 V<$V_{DD}$<2 V | 4.5 | | | |
| tvr(OUT), tvf(OUT) | Data output valid time | 2.7 V<$V_{DD}$<3.6 V | - | 8 | 10.5 | |
| | | 1.71 V<$V_{DD}$<3.6 V DHHC=0 | - | 8 | 14.5 | |
| | | DHHC=1 Pres=1, 2... | - | Thclk/2 +1.75 | Thclk/2 +2.25 | |
| thr(OUT), thf(OUT) | Data output hold time | DHHC=0 | 7.5 | - | - | |
| | | DHHC=1 Pres=1, 2... | Thclk/2 +1.5 | - | - | |

1. Guaranteed by characterization results.

**Figure 72. Quad-SPI timing diagram - SDR mode**

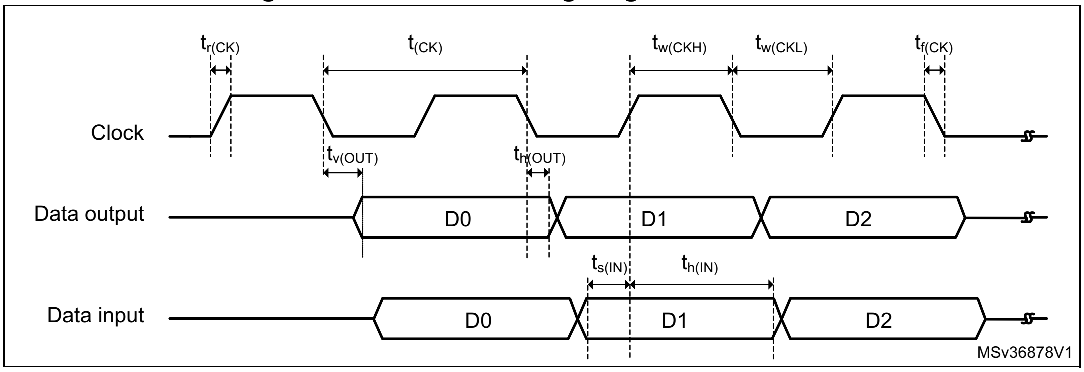
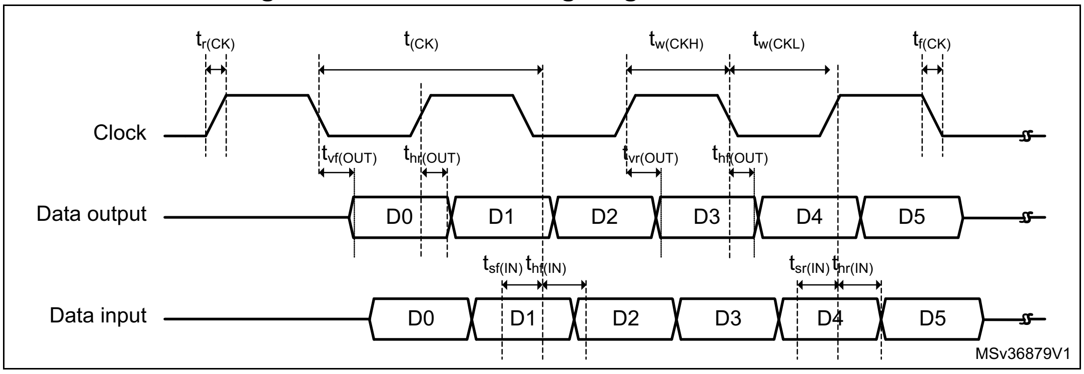



**Figure 73. Quad-SPI timing diagram - DDR mode**




## 6.3.29 Camera interface (DCMI) timing specifications

Unless otherwise specified, the parameters given in *Table 109* for DCMI are derived from tests performed under the ambient temperature, $f_{HCLK}$ frequency and $V_{DD}$ supply voltage summarized in *Table 18*, with the following configuration:

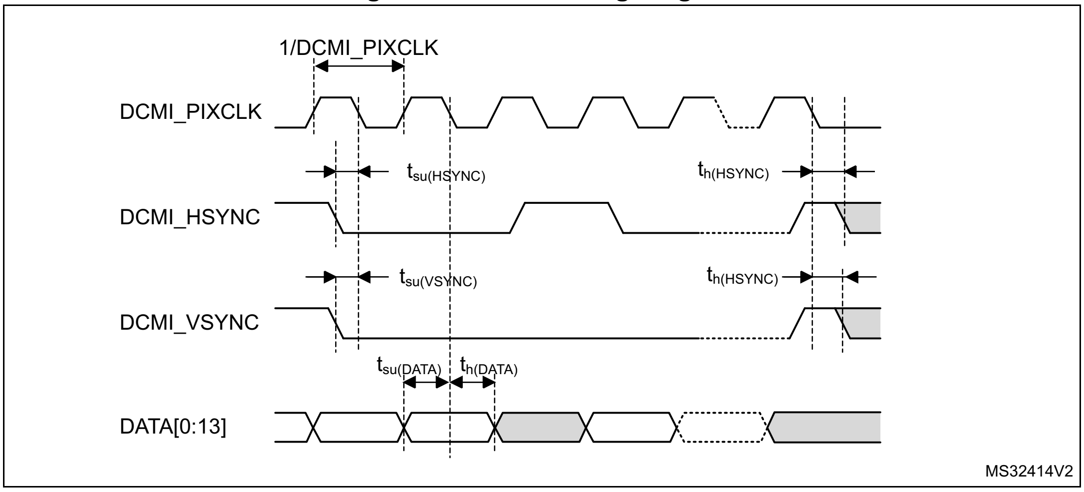
- DCMI_PIXCLK polarity: falling
- DCMI_VSYNC and DCMI_HSYNC polarity: high
- Data formats: 14 bits

**Table 109. DCMI characteristics(1)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| - | Frequency ratio DCMI_PIXCLK/$f_{HCLK}$ | - | 0.4 | |
| DCMI_PIXCLK | Pixel clock input | - | 54 | MHz |
| $D_{Pixel}$ | Pixel clock input duty cycle | 30 | 70 | % |
| $t_{su(DATA)}$ | Data input setup time | 3.5 | - | ns |
| $t_{h(DATA)}$ | Data input hold time | 0 | - | |
| $t_{su(HSYNC)}$ $t_{su(VSYNC)}$ | DCMI_HSYNC/DCMI_VSYNC input setup time | 2.5 | - | |
| $t_{h(HSYNC)}$ $t_{h(VSYNC)}$ | DCMI_HSYNC/DCMI_VSYNC input hold time | 0 | - | |

1. Guaranteed by characterization results.

**Figure 74. DCMI timing diagram**




## 6.3.30 LCD-TFT controller (LTDC) characteristics

Unless otherwise specified, the parameters given in *Table 110* for LCD-TFT are derived from tests performed under the ambient temperature, $f_{HCLK}$ frequency and $V_{DD}$ supply voltage summarized in *Table 18*, with the following configuration:

- LCD_CLK polarity: high
- LCD_DE polarity : low
- LCD_VSYNC and LCD_HSYNC polarity: high
- Pixel formats: 24 bits

**Table 110. LTDC characteristics [(1)]**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $f_{CLK}$ | LTDC clock output frequency | - | 83 | MHz |
| $D_{CLK}$ | LTDC clock output duty cycle | 45 | 55 | % |
| $t_{w(CLKH)}$<br>$t_{w(CLKL)}$ | Clock High time, low time | tw(CLK)/2 − 0.5 | tw(CLK)/2+0.5 | ns |
| $t_{v(DATA)}$ | Data output valid time | - | 6 | ns |
| $t_{h(DATA)}$ | Data output hold time | 2 | - | ns |
| $t_{v(HSYNC)}$<br>$t_{v(VSYNC)}$<br>$t_{v(DE)}$ | HSYNC/VSYNC/DE output valid time | - | 3 | ns |
| $t_{h(HSYNC)}$<br>$t_{h(VSYNC)}$<br>th(DE) | HSYNC/VSYNC/DE output hold time | 0.5 | - | ns |

1. Guaranteed by characterization results.

Figure 75. LCD-TFT horizontal timing diagram

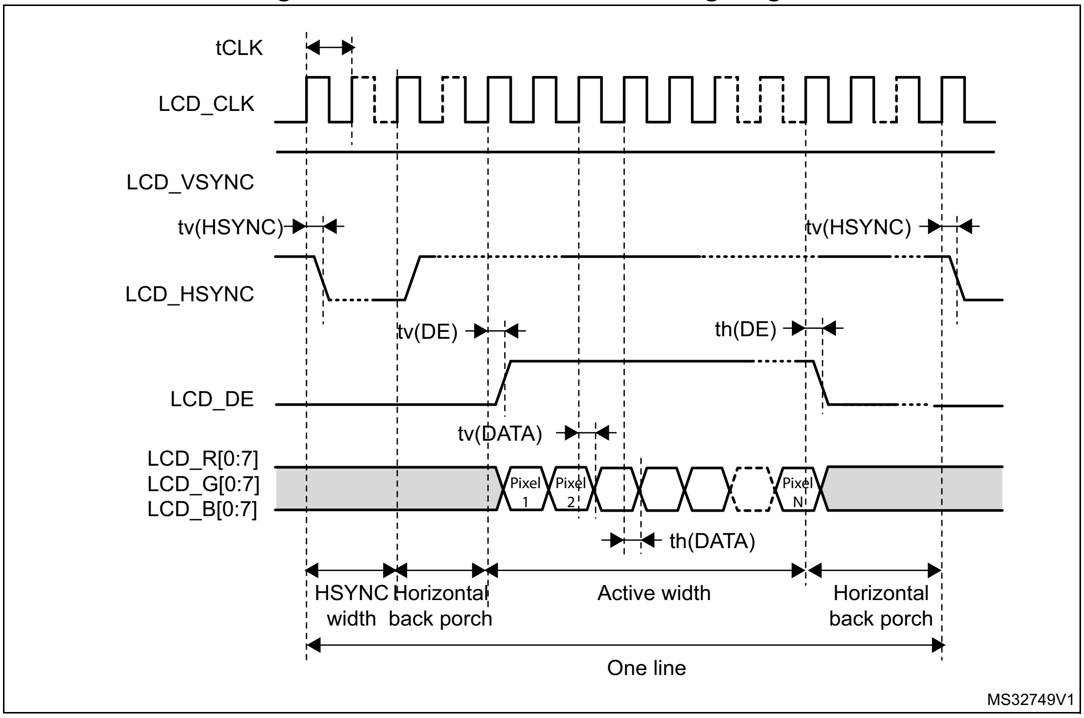
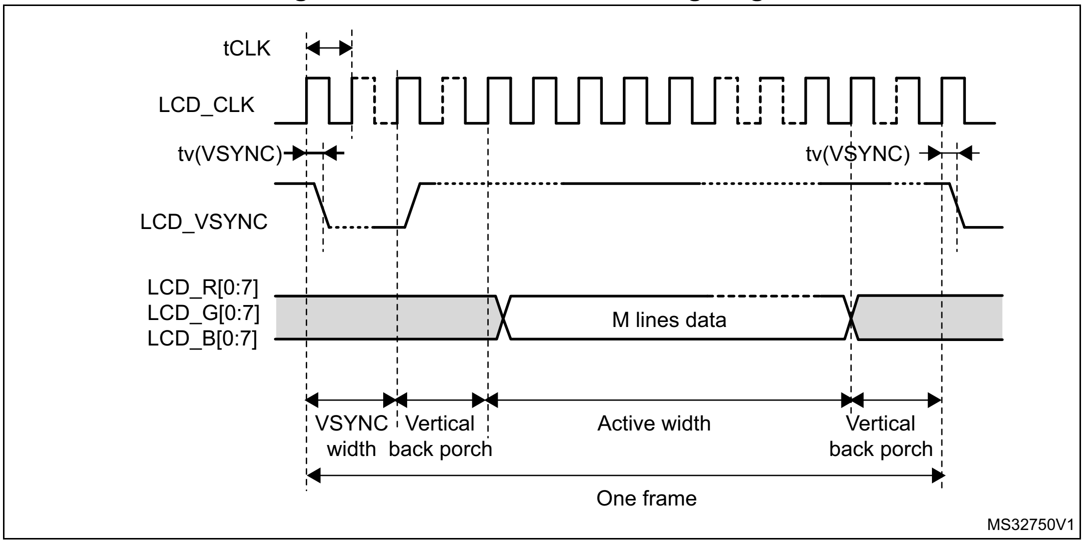



Figure 76. LCD-TFT vertical timing diagram



### 6.3.31 SD/SDIO MMC card host interface (SDMMC) characteristics

Unless otherwise specified, the parameters given in *Table 111* for the SDIO/MMC interface are derived from tests performed under the ambient temperature, $f_{PCLK2}$ frequency and $V_{DD}$ supply voltage conditions summarized in *Table 18*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$

Refer to *Section 6.3.17: I/O port characteristics* for more details on the input/output characteristics.

**Figure 77. SDIO high-speed mode**

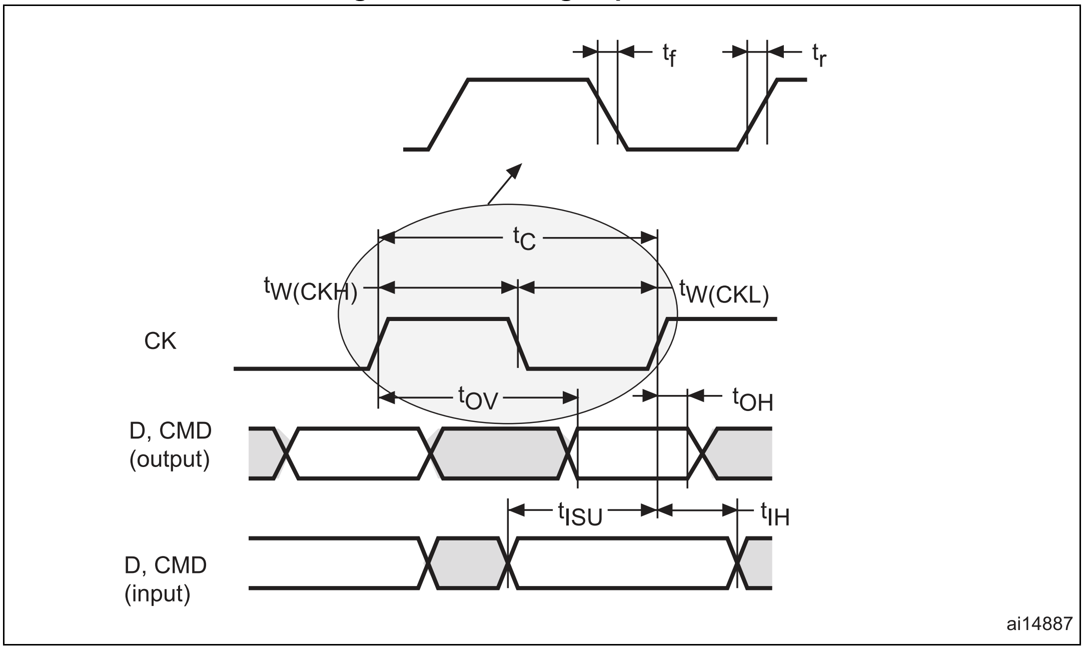



**Figure 78. SD default mode**

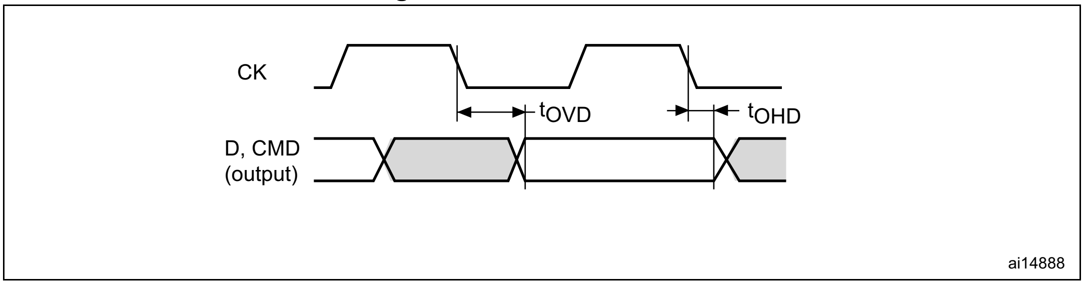


**Table 111. Dynamic characteristics: SD / MMC characteristics, $V_{DD}$=2.7V to 3.6V(1)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{PP}$ | Clock frequency in data transfer mode | - | 0 | - | 50 | MHz |
| - | SDMMC_CK/fPCLK2 frequency ratio | - | - | - | 8/3 | - |
| $t_{W(CKL)}$ | Clock low time | fpp =50 MHz | 9.5 | 10.5 | - | ns |
| $t_{W(CKH)}$ | Clock high time | fpp =50 MHz | 8.5 | 9.5 | - | ns |
| **CMD, D inputs (referenced to CK) in MMC and SD HS mode** | | | | | | |
| $t_{ISU}$ | Input setup time HS | fpp =50 MHz | 2.5 | - | - | ns |
| $t_{IH}$ | Input hold time HS | fpp =50 MHz | 3 | - | - | ns |
| **CMD, D outputs (referenced to CK) in MMC and SD HS mode** | | | | | | |
| $t_{OV}$ | Output valid time HS | fpp =50 MHz | - | 11.5 | 12 | ns |
| $t_{OH}$ | Output hold time HS | fpp =50 MHz | 10.5 | - | - | ns |
| **CMD, D inputs (referenced to CK) in SD default mode** | | | | | | |
| tISUD | Input setup time SD | fpp =25 MHz | 2 | - | - | ns |
| tIHD | Input hold time SD | fpp =25 MHz | 4 | - | - | ns |
| **CMD, D outputs (referenced to CK) in SD default mode** | | | | | | |
| tOVD | Output valid default time SD | fpp =25 MHz | - | 1.5 | 2 | ns |
| tOHD | Output hold default time SD | fpp =25 MHz | 0.5 | - | - | ns |

1. Guaranteed by characterization results,.

**Table 112. Dynamic characteristics: eMMC characteristics, $V_{DD}$=1.71V to 1.9V(1)(2)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{PP}$ | Clock frequency in data transfer mode | - | 0 | - | 50 | MHz |
| - | SDMMC_CK/fPCLK2 frequency ratio | - | - | - | 8/3 | - |
| $t_{W(CKL)}$ | Clock low time | fpp =50 MHz | 9.5 | 10.5 | - | ns |
| $t_{W(CKH)}$ | Clock high time | fpp =50 MHz | 8.5 | 9.5 | - | ns |
| **CMD, D inputs (referenced to CK) in eMMC mode** | | | | | | |
| $t_{ISU}$ | Input setup time HS | fpp =50 MHz | 0.5 | - | - | ns |
| $t_{IH}$ | Input hold time HS | fpp =50 MHz | 3.5 | - | - | ns |
| **CMD, D outputs (referenced to CK) in eMMC mode** | | | | | | |
| $t_{OV}$ | Output valid time HS | fpp =50 MHz | - | 12 | 12.5 | ns |
| $t_{OH}$ | Output hold time HS | fpp =50 MHz | 11 | - | - | ns |

1. Guaranteed by characterization results.
2. Cload = 20 pF.

# 7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

## 7.1 Device marking

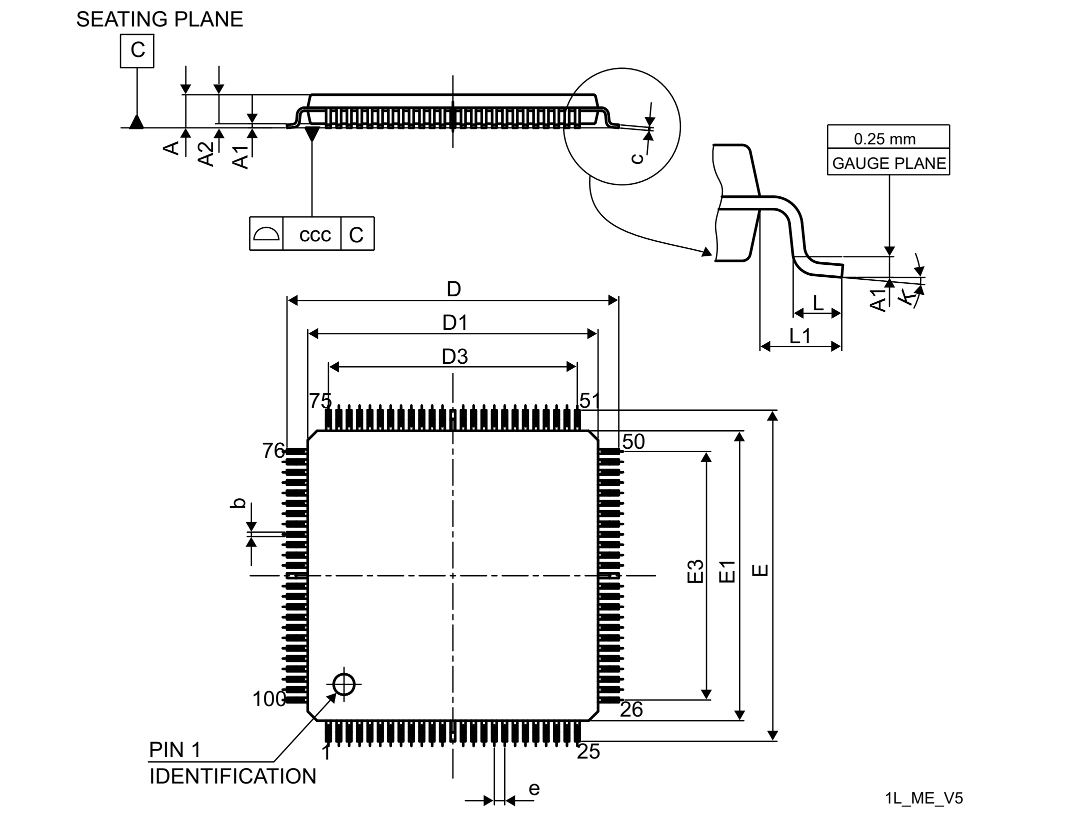
Refer to technical note “Reference device marking schematics for STM32 microcontrollers and microprocessors” (TN1433) available on *www.st.com*, for the location of pin 1 / ball A1 as well as the location and orientation of the marking areas versus pin 1 / ball A1.

Parts marked as “ES”, “E” or accompanied by an engineering sample notification letter, are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

A WLCSP simplified marking example (if any) is provided in the corresponding package information subsection.

## 7.2 LQFP100, 14 x 14 mm low-profile quad flat package information

**Figure 79. LQFP100, 14 x 14 mm 100-pin low-profile quad flat package outline**




1. Drawing is not to scale.

**Table 113. LQPF100, 14 x 14 mm 100-pin low-profile quad flat package mechanical data**

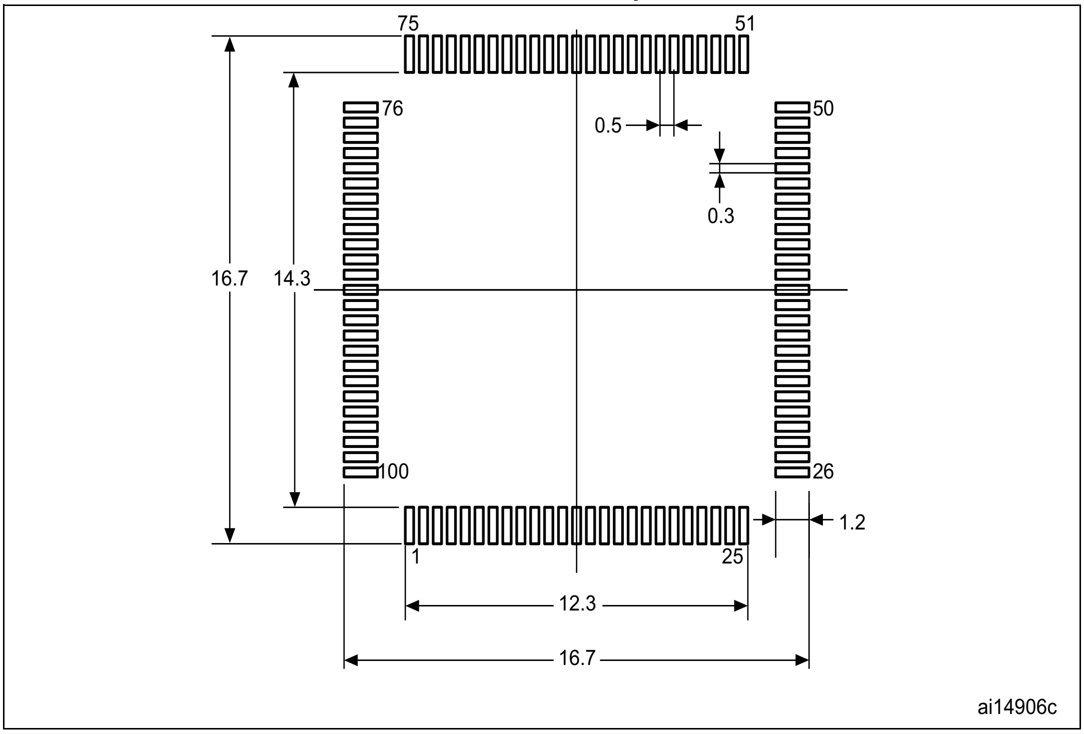
| Symbol | millimeters | | | inches(1) | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | - | - | 1.600 | - | - | 0.0630 |
| A1 | 0.050 | - | 0.150 | 0.0020 | - | 0.0059 |
| A2 | 1.350 | 1.400 | 1.450 | 0.0531 | 0.0551 | 0.0571 |
| b | 0.170 | 0.220 | 0.270 | 0.0067 | 0.0087 | 0.0106 |
| c | 0.090 | - | 0.200 | 0.0035 | - | 0.0079 |
| D | 15.800 | 16.000 | 16.200 | 0.6220 | 0.6299 | 0.6378 |
| D1 | 13.800 | 14.000 | 14.200 | 0.5433 | 0.5512 | 0.5591 |
| D3 | - | 12.000 | - | - | 0.4724 | - |
| E | 15.800 | 16.000 | 16.200 | 0.6220 | 0.6299 | 0.6378 |

**Table 113. LQPF100, 14 x 14 mm 100-pin low-profile quad flat package mechanical data (continued)**

| Symbol | millimeters | | | inches[(1)] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| E1 | 13.800 | 14.000 | 14.200 | 0.5433 | 0.5512 | 0.5591 |
| E3 | - | 12.000 | - | - | 0.4724 | - |
| e | - | 0.500 | - | - | 0.0197 | - |
| L | 0.450 | 0.600 | 0.750 | 0.0177 | 0.0236 | 0.0295 |
| L1 | - | 1.000 | - | - | 0.0394 | - |
| k | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| ccc | - | - | 0.080 | - | - | 0.0031 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

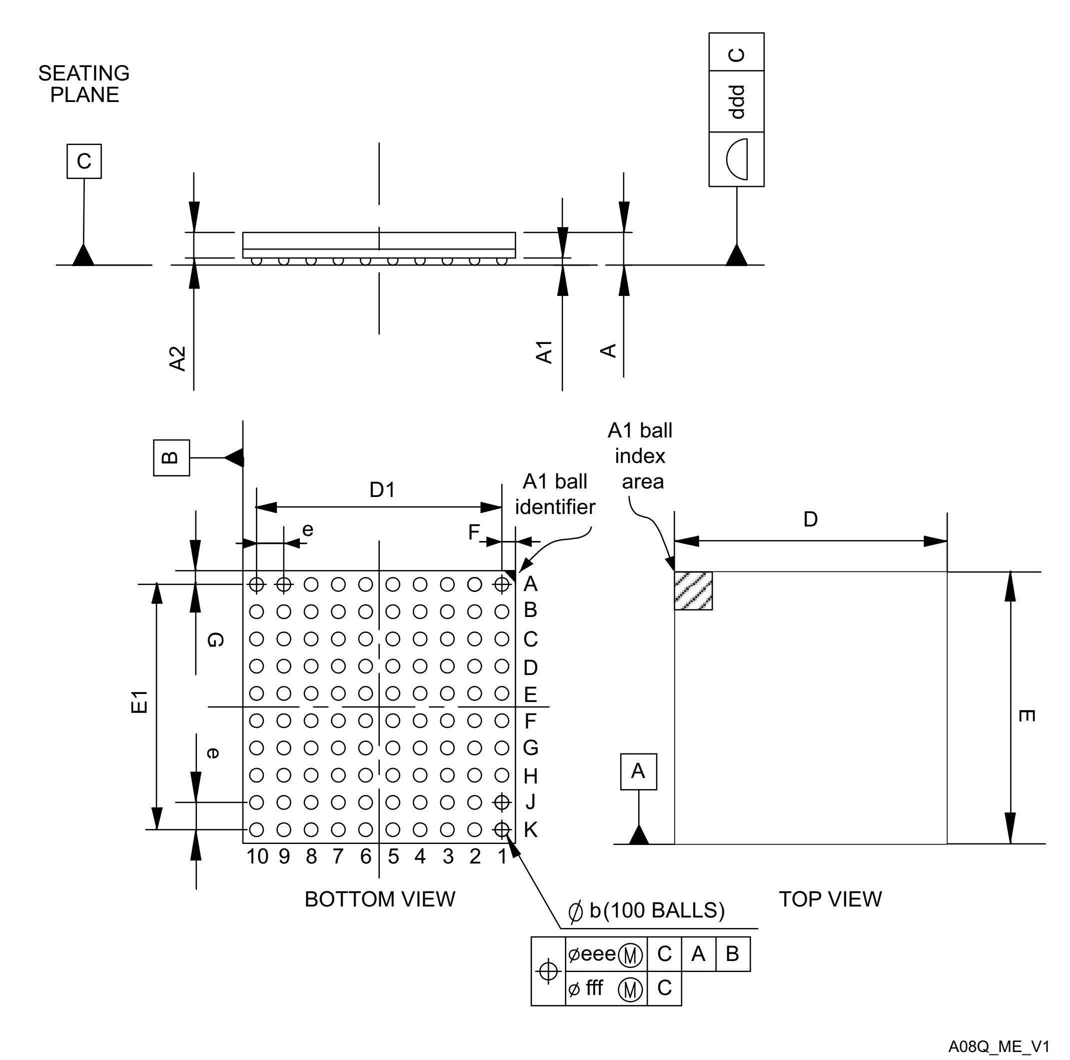
**Figure 80. LQFP100, 14 x 14 mm, 100-pin low-profile quad flat package recommended footprint**




1. Dimensions are expressed in millimeters.

## 7.3 TFBGA100, 8 x 8 x 0.8 mm thin fine-pitch ball grid array package information

**Figure 81. TFBGA100, 8 × 8 × 0.8 mm thin fine-pitch ball grid array package outline**




1. Drawing is not to scale.

**Table 114. TFBGA100, 8 x 8 × 0.8 mm thin fine-pitch ball grid array package mechanical data**

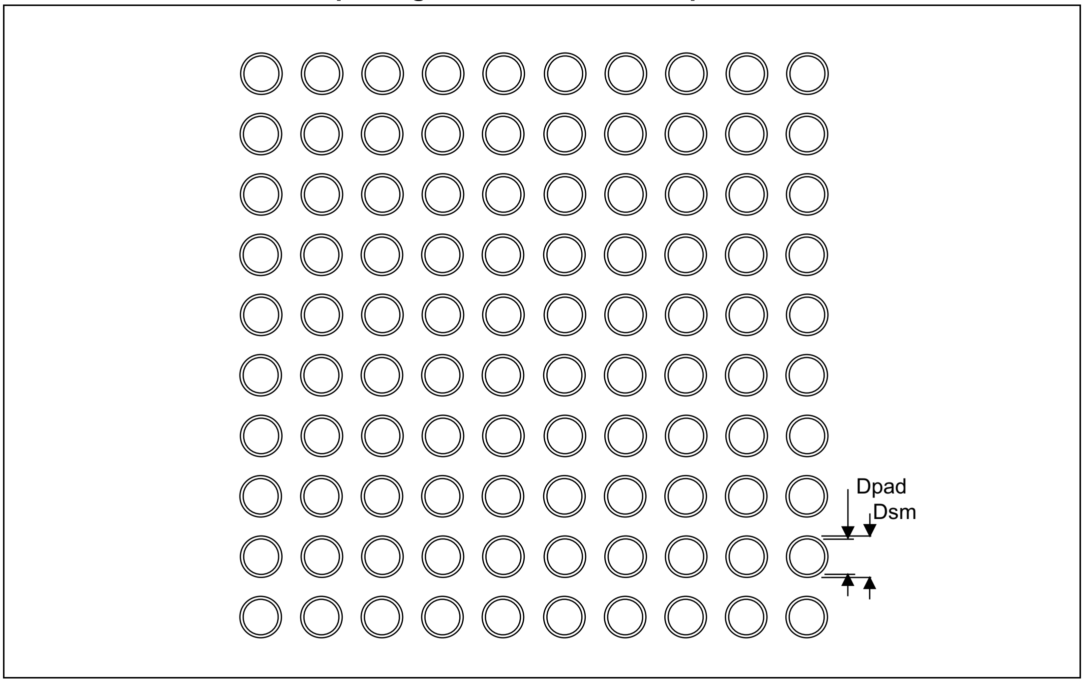
| Symbol | millimeters | | | inches[(1)] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | - | - | 1.100 | - | - | 0.0433 |
| A1 | 0.150 | - | - | 0.0059 | - | - |
| A2 | - | 0.760 | - | - | 0.0299 | - |
| b | 0.350 | 0.400 | 0.450 | 0.0138 | 0.0157 | 0.0177 |

**Table 114. TFBGA100, 8 x 8 × 0.8 mm thin fine-pitch ball grid array package mechanical data (continued)**

| Symbol | millimeters | | | inches(1) | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| D | 7.850 | 8.000 | 8.150 | 0.3091 | 0.3150 | 0.3209 |
| D1 | - | 7.200 | | - | 0.2835 | - |
| E | 7.850 | 8.000 | 8.150 | 0.3091 | 0.3150 | 0.3209 |
| E1 | - | 7.200 | - | - | 0.2835 | - |
| e | - | 0.800 | - | - | 0.0315 | - |
| F | - | 0.400 | - | - | 0.0157 | - |
| G | - | 0.400 | - | - | 0.0157 | - |
| ddd | - | - | 0.100 | - | - | 0.0039 |
| eee | - | - | 0.150 | - | - | 0.0059 |
| fff | - | - | 0.080 | - | - | 0.0031 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

**Figure 82. TFBGA100, 8 x 8 x 0.8 mm thin fine-pitch ball grid array package recommended footprint**



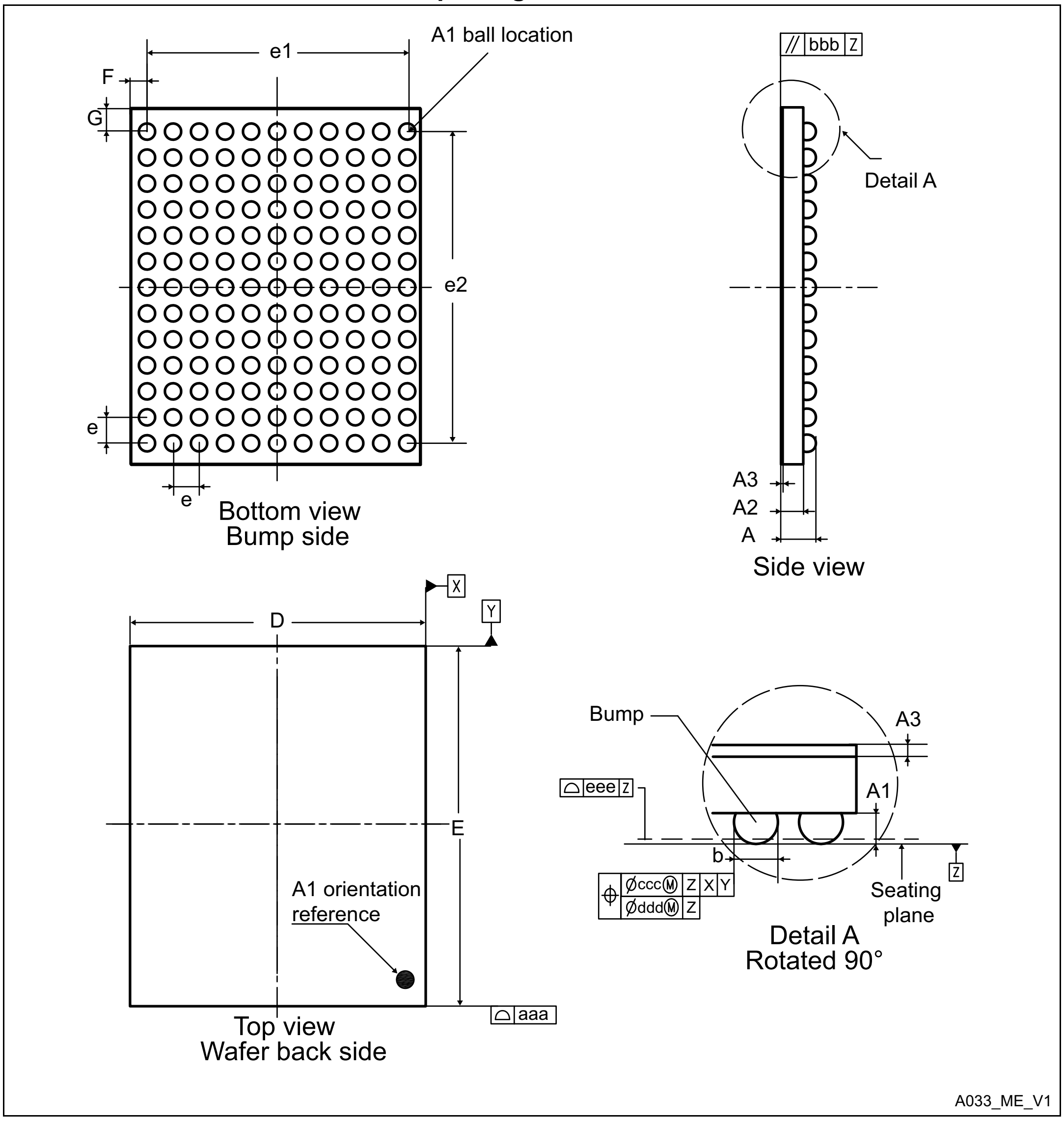

1. Dimensions are expressed in millimeters.

**Table 115. TFBGA100 recommended PCB design rules (0.8 mm pitch BGA)**

| Dimension | Recommended values |
|---|---|
| Pitch | 0.8 |
| Dpad | 0.400 mm |
| Dsm | 0.470 mm typ (depends on the soldermask registration tolerance) |
| Stencil opening | 0.400 mm |
| Stencil thickness | Between 0.100 mm and 0.125 mm |
| Pad trace width | 0.120 mm |

## 7.4 WLCSP143, 4.539x 5.849 mm, 0.4 mm pitch wafer level chip scale package information

**Figure 83. WLCSP143, 4.539x 5.849 mm, 0.4 mm pitch wafer level chip scale package outline**




1. Drawing is not to scale.

**Table 116. WLCSP143, 4.539x 5.849 mm, 0.4 mm pitch wafer level chip scale package mechanical data**

| Symbol | millimeters | | | inches(1) | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | 0.525 | 0.555 | 0.585 | 0.0207 | 0.0219 | 0.0230 |
| A1 | - | 0.175 | - | - | 0.0069 | - |

**Table 116. WLCSP143, 4.539x 5.849 mm, 0.4 mm pitch wafer level chip scale package mechanical data (continued)**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A2 | - | 0.380 | - | - | 0.0150 | - |
| A3[2] | - | 0.025 | - | - | 0.0010 | - |
| b[3] | 0.220 | 0.250 | 0.280 | 0.0087 | 0.0098 | 0.0110 |
| D | 4.504 | 4.539 | 4.574 | 0.1773 | 0.1787 | 0.1801 |
| E | 5.814 | 5.849 | 5.884 | 0.2289 | 0.2303 | 0.2317 |
| e | - | 0.400 | - | - | 0.0157 | - |
| e1 | - | 4.000 | - | - | 0.1575 | - |
| e2 | - | 4.800 | - | - | 0.1890 | - |
| F | - | 0.2695 | - | - | 0.0106 | - |
| G | - | 0.5245 | - | - | 0.0206 | - |
| aaa | - | - | 0.100 | - | - | 0.0039 |
| bbb | - | - | 0.100 | - | - | 0.0039 |
| ccc | - | - | 0.100 | - | - | 0.0039 |
| ddd | - | - | 0.050 | - | - | 0.0020 |
| eee | - | - | 0.050 | - | - | 0.0020 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Back side coating.
3. Dimension is measured at the maximum bump diameter parallel to primary datum Z.

**Figure 84. WLCSP143, 4.539x 5.849 mm, 0.4 mm pitch wafer level chip scale package recommended footprint**

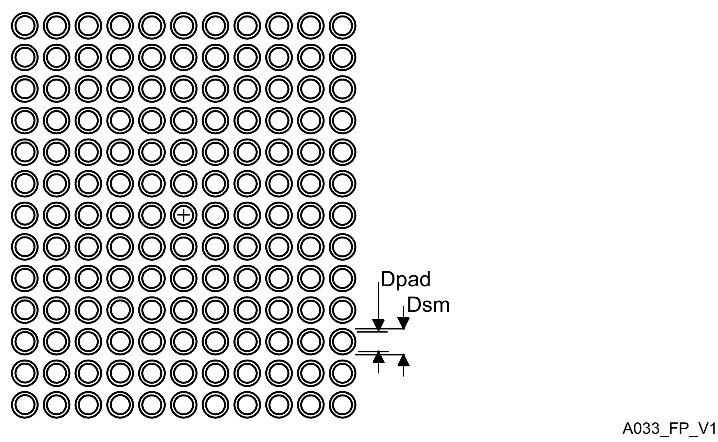


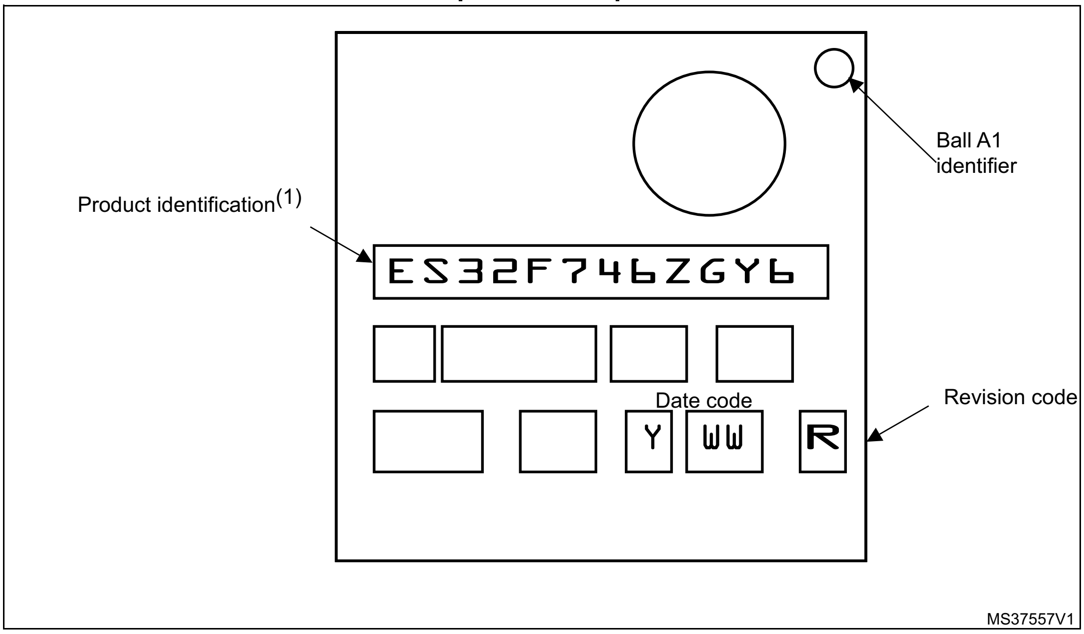
Table 117. WLCSP143 recommended PCB design rules

| Dimension | Recommended values |
|---|---|
| Pitch | 0.4 |
| Dpad | 0.225 mm |
| Dsm | 0.290 mm typ. (depends on the soldermask registration tolerance) |
| Stencil opening | 0.250 mm |
| Stencil thickness | 0.100 mm |

## Marking of engineering samples

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

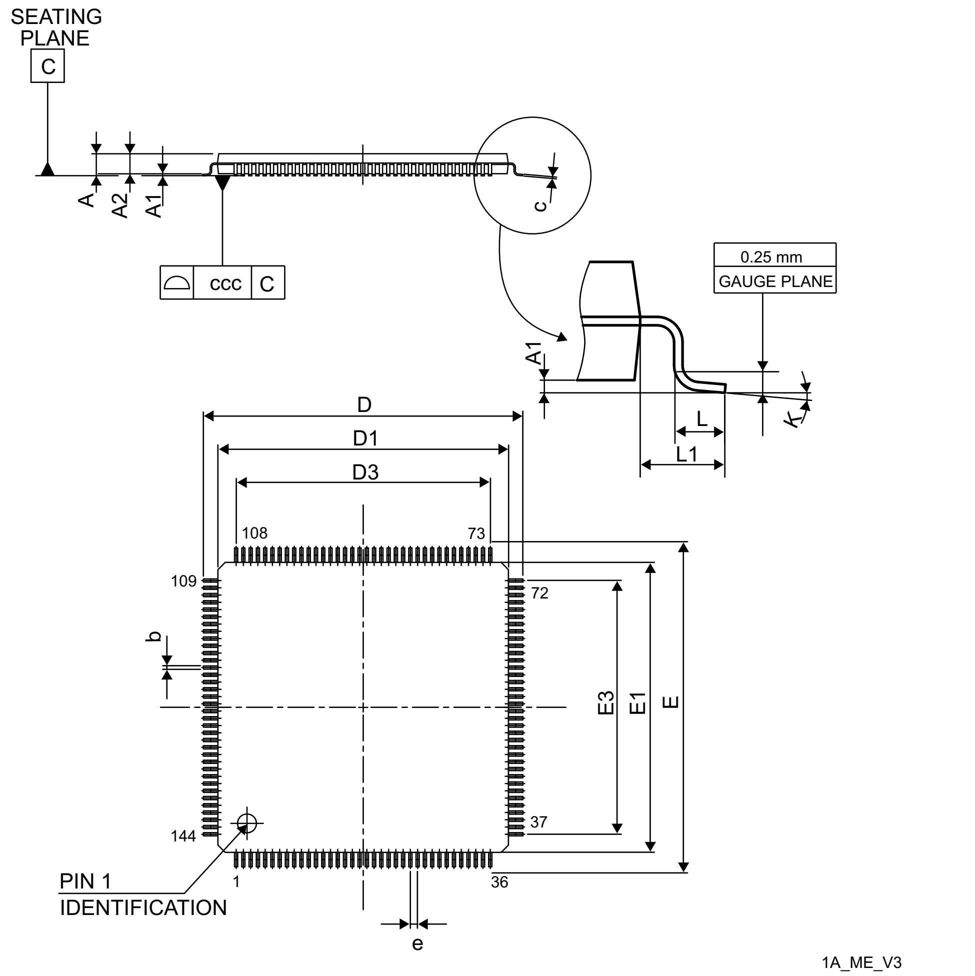
Figure 85. WLCSP143, 0.4 mm pitch wafer level chip scale package top view example




1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

## 7.5 LQFP144, 20 x 20 mm low-profile quad flat package information

**Figure 86. LQFP144, 20 x 20 mm, 144-pin low-profile quad flat package outline**




1. Drawing is not to scale.

**Table 118. LQFP144, 20 x 20 mm, 144-pin low-profile quad flat package mechanical data**

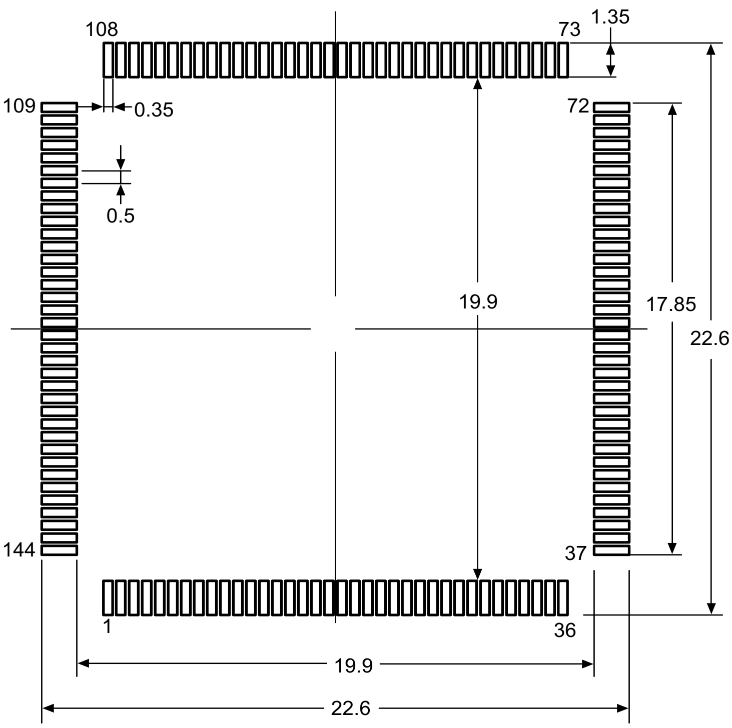
| Symbol | millimeters | | | inches(1) | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | - | - | 1.600 | - | - | 0.0630 |
| A1 | 0.050 | - | 0.150 | 0.0020 | - | 0.0059 |
| A2 | 1.350 | 1.400 | 1.450 | 0.0531 | 0.0551 | 0.0571 |
| b | 0.170 | 0.220 | 0.270 | 0.0067 | 0.0087 | 0.0106 |
| c | 0.090 | - | 0.200 | 0.0035 | - | 0.0079 |
| D | 21.800 | 22.000 | 22.200 | 0.8583 | 0.8661 | 0.874 |

**Table 118. LQFP144, 20 x 20 mm, 144-pin low-profile quad flat package mechanical data (continued)**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| D1 | 19.800 | 20.000 | 20.200 | 0.7795 | 0.7874 | 0.7953 |
| D3 | - | 17.500 | - | - | 0.689 | - |
| E | 21.800 | 22.000 | 22.200 | 0.8583 | 0.8661 | 0.8740 |
| E1 | 19.800 | 20.000 | 20.200 | 0.7795 | 0.7874 | 0.7953 |
| E3 | - | 17.500 | - | - | 0.6890 | - |
| e | - | 0.500 | - | - | 0.0197 | - |
| L | 0.450 | 0.600 | 0.750 | 0.0177 | 0.0236 | 0.0295 |
| L1 | - | 1.000 | - | - | 0.0394 | - |
| k | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| ccc | - | - | 0.080 | - | - | 0.0031 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

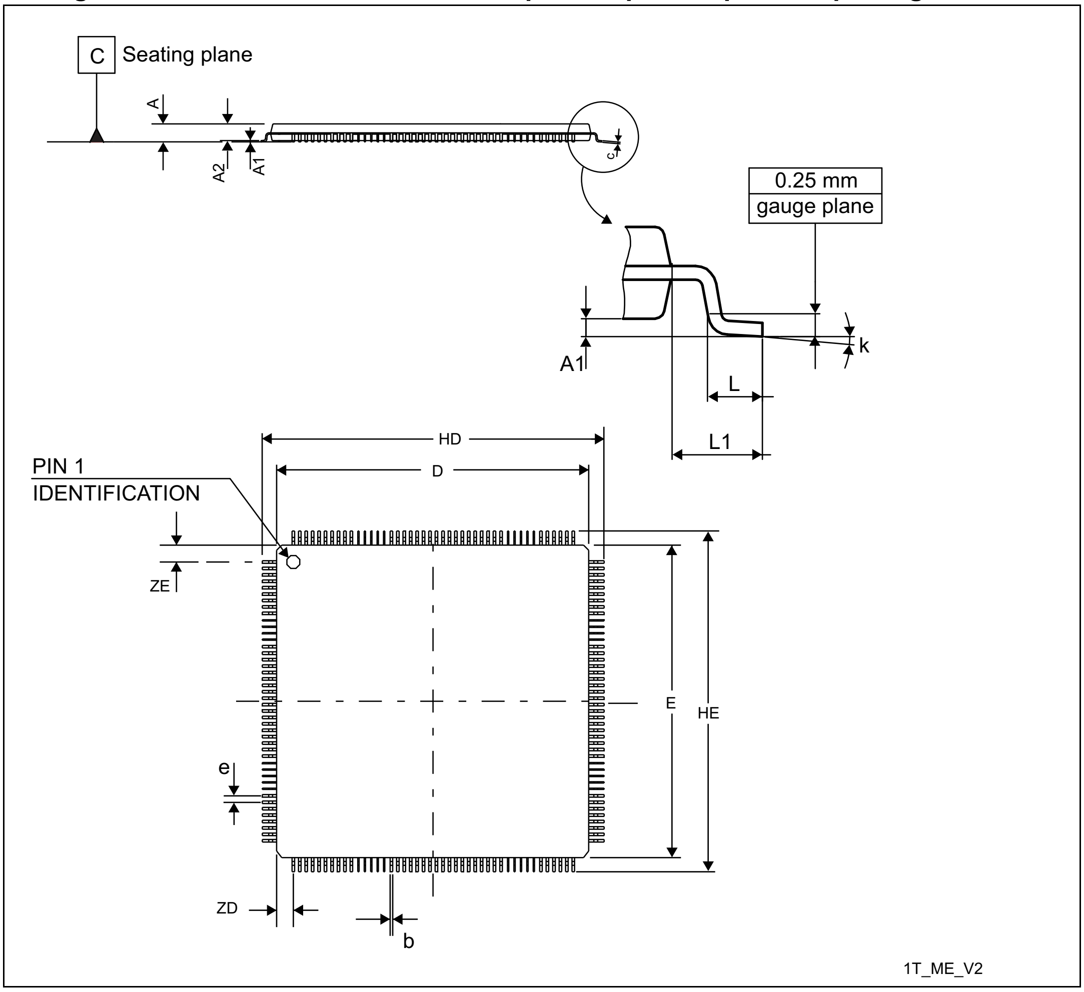
**Figure 87. LQFP144, 20 x 20 mm, 144-pin low-profile quad flat package recommended footprint**




1. Dimensions are expressed in millimeters.

## 7.6 LQFP176, 24 x 24 mm low-profile quad flat package information

**Figure 88. LQFP176, 24 x 24 mm, 176-pin low-profile quad flat package outline**




1. Drawing is not to scale.

**Table 119. LQFP176, 24 x 24 mm, 176-pin low-profile quad flat package mechanical data**

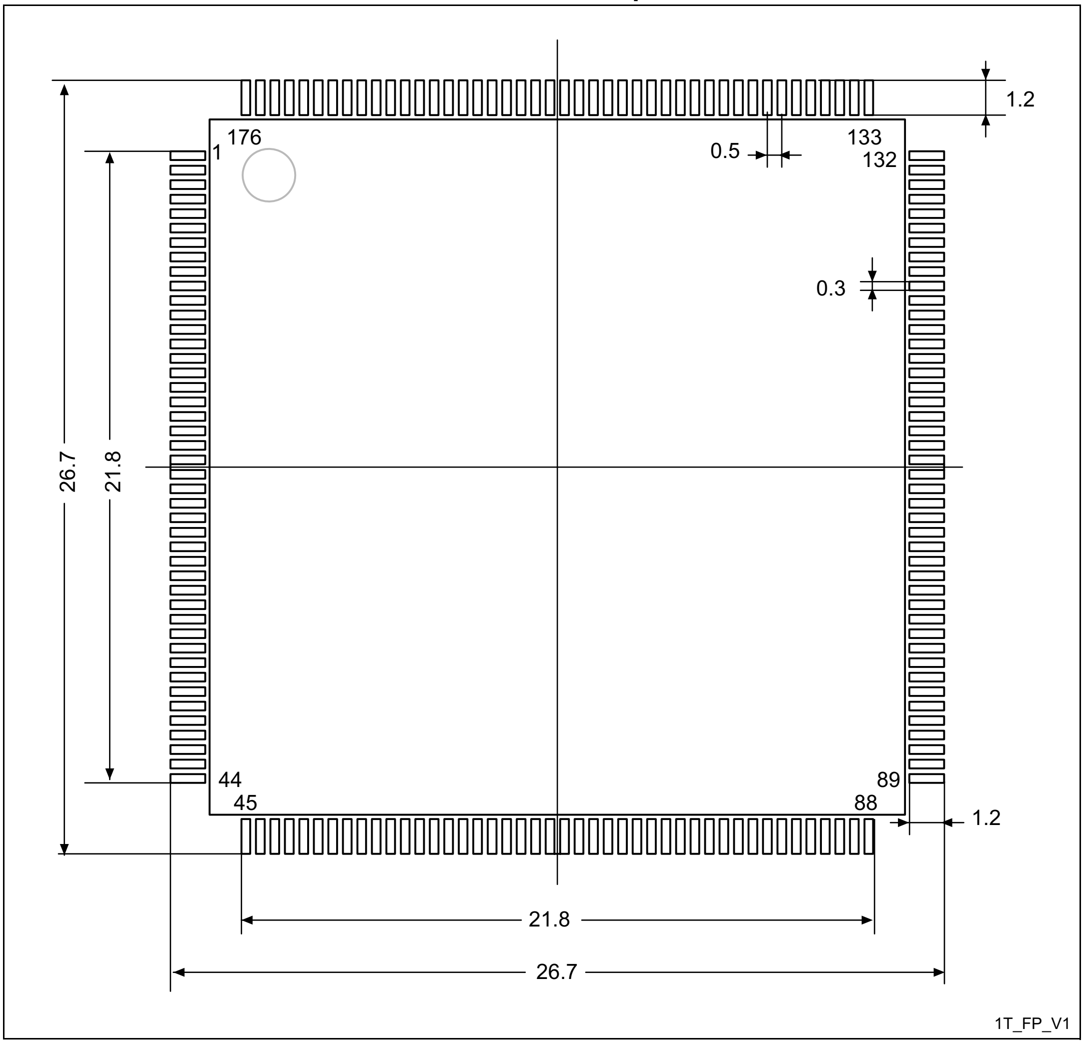
| Symbol | millimeters | | | inches(1) | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | - | - | 1.600 | - | - | 0.0630 |
| A1 | 0.050 | - | 0.150 | 0.0020 | - | 0.0059 |
| A2 | 1.350 | - | 1.450 | 0.0531 | - | 0.0060 |
| b | 0.170 | - | 0.270 | 0.0067 | - | 0.0106 |
| C | 0.090 | - | 0.200 | 0.0035 | - | 0.0079 |
| D | 23.900 | - | 24.100 | 0.9409 | - | 0.9488 |

**Table 119. LQFP176, 24 x 24 mm, 176-pin low-profile quad flat package mechanical data (continued)**

| Symbol | millimeters | | | inches[(1)] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| E | 23.900 | - | 24.100 | 0.9409 | - | 0.9488 |
| e | - | 0.500 | - | - | 0.0197 | - |
| HD | 25.900 | - | 26.100 | 1.0200 | - | 1.0276 |
| HE | 25.900 | - | 26.100 | 1.0200 | - | 1.0276 |
| L | 0.450 | - | 0.750 | 0.0177 | - | 0.0295 |
| L1 | - | 1.000 | - | - | 0.0394 | - |
| ZD | - | 1.250 | - | - | 0.0492 | - |
| ZE | - | 1.250 | - | - | 0.0492 | - |
| ccc | - | - | 0.080 | - | - | 0.0031 |
| k | 0 ° | - | 7 ° | 0 ° | - | 7 ° |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

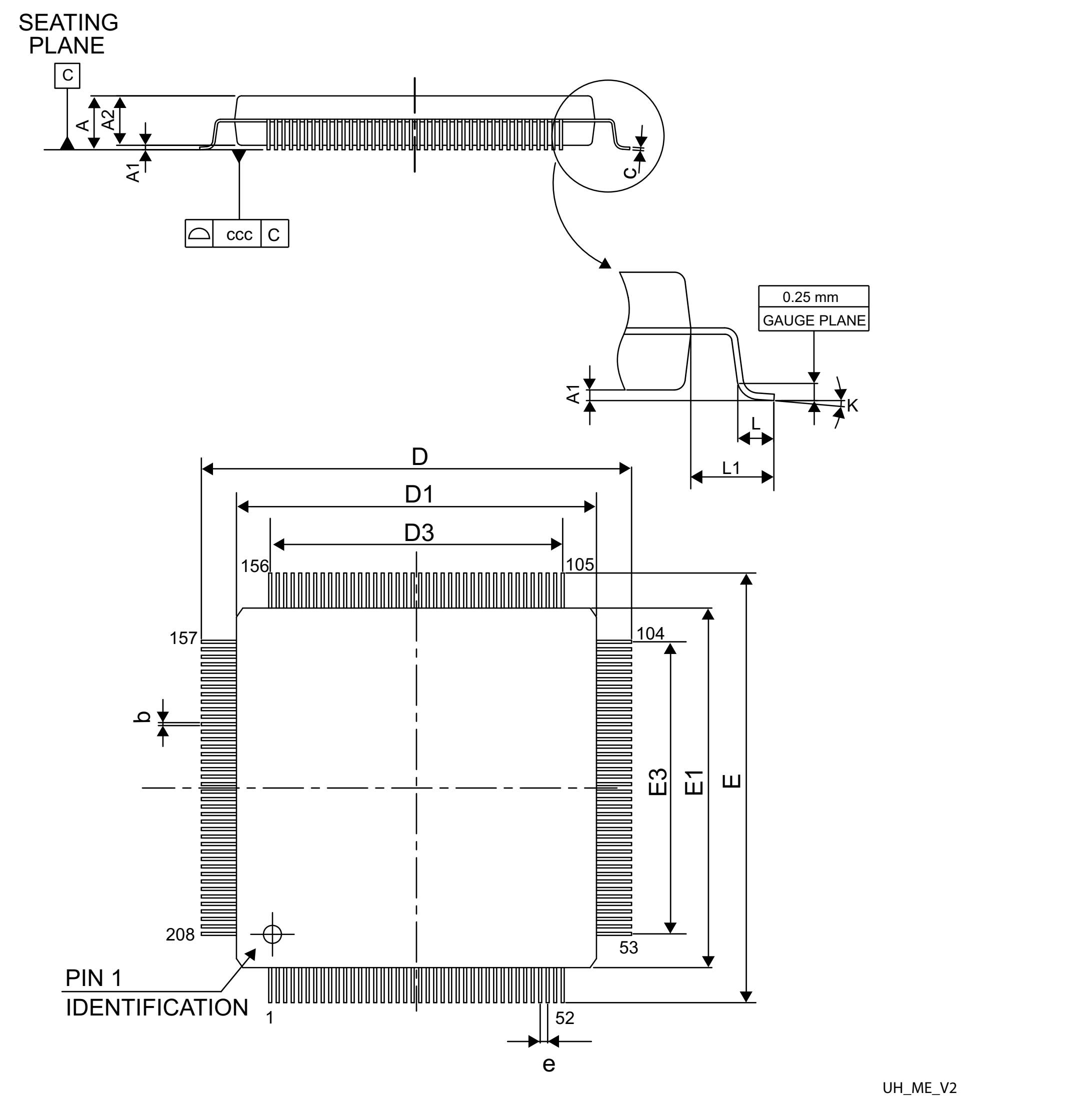
**Figure 89. LQFP176, 24 x 24 mm, 176-pin low-profile quad flat package recommended footprint**




1. Dimensions are expressed in millimeters.

## 7.7 LQFP208, 28 x 28 mm low-profile quad flat package information

**Figure 90. LQFP208, 28 x 28 mm, 208-pin low-profile quad flat package outline**




1. Drawing is not to scale.

**Table 120. LQFP208, 28 x 28 mm, 208-pin low-profile quad flat package mechanical data**

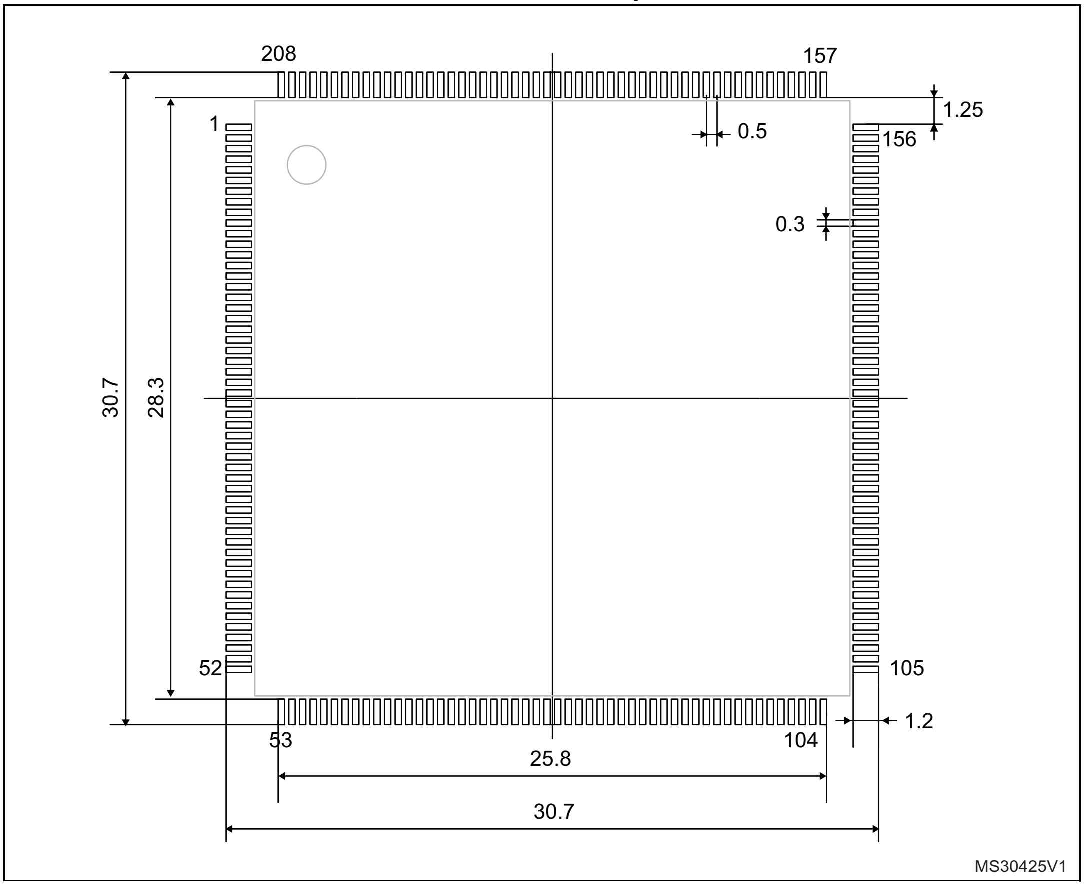
| Symbol | millimeters | | | inches(1) | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | - | - | 1.600 | -- | - | 0.0630 |
| A1 | 0.050 | - | 0.150 | 0.0020 | - | 0.0059 |
| A2 | 1.350 | 1.400 | 1.450 | 0.0531 | 0.0551 | 0.0571 |

Table 120. LQFP208, 28 x 28 mm, 208-pin low-profile quad flat package mechanical data (continued)

| Symbol | millimeters | | | inches(1) | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| b | 0.170 | 0.220 | 0.270 | 0.0067 | 0.0087 | 0.0106 |
| c | 0.090 | - | 0.200 | 0.0035 | - | 0.0079 |
| D | 29.800 | 30.000 | 30.200 | 1.1732 | 1.1811 | 1.1890 |
| D1 | 27.800 | 28.000 | 28.200 | 1.0945 | 1.1024 | 1.1102 |
| D3 | - | 25.500 | - | - | 1.0039 | - |
| E | 29.800 | 30.000 | 30.200 | 1.1732 | 1.1811 | 1.1890 |
| E1 | 27.800 | 28.000 | 28.200 | 1.0945 | 1.1024 | 1.1102 |
| E3 | - | 25.500 | - | - | 1.0039 | - |
| e | - | 0.500 | - | - | 0.0197 | - |
| L | 0.450 | 0.600 | 0.750 | 0.0177 | 0.0236 | 0.0295 |
| L1 | - | 1.000 | - | - | 0.0394 | - |
| k | 0° | 3.5° | 7.0° | 0° | 3.5° | 7.0° |
| ccc | - | - | 0.080 | - | - | 0.0031 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

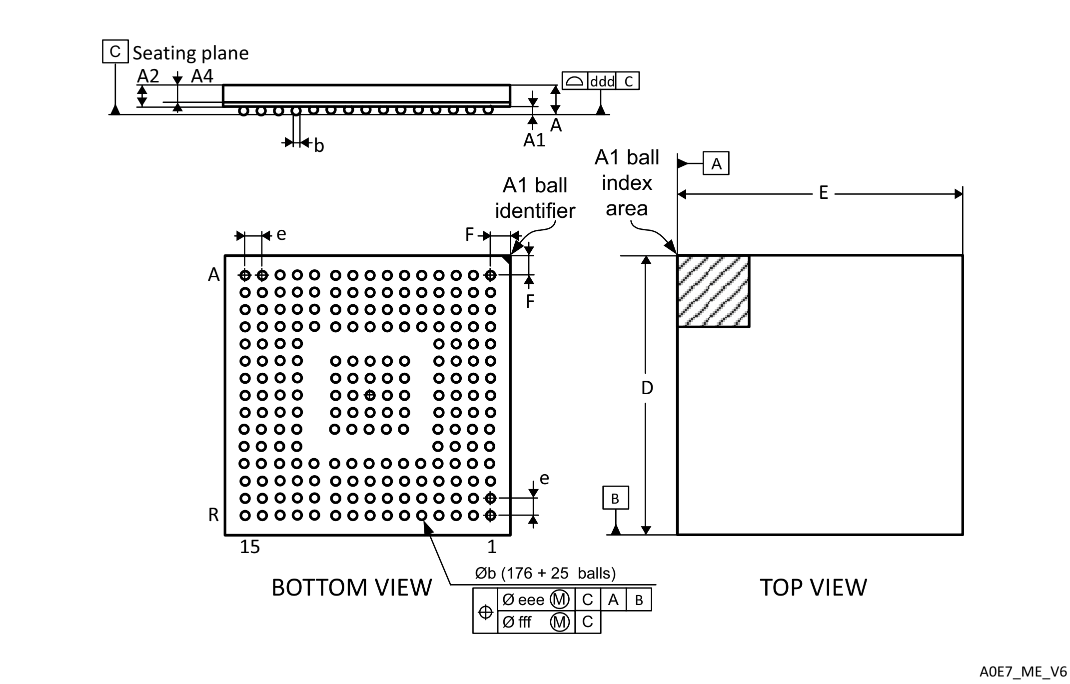
**Figure 91. LQFP208, 28 x 28 mm, 208-pin low-profile quad flat package recommended footprint**




1. Dimensions are expressed in millimeters.

## 7.8 UFBGA 176+25, 10 x 10 x 0.65 mm ultra thin-pitch ball grid array package information

**Figure 92. UFBGA 176+25, 10 × 10 × 0.65 mm ultra thin fine-pitch ball grid array package outline**




1. Drawing is not to scale.

**Table 121. UFBGA 176+25, 10 × 10 × 0.65 mm ultra thin fine-pitch ball grid array package mechanical data**

| Symbol | millimeters | | | inches[(1)] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | 0.460 | 0.530 | 0.600 | 0.0181 | 0.0209 | 0.0236 |
| A1 | 0.050 | 0.080 | 0.110 | 0.002 | 0.0031 | 0.0043 |
| A2 | 0.400 | 0.450 | 0.500 | 0.0157 | 0.0177 | 0.0197 |
| b | 0.230 | 0.280 | 0.330 | 0.0091 | 0.0110 | 0.0130 |
| D | 9.950 | 10.000 | 10.050 | 0.3917 | 0.3937 | 0.3957 |
| E | 9.950 | 10.000 | 10.050 | 0.3917 | 0.3937 | 0.3957 |
| e | - | 0.650 | - | - | 0.0256 | - |
| F | 0.400 | 0.450 | 0.500 | 0.0157 | 0.0177 | 0.0197 |
| ddd | - | - | 0.080 | - | - | 0.0031 |
| eee | - | - | 0.150 | - | - | 0.0059 |
| fff | - | - | 0.080 | - | - | 0.0031 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 93. UFBGA176+25, 10 x 10 x 0.65 mm, ultra fine-pitch ball grid array package recommended footprint

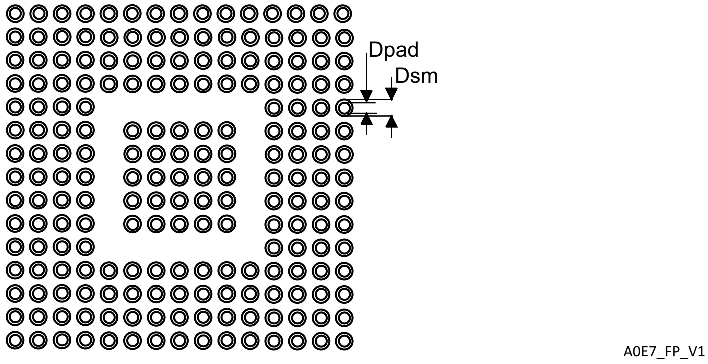
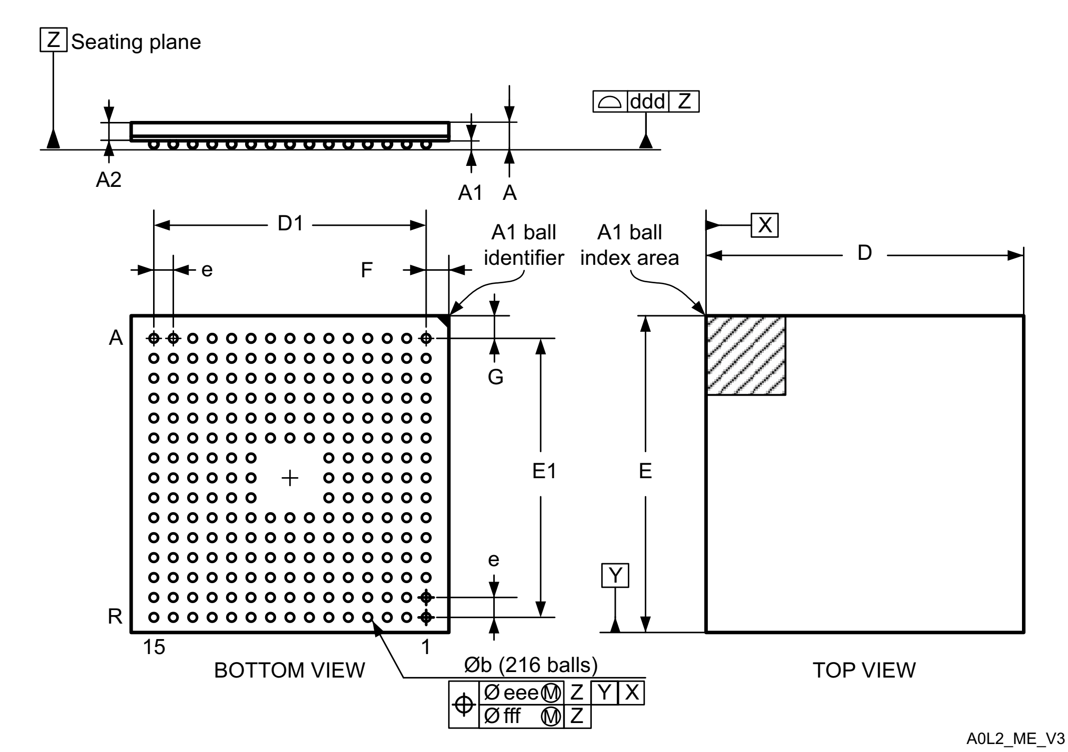



Table 122. UFBGA176+25 recommended PCB design rules (0.65 mm pitch BGA)

| Dimension | Recommended values |
|---|---|
| Pitch | 0.65 mm |
| Dpad | 0.300 mm |
| Dsm | 0.400 mm typ. (depends on the soldermask registration tolerance) |
| Stencil opening | 0.300 mm |
| Stencil thickness | Between 0.100 mm and 0.125 mm |
| Pad trace width | 0.100 mm |

## 7.9 TFBGA216, 13 × 13 × 0.8 mm thin fine-pitch ball grid array package information

**Figure 94. TFBGA216, 13 × 13 × 0.8 mm thin fine-pitch ball grid array package outline**




1. Drawing is not to scale.

**Table 123. TFBGA216, 13 × 13 × 0.8 mm thin fine-pitch ball grid array package mechanical data**

| Symbol | millimeters | | | inches(1) | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | - | - | 1.100 | - | - | 0.0433 |
| A1 | 0.150 | - | - | 0.0059 | - | - |
| A2 | - | 0.760 | - | - | 0.0299 | - |
| b | 0.350 | 0.400 | 0.450 | 0.0138 | 0.0157 | 0.0177 |
| D | 12.850 | 13.000 | 13.150 | 0.5118 | 0.5118 | 0.5177 |
| D1 | - | 11.200 | - | - | 0.4409 | - |
| E | 12.850 | 13.000 | 13.150 | 0.5118 | 0.5118 | 0.5177 |
| E1 | - | 11.200 | - | - | 0.4409 | - |
| e | - | 0.800 | - | - | 0.0315 | - |
| F | - | 0.900 | - | - | 0.0354 | - |

Table 123. TFBGA216, 13 × 13 × 0.8 mm thin fine-pitch ball grid array package mechanical data (continued)

| Symbol | millimeters | | | inches[(1)] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| G | - | 0.900 | - | - | 0.0354 | - |
| ddd | - | - | 0.100 | - | - | 0.0039 |
| eee | - | - | 0.150 | - | - | 0.0059 |
| fff | - | - | 0.080 | - | - | 0.0031 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 95. TFBGA216, 13 x 13 x 0.8 mm thin fine-pitch ball grid array package recommended footprint

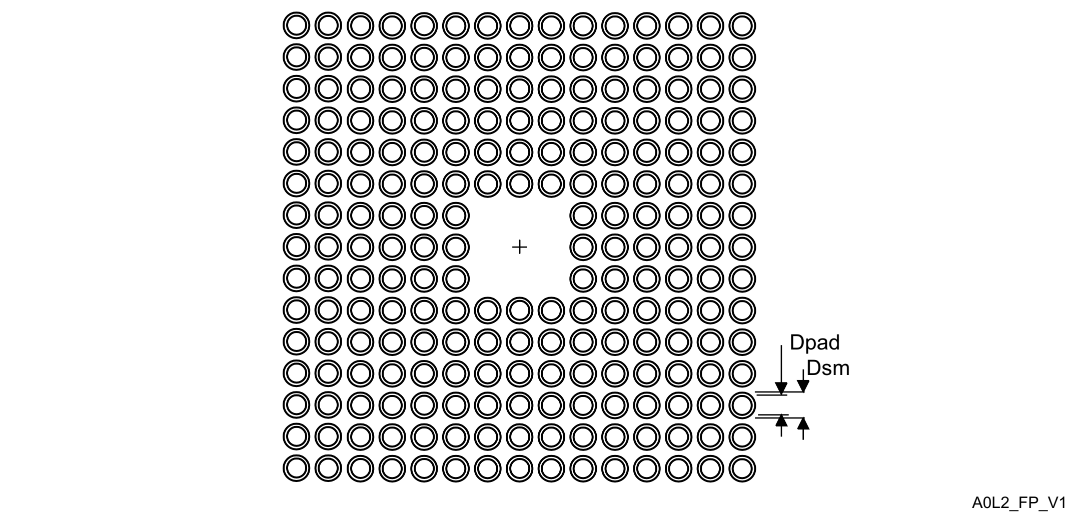



Table 124. TFBGA216 recommended PCB design rules (0.8 mm pitch BGA)

| Dimension | Recommended values |
|---|---|
| Pitch | 0.8 |
| Dpad | 0.400 mm |
| Dsm | 0.470 mm typ. (depends on the soldermask registration tolerance) |
| Stencil opening | 0.400 mm |
| Stencil thickness | Between 0.100 mm and 0.125 mm |
| Pad trace width | 0.120 mm |

1.

## 7.10 Thermal characteristics

The maximum chip-junction temperature, $T_J$ max, in degrees Celsius, may be calculated using the following equation:

$T_J$ max = $T_A$ max + ($P_D$ max x $\Theta_{JA}$)

Where:

- $T_A$ max is the maximum ambient temperature in °C,
- $\Theta_{JA}$ is the package junction-to-ambient thermal resistance, in °C/W,
- $P_D$ max is the sum of $P_{INT}$ max and $P_{I/O}$ max ($P_D$ max = $P_{INT}$ max + $P_{I/O}$max),
- $P_{INT}$ max is the product of $I_{DD}$ and $V_{DD}$, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$P_{I/O}$ max = $\Sigma$ ($V_{OL}$ × $I_{OL}$) + $\Sigma$(($V_{DD}$ – $V_{OH}$) × $I_{OH}$),

taking into account the actual $V_{OL}$ / $I_{OL}$ and $V_{OH}$ / $I_{OH}$ of the I/Os at low and high level in the application.

**Table 125. Package thermal characteristics**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $\Theta_{JA}$ | **Thermal resistance junction-ambient** LQFP100 - 14 × 14 mm / 0.5 mm pitch | 43 | °C/W |
| | **Thermal resistance junction-ambient** TFBGA100 - 8 × 8 mm / 0.8 mm pitch | 57 | |
| | **Thermal resistance junction-ambient** WLCSP143 | 31.2 | |
| | **Thermal resistance junction-ambient** LQFP144 - 20 × 20 mm / 0.5 mm pitch | 40 | |
| | **Thermal resistance junction-ambient** LQFP176 - 24 × 24 mm / 0.5 mm pitch | 38 | |
| | **Thermal resistance junction-ambient** LQFP208 - 28 × 28 mm / 0.5 mm pitch | 19 | |
| | **Thermal resistance junction-ambient** UFBGA176 - 10 × 10 mm / 0.65 mm pitch | 39 | |
| | **Thermal resistance junction-ambient** TFBGA216 - 13 × 13 mm / 0.8 mm pitch | 29 | |

### Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org.

# 8 Ordering information

**Table 126. Ordering information scheme**

Example: STM32 F 746 V G T 6 xxx

**Device family**

STM32 = ARM-based 32-bit microcontroller

**Product type**

F = general-purpose

**Device subfamily**

745= STM32F745xx, USB OTG FS/HS, camera interface Ethernet
746= STM32F746xx, USB OTG FS/HS, camera interface, Ethernet, LCD-TFT

**Pin count**

V = 100 pins

Z = 143 and 144 pins

I = 176 pins

B = 208 pins

N = 216 pins

**Flash memory size**

E = 512 Kbytes of Flash memory

G = 1024 Kbytes of Flash memory

**Package**

T = LQFP

K = UFBGA

H = TFBGA

Y = WLCSP

**Temperature range**

6 = Industrial temperature range, –40 to 85 °C.

7 = Industrial temperature range, –40 to 105 °C.(1)

**Options**

xxx = programmed parts

TR = tape and reel

1. Not available for WLCSP packages.

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.

# Appendix A Recommendations when using internal reset OFF

When the internal reset is OFF, the following integrated features are no longer supported:

- The integrated power-on reset (POR) / power-down reset (PDR) circuitry is disabled.
- The brownout reset (BOR) circuitry must be disabled.
- The embedded programmable voltage detector (PVD) is disabled.
- $V_{BAT}$ functionality is no more available and VBAT pin should be connected to $V_{DD}$.
- The over-drive mode is not supported.

## A.1 Operating conditions

**Table 127. Limitations depending on the operating power supply range**

| Operating power supply range | ADC operation | Maximum Flash memory access frequency with no wait states ($f_{Flashmax}$) | Maximum Flash memory access frequency with wait states (1)(2) | I/O operation | Possible Flash memory operations |
|---|---|---|---|---|---|
| $V_{DD}$ =1.7 to 2.1 V(3) | Conversion time up to 1.2 Msps | 20 MHz | 180 MHz with 8 wait states and over-drive OFF | – No I/O compensation | 8-bit erase and program operations only |

1. Applicable only when the code is executed from Flash memory. When the code is executed from RAM, no wait state is required.
2. Thanks to the ART accelerator on ITCM interface and L1-cache on AXI interface, the number of wait states given here does not impact the execution speed from the Flash memory since the ART accelerator or L1-cache allows to achieve a performance equivalent to 0-wait state program execution.
3. $V_{DD}/V_{DDA}$ minimum value of 1.7 V, with the use of an external power supply supervisor (refer to *Section 3.17.1: Internal reset ON*).

# 9 Important security notice

The STMicroelectronics group of companies (ST) places a high value on product security, which is why the ST product(s) identified in this documentation may be certified by various security certification bodies and/or may implement our own security measures as set forth herein. However, no level of security certification and/or built-in security measures can guarantee that ST products are resistant to all forms of attacks. As such, it is the responsibility of each of ST's customers to determine if the level of security provided in an ST product meets the customer needs both in relation to the ST product alone, as well as when combined with other components and/or software for the customer end product or application. In particular, take note that:

- ST products may have been certified by one or more security certification bodies, such as Platform Security Architecture (www.psacertified.org) and/or Security Evaluation standard for IoT Platforms (www.trustcb.com). For details concerning whether the ST product(s) referenced herein have received security certification along with the level and current status of such certification, either visit the relevant certification standards website or go to the relevant product page on www.st.com for the most up to date information. As the status and/or level of security certification for an ST product can change from time to time, customers should re-check security certification status/level as needed. If an ST product is not shown to be certified under a particular security standard, customers should not assume it is certified.
- Certification bodies have the right to evaluate, grant and revoke security certification in relation to ST products. These certification bodies are therefore independently responsible for granting or revoking security certification for an ST product, and ST does not take any responsibility for mistakes, evaluations, assessments, testing, or other activity carried out by the certification body with respect to any ST product.
- Industry-based cryptographic algorithms (such as AES, DES, or MD5) and other open standard technologies which may be used in conjunction with an ST product are based on standards which were not developed by ST. ST does not take responsibility for any flaws in such cryptographic algorithms or open technologies or for any methods which have been or may be developed to bypass, decrypt or crack such algorithms or technologies.
- While robust security testing may be done, no level of certification can absolutely guarantee protections against all attacks, including, for example, against advanced attacks which have not been tested for, against new or unidentified forms of attack, or against any form of attack when using an ST product outside of its specification or intended use, or in conjunction with other components or software which are used by customer to create their end product or application. ST is not responsible for resistance against such attacks. As such, regardless of the incorporated security features and/or any information or support that may be provided by ST, each customer is solely responsible for determining if the level of attacks tested for meets their needs, both in relation to the ST product alone and when incorporated into a customer end product or application.
- All security features of ST products (inclusive of any hardware, software, documentation, and the like), including but not limited to any enhanced security features added by ST, are provided on an "AS IS" BASIS. AS SUCH, TO THE EXTENT PERMITTED BY APPLICABLE LAW, ST DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, unless the applicable written and signed contract terms specifically provide otherwise.

# Revision history

**Table 128. Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 26-May-2015 | 1 | Initial release. |
| 20-Oct-2015 | 2 | Updated *Table 55: ESD absolute maximum ratings* adding packages.<br>Updated note of *Table 34: Typical and maximum current consumptions in Standby mode*.<br>Updated *Figure 11: STM32F750V8 LQFP100 pinout* replacing PB13 and PB14 by PE13 and PE14.<br>Updated *Table 53: EMS characteristics* replacing 168 MHz by 216 MHz.<br>Updated *Section 3.9: Quad-SPI memory interface (QUADSPI)* removing ‘STM32F75xx’.<br>Updated *Section 3.22.2: General-purpose timers (TIMx)* and *Section 3.44: Embedded Trace Macrocell™* modifying STM32F756xx by STM32F74xxx.<br>Updated *Section 3.1: ARM® Cortex®-M7 with FPU* modifying STM32F756xx family by STM32F745xx and STM32F746xx devices.<br>Removed Table 86. Ethernet DC electrical characteristics.<br>Updated all the notes removing ‘not tested in production’.<br>Updated *Table 45: Main PLL characteristics*, *Table 46: PLLI2S characteristics* and *Table 47: PLLISAI characteristics* fVCO_OUT output at min value ‘100’ and VCO freq at 100 MHz.<br>Updated *Table 15: STM32F750x8 register boundary addresses* replacing cortex-M4 by Cortex-M7.<br>Updated *Table 89: Dynamics characteristics: Ethernet MAC signals for MII* td (TXEN) and td (TXD) min value at 6.5 ns. |
| 10-Dec-2015 | 3 | Updated *Table 11: STM32F750x8 pin and ball definition* additional functions column: WKUP1, 2, 3, 4, 5, 6 must be respectively PA0, PA2, PC1, PC13, PI8, PI11.<br>Updated *Table 64: ADC characteristics* adding $V_{REF-}$ negative voltage reference.<br>Update *Table 16: Voltage characteristics* adding table note 3.<br>Updated *Table 71: Temperature sensor calibration values* memory addresses.<br>Updated *Table 74: Internal reference voltage calibration values* memory addresses. |

**Table 128. Document revision history (continued)**

| Date | Revision | Changes |
|---|---|---|
| 18-Feb-2016 | 4 | Updated *Table 54: EMI characteristics* modifying 25/180 MHz by 25/200 MHz.<br>Updated *Figure 13: STM32F756ZxSTM32F74xZx WLCSP143 ballout*.<br>Added TFBGA100 8 x 8 mm package:<br>– Updated Cover page.<br>– Updated *Section 1: Introduction*.<br>– Updated *Table 4: STM32F750x8 features and peripheral counts*.<br>– Updated *Table 6: Regulator ON/OFF and internal reset ON/OFF availability*.<br>– Updated *Section 4: Pinouts and pin description* adding *Figure 12: STM32F756VxSTM32F74xVx TFBGA100 ballout* and adding TFBGA100 ball description in *Table 11: STM32F750x8 pin and ball definition*.<br>– Updated *Table 19: General operating conditions*.<br>– Updated *Table 55: ESD absolute maximum ratings*.<br>– Updated notes below *Figure 38* and *Figure 39*.<br>– Updated *Section 7: Package information* adding TFBGA100 package information and adding thermal resistance in *Table 126: Package thermal characteristics*.<br>– Updated *Table 11: STM32F750x8 pin and ball definition* note 5.<br>Updated *Table 37: Peripheral current consumption* peripheral consumption on APB1 and APB2.<br>Updated *Figure 13: STM32F750N8 TFBGA216 ballout*. |
| 23-Jul-2025 | 5 | Updated:<br>– Features<br>– *Chapter 1: Introduction*<br>– *Table 2: STM32F745xx and STM32F746xx features and peripheral counts*<br>– *Chapter 3.37: True Random number generator (RNG)*<br>– *Section Table 10.: STM32F745xx and STM32F746xx pin and ball definition*<br>– *Section Table 23.: Reset and power control block characteristics*<br>– *Section 6.3.7: Supply current characteristics*<br>– *Table 42: HSI oscillator characteristics*<br>– *Table 53: EMI characteristics*<br>– *Section 6.3.17: I/O port characteristics*<br>– *Figure 39: I/O AC characteristics definition*<br>– *Figure 41: ADC accuracy characteristics*<br>– *Figure 42: Typical connection diagram using the ADC*<br>– *Figure 66: NAND controller waveforms for read access*<br>– *Figure 67: NAND controller waveforms for write access*<br>– *Section 8: Ordering information* |