ADA University, School of IT and Engineering

ENCE 2301 – Digital Logic Design

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Schedule: **Monday / Wednesday 13:00 - 14:15, A 301/ B 301**

Course Information

This course provides an introduction to digital logic design and the basic building blocks used in digital systems, particularly in digital computers. It starts with revision of number systems, conversion between them and arithmetic operations. Logic gates, Boolean operations and Combinational circuits are then introduced together with commonly used building blocks like Multiplexers, Decoders, Adders, etc. Later these topics are followed by Lathces, Flip-Flops and Sequential circuits. In this context, mainly the Synchronous Sequential Circuits (Finite State Machines) are studied by using state transition diagrams and tables. Registers and counters are covered as most commonly used sequential blocks with different functionalities and applied to real case problems. During the last stage of the course design at the Register Transfer Level is briefly introduced with Algorithmic State Machines and simple hardware design examples. The course has an accompanying lab component that employs circuit simulators.

Learning Outcomes

Students finishing the course successfully are able to:

- Analize combinational circuits by building truth tables, writing Boolean expressions and simplifying them algebraically or by using Karnaugh maps. Assess the efficiency of different approaches for special and general cases separately by identifying advantages and disadvantages.
- Design small scale general combinational circuits by employing truth tables or Karnaugh maps. Efficiently use commonly used or specially designed building blocks to design relatively large-scale circuits. Make use of different implementation techniques to match the design with available hardware components or to meet certain optimality criteria for speed, efficiency and similar objectives.
- Analize Finite State Machines by constructing state diagrams and describing the circuit operation. Design small scale general Synchronous Sequential Circuits with flip-flops by using excitation tables. Build state diagram for a given problem, design it by using flip-flops and decide on the type of flip-flops for optimal result.
- Modify commonly used building blocks to add different functionalities and use them for building relatively large-scale Sequential Circuits.
- Analize how timing constraints are met for a given Sequential Circuit and fix problems if any. Identify advantages and disadvantages of parallel and serial operation in Logic circuits for a given problem.
- Use combinational and sequential components together to develop solutions to simple real-world examples and simulate the results. Use this knowledge towards more systematical approach at Register Transfer Level via ASMD charts and designing the corresponding hardware parts.

Prerequisites

Students should be familiar with discrete mathematics (Boolean algebra, number systems).

Textbooks

- M. Morris Mano and Michael D. Ciletti, Digital Design, 5th ed., Prentice-Hall, 2006
- David Money Harris, Sarah Harris, Digital Design and Computer Architecture, 2nd Edition.

Simulation Software

During the semester, most of the assignments/labs will be based on Logisim – logic design/circuit simulation software. Original version can be downloaded from this link: https://sourceforge.net/projects/circuit.

Topics covered

Course outline is given below (tentative, subject to modifications if necessary):

Binary numbers and arithmetic operations:

- Number systems and conversion
- Arithmetic operations in different systems
- Subtraction by using complements
- Signed and unsigned numbers, different systems for representing signed numbers
- Gray code, BCD, other binary codes
- BCD addition

Boolean Algebra and Logic Gates:

- Logic gates, their operation, Boolean variables
- Boolean algebra: axioms and theorems
- Standard representations: Sum of minterms and Product of maxterms
- Function simplification by using Boolean algebra
- Circuit diagrams and their simplification
- Karnaugh maps for function simplification
- Two level implementations of Boolean functions
- NAND gate and NOR gate as universal gates
- XOR and XNOR gates as “ODD” and “EVEN” functions

Combinational Logic:

- Definition of Combinational circuits
- Analysis and Design by using previous methods
- Decoders, Encoders, Multiplexers, Demultiplexers
- Adder, Subtractor, Binary multiplier, Magnitude comparators
- Decimal adder
- Timing considerations, speed and glitches

Synchronous Sequential Logic:

- Internal design of Latches and Flip-flops
- Definition of Sequential circuits
- Asynchronous and synchronous sequential circuits
- Types of flip-flops and their operation
- Finite State Machines: Mealy and Moore type
- Analysis of Synchronous Sequential Circuits via state tables and diagrams
- Design of Finite State Machines by using excitation characteristics of flip-flops
- Timing considerations: hold time constraint and setup time constraint

Registers and Counters:

- Registers, Shift registers

- Synchronous counters
- Ripple counters
- Designing synchronous sequential circuits by using registers and counters
- Serial vs parallel way of operation: illustration by using serial adder

Memory and Programmable Logic Devices:

- Random Access Memory
- Read Only Memory
- PLA, PAL

Design at the Register Transfer Level:

- Algorithmic State Machines
- Designing hardware for ASM
- Example: Sequential binary multiplier

Grading criteria

Students are expected to actively participate in classes, gain knowledge and demonstrate it via written assessments. Homework assignments require detailed solution to problems posted theoretically or via simulations. Originality of the solutions, clear description of the steps towards solution and correct results are main criteria for homework assessments. Quizzes are short in class exams to assess student's knowledge in time-limited basis. During the quizzes students are expected to solve related theoretical problems within the time limits without using any material or help, which also prepares them for the exams. Attendance and active participation in classes is expected and encouraged via 10 points. Midterm exam covers topics from first half of the semester while the Final exam may cover all topics. Students are expected to solve exam questions within the time limits and clearly show all steps of their solution together with the result. Students are expected to learn solution methods and apply them systematically to problems for deriving the answer. **Therefore, bare answers are not acceptable even if they are correct**! The distribution of grade weights over the assessment components is given below:

- **Attendance** **10%**
- **Quizzes** **10%**
- **Midterm** **20%**
- **Homework** **40%**
- **Final** **20%**

Course Policies

- **General**
  - Quizzes and exams are closed book, closed notes.
  - They may not be announced in advance.
- **Grades**
  - Passing grade for this course is D (>= 59.50)
  - Grades in the C range represent performance that meets expectations; Grades in the B range represent performance that is substantially better than the expectations; Grades in the A range represent work that is excellent.
  - Grades will be maintained in Blackboard. Students are responsible for tracking their progress by referring to the online gradebook.
- **Labs and Assignments**
  - Lab refers to a graded practical in-class assignment, which should be done individually by each student. Solutions for lab tasks should be designed using appropriate software and submitted till the end of class.
  - Quiz refers to a written in-class assignment, which should be done individually by each student. Solutions are paper based and should be submitted till the end of class.
  - Students are expected to work independently. Offering and accepting solutions from others is an

act of plagiarism, which is a serious offense and all involved parties will be penalized according to the Academic Honesty Policy. Discussion amongst students is encouraged, but when in doubt, direct your questions to the professor, tutor, or lab assistant.
    - No late assignments will be accepted under any circumstances.
- **Attendance**
    - Attendance is expected and will be taken each class. You are not allowed to miss more than 25% of the classes, as it will result in automatically failing the course.
    - Students are responsible for all missed work, regardless of the reason for absence. It is also the absentee's responsibility to get all missing notes or materials.

Academic Honesty Policy

You can find the ADA Honor Code and ADA Student Code of Conduct under following links:

https://www.ada.edu.az/frq-content/plugins/policies_x1/entry/20231011145604_47458900.pdf

https://www.ada.edu.az/frq-content/plugins/policies_x1/entry/20221226170144_27740900.pdf