Genetic Approach to Network Topology Optimization of Integrated 3D Multi-chip Systems

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***Abstract*—Integrated 3D multichip systems consist of multiple microprocessor chips stacked together in some layout configuration. Stacking chips together allows for many chips to be contained with in a single system which affords that system great computational power and it is beneficial for the running of parallel applications. Physical constraints as well as the avoidance of communication interference that can occur with wireless inter-chip communication presents network design challenges. A genetic algorithm was used to explore different designs in an attempt to achieve the best network inter-chip topology that complies with the physical constraints. The genetic algorithm was successful and layouts were generated with comparable network characteristics to a previously proposed layout known as the checkerboard.**

***Keywords*—Genetic Algorithm, Genetic Variation, Gene Flow, Integrated 3D Multi-Chip Systems**

I. Introduction

intro goes here

II. Methods

1) Mutation:

III. Resulting GA Generated Layouts

IV. Conclusion