DYNA FAMILY

SM3257ENBA

High Speed USB 2.0 Flash Memory Controller

Datasheet

Revision 1.0 **Sep 2014**

Revision History

Revision	Date	Description
0.1	Aug 2, 2013	Preliminary release
1.0	Sep 30, 2014	Formal release • Added the 48-pin TQFP pin assignments/marking and package outline (1.1)(1.2)(2.1)(4.2)(4.4)(5) • Added the product ordering information of die form (1.1)(1.2) (5)

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1. Overview

1.1 Product Description

The SM3257ENBA is a feature-enhanced USB 2.0 Flash Disk controller with high compatibility and best performance designed to support MLC and TLC NAND flash. The controller also supports high speed ONFI 2.x and Toggle mode NAND. Compliant with USB version 2.0 specification and USB Mass Storage Class version 1.0 specification, the SM3257ENBA provides write protect, PC boot-up from USB 2.0 Flash Disk, password protection, secured partitioning functions, etc.

The SM3257ENBA delivers high data transfer rate, and ensures data accuracy and reliability with the powerful ECC engine which can overcome the read/write disturbances in 3xnm, 2xnm, and 1xnm MLC/TLC flash. By integrating an embedded crystal, regulators and other components, the controller can reduce customer overall cost at a system level. The SM3257ENBA is available in LQFP/TQFP 48-pin, QFN 40-pin packages and die form with a manufacturing-ready turnkey solution.

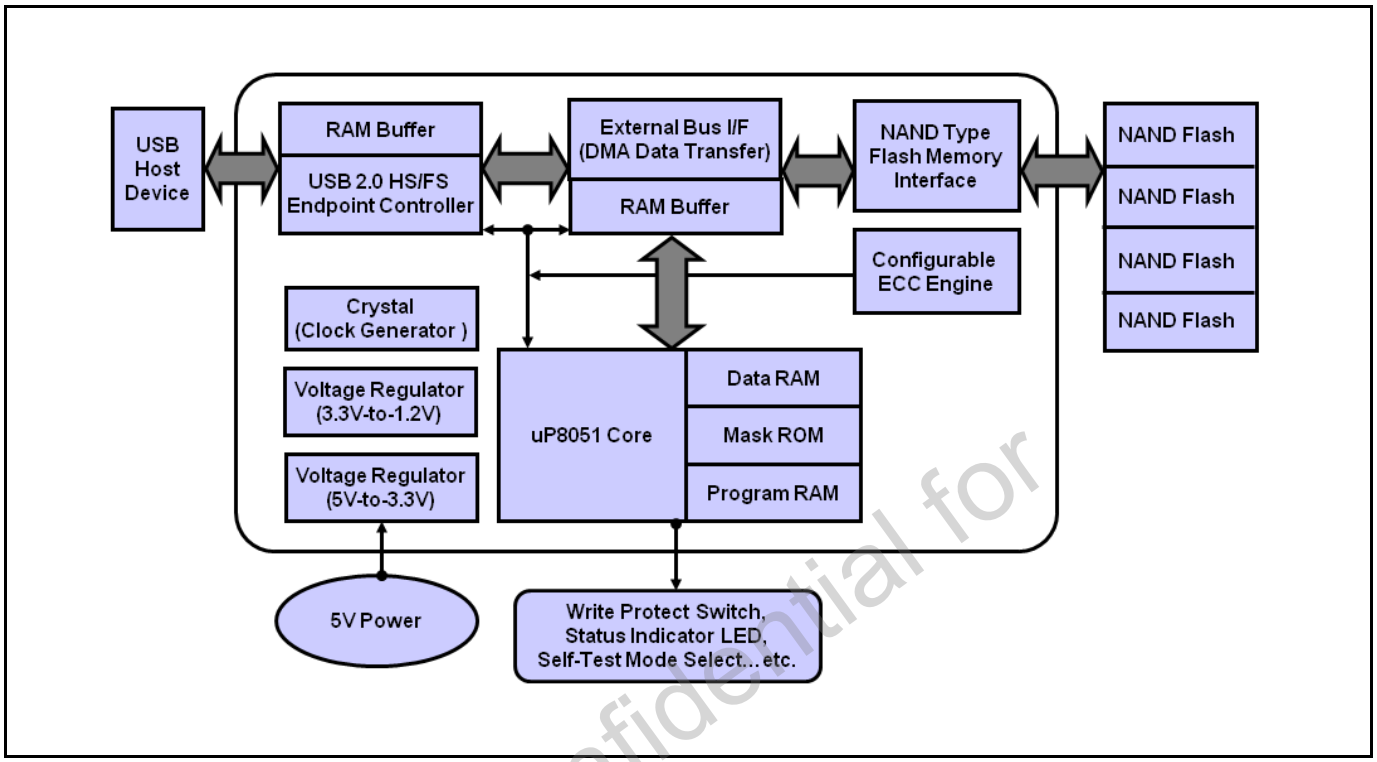
1.2 Key Features

- Embedded crystal offers lower BOM cost
- 1.2V low-power core operation
- Built-in 5V/3.3V and 3.3V/1.2V voltage regulators
- Complete compatibility with USB (Universal Serial Bus) Specification Rev. 2.0
- Complies with USB Mass Storage Class Specification Rev. 1.0
- USB Mass Storage Class Bulk-Only Transport Protocol
- Complies with USB power specifications for bus-powered devices
- Integrated 80C51-compatible, 8-bit microprocessor with enhanced features
- Supports suspend mode and wake-up resume
- Configurable ECC engine with correction capability up to 72-bit/1KB
- Supports high-speed DDR Toggle NAND and ONFI NAND flash
- Supports MLC/TLC up to 4 NAND flash devices
- Supports Bad Column Management
- Supports the operating systems: Windows 8, Windows 7, Windows Vista, Windows XP, Windows 2000, Windows ME, Windows 98/98SE, Mac OS 10.x, and Linux kernel 2.4
- Supports Windows 8, Windows 7 and Windows Vista ReadyBoost function
- In System Programming (ISP) firmware update capability

- Supports VID, PID, serial number, and vendor information updates
- Supports LED indicator to indicate the USB Flash Disk is in the Ready/Working mode
- Supports “Write Protect” security function to protect the data in USB Flash Disk
- Available in 48-pin LQFP/TQFP, 40-pin QFN packages and die Form

1.3 Block Diagram

Figure 1: SM3257ENBA Block Diagram



2. Pin Assignments and Signal Descriptions

2.1 Pin Assignments

Figure 2: 48-pin LQFP/TQFP Pin Assignments

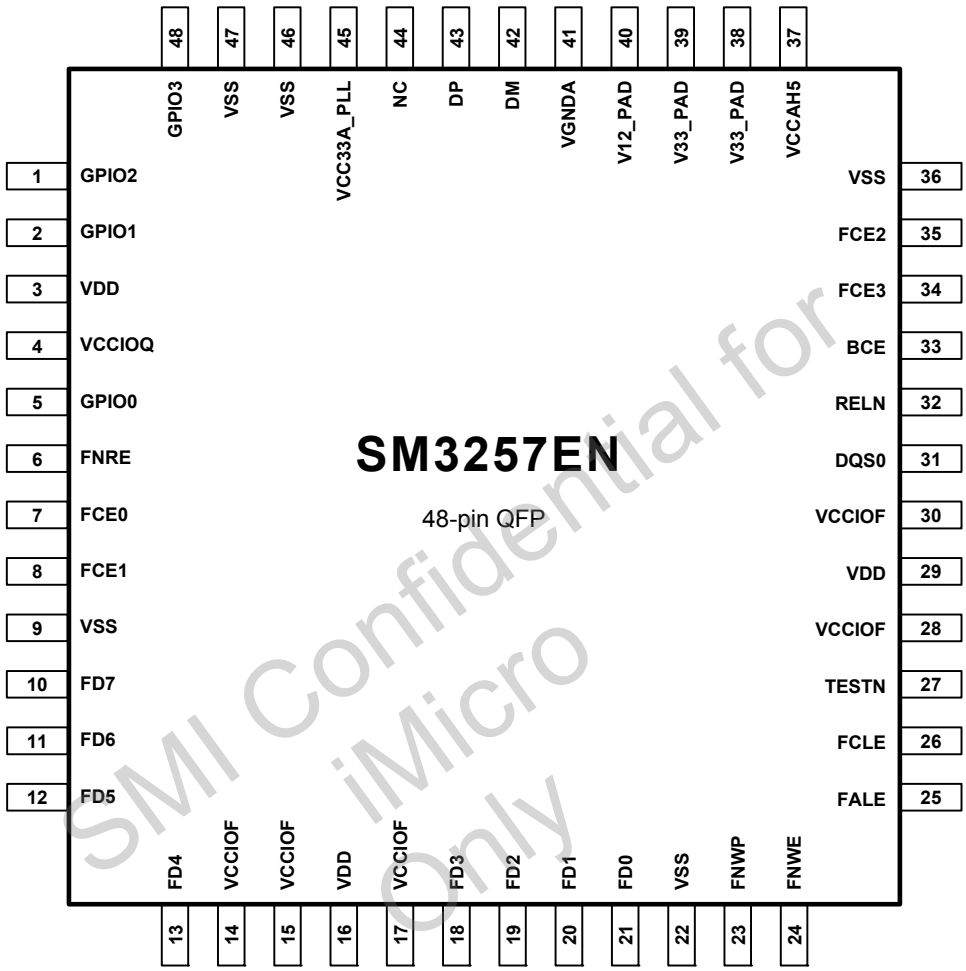
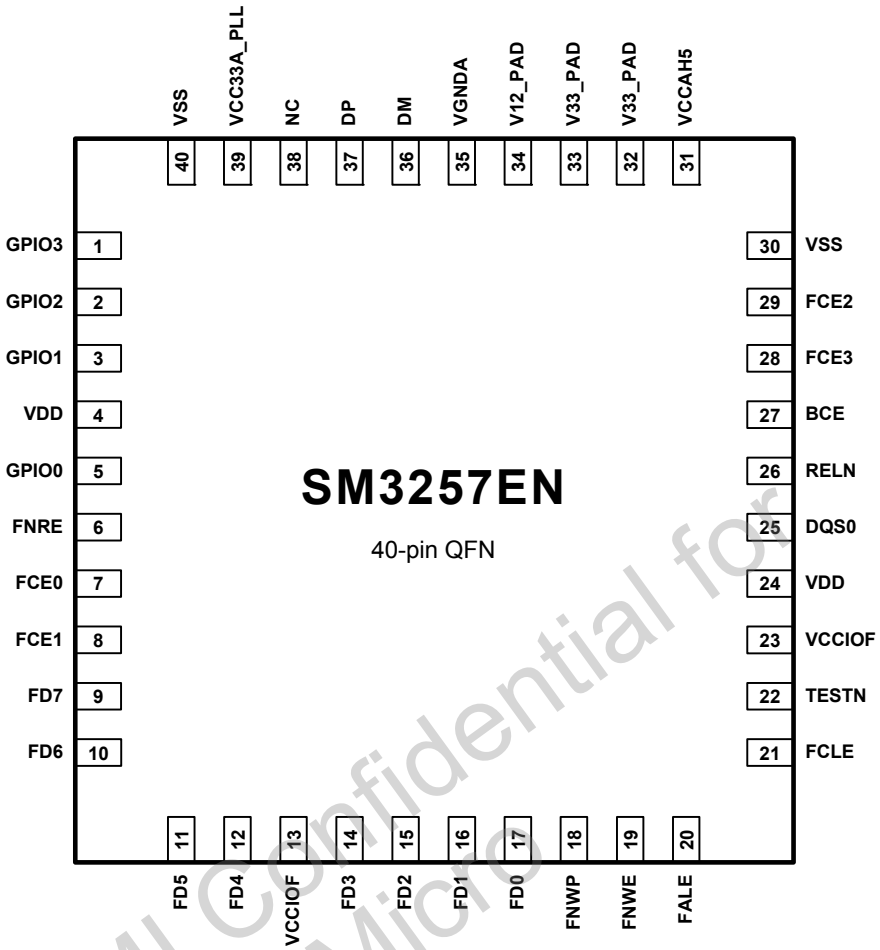


Figure 3: 40-pin QFN Pin Assignments



2.2 Signal Descriptions

Table 1: SM3257ENBA Signals

40-pin	48-pin	Signal	Type	Description
1	48	GPIO3	I/O	General Purpose I/O 1[3] This signal can also be used to connect UFD LED (active low).
2	1	GPIO2	I/O	General Purpose I/O 1[2] This signal can also be used as write protect (active low).
3	2	GPIO1	I/O	General Purpose I/O 1[1] This signal can also be used as Flash Ready/Busy 1.
4	3	VDD	PWR	Core Power
	4	VCCIOQ	PWR	I/O Power
5	5	GPIO0	I/O	General Purpose I/O 1[0] This signal can also be used as Flash Ready/Busy 0.
6	6	FNRE	O	Flash Read Enable (active low).
7	7	FCE0	I/O	CE0: Flash Chip Enable 0 This signal can also be used as General Purpose I/O 0[0].
8	8	FCE1	I/O	CE1: Flash Chip Enable 1 This signal can also be used as General Purpose I/O 0[1].
	9	VSS	GND	Ground for I/O and Core
9	10	FD7	I/O	Flash Data Bus[7]
10	11	FD6	I/O	Flash Data Bus[6]
11	12	FD5	I/O	Flash Data Bus[5]
12	13	FD4	I/O	Flash Data Bus[4]
13	14	VCCIOF	PWR	I/O Power
	15	VCCIOF	PWR	I/O Power
	16	VDD	PWR	Core Power
	17	VCCIOF	PWR	I/O Power
14	18	FD3	I/O	Flash Data Bus[3]
15	19	FD2	I/O	Flash Data Bus[2]
16	20	FD1	I/O	Flash Data Bus[1]
17	21	FD0	I/O	Flash Data Bus[0]
	22	VSS	GND	Ground for I/O and Core
18	23	FNWP	O	Flash Write Protect (active low)
19	24	FNWE	O	Flash Write Enable (active low)
20	25	FALE	O	Flash Address Latch Enable
21	26	FCLE	O	Flash Command Latch Enable
22	27	TESTN	I	Test Signal (active low)
23	28	VCCIOF	PWR	I/O Power
24	29	VDD	PWR	Core Power

40-pin	48-pin	Signal	Type	Description
	30	VCCIOF	PWR	I/O Power
25	31	DQS0	I/O	Data Strobe. Output with read data, input with write data. Edge-aligned with read data, centered in write data.
26	32	RELN	I	Reliable Mode Enable
27	33	BCE	I	Bad Column Enable
28	34	FCE3	I/O	CE3: Flash Chip Enable 3 This signal can also be used as General Purpose I/O 0[3].
29	35	FCE2	I/O	CE2: Flash Chip Enable 2 This signal can also be used as General Purpose I/O 0[2].
30	36	VSS	GND	Ground for I/O and Core
31	37	VCCAH5	PWR	Regulator 5V Power Input
32	38	V33_PAD	PWR	Regulator 3.3V Power Input/Output
33	39	V33_PAD	PWR	Regulator 3.3V Power Input/Output
34	40	V12_PAD	PWR	Regulator 1.2V Power Output
35	41	VGNDA	GND	Analog Ground
36	42	DM	I/O	USB2.0 Data Negative Signal
37	43	DP	I/O	USB2.0 Data Positive Signal
38	44	NC	-	No Connect
39	45	VCC33A_PLL	PWR	Analog 3.3V Power (for USB PHY and PLL)
40	46	VSS	GND	Ground for I/O and Core
	47	VSS	GND	Ground for I/O and Core

3. Electrical Characteristics

3.1 DC Characteristics

Table 2: Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Operating Temperature	Ta	0	70	°C
Storage Temperature	Tstg	-55	+150	°C
Voltage with Respect to Ground		-0.3	+5.5	V
Core Power Supply Voltage	VDD	1.08	1.32	V
I/O Supply Voltage	VCCIOQ	3.0	3.6	V
Analog 3.3V Input Voltage	V33_PAD	3.0	3.6	V
PHY I/O Voltage	VCC33A_PLL	3.0	3.6	V

Table 3: General DC Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	VCCIOQ	2.7	3.3	3.6	V
Analog 5V Input Voltage	VCCAH5	4.2	5.0	5.5	V
Analog 3.3V Input Voltage	V33_PAD	3.0	3.3	3.6	V
Regulated 1.2V Output Voltage	V12_PAD		1.2		V
Output High Voltage	V_{OH}	2.4			V
Output Low Voltage	V_{OL}			0.4	V
Input High Voltage	V_{IH}	2.0			V
Input Low Voltage	V_{IL}			0.8	V

3.2 Flash Interface AC Characteristics

3.2.1 Traditional NAND Mode

Table 4: Traditional Flash Interface Timing Parameters

Parameter	Symbol	Min	Max	Unit
CLE Setup Time	tCLS	1		tCK
CLE Hold Time	tCLH	1		tCK
CE Setup Time	tCS	>20		ns
CE Hold Time	tCH	1		tCK
ALE Setup Time	tALS	1		tCK
ALE Hold Time	tALH	1		tCK
WE Pulse Width	tWP	1		tCK
Data Setup Time	tDS	1		tCK
Data Hold Time	tDH	1		tCK
Write Cycle Time	tWC	2		tCK
WE High Hold Time	tWH	1		tCK
Read Cycle Time	tRC	2		tCK
RE High Hold Time	tREH	1		tCK
R/B Ready to RE Low	tRR	5		tCK

Note: tCK = system clock operation period.

Figure 4: Command Latch Cycle Timing

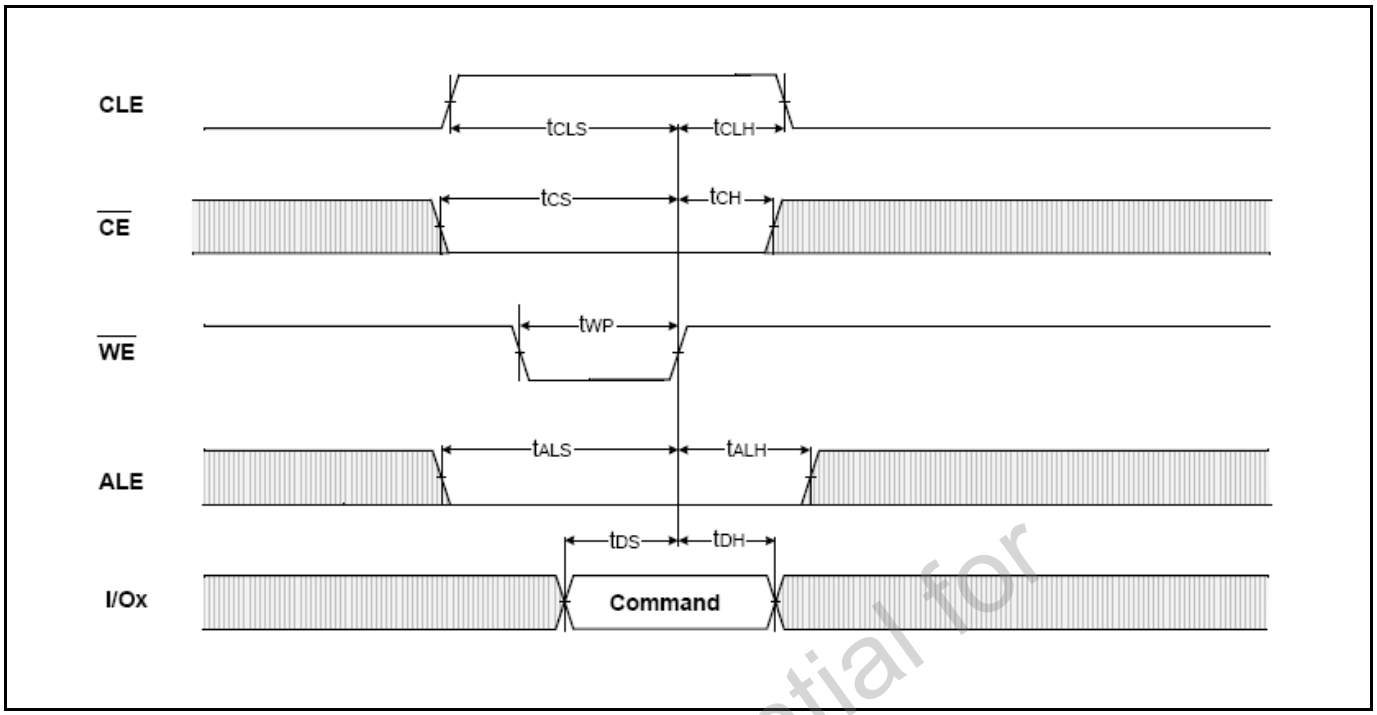


Figure 5: Address Latch Cycle Timing

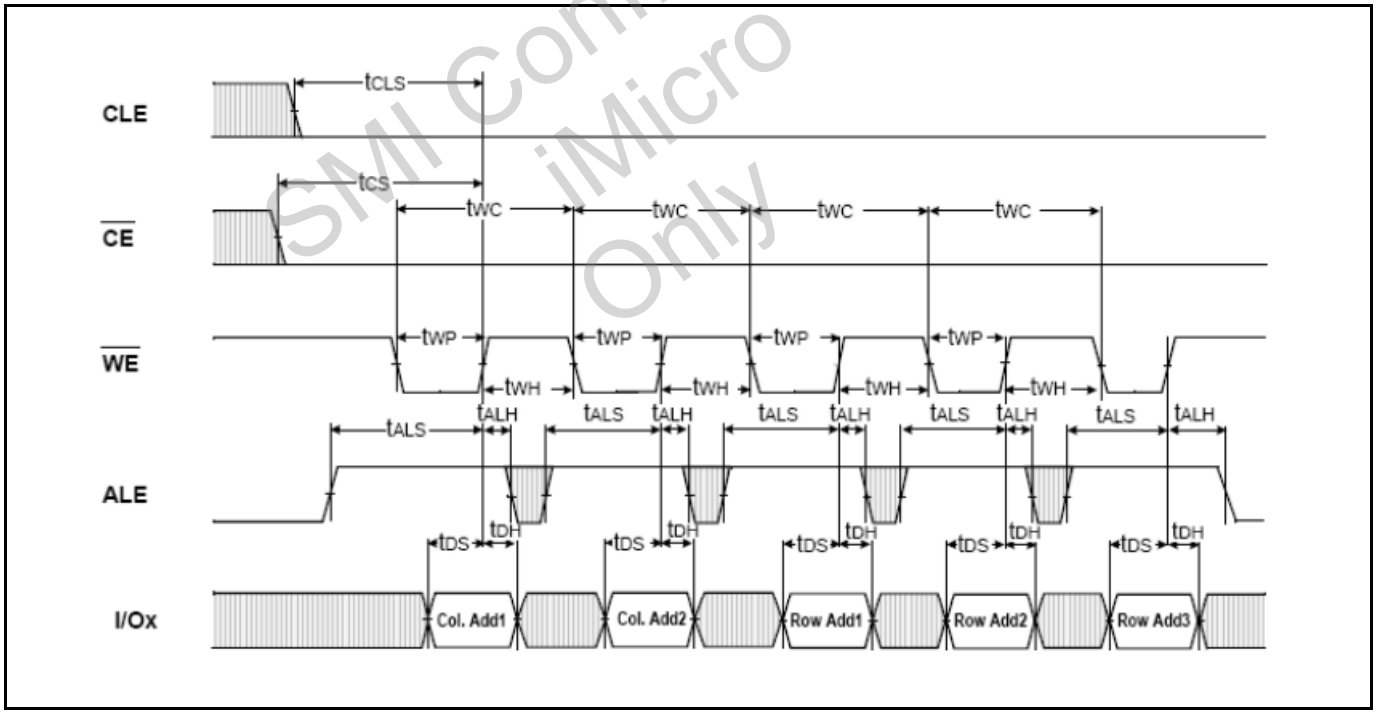


Figure 6: Input Data Latch Cycle Timing

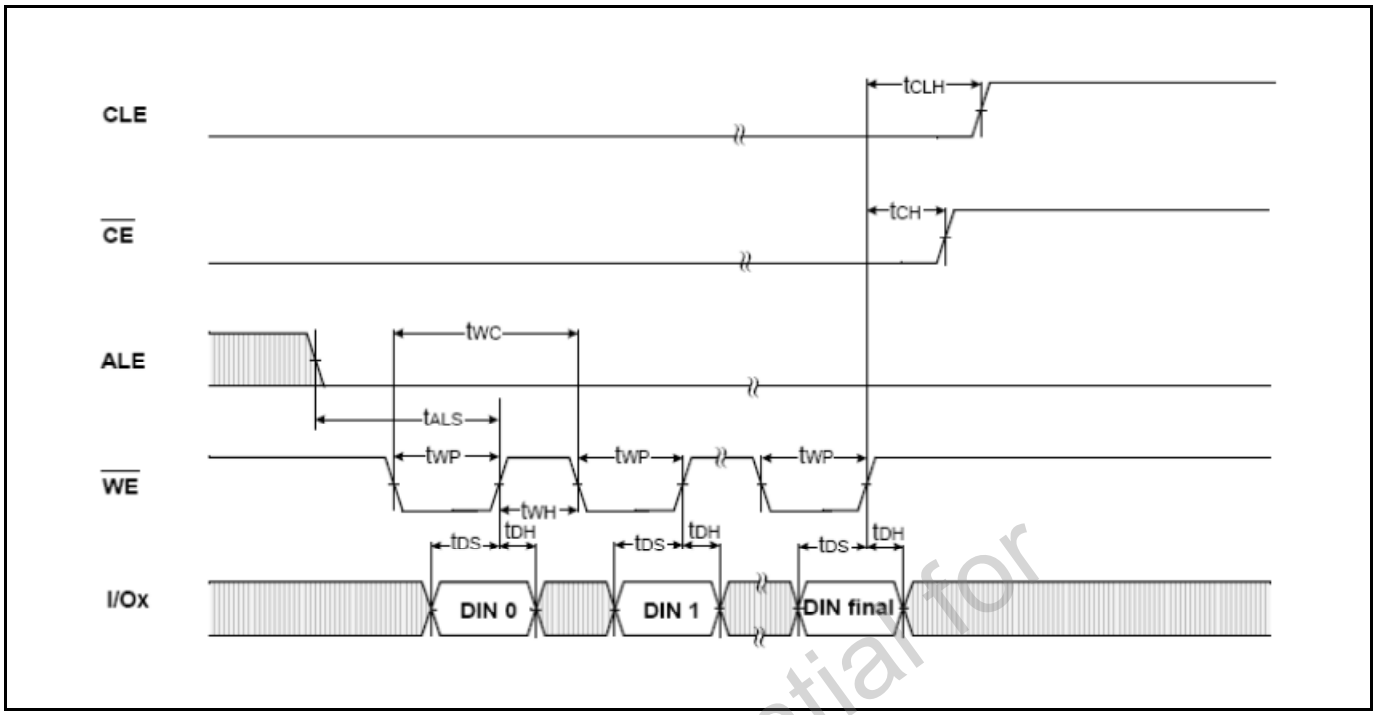
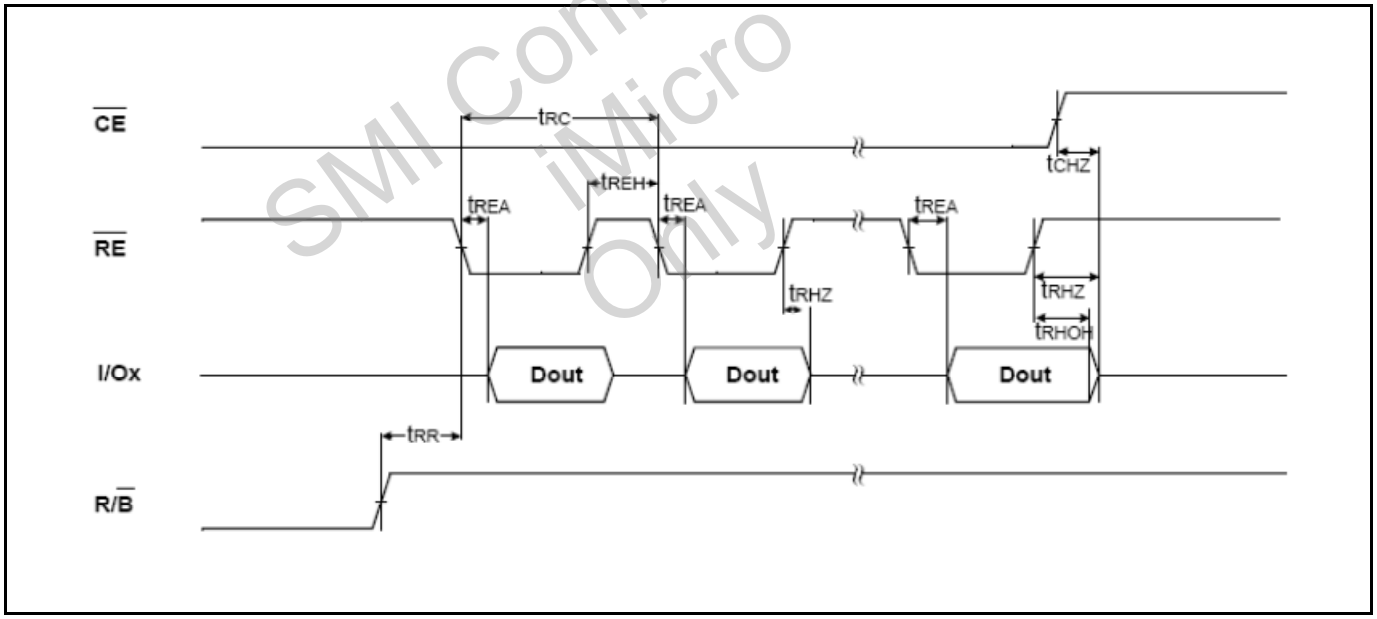


Figure 7: Serial Access Cycle after Read



3.2.2 Toggle Mode

Table 5: Toggle Mode Flash Interface Timing Parameters

Parameter	Symbol	Min	Max	Unit
CLE/ALE Setup Time	tCALS	1		tCK
CLE/ALE Hold Time	tCALH	1		tCK
DQS Setup Time for Data Input Start	tCDQSS	> 100		ns
CE Setup Time	tCS	> 20		ns
CE Hold Time	tCH	> 5		ns
Command/Address Setup Time	tCAS	1		tCK
Command/Address Hold Time	tCAH	1		tCK
Data Setup Time	tDS	0.5		tCK
Data Hold Time	tDH	0.5		tCK
Write Cycle Time	tWC	2		tCK
WE High Pulse Width	tWH	1		tCK
WE Low Pulse Width	tWP	1		tCK
Read Cycle Time	tRC	2		tCK
RE High Pulse Width	tREH	1		tCK
RE Low Pulse Width	tRP	1		tCK
Data Strobe Cycle Time	tDSC	2		tCK
DQS Input Low Pulse Width	tDQSL	1		tCK
DQS Input High Pulse Width	tDQSH	1		tCK
Read Preamble	tRPRE	2		tCK
Read Postamble	tRPST	> 100		ns
Read Postamble Hold Time	tRPSTH	> 100		ns
Write Preamble	tWPRE	> 83		ns
Write Postamble	tWPST	> 83		ns
Write Postamble Hold Time	tWPSTH	> 5		ns

Note: tCK = system clock operation period.

Figure 8: Toggle Mode – Command Latch Cycle Timing

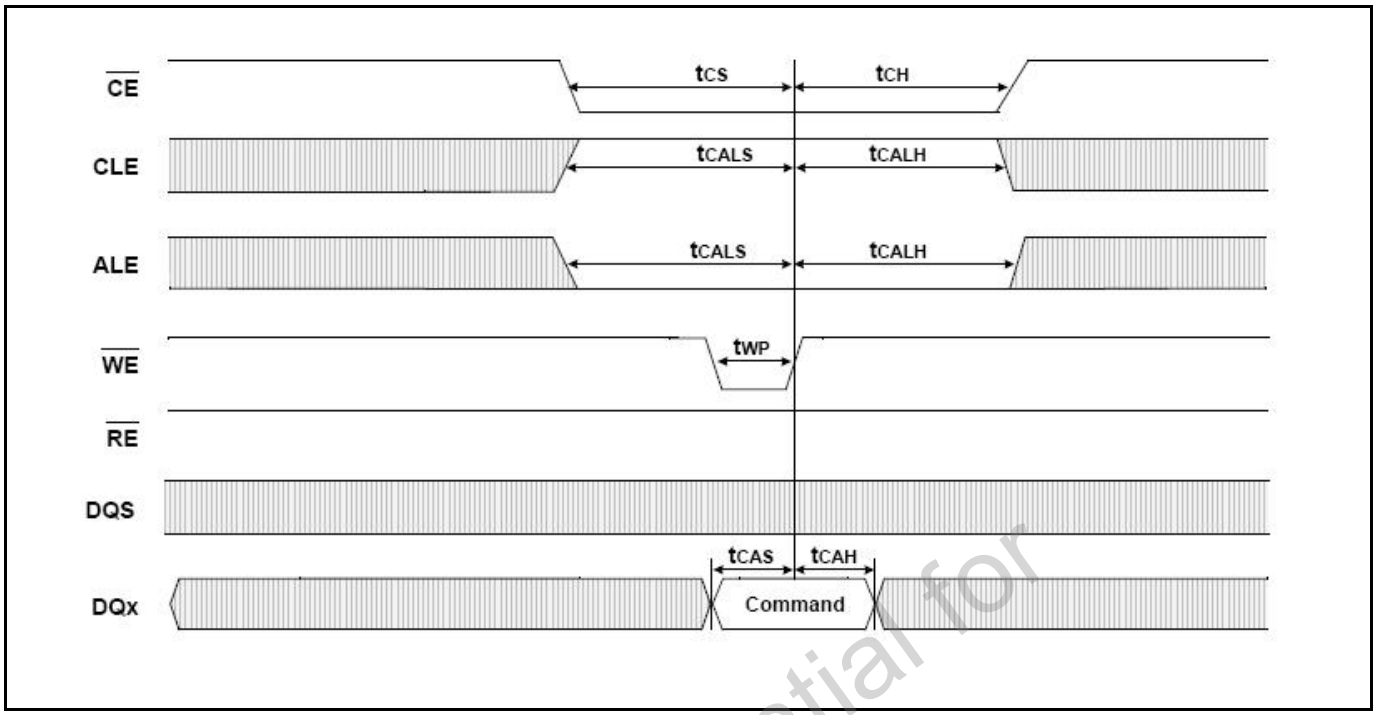


Figure 9: Toggle Mode – Address Latch Cycle Timing (1)

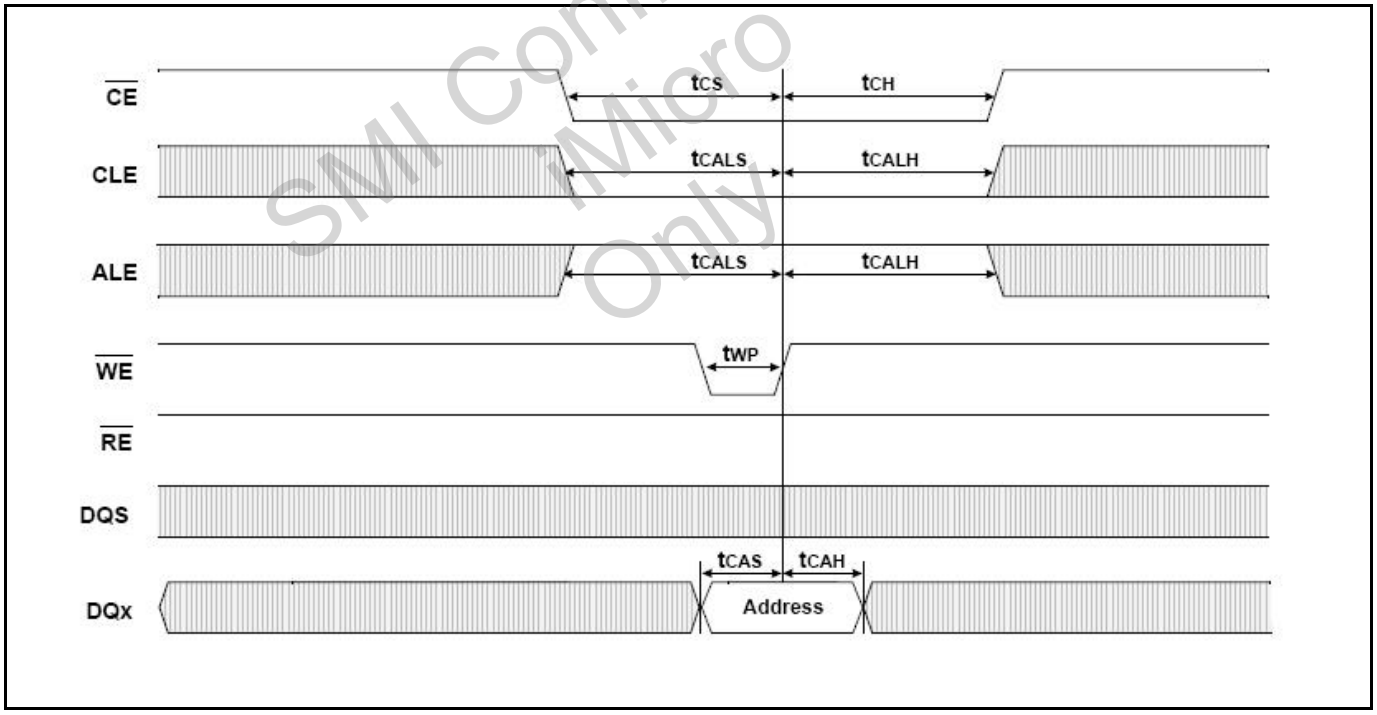


Figure 10: Toggle Mode – Address Latch Cycle Timing (2)

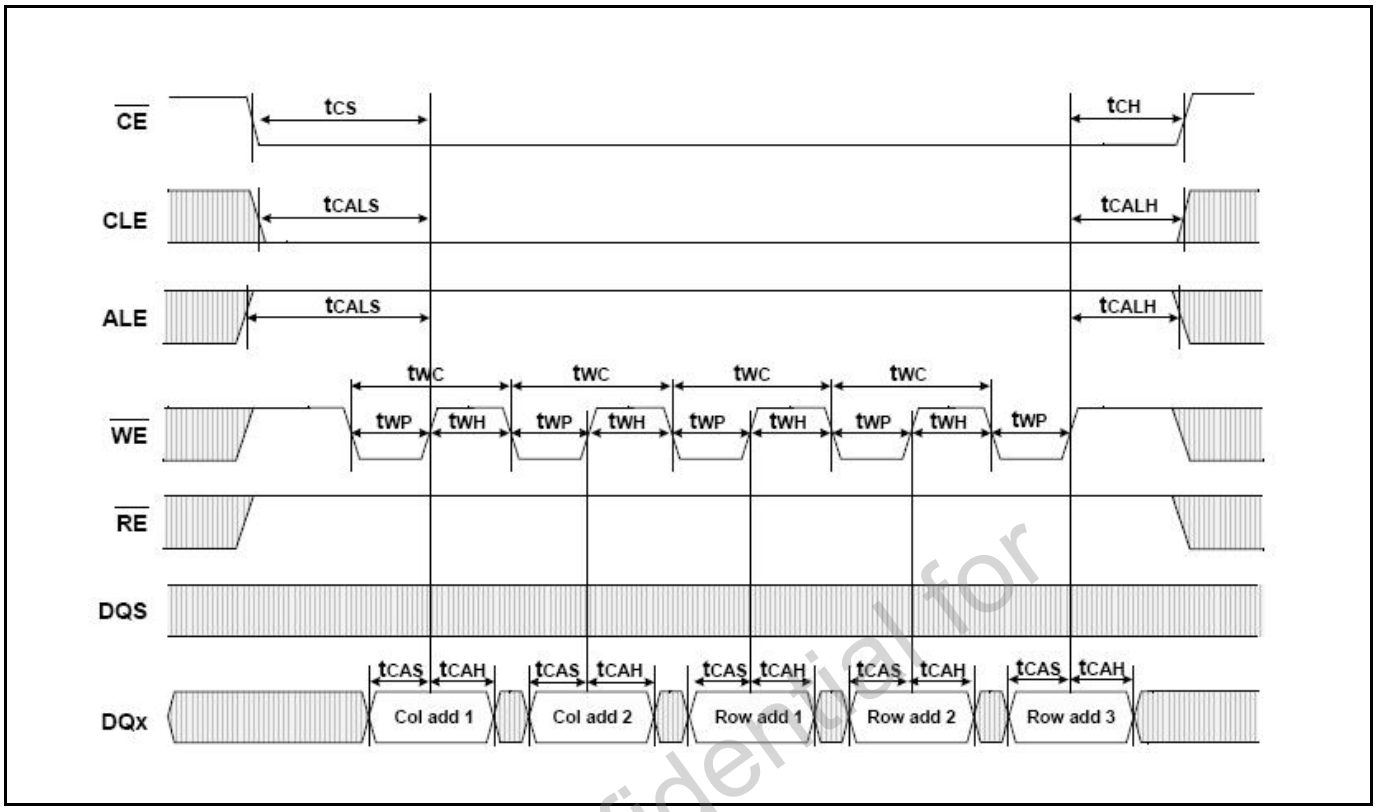


Figure 11: Toggle Mode – Output Data (Write) Cycle Timing

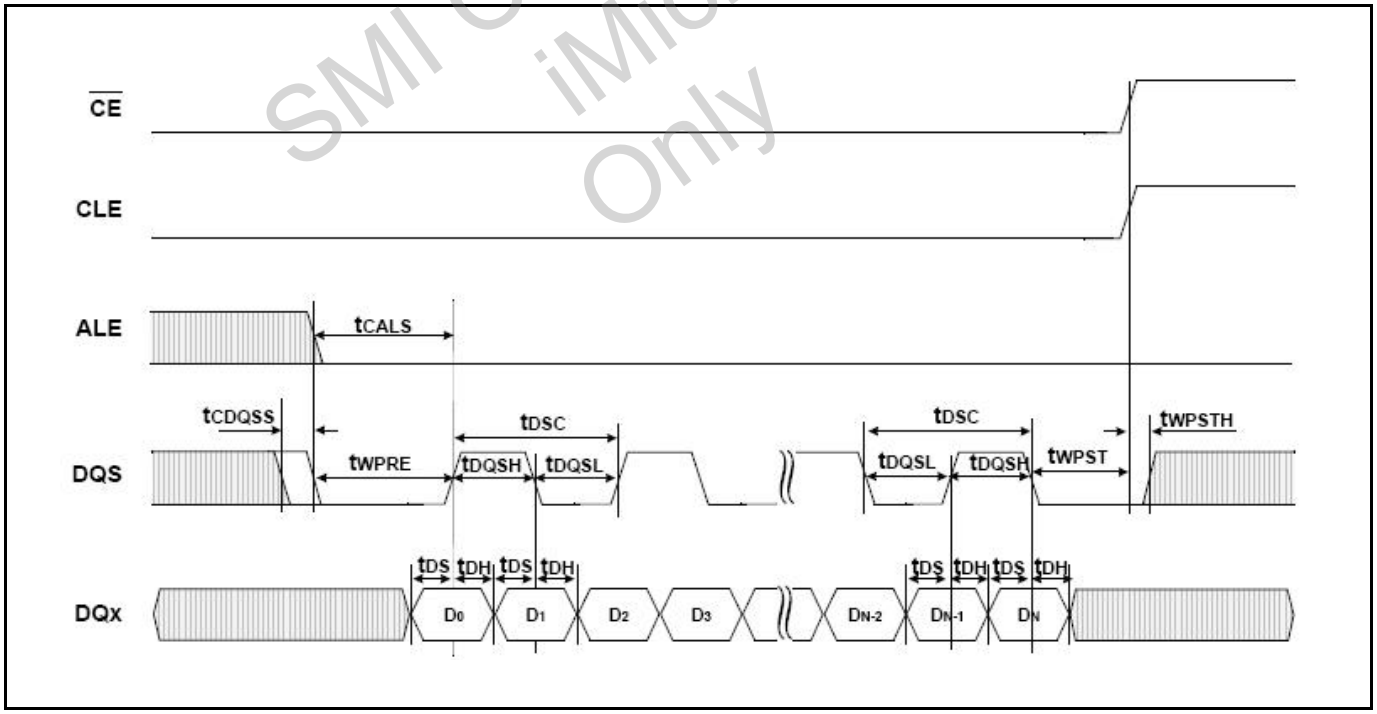
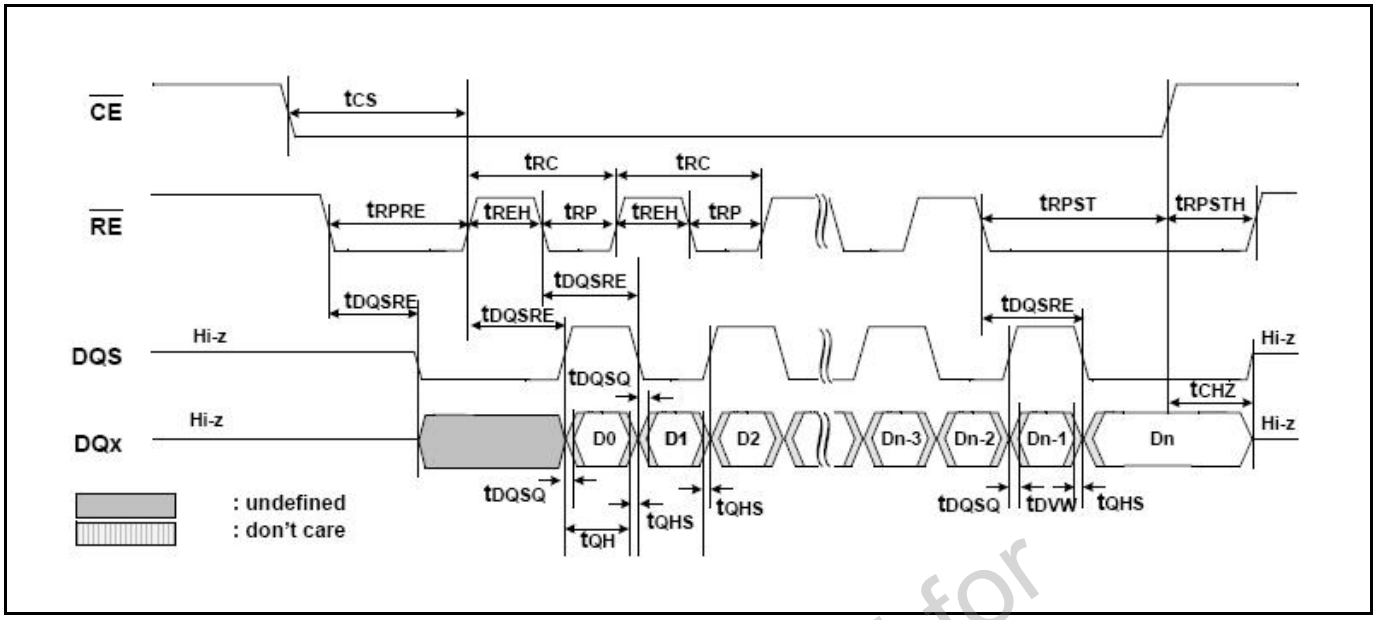
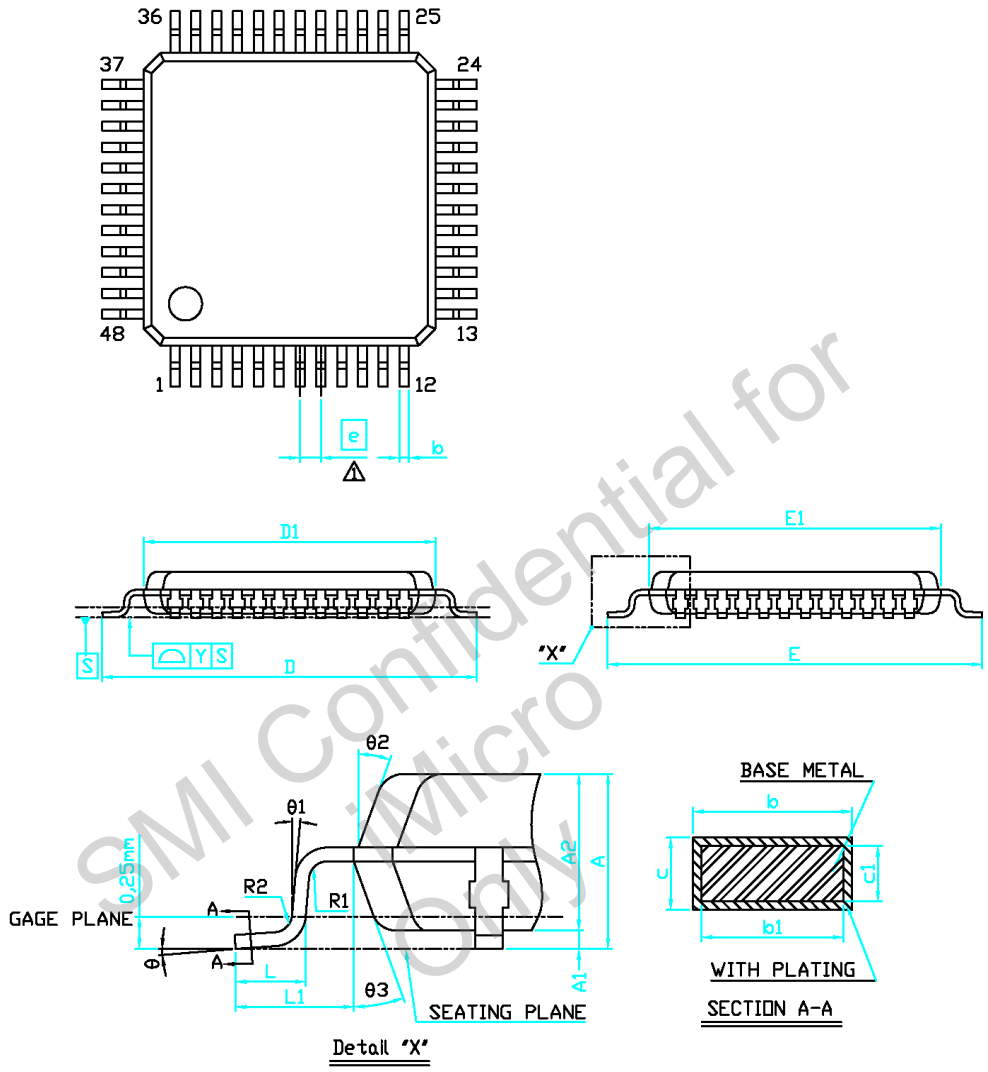


Figure 12: Toggle Mode – Input Data (Read) Cycle Timing



4. Package Information

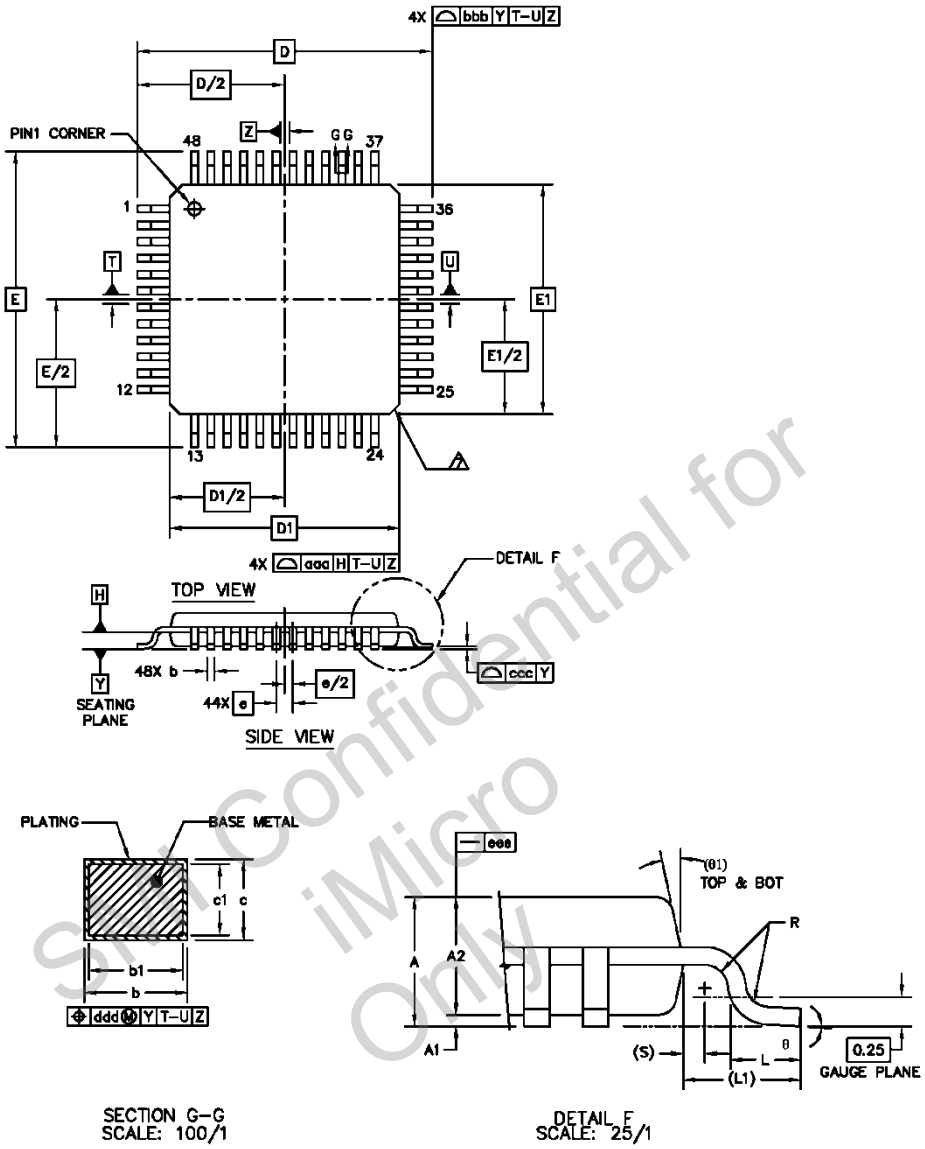
4.1 48-Pin LQFP Package Outline



SYMBOL	MIN	NOM	MAX	SYMBOL	MIN	NOM	MAX
A	---	---	1.60	e	0.35	0.50	0.65
A1	0.05	---	0.15	L	0.45	0.60	0.75
A2	1.35	1.40	1.45	L1	1.00 REF		
b	0.17	0.22	0.27	R1	0.08	---	---
b1	0.17	0.20	0.23	R2	0.08	---	0.20
c	0.09	---	0.20	Y	---	---	0.075
c1	0.09	---	0.16	θ	0°	3.5°	7°
D	9.00 BSC			θ1	0°	---	---
D1	7.00 BSC			θ2	11°	12°	13°
E	9.00 BSC			θ3	11°	12°	13°
E1	7.00 BSC						

Notes:
1. Refer to JEDEC MS-026/BBC.
2. Dimension D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side D1 and E1 are maximum plastic body size dimension including mold mismatch.
3. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08 mm.
4. All dimensions are in millimeters.

4.2 48-Pin TQFP Package Outline

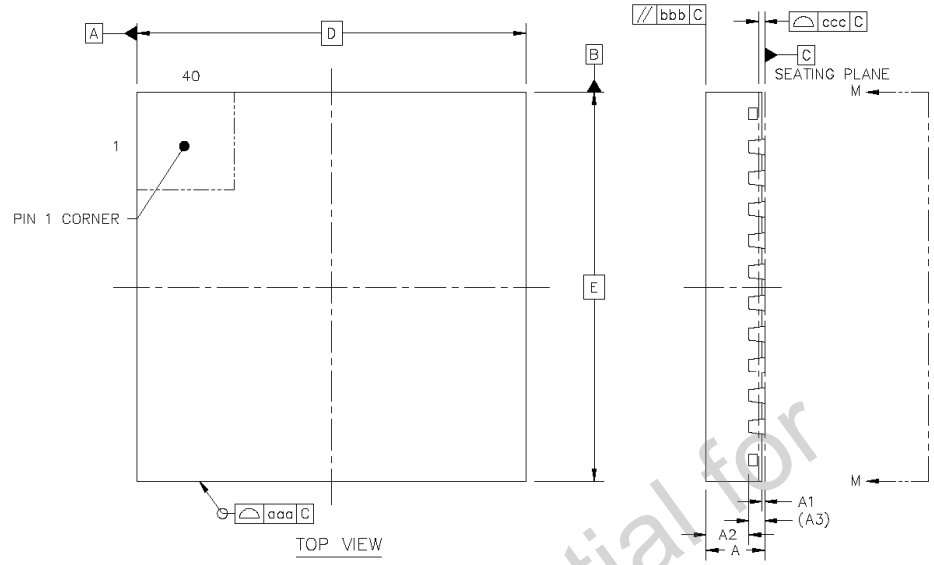


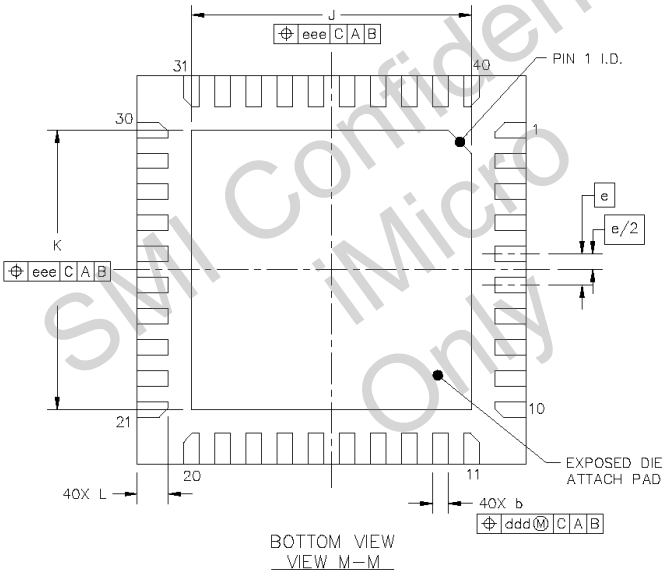
		Symbol	MIN	NOM	MAX		Symbol	MIN	NOM	MAX
Total Thickness		A	1	---	1.2		L	0.5	---	0.7
Stand Off		A1	0.05	---	0.15	Foot Print	L1	1 REF		
Mold Thickness		A2	0.95	---	1.05		θ	1°	---	5°
Lead Width (Plating)		b	0.17	---	0.27		θ1	12° REF		
Lead Width		b1	0.17	---	0.23		R	0.15	---	0.25
L/F Thickness (Plating)		c	0.09	---	0.2		S	0.2 REF		
L/F Thickness		c1	0.09	---	0.16	Package Edge Tolerance	aaa	0.2		
	X	D	9 BSC			Lead Edge Tolerance	bbb	0.2		
	Y	E	9 BSC			Coplanarity	ccc	0.08		
Body Size	X	D1	7 BSC			Lead Offset	ddd	0.08		
	Y	E1	7 BSC			Mold Flatness	eee	0.05		
Lead Pitch		e	0.5 BSC							

Notes:

1. Datum plane H is located at bottom of lead and is coincident with the lead exits the plastic body at the bottom of the parting line.
2. Datums T, U and Z to be determined at datum plan H.
3. Dimensions D and E to be determined at seating plane datum Y.
4. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. Dimensions D1 and E1 do include mold mismatch and are determined at datum plan datum H.
5. Dimension b does not include dambar protrusion. Dambar protrusion shall not cause the dimension b to exceed 0.35.
6. Minimum solder plate thickness shall be 0.0076.
7. Exact shape of each corner is optional.
8. Controlling Dimension: Millimeter.

4.3 40-Pin QFN Package Outline





		SYMBOL	MIN	NOM	MAX			SYMBOL	MIN	NOM	MAX
Total Thickness		A	0.7	0.75	0.8	EP Size	X	J	3.5	3.6	3.7
Stand Off		A1	0	0.035	0.05		Y	K	3.5	3.6	3.7
Mold Thickness		A2	---	0.55	0.57	Lead Length		L	0.35	0.4	0.45
L/F Thickness		A3	0.203 REF			Package Edge Tolerance		aaa	0.1		
Lead Width		b	0.15	0.2	0.25	Mold Flatness		bbb	0.1		
Body Size	X	D	5 BSC			Coplanarity		ccc	0.08		
	Y	E	5 BSC			Lead Offset		ddd	0.1		
Lead Pitch		e	0.4 BSC			Exposed Pad Offset		eee	0.1		

Note: Coplanarity applies to leads, corner leads and die attach pad. Controlling Dimension: Millimeter.

4.4 Top Marking

Figure 13: Top Marking of 48-pin LQFP

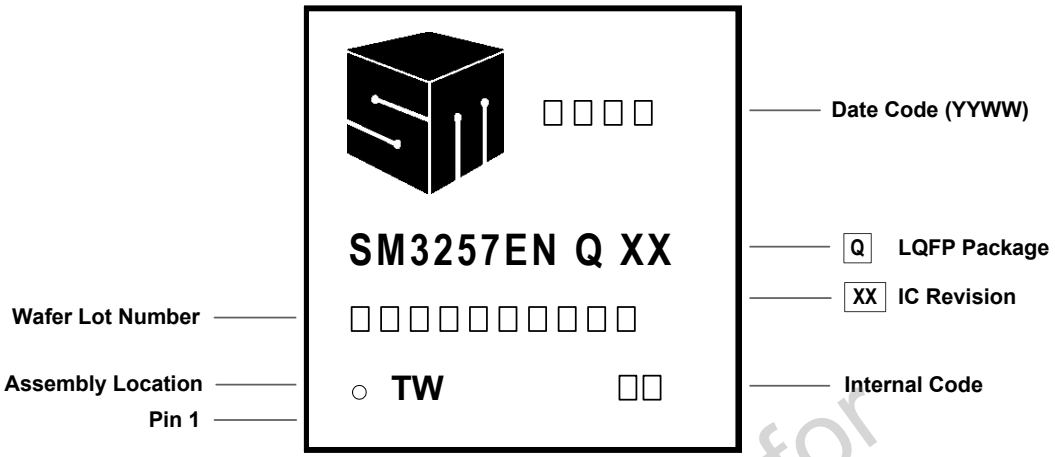


Figure 14: Top Marking of 48-pin TQFP

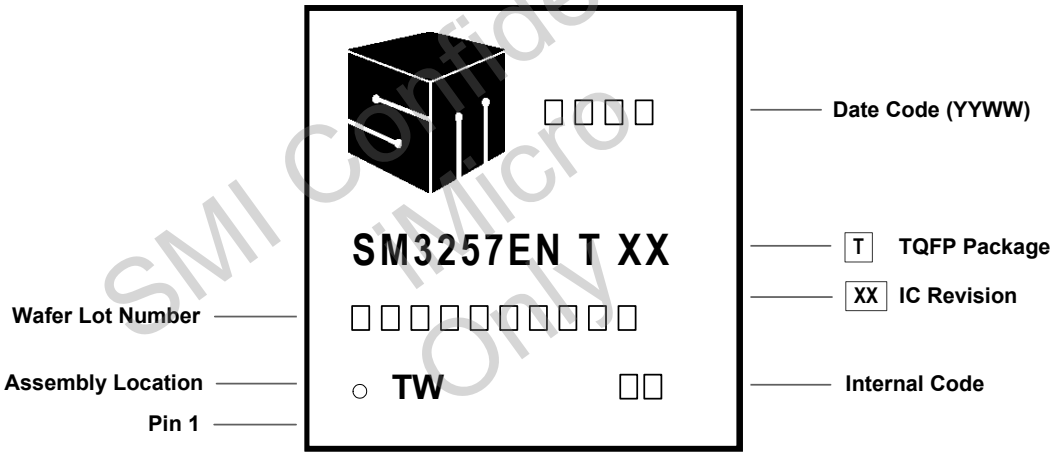
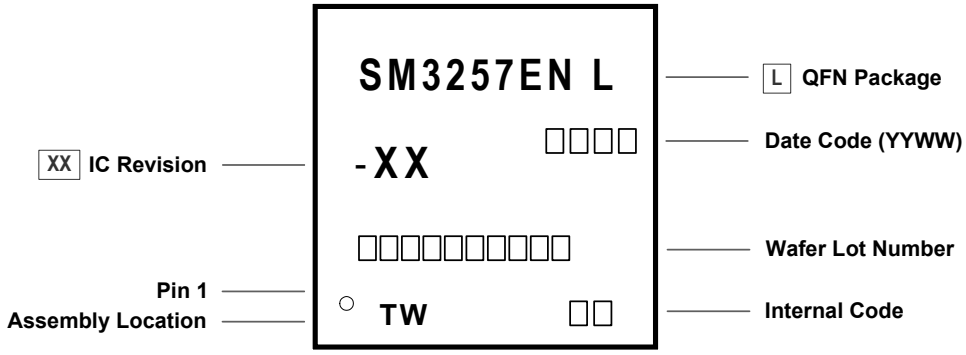


Figure 15: Top Marking of 40-pin QFN



5. Product Ordering Information

Table 6: Ordering Information

Ordering Number	Operating Temperature	Package	Description
SM325QX0700EN-BA	0°C ~ 70°C	48-pin LQFP	7 x 7 x 1.4 (mm)
SM325TX0700EN-BA	0°C ~ 70°C	48-pin TQFP	7 x 7 x 1.0 (mm)
SM325LX0700EN-BA	0°C ~ 70°C	40-pin QFN	5 x 5 x 0.8 (mm)
DF32570EN0000-BA	0°C ~ 70°C	Die Form	--