## 2.1 Instruction Set Summary

## 2.1.1 Format Summary

The AMO instruction set formats are shown below.

3 3 2 2 2 2 1 0 9 8 7 6	2 2 2 2 2 5 4 3 2 1	2 1 1 1 1 0 9 8 7 6	1 1 1 1 1 5 4 3 2 1	1 0 9 8 7 6 5 4 3 2 1 0		
Opcode	Rd	Rs			Data Transfer	
Opcode	Rd		Imm	ediate		
Opcode	Rd	Base		Immediate	Load/Store	
Opcode	Rd		Immediate		_ Load/Store	
Opcode	Rd	Rn	Rs		Logical/Arithmetic	
Opcode	Rd	Rs		Immediate		
Opcode	Rd	Rs		Immediate	Branch	
Opcode	Rd					
_	Rα				Jump	
Opcode			Immediate			
Opcode					System Call	

## 2.1.2 Instruction Summary

Mnemonic	Example	Instruction	DEFAULT
MOV	mov Rd, Rs/imm21	Rd ← Rs/imm21	
	mov Rd, imm32/symbol	literal pool (pseudo)	
LDR	ldr Rd, [base, offset]	Rd ← mem[base + offset]	
	ldr Rd, [relative]	Rd ← mem[pc + relative]	
STR	str [base, offset], Rs	mem[base + offset] ← Rs	
	str [relative], Rs	mem[pc + relative] ← Rs	
LDRB	ldrb Rd, [base, offset]	Rd ← mem[base + offset]	
	ldrb Rd, [relative]	Rd ← mem[pc + relative]	
STRB	strb [base, offset], Rs	$mem[base + offset] \leftarrow Rs$	_
	strb [relative], Rs	$mem[pc + relative] \leftarrow Rs$	
LDRH	ldrh Rd, [base, offset]	Rd ← mem[base + offset]	
	ldrh Rd, [relative]	Rd ← mem[pc + relative]	
STRH	strh [base, offset], Rs	$mem[base + offset] \leftarrow Rs$	
	strh [relative], Rs	mem[pc + relative] ← Rs	

ADD	add Rd, Rn, Rs/imm16	Rd ← Rn + Rs/imm16
ADC	adc Rd, Rn, Rs/imm16	$Rd \leftarrow Rn + Rs/imm16 + Carry$
SUB	sub Rd, Rn, Rs/imm16	Rd ← Rn - Rs/imm16
AND	and Rd, Rn, Rs/imm16	Rd ← Rn AND Rs/imm16
OR	or Rd, Rn, Rs/imm16	Rd ← Rn OR Rs/imm16
XOR	xor Rd, Rn, Rs/imm16	Rd ← Rn XOR Rs/imm16
NOT	not Rd, Rs/imm16	Rd ← NOT Rs/imm16
LSL	lsl Rd, Rn, Rs/imm16	Rd ← Rn << Rs/imm16
LSR	lsr Rd, Rn, Rs/imm16	Rd ← Rn >> Rs/imm16
ASR	asr Rd, Rn, Rs/imm16	Rd ← Rn >>> Rs/imm16
BEQ	beq Rd, Rs, imm16	$PC \leftarrow PC + (imm16 << 2) if Rd == Rs$
BNE	bne Rd, Rs, imm16	PC ← PC + (imm16 << 2) if Rd != Rs
BLT	blt Rd, Rs, imm16	$PC \leftarrow PC + (imm16 << 2) if Rd < Rs$
BLE	ble Rd, Rs, imm16	$PC \leftarrow PC + (imm16 << 2) if Rd <= Rs$
BLTU	bltu Rd, Rs, imm16	$PC \leftarrow PC + (imm16 << 2) if Rs < Rn$
BLEU	bleu Rd, Rs, imm16	$PC \leftarrow PC + (imm16 << 2) if Rs <= Rn$
JMP	jmp Rs/imm26	PC = Rs/(imm26 << 2)
JAL	jal Rs/imm26	PC = (imm26 << 2)
		LR = PC
SWI	swi imm6	Jump to Interrupt Vector (Trap)
EXT	ext Rd, Rs, Opt	Rd ← [Sign/Unsign]Extend (Rs)
SETVT	setvt Rs, Type	Set the Vector Table
		Type 0: Interrupt Vector Table
RET	ret Rs	PC = Rs/(imm26 << 2)
		InterruptBlocking = false
LOCK	lock	InterruptBlocking = !InterruptBlocking
		(for atomic operation)