Design of Low Power 4x4 Magnitude Comparator Using Static gates and sizing Transistors Technique

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***Abstract*—In this project, we present the design and implementation of a low-power, high-speed 4x4 magnitude comparator using static gates and optimized transistor sizing. The primary objective is to minimize power consumption and reduce propagation delay in the circuit. The design leverages conventional CMOS logic styles, and specific techniques have been employed to enhance performance metrics.**

I. INTRODUCTION

I.I. Magnitude Comparator

A magnitude comparator is a primary digital circuit that compares the value magnitudes of two binary parameters. This circuit generates signals that indicate whether one number is larger than, less than, or equal to another, resulting in a vital part in digital systems including processors, systems for sorting, and mathematical units. Magnitude comparators must be present for efficient information handling and decision-making within electronic devices and systems, ranging from simple controllers to advanced microprocessors.

This device compares the bits of two numbers, beginning with the most significant bit (MSB) and then going down to the least significant bit (LSB). At each bit location, the numbers' two corresponding bits are compared. If the bit in the first number is bigger than the equivalent bit in the second number, the A>B output is set to one, and the circuit knows that the first number is greater than the second. If the bit in the second number is bigger than the corresponding bit in the first number, the A/B output is set to 1, indicating that the first number is smaller than the second.

If the two matching bits are equal, the circuit advances to the next bit location and checks the following pair of bits. The procedure continues until all of the bits have been checked. Suppose the circuit detects at any time throughout the analysis that the first number is larger or less than the second number. In that case, it terminates the comparison and generates the appropriate output. If all of the bits are equal, the circuit produces an A=B output, which indicates that the two numbers are equal.

A magnitude comparator's efficiency is defined by how well it can execute those comparisons rapidly and correctly while consuming minimum power. Advanced comparator designs, prioritize addressing these elements to improve the general efficiency of digital circuits and systems. By improving their logical structure and utilizing advanced technology, Magnitude comparators may considerably enhance the speed and effectiveness of processing information in modern electronic systems [1].

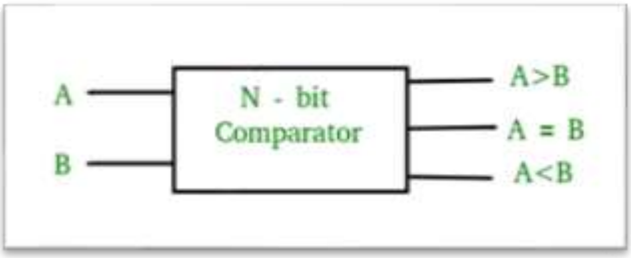


Figure 1: Conceptual view of a Magnitude Comparator [1]

I.II. Motivation

We point out the design and construction of a low-power device, a fast speeds 4x4 magnitude comparator. Our solution uses static gates and optimized transistor size strategies to reduce energy use and delay throughout propagation. Using 22nm technology, we obtain considerable gains in performance parameters. This new technology allows for lower leakage currents and faster switching rates, improving our comparator's efficiency and reliability.

signifies a thorough examination of existing comparator designs, to maximize power, speed, and area. A developed magnitude comparator that fits the tough specifications of current electronic applications by combining traditional CMOS logic designs with specialized design strategies. The results show significant improvements in energy utilization and speed, demonstrating the efficacy of the design technique and attempting to present a full account of the designing procedure, including schematic layouts, simulation outcomes, and performance contrasts, highlighting the important optimizations and design decisions.

II. LITERATURE REVIEW

The binary or digital comparator may be built with ordinary AND, NOR, and NOT gates for contrasting the digital signals received at their input terminals while generating an output based on the state of those inputs. As an illustration, in addition to adding and subtracting binary numbers, we must be able to compare them and establish if the value of input A is higher than, less than, or equal to the value of input B, and so on. The digital comparator does this by employing many logic gates based on Boolean Algebra. There are two primary types of digital comparators available, First, the Identity Comparator - an Identification Comparator is a digital comparator with only one results terminal: when A equals B, either A = B = 1 (HIGH) or A = B = 0 (LOW) [2].

Secondly, a Magnitude Comparator is a digital comparator with three output terminals: equality (A = B), larger than (A > B), and less than (A < B). A 1-bit magnitude comparator is an electronic component that compares two binary bits and provides three outputs based on each of their magnitudes, and a 2-bit magnitude comparator compares two binary values (each with two bits) and returns three outputs based on the relative magnitudes of the binary bits [3].

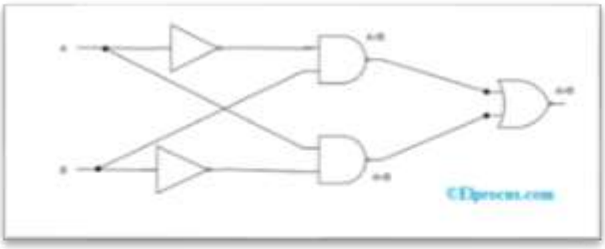
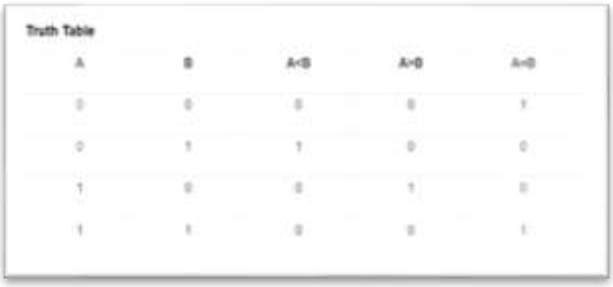


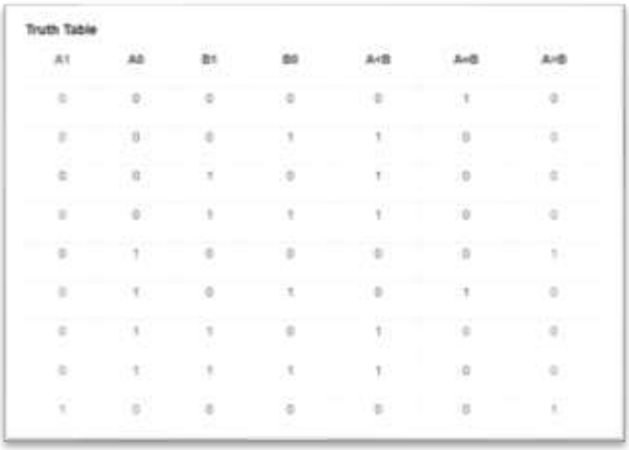
Figure 2: 1-bit Magnitude Comparator circuit [3]



Truth Table

A	B	A<B	A>B	A=B
0	0	0	0	1
0	1	1	0	0
1	0	0	1	0
1	1	0	0	1

Figure 3: The Truth Table for the 1-bit Magnitude Comparator [3]



Truth Table

A1	A0	B1	B0	A<B	A=B	A>B
0	0	0	0	0	1	0
0	0	0	1	1	0	0
0	0	1	0	1	0	0
0	0	1	1	1	0	0
0	1	0	0	0	0	1
0	1	0	1	0	1	0
0	1	1	0	1	0	0
0	1	1	1	1	0	0
1	0	0	0	0	0	1

Figure 4 : 2-bit magnitude comparator Truth table sample [3]

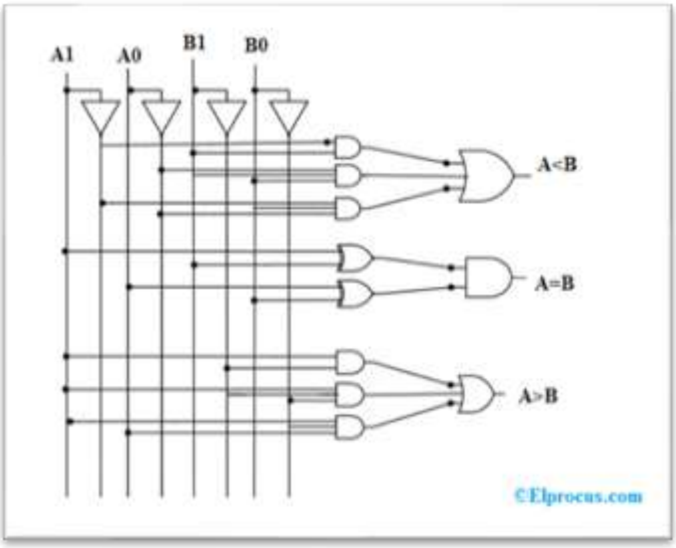


Figure 5: 2-bit magnitude comparator circuit design [3]

Digital comparators utilize Exclusive-NOR gates to compare the two different pairs of bits. When we compare two digital or BCD values or variables, we are looking at the "magnitude" of these values, a logic "0" versus a logic "1", which is where the phrase Magnitude Comparator originates from. In addition to contrasting individual bits, we can create bigger bit comparisons by cascading n of them to build an n-bit comparator, as we did with the n-bit adder in the last tutorial. Multi-bit comparators may be constructed to compare full binary or BCD words and return an output indicating whether one word is larger, equal to, or smaller than another. Four-bit Magnitude Comparator. Here, two 4-bit words ("nibbles") are compared to each other to create the required output, with one word connected to input A and the other to input B, as seen below [3].

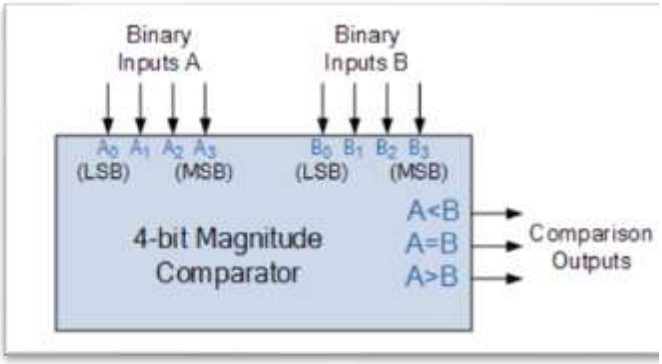


Figure 6: the 4-bit Magnitude comparator [3]

III. Design and Proceduer

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We are going to utilize 22 nm architecture with 0.1µm width for NMOS semiconductors, 0.2µm width for PMOS transistors, and a total length of 0.02µm. We'll deploy static gates and improve transistor sizing approaches. We decide on the 22 nm process for a variety of factors. First of all, it has minimal energy use thanks to characteristics like low-power transistors, fewer leakage currents that are chosen, and enhanced distribution of power connections, all of which lead to lower overall energy use in electronic devices. Second, the smaller dimensions of features in 22 nm technology allow for quicker switching rates and shorter transmission delays, resulting in enhanced efficiency and faster functioning, which is critical for our magnitude comparator. Finally, 22 nm technology guarantees dependability through extensive testing and validation procedures. The lower feature sizes increase resistance to noise and minimize sensitivity to numerous types of error, hence increasing the overall dependability of our device [4].

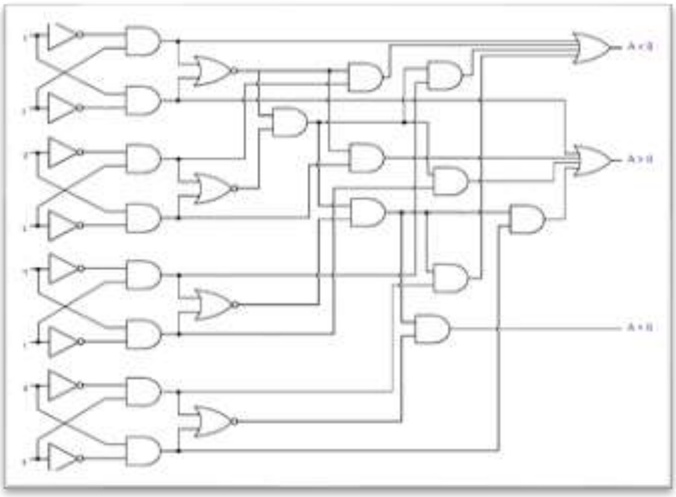
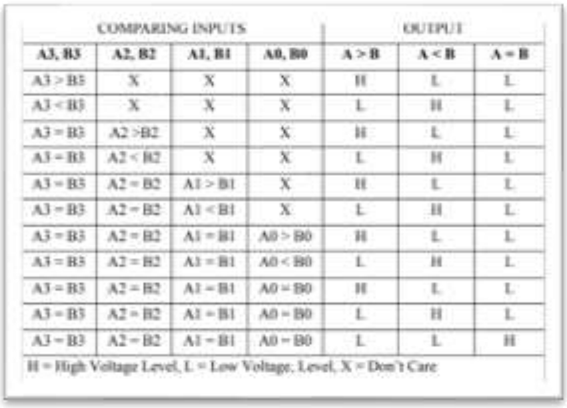


Figure 7: 4-bit Magnitude Comparator circuit [4]

(1) IF A= B : A3=B3, A2=B2, A1=B1, A0=B0 xi = AiBi + Ai’Bi’
 XOR-Invert = (AiBi’+Ai’Bi)’
 = (Ai’+Bi)(Ai+Bi’)
= Ai’Ai + Ai’Bi’ + AiBi + BiBi’
 = AiBi + Ai’Bi’
Output: x3x2x1x0
(2) IF A> B
Output: A3B’3 + x3A2B’2 + x3x2A1B’1+ x3x2x1A0B’0
(3) IF (A< B)
Output: A’3B3 + x3A’2B2 + x3x2A’1B1+ x3x2x1A’0B0



COMPARING INPUTS				OUTPUT		
A3, B3	A2, B2	A1, B1	A0, B0	A > B	A < B	A = B
A3 > B3	X	X	X	H	L	L
A3 < B3	X	X	X	L	H	L
A3 = B3	A2 >B2	X	X	H	L	L
A3 = B3	A2 < B2	X	X	L	H	L
A3 = B3	A2 = B2	A1 > B1	X	H	L	L
A3 = B3	A2 = B2	A1 < B1	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 > B0	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 < B0	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	H

H = High Voltage Level, L = Low Voltage; Level, X = Don't Care

Figure 8: Simple Truth Table

III.I Gates Circuits Design

Since the chosen procedure was the static gates, the circuits were built using the electric tool, and the process was to build the schematics, and the layout, then make an icon for the circuit.

1) Invertor

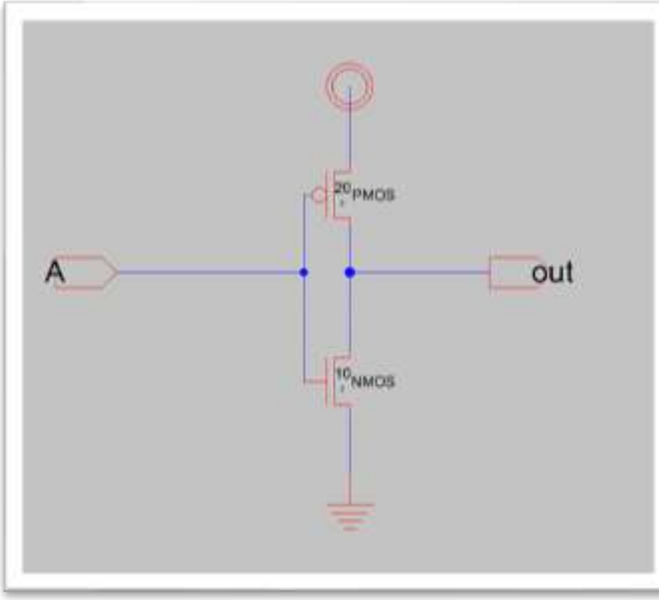


Figure 9: Invertor schematics

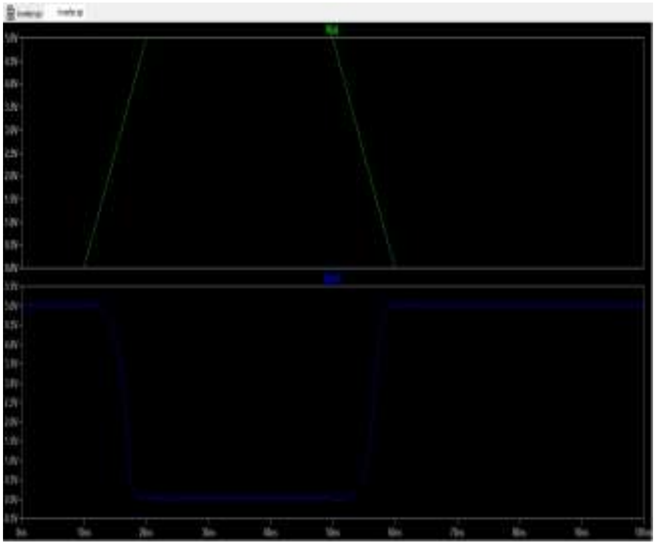


Figure 10: Invertor Simulation

Figure 9 represents the schematics of the inverter circuit, that was used later to implement the 4-bit magnitude comparator. The sizing was 20 to 2 for the PMOS, while the NMOS was 10-2, and that is related to the technology that was used, Figure 10 represents the simulation of the inverter circuit, and Figure 11 represents the layout of the inverter circuit

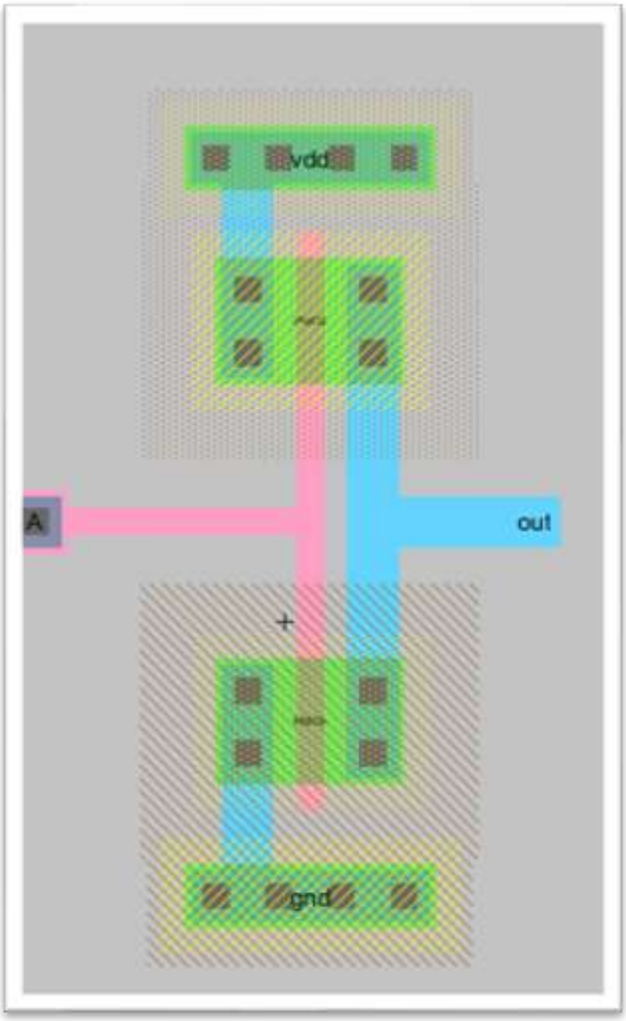


Figure 11: Invertor Layout

2) NOR

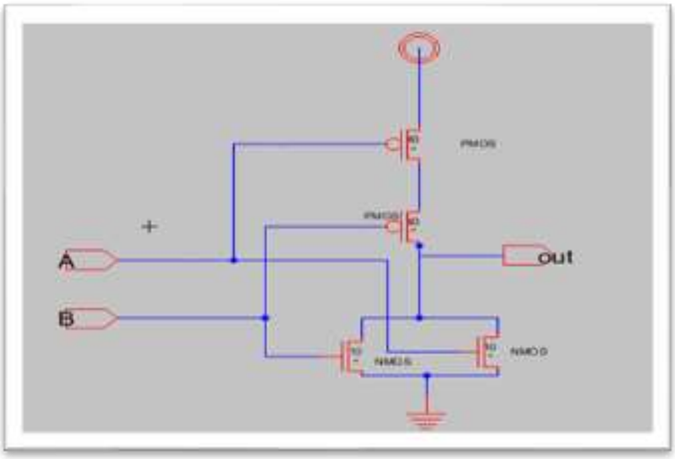


Figure 12: NOR schematics

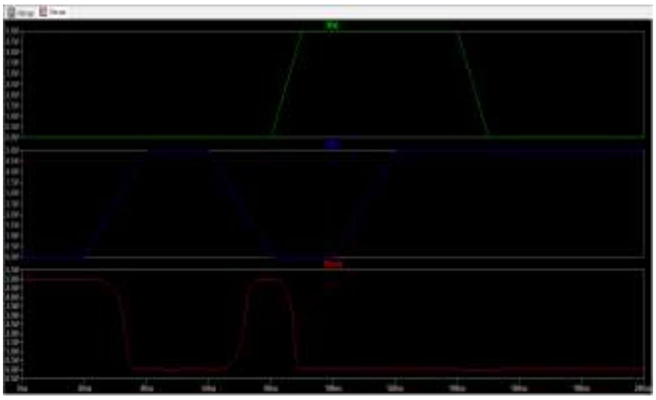


Figure 13: NOR Simulation

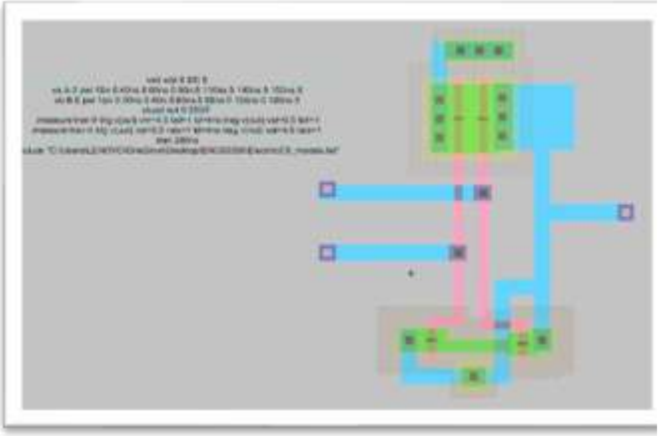


Figure 14: NOR Layout

Figure 12 shows the schematics of the NOR circuit, that was used later to implement the 4-bit magnitude comparator. The sizing was 20 to 2 for the PMOS, while the NMOS was 10-2, Figure 13 represents the simulation of the NOR circuit, and Figure 14 represents the layout of the NOR circuit.

3) 2-Input OR

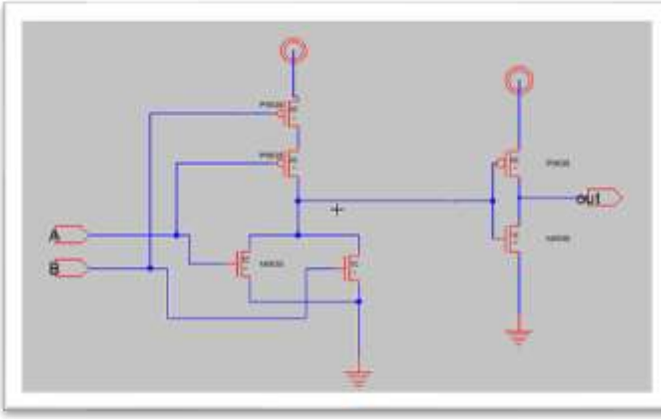


Figure 15: OR schematics

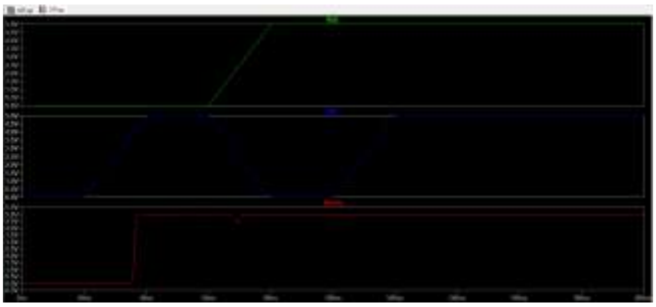


Figure 16: OR Simulation

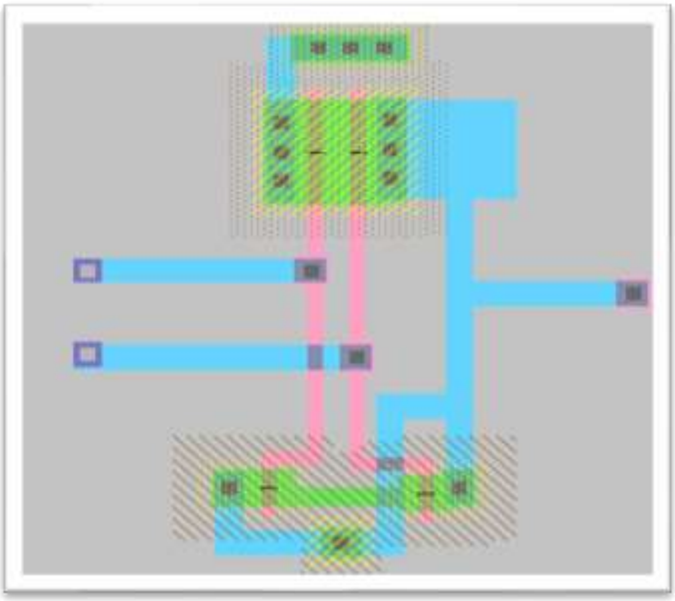


Figure 17: OR Layout

Figure 15 indicates the OR circuit's schematics, which were used later to implement the 4-bit magnitude comparator. The sizing was 20 to 2 for the PMOS, while the NMOS was 10 to 2, Figure 16 represents the OR circuit simulation, and Figure 17 represents the OR circuit layout.

4) AND

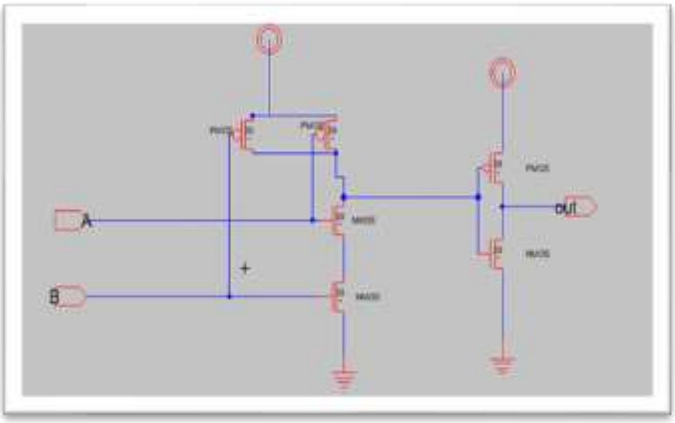


Figure 18: AND schematics

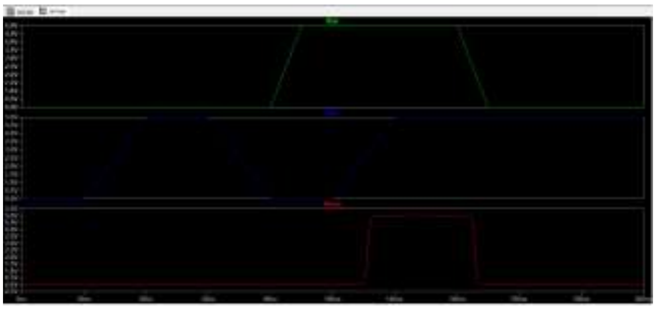


Figure 19: AND Simulation

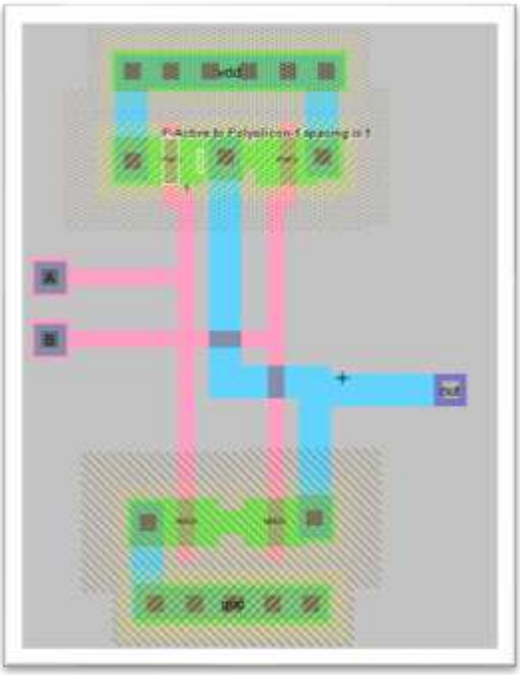


Figure 20: AND layout

Figure 18 shows the schematics of the AND circuit, that was used later to implement the 4-bit magnitude comparator. The sizing was 20 to 2 for the PMOS, while the NMOS was 10 to 2, Figure 19 represents the simulation of the AND circuit, and Figure 20 represents the layout of the AND circuit.

IV. Results of the comparator and its simulation

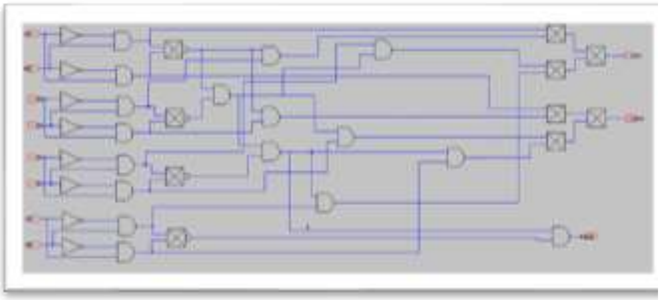


Figure 21: The Comparator Schematics

After building the schematics of the 4X4 magnitude comparator using the static gates, sizing techniques, and the 22nm technology, it was time for testing we built test cases and tried them via the code, and that will be shown in Figure 22.

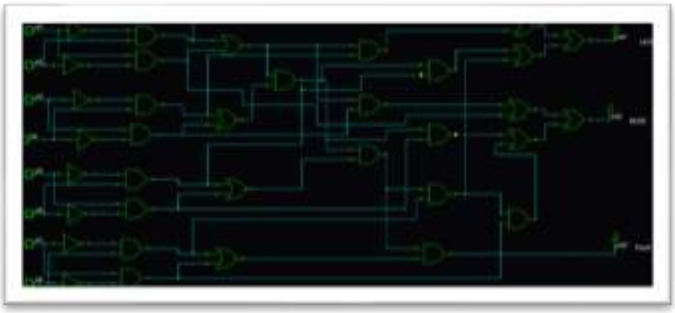


Figure 22: Schematics using Micro wind

Since the IC design is big we used the micro-wind tool to have a precise layout design, so the schematics were built again, and then a Verilog Code and spice code were used to generate the layout that is shown in Figure 23.

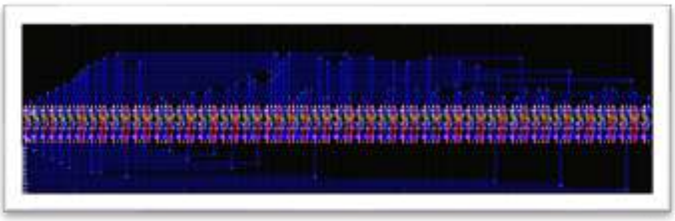


Figure 23: Comparator layout

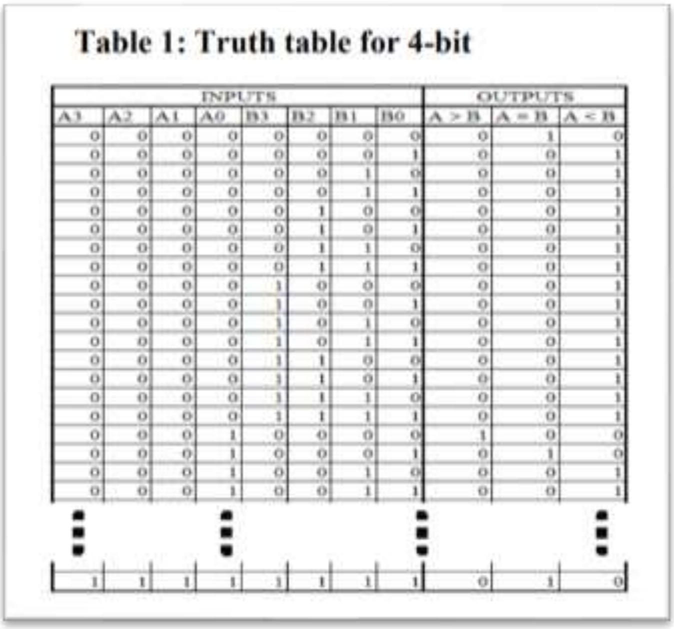
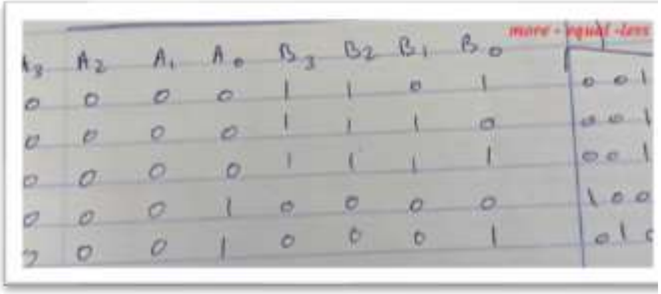


Table 1: Truth table for 4-bit

INPUTS								OUTPUTS		
A3	A2	A1	A0	B3	B2	B1	B0	A > B	A = B	A < B
0	0	0	0	0	0	0	0	0	1	0
0	0	0	0	0	0	0	1	0	0	1
0	0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	0	1	1	0	0	1
0	0	0	0	0	1	0	0	0	0	1
0	0	0	0	0	1	0	1	0	0	1
0	0	0	0	0	1	1	0	0	0	1
0	0	0	0	0	1	1	1	0	0	1
0	0	0	0	1	0	0	0	0	0	1
0	0	0	0	1	0	0	1	0	0	1
0	0	0	0	1	0	1	0	0	0	1
0	0	0	0	1	0	1	1	0	0	1
0	0	0	0	1	1	0	0	0	0	1
0	0	0	0	1	1	0	1	0	0	1
0	0	0	0	1	1	1	0	0	0	1
0	0	0	0	1	1	1	1	0	0	1
0	0	0	1	0	0	0	0	1	0	0
0	0	0	1	0	0	0	1	0	1	0
0	0	0	1	0	0	1	0	0	0	1
0	0	0	1	0	0	1	1	0	0	1
⋮			⋮				⋮			⋮
1	1	1	1	1	1	1	1	0	1	0

Figure 24: Truth table of the Comparator

Figure 24, shows the truth table that was built and followed in testing the design. Figure 23 indicates the test cases that were tried.



more - equal -less

A3	A2	A1	A0	B3	B2	B1	B0	more	equal	less
0	0	0	0	1	1	0	1	0	0	1
0	0	0	0	1	1	1	0	0	0	1
0	0	0	0	1	1	1	1	0	0	1
0	0	0	1	0	0	0	0	1	0	0
0	0	0	1	0	0	0	1	0	1	0

Figure 25: Test Cases

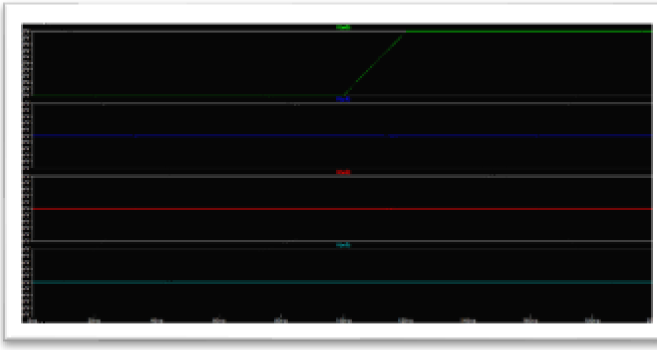
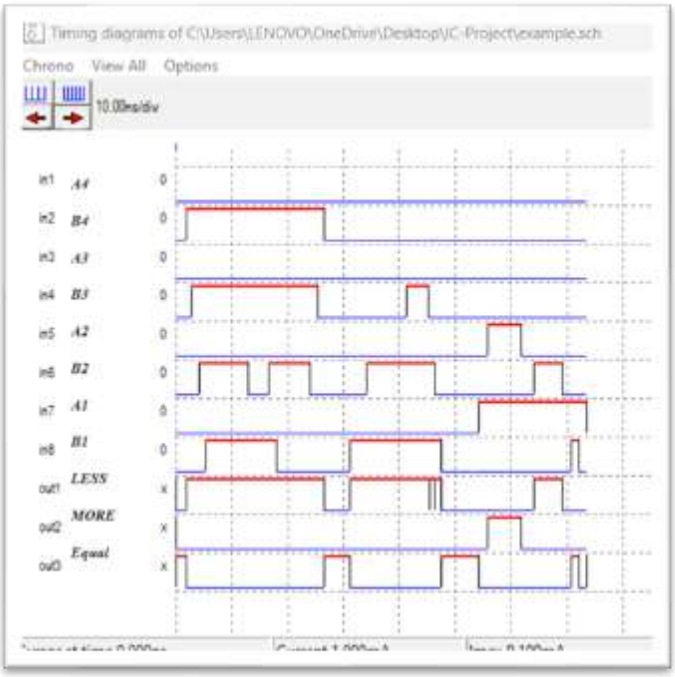


Figure 26: T the test case A

Figure 27: In the test case B



Timing diagrams of C:\Users\LENOVO\OneDrive\Desktop\IC-Project\example.sch

Figure 28: The simulation of the comparator

Various imperfections were discovered as related to the comparator's outcome. Variations or instabilities in the power supply created inconsistent voltage levels, resulting in drops or jumps in output signals. Accidental capacitance parasites in the circuit caused latencies and voltage dips between switching events, limiting short-term responsiveness. Incorrect transistor size had led to poor switching.

This leads to inaccurate or shifted output levels. Load improper impedance caused thoughts and voltage level difficulties since the load did not match the design resistance. Finally, differences between predicted and observed conduct resulted from simulation setting parameters that failed to sufficiently reflect real working conditions.

V. Conclusion and Future Improvement

Lastly, our study utilizes modern 22 nm technology to generate a high-performance and dependable 4-bit magnitude comparator. Our design addresses low-power and high-speed requirements with transistor widths of 0.1µm for NMOS, 0.2µm for PMOS, and lengths of 0.02µm. The use of static gates and transistor size optimization improves the efficiency and efficacy of our design.

The implementation of 22 nm technology has been driven by its built-in advantages in power usage, speed, and dependability. The low-power semiconductors and improved distribution systems for power greatly reduce total power consumption, while smaller feature sizes allow for quicker switching speeds and shorter transmission delays, resulting in improved performance. Furthermore, the thorough testing and validation processes related to advanced materials such as 22 nm, and decreased error sensitivity, provide an excellent basis for our comparator architecture.

In terms of power efficiency, 22 nm technology outperforms previous nodes such as 28 nm. the manufacturer TSMC, the 22nm technique reduces power consumption by 30% while preserving or even boosting performance parameters. This gain is due to lower feature sizes, which minimize leakage currents and optimize power distribution networks, hence improving total energy efficiency [5].

22nm ultra-low leakage (22ULL) technology development was completed and put into risk production in the fourth quarter of 2018 to enable IoT and wearable device applications. New ULL devices and ULL SRAM (static random-access memory) can consume less power than 40ULP and 55ULP solutions [5].

For improved performance of the 4-bit comparator shortly, many approaches might be investigated. Going to lower technological nodes, like as 14 nm or 10 nm, may substantially decrease power consumption and boost speed. Applying low-power design approaches, like dynamic voltage development, power blocking, and multi-threshold CMOS, can maximize power efficiency. Enhancing comparator algorithms can result in quicker decision-making and decreased power usage. these solutions can boost the effectiveness, energy conservation, and dependability of the comparator.

VI. References

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