Project Instructions :

- 2-3 in each group
- Due date **Wednesday 22 May 2024**
- Idea: Design of Low Power NXN Magnitude or Signed Comparator Using [DEFINE YOUR TECHNIQUES] Technique

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Introduction

Digital Comparator

Motovations

Literature Review

Digital Comparator

Comparator Architectures

Add as much as you can summary and table to compare existing methods, speed, power ..etc

Proposed Multiplier Architecture/Algorithm

- ***Schematic and layout of the* Comparator *cell.***
- ***Annotate schematic with gate sizes***
- ***Simulation showing worst case propogation delay using ??nm Electric EDA tool***
- ***Identify the critial path and show hand calculation of delay and power. Worst-case delay simulation showing the critical signals. Explain your design decisions and approach. Schematics of any new and non-obvious gates.***
- ***Annotated schematic or block diagram and layout of the complete array. Simulation showing functional read with worst-case delay and timing of critical signals,***
- ***You should provide highlights of the key optimizations/design decisions you made***

Results & Performance Comparison

- Grades will be based on
  - Power, Area, Speed, Optimizations
  - Simulations results for schematic and layout
  - Report in Journal format from

Title: Design of Low Power NXN Magnitude Comparator Using [DEFINE YOUR TECHNIQUES] Technique

Abstract :

Design for Low power, high speed and reliable design is a very important role in emerging technologies in Integrated circuit. To reduce power consumption and propagation delay involved in the circuit , the paper presents YOUR TECHNIQUES technique for implementation of digital logic circuit . In this paper ,nxn bit magnitude /Signed comparator is designed using conventional CMOS logic style and YOUR TECHNIQUES technique. The proposed YOUR TECHNIQUES magnitude /Signed Comparator requires ??? transistors and implementation using CMOS logic requires 226 transistors. The power consumed by the nxn bit magnitude /Signed CMOS comparator is ?? µw and the power consumed by the nxn YOUR TECHNIQUES magnitude /Signed I comparator is YOUR DESIGN which is very less/LARGER as compared to conventional CMOS Style. Delay present in the conventional CMOS magnitude comparator is in ???µsec whereas the delay produced by YOUR TECHNIQUES for magnitude comparator ??µsec. Delay is also reduced in the proposed YOUR TECHNIQUES. Thus proposed YOUR TECHNIQUES technique shows ???% efficiency for power measurement. All this circuit simulation is done by using ELECTRIC TOOL EDA version ?? at ?? nm process technology.

References :

- https://papers.ssrn.com/sol3/papers.cfm?abstract_id=3166515
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