AMSL Report

DASHUN LIU

s2608687@ed.ac.uk

1 Introduction

The purpose of this course is to create PCB boards and to implement the conversion of light signals LiFi into audio signals, displaying part of the signals on an oscilloscope, testing related performance, and recording data such as Q-factor, Bandwidth, etc. The main body of the circuit consists of seven blocks: power protection circuit, TIA, HPF, Sallen-Key active filter, Amp-2, path-1, and path-2.

2.1 Power protection circuit

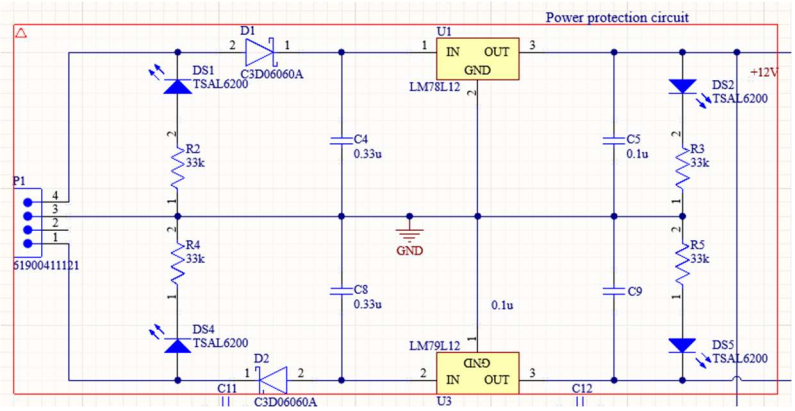


Figure 1，schematic of Power protection circuit

The description involves setting up a circuit with a 4-position header (P1) shown in figure1, through which +15V DC voltage is provided at pin 4, -15V DC voltage at pin 1, and ground is connected at pin 3. Pin 2 can also be grounded, although it's not grounded in the diagram provided. The key components of this circuit are the LM78L12 and LM79L12 chips. For LM78L12, pin 2 should be grounded, while for LM79L12, pin 1 should be grounded. Reversing these connections, such as swapping pins 2 and 3 on the LM78L12, may cause the chip to overheat. DS1 and DS4 are red diodes; DS2 and DS5 are green diodes. If connected correctly, the green lights will be on, and the red lights will be off. D1 and D2 are diodes, and their orientation is important. The primary purpose of this circuit is to provide +12V and -12V voltages, as well as a ground connection.

2.2 TIA

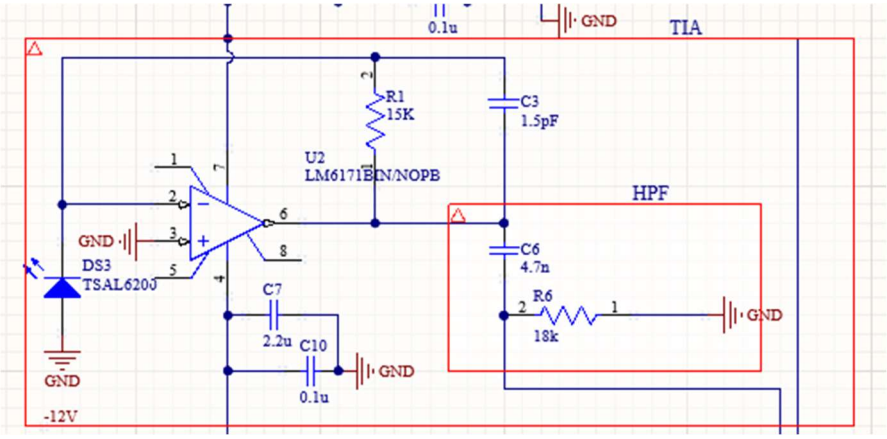


Figure 2，schematic of TIA

TIA is trans-impedance amplifier shown in figure 2, whose aim is converting the input current from photo-diode into output voltage. The chip used is the LM6171, which requires a ±12V voltage, as well as the corresponding protection capacitors (consisting of 2.2u and 0.1u capacitors). Among them, R1 and C3 are related to the cutoff frequency, according to the formula:

$$f_{-3dB} = \sqrt{\frac{GBW}{2\pi C_T R_1}} \qquad C_3 = \sqrt{\frac{C_T}{2\pi R_1 (GBW)}}$$

From the given datasheet, $C_T = C_{PD} + C_{IN} + C_{stray}$, $C_{PD} = 11pF$, $C_{IN} = 10pF$, C_{stray} can be ignored for the moment, and $GBW = 100MHz$, so can get the

$$f_{-3dB} = 8.71 \times 10^8 \sqrt{\frac{1}{R_1}} \qquad C_1 = 1.83 \times 10^{-10} \sqrt{\frac{1}{R_1}}$$

When the resistor is equal to 12K, the frequency is 7.11Mhz and the capacitor is 1.5pF.

2.3 HPF

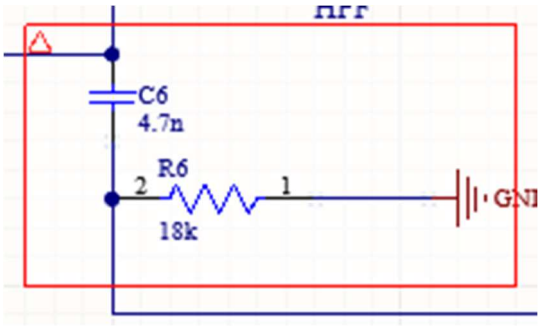


Figure 3，schematic of HPF

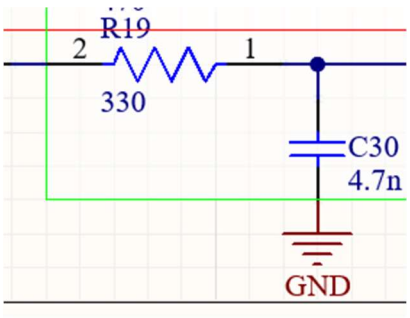


Figure 4，schematic of LPF

HPF (high pass filter) shown in figure 3 is the next block after TIA, and LPF (low pass filter) shown in figure 4 is associated with it. For both of them are used in this circuits, and they have same cut-off frequency:

$$f_{-3dB} = \frac{1}{2\pi RC}$$

The distinction between High Pass Filters (HPF) and Low Pass Filters (LPF) lies in their frequency handling capabilities: HPFs allow frequencies higher than the cutoff frequency to pass, whereas LPFs enable frequencies lower than a certain cutoff frequency to go through. When an HPF is connected after a Transimpedance Amplifier (TIA), its aim is to filter out noise emanating from direct current (DC) sources. For this purpose, the cutoff frequency is set to be approximately under 2 kHz. The selection of resistor and capacitor values, 18k ohms and 4.7n farads respectively, is crucial in achieving the desired cutoff frequency, in this case, around 1.88 kHz.

2.4 Sallen-key active filter

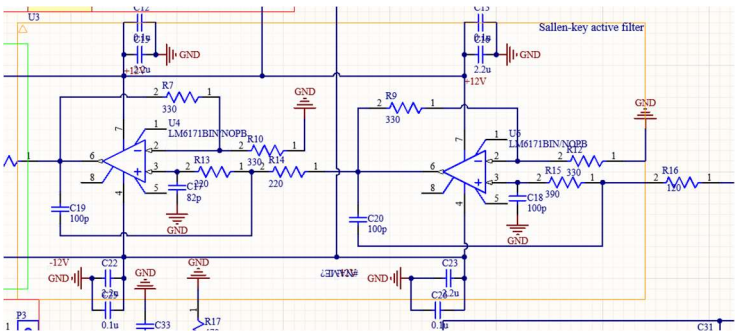
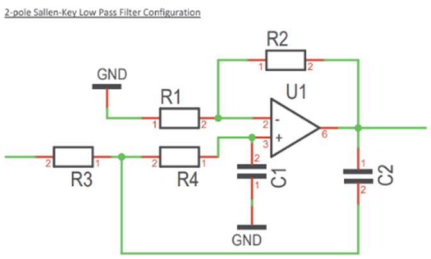


Figure 5，schematic of Sallen-key active filter

The part following HPF is Sallen-key active filter which is composed of two 2-pole Sallen-key low pass filters shown in figure 6. The important points of 2-pole Sallen-key low pass filters (shown as below) are their cut-off frequency, gain and Q-factor, their simplified formula are:



$$f_{c(LPF)} = \frac{1}{2\pi\sqrt{R_3 R_4 C_1 C_2}}$$

$$Gain = 1 + \frac{R_2}{R_1}$$

$$Q = \frac{\sqrt{R_3 R_4 C_1 C_2}}{R_3 C_1 + R_4 C_1 - \frac{R_3 R_2}{R_1} C_2} = \frac{\sqrt{\frac{R_4}{R_3}\frac{C_2}{C_1}}}{1 + \frac{R_4}{R_3} - \frac{R_2}{R_1}\frac{C_2}{C_1}}$$

Figure 6，circuit of 2-pole Sallen-key low pass filter

The requirements for the Sallen-Key active filter are "Filter order ≥ 4, frequency f between 3MHz and 8MHz," "Q1=0.54, Q2=1.31" shown in table 1[(1)]. There is a considerable amount of target data needed, so it is more convenient to use Excel spreadsheets to assist with calculations. Moreover, by setting the gain value to 2, thus making R2 equal to R1, the calculation can be simplified. The budget results follow in. Another point to note is that this uses the LM6171 chip, so attention must be paid to the positive and negative 12 volts of voltage as well as grounding.

Table 1. Butterworth Filter Table

FILTER ORDER	Stage 1		Stage 2		Stage 3		Stage 4		Stage 5	
	FSF	Q	FSF	Q	FSF	Q	FSF	Q	FSF	Q
2	1.000	0.7071								
3	1.000	1.0000	1.000							
4	1.000	0.5412	1.000	1.3065						
5	1.000	0.6180	1.000	1.6181	1.000					
6	1.000	0.5177	1.000	0.7071	1.000	1.9320				
7	1.000	0.5549	1.000	0.8019	1.000	2.2472	1.000			
8	1.000	0.5098	1.000	0.6013	1.000	0.8999	1.000	2.5628		
9	1.000	0.5321	1.000	0.6527	1.000	1.0000	1.000	2.8802	1.000	
10	1.000	0.5062	1.000	0.5612	1.000	0.7071	1.000	1.1013	1.000	3.1969

Table 1，table of Butterworth filter

Values of Sallen-key active filter				
R3	120	R1	330	
R4	390	R2	330	
C1	1E-10	F1	7.35694	3< <8
C2	1E-10	Q1	0.5547	0.54
R3	220	R1	330	
R4	220	R2	330	
C1	8.2E-11	F2	7.988965	3< <8
C2	1E-10	Q2	1.414904	1.3

Table 2, outcome of the values of Rs and Cs

2.5 Amp-2

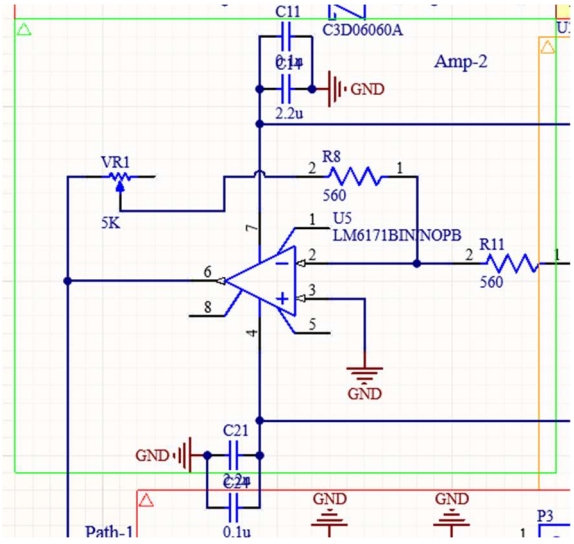


Figure 7，schematic of Amp-2

Amp-2 is an inverting amplifier shown in the figure 7. Its function is to adjust the amplification factor based on the slide potentiometer, achieving the purpose of amplifying the voltage. The specified range of amplification factor adjustment for Amp-2 is [0dB, 20dB], which corresponds to a voltage amplification from 1 to 10 times, which means that $\frac{VR_1 + R_8}{R_{11}} \in [1, 10]$. The actual values for resistors R8 and R11 are 560 ohms, and for the variable resistor VR1, it's 5k ohms. This results in an actual amplification range of 1 to 9.93 times. Additionally, the chip used in this design is the LM6171.

2.6 Path-1

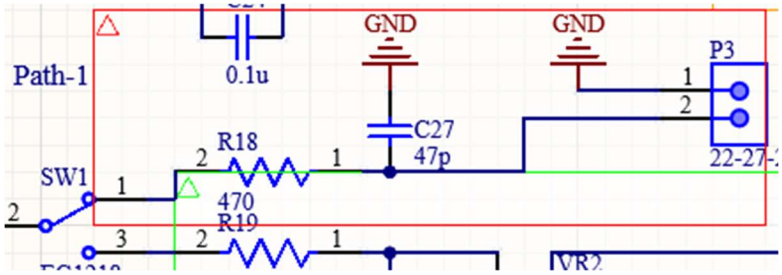


Figure 8，schematic of Amp-2

Connected to amp-2 is a double-throw switch SW1, which controls the selection between path-1 and path-2. Path-1 shown in figure 8 primarily consists of a low-pass filter and a detection point. The details of the low-pass filter are mentioned in the HPF section. The selected resistance is 470 ohms, and the capacitance is 47 pF, with an actual cutoff frequency of 7.20 MHz. And the output end of LPF is connected to P3, which is 2 ways board header, and this is not directly provided when soldering PCB board, we need to cut 4 ways board header in half.

2.7 Path-2

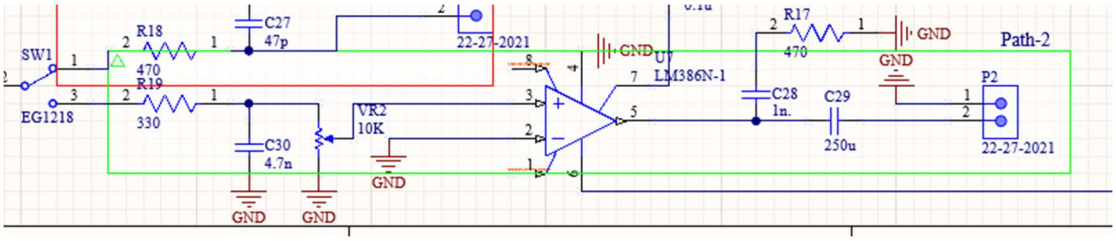


Figure 9，schematic of Amp-2

In the other path, path-2 shown in figure 9, there is also a Low-Pass Filter (LPF), but its cutoff frequency is set to 100kHz, which differs from path-1's 3MHz to 8MHz range. The selected resistance is 330 ohms, and the capacitance is 4.7nF, resulting in an actual cutoff frequency of 103kHz. The difference between the two paths is due to the varying frequency requirements for audio out and signal out. Following the LPF is an audio amplifier, as illustrated below. Adjusting a 10k sliding potentiometer can change the final audio volume, similar to its function in amp-2, and the chip used here is LM386 rather than LM6171, and there should exist positive 12 voltage on the pin 6 of LM386[(2)].

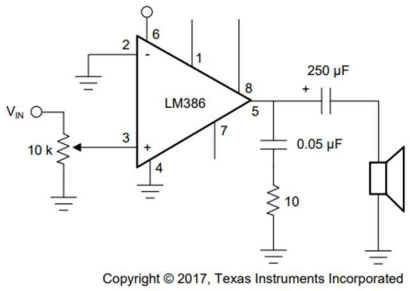


Figure 10，circuit of audio amplifier

2.8 Overall Schematic

During the process of sequentially connecting the aforementioned blocks, there are some key points to note. Firstly, it is not necessary to number the components at the beginning; instead, wait until the basic assembly is complete, then use "annotate schematic" (found under "annotate" in the "design" menu).

Secondly, components used in schematics should be chosen through the "Manufacturer Part Search" panel instead of the generic "component" library in Altium Designer. This distinction is important because items selected from the "component" library are typically intended for simulation purposes and lack the physical

footprints necessary for PCB design.

Moreover, for presentation purposes, different areas can be marked as shown in the diagram on the left. Furthermore, for specific values and search names of various components, refer to the table below. Additionally, requirements for components such as 2.54 pitch, through-hole resistor, etc., should be noted.

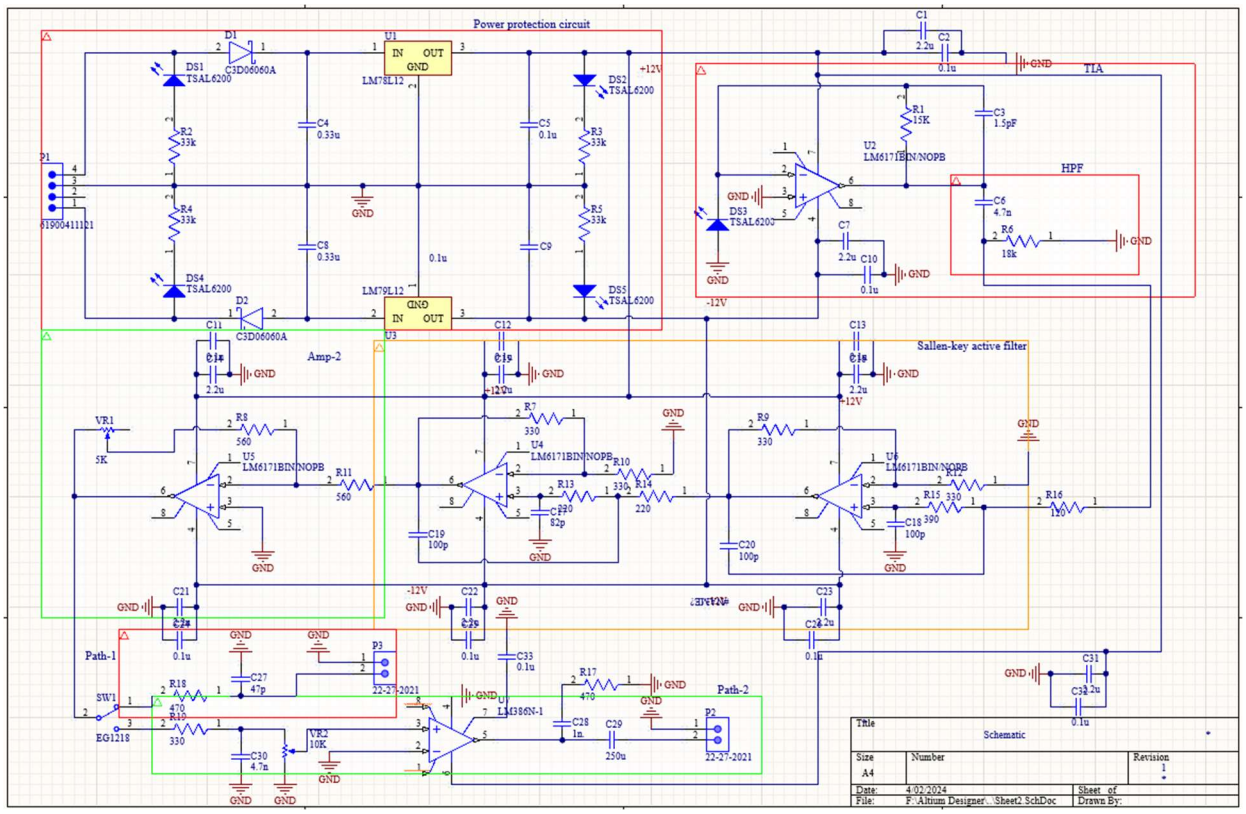


Figure 11，overall schematic

Designator	Name to seach	Name/value	Designator	Name to seach	Name/value	Designator	Name to seach	Name/value
R1	RLR07C1002FSB14	15K	U3	LM7912CT/NOPB	LM79L12	C17	C330C105M5U5TA	82p
R2	RLR07C1002FSB14	33k	U1	LM340T-12	LM78L12	C18	C330C105M5U5TA	100p
R3	RLR07C1002FSB14	33k	P1	61900411121	61900411121	C19	C330C105M5U5TA	100p
R4	RLR07C1002FSB14	33k	SW1	EG1218	EG1218	C20	C330C105M5U5TA	100p
R5	RL R07C1002FSB14	33k	VR1	3362P-1-104LF	5K	C21	C330C105M5U5TA	2.2u
R6	RL R07C1002FSB14	18k	VR2	3362P-1-104LF	10K	C22	C330C105M5U5TA	2.2u
R7	RL R07C1002FSB14	330	P2	22-27-2021	22-27-2021	C23	C330C105M5U5TA	2.2u
R8	RL R07C1002FSB14	560	P3	22-27-2021	22-27-2021	C24	C330C105M5U5TA	0.1u
R9	RL R07C1002FSB14	330	C1	C 330C 105M5U5TA	2.2u	C25	C330C105M5U5TA	0.1u
R10	RL R07C1002FSB14	330	C2	C330C105M5U5TA	0.1u	C26	C330C105M5U5TA	0.1u
R11	RLR07C1002FSB14	560	C3	C330C105M5U5TA	1.5pF	C27	C330C105M5U5TA	47p
R12	RLR07C1002FSB14	330	C4	C330C105M5U5TA	0.33u	C28	C330C105M5U5TA	1n.
R13	RLR07C1002FSB14	220	C5	C330C105M5U5TA	0.1u	C29	C330C105M5U5TA	250u
R14	RLR07C1002FSB14	220	C6	C330C105M5U5TA	4.7n	C30	C330C105M5U5TA	4.7n
R15	RLR07C1002FSB14	390	C7	C330C105M5U5TA	2.2u	C31	C330C105M5U5TA	2.2u
R16	RLR07C1002FSB14	120	C8	C330C105M5U5TA	0.33u	C32	C330C105M5U5TA	0.1u
R17	RLR07C1002FSB14	470	C9	C330C105M5U5TA	0.1u	C33	C330C105M5U5TA	0.1u
R18	RL R07C1002FSB14	470	C10	C330C105M5U5TA	0.1u	DS1	TSAL6200	TSAL6200
R19	RL R07C1002FSB14	330	C11	C330C105M5U5TA	0.1u	DS2	TSAL6200	TSAL6200
U2	LM6171BIN/NOPB	LM6171BIN/NOPB	C12	C330C105M5U5TA	0.1u	DS3	TSAL6200	TSAL6200
U4	LM6171BIN/NOPB	LM6171BIN/NOPB	C13	C330C105M5U5TA	0.1u	DS4	TSAL6200	TSAL6200
U5	LM6171BIN/NOPB	LM6171BIN/NOPB	C14	C330C105M5U5TA	2.2u	DS5	TSAL6200	TSAL6200
U6	LM6171BIN/NOPB	LM6171BIN/NOPB	C15	C330C105M5U5TA	2.2u	D1	C3D06060A	C3D06060A
U7	LM386N-1	LM386N-1	C16	C330C105M5U5TA	2.2u	D2	C3D06060A	C3D06060A

Table 3, the data of all components in schematic

3.1 PCB board design

After finalizing the components and structure of the schematic, you can convert it to a PCB via the "Update" option in the "Design" menu. Once converted, check that all components are correct and meet requirements. The next step involves adjusting the "rules", such as setting the power and ground lines to a width of 1mm, signal lines to 0.5mm, and ensuring a track separation of no less than 0.5mm.

Next, adjust the shape of the PCB board. This can be addressed later during the copper pouring process. First, set the origin point (E+O+S), then start drawing the border from this origin point. After selecting the border, form the board shape (D+S+T). You can add arcs to the corners of the board to prevent cuts. For components with names that are too large, you can adjust them together using the "find similar objects" feature.

Following this, you can place components, starting with the power interface at the edge of the board. Then, place components according to their block, ensuring to avoid placing components too densely and trying to keep chip orientations as consistent as possible. After placement, consider routing. Since the PCB requires single-layer routing, which can be challenging, outline the positive and negative 12-volt power lines first—one on the perimeter and one internally. Then, start routing according to the blocks, using the gaps between components for crossing when components are enclosed by lines.

After adding the name, can proceed with copper pouring. Since the polygon plane needs to be grounded, select GND for the polygon plane's net. Also, note that copper pouring should be done on the bottom layer. Regarding the PCB reference, the four mounting holes need not be drawn; lab personnel will add them. The school emblem might not print on the final board if it's on the top layer.

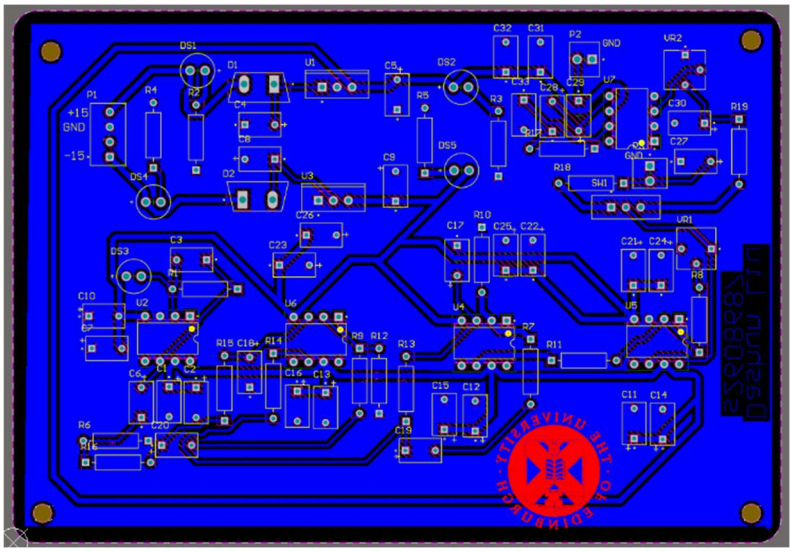


Figure 12，PCB in 2D

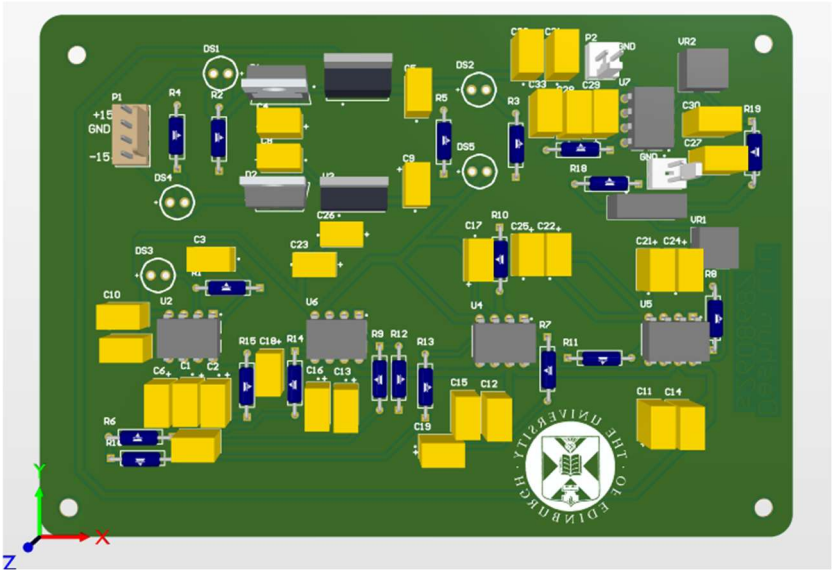


Figure 13，PCB in 3D

3.2 PCB board solder

After printing the PCB board, conduct an initial inspection to identify any easily noticeable issues before proceeding

with soldering. Begin by connecting and soldering the components of the voltage protection circuit, then test the positive and negative 12-volt outputs. Generally, if the green LED lights up normally, there should be no problem. Next is the TIA. After connecting the TIA, you need to check its output voltage, which typically should be a sine voltage between 80mV and 160mV. Regarding capacitor C3, theoretically, its value is 1.5F, but such a small capacitor does not exist, and it has been found that not soldering the capacitor (C3=0) yields better results. Following that, each 2-pole Sallen-Key filter must be tested for its cutoff frequency, maximum voltage, and amplification factor, with similar methods applied to test the other parts.

For issues with the audio output not producing sound, further investigation can be done by checking its voltage output. If one green light is on and the other is off, observing the DC power supply might reveal that one side's output voltage is significantly less than 15 volts. At this point, it's advisable to use a digital multimeter in ACV and Cont modes to inspect the circuit. The issue could be due to a poorly soldered voltage input, a malfunctioning capacitor or chip, a burnt-out LED, or excessive solder causing a short circuit.

Other potential issues with the PCB board may include un-drilled component holes or incorrect circuit design requiring jump wires. These issues can be attempted to be resolved independently, but it's crucial to understand the problem clearly to avoid further mistakes.

4.1 Frequency response measurement and Bode plot creation (Task F)

In this section, two measurements are required: one for the breadboard and one for the output of path-1 on the PCB board. The measurement method for both is similar. After connecting the board to be measured, the transmitter board, and the power supply, connect the oscilloscope to the transmitter board and place the 1m optical fiber in the photodiode. Then, connect one end of the oscilloscope's trigger to the test pin and the other end to the ground. Turn on the power supply, press the wave gen button, and the wave gen settings will be displayed.

According to the requirements, "Set the signal generator to a sine wave of frequency 200 kHz, 125 mV peak-to-peak amplitude, and output impedance of 50Ω." Then, adjust the first sliding resistor on the board to set the Vout (i.e., the pk-pk value on the oscilloscope) between 1 to 2 volts, with anything below 2 volts being acceptable. Record the Vout data at this time, and use a step increase of no more than 500kHz to increase the frequency. Record the Vout at each frequency and process the Vout data by $G = 20\log_{10}\left(\frac{V_{out}}{V_{in}}\right)$. Then using MATLAB, Excel, or Python to draw the Bode plots for the breadboard and PCB board which are shown in the figure below.

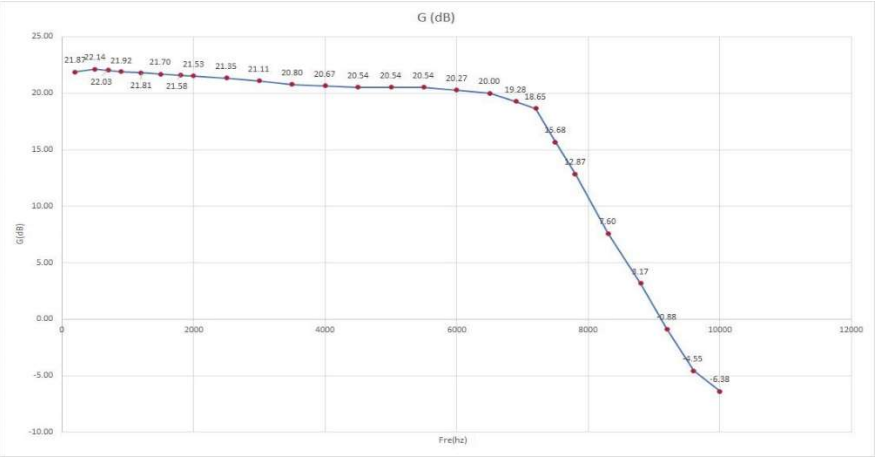


Figure 14, bode diagram for bread board

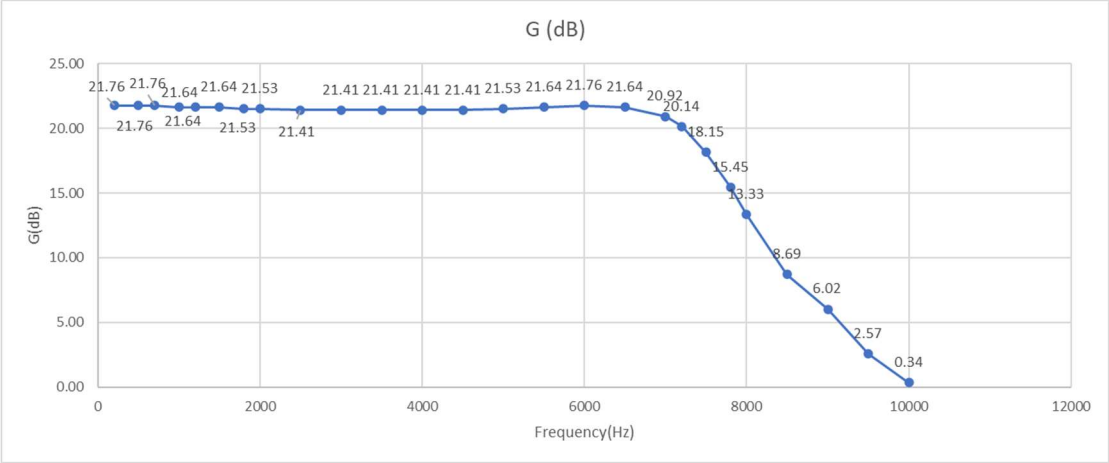


Figure 15, bode diagram for PCB

It can be observed that the cutoff frequency on the breadboard is around 7000Hz, while on the PCB, it's approximately 7200Hz. Additionally, there are other subtle differences, such as the rate of voltage drop, which could be attributed to the parasitic capacitance on the breadboard, the use of different oscilloscopes, and the replacement of the transmitter board during the process.

Block	Sallen-key1	Sallen-key2	LPF-2
Fre(MHz)	7.357	7.989	7.205

Table 4, the cutoff frequency of each block

Since the final cutoff frequency of this circuit is determined by the lowest cutoff frequency, the cutoff frequencies of modules with a cutoff frequency have a minimum value of 7.205MHz, which aligns closely with the results on the PCB. The corresponding bandwidth is 7.2MHz.

4.2 Record rise time and compare bandwidth (Task I)

First, connect all the boards as in Task F, and then set the signal generator according to the requirements: "125 mV Vpp, 50% duty cycle, 50 output impedance, 100 kHz frequency." After pressing the “mess” button, add measurements for rise time and fall time. Adjust the sliding resistor to make the peak-to-peak value of the received signal approximately 1.5V, recording the rise time and fall time as 56.5ns and 53.0ns, respectively. Through multiple measurements, it was found that the rise time is always greater than the fall time, possibly due to the circuit design, leading to different charging and discharging times of the current.

According to the given formula $B_{theoretical} \cong \frac{0.35}{t_r}$ $t_r = 56.5ns$, the theoretical bandwidth is 6.195MHz, which is less than the actual bandwidth of 7.2MHz. This discrepancy might have several reasons: first, the theoretical bandwidth formula might not fully apply to the target circuit 1, which corresponds to an ideal first-order RC circuit[3]. Second, the measured rise time might be slightly larger, resulting in a smaller value for the theoretical bandwidth. Third, many oscilloscopes have a faster roll-off to provide a flatter frequency response in the pass band, potentially increasing the numerator to 0.45 or even higher.

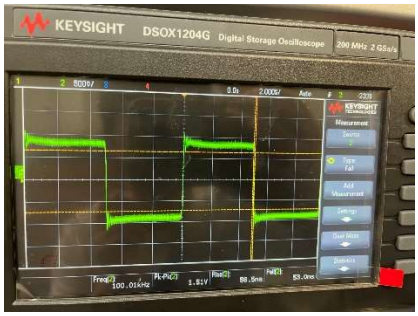


Figure 16, the rise time and fall time on oscilloscope

4.3 Measure the performance of an optical data transmission(Task K)

1) Estimate the received signal power, P_{signal}

Just use the same set-up in Task J, record received signal peak-to-peak value $V_{Rxd}=1.51V$, and get the received signal power $P_{signal}=V_{Rxd}^2/4R_{Load}=1.51^2/200=0.0114005$.

2) Estimate the received noise power, σ_{Noise}^2

Switch off the transmitter and copy the noise signals from oscilloscope by U-drives, then use software get the corresponding histogram, the diagram shown as below

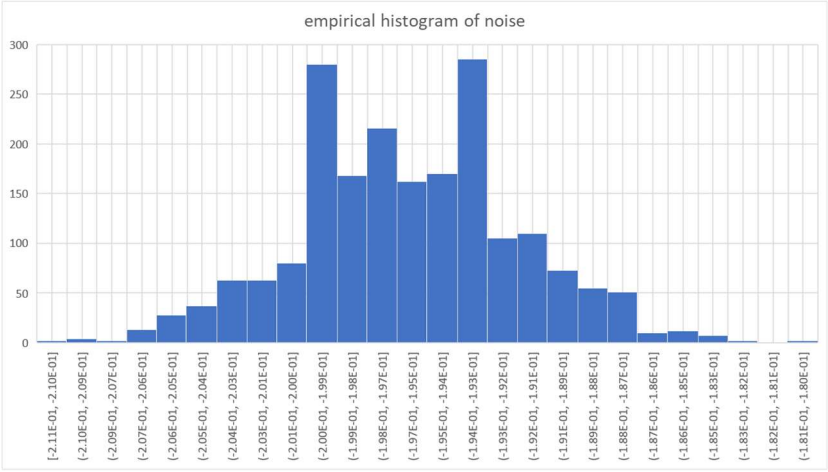


Figure 17, histogram of noise

The histogram should follow a random or Poisson distribution. However, the noise is more concentrated in the ranges [-0.200, -0.199] and [-0.194, -0.193], which could be due to specific environmental interference or insufficient data. This phenomenon suggests that the received noise power may not be uniformly distributed across the measured spectrum. Such concentrations of noise could indicate anomalies in the data collection process or external factors affecting the signal. The received noise power $\sigma_{Noise}^2=1.95E-05$.

3) Estimate the received signal-to-noise ratio, SNR.

$$SNR=P_{signal}/\sigma_{Noise}^2=0.0114/(1.95\times10^{-5})=584.615$$

4) Estimate the maximum possible data rate, R.

$$R\leqslant B\log_2(1+SNR)=6.195\times\log_2(1+584.615)=56.9556$$

5) Calculate the Q-factor.

$$Q-factor=V_{Rxd}/2\sigma_{Noise}=1.51/\left(2\sqrt{1.95\times10^{-5}}\right)=170.974$$

6) Briefly discuss and comment on the estimated maximum attainable data rate, R, and the Q-factor in relation to error performance

The maximum data rate R of a channel depends on the bandwidth B of the channel and the Signal-to-Noise Ratio (SNR), highlighting the importance of noise reduction in information transmission. However, due to network congestion, signal attenuation, interference, and hardware performance limitations, it's often challenging to reach the estimated maximum attainable data rate R. The size of the Q-factor is inversely related to the amount of noise, but it is also associated with Intersymbol Interference (ISI), which is caused by long time domain received symbol tails. Since ISI can be improved through the use of an equalizer, introducing an equalizer may lead to increased noise. Therefore, a balance between noise and ISI must be achieved to obtain a satisfactory Q-factor.

5 Personal understanding

This course is time-consuming, despite being only 12 weeks long. It spans from breadboard experimentation to schematics, PCB design, PCB soldering, PCB debugging, and summarizing reports, with a significant portion of time devoted to debugging. The breadboard testing is crucial during this process but often doesn't receive enough attention in the early stages of the course. The fine-tuning of outputs usually takes place on the PCB, hence the PCB's appearance may not be flawless. Overall, I gained a lot from this course, but it required a substantial amount of time outside of scheduled class hours

6 Used devices

The used devices: DSOX1204G Digital Storage Oscilloscope, EDU34450A 5 1/2 Digit Multimeter, EDU36311A Triple Output Programmable DC Power Supply, soldering machine

7 Reference

(1)
”Active Low-Pass Filter Design” Jim Karki, Texas Instruments, September 2002
https://www.ti.com/lit/an/sloa049d/sloa049d.pdf?ts=1712216396557
(2)
“LM386 Low Voltage Audio Power Amplifier” Texas Instruments, August 2023
https://www.ti.com/lit/ds/symlink/lm386.pdf?ts=1712267852897&ref_url=https%253A%252F%252Fwww.mouser.co.uk%252F
(3)
“Rise Time, Frequency Response, and 3 dB Bandwidth” Thorlabs,
https://www.thorlabs.com/images/TabImages/Rise_Time_3dB_Bandwidth_Relationship_Lab_Fact.pdf

The theoretical bandwidth:

The frequency response magnitude (H) of first order low pass filter circuit can be showed as

$$|H(2\pi f)| = \frac{1}{\sqrt{[2\pi fRC]^2+1}}$$

For -3db,

$$\left|\frac{\sqrt{2}}{2}\right| = \frac{1}{\sqrt{[2\pi fRC]^2+1}} \Rightarrow f = \frac{1}{2\pi RC}$$

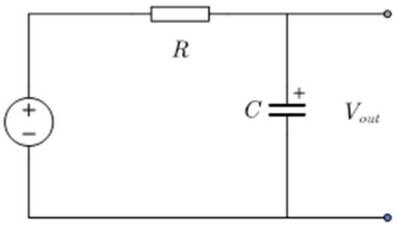


figure 18, RC circuit

And the time-dependent equation for the rising edge of a pulse is

$$v_{out}(t) = v_{in}(1-e^{-t/RC})$$

Additionally rise time is t1-t2, and the amplitude at t1 is 0.1, the amplitude at t2 is 0.9, so

$$0.1v_{in} = v_{in}(1-e^{-t_1/RC}),\ 0.9v_{in} = v_{in}(1-e^{-t_2/RC}) \ \Rightarrow\ t_r = RC\ln 9 = \frac{\ln 9}{2\pi f} \cong \frac{0.35}{f}$$