電子學(一) 期末考 Chapter 6, 3.1~3.4, 4.1~4.7 2023.12.18 10:20-12:10

($V_{BE}(\text{on}) = 0.7$ V, $V_{CE}(\text{sat}) = 0.2$ V, $V_A = \infty$, and $\beta = 100$ if not specifically mentioned)

1. (12%) For the circuit shown in Figure 1, the transistor parameters are $\beta = 100$, and $V_A = \infty$. (a) Determine the dc voltages at the collector, base, and emitter terminals. (b) Determine the small-signal voltage gain $A_v = v_o/v_s$. (c) Find the input resistance R_i.

2. (10%) For the circuit shown in Figure 2, the transistor parameters are $\beta = 100$, and $V_A = \infty$. The total instantaneous C-E voltage is to remain in the range $0.5 \le v_{CE} \le 20$ V and the total instantaneous collector current is $i_C \ge 0.2$ mA. (a) Find the value of I_{CQ} (3%). (b) Assuming that the difference between i_C and i_E is neglectable, find the slopes of dc load line and ac load line (3%). (c) Determine the maximum undistorted in the output current (peak-to-peak Δi_c) (4%).

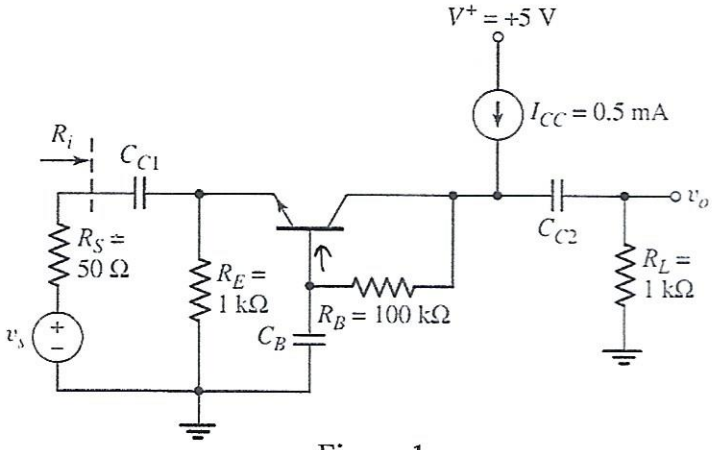

Figure 1

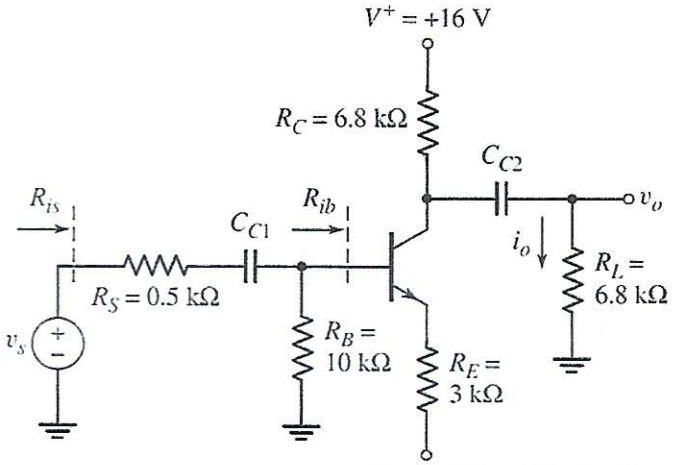

Figure 2

3. (18%) Consider the circuit shown in Figure 3 with transistor parameters $\beta = 120$ and $V_A = \infty$. (a) Determine the Q-point value for both transistors (I_{CQ1} and I_{CQ2}) (b) Determine the overall small-signal voltage gain $A_v = v_o/v_s$. (c) Determine the input resistance R_{is} and the output resistance R_O.

4. (4%) What is channel length modulation and how does it affect the current-voltage characteristic?

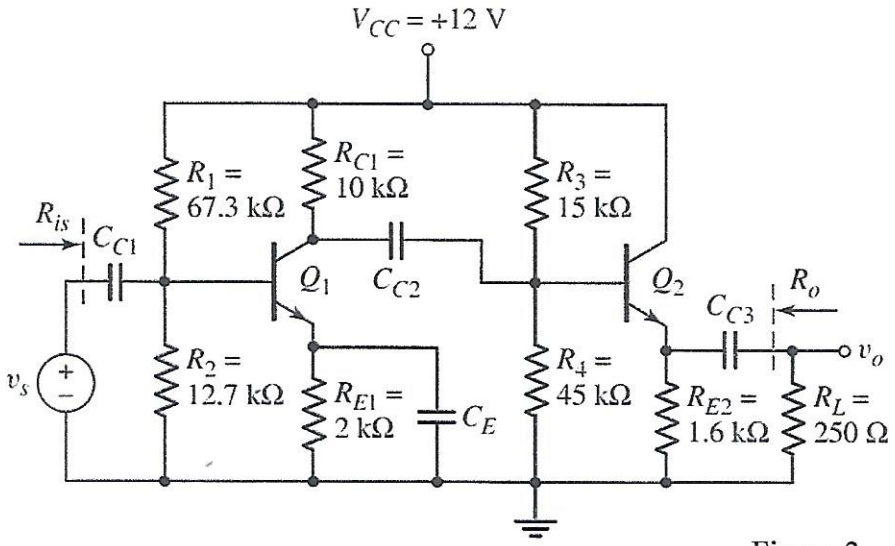

Figure 3

5. (14%) Consider the circuit shown in Figure 5. The transistor parameters are $V_{TP} = -0.3$ V, $K_p = 120\ \mu A/V^2$, and $\lambda = 0$. (a) If $R_1 = 255$ kΩ and $R_2 = 345$ kΩ, calculate V_{SG} and I_D for the circuit (6%). (b) Design R_1 and R_2 such that the MOS is exactly working at transition point and $R_1 + R_2 = 500$ kΩ (8%).

6. (12%) Consider the circuit shown in Figure 6. The transistor parameters are: $V_{TP} = 0.8$ V, $K_p = 0.5\ mA/V^2$, and $\lambda = 0$. (a) Design R_D and R_S such that $I_{DQ} = 0.8$ mA and $V_{SDQ} = 3$ V. (b) Find the small-signal voltage gain $A_v = v_o/v_i$.

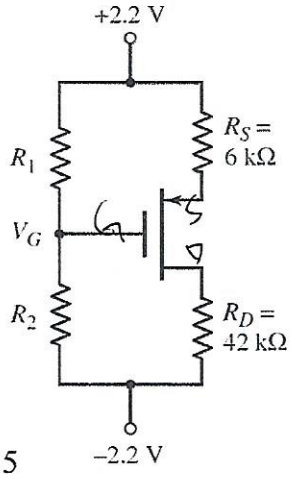

Figure 5

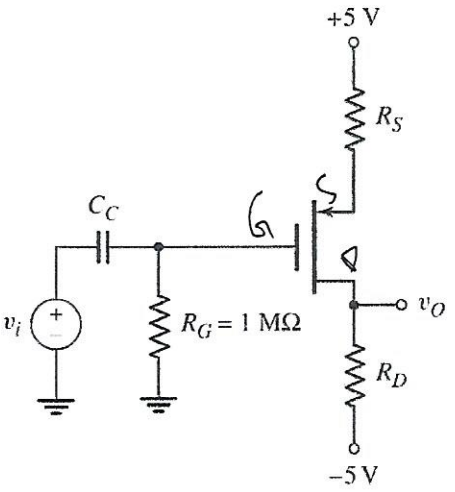

Figure 6

7. (15%) The parameters of the circuit in Figure 7 are $R_S = 2$ kΩ, $R_L = 2$ kΩ, $k_p' = 80\ \mu A/V^2$, $V_{TP} = -1.2$ V, and $\lambda = 0$. (a) Design the width-to-length ratio (W/L) such that $I_{DQ} = 1.5$ mA. (b) Find the small-signal voltage gain $A_v = v_o/v_i$. (c) Find the small-signal output resistance R_o.

8. (15%) Considering the circuit shown in Figure 8. Assume the bias current $I_{Bias} = 0.25$ mA and the bias voltage $V_{DD} = 10$ V. The transistor parameters are: $V_{TN} = 0.8$ V, $V_{TP} = -0.8$ V, $K_n = 0.8\ mA/V^2$, $K_p = 0.5\ mA/V^2$, $\lambda_n = 0.01\ V^{-1}$, and $\lambda_p = 0.02\ V^{-1}$.(a) Determine the small-signal voltage gain $A_v = v_o/v_i$. (b) Determine the output resistance of the circuit R_o. (c) If the desired voltage gain $A_v = 200$, assuming all transistor parameters remains the same, what are the required values of I_{Bias}?

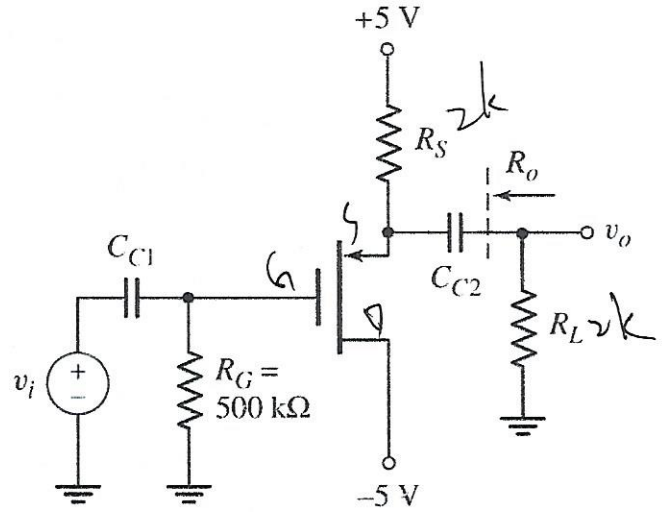

Figure 7

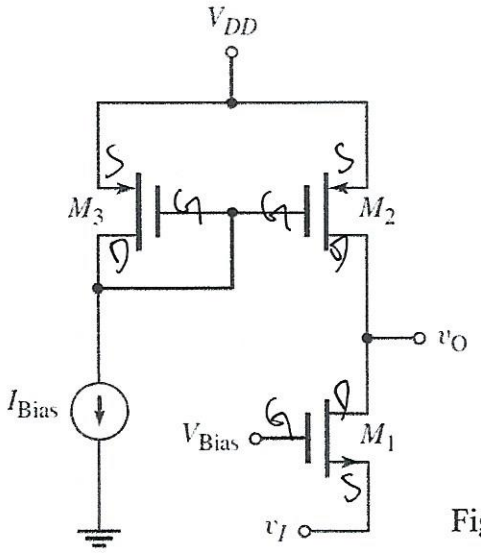

Figure 8

Have a nice winter vacation and a happy new year!