TAIWAN TECH National Taiwan University of Science and Technology

Introduction to Analog Integrated Circuit Design

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Single-Stage Amplifiers

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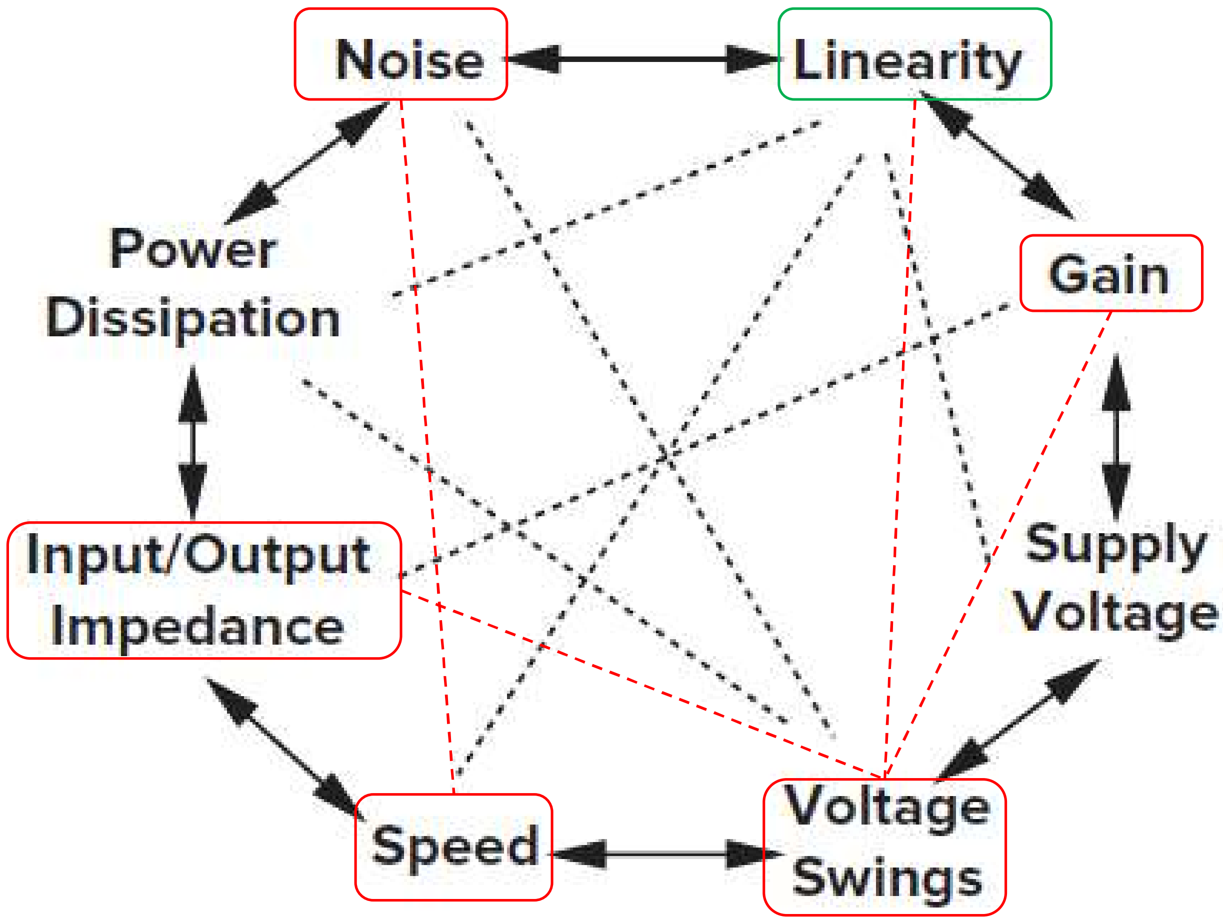
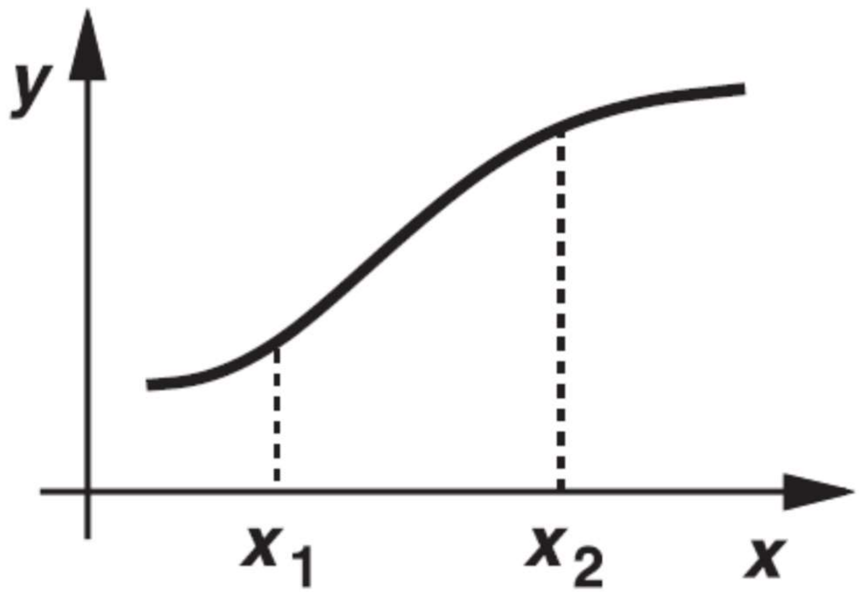
類比設計八邊形



Noise
Linearity
Gain
Supply Voltage
Voltage Swings
Speed
Input/Output Impedance
Power Dissipation

放大器之輸入－輸出特性



一個放大器之輸入－輸出特性通常為一非線性函數

$$y(t) \approx \alpha_0 + \alpha_1 x(t) + \alpha_2 x^2(t) + \cdots + \alpha_n x^n(t) \quad x_1 \le x \le x_2$$

x 的範圍夠小時 $y(t) \approx \alpha_0 + \alpha_1 x(t)$

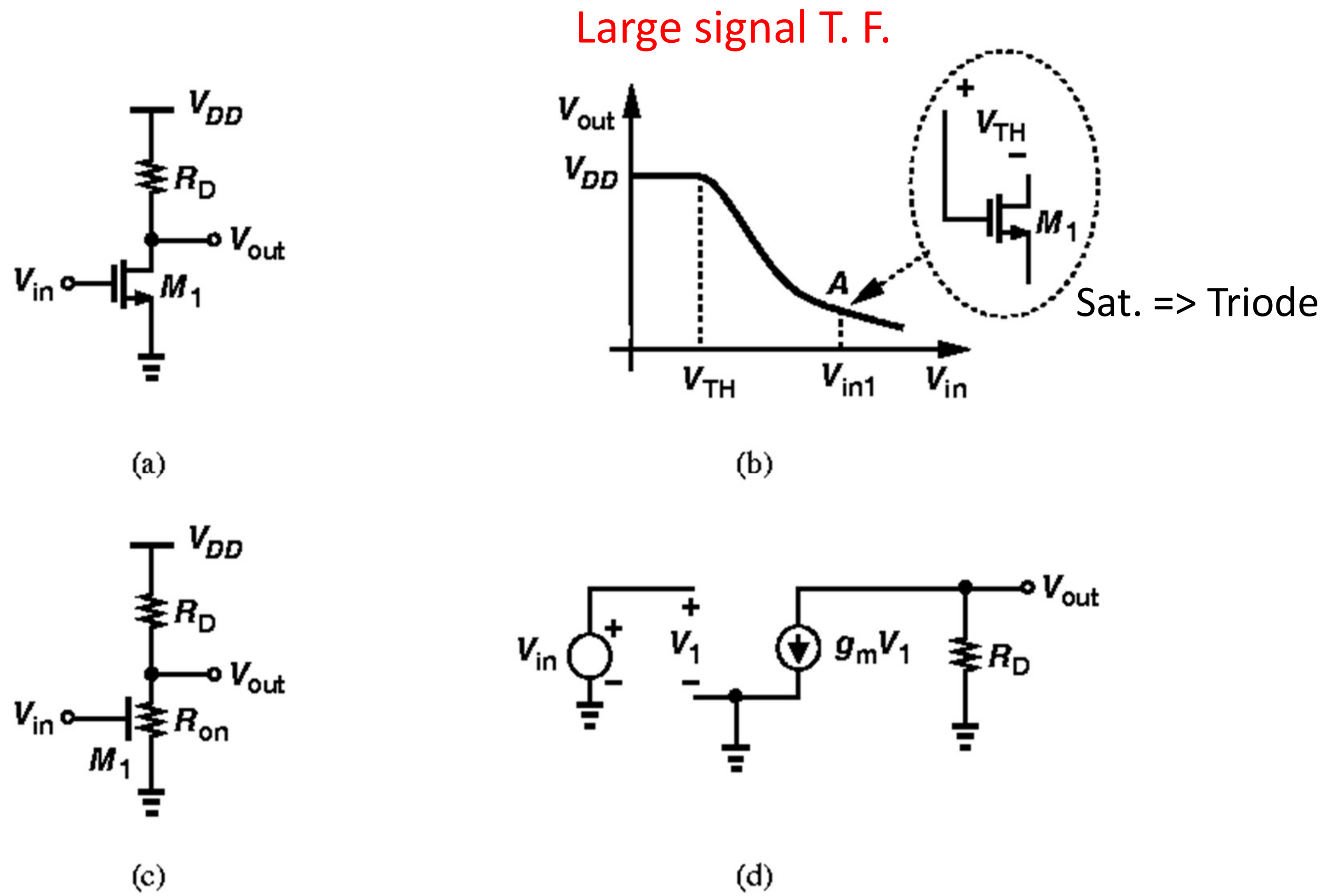
Chapter 3
Single-Stage Amplifiers

Amplifier Categories

Common-Source Stage	Source Follower	Common-Gate Stage	Cascode
With Resistive Load	With Resistive Bias	With Resistive Load	Telescopic
With Diode-Connected Load	With Current-Source Bias	With Current-Source Load	Folded
With Current-Source Load			
With Active Load			
With Source Degeneration			

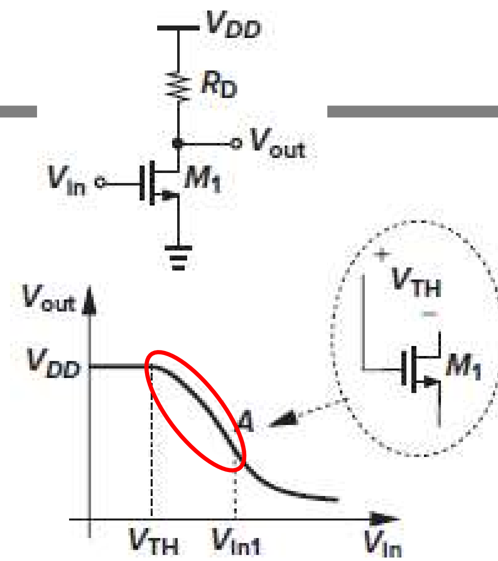
- 在看類比電路時，先思考電路的本質:
  - 這個電路的目的是甚麼?
  - 運用電子學與電路學的基礎知識
- 接著，分析這個電路 (DC Gain, Rin and Rout (Zin and Zout))
  - 至少用兩種方式交叉驗證 (在你沒自信之前!!)

負載電阻之共源極組態



(a)共源極組態；(b)輸入一輸出特性圖；
(c)深三極管區之等效電路；(d)飽和區之小信號模型。

共源極組態之特性



1. V_{in} 由零開始時，M_1 關閉， $V_{out}=V_{DD}$。

2. V_{in} 略大於 V_{TH} 時 (飽和區)，

$$V_{out}=V_{DD}-R_D\frac{1}{2}\mu_nC_{ox}\frac{W}{L}(V_{in}-V_{TH})^2$$

3. V_{in} 比 V_{out} 高 V_{TH} 以上時，如圖A點 (V_{GS} - V_{TH}= V_{DS})

$$\underline{V_{in1}}-V_{TH}=V_{DD}-R_D\frac{1}{2}\mu_nC_{ox}\frac{W}{L}(V_{in1}-V_{TH})^2$$ => V_{in1}=?

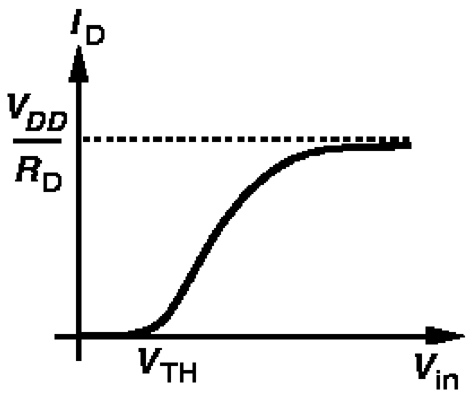
4. $V_{in}>V_{in1}$ 時，M_1 位於三極管區

$$V_{out}=V_{DD}-R_D\frac{1}{2}\mu_nC_{ox}\frac{W}{L}[2(V_{in}-V_{TH})V_{out}-V_{out}^2]$$

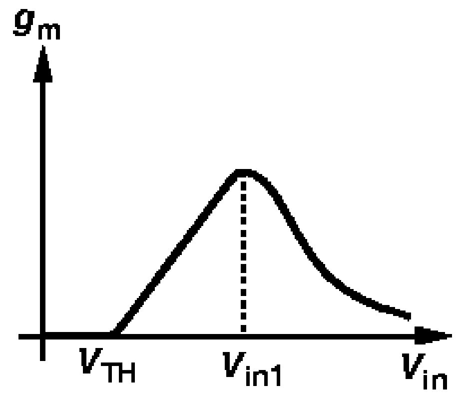
5. V_{in} 夠大足以驅動 M_1 進入深三極管區時，$V_{out}<< 2(V_{in} - V_{TH})$

$$V_{out}=V_{DD}\frac{R_{on}}{R_{on}+R_D}=\frac{V_{DD}}{1+\mu_nC_{ox}\frac{W}{L}R_D(V_{in}-V_{TH})}$$

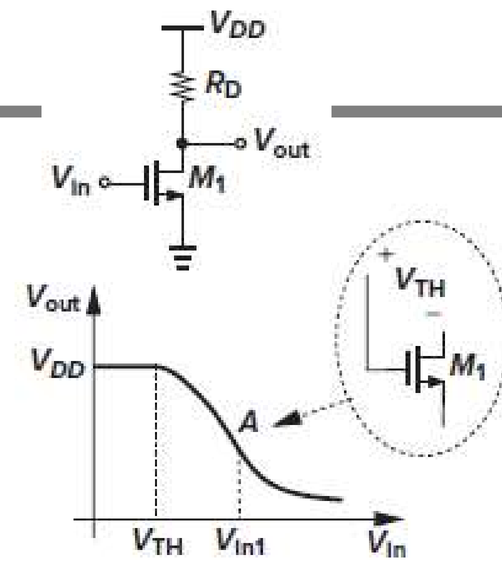
電壓增益



(a)



(b)



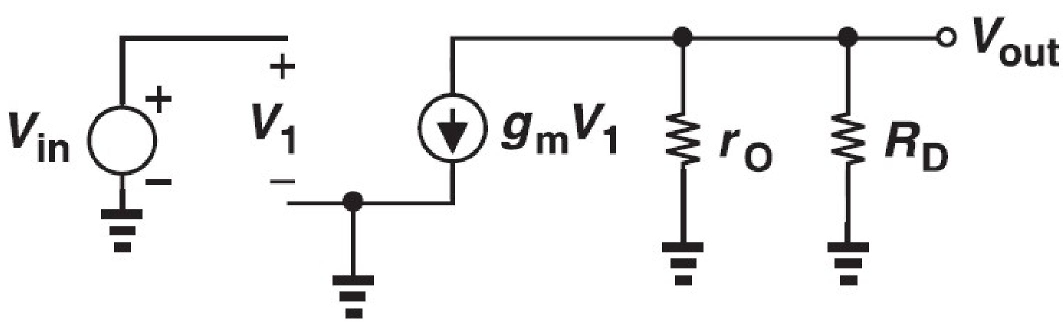
因為在三極管區中轉導會下降，通常會確保 $V_{out} > V_{in} - V_{TH}$，並視其斜率為小信號增益，可得

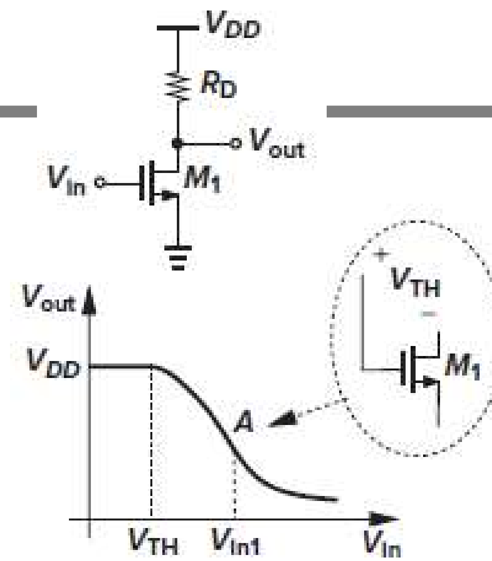
$$A_v = \frac{\partial V_{out}}{\partial V_{in}} = -R_D \mu_n C_{ox} \frac{W}{L}(V_{in} - V_{TH}) = -g_m R_D$$

$$A_v = -\sqrt{2\mu_n C_{ox} \frac{W}{L} I_D} \frac{V_{RD}}{I_D} = -\sqrt{2\mu_n C_{ox} \frac{W}{L}} \frac{V_{RD}}{\sqrt{I_D}}$$

欲將共源極之電壓增益最大化，如果其它參數保持固定，可藉由增加 W/L 或 V_{RD}，或是減少 I_D 來增加 A_v 之大小。

小信號模型





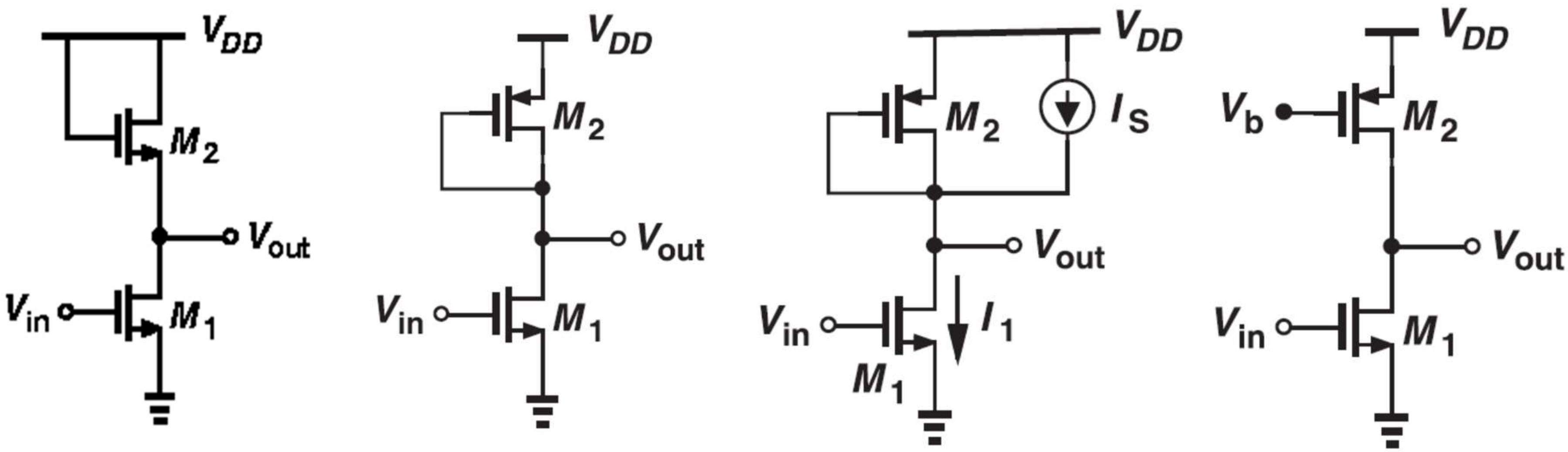
$$V_{out} = V_{DD} - R_D \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{in} - V_{TH})^2 (1 + \lambda V_{out})$$

$$\frac{\partial V_{out}}{\partial V_{in}} = -R_D \mu_n C_{ox} \frac{W}{L}(V_{in} - V_{TH})(1 + \lambda V_{out})$$

$$- R_D \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{in} - V_{TH})^2 \lambda \frac{\partial V_{out}}{\partial V_{in}}$$

$$A_v \approx -R_D g_m - R_D I_D \lambda A_v = -\frac{g_m R_D}{1 + R_D \lambda I_D} = -g_m \frac{r_O R_D}{r_O + R_D} = \underline{-g_m (r_O // R_D)}$$

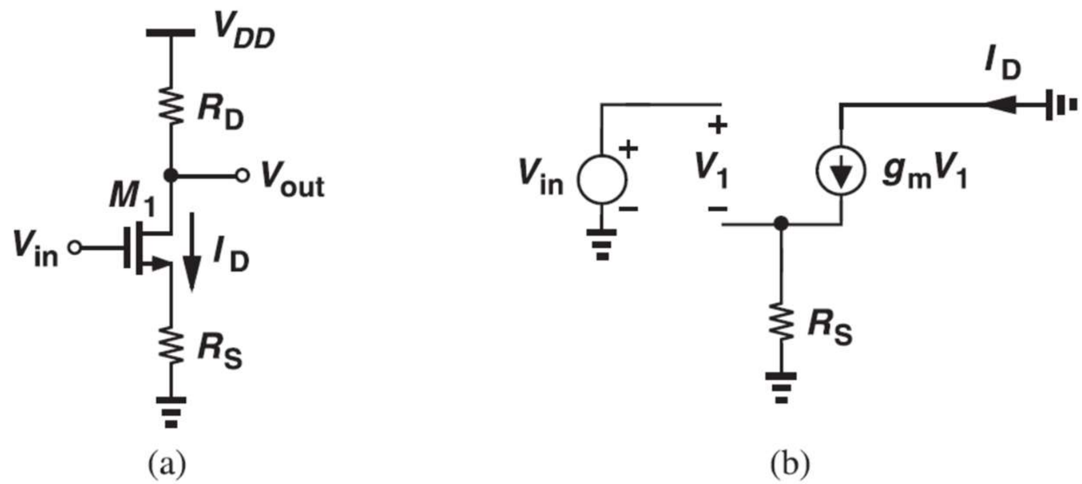
四種共源級放大器



- Homework (HW2.1)
  - Find DC voltage gain and output resistance of each amplifier

源極退化共源極組態之小信號增益

Ignore body effect



$V_{GS} = V_{in} - I_D R_S$

$V_{out} = V_{DD} - I_D R_D$，$\partial V_{out} / \partial V_{in} = -(\partial I_D / \partial V_{in}) R_D$，假設 $I_D = f(V_{GS}) = g_m V_{GS}$

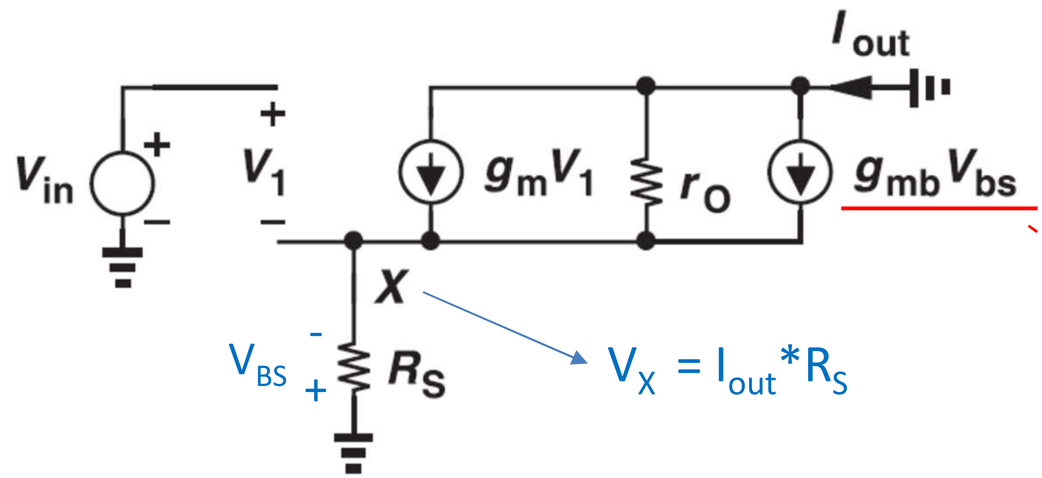
$$G_m = \frac{\partial I_D}{\partial V_{in}} = \frac{\partial f}{\partial V_{GS}} \frac{\partial V_{GS}}{\partial V_{in}} = \left(1 - R_S \frac{\partial I_D}{\partial V_{in}}\right) \frac{\partial f}{\partial V_{GS}}$$

$\partial f / \partial V_{GS}$ 為 M_1 之轉導 g_m，則 $G_m = \dfrac{g_m}{1 + g_m R_S}$

因此，小信號增益等於 $A_v = -G_m R_D = \dfrac{-g_m R_D}{1 + g_m R_S}$ $\left(= -\dfrac{g_m}{1 + g_m R_S} R_D\right)$

源極退化共源極組態之小信號模型

Considering body effect



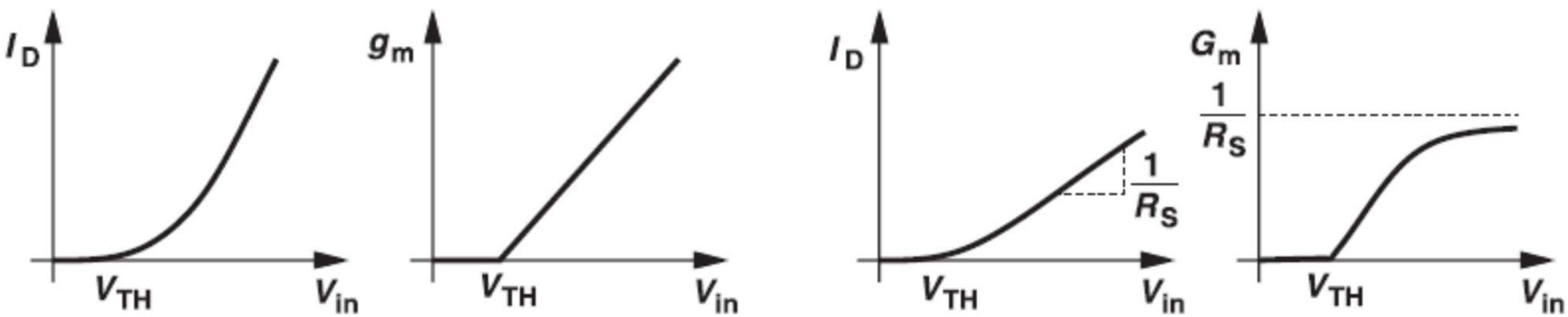
$$I_{out} = g_m V_1 - g_{mb} V_X - \frac{I_{out} R_S}{r_O}$$

$$= g_m (V_{in} - I_{out} R_S) + g_{mb}(-I_{out} R_S) - \frac{I_{out} R_S}{r_O}$$

$$G_m = \frac{I_{out}}{V_{in}} = \frac{g_m r_O}{R_S + [1 + (g_m + g_{mb}) R_S] r_O} \approx \frac{g_m}{1 + (g_m + g_{mb}) R_S}$$

共源極元件之汲極電流和轉導值

g_m is not constant　　　　G_m is constant if large Vin



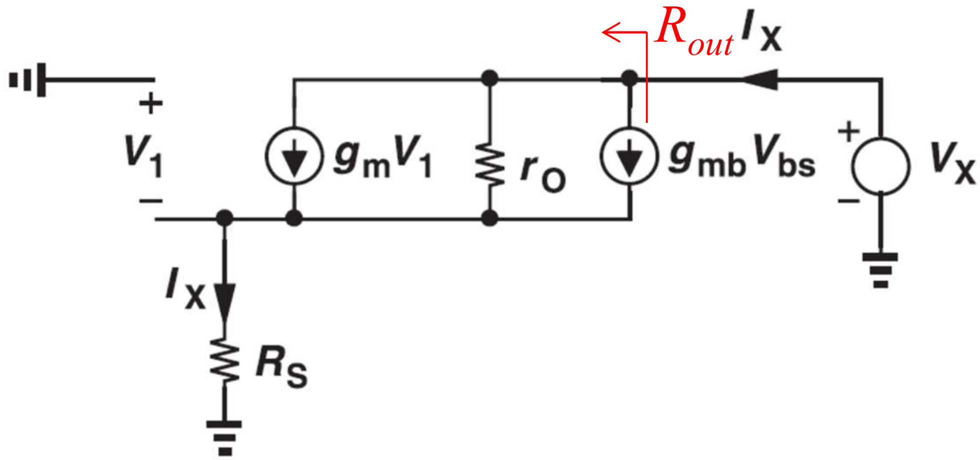
(a)源極無退化現象時；　　　　(b)源極有退化現象時。

$$i_D = \beta(V_{in} - V_{TH})^2$$

$$g_m = \frac{\partial i_D}{\partial V_{GS}} = 2\beta(V_{in} - V_{TH})$$

$$G_m = \frac{g_m}{1 + g_m R_S}$$

源極退化共源極組態之輸出電阻



流經 R_s 之電流為 I_X，$V_1= -I_X R_s$

流經 r_O 之電流為 $I_X-(g_m+g_{mb})V_1=I_X+(g_m+g_{mb})R_s I_X$

$$r_O[I_X+(g_m+g_{mb})R_S I_X]+I_X R_S=V_X$$

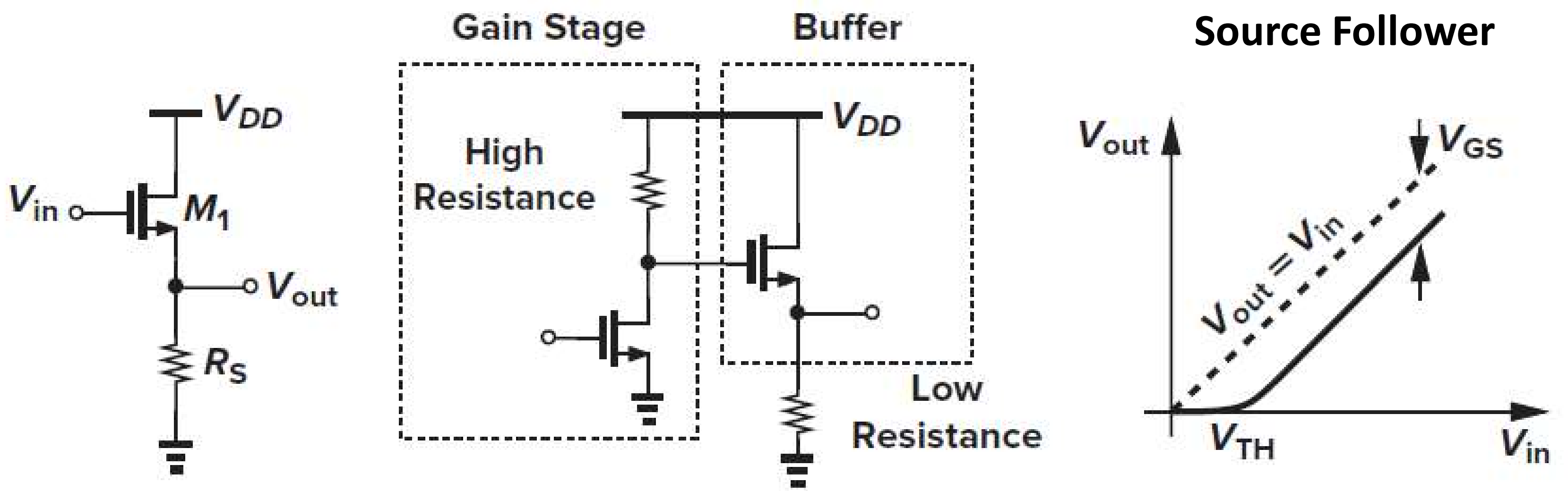
$$R_{out}=[1+(g_m+g_{mb})R_S]r_O+R_S$$

$$=[1+(g_m+g_{mb})r_O]R_S+r_O$$

$$\approx (g_m+g_{mb})r_O R_S+r_O$$

$$=[1+(g_m+g_{mb})R_S]r_O$$

源極隨耦器 (Source Follower)

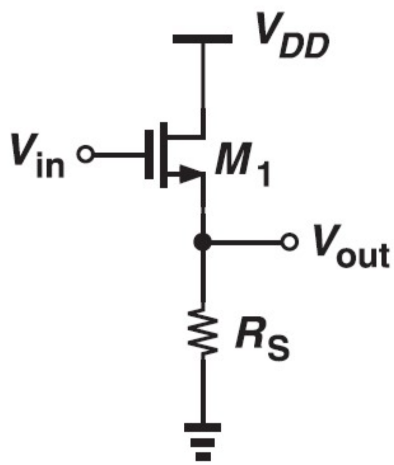


(a) (b) (c)

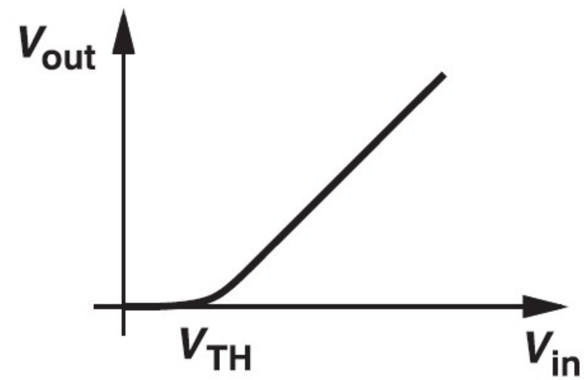
Gain=? How to improve?

Actually, using R_S at the output node V_{out} is not a good idea. Do you know why?

源極隨耦器 (Source Follower)



(a)



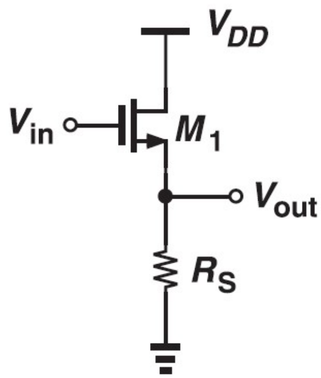
(b)

$V_{in} < V_{TH}$，M_1 關閉且 $V_{out} = 0$。

$V_{in} > V_{TH}$ 時，$\frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{in} - V_{TH} - V_{out})^2 R_S = V_{out}$

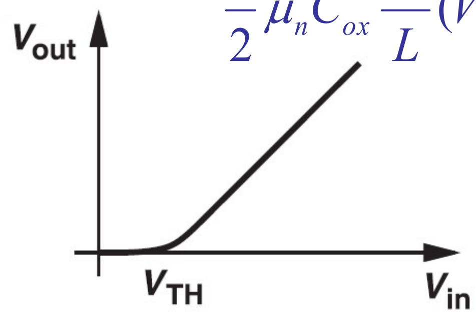
$V_{out} = f(V_{in})$, a nonlinear function

源極隨耦器之增益



(a)

$$\frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{in}-V_{TH}-V_{out})^2 R_S = V_{out}$$



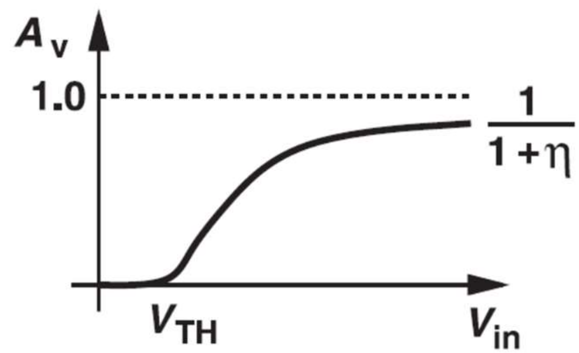
(b)

對 V_{in} 微分 $$\underbrace{\frac{1}{2}\mu_n C_{ox}\frac{W}{L}2(V_{in}-V_{TH}-V_{out})}_{g_m}\left(1-\frac{\partial V_{TH}}{\partial V_{in}}-\frac{\partial V_{out}}{\partial V_{in}}\right)R_S = \frac{\partial V_{out}}{\partial V_{in}}$$

因為 $\partial V_{TH}/\partial V_{in} = \eta\,\partial V_{out}/\partial V_{in}$

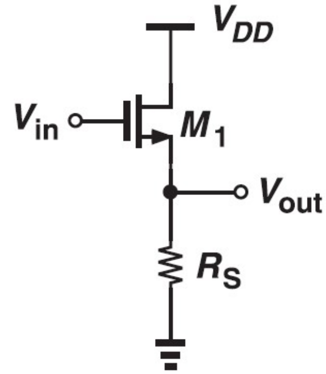
$$\frac{\partial V_{out}}{\partial V_{in}} = \frac{\mu_n C_{ox}\frac{W}{L}(V_{in}-V_{TH}-V_{out})R_S}{1+\mu_n C_{ox}\frac{W}{L}(V_{in}-V_{TH}-V_{out})R_S\underline{(1+\eta)}}$$

$$g_m = \mu_n C_{ox}\frac{W}{L}(V_{in}-V_{TH}-V_{out})$$

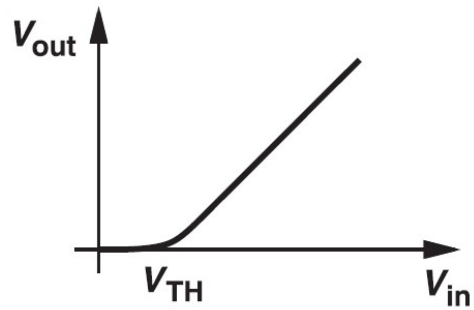


$$A_v = \frac{g_m R_S}{1+g_m(1+\eta)R_S}$$

Supplement



(a)



(b)

How to get $\partial V_{TH} / \partial V_{in} = \eta \partial V_{out} / \partial V_{in}$

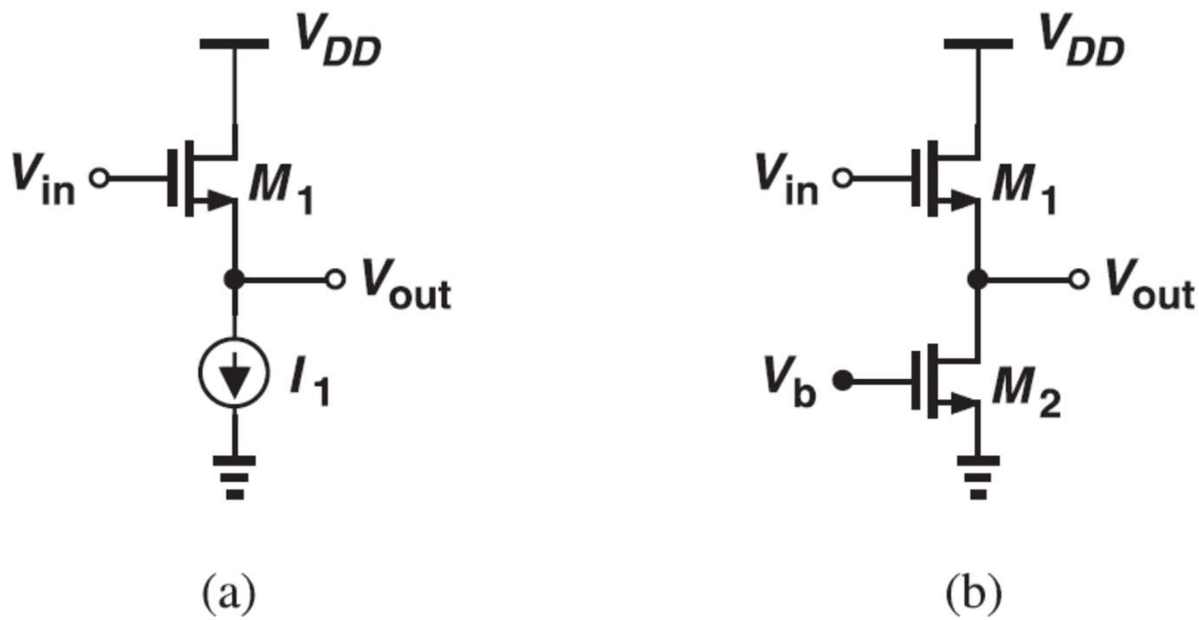
$$V_{TH} = V_{TH0} + \gamma \left(\sqrt{2\Phi_F + V_{SB}} - \sqrt{|2\Phi_F|} \right)$$

Since $V_{SB} = V_{out}$

$$\frac{\partial V_{TH}}{\partial V_{in}} = \frac{\gamma}{2}(2\emptyset_F + V_{out})^{-1/2} \cdot \frac{\partial V_{out}}{\partial V_{in}} = \eta \cdot \frac{\partial V_{out}}{\partial V_{in}}$$

where $\eta = \frac{\gamma}{2}(2\emptyset_F + V_{out})^{-1/2}$

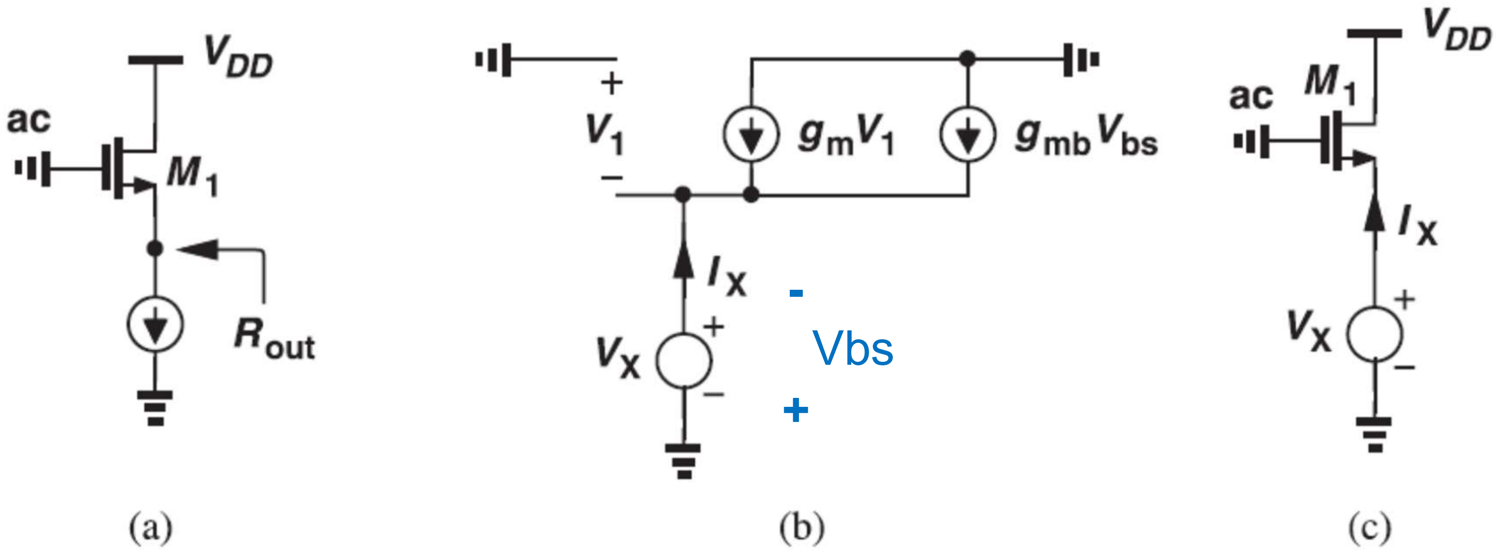
電流源取代電阻之源極隨耦器



使用NMOS電晶體作為電流源之源極隨耦器。

Q: Why is it a better design? ANS: Current is constant!!

源極隨耦器之輸出阻抗



$$R_{out} = \frac{1}{g_m} \| \frac{1}{g_{mb}}$$

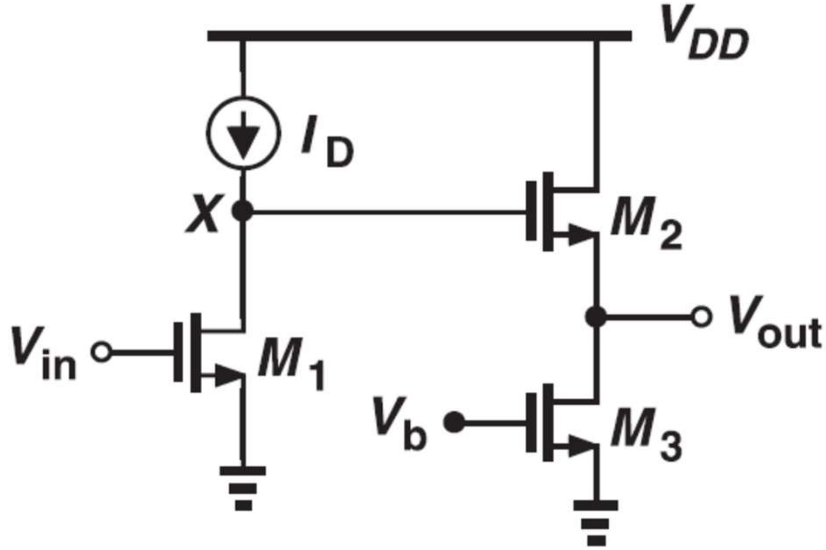
$$= \frac{1}{g_m + g_{mb}}$$

If considering r_o? → $R'_{out} = R_{out} || r_o$

How about a fast watching!!

共源極組態和源極隨耦器之疊加組態

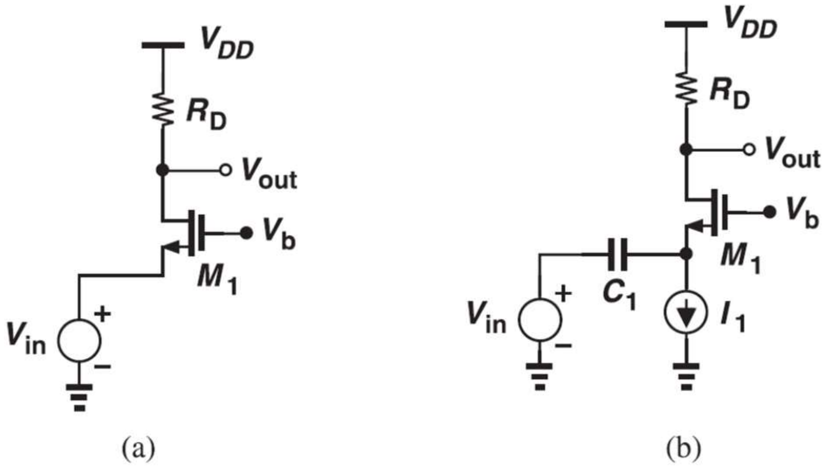
疊加 (cascade)

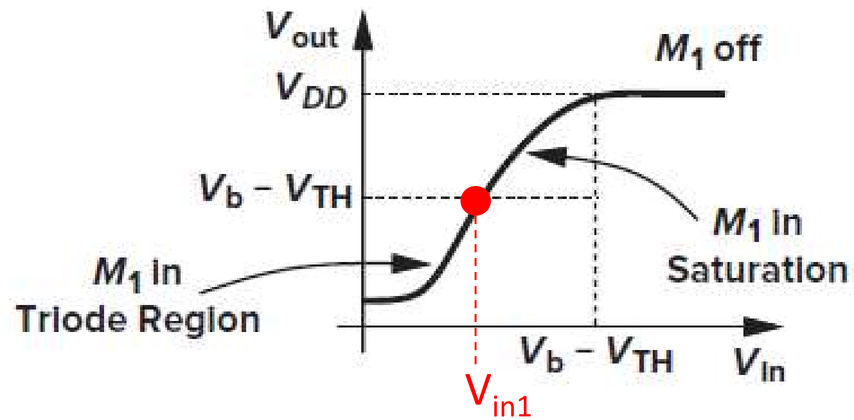


Gain stage　Output stage

- 無源極隨耦器時，V_X之最小允許值為 $V_{GS1} - V_{TH1}$
- 考慮源極隨耦器時，V_X必須大於 $V_{GS2} + V_{\text{out,max}}$

共閘極組態之輸出－輸入特性





For (a), $V_{DD} - \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_b - V_{in} - V_{TH})^2 R_D = V_b - V_{TH}$ ➡ If $V_{in} > V_{in1}$

$$\boxed{V_{out} = V_{DD} - \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_b - V_{in} - V_{TH})^2 R_D}$$

$$\frac{\partial V_{out}}{\partial V_{in}} = -\mu_n C_{ox}\frac{W}{L}(V_b - V_{in} - V_{TH})\left(-1 - \frac{\partial V_{TH}}{\partial V_{in}}\right)R_D$$

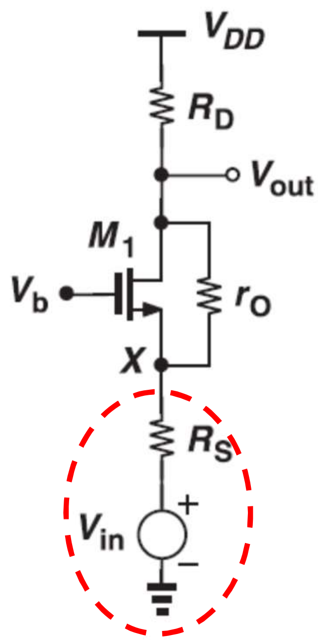
$\partial V_{TH}/\partial V_{in} = \partial V_{TH}/\partial V_{SB} = \eta$

$$\frac{\partial V_{out}}{\partial V_{in}} = \mu_n C_{ox}\frac{W}{L}R_D(V_b - V_{in} - V_{TH})(1+\eta)$$

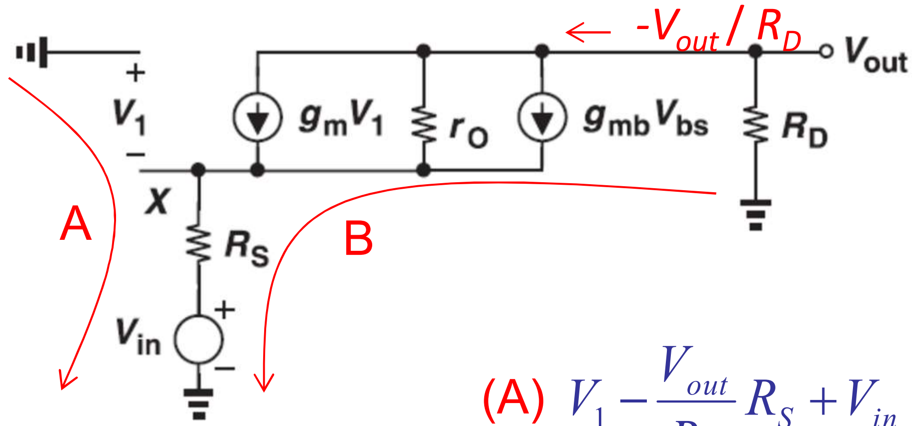
$$= \underline{g_m(1+\eta)R_D}$$

CG is a positive gain amp. But, in general, it is used as a current buffer

共閘極組態之電壓增益(小訊號分析)



(a)



(b)

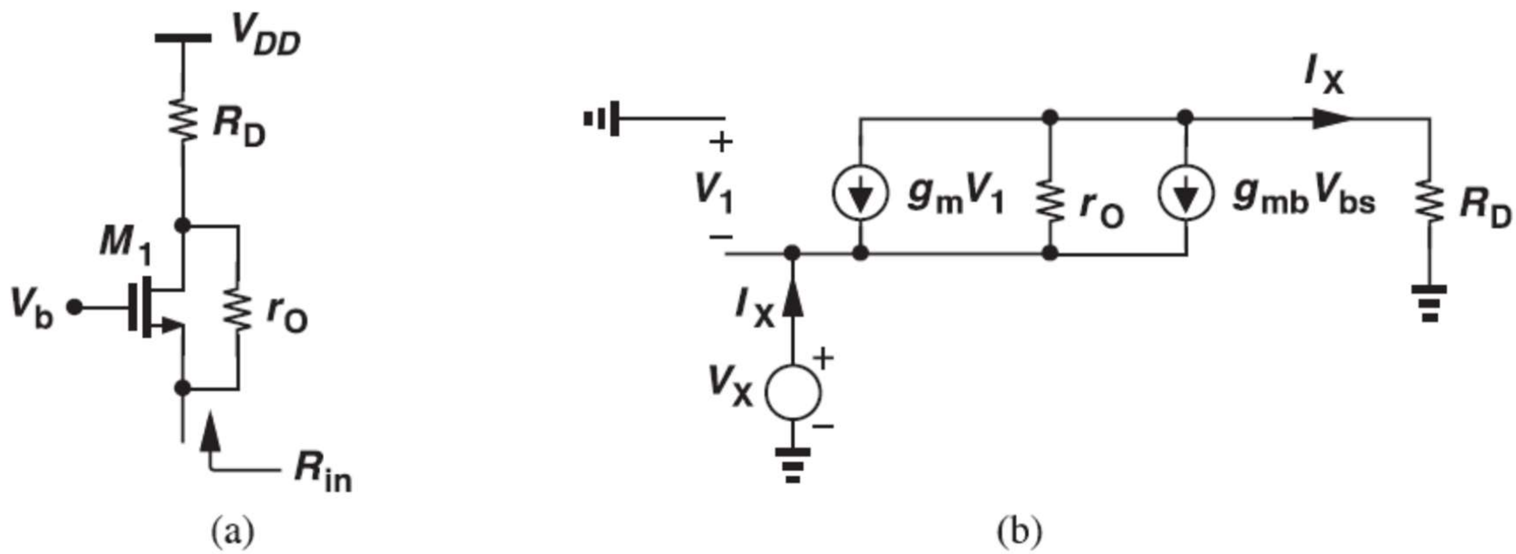
(A) $V_1 - \dfrac{V_{out}}{R_D} R_S + V_{in} = 0$

(B) $r_O\left(\dfrac{-V_{out}}{R_D} - g_m V_1 - g_{mb} V_1\right) - \dfrac{V_{out}}{R_D} R_S + V_{in} = V_{out}$

$$r_O\left[\frac{-V_{out}}{R_D} - (g_m + g_{mb})\left(V_{out}\frac{R_S}{R_D} - V_{in}\right)\right] - \frac{V_{out}}{R_D} R_S + V_{in} = V_{out}$$

$$\frac{V_{out}}{V_{in}} = \frac{(g_m + g_{mb})r_O + 1}{r_O + (g_m + g_{mb})r_O R_S + R_S + R_D} R_D \approx \underline{\frac{(g_m + g_{mb})R_D}{1 + (g_m + g_{mb})R_S}}$$

共閘極組態之輸入阻抗

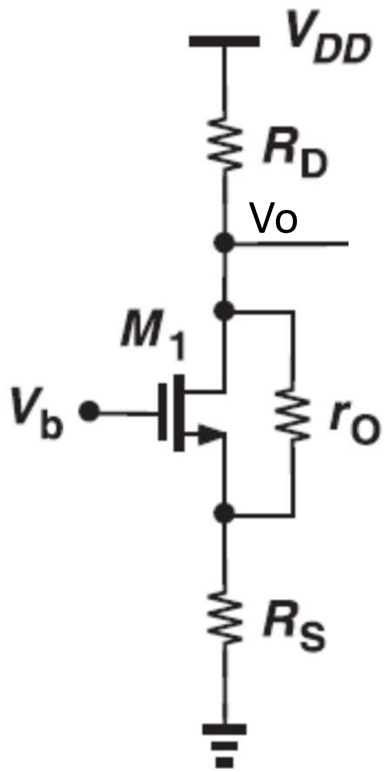


$$R_D I_X + r_O[I_X - (g_m + g_{mb})V_X] = V_X$$

$$\frac{V_X}{I_X} = \frac{R_D + r_O}{1 + (g_m + g_{mb})r_O} \approx \underline{\frac{R_D}{(g_m + g_{mb})r_O} + \frac{1}{g_m + g_{mb}}}$$

$R_D = 0$ 時，
$$\frac{V_X}{I_X} = \frac{r_O}{1 + (g_m + g_{mb})r_O} = \frac{1}{\frac{1}{r_O} + g_m + g_{mb}} = \underline{r_O \,//\, \frac{1}{g_m + g_{mb}}}$$

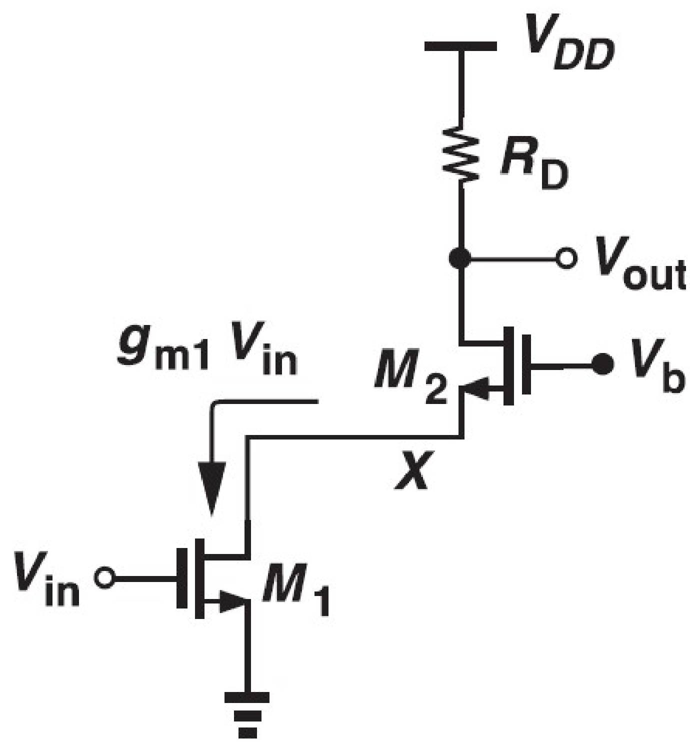
共閘極組態之輸出阻抗



$$R_{out} = \{[1+(g_m+g_{mb})r_O]R_S + r_O\} \,//\, R_D$$
$$\approx (g_m+g_{mb})r_O R_S \,//\, R_D$$

HW2.2

Cascode Circuits

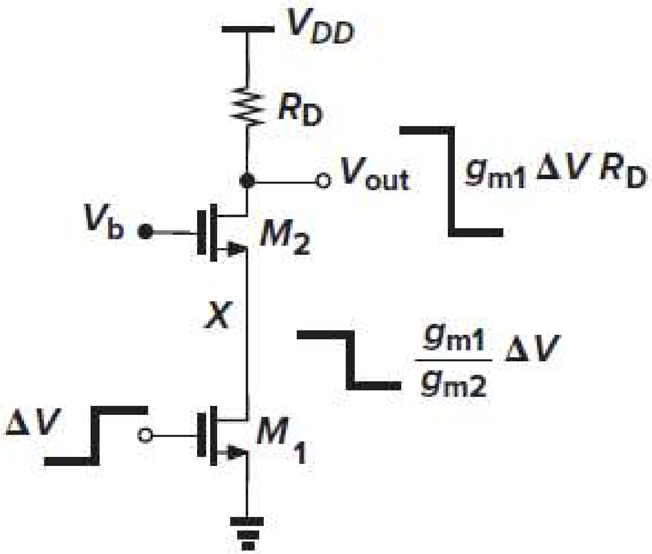


將一共源極組態和一共閘極組態疊加即為一疊接組態**(cascode)**

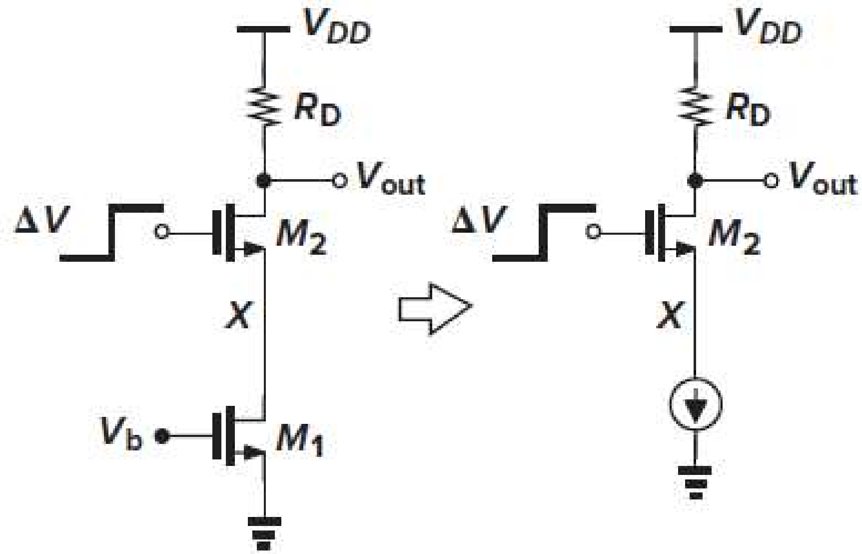
Common-source + Common-gate => Cascode

Q: Why do we use this configuration?

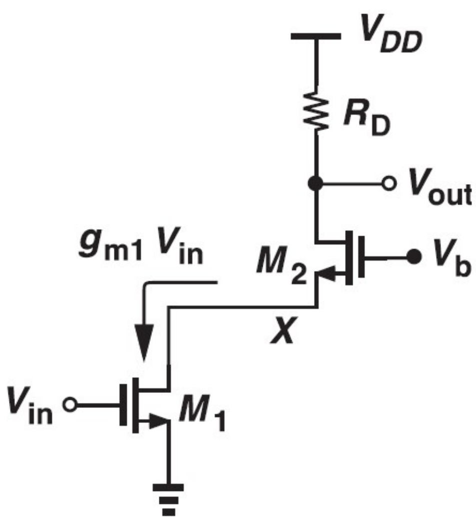
Cascode Circuits



(a)



(b)



What do you get from this?

=> Vout is constant, Av=0

HW2.3:

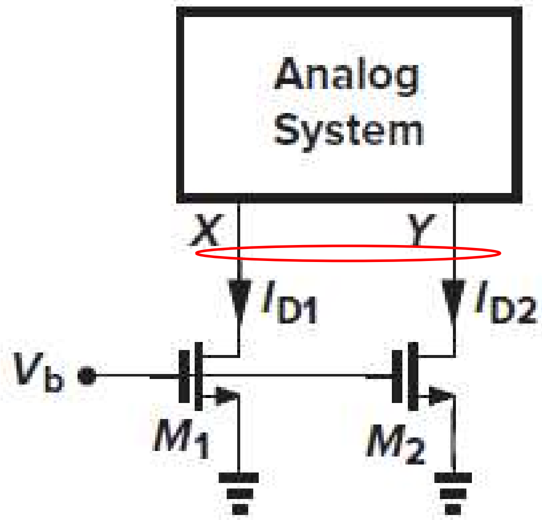
Q1: The range of Vin = ?

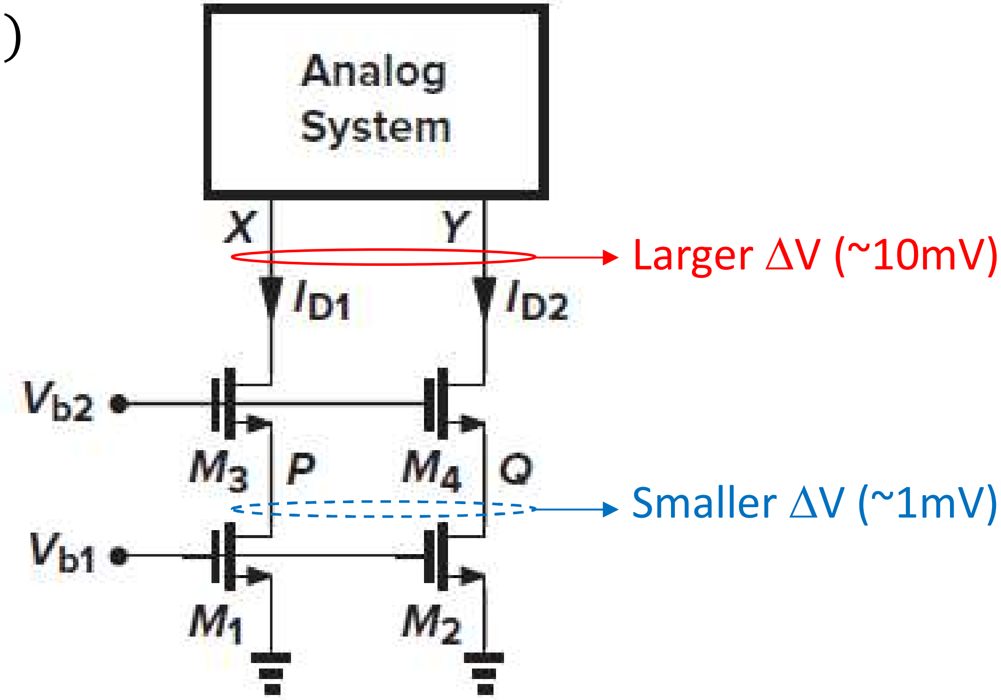
Q2: What is the relationship between Vin and Vout?

Shielding Property

Using the current formula of MOSFET,

$$I_D = \beta(V_{GS} - V_{TH})^2(1 + \lambda V_{DS})$$

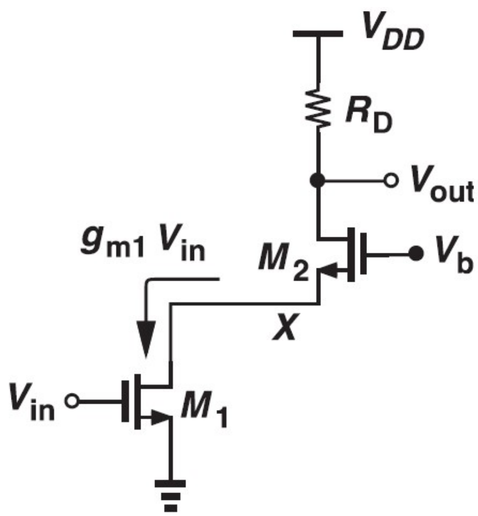




Cascode Current Source

How does the shielding work? => Please see **Example 3.24** in the textbook

摺疊疊接組態

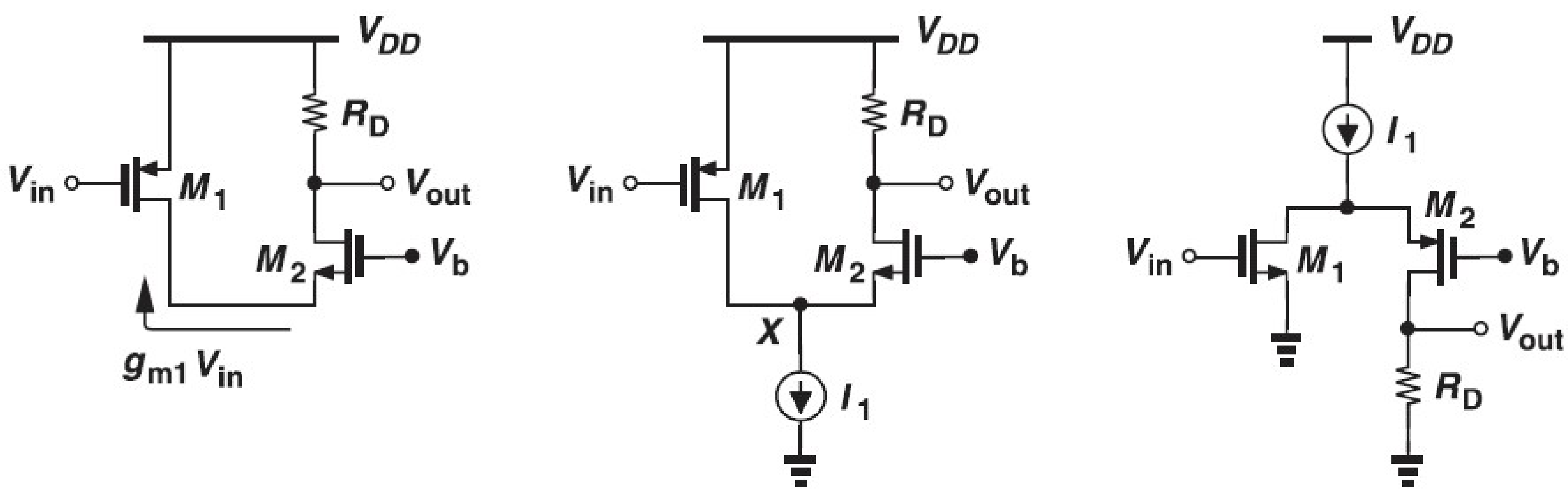


From Cascode to Folded-Cascode

(a)簡單摺疊疊接組態 (it is not real)

(b)適當偏壓之疊接組態 (using I_1)

(c)負載為NMOS輸入之疊接組態



(a) (b) (c)

Examples to Calculate Rout

Please answer the question to find Rout (HW 2.4)