TAIWAN TECH NATIONAL TAIWAN UNIVERSITY OF SCIENCE AND TECHNOLOGY

Lab1 MOSFET

Department of Electronic and Computer Engineering
National Taiwan University of Science of Science and Technology
MSIC Lab

Professor : 鍾勇輝

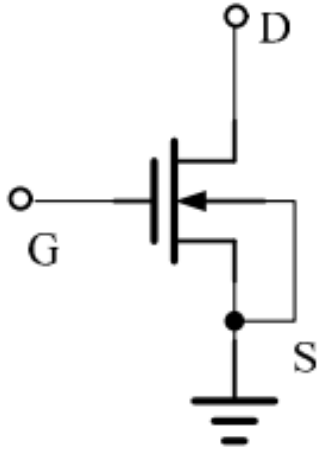
TA : 郭駿浩、郭哲原

2024/03/06

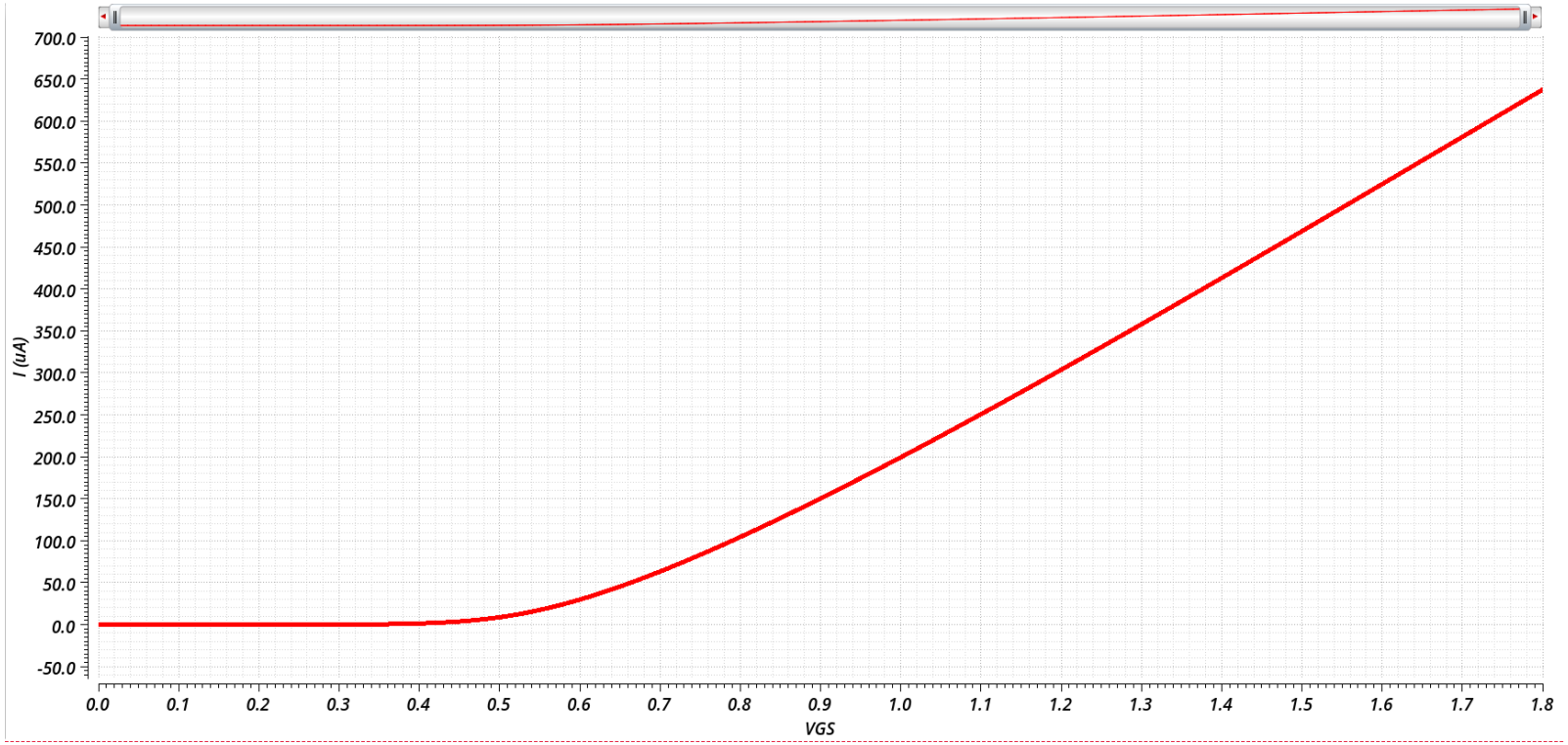
Analog Integrated Circuit Design and Applications

MOSFET I-V Curve

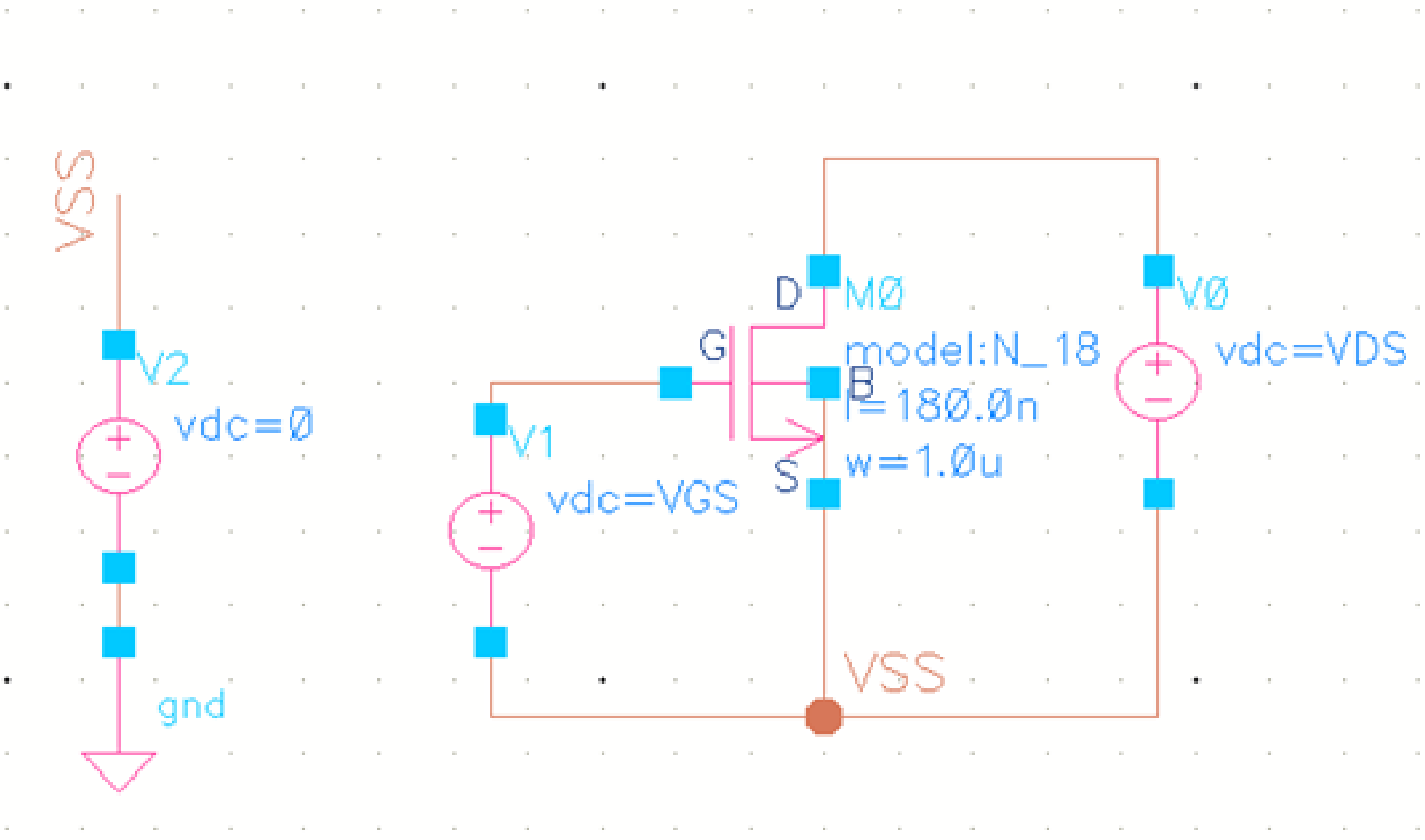
- Lab1_1：利用Virtuoso了解MOSFET的特性。
- 實驗步驟：試著利用Virtuoso將圖一的電路描述出來，讓Length = 0.18um，Width = 1um，V_{DS} = 1.8 V。試著將V_{GS}從0 V到1.8 V每次增加0.01 V，觀察I_{DS}。即為模擬$I_{DS} - V_{GS}$ Characteristic Curve。



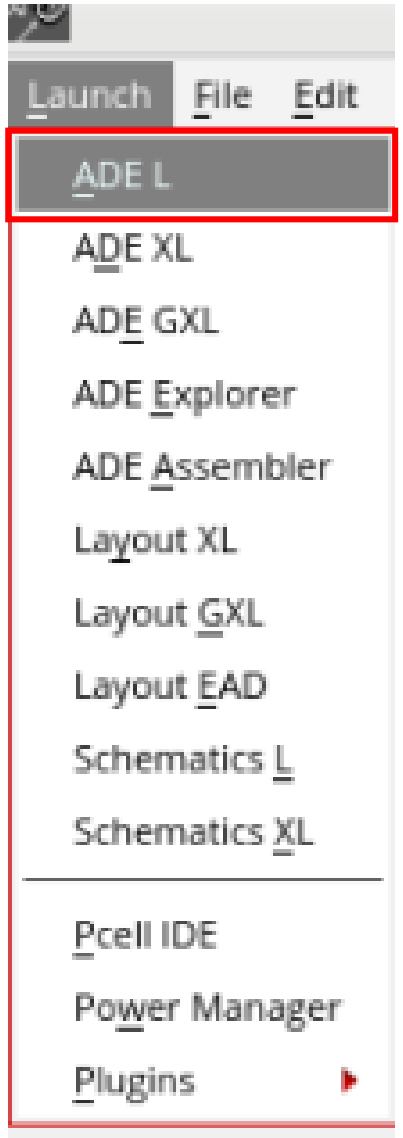
$$\frac{W}{L} = \frac{1um}{0.18um}$$

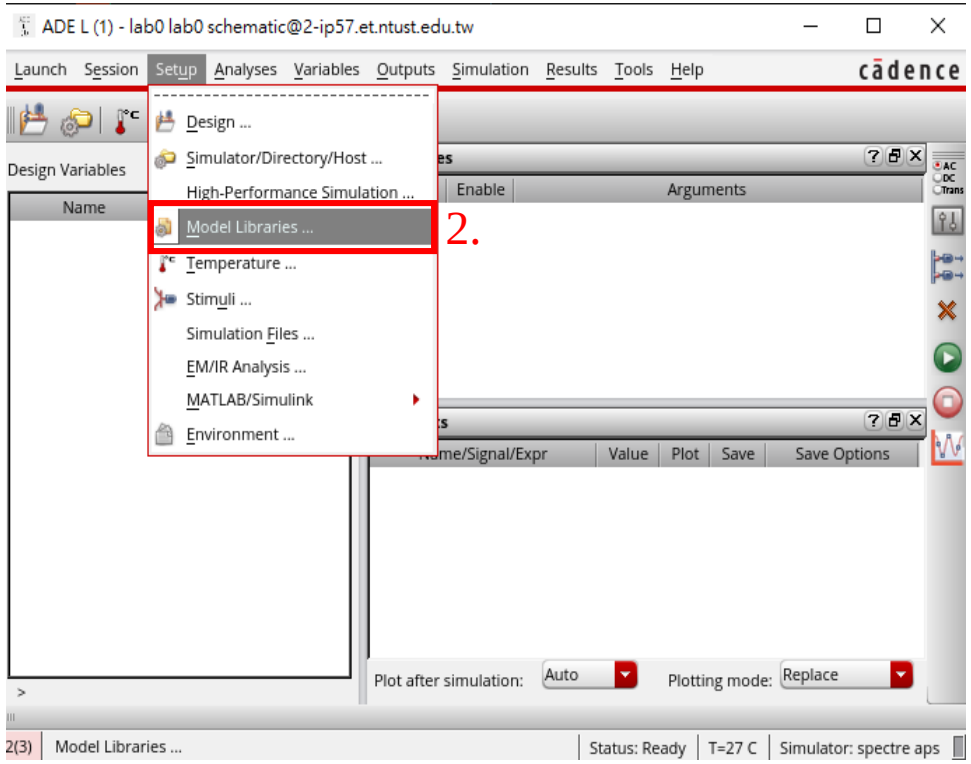


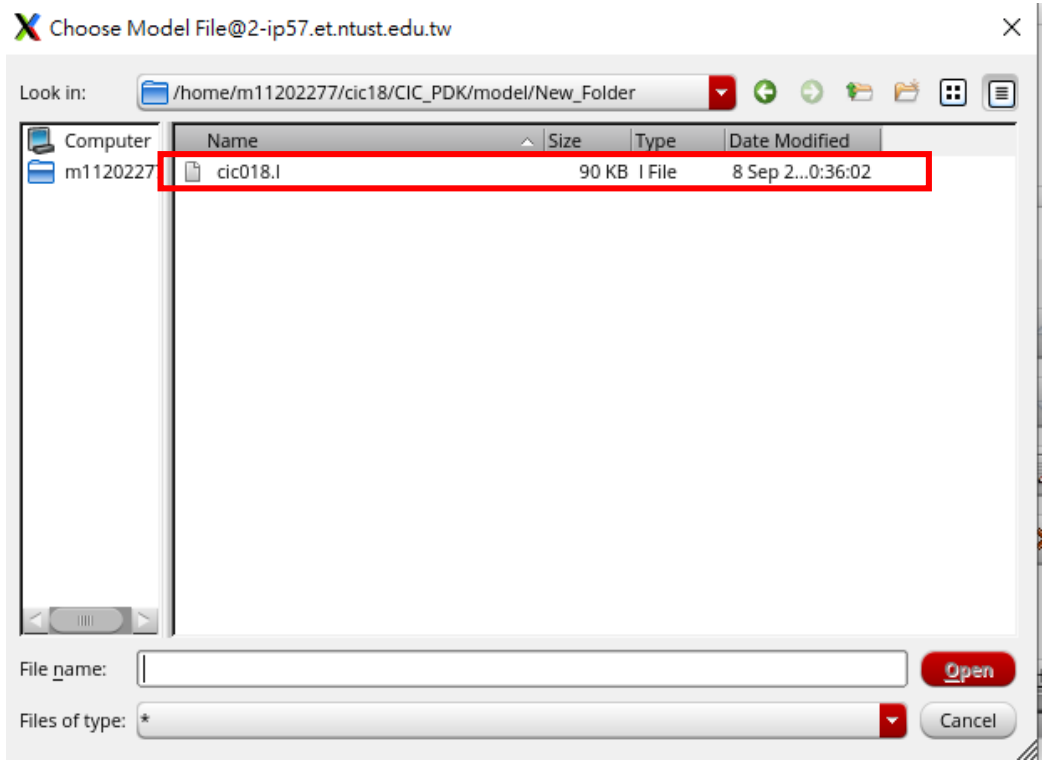
MOSFET I-V Curve



MOSFET I-V Curve

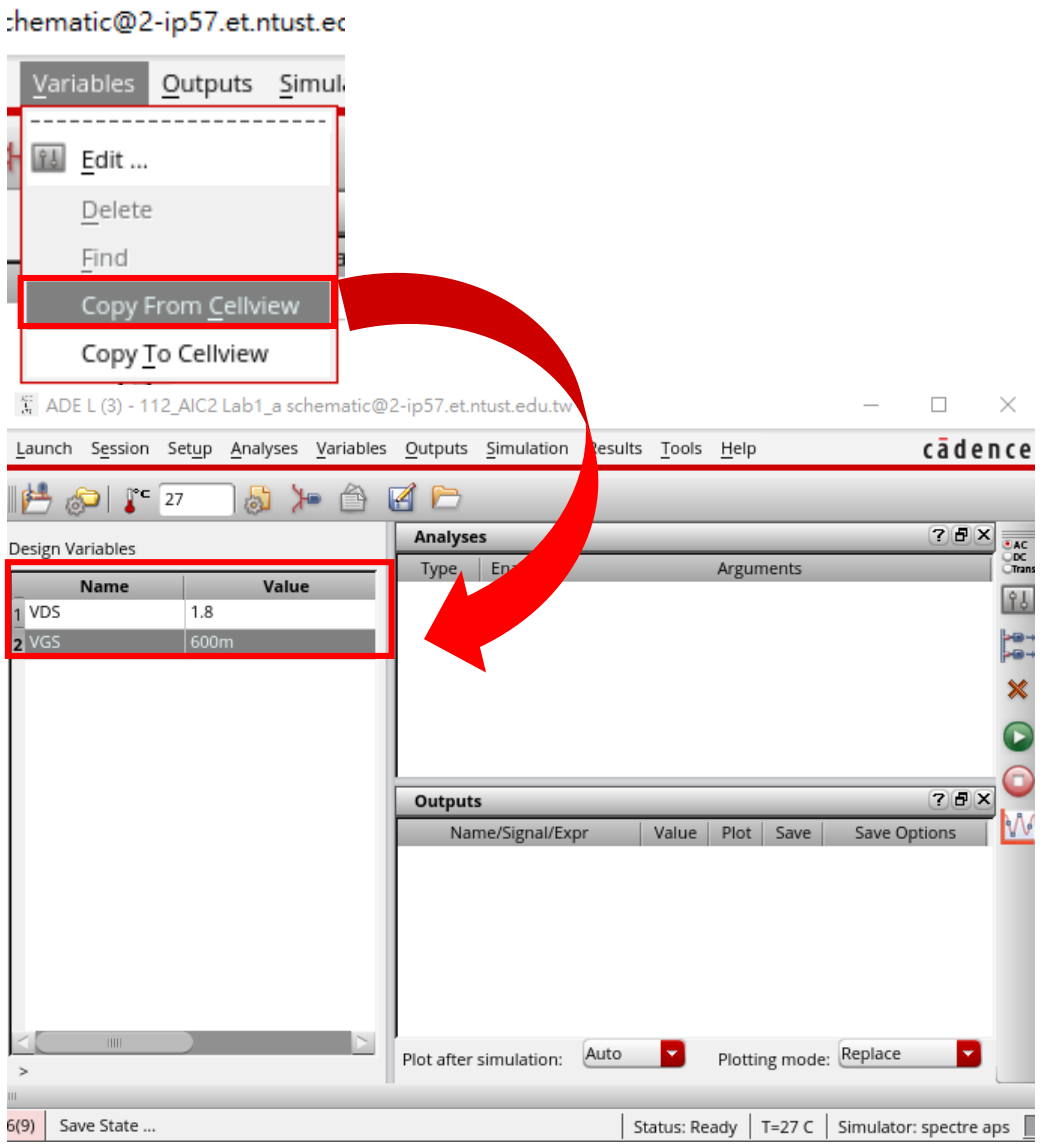


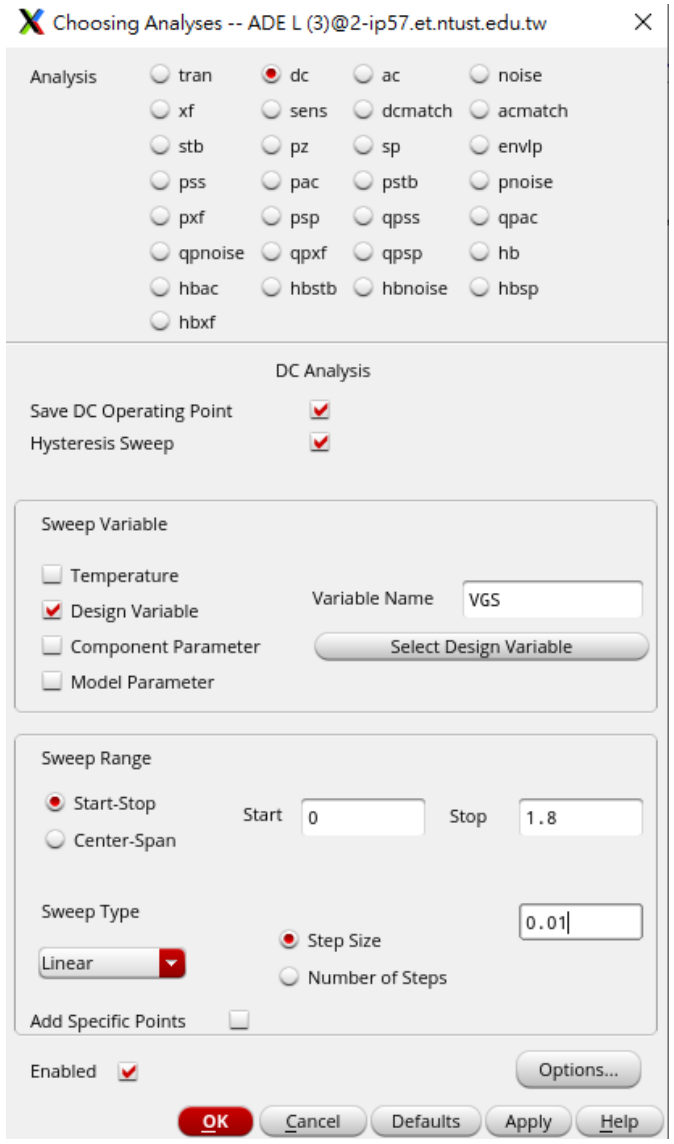




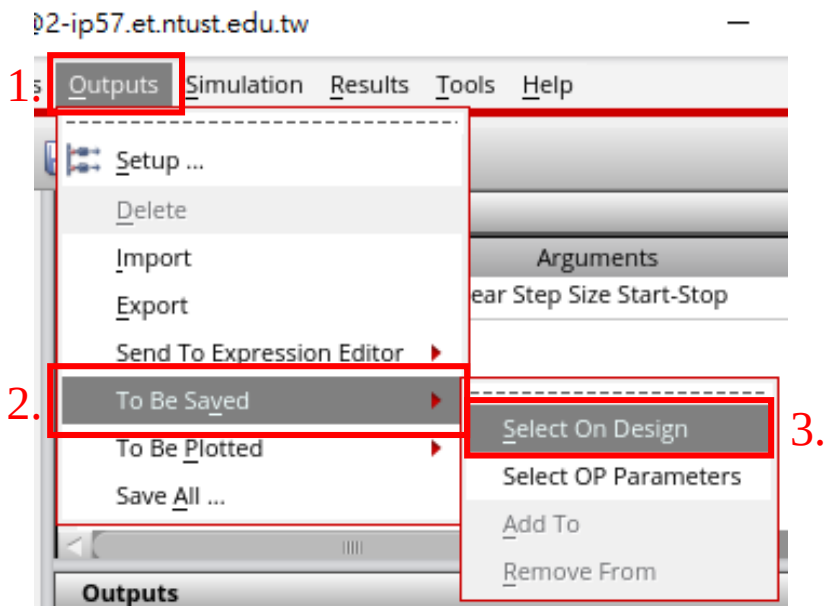
3.選擇cic018.l這個檔案
（路徑：/home/學號/cic18/CIC_PDK/model/New_Folder）

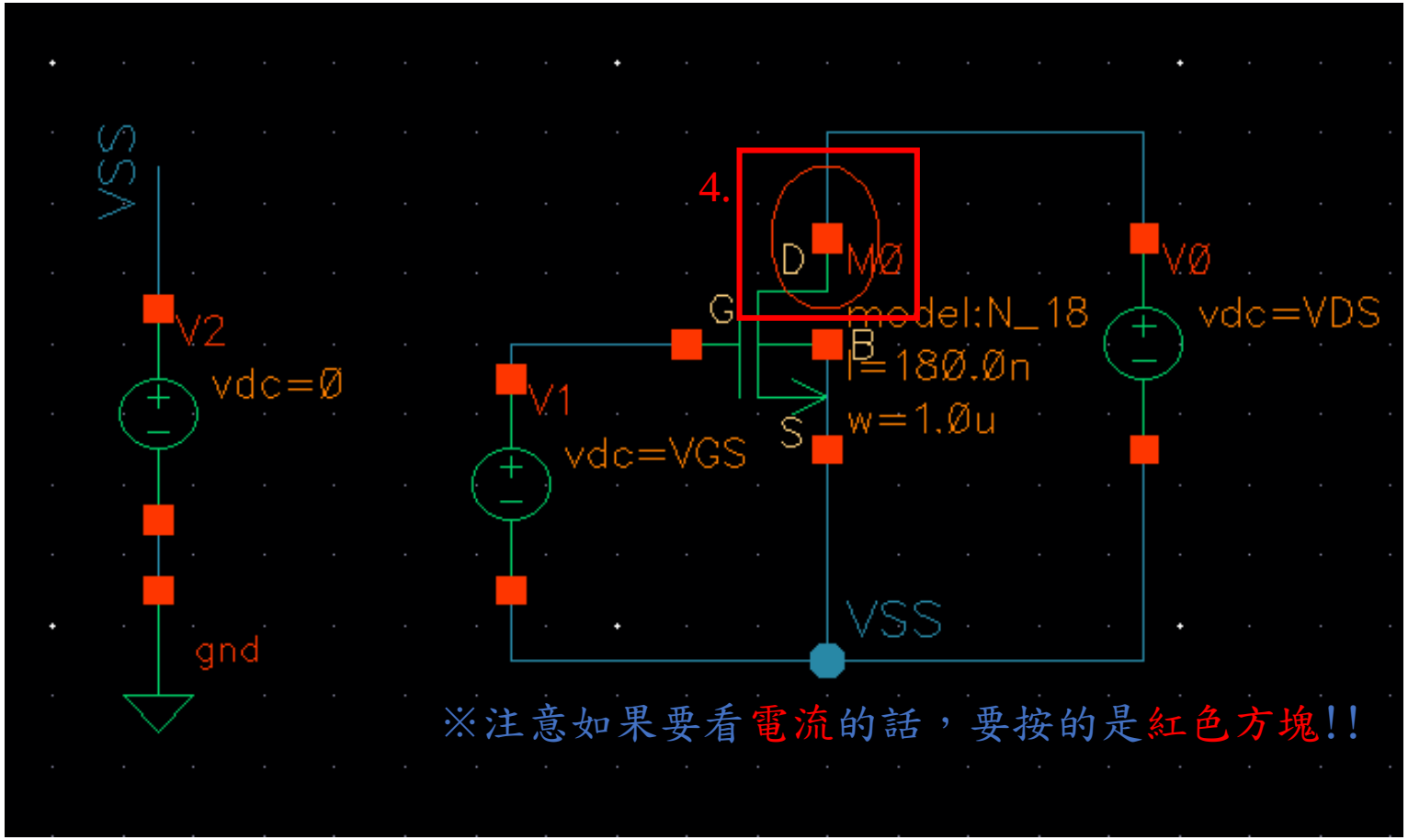
MOSFET I-V Curve





MOSFET I-V Curve

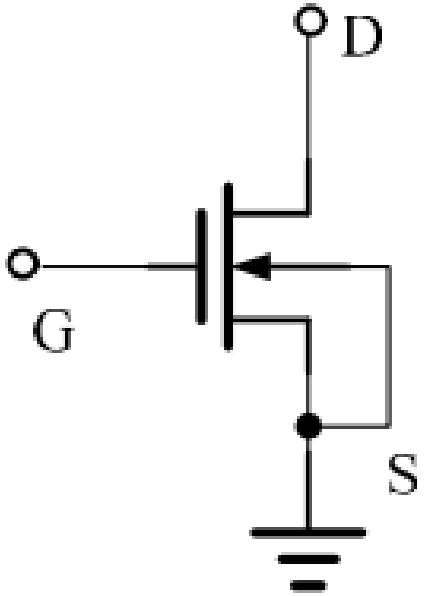




MOSFET I-V Curve

MOSFET I-V Curve

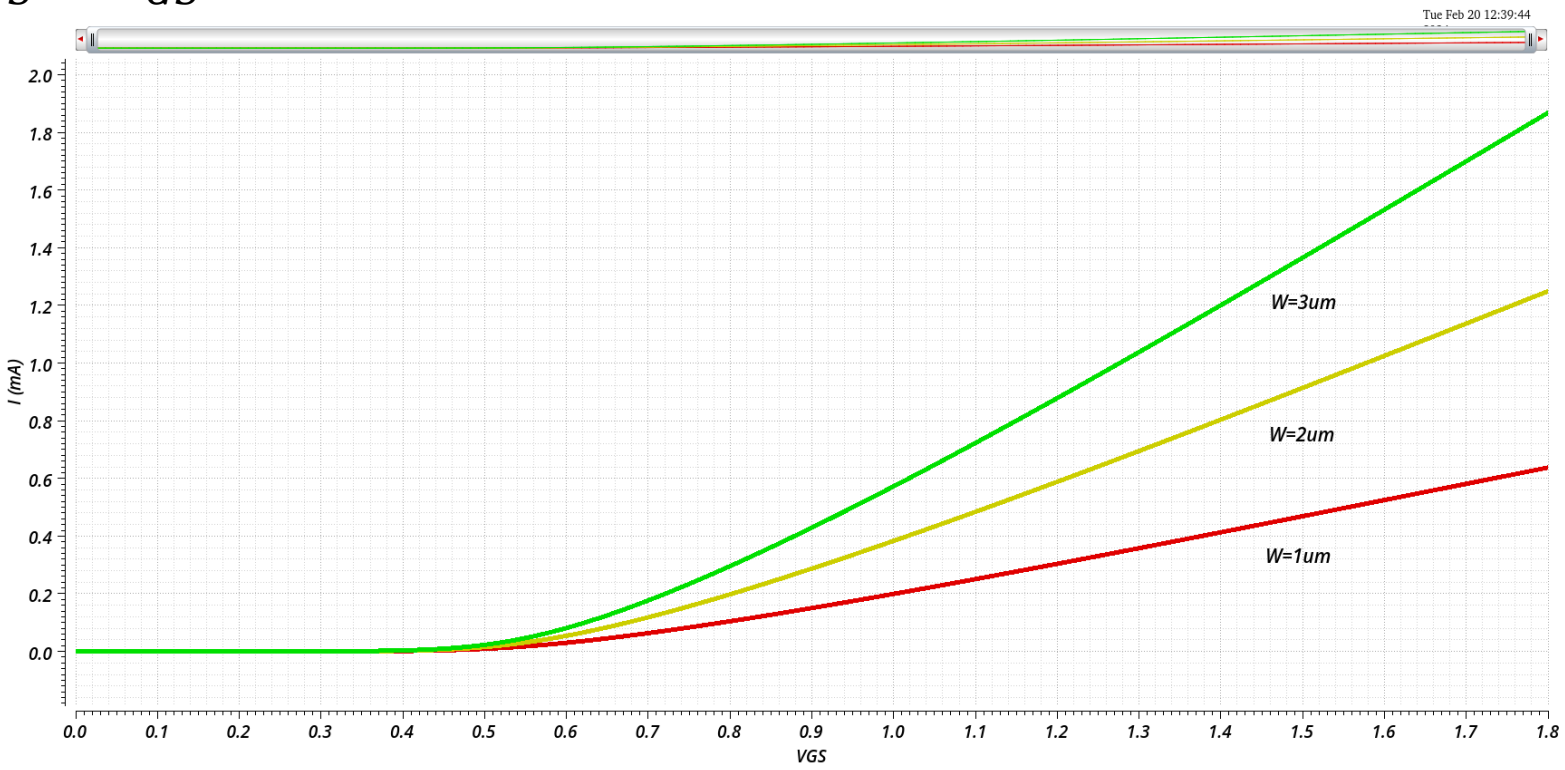
- Lab1_2：改變NMOS的Width，例如把Width放大兩倍，放大三倍，模擬$I_{DS}-V_{GS}$ Characteristic Curve觀察I_D的變化。
- 實驗步驟：試著利用Hspice將圖一的電路描述出來，讓 Length = 0.18um，Width = 1um/ 2um / 3um，V_{DS} = 1.8 V。試著將V_{GS}從0 V到1.8 V每次增加0.01 V，觀察I_{DS}。即為模擬$I_{DS}-V_{GS}$ Characteristic Curve。



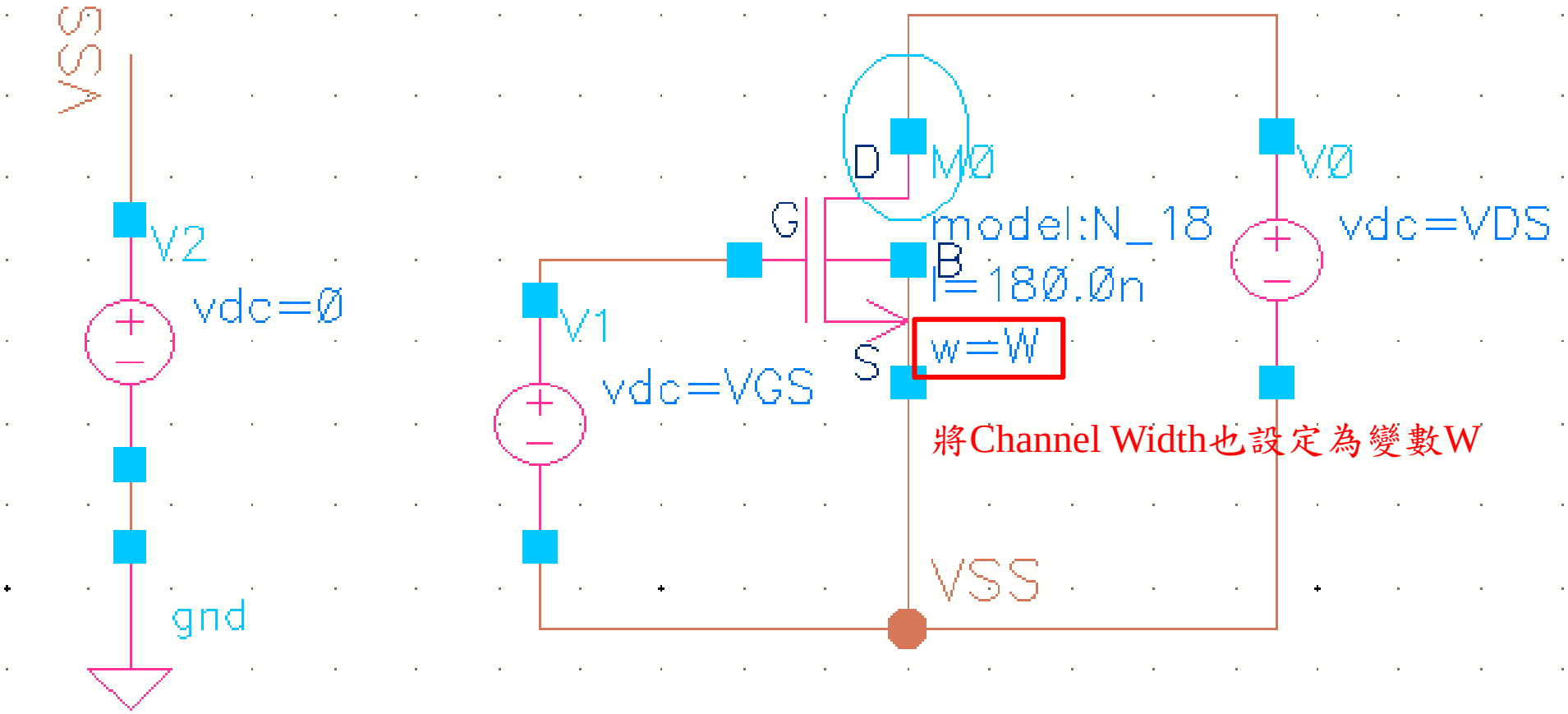
$$\frac{W}{L}=\frac{1um}{0.18um}$$

$$\frac{W}{L}=\frac{2um}{0.18um}$$

$$\frac{W}{L}=\frac{3um}{0.18um}$$

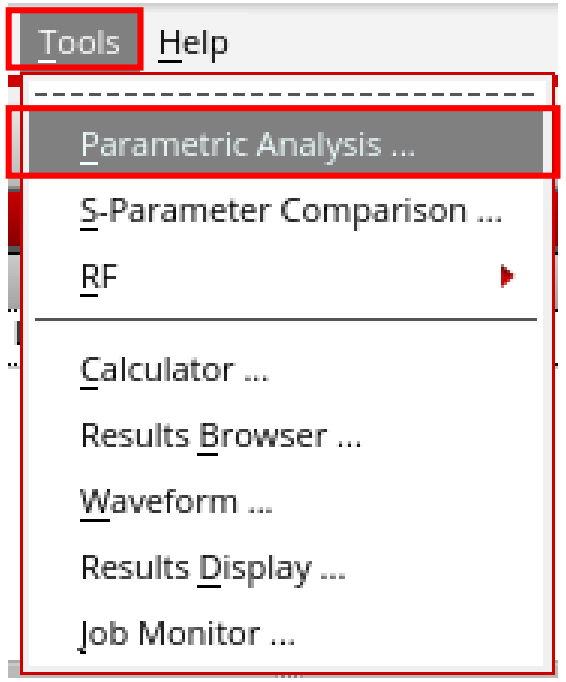


MOSFET I-V Curve



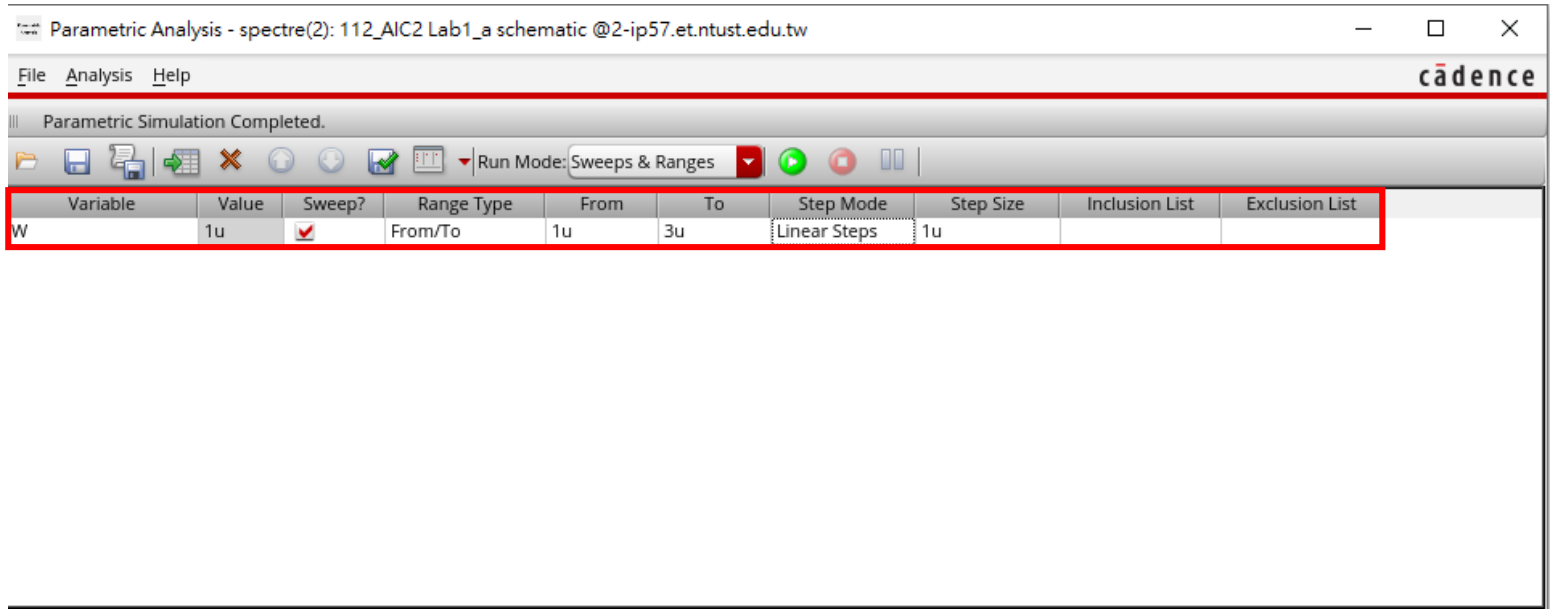
MOSFET I-V Curve

1. Tools → Parametric Analysis ...

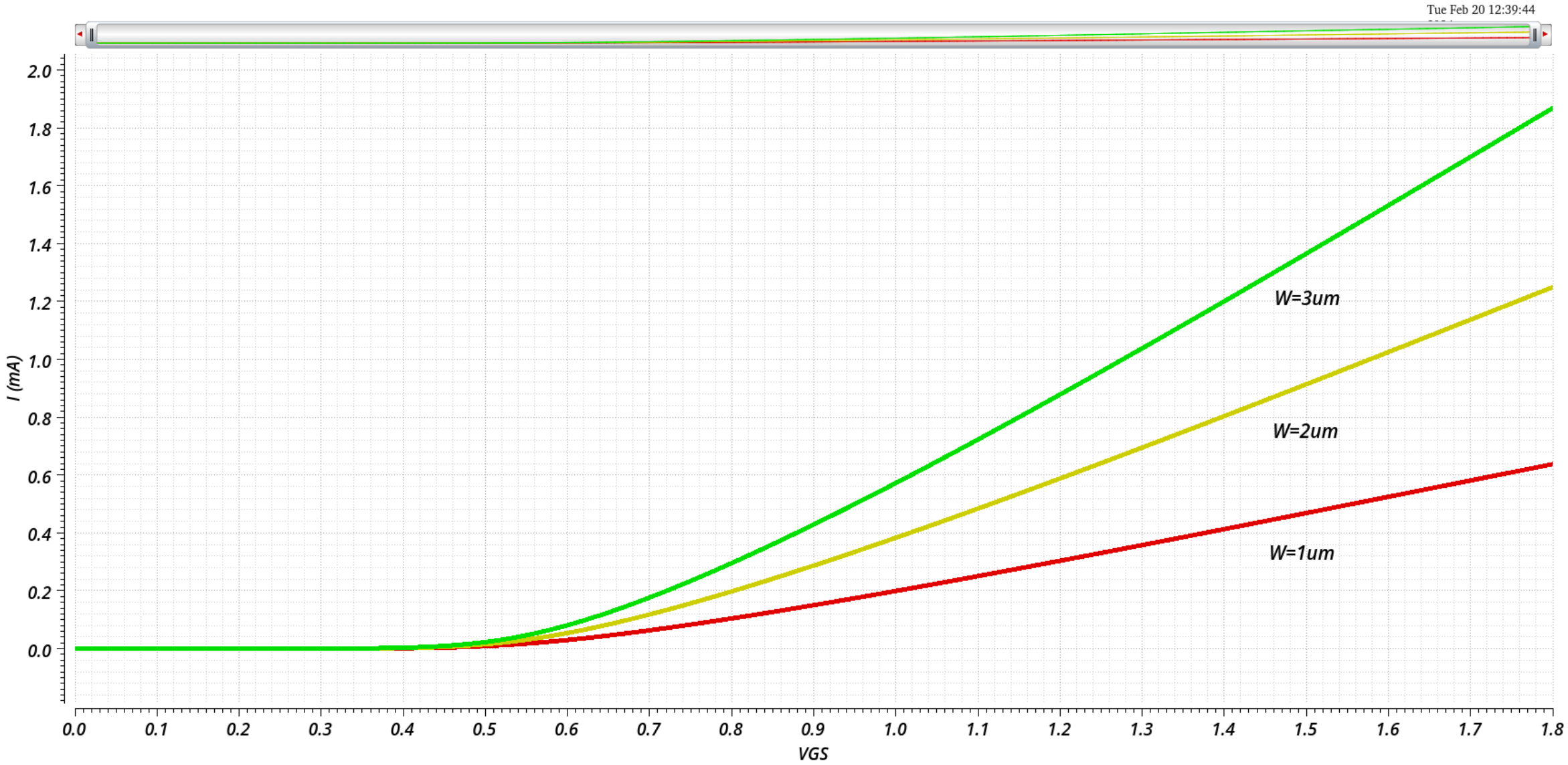


2. Parametric Analysis ...

3.

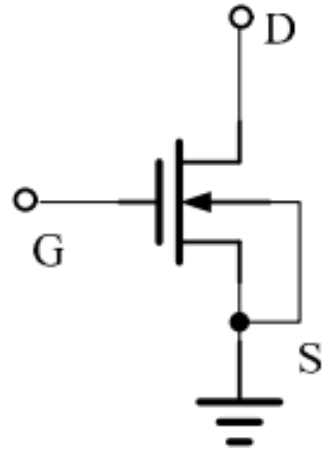


MOSFET I-V Curve

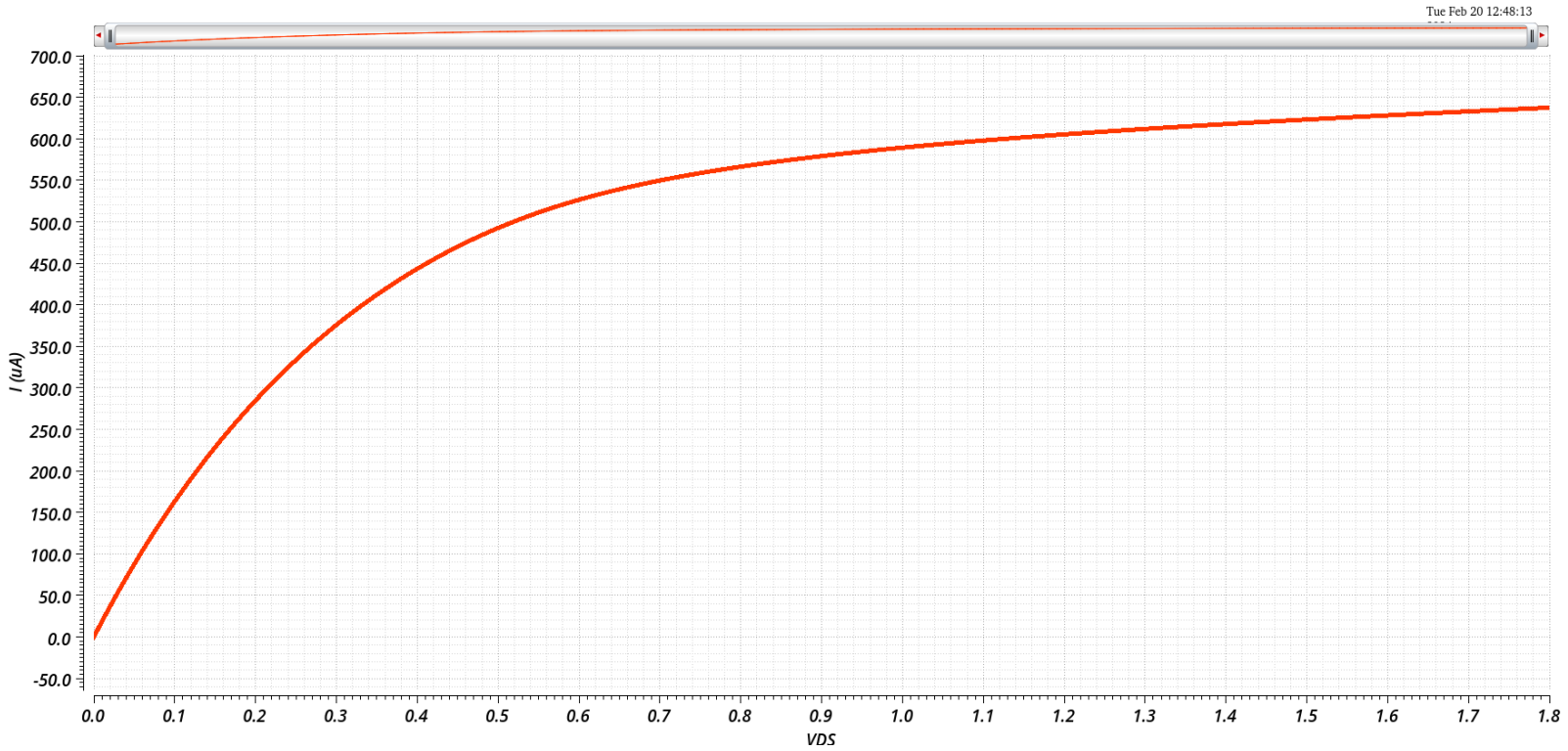


MOSFET I-V Curve

- Lab1_3：由Gate端輸入偏壓V_{GS} = 1.8 V，接著將V_{DS}從0 V到1.8 V每次增加0.01 V，觀察$I_{DS} - V_{DS}$ Characteristic Curve。



$$\frac{W}{L} = \frac{1um}{0.18um}$$



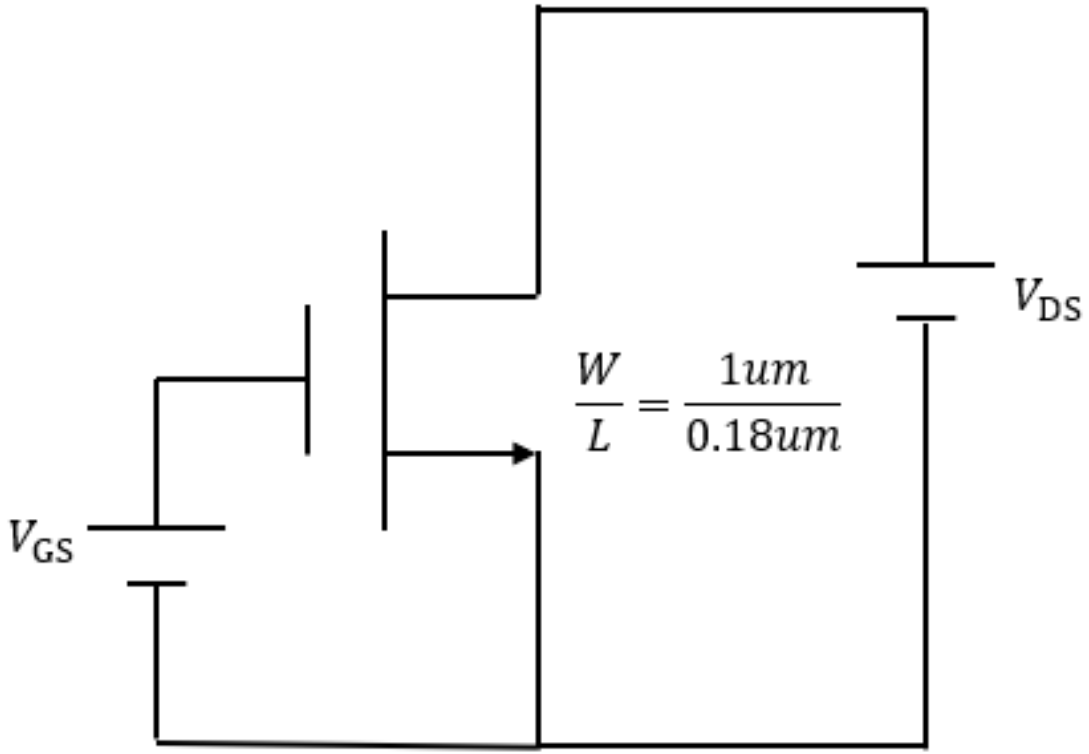
MOSFET I-V Curve

- 改變Gate端的偏壓V_{GS} = 1.5 V、V_{GS} = 1.2 V、V_{GS} = 0.9 V、 V_{GS} = 0.6 V、V_{GS} = 0.3 V、 V_{GS} = 0 V，看$I_{DS} - V_{DS}$ Characteristic Curve，因為MOS在飽和區時，$I_{DS} = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2$由模擬可知，在只有改變$V_{GS}$值的情況下，可以証明得知$I_{DS}$與$V_{GS}$的平方成正比。

- 使V_{GS} = 1.8 V，V_{DS} = 1.8 V改變NMOS元件Channel Width，讓Width = 1.2um，Width = 1.8um，Width = 2.4um，模擬$I_{DS} - V_{DS}$ Characteristic Curve，$I_{DS} = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2$，由模擬可知道，$I_{DS}$與Width成正比，而模擬出來的結果確實也成線性關係。

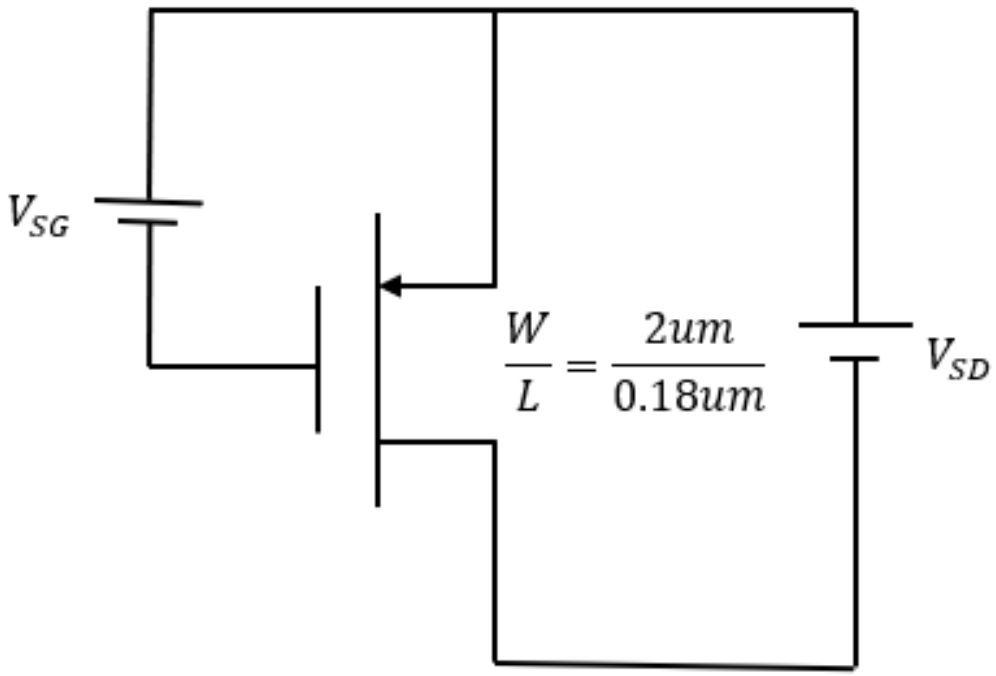
Lab1.a-1

- 用.dc看NMOS特性曲線
  1. I_D對V_{GS}
     (V_{GS} = 0 ~ 1.8 V ; V_{DS} = 0.9 V)
  2. I_D對V_{DS}
     (V_{DS} = 0 ~ 1.8 V ; Sweep V_{GS} = 0.6、0.7、0.8 V)



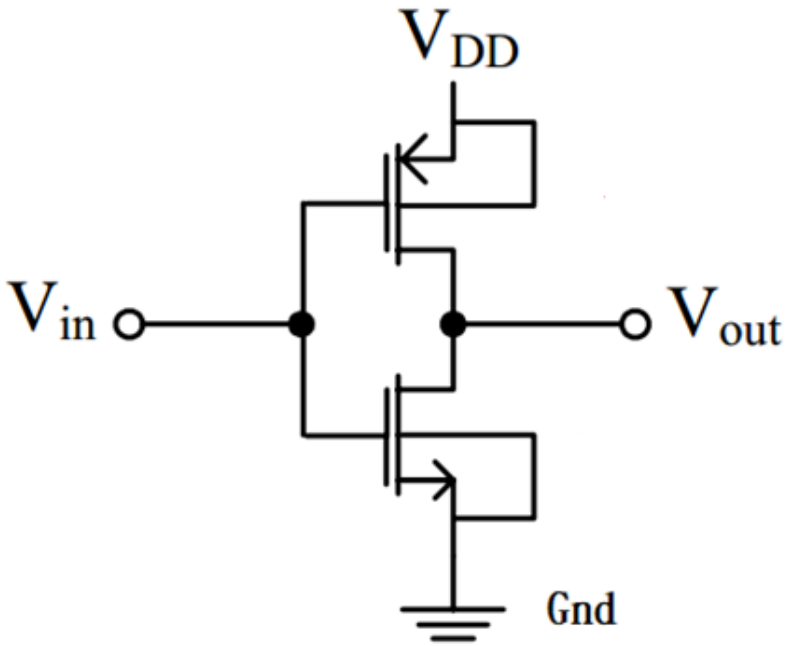
Lab1.a-1

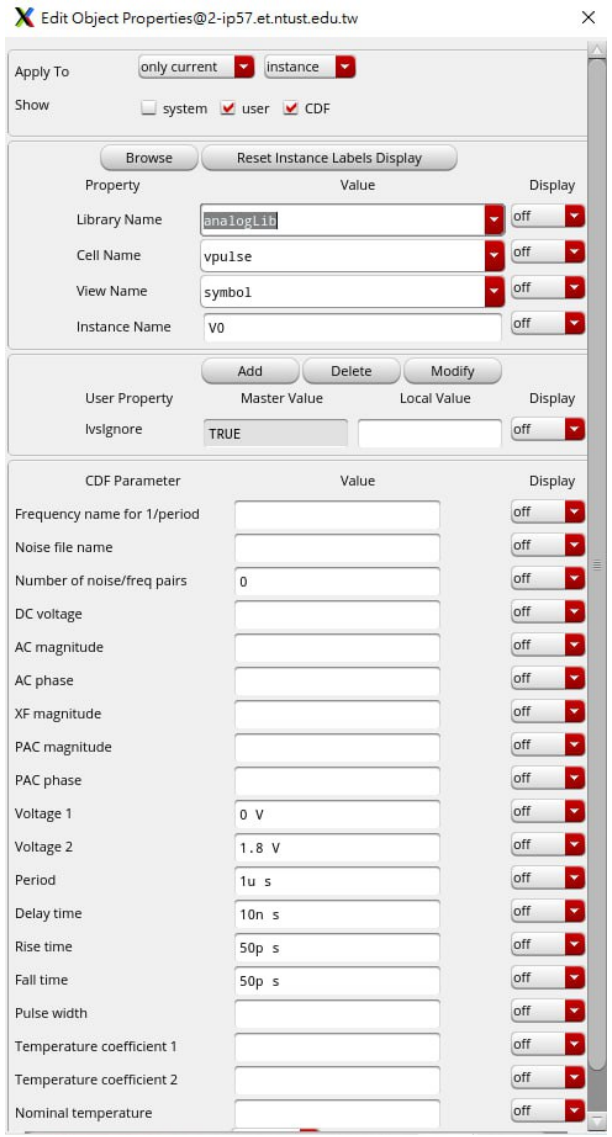
- 用.dc看PMOS特性曲線
  1. I_D對V_{SG}
     (V_{SG} = 0 ~ 1.8 V ; V_{SD} = 0.9 V)
  2. I_D對V_{SD}
     (V_{SD} = 0 ~ 1.8 V ; Sweep V_{SG} = 0.6、0.7、0.8 V)
  3. V_{TH}對V_{BS}
     (V_{BS} = 0 ~ 1.8 V ; V_{SG} = 0.7 V ; V_{SD} = 0.9 V)



Lab1.b

- 利用Virtuoso模擬Inverter電路，使用.tran看輸入和輸出的時序圖
- V_{out}'s loading cap is 50f F
- Design (W/L) to meet
  - L-H and H-L delays less than 100ps
  - Both rise and fall time of V_{out} are less than 100ps





Homework Submission Requirements

- **檔名：Lab1_學號.pdf**

- **請勿抄襲，抄襲者0分**

- **評分標準：**
  - 規定時間內繳交，逾時者會扣分(如有其他原因導致未繳交請與助教聯絡)
  - 符合題目要求規格
  - 完整的設計流程(考慮的原因詳細分析，設計參數如何決定)
  - 模擬結果與分析
  - 面積越小分數越高

Thank You For Your Attention