B卷　以下內容用藍色框框住的部分為題目　　題目小多，可能會寫不完

國立臺灣科技大學答案卷

National Taiwan University of Science and Technology Answer Sheet

評分 Score	教師簽章 Signature of Lecturer
85.5	

姓名/Name 張恒豪　學號/Student ID B110021100　班級/Class 四電子三乙

科目/Course title 嵌入式系統設計　日期/Date 112.10.25

1-1 Please explain what is hard real-time operating system.
1-2 Please explain what is soft real-time operating system.
1-3 Please explain what is firm real-time operating system.

記分欄……不得續用其他紙張作答。/Please write from here.

1 1-1 hard real-time 作業系統一定要符合所有deadline，一個會 miss deadline 的 hard real-time 作業系統沒有任何價值可言。此類系統常用於醫材或軍用設備等關鍵場所。

1-2 soft real-time 作業系統會嘗試符合所有deadline；但如果 miss deadline 的話並不會對系統造成嚴重影響，然而頻繁 miss deadline 會造成系統效能低落。應用在商用電子產品。

1-3 firm real-time 作業系統基本要符合所有deadline，如果 miss deadline 會造成某些應做的工作沒有被做到，但不會造成致命性影響。常應用自動化加工製造機台。 -1.5

firm real-time 作業系統 必須 嘗試滿足所有的 deadline。 (Recall: CH5 ppt, P.15)

2. Please contrast the features of NOR flash memory and NAND flash memory in three aspects.

2

	NOR flash	NAND flash
容量	較小	較大
讀取速度	較快	較慢
寫入速度	較慢	較快

3. ARM uses a load-store model for memory access, which means that only load/store (LDR and STR) instructions can access memory. Complete the execution of the following instructions, show your calculation step by step, and answer the final values of R2.

LDR R2, [R0]
STR R2, [R1]
STR R2, [R1, #4]
LDR R2, [R0, #8]

R0	R1	R2
0x0090	0x0094	0x0098

Address	Memory
0x0098	0x201
0x0094	0x017
0x0090	0x354

3

LDR R2, [R0]

R0	R1	R2
0x0090	0x0094	0x354

Address	Memory
0x0098	0x201
0x0094	0x017
0x0090	0x354

STR R2, [R1]

R0	R1	R2
0x0090	0x0094	0x354

Address	Memory
0x0098	0x201
0x0094	0x354
0x0090	0x354

STR R2, [R1, #4]

R0	R1	R2
0x0090	0x0094	0x354

Address	Memory
0x0098	0x354
0x0094	0x354
0x0090	0x354

LDR R2, [R0, #8]

R0	R1	R2
0x0090	0x0094	0x354

Address	Memory
0x0098	0x354
0x0094	0x354
0x0090	0x354

4-1 What is the utilization bound for Rate Monotonic Scheduling?
4-2 What is the utilization bound for Earliest Deadline First Scheduling?
4-3 When might an operating system miss a deadline?

4. 4-1 $\sum_{k=1}^{n} \frac{C_k}{T_k} \le n(2^{\frac{1}{n}}-1)$, where:

n = number of periodic tasks
C_k: burst time of the task
T_k: period of the task

4-2 $\sum_{k=1}^{n} \frac{C_k}{T_k} \le 1$, where:

n = number of periodic tasks
C_k = burst time of the task
T_k = period of the task

4-3 如果系統使用率高於最低上限，系統可能發生 miss deadline

5. Two widely used priority-driven scheduling algorithms are the Rate Monotonic Scheduling and the Earliest Deadline First Scheduling. The Earliest Deadline First Scheduling has higher schedulability than the Rate Monotonic Scheduling. However, many real-time applications still use the Rate Monotonic Scheduling. Discuss why this might be.

記分欄 轉頁從此開始寫起。

5. 因為大部份的系統中任務的優先級會被固定，且 Rate Monotonic 不需要反覆計算任務優先級，這樣能減少 scheduling 對系統造成的負擔。

如此能使系統盡可能快速地處理關鍵的任務；
而不像使用 Earliest Deadline First 可能導致關鍵任務被某些較不重要但到來到來週期較為頻繁的任務搶占資源。

6-1 What is the solution to prevent Unbounded Priority Inversion?
6-2 Continuing with 6-1, how does this mechanism work?
6-3 Please compare and explain the difference between the Bounded Priority Inversion and Unbounded Priority Inversion.

6 6-1 Priority Ceiling Protocol

6-2 將正在占用 locked resource 的 task 的優先級提高至和可能會用到此 resource 的最高優先級的 task 相同，這樣能避免 Unbound Priority Inversion 的情況發生。

6-3

	Bound Priority Inversion	Unbound Priority Inversion
高優先級任務無法被及時執行	和使用 lock 的較低優先級任務有關	和使用 lock 的較低優先級任務沒有直接關係，反而與搶佔該任務的中等優先級任務有關

7. Given the following system definition (all tasks are independent, and are scheduled preemptively on a single processor system):

7-1 Can these tasks be scheduled with the Earliest Deadline First Scheduling and a Total Bandwidth Server? Explain your answer with the utilization bound.

7-2 How to schedule these tasks with the Earliest Deadline First Scheduling and a Constant Utilization Server? Explain your answer step by step and show the variance of the server budget with the timeline of the task execution from t = 0 to t = 12.

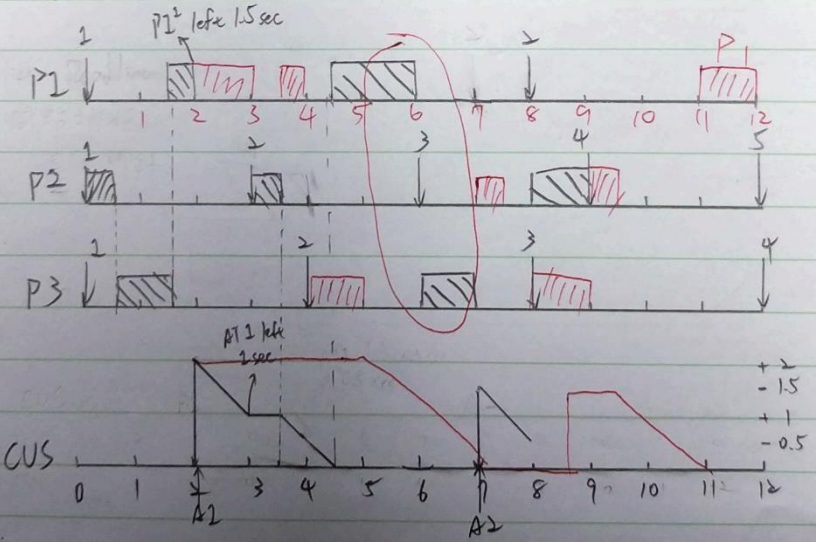
	Process	Arrival Time	Burst Time	Period
Periodic Tasks	P1	0	2	8
	P2	0	0.5	3
	P3	0	1	4
Aperiodic Tasks with Dynamic Priority Server ($U_s = 0.3$)	A1	2	2	-
	A2	7	1.5	-

7 7-1

利用率低於 100%，就能用 Total Bandwidth 排程：

$$\frac{e_{P1}}{P_{P1}} + \frac{e_{P2}}{P_{P2}} + \frac{e_{P3}}{P_{P3}} + U_s^{0.3} = \frac{1}{2} + \frac{1}{6} + \frac{3}{10} \le 1 \Rightarrow \text{可以用 Total Bandwidth 排程}$$

7-2



訂正在 P.4

At t=0:
$P(P1^1) = 0+8 = 8$
$P(P2^1) = 0+3 = 3$
$P(P3^1) = 0+4 = 4$
$d=0, e_s=0$

At t=2:
$d = t + \frac{e_s}{U_s} = 2 + \frac{2}{0.3} = \frac{26}{3}$
$P(P1^2) = 8$

At t=3:
$d = \frac{20}{3}$
$P(P1^2) = 8$
$P(P2^2) = 3+3 = 6$

At t=4
$d = \frac{20}{3}$
$P(P1^2) = 8$
$P(P3^2) = 4+4 = 8$

At t=6:
$P(P2^3) = 6+3 = 9$
$P(P3^2) = 8$

At t=7:
$P(A2) = 7 + \frac{e_s}{U_s} = 12$
$P(P2^3) = 9$

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科目/Course title 嵌入式系統設計　日期/Date 112.10.25

8. List two of the challenges of System-on-Chip (SoC) with detailed explanations.

8 1.研發成本高，因為SoC不僅需要設計 Micro Controller，還要設計周邊的 RAM, ROM，甚至是 DSP

2.可調整彈性低，因為SoC是將整個系統做在單一晶片中，因此要更改系統中的個別元件規格就需要重新流片生產。

9. List three of the features of Field Programmable Gate Array (FPGA) with detailed explanations.

9 1.~~可重複使~~用性：內部電路能反覆利用燒錄的方式更改。

2.低耗能：相比於 Micro Processor，FPGA 功耗更低。

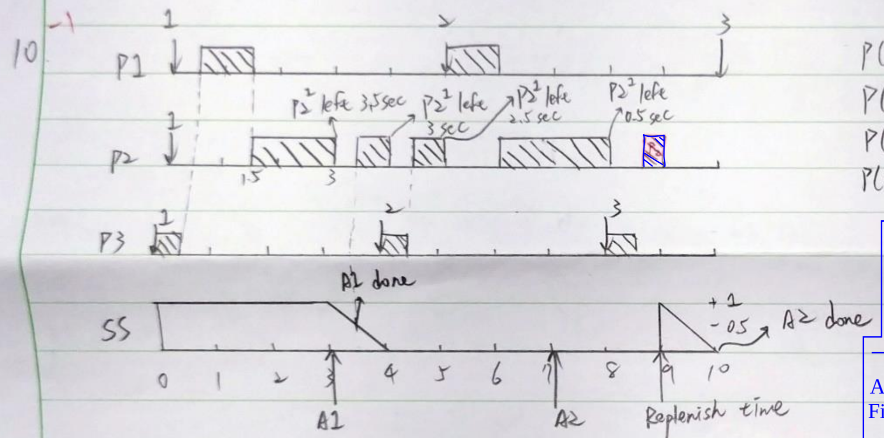
3.平行處理：由於內部是數位電路，因此資料的運算可以被同時運行。

10. Given the following system definition (all tasks are independent, and are scheduled preemptively on a single processor system):

	Process	Arrival Time	Burst Time	Period
Periodic Tasks	P1	0	1	5
	P2	0	5	40
	P3	0	0.5	4
Aperiodic Tasks with Fixed-Priority Server. (Arrival Time = 0 Burst Time = 1 Period = 6)	A1	3	0.5	-
	A2	7	1	-

How to schedule these tasks with the Rate Monotonic Scheduling and a Sporadic Server? Explain your answer step by step and show the variance of the server budget with the timeline of the task execution form t = 0 to t = 10.

10



$P(P1) = \frac{1}{5}$ ②

$P(P2) = \frac{1}{40}$ ④

$P(P3) = \frac{1}{4}$ ①

$P(SS) = \frac{1}{6}$ ③

At t=3:

$t_r(3) > END(1.5) \Rightarrow t_e = t_f = 3$

⇒ next replenish time:

$t_e + P_s = 3 + 6 = 9$

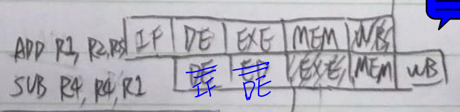
At t=3.5:

END < t && SS has consumed its budget since t_f(0)

⇒ keep consuming budget.

11. List two of the possible Pipeline Hazards with detailed explanations.

11 Data Hazard：正在執行的指令需要現在正在處理中的資料



需要知道R4要被減多少，但R1值尚被更
→ Data Hazard

Structure Hazard：同時需要利用到一樣的元件，例如：同時執行多條指令 load 和 store，但電路只有一個 memory。

7. Given the following system definition (all tasks are independent, and are scheduled preemptively on a single processor system):

7-1 Can these tasks be scheduled with the Earliest Deadline First Scheduling and a Total Bandwidth Server? Explain your answer with the utilization bound.

7-2 How to schedule these tasks with the Earliest Deadline First Scheduling and a Constant Utilization Server? Explain your answer step by step and show the variance of the server budget with the timeline of the task execution from t = 0 to t = 12.

	Process	Arrival Time	Burst Time	Period
Periodic Tasks	P1	0	2	8
	P2	0	0.5	3
	P3	0	1	4
Aperiodic Tasks with Dynamic Priority Server ($U_s = 0.3$)	A1	2	2	-
	A2	7	1.5	-

先把規則列出來：

當 Aperiodic Task 到來時：

if: deadline 還沒到

把到來的 Aperiodic Task 丟到 queue

else

if: queue 為空

$d = t + \frac{e}{U_s}$

$e_s = e$

else

把到來的 Aperiodic Task 丟到 queue

當一個 Aperiodic Task 做完後，queue 還有其他 Aperiodic Task

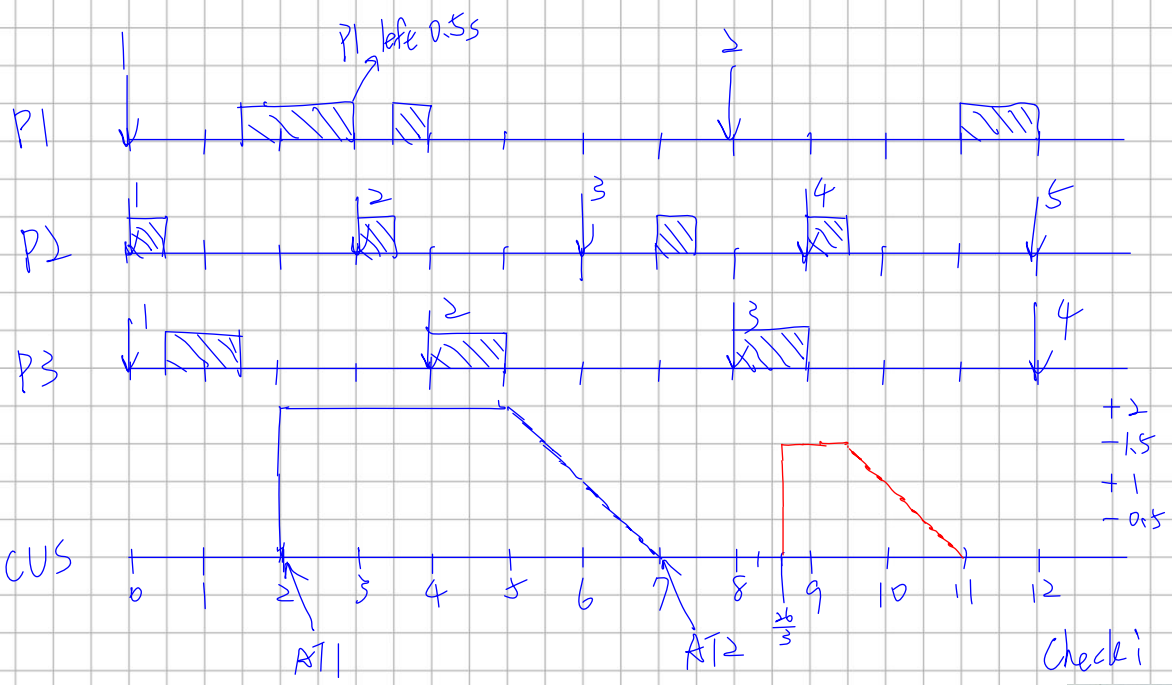
if deadline 還沒到

啥也不做

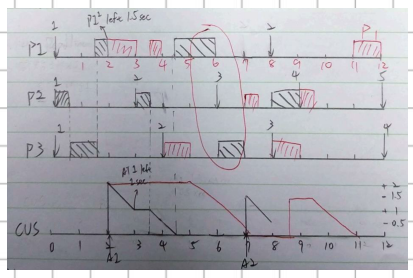
else

$d = d + \frac{e}{U_s}$

$e_s = e$



Check:



OK

t=0:

P(P1') = 0+8 = 8

P(P2') = 0+3 = ③

P(P3') = 0+4 = 4

t=0.5

P(P1') = 8

P(P3') = ④

t=1.5

P(P1') = ⑧

t=2:

P(P1') = ⑧

$P(d1) = 2 + \frac{1}{0.3} = \frac{26}{3}$

t=3:

P(P1') = 8

$P(d1) = \frac{26}{3}$

P(P2') = 3+3 = ⑥

t=3.5:

P(P1') = ⑧

$P(d1) = \frac{26}{3}$

t=4:

$P(d1) = \frac{26}{3}$

P(P3') = 4+4 = ⑧

t=6:

P(d1) = ⑨

P(P2') = 6+3 = 9

t=7:

P(P2') = ⑨

$t < \frac{26}{3}$

⇒ AT2 to the queue

t=8:

P(P1') = 8+8 = 16

P(P3') = 8+4 = ⑫

$t < \frac{26}{3}$

⇒ keep AT2 in queue

$t = \frac{26}{3}$:

P(P1') = 16

P(P3') = ⑫

$P(d2) = \frac{26}{3} + \frac{1.5}{0.3} = \frac{41}{3}$

t=9:

P(P1') = 16

$P(d2) = \frac{41}{3}$

P(P3') = 9+3 = ⑫

t=11:

P(P1') = ⑯