3. (10%) The external interrupt of MCS-51 refers to the interrupt from the chip hardware pins INT0 and INT1. These two external interrupts can be triggered by (P3.2) and (P3.3).

正確 P3.2 負緣觸發 低準位觸發 -10

4. (10%) There are two ways for a single chip to process external input and output signals, (INT P3.0) cannot process some time-sensitive external input signals immediately, but (timer) can immediately make immediate response and processing. I/O -10

5. (10%) What is the purpose of IE.2 and IE.7?

IE.7	IE.6	IE.5	IE.4	IE.3	IE.2	IE.1	IE.0
EA	--	ET2	ES	ET1	EX1	ET0	EX0

(EA=1) (EX=1)

Enable IE register的功能 Enable INT X

6. (10%) What is the purpose of TCON.0 and TCON.1? IE：中斷發生時自動設1，結束變0。 -5

TCON.7	TCON.6	TCON.5	TCON.4	TCON.3	TCON.2	TCON.1	TCON.0
TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

IT0=0, IT1=0, timer interrupt為低準位觸發，為1則是負緣觸發。

7. (20%) Please correctly order the interrupt process flow by filling in the number.
(2) -> (1) -> (3) -> (5) -> (4)

(1) When an interrupt occurs, confirm the interrupt and priority order

(2) Setting of IE, IP or TCON registers, etc.

(3) Save PC/SFR to the stack and pause the current program

(4) After the interrupt function is completed, the PC/SFR are retrieved from the stack and continue the previously executed program

(5) PC gets the corresponding interrupt vector address and jumps to the interrupt function