1. (12%) Assuming silicon is doped with phosphorus (P) at a concentration of 2×10^{16} cm^{-3} at 60°C. Other parameters for the silicon sample include: $B = 5.23 \times 10^{15} \mathrm{cm^{-3}K^{-3/2}}$, $E_g = 1.1$ eV, $\mu_n = 1250\ \mathrm{cm^2/V \cdot s}$, $\mu_p = 450\ \mathrm{cm^2/V \cdot s}$, $D_n = 35\ \mathrm{cm^2/s}$, and $D_p = 10\ \mathrm{cm^2/s}$. (a) What are the concentrations of electrons and holes for this silicon (4%)? (b) Calculate the current density if an electric field of $E = 50\ \mathrm{V/cm}$ is applied to the material (4%). (c) Following (b), if this doped semiconductor material is placed at 0°C, will the current density be significantly increased, slightly increased, slightly decreased, or significantly decreased? (2%) and explain why (2%).

2. (10%) The diode in the circuit shown in Figure 2 has a reverse-saturation current of $I_S = 5 \times 10^{-13}$ A. (a) Assume the cut-in voltage of the diode is $V_\gamma = 0.6$ V, determine the approximate diode voltage and current using piecewise linear model (4%). (b) Using the diode current equation and iteration method, determine the exact values of diode voltage and current (6%)?

3. (12%) Let $V_\gamma = 0.7$ V for each diode in the circuit in Figure 3, and $R_1 = 5$ kΩ, $R_2 = 10$ kΩ. (a) For $V_I = 10$ V, find I_{D1} and V_O (4%). (b) Plot V_O versus V_I for $-10 \le V_I \le 10\,V$. Indicate the breakpoints and the state of each diode in the various region of the plot (8%).

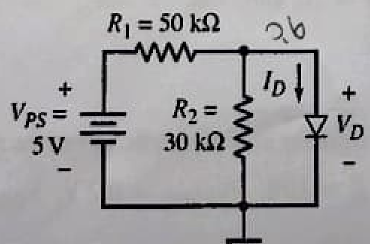

Figure 2

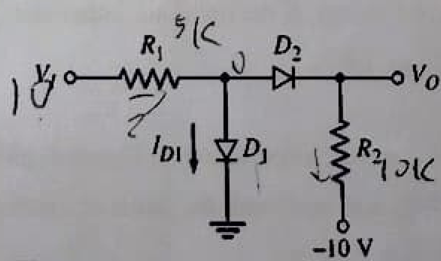

Figure 3

4. (16%) Consider the rectifier circuit shown in Figure 4 with an input voltage $v_S = 6 * sin\omega t$, and assume the diode cut-in voltage $V_\gamma = 0.6$ V. (a) Plot the v_O versus time and indicate the maximum and minimum value of v_O. (b) Determine the fraction (percent) of time that the diode D_1 is conducting. (c) What is the PIV rating of the diodes? (d) Assume a filter capacitance is connected in parallel with $R_L = 1$ kΩ, and the ripple voltage is to be limited to 0.1 V. Find the required value of the capacitor.

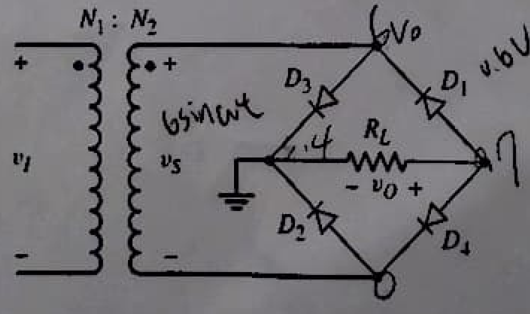

Figure 4

5. (10%) A Zener diode is connected in a voltage regulator circuit as shown in Figure 5. The Zener voltage is $V_{Z0} = 10\text{ V}$ and the Zener resistance is assumed to be $r_Z = 0$. The output load current varies between $I_L = 50\sim500\text{ mA}$ and the input voltage varies from $V_{PS} = 15\sim20\text{ V}$. (a) Determine the value of R_i such that $I_Z(\min) = 0.2 * I_Z(\max)$. (b) Following (a), if $r_Z = 5\ \Omega$, determine the percent source regulation (assume minimum load current)

6. (8%) For the circuit shown in Figure 6, the transistor parameters are: $\beta = 50$, $V_{BE(on)} = 0.6\text{ V}$, $V_{CE(sat)} = 0.2\text{ V}$, and $V_A = \infty$. Determine the values of (a) I_C and (b) V_{CE}.

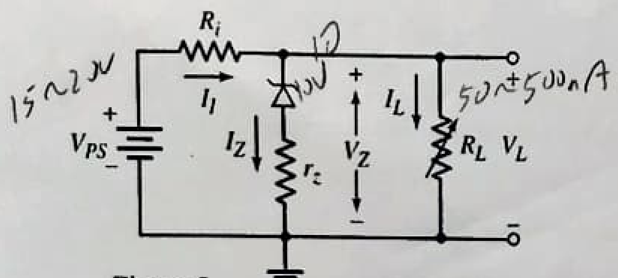

Figure 5

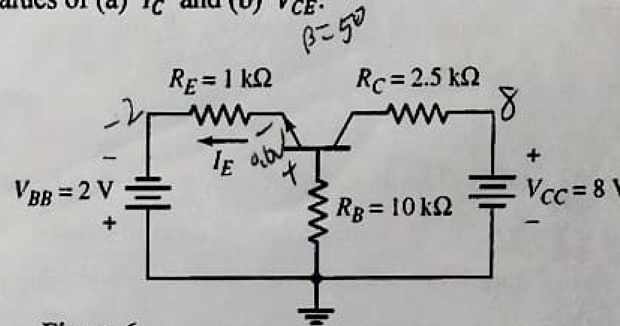

Figure 6

7. (18%) For the circuit shown in Figure 7, the transistor parameters are: $\beta = 150$, $V_{BE(on)} = 0.7\text{ V}$, $V_{CE(sat)} = 0.2\text{ V}$, and $V_A = \infty$. (a) sketch the load line and show the slope (3%). (b) Determine the required value of I_{CQ} such that the Q-point is in the center of the load line (3%). (c) Design R_1 and R_2 such that the circuit is bias-stable (6%). (d) Following (c), for the designed circuit, if the transistor parameter β is changed to 50, calculate the new value of I_{CQ} and V_{CEQ} (6%).

8. (14%) For the circuit shown in Figure 8, plot the voltage transfer characteristics over the range $0 \le V_I \le 5\ V$ and mark the status of transistor. Assume $\beta = 100$, $V_{EB(on)} = 0.7\text{ V}$, $V_{EC(sat)} = 0.2\text{ V}$, and $V_A = \infty$.

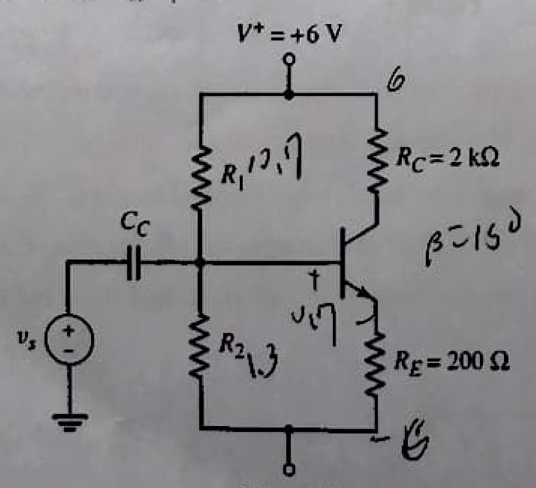

Figure 7

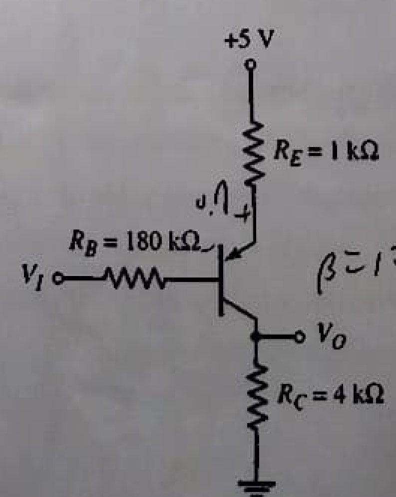

Figure 8

$\frac{5-0.7-V_I}{180k}$