TAIWAN TECH National Taiwan University of Science and Technology

Introduction to Analog Integrated Circuit Design

Fall 2023

MOST Physics

Yung-Hui Chung

MSIC Lab

DECE, NTUST

Mixed-Signal IC Laboratory NTUST

Understanding MOS Transistors

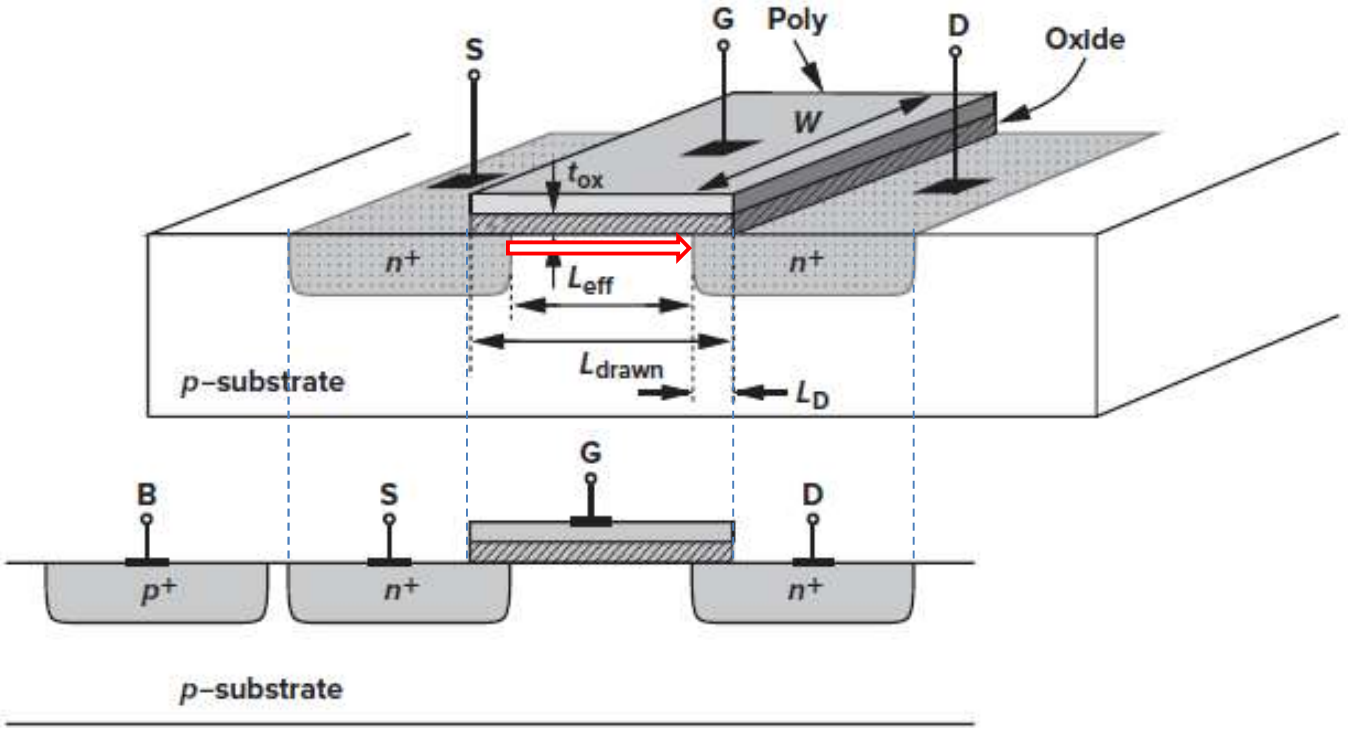
CMOS Transistors

- Quantum mechanics
- Solid-state physics
- Semiconductor device physics
- Device modeling
- Design of circuits

- **Current formula**
- **Basic Operation and MOS Physics**
- **Short-Channel Effects**
- **Second-Order Effects**
- **Design of circuits, …**

Why CMOS?

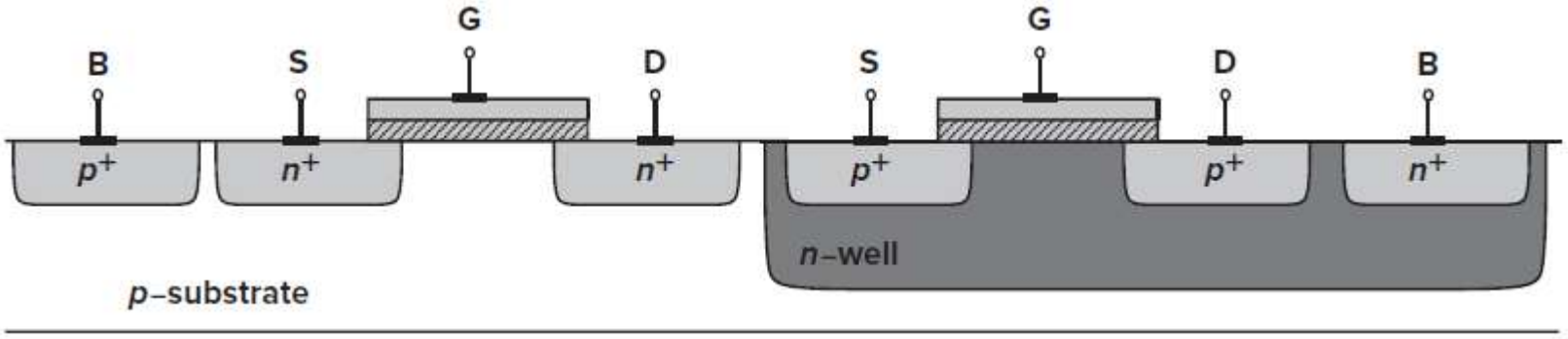
MOS Device Structure



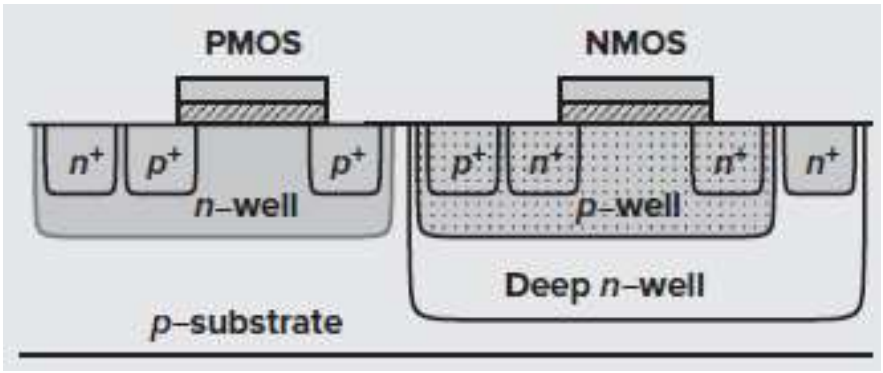
- **2D-device: planar CMOS transistors**
  - Source/Drain: Diffusion
  - Substrate/Well : p-sub/n-well
  - Gate oxide: SiO2, t_{ox}
  - Poly Gate → HKMG (High-K and Metal Gate) in nanometer CMOS
- 3D-device: FinFET MOS Transistors

MOS Device Structure

Basic p/nMOS Transistors (pMOST and nMOST in CMOS VLSI)

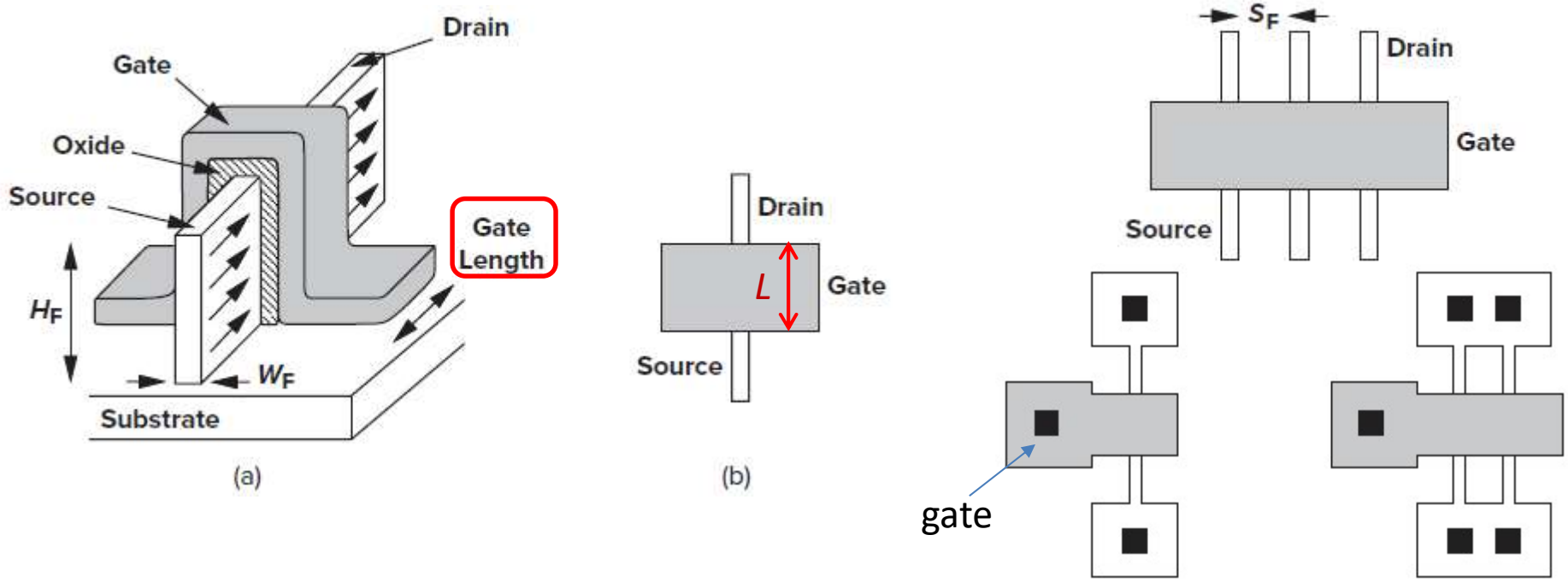


- Twin-Well Process
- Deep-Nwell Process



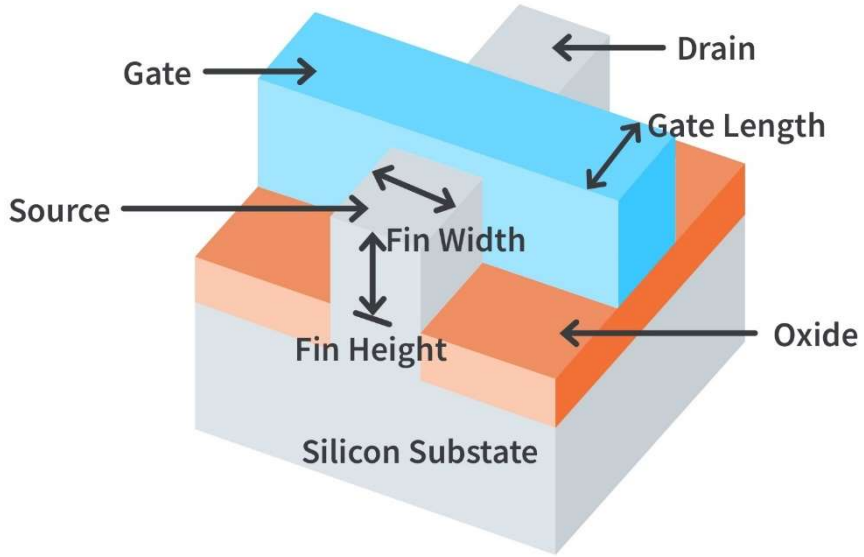
- Various device types (by its threshold voltage or …):
  - SP_LVT; SP_RVT; SP_HVT; Zero-VT; Native; …

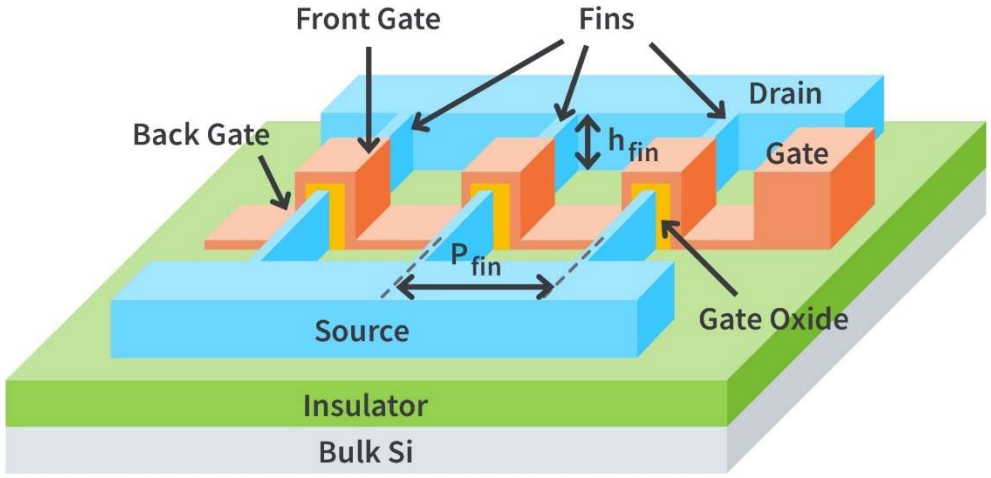
FinFET (3D-MOS Transistors)

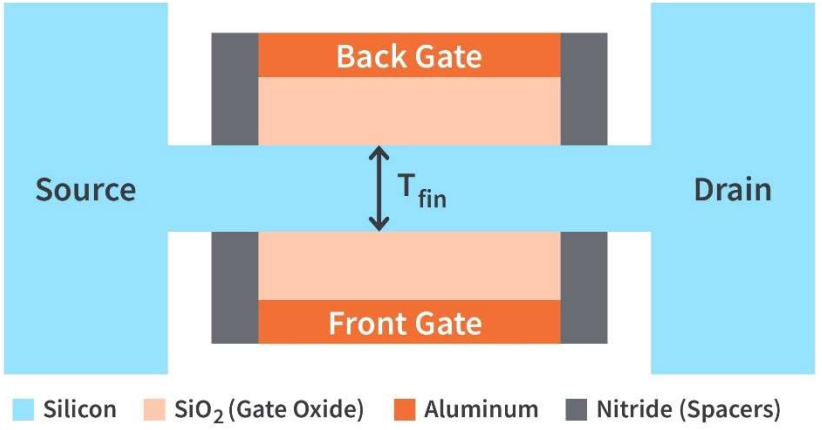


- L < 20 nm => **FinFET era** (**TSMC**, Samsung, Intel, …)
- In fact, FinFET I/V characteristics are closer to square-law behavior, making our simple large-signal mode relevant again
- Channel width: **W** = $W_F + 2H_F$ (fixed) → W' = Nf*W, Nf is # of Fins
- The spacing between the fins, $\mathbf{S_F}$, also plays a significant role in the performance

FinFET (3D-MOS Transistors)

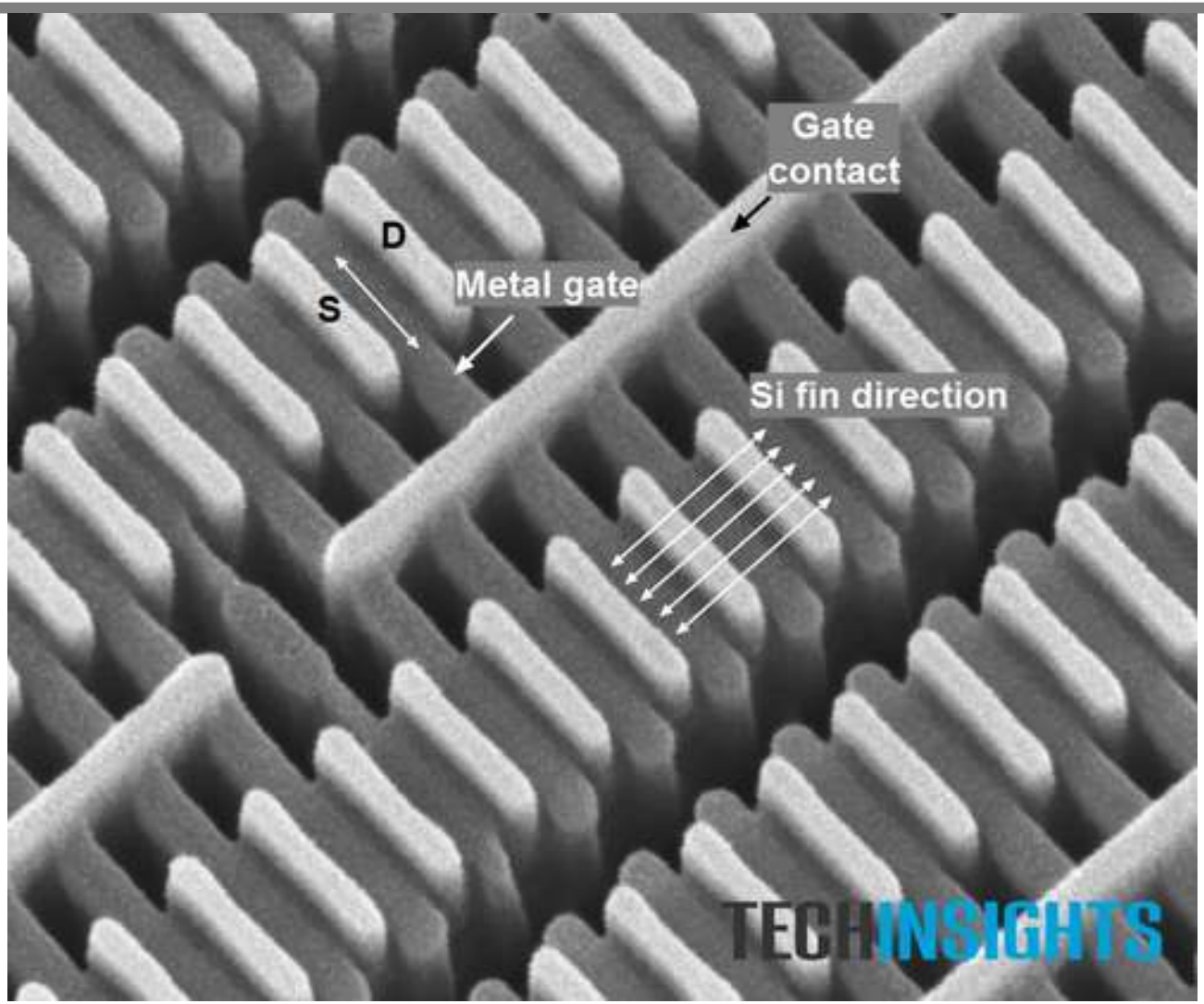






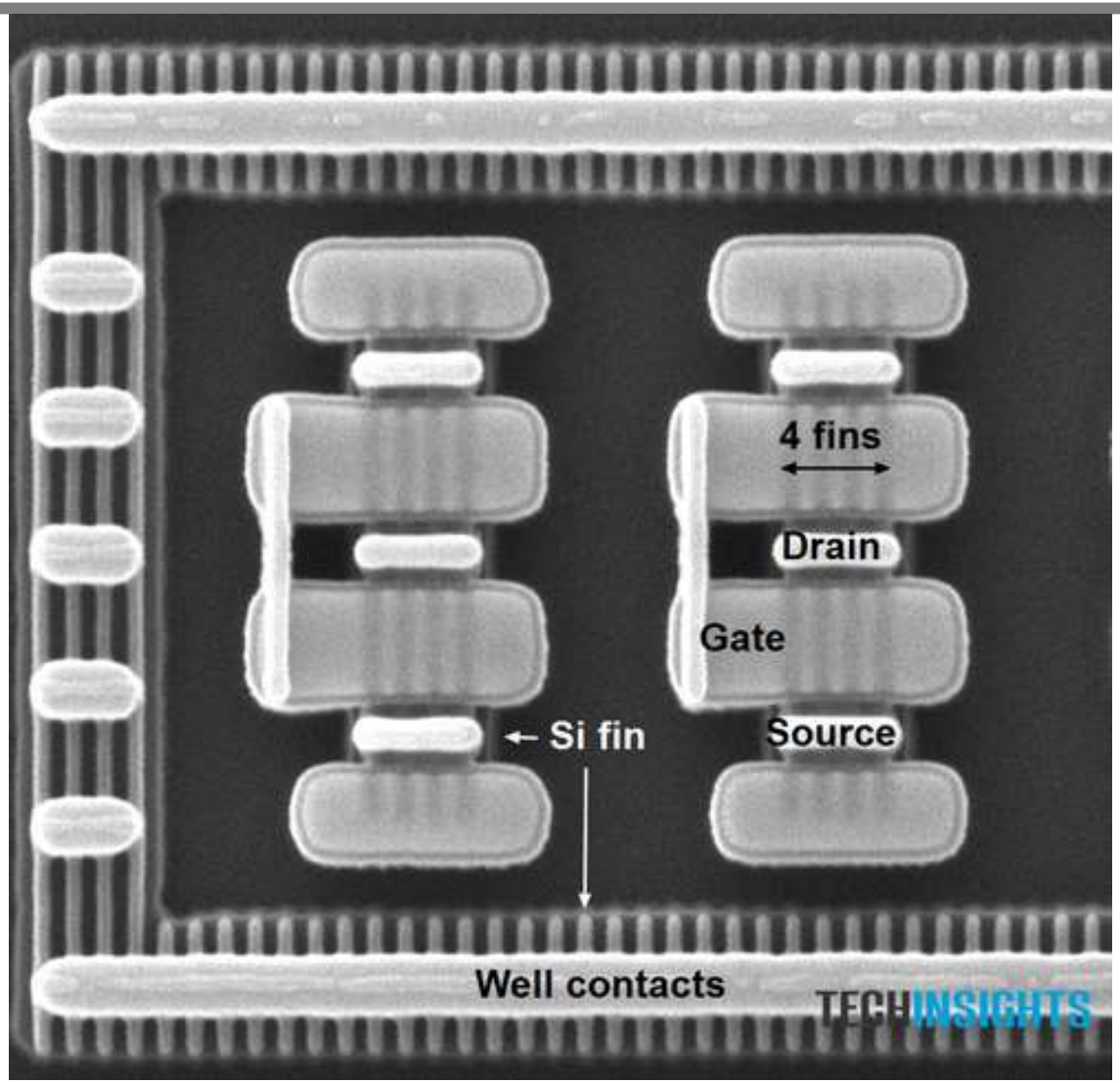
https://www.circuitbread.com/ee-faq/what-isa-finfet

FinFET Transistors: SEM Image



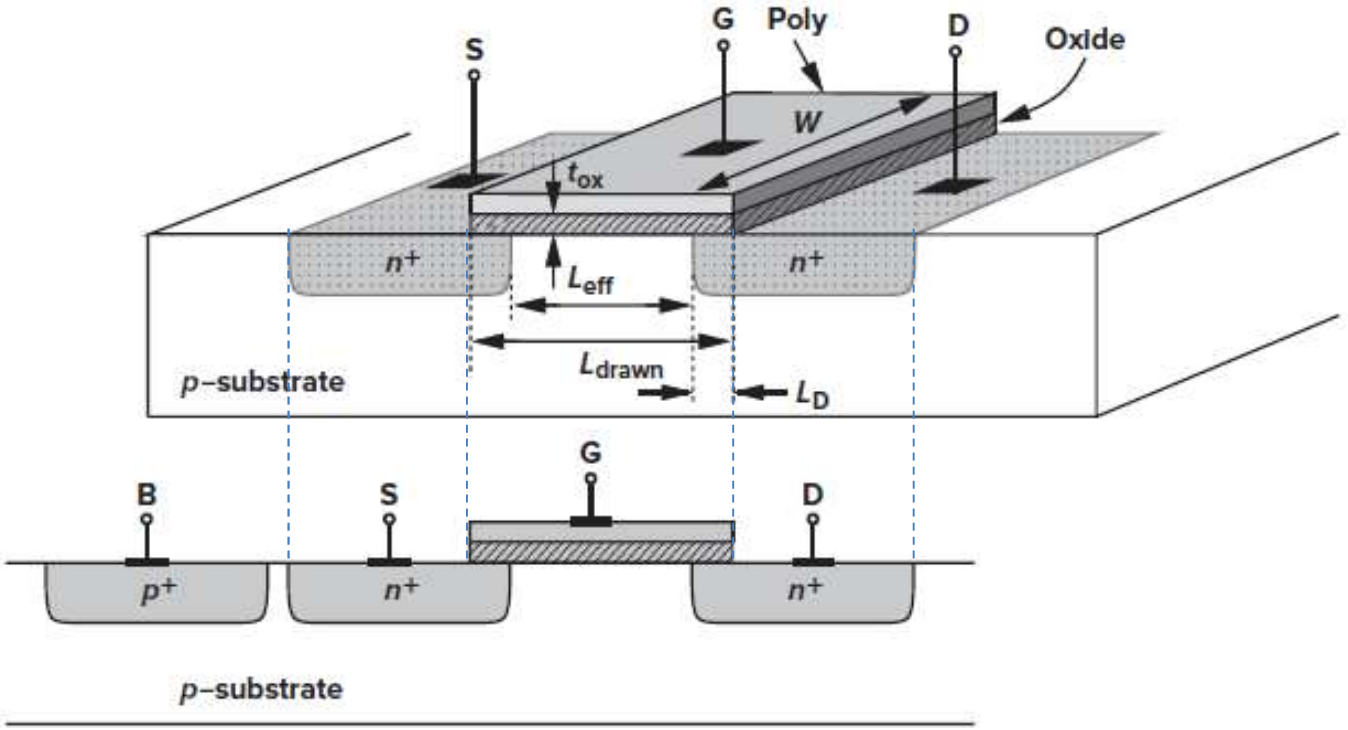
Tilt view SEM image of Samsung 14 nm FinFET transistors (Source: *Samsung 14 nm Exynos 7 7420 Logic Detailed Structural Analysis*, TechInsights)

FinFET Transistors: SEM Image



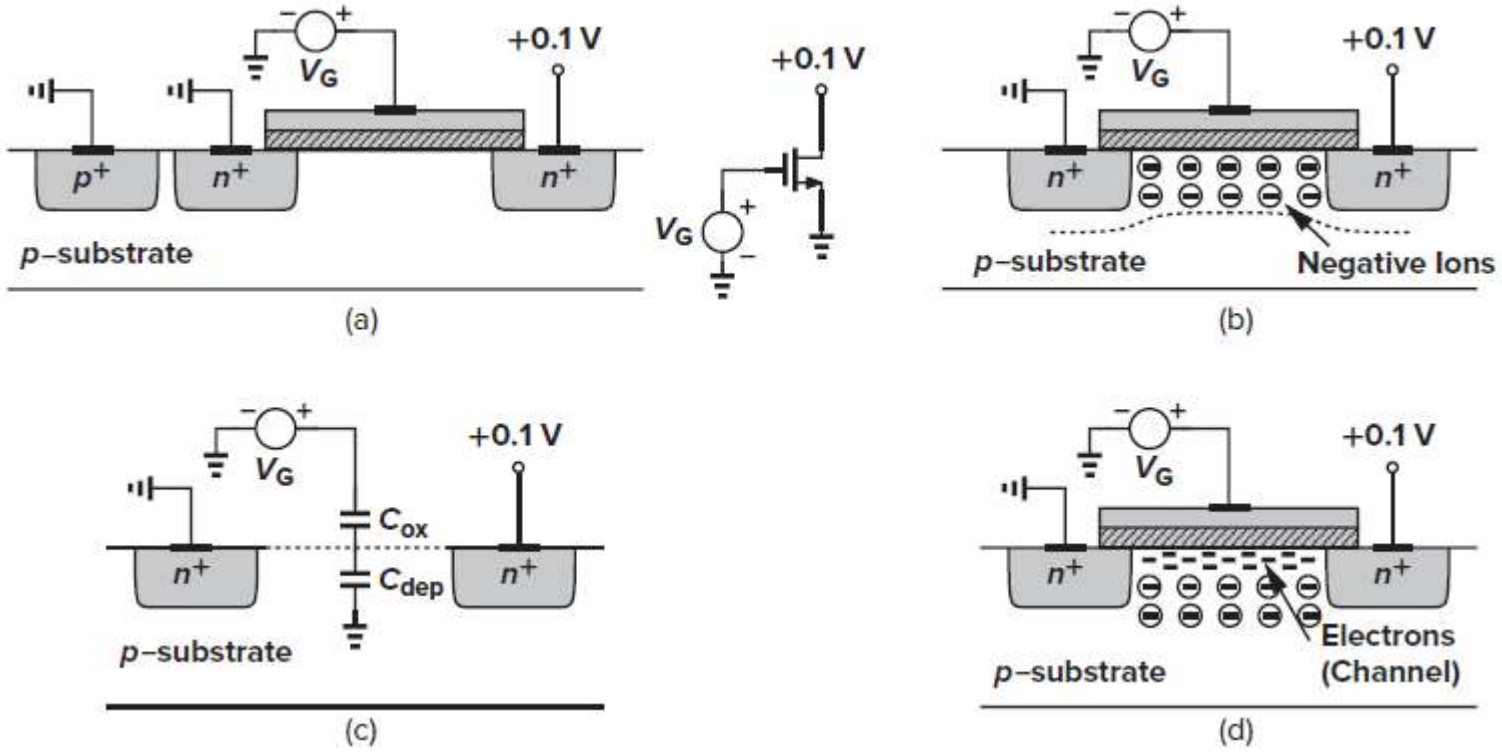
Plan view image of Samsung 14 nm FinFET transistors (Source: *Samsung 14 nm Exynos 7 7420 Logic Detailed Structural Analysis*, TechInsights)

MOSFET Control



V_{GS} VS. V_{DS}

A MOSFET Driven by a Gate Voltage



V_{GS} varies from zero to a high voltage:

(a) Off region ($V_{GS} = 0$)

(b) Subthreshold region ($V_{GS} < V_{TH}$)

(c) Neutralization point ($V_{GS} = V_{TH}$)

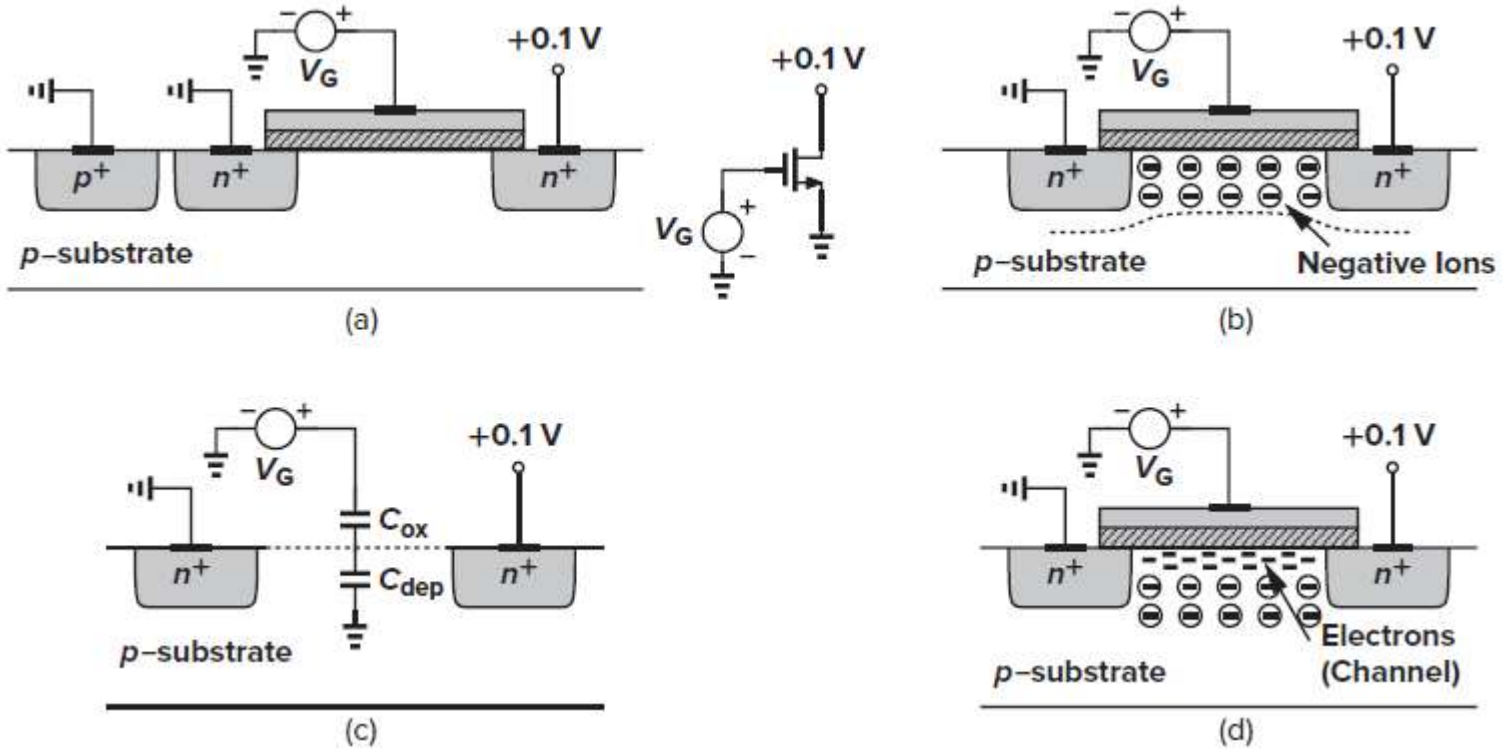
(d) Strong Inversion region ($V_{GS} > V_{TH}$ +200mV)

$$V_{TH} = \Phi_{MS} + 2\Phi_F + \frac{Q_{dep}}{C_{ox}}$$

$$\Phi_F = (kT/q)\ln(N_{sub}/n_i)$$

$$Q_{dep} = \sqrt{4q\epsilon_{si}|\Phi_F|N_{sub}}$$

A MOSFET Driven by a Gate Voltage

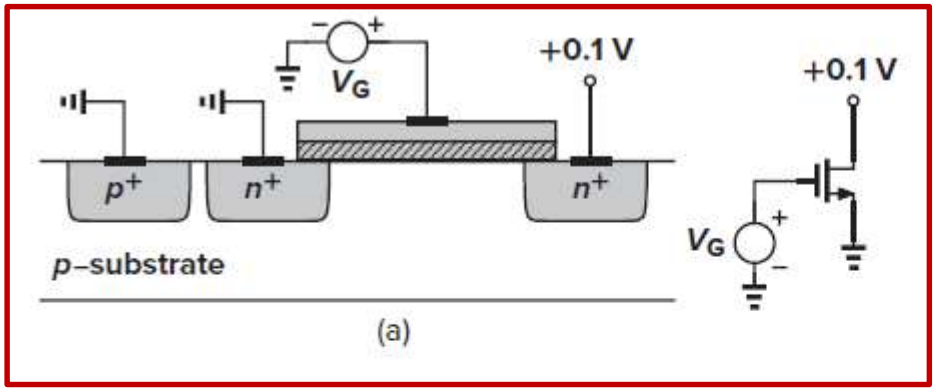


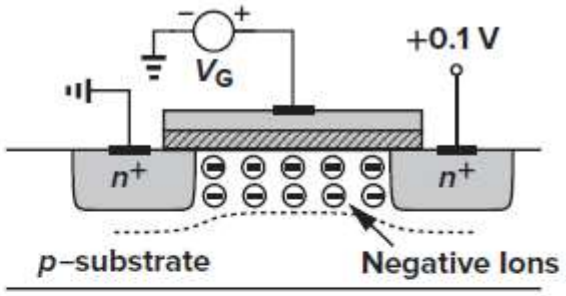
Description in textbook,

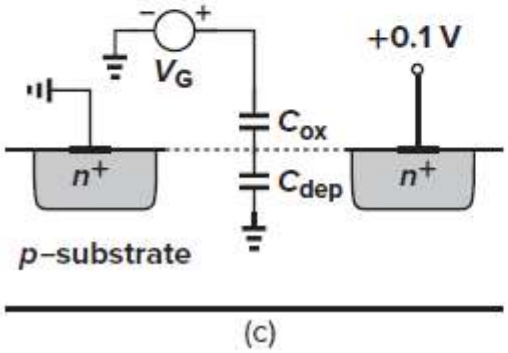
$$V_{TH} = \Phi_{MS} + 2\Phi_F + \frac{Q_{dep}}{C_{ox}}$$

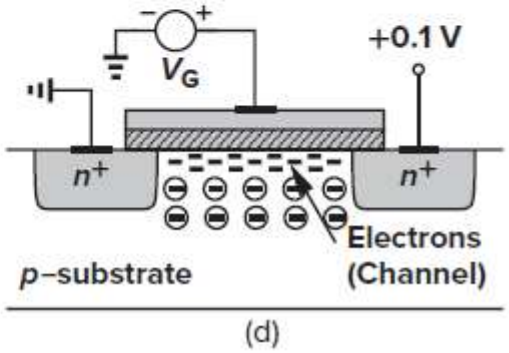
where Φ_{MS} is the difference between the work functions of the polysilicon gate and the silicon substrate, $\Phi_F = (kT/q)\ln(N_{sub}/n_i)$, k is Boltzmann's constant, q is the electron charge, N_{sub} is the doping density of the substrate, n_i is the density of electrons in undoped silicon, Q_{dep} is the charge in the depletion region, and C_{ox} is the gate-oxide capacitance per unit area. From pn junction theory, $Q_{dep} = \sqrt{4q\epsilon_{si}|\Phi_F|N_{sub}}$,

MOSFET in "OFF" Region









V_{GS} is much less than V_{TH}:

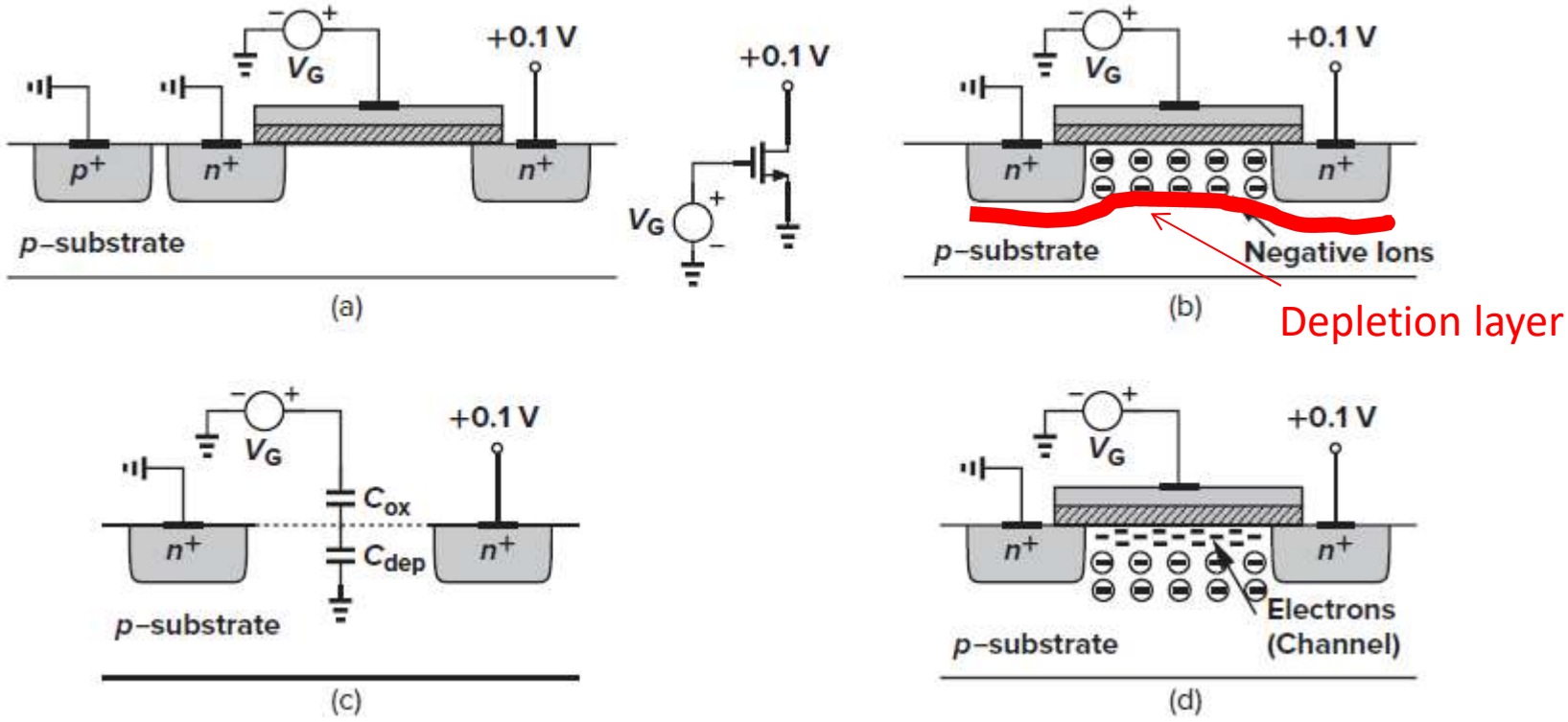
- Some negative ions in channel region
- There is no active charges from source to drain
- The MOSFET can be seen disabled
- But, it is not really inactive => leakage issue

$$V_{TH} = \Phi_{MS} + 2\Phi_F + \frac{Q_{dep}}{C_{ox}}$$

$$\Phi_F = (kT/q)\ln(N_{sub}/n_i)$$

$$Q_{dep} = \sqrt{4q\epsilon_{si}|\Phi_F|N_{sub}}$$

MOSFET in "Subthreshold" Region



V_{GS} is approaching to V_{TH} (from zero voltage):

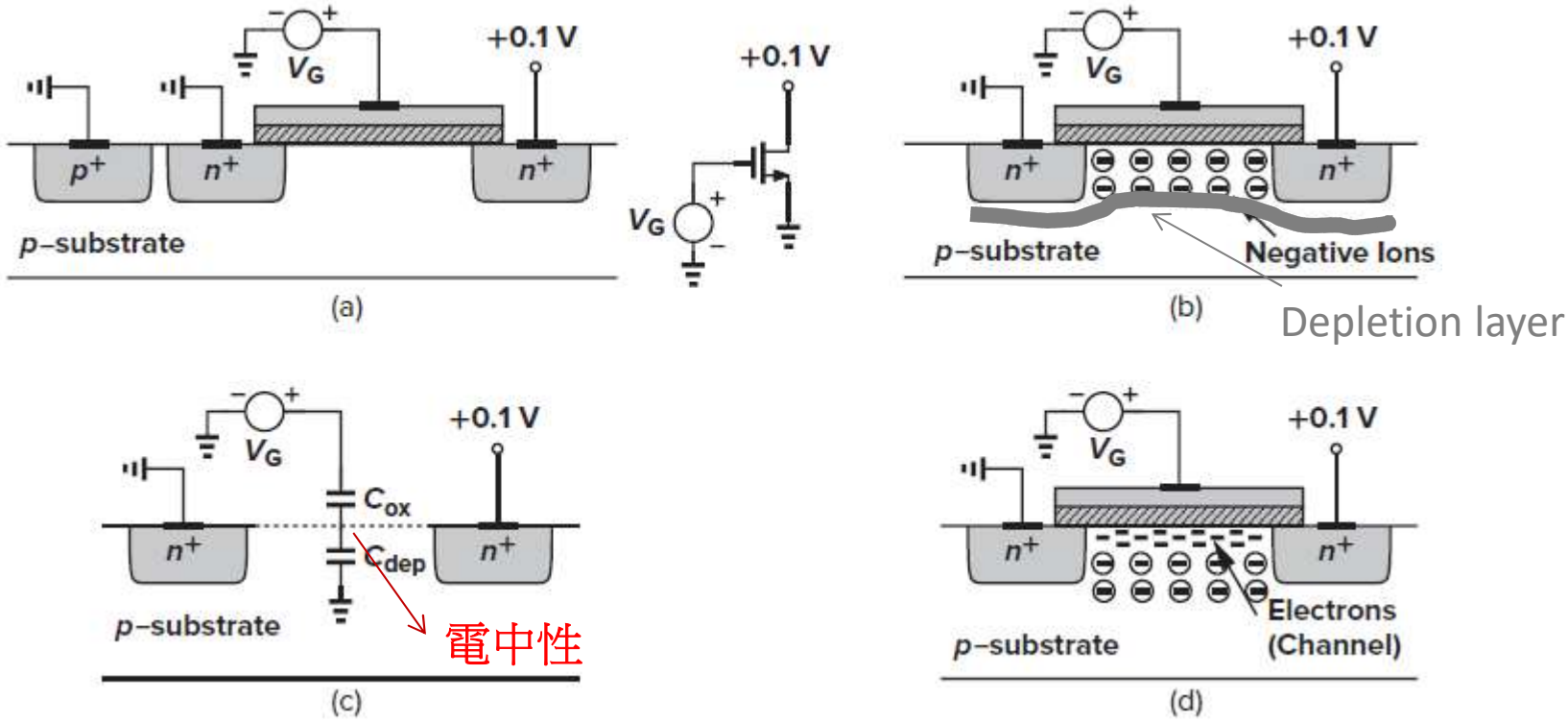
- The "mobile" charges are negative ions, not electrons
- These negative ions are contributed from the p-substrate and attracted by a positive gate voltage

$$V_{TH} = \Phi_{MS} + 2\Phi_F + \frac{Q_{dep}}{C_{ox}}$$

$$\Phi_F = (kT/q)\ln(N_{sub}/n_i)$$

$$Q_{dep} = \sqrt{4q\epsilon_{si}|\Phi_F|N_{sub}}$$

MOSFET at "Neutralization" State



V_{GS} is equal to V_{TH}:

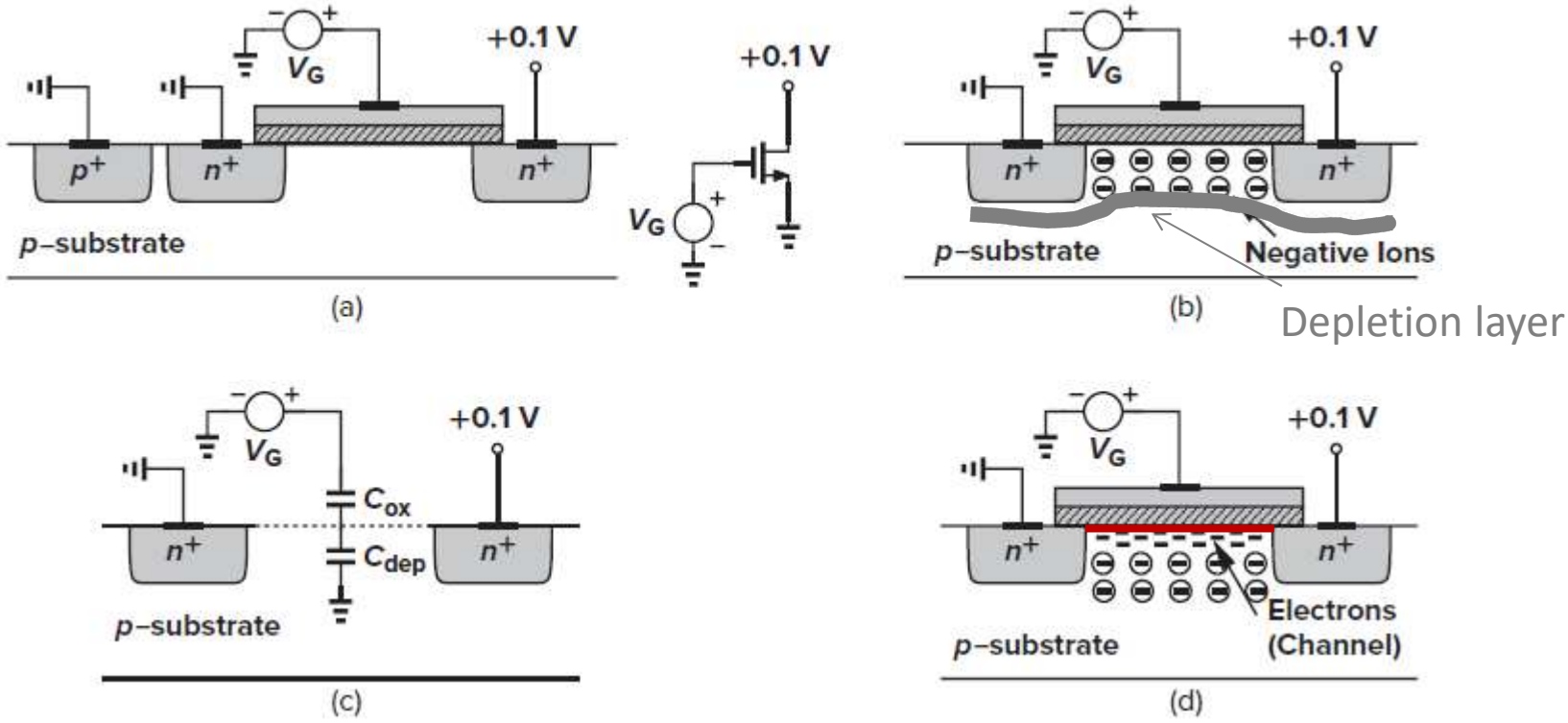
- The attracted negative ions are equal to the majority carriers (positive ions). It means $V_{GS} = V_{TH}$
- Now, the position below gate oxide is floating => up is a Cox and down is a Cdep => C_{GB} = ?

$$V_{TH} = \Phi_{MS} + 2\Phi_F + \frac{Q_{dep}}{C_{ox}}$$

$$\Phi_F = (kT/q)\ln(N_{sub}/n_i)$$

$$Q_{dep} = \sqrt{4q\epsilon_{si}|\Phi_F|N_{sub}}$$

MOSFET in "Strong Inversion" Region



V_{GS} is larger than V_{TH} by a certain voltage:

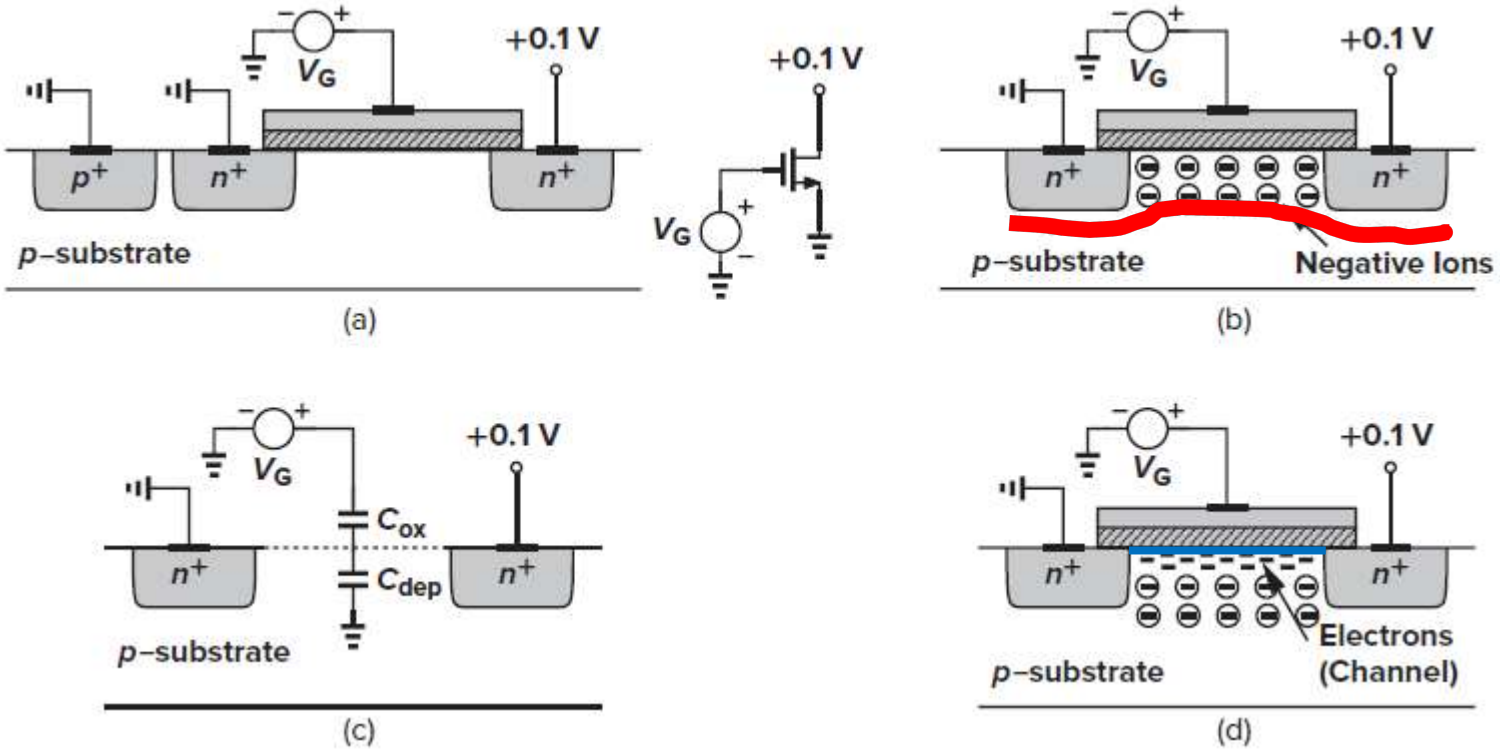
- The mobile charges are electrons, moved from source to drain. The conduction path is called "inversion channel".
- Inversion means the charges on the channel are "positive => negative"

$$V_{TH} = \Phi_{MS} + 2\Phi_F + \frac{Q_{dep}}{C_{ox}}$$

$$\Phi_F = (kT/q)\ln(N_{sub}/n_i)$$

$$Q_{dep} = \sqrt{4q\epsilon_{si}|\Phi_F|N_{sub}}$$

MOSFET Summary by V_{GS}



- t_{ox}=20Å to get C_{ox}~17.25fF/μm^2
- Native device (V_{TH} ~ 0), how?
  - Adjusting the doping (***N_{sub}***) to change V_{TH}

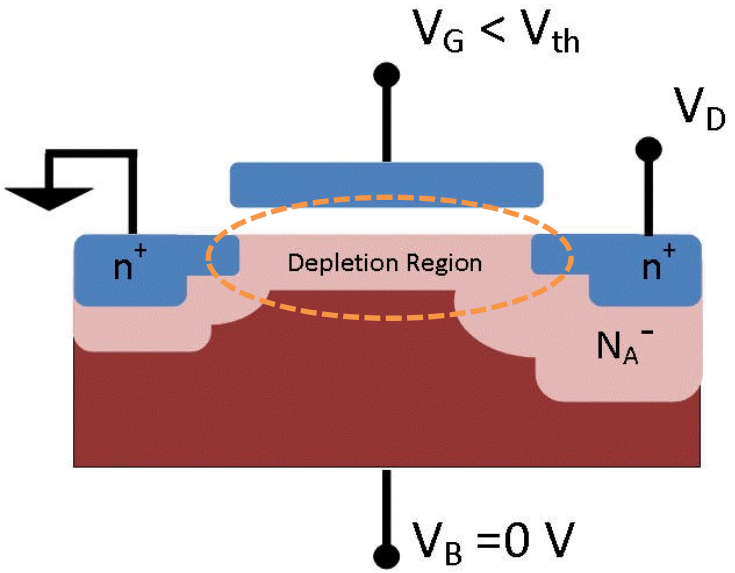
$$V_{TH} = \Phi_{MS} + 2\Phi_F + \frac{Q_{dep}}{C_{ox}}$$

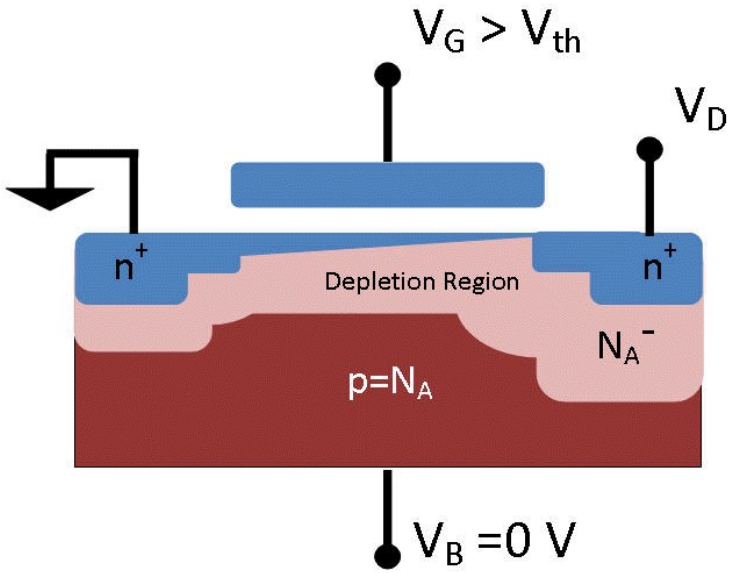
$$\Phi_F = (kT/q)\ln(N_{sub}/n_i)$$

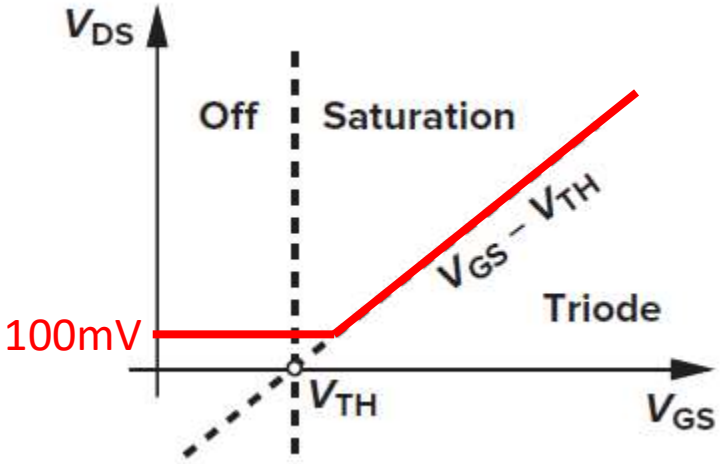
$$Q_{dep} = \sqrt{4q\epsilon_{si}|\Phi_F|N_{sub}}$$

- PMOS have similar phenomenon but majority carrier is "**hole**"

MOSFET Summary by V_{GS}





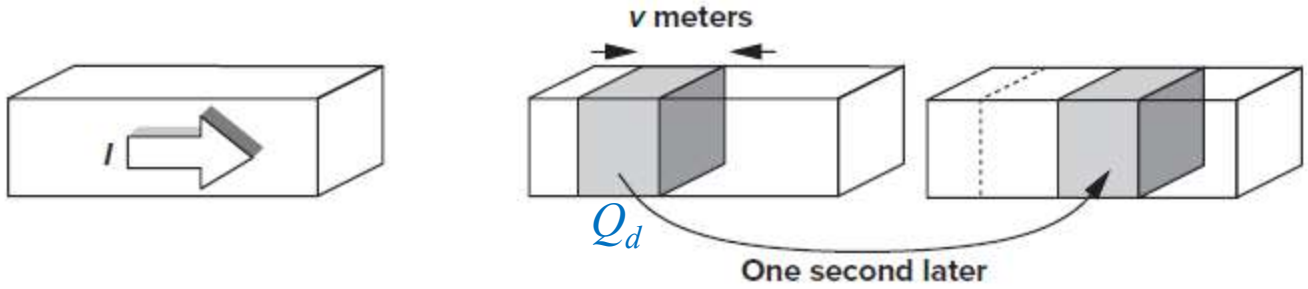


While we ask "the MOSFET is at strong or weak inversion (or OFF) mode", it means **V_{GS}** is large or small

While we ask "the MOSFET is triode or saturation region", it means **V_{DS}** is large enough or not?

MOSFET: Drain Current

Channel Charge Model in triode region



Drift Velocity

$$v = \mu E$$

$$E(x) = -dV/dx$$

$$I = Q_d \cdot v$$

$$Q_d = WC_{ox}(V_{GS} - V_{TH})$$

$$Q_d(x) = WC_{ox}[V_{GS} - V(x) - V_{TH}]$$

where x: 0-L

$$I_D = -WC_{ox}[V_{GS} - V(x) - V_{TH}]v$$

$$I_D = WC_{ox}[V_{GS} - V(x) - V_{TH}]\mu_n \frac{dV(x)}{dx}$$

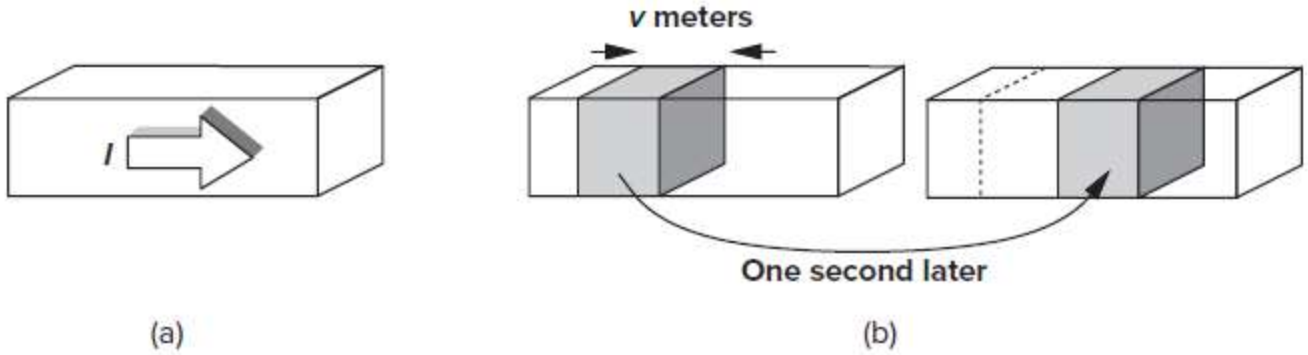
$$\int_{x=0}^{L} I_D dx = \int_{V=0}^{V_{DS}} WC_{ox}\mu_n[V_{GS} - V(x) - V_{TH}]dV$$

$$I_D = \mu_n C_{ox}\frac{W}{L}\left[(V_{GS} - V_{TH})V_{DS} - \frac{1}{2}V_{DS}^2\right]$$

Note:
Q_d: 線電荷 (Q/L)

MOSFET: Drain Current

Channel Charge Model in triode region



Drift Velocity

$$v = \mu E$$

$$E(x) = -dV/dx$$

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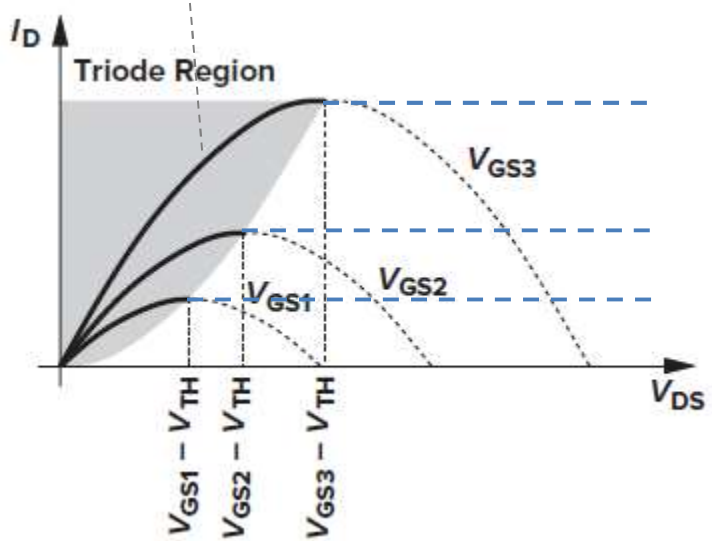


This current conduction is true before **pinch-off effect** occurs!!

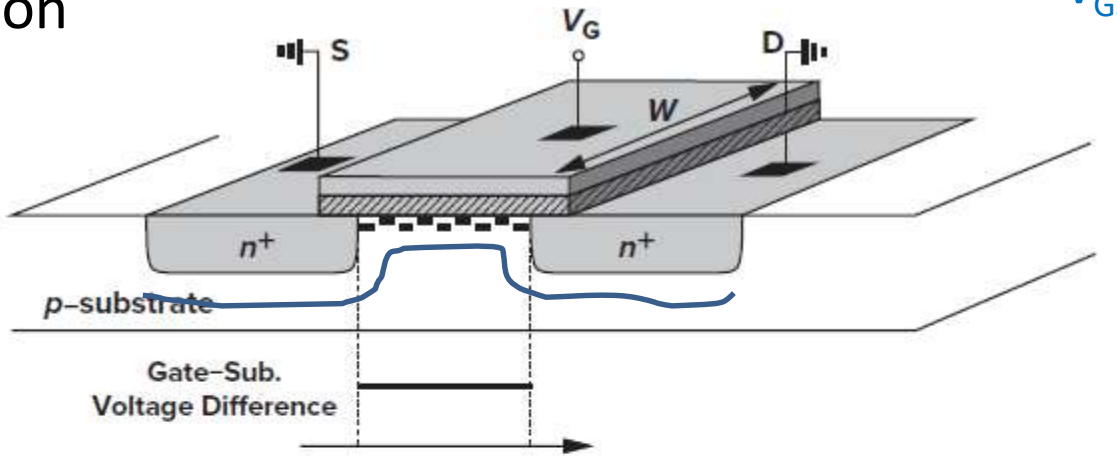
$$V_{DS} = V_{GS} - V_{TH}$$

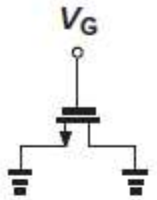
$$I_{D,max} = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH})^2$$

Channel Charge vs. V_{DS}

Triode region

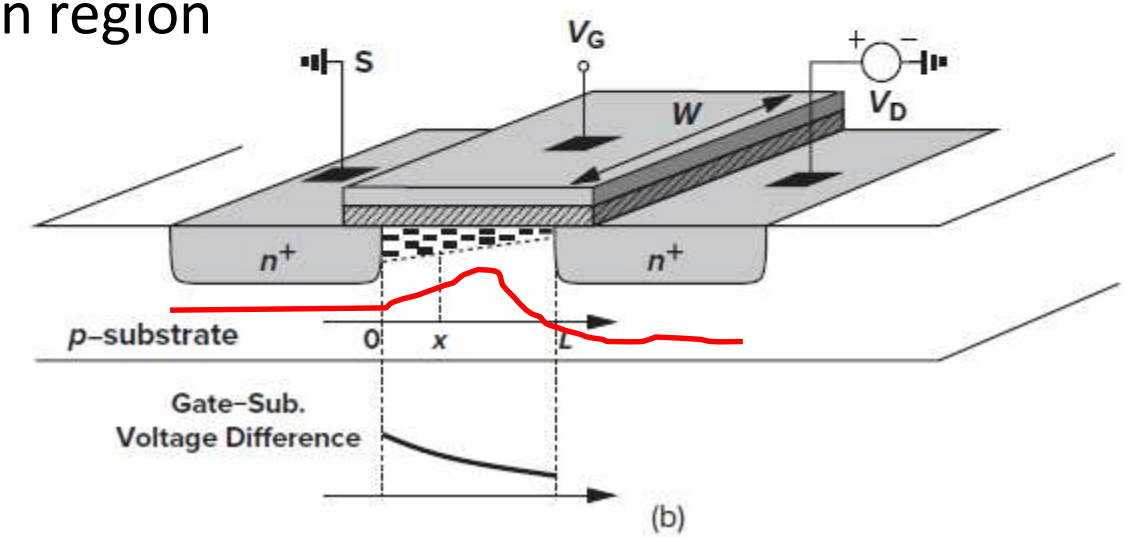
V_{GS} is constant

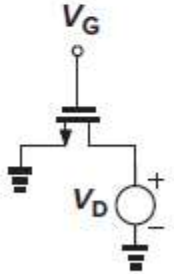




(a)

Saturation region

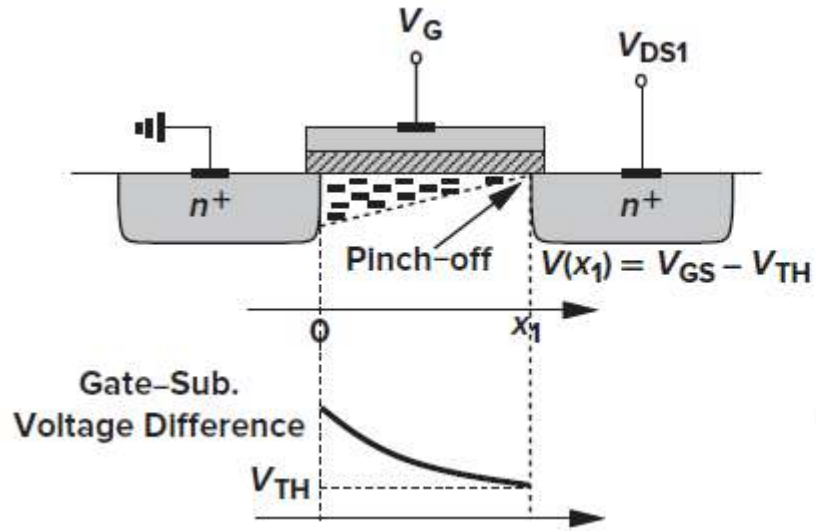


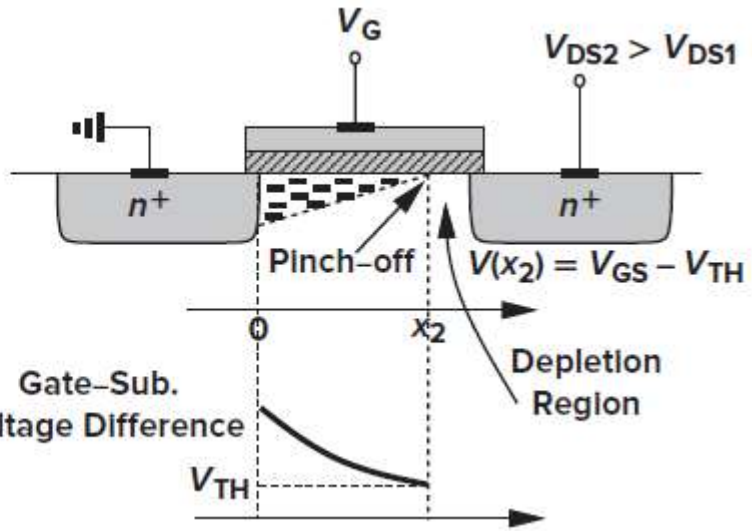


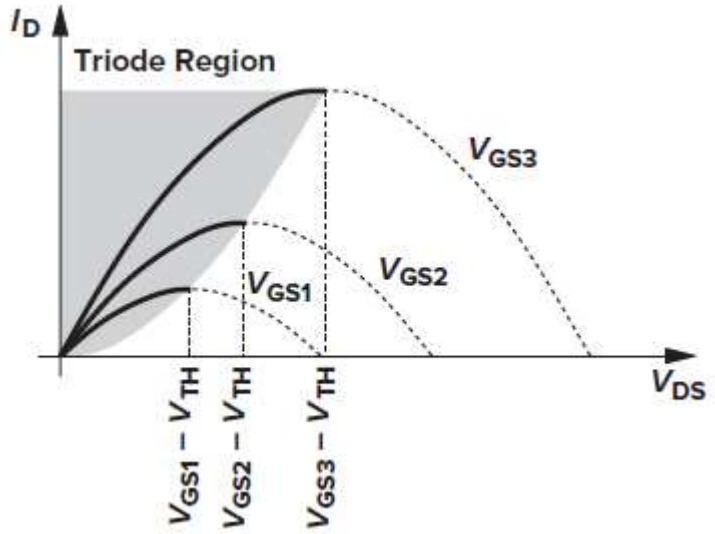
(b)

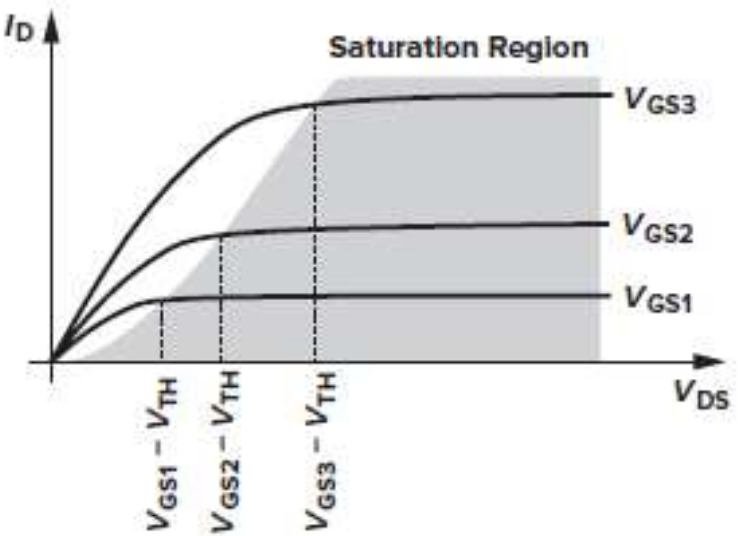
$V_{DS}=V_{GS}-V_{TH}$

Pinch-off Behavior

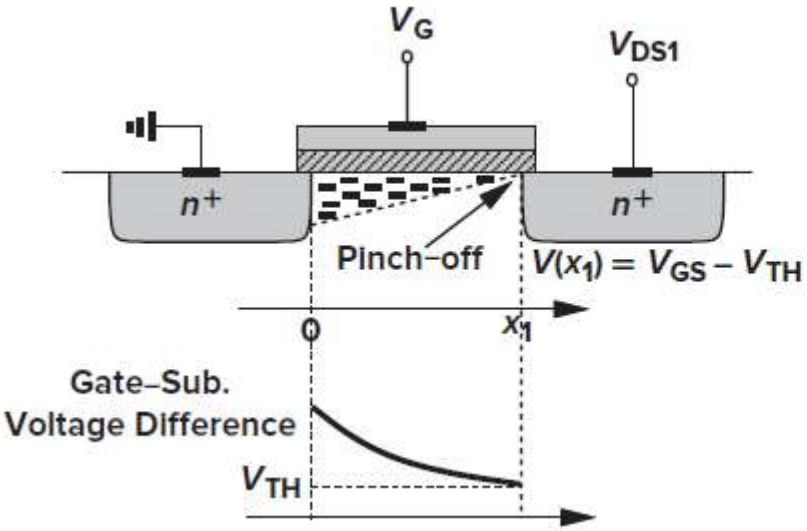


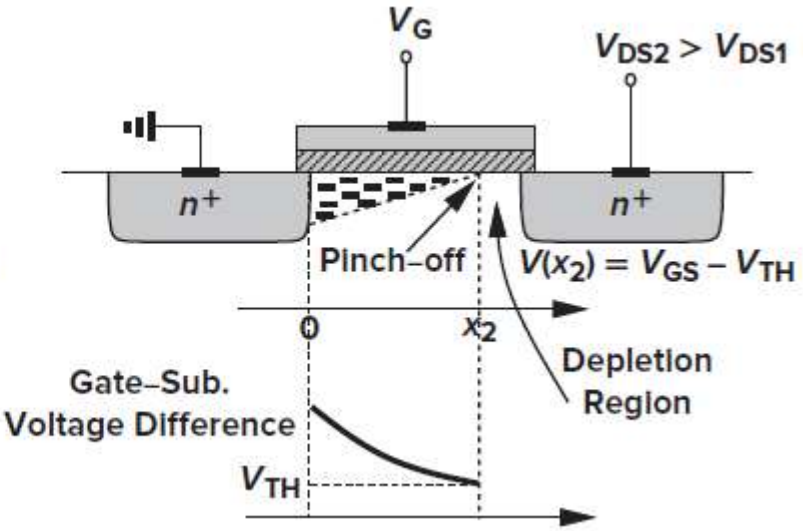






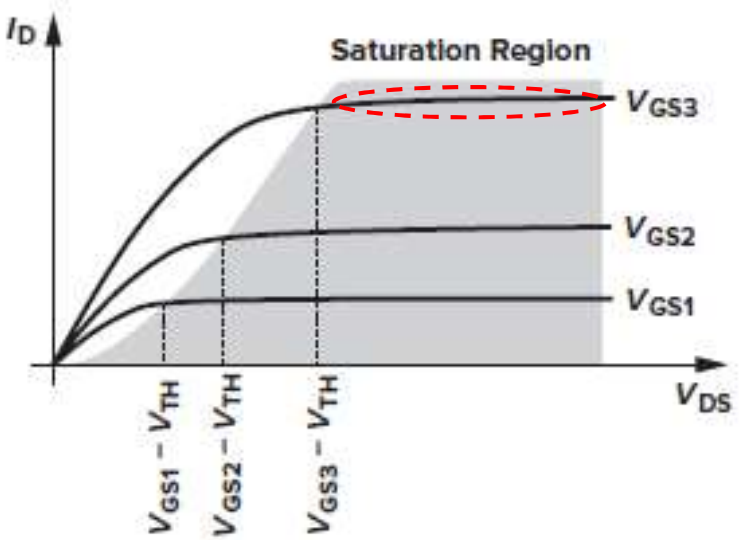
Pinch-off Behavior





$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L'}(V_{GS} - V_{TH})^2$$

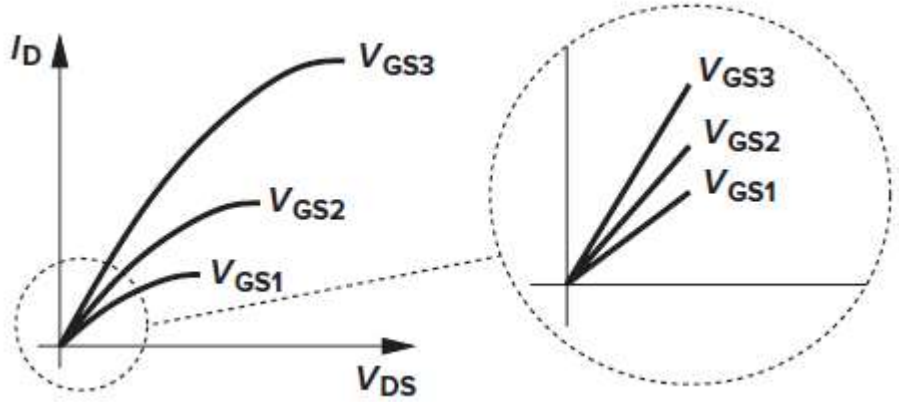
Channel Length Modulation



MOSFET as a Resistor

Deep Triode Region

$$I_D = \mu_n C_{ox} \frac{W}{L} \left[(V_{GS} - V_{TH}) V_{DS} - \frac{1}{2} V_{DS}^2 \right]$$



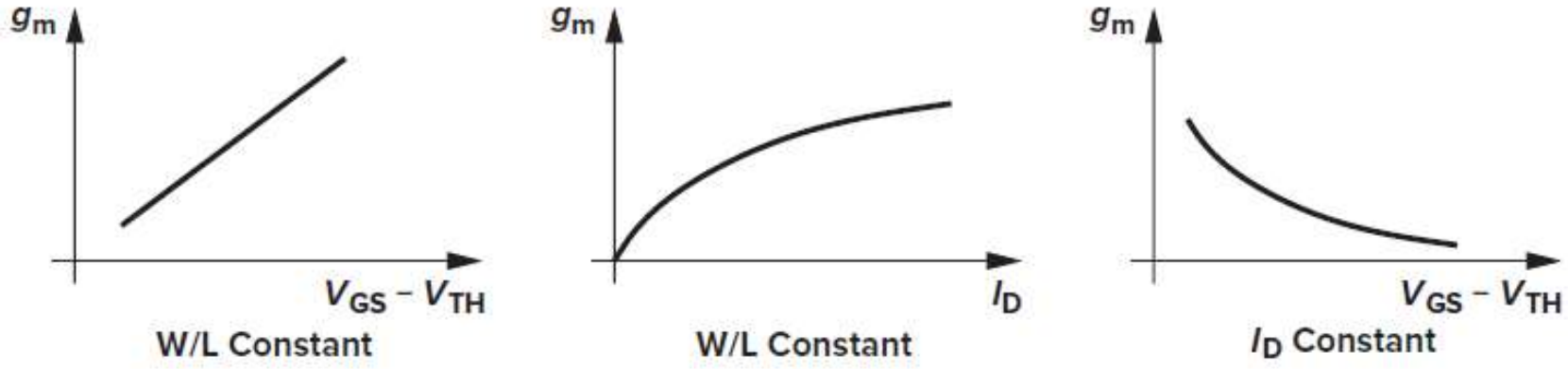
$$I_D \approx \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH}) V_{DS}$$

$$R_{on} = \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})}$$

A voltage-controlled resistor

MOSFET as an Amplifier

g_m Representation



$$g_m = \left.\frac{\partial I_D}{\partial V_{GS}}\right|_{VDS\ \text{const.}} = \mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})$$

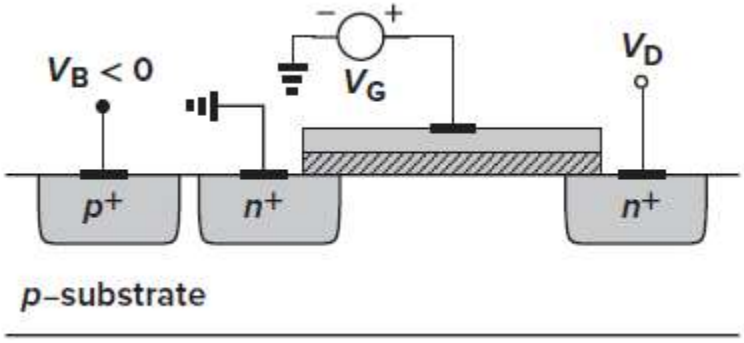
$$g_m = \sqrt{2\mu_n C_{ox}\frac{W}{L} I_D} = \frac{2I_D}{V_{GS} - V_{TH}}$$

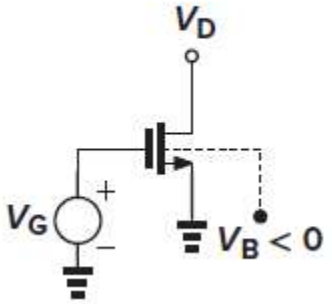
MOSFET: Second-Order Effects

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2(1 + \lambda V_{DS})$$

- **Body Effect**
  - $V_{TH} \sim f(V_{SB})$
- **Channel-Length Modulation**
  - $r_o \sim f(L, V_{DS})$
- **Subthreshold Conduction**
  - $V_{GS} \sim V_{TH}$
- **Voltage Limitation**
  - High V_{DD}

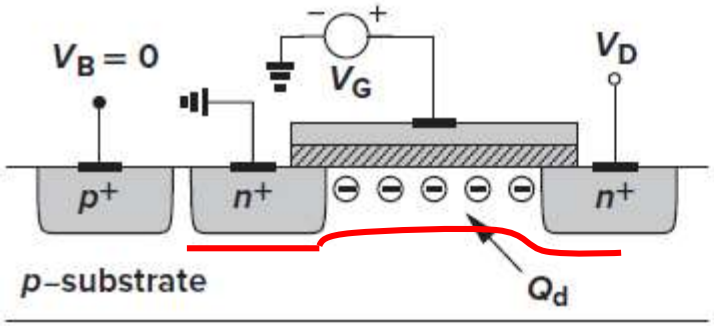
Body Effect (1)

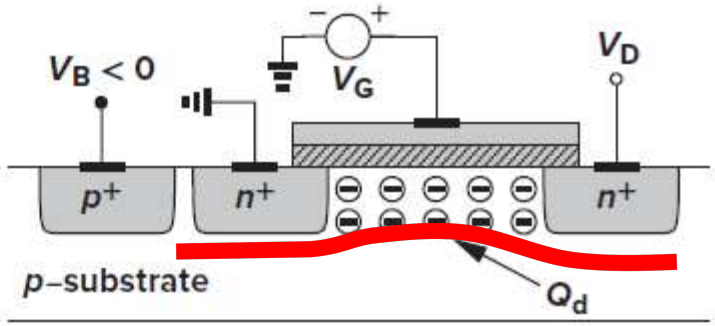




$V_{SB} > 0$

$V_{SB} \neq 0$





Note:

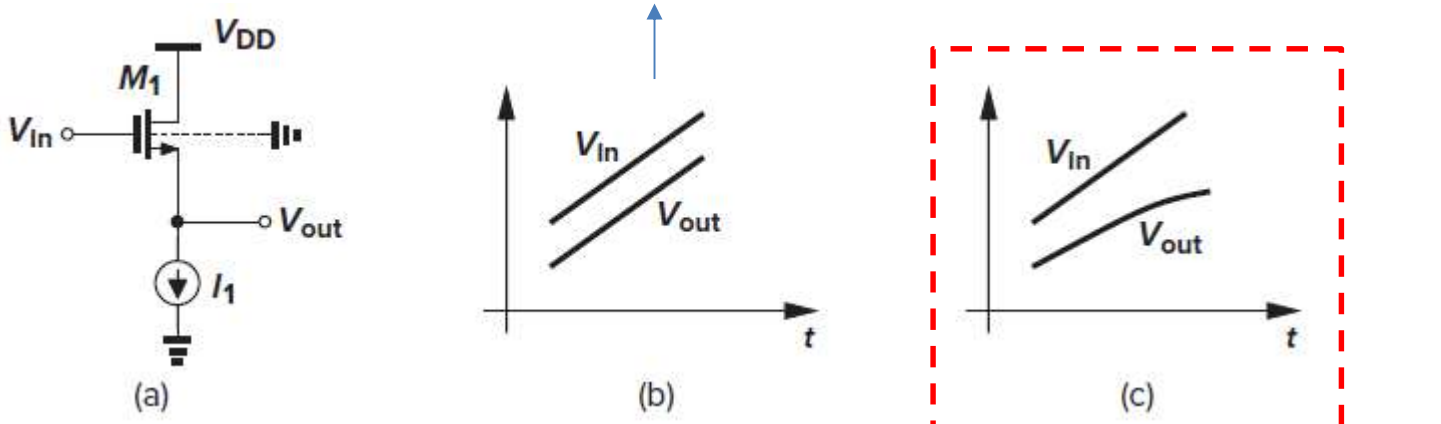
$C_{ox} = C_{gate}/WL$

$$V_{TH} = V_{TH0} + \gamma\left(\sqrt{2\Phi_F + V_{SB}} - \sqrt{|2\Phi_F|}\right)$$

$$\gamma = \sqrt{2q\epsilon_{si}N_{sub}}/C_{ox}$$ (γ = 0.3 ~ 0.4, by process)

Body Effect (2)

An ideal voltage follower: Vin-Vout=constant

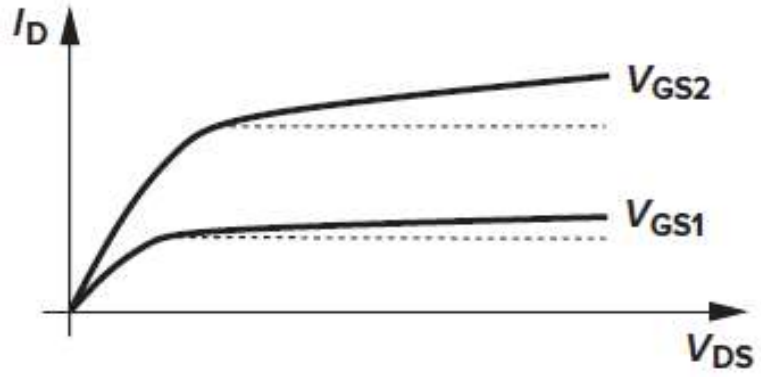


Nonideal voltage follower

$$I_1 = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{in} - V_{out} - V_{TH})^2$$

We may conclude that the body effect causes a nonlinear error (distortion) in this nMOST source follower

Channel-Length Modulation



$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L'}(V_{GS}-V_{TH})^2$$

$$L' = L - \Delta L \text{ (pinch-off effect)}$$

$$\frac{1}{L'} = \frac{1}{L-\Delta L} = \frac{1}{L}\cdot\frac{1}{1-\Delta L/L} \sim \frac{1}{L}\left(1+\frac{\Delta L}{L}\right)$$

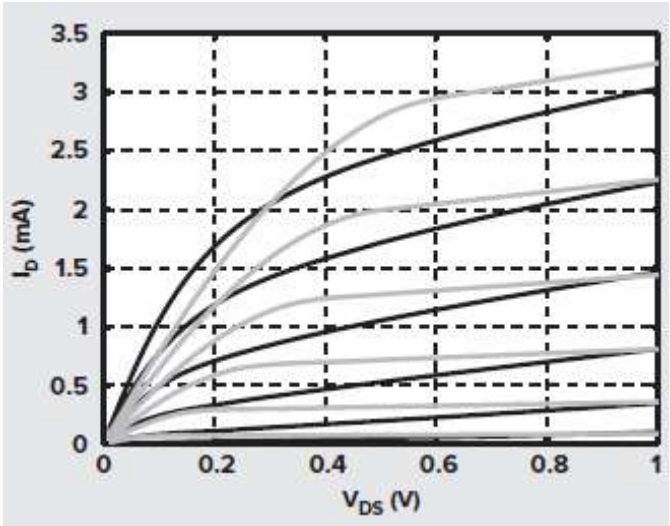
$\Delta L/L$與V_{DS}有關

$$I_D \sim \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{TH})^2(1+\lambda V_{DS})$$

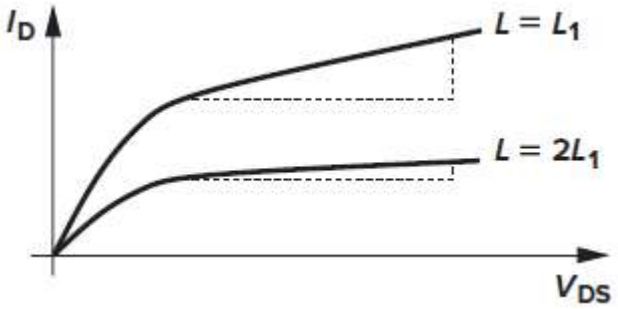
$$g_m = \mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{TH})(1+\lambda V_{DS})$$

$$= \sqrt{2\mu_n C_{ox}(W/L)I_D(1+\lambda V_{DS})}$$

nanometer NMOS Transistors



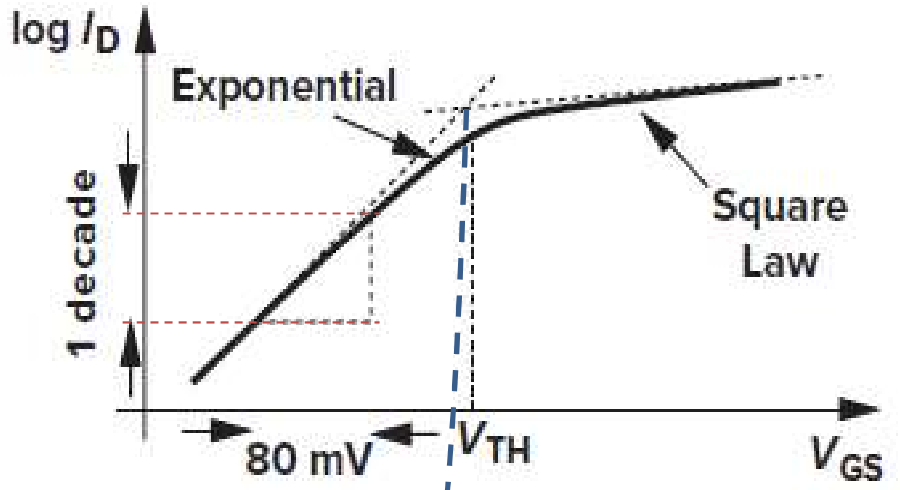
an NFET with $W/L = 5\ \mu$m/40 nm for $V_{GS} = 0.3$ V $\cdots$ 0.8 V.

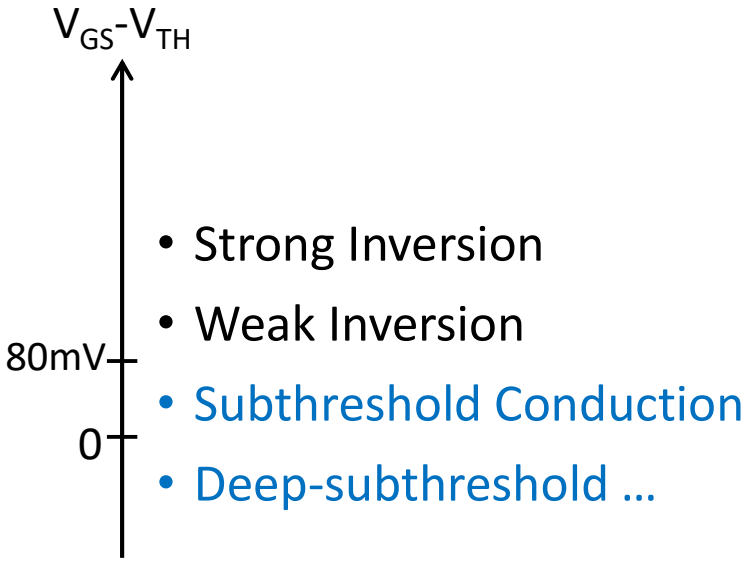


Example (2.7)

Subthreshold Conduction

$I_D = 0$ if $V_{GS} < V_{TH}$? The answer is not!!





Subthreshold Current Model (by Foundry Device Model)

$$I_D = I_0 e^{\frac{V_{GS}}{\xi V_T}}$$

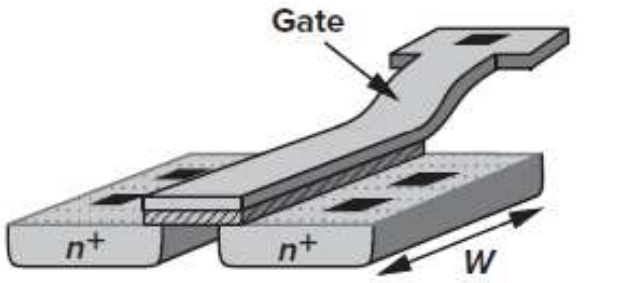
$$\frac{I_D}{\xi V_T} = \frac{2I_D}{V_{GS} - V_{TH}}$$

$$V_{GS} - V_{TH} = 2\xi V_T \sim 80 \text{ mV (@27°C)}$$

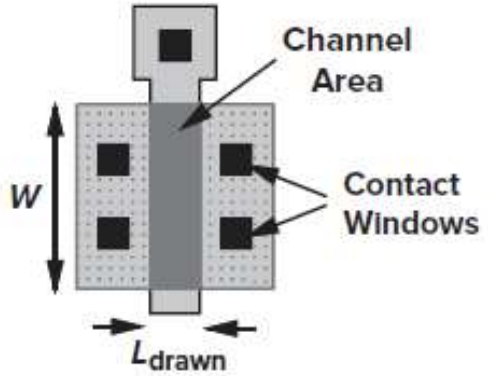
$\xi \sim 1.5$ => Subthreshold boundary

Ξξ Xi

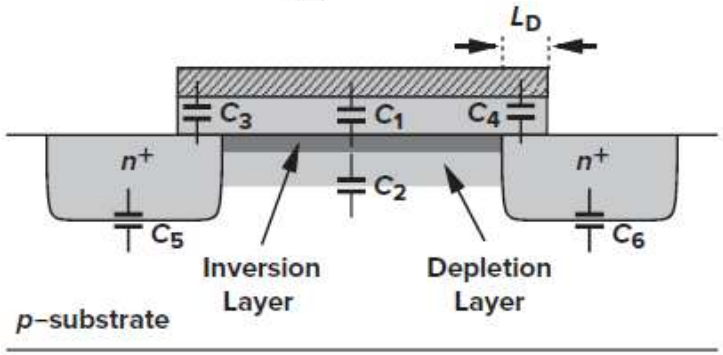
MOS Capacitor Model



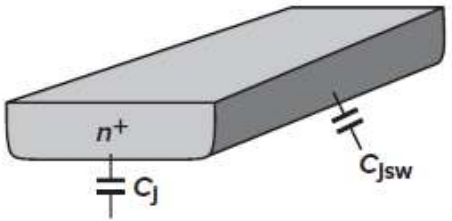
(a)



(b)



(a)



(b)

空乏電容

平板電容

$$C_1 = WLC_{ox}$$

$$C_2 = WL\sqrt{q\varepsilon_{si}N_{sub}/(4\phi_F)}$$

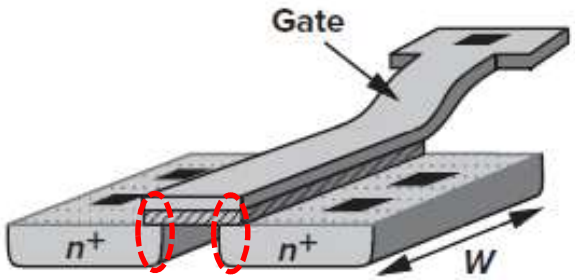
$$C_3 = C_4 = WL_D C_{ox} = WC_{ov}$$

$$C_j = C_{j0}/(1+V_R/\phi_B)^m$$

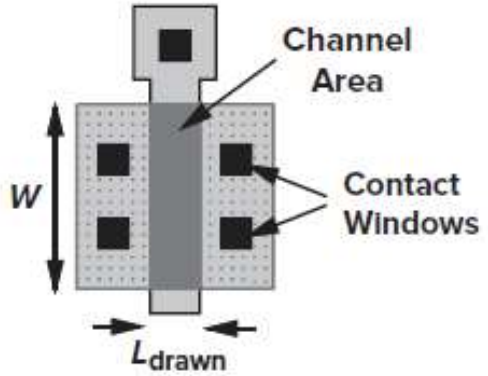
$$C_{jsw} = C_{jsw0}/(1+V_R/\phi_B)^m$$

$$m = 0.3 \sim 0.4$$

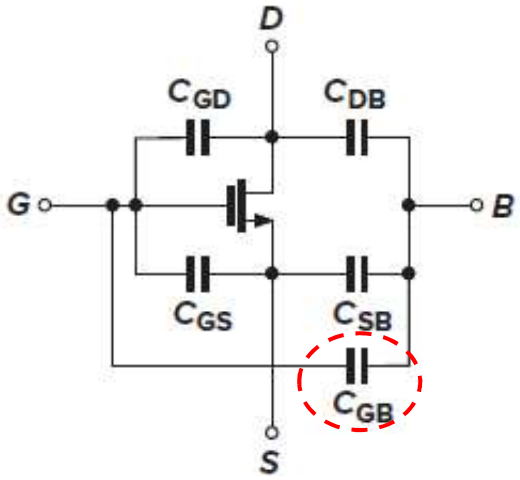
MOS Capacitor Model



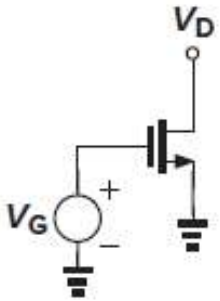
(a)

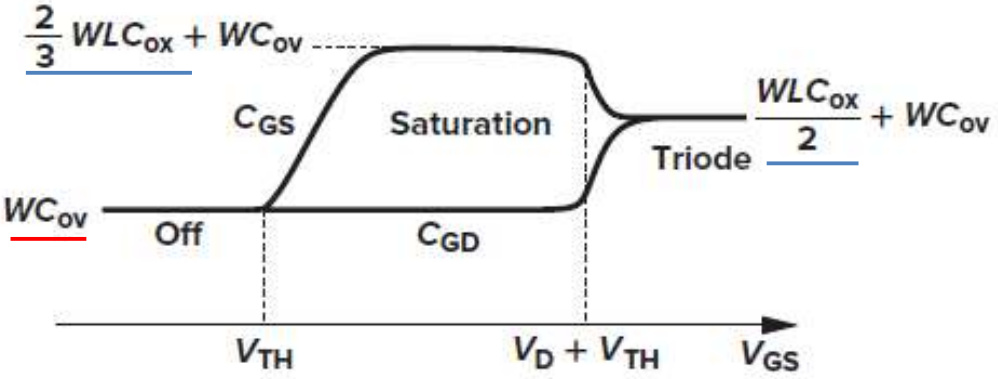


(b)

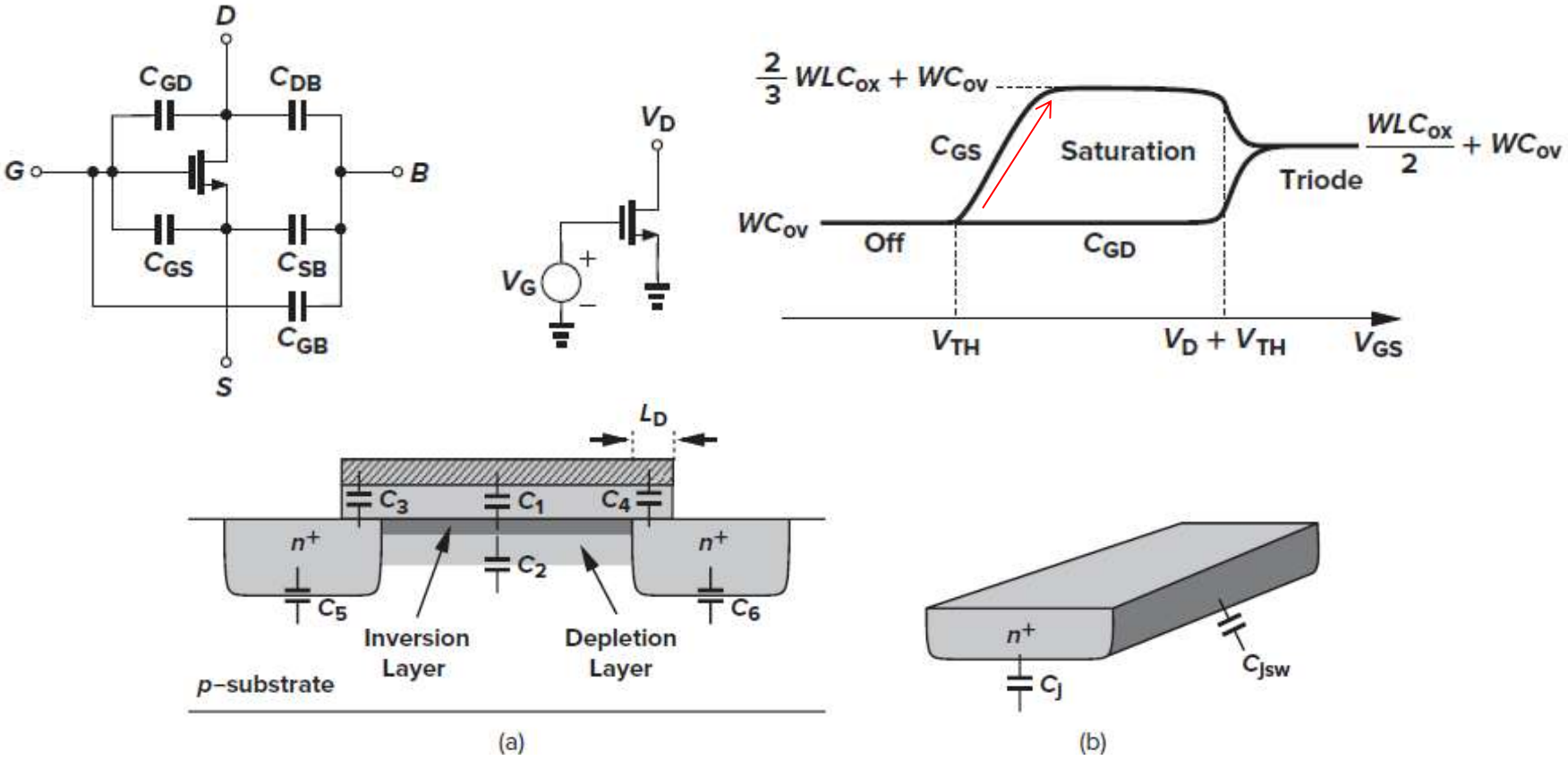


C_{GS} and C_{GD}





MOS Capacitor Model



$$C_1 = WLC_{ox}$$

$$C_2 = WL\sqrt{q\varepsilon_{si}N_{sub}/(4\varphi_F)}$$

$$C_3 = C_4 = WL_{\mathrm{D}}C_{ox} = WC_{ov}$$

$$C_j = C_{j0}/(1 + V_R/\varphi_B)^m$$

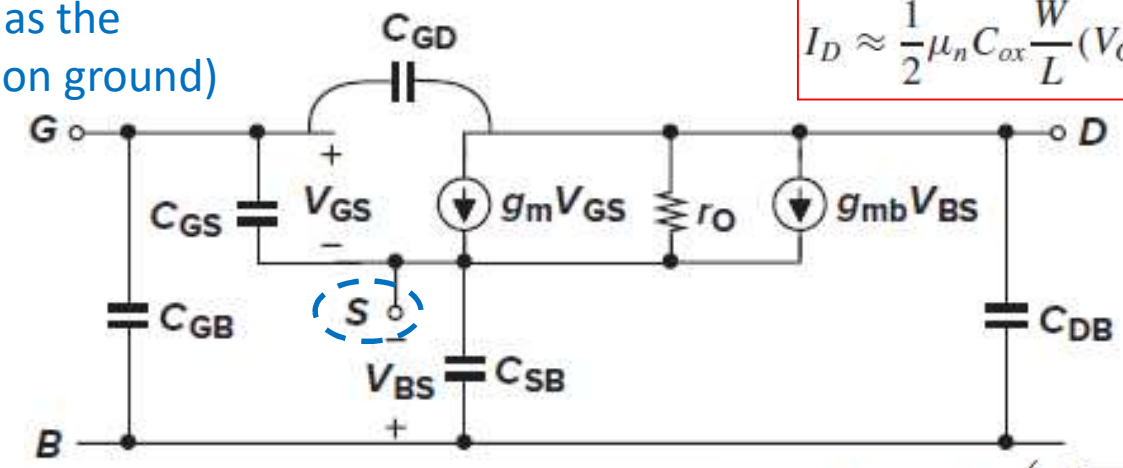
$$C_{jsw} = C_{jsw0}/(1 + V_R/\varphi_B)^m$$

$$m = 0.3\sim0.4$$

MOS Small-Signal Model

Use source node as the reference (common ground)

$$I_D \approx \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{TH})^2(1+\lambda V_{DS})$$



$$r_O = \frac{\partial V_{DS}}{\partial I_D}$$

$$= \frac{1}{\partial I_D/\partial V_{DS}}$$

$$= \frac{1}{\frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{TH})^2\cdot\lambda}$$

$$\approx \frac{1+\lambda V_{DS}}{\lambda I_D}$$

$$\approx \frac{1}{\lambda I_D}$$

$$V_{TH} = V_{TH0} + \gamma\left(\sqrt{2\Phi_F + V_{SB}} - \sqrt{|2\Phi_F|}\right)$$

$$g_{mb} = \frac{\partial I_D}{\partial V_{BS}}$$

$$= \mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{TH})\left(-\frac{\partial V_{TH}}{\partial V_{BS}}\right)$$

$$\frac{\partial V_{TH}}{\partial V_{BS}} = -\frac{\partial V_{TH}}{\partial V_{SB}}$$

$$= -\frac{\gamma}{2}(2\Phi_F + V_{SB})^{-1/2}$$

$$g_{mb} = g_m\frac{\gamma}{2\sqrt{2\Phi_F + V_{SB}}}$$

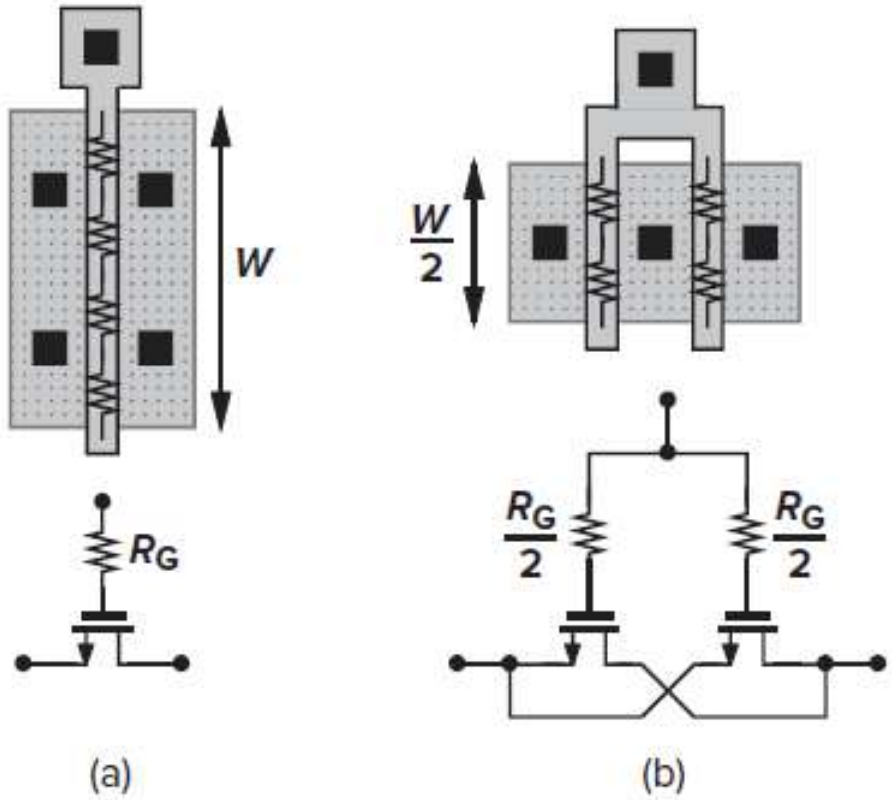
$$= \eta g_m$$

(That's why we call the back-gate effect)

Reduction of gate resistance

Folding structure to reduce the gate resistance

$R_G \propto W/L$



- The resistance on drain and source can be reduced by the same concept!!
- Don't use too wide transistors. For example, W=20u, L=0.2u
- Using multiplier (m) or finger (nf) to implement a wide transistor

SPICE Models

NMOS Model			
LEVEL = 1	VTO = 0.7	GAMMA = 0.45	PHI = 0.9
NSUB = 9e+14	LD = 0.08e−6	UO = 350	LAMBDA = 0.1
TOX = 9e−9	PB = 0.9	CJ = 0.56e−3	CJSW = 0.35e−11
MJ = 0.45	MJSW = 0.2	CGDO = 0.4e−9	JS = 1.0e−8
PMOS Model			
LEVEL = 1	VTO = −0.8	GAMMA = 0.4	PHI = 0.8
NSUB = 5e+14	LD = 0.09e−6	UO = 100	LAMBDA = 0.2
TOX = 9e−9	PB = 0.9	CJ = 0.94e−3	CJSW = 0.32e−11
MJ = 0.5	MJSW = 0.3	CGDO = 0.3e−9	JS = 0.5e−8

$$\gamma = \sqrt{2q\epsilon_{si}N_{sub}}/C_{ox}$$

$$C_{ox} = \varepsilon_{ox}/t_{ox}$$

$$C_j = C_{j0}/\left(1+V_R/\phi_B\right)^m$$

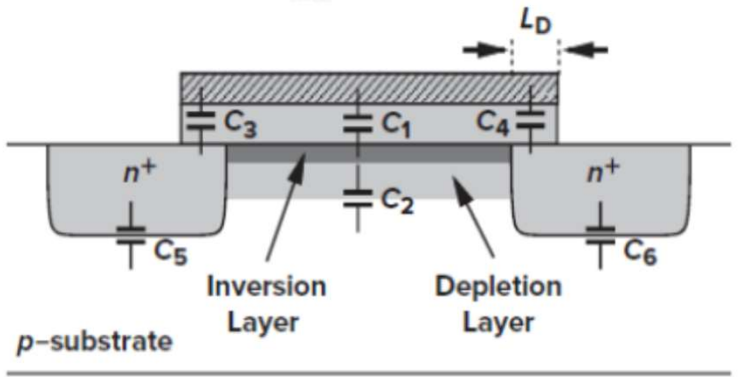
$$C_{jsw} = C_{jsw0}/\left(1+V_R/\phi_B\right)^m$$

$$m = 0.3 \sim 0.4$$

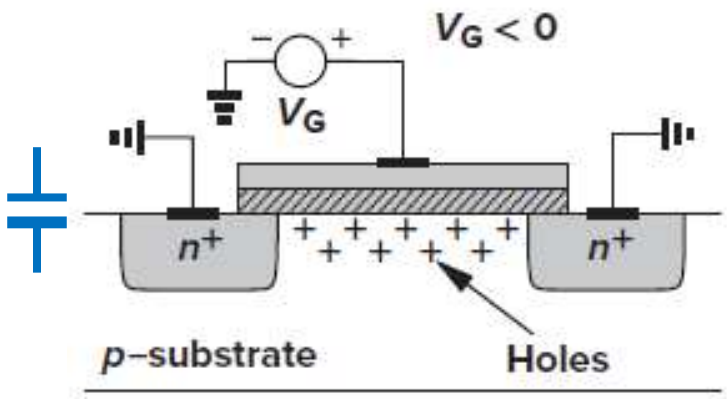
VTO: threshold voltage with zero V_{SB} (unit: V)
GAMMA: body-effect coefficient (unit: $V^{1/2}$)
PHI: $2\Phi_F$ (unit: V)
TOX: gate-oxide thickness (unit: m)
NSUB: substrate doping (unit: cm^{-3})
LD: source/drain side diffusion (unit: m)
UO: channel mobility (unit: $cm^2/V/s$)
LAMBDA: channel-length modulation coefficient (unit: V^{-1})
CJ: source/drain bottom-plate junction capacitance per unit area (unit: F/m^2)
CJSW: source/drain sidewall junction capacitance per unit length (unit: F/m)
PB: source/drain junction built-in potential (unit: V)
MJ: exponent in CJ equation (unitless)
MJSW: exponent in CJSW equation (unitless)
CGDO: gate-drain overlap capacitance per unit width (unit: F/m)
CGSO: gate-source overlap capacitance per unit width (unit: F/m)
JS: source/drain leakage current per unit area (unit: A/m^2)

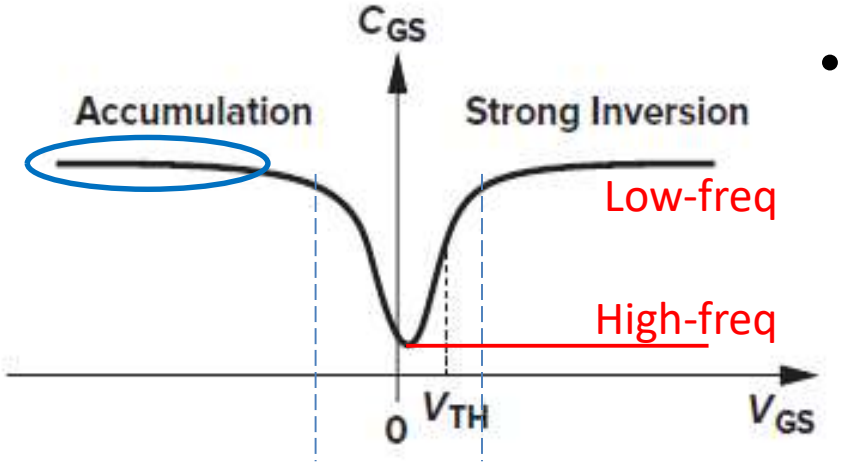
$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{TH})^2(1+\lambda V_{DS})$$

$$V_{TH} = V_{TH0} + \gamma\left(\sqrt{2\Phi_F + V_{SB}} - \sqrt{|2\Phi_F|}\right)$$



MOSFET as a Capacitor





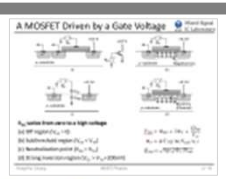
Depletion cap included

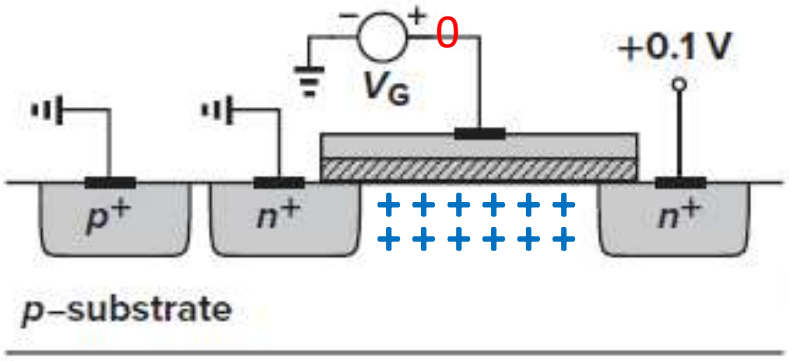
- **Accumulation** mode
  - Hole concentration is increased if V_{GS} is more negative (plate is formed by a hole layer)
- **Depletion** mode
  - Hole concentration is decreased and electron concentration is increased if V_{GS} is from negative to positive (acts like a floating point)
- **Inversion** mode
  - Inversion layer is formed to act as a plate. For high-frequency gate variations, layer is not formed in time (>1MHz); for low-freq gate variation, layer is always formed (<100Hz)

Non-Quasi Static (NQS) Effect

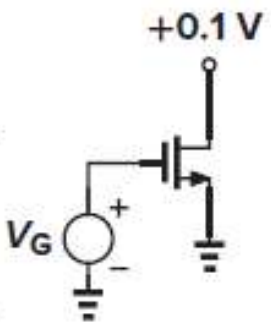
Appendix: MOSFET Simple Description

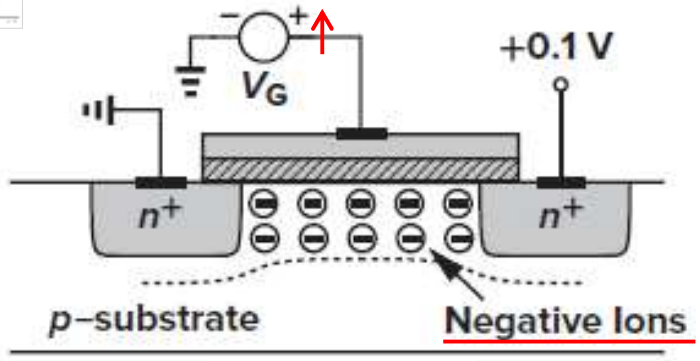
Detail information is shown on page 6-10



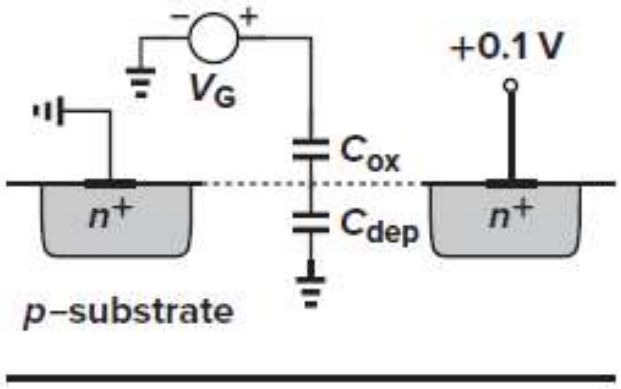


$V_G = 0$

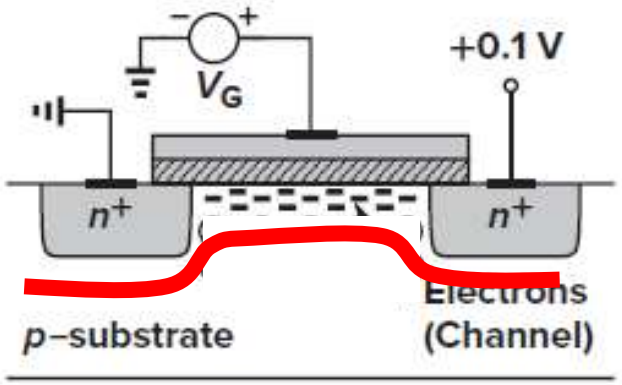




$0 < V_G < V_{TH}$



$V_G = V_{TH}$



$V_G > V_{TH}$

*Physically, it is driven by "energy band model, changed by V_G"