TAIWAN TECH National Taiwan University of Science and Technology

Introduction to Analog Integrated Circuit Design

Fall 2023

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MSIC Lab

DECE, NTUST

Mixed-Signal IC Laboratory NTUST

Instructor and Grading

- **Instructor: Yung-Hui Chung**
  - Course time: T6/T7, W2
  - Classroom: T6/T7(IB-305), W2(IB-307)
  - Office hours: Tue. 09:30~11:30 (by email)
  - Office: EE601-2
  - TEL: 02-27376394 (#6394)
  - Email: yhchung@mail.ntust.edu.tw
  - TA: 張繼元/郭哲原 (Lab: EE601-2, #7138)

- **Grading**
  - Homework: 40%
  - Mid-Exam: 30%
  - Final-Exam: 30%

Textbooks and References

- **Textbook:**
  - Behzad Razavi, **Design of Analog CMOS Integrated Circuits**, McGraw-Hill, 2nd Edition, 2017

- **References:**
  - Phillip E. Allen, Douglas E. Holberg, **CMOS Analog Circuit Design**, 3rd Edition, Oxford, 2011
  - Tony Chan Carusone, David A. Johns and Kenneth W. Martin, **Analog Integrated Circuit Design**, 2nd Edition, Wiley, 2011
  - Gray, Hurst, Lewis and Meyer, **Analysis and Design of Analog Integrated Circuits**, 5th Edition, Wiley, 2008

Course Content

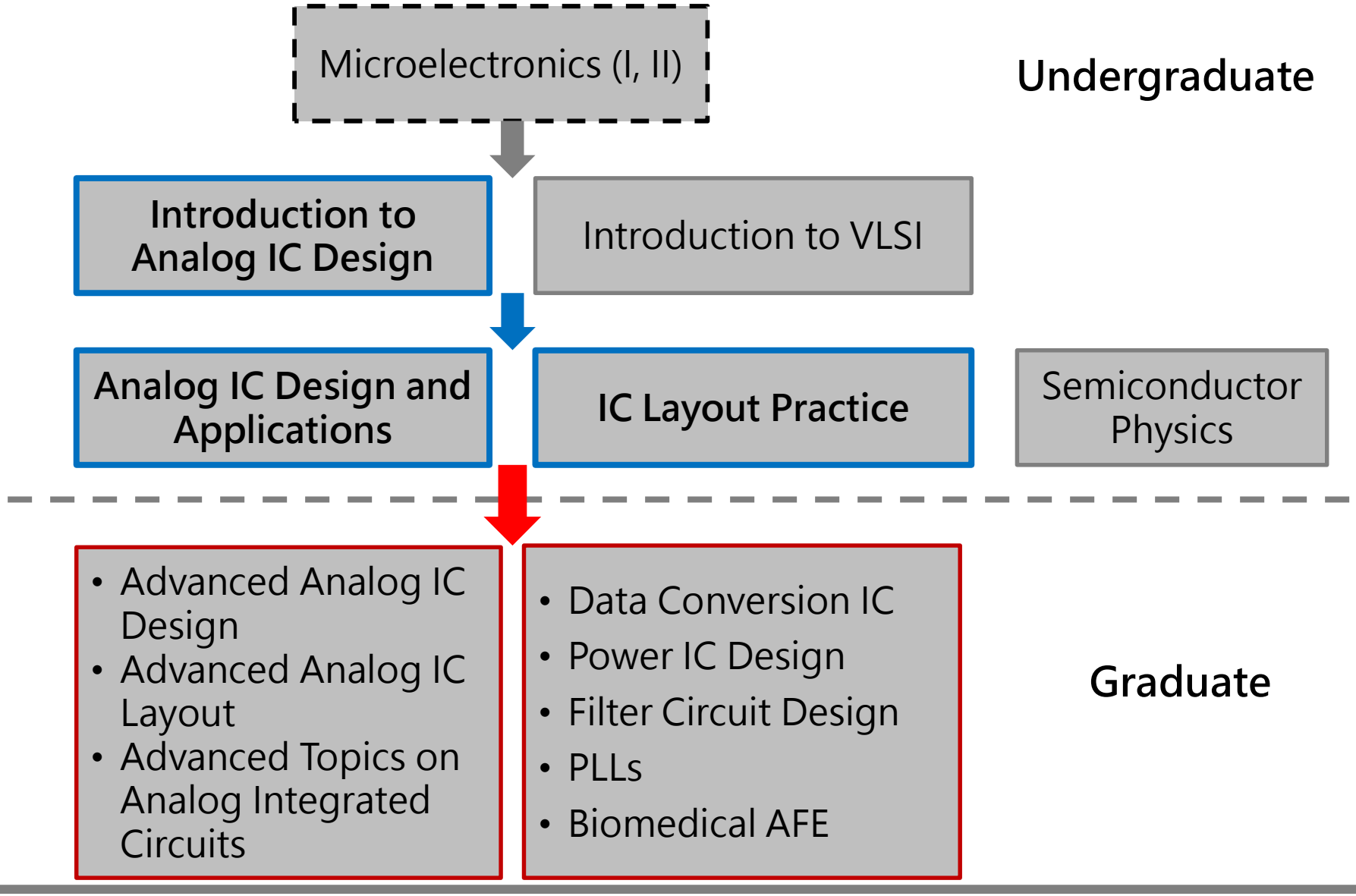
- **AIC1 (Introduction to Analog IC Design)**
  - MOS Device Physics and Modeling
  - Review of Amplifiers
  - Current Mirrors and Biasing Techniques
  - Frequency Response
  - Feedback
  - Stability and Frequency Compensation
  - Short Channel Effects
- AIC2 (Analog IC Design and Applications)
  - Noise
  - Operational Amplifiers (Opamps)
  - Bandgap References
  - Advanced Opamps
  - Nonlinearity and Mismatch
  - Switched-Capacitor Circuits

Course Schedule

Week	Date	Lecture Content (chapter in textbook)	Homework
1	9/5,6	MOST Physics (2)	
2	9/12,13	Review of Amplifiers (3)	
3	9/19,20	Review of Amplifiers (3/4)	HW1
4	9/26,27	Review of Amplifiers (4)	
5	10/3,4	Current Mirrors and Biasing Techniques (5)	HW2
6	10/10,11	Frequency Response (6)	
7	10/17,18	Frequency Response (6)	HW3
8	10/24,25	Midterm Exam	
9	10/31,11/1	Feedback (8)	
10	11/7,8	Feedback (8)	HW4
11	11/14,15	Feedback (8)	
12	11/21,22	Feedback (8) / Stability (10)	HW5
13	11/28,29	Stability and Freq. Compensation (10)	
14	12/5,6	Stability and Freq. Compensation (10)	HW6
15	12/12,13	Short Channel Effects (17)	
16	12/19,20	Final Exam	

*Week 17 and 18 are reserved for case study of analog IC design

Analog IC Courses



Analog Design Challenges

- Transistor Imperfections
- Declining Supply Voltages
  - 5V→2.5V→1.2V→0.9V
- Low Power Request
- Circuit Complexity

- Sensitive to PVT Variations
  - Process Corner: TT, FF, SS, SNFP, FNSP
  - Supply Voltage: VDD +/- 10%
  - Temperature: -40°C ~ +125°C

Abstraction Levels in Circuit Design

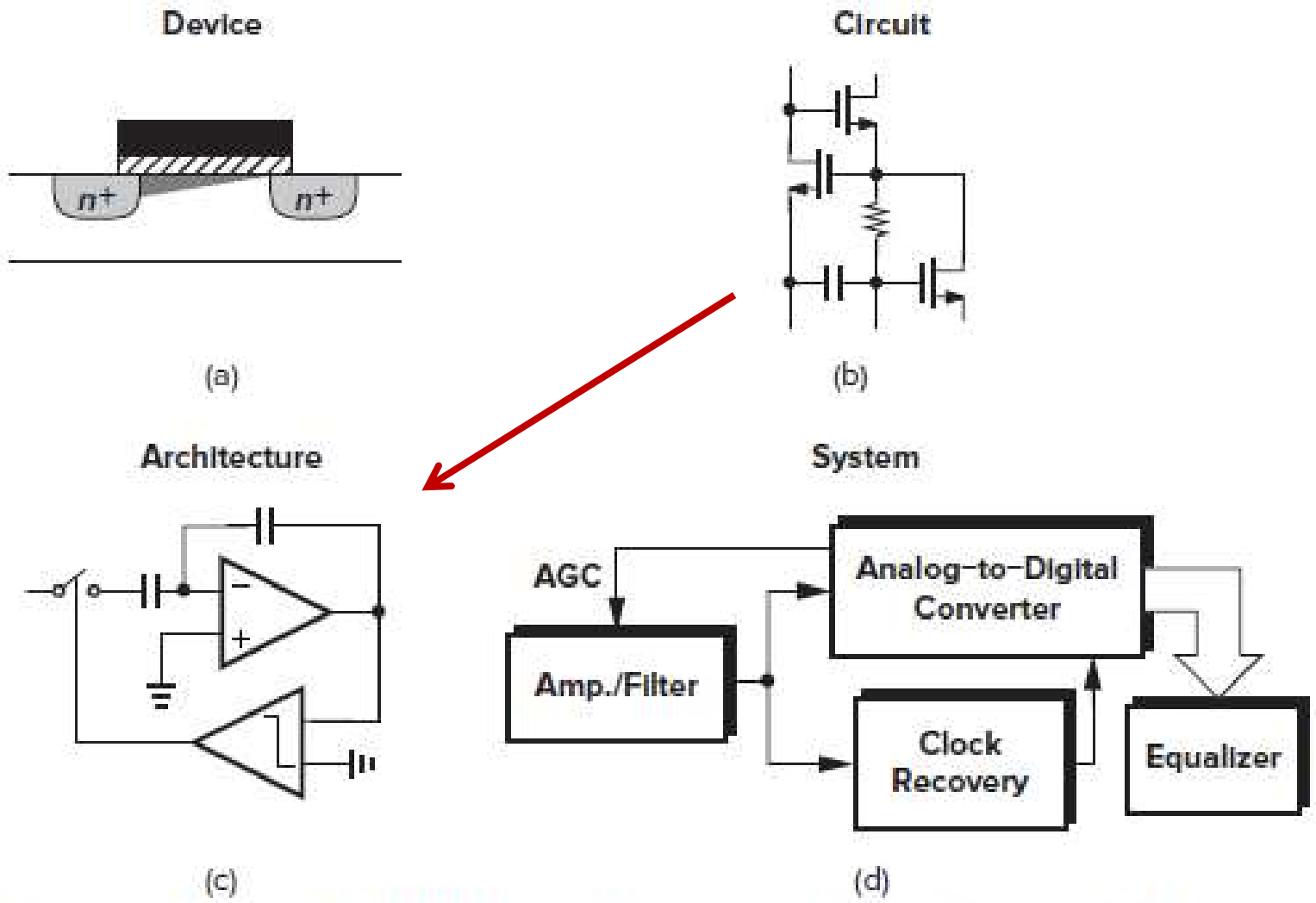
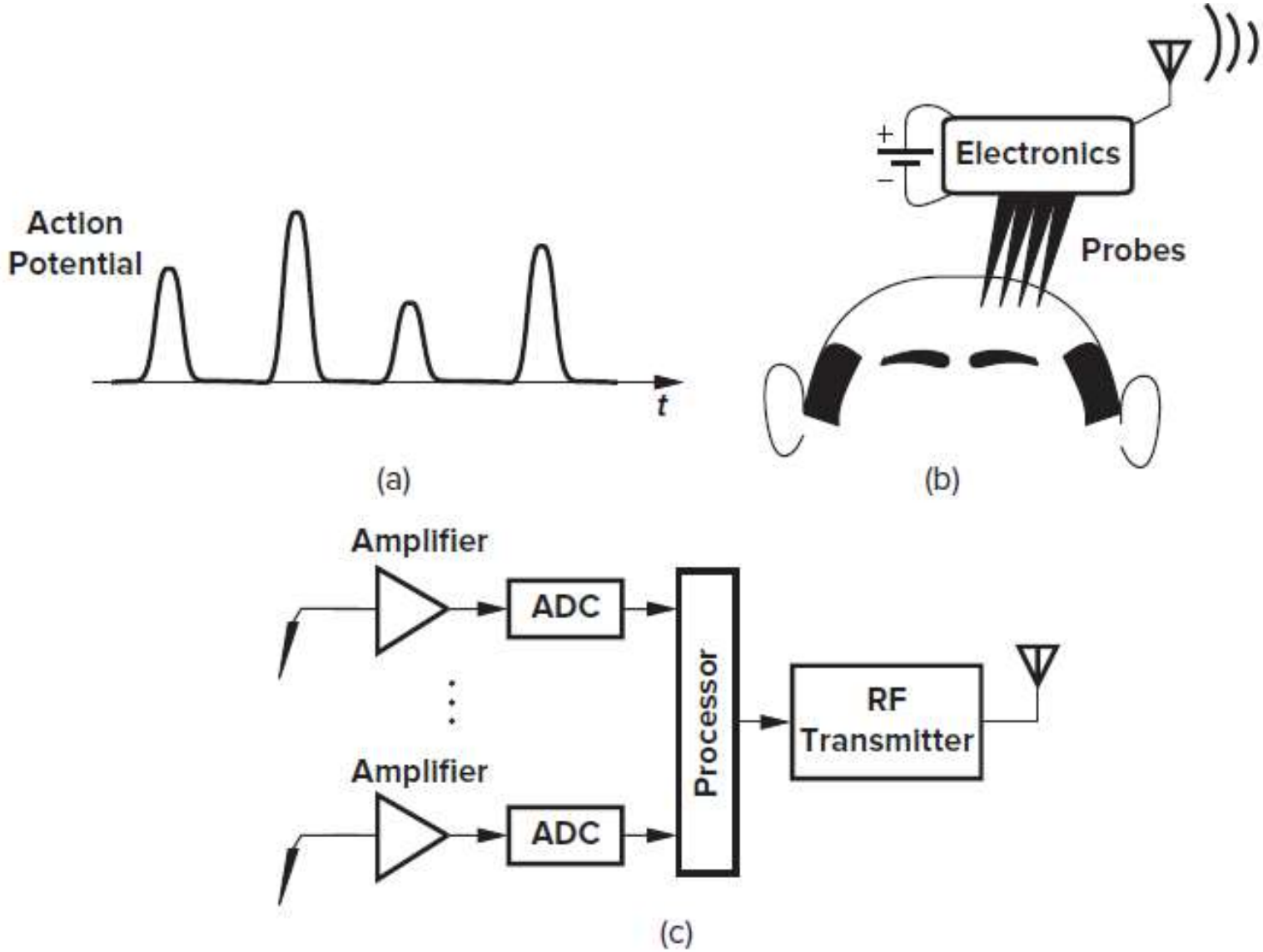
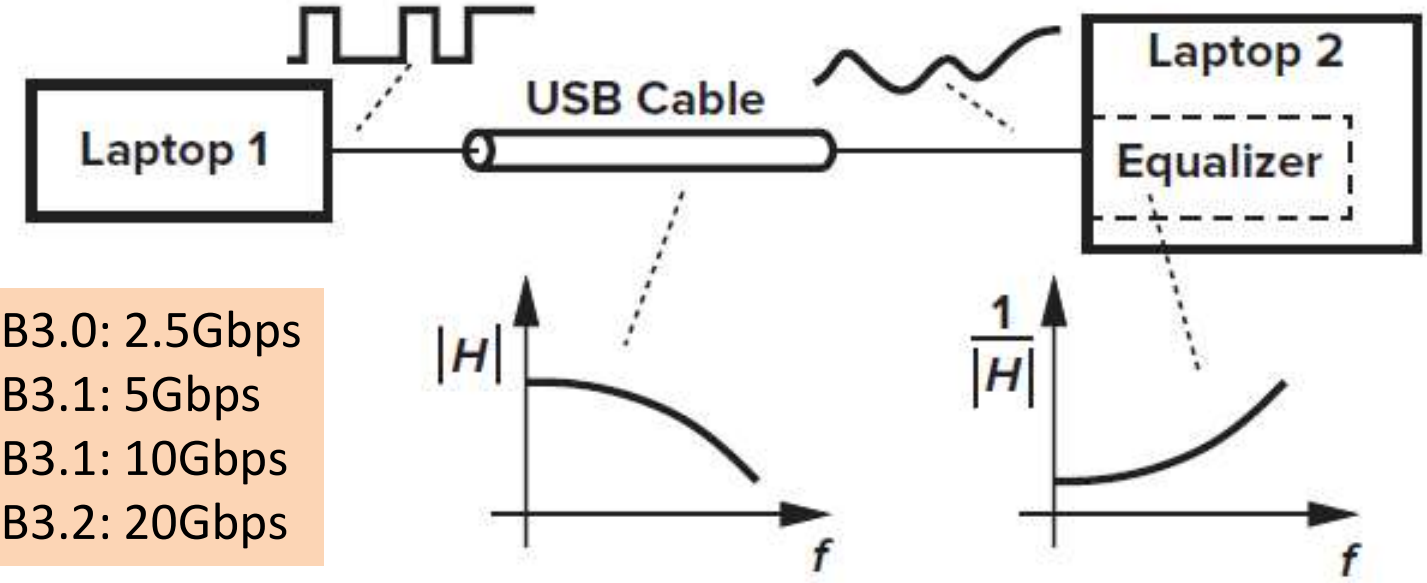


Figure 1.5 Abstraction levels in circuit design: (a) device level, (b) circuit level, (c) architecture level, (d) system level.

Biomedical Analog Front-End



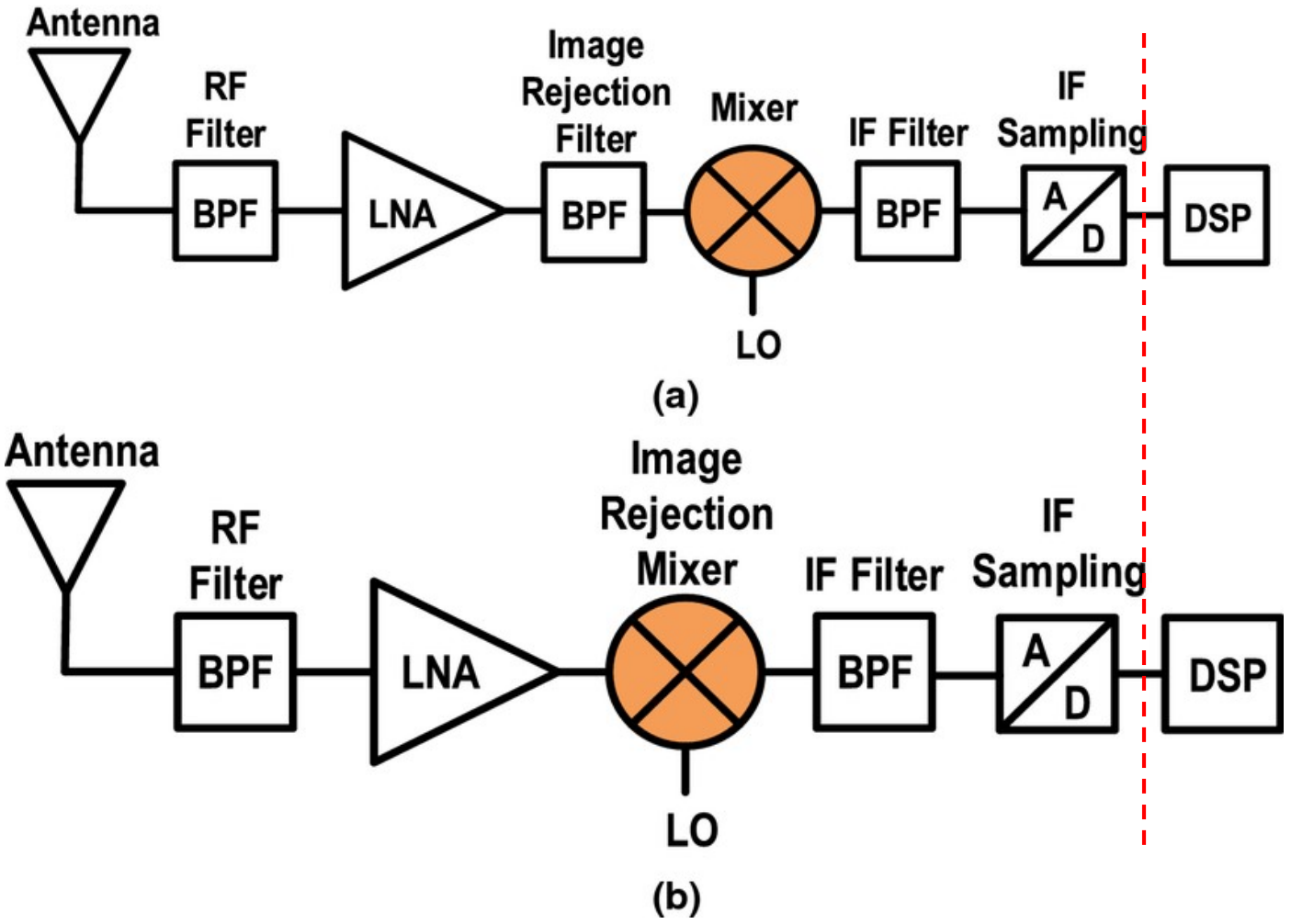
USB 3.0 (Serdes Applications)



USB3.0: 2.5Gbps
USB3.1: 5Gbps
USB3.1: 10Gbps
USB3.2: 20Gbps

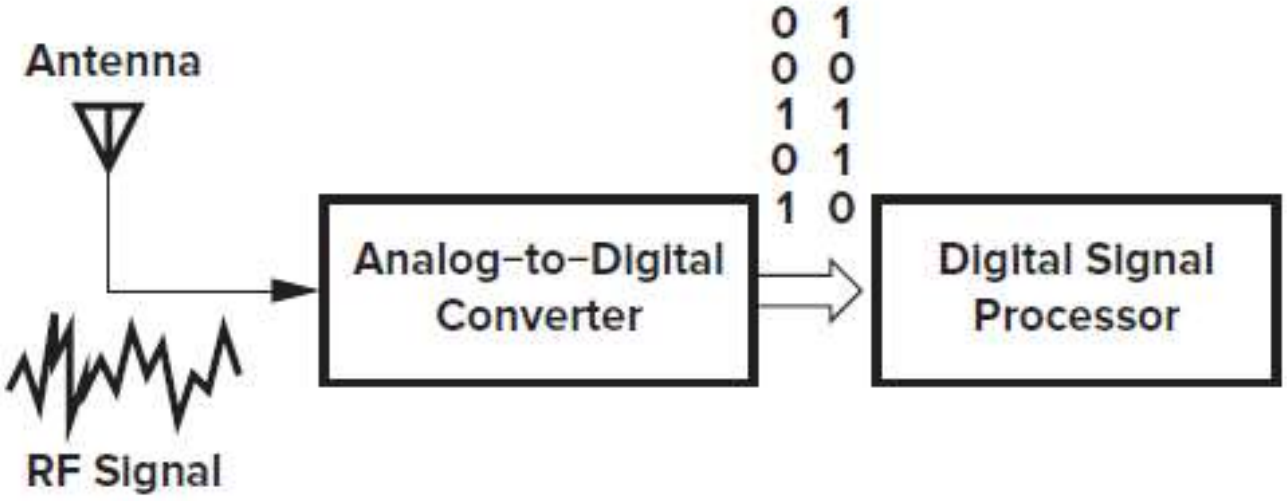
- Laptop 1 delivers the data to the cable in the form of a sequence of ONEs and ZEROs
- Since the cable attenuates high frequencies, we may design the equalizer to amplify such frequencies
- Serdes: Serializer and Deserializer (USB, PCIE, SATA, …)

Conventional RF Communication



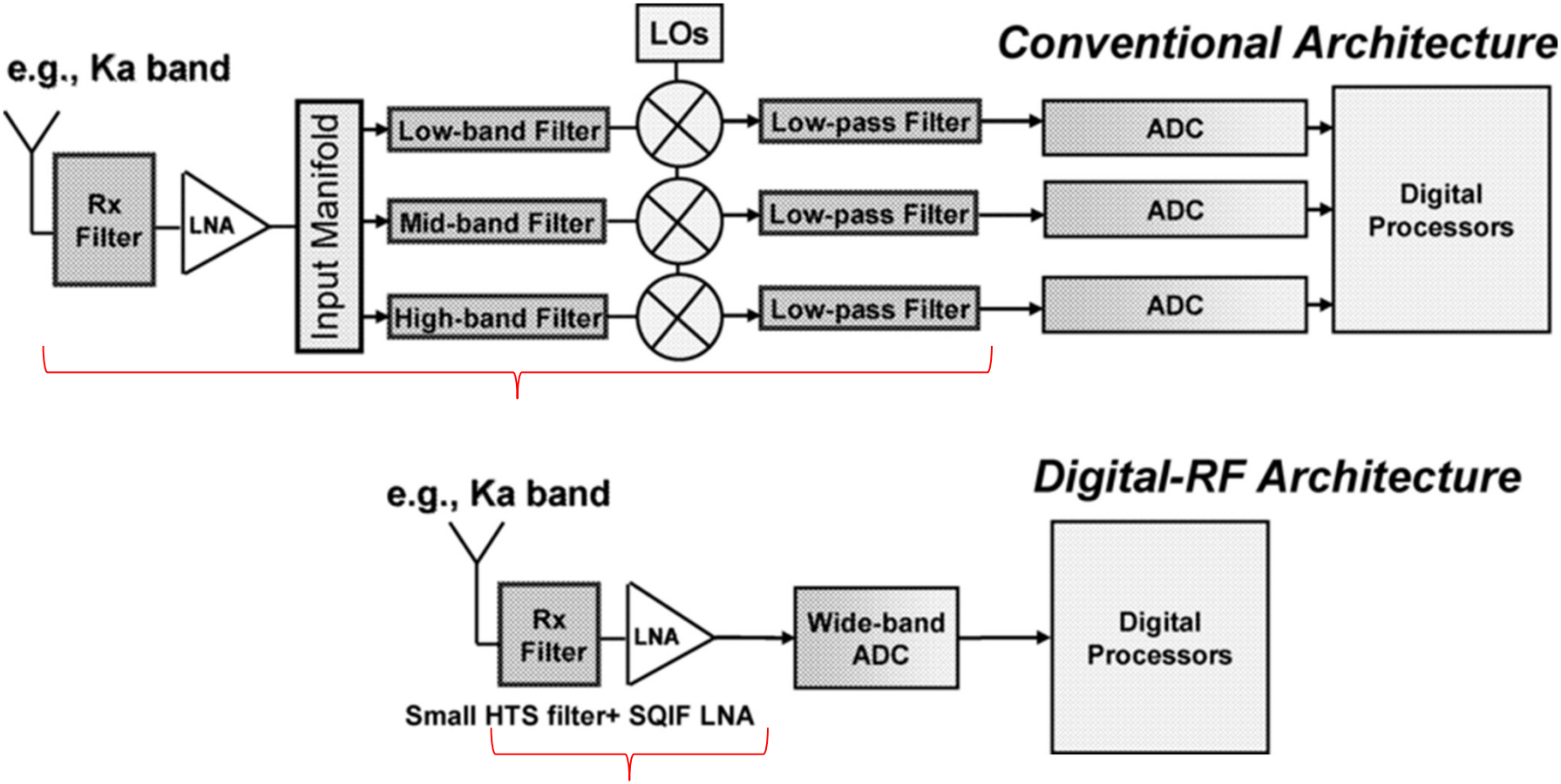
- May 2021, Circuits Systems and Signal Processing 40(7): 1-17
- DOI: 10.1007/s00034-020-01579-4

Advanced RF Receiver



- Direct RF Sampling to save more analog circuits (LNA, mixer, PLL, AAF, …) before ADCs
- As advanced CMOS technologies developed, ADC can be fast enough to directly sampling the RF signal (2.5GHz or higher)

RF Receiver Comparison



- March 2008, IEICE Transactions on Electronics 91-C(3):306-317
- DOI: 10.1093/ietele/e91-c.3.306