1071 Electronics Midterm 2 Chapter 5,6 2018/12/3 10:20~12:10

($V_{BE}(\text{on}) = V_{EB}(\text{on}) = 0.7$ V, $V_{CE}(\text{sat}) = V_{EC}(\text{sat}) = 0.2$ V, $V_A = \infty$, and $\beta = 100$ if not specified)

1. (10%) For the circuit shown in Figure 1, assume that Q_1 and Q_2 are matched and the transistor parameters are $\beta = 40$, $V_{BE}(\text{on}) = 0.7$ V, and $V_A = \infty$. (a) Use β to indicate the relationship between I_1 and I_Q. (b) Let $R_B = 0$. Design R_1 and R_C such that $I_Q = 0.25$ mA and $V_{CEQ0} = 3$ V.

2. (10%) Let $\beta = 25$ for the transistor in the circuit shown in Figure 2. Determine the range of V_1 such that $1 \leq V_{CE} \leq 4.5$V. Sketch the load line for I_C and V_{CE}.

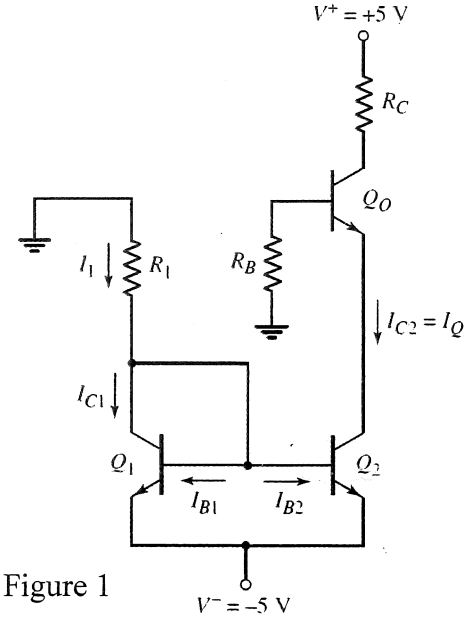

Figure 1

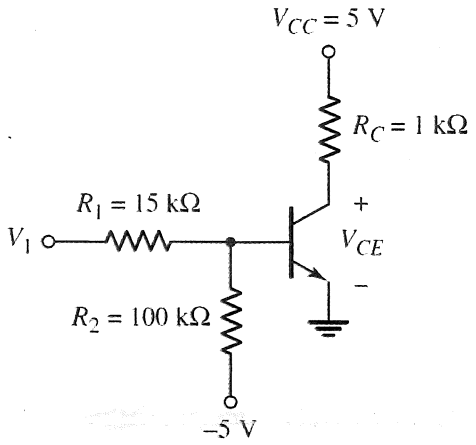

Figure 2

3. (15%) The common-emitter current gain of the transistor in Figure 3 is $\beta = 75$. Plot the voltage transfer characteristics over the range $0 \leq V_I \leq 5$V (9%). Please mark the status of the pnp transistor (6%).

4. (15%) The transistor shown in Figure 5 has parameters $\beta = 100$, and $V_A = \infty$. (a) Determine the quiescent values I_{CQ} and V_{ECQ}. (b) Determine the small-signal voltage gain $A_v = v_o/v_s$. (c) Find the input resistance R_i.

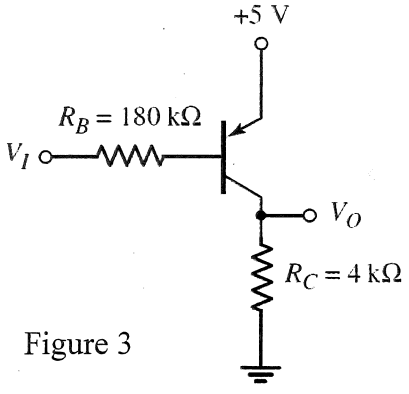

Figure 3

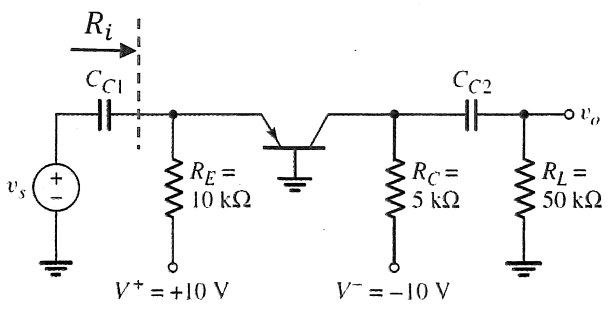

Figure 4

5. (15%) For the circuit shown in Figure 4, $V_{CC} = 3.3$ V, $R_L = 4$ kΩ, $R_1 = 585$ kΩ, $R_2 = 135$ kΩ, and $R_E = 12$ kΩ. The transistor parameters are $\beta = 75$ and $V_A = 60$ V (a) Determine the quiescent values I_{CQ} and V_{ECQ}. (b) Determine the small-signal voltage gain $A_v = v_o/v_s$. (c) Determine R_{ib} and R_o.

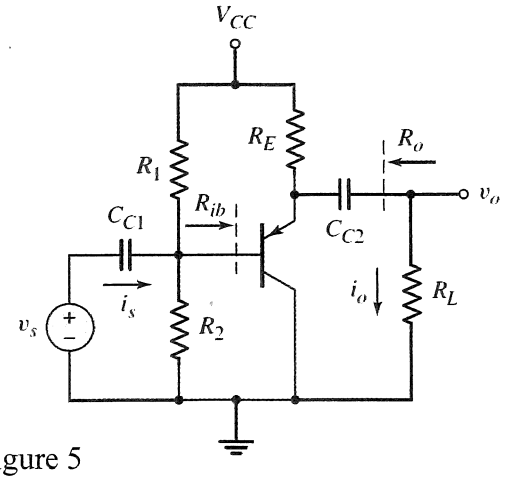

Figure 5

6. (15%) Consider the circuit shown in Figure 6. The transistor parameters are $\beta = 80$ and $V_A = \infty$. (a) Determine the quiescent collector current I_{CQ}. (b) Plot the dc and ac load line on the same graph and mark the slope. (c) Determine the maximum symmetrical swing in the output voltage ($\Delta v_{ec,peak-to-peak}$) if the total instantaneous C-E voltage is to remain in the range $0.7 \leq v_{EC} \leq 9$ V and the total instantaneous collector current is to be $i_C \geq 0$ mA.

7. (20%) For each transistor in the circuit in Figure 7, the parameters are $\beta = 125$, $V_{BE}(\text{on}) = 0.7$ V, and $r_o = \infty$. (a) Determine the Q-point of each transistor (I_{CQ} and V_{CEQ} for both Q_1 and Q_2) (4%). (b) Determine the small-signal parameters g_m, r_π , and r_o for both transistors (4%). (c) Find the overall small-signal voltage gain $A_v = v_o/v_s$ (6%). (d) Determine the input resistance R_i and output resistance R_o (6%).

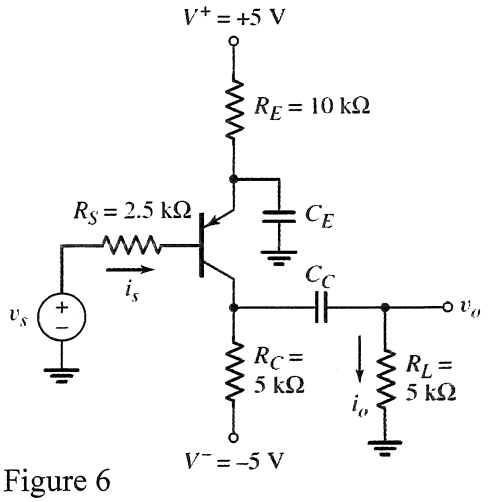

Figure 6

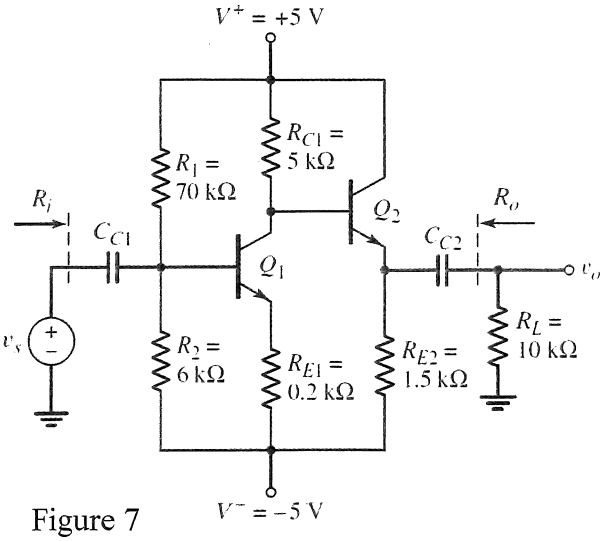

Figure 7