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TECHNICAL PAPER

A low power, temperature compensated, robust design of CS amplifier in nanoscale regime

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Abstract
A low power, temperature compensated, robust design of CS amplifier is proposed in this paper. A new voltage reference is introduced to enhance reliability of the design and decrease sensitivity of design metrics to temperature changes. The temperature compensation effect is explained and analytically modeled. Further, the amplifier consumes 1.34× less power than the other topologies available in literature due to subthreshold operation of devices in the biasing circuit and is suitable for extremely high temperature applications. All theoretical results are validated with simulation results obtained by simulating the circuit using Virtuoso Analog Design Environment of Cadence @ 45-nm technology node using metal gate/high-K/strained silicon BSIM4 model.

1 Introduction

Thermal instability of device parameters such as energy band gap, threshold voltage (Vth), leakage current, carrier density, diffusion and mobility (μ) pose great obstacles in the design of reliable and variation-aware analog circuits. The above phenomenon is even more severe in the nanoscale regime due to the decreasing difference between the supply and threshold voltage. This has made it extremely difficult to limit the design metrics within given boundaries.

A number of temperature compensation methodologies have been adopted in literature to overcome these issues. Biasing circuits that provide a fairly constant voltage, current or transconductance (gm) within a specified temperature range are presented in Theng et al. (2003) and Chen and Shi (2003). For an RF LNA authors in Gomez et al. (2010), proposed an adaptive biasing scheme, which counteracts the effects of temperature variations thereby making the design more reliable. This scheme exploits the conventional constant-gm voltage references to generate the required voltage–temperature characteristics. A low-supply bandgap voltage reference is used in Bendali and Audet (2007), to design a temperature stabilized current source, which is fabricated in a standard 180-nm CMOS process. This circuit topology also provides Vth compensation for process variations.

Numerous papers reported in the literature, examine the impact of temperature variations on design metrics of different analog and digital integrated circuits. These articles have laid down the guidelines to reduce the impact of temperature deviations. One such work is testified in Chen and Yuan (2011), in which the researchers have attempted to reduce the drift in output power of power amplifiers due to temperature variation and hence improve its efficiency. Further, the temperature compensation effect is described and modeled. A fairly similar study for the noise figure of a cascode low-noise CMOS amplifier is presented in Zhang and Yuan (2012). This study also presented mathematical equations for predicting the temperature compensation effect. However, the common source amplifier (CSA) has been largely ignored in this regard despite being a basic amplification cell used in numerous analog and mixed signal applications. Typically, in an amplifier formed by cascading a number of stages, the bulk of the voltage gain is obtained by using one or more CS stages in cascade.

In view of the above, this paper makes the following contributions:

1. The impact of temperature variations on the design metrics of CS amplifier such as gain, slew rate, bandwidth, output voltage swing, 1-dB compression

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point, noise figure and power dissipation is investigated.
2. A new biasing topology is proposed which not only enhances the reliability of the design but also reduces the power dissipation significantly. Further, its performance is compared with voltage references already available in the literature.
3. The temperature compensation effect is explained and analytically modeled.

The rest of the paper is organized as follows. Section 2 presents the temperature dependence of the device threshold and mobility. The simulation setup used is described in Sect. 3 and the existing biasing schemes are reviewed in Sect. 4. The proposed voltage reference is introduced in Sect. 5 and analytical expressions for its bias voltage are determined. The impact of temperature variations on the amplifier performance is studied in Sect. 6. Further, the temperature compensation effect is also modeled within the same section. Simulation results and discussions are presented in Sect. 7 and the concluding remarks are provided in Sect. 8.

2 Dependence study of device threshold and carrier mobility on temperature

The temperature reliance of MOS device metrics is primarily due to threshold voltage and mobility. The threshold voltage V_{th} exhibits a linear dependence on temperature which can be modeled as Kanda et al. (2001):

$$V_{th}(T) = V_{th}(T_o) + \alpha_{VT}(T - T_o). \quad (1)$$

Here, α_{VT} is the threshold voltage temperature coefficient and T_o is the reference temperature (300 K). For all design purposes, α_{VT} is an extracted parameter and has the following definition in BSIM4 model:

$$\alpha_{VT} = \frac{1}{T_o}\left(\alpha_1 + \frac{\alpha_L}{L_{eff}} + \alpha_2 V_{BSeff}\right), \quad (2)$$

where α_1 is the temperature coefficient for the threshold voltage, α_L is the dependence of temperature coefficient on channel length and α_2 is the body-bias coefficient of the V_{th} temperature effect with commonly used values of − 0.11, 0, and 0.022 respectively. However, for the sake of simplicity the threshold voltage temperature coefficient is assumed to be a constant varying from − 1 to − 4 mV/°C (Tsividis 1987; Laker and Sansen 1994) with the most frequently used figure being − 2 mV/°C.

Likewise, it is established that mobility demonstrates a negative exponential dependence on temperature which is captured using Filanovsky and Allam (2001), Wolpert and Ampadu (2012), Sze (1981), Yeric et al. (1990) and Cheng and Woo (1997):

$$\mu_N(T) = \mu_N(T_o)\left(\frac{T}{T_o}\right)^{\alpha_\mu}, \quad (3)$$

where, α_μ is the mobility temperature exponent and is also an extracted parameter like α_{VT}. Typically, α_μ is approximated as:

$$\alpha_\mu = \alpha_{\mu 0} + \alpha_{\mu 1}\left(\frac{\Delta T}{T_o}\right). \quad (4)$$

For an n-channel device, both $\alpha_{\mu 0}$ and $\alpha_{\mu 1}$ are negative and lie in the range from − 2.1 to − 1.9 and from − 0.05 to − 0.01 respectively (Berkeley 2011). Yet again, for convenience α_μ is considered to be a constant typically equal to − 1.5.

To validate the above models, the variation of threshold voltage and effective mobility of an n-type MOS device with specification tabulated in Table 1 is shown in Fig. 1.

3 Simulation setup

The devices in the common source amplifier are biased in saturation region and the output dc voltage level is kept at $V_{DD}/2$ so as to provide maximum room for the amplified output signal to swing. Five biasing methodologies (constant bias, three existing voltage references as shown in Fig. 2 and the proposed topology) are used to bias the amplifying device and performance of each scheme is studied separately.

Further, the transistors are sized appropriately so as to minimize the threshold voltage modulation due to process mismatch. The specifications of the amplifying and the load transistors are tabulated in Table 2. Table 3 shows the values of the bias voltages (of amplifying device) and currents used along with the coupling and load capacitances.

Finally, the 45-nm BSIM4 technology model using metal gate/high-K/strained silicon is utilized for simulation. Straining the crystalline silicon improves the device switching due to enhanced carrier mobility and drive current as compared to conventional devices (Geppert 2002). The gate leakage in the nanoscale regime can be

Table 1 Specifications of the transistor used for simulation

Type	Channel length (L), nm	Channel width (W), nm	Threshold voltage (V_{th}), mV	Temperature (°C)
NMOS	45	90	408.8	27

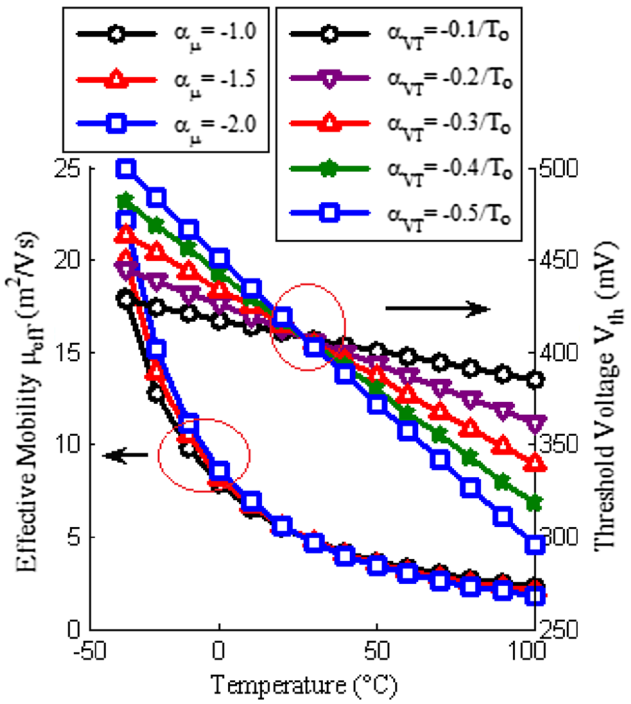

Fig. 1 Variation of threshold voltage V_{th} with temperature for different values of temperature coefficient α_{VT} at V_{GS} = 0.5 V, V_{DS} = 0.5 V, V_{BS} = 0 V and effective mobility (μ_{eff}) with temperature for different values of temperature coefficient α_{μ} at V_{GS} = 0.5 V, V_{DS} = 0.5 V and V_{BS} = 0 V

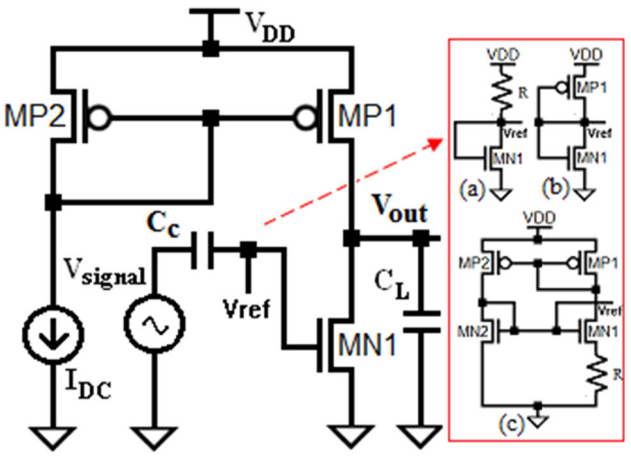

Fig. 2 Circuit description of the simulation setup and the existing biasing topologies (a) resistor-MOS, (b) MOS-only, (c) constant-g_m

considerably reduced by incorporating materials such as hafnium dioxide (HfO_2) which allow an increase in the physical thickness of the gate while keeping the EOT (equivalent oxide thickness) constant (Ribes et al. 2005). Finally, metal gates are employed to improve the control over the channel. The conventional polysilicon gates when biased, lead to the formation of a depletion region at the surface of the gate in contact with the insulator. The width

Table 2 Specifications of the amplifying and load transistor

Transistor	Channel length (L), nm	Channel width (W), μm	Threshold voltage (V_{th}), mV
MN1	180	2.7	468.663
MP1	180	4.9	− 417.481

Table 3 DC bias voltages for amplifying device, DC bias current, and values of coupling and load capacitances

DC bias current (I_{DC}), μA	Coupling capacitance (C_C), μF	Load capacitance (C_L), fF	$V_{GS(MN1)}$, mV	$V_{DS(MN1)}$, mV
10	10	100	477.5	517.36

of this depletion layer is about half a nanometer which adds to the effective thickness of the gate oxide thereby reducing coupling.

4 Review of existing biasing topologies

The fractional temperature coefficient (TC_F) for the reference voltage (V_{ref}) is typically used to quantify the temperature dependence of V_{ref} at a specific temperature and is an important parameter which is significant while examining temperature performance. It can be expressed as Allen and Holberg (2012):

$$TC_F(V_{ref}) = \frac{1}{V_{ref}} \cdot \frac{\partial V_{ref}}{\partial T} = \frac{1}{T} S_T^{V_{ref}}, \tag{5}$$

where, S is the sensitivity of V_{ref} with respect to temperature and is defined using:

$$S_T^{V_{ref}} = \frac{T}{V_{ref}} \frac{\partial V_{ref}}{\partial T}. \tag{6}$$

For non-linear dependencies, the effective temperature coefficient (TC_{eff}) is used within the specified temperature range and can be defined as Yuan (2011):

$$TC_{eff} = \frac{1}{V_{ref,avg}(T_{\max} - T_{\min})} \int_{T_{\min}}^{T_{\max}} V_{ref}(T) dT. \tag{7}$$

In (7), $V_{ref,avg}$ is the average value of the reference voltage over the specified temperature range and T_{max} and T_{min} specify the lower and upper extremities of the temperature range. Since the analytical modeling of V_{ref} is complex, the above can be approximated as:

$$TC_{eff} = \frac{1}{V_{ref,avg}} \left(\frac{V_{ref,\max} - V_{ref,\min}}{T_{\max} - T_{\min}} \right), \tag{8}$$

where, $V_{ref,max}$ and $V_{ref,min}$ are the maximum and minimum values that the reference voltage assumes within the particular temperature span. Hence, the rate of change of reference voltage with temperature would be a figure of interest.

The drain current I_D for a MOS device in saturation can be defined as Kumar et al. (2017):

$$I_D = \frac{\mu_{eff} C_{ox} W}{2L}(V_{GS} - V_{th})^2(1 + \lambda V_{DS}), \tag{9}$$

where μ_{eff}, C_{ox}, L, W, V_{GS}, V_{th}, V_{DS} and λ have their usual meaning.

The effective mobility μ_{eff} can be expressed as:

$$\mu_{eff} = \frac{\mu_N}{1 + \frac{E_{eff}}{E_o}} = \frac{\mu_N}{1 + \theta(V_{GS} - V_{th})}, \tag{10}$$

where, θ is the velocity saturation parameter inversely proportional to oxide thickness. From (10), it is clear that the effective mobility is inversely related to the gate drive.

Likewise, the transconductance g_m is equal to the slope of the $I_D - V_{GS}$ characteristics at the bias point and in the saturation region is defined as:

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \frac{\mu_N C_{ox} W}{2L}\left\{\frac{2(V_{GS} - V_{th})}{1 + \theta(V_{GS} - V_{th})} - \frac{\theta(V_{GS} - V_{th})^2}{[1 + \theta(V_{GS} - V_{th})]^2}\right\} \times (1 + \lambda V_{DS}). \tag{11}$$

The reference voltages as explained subsequently are sensitive to temperature variations since I_D and g_m exhibit a functional dependence on temperature. Because mobility (μ) and threshold voltage (V_{th}) primarily govern this temperature reliance, it can be deduced that:

$$\frac{\partial I_D}{\partial T} = \frac{\partial I_D}{\partial \mu_N}\frac{\partial \mu_N}{\partial T} + \frac{\partial I_D}{\partial V_{th}}\frac{\partial V_{th}}{\partial T}, \tag{12}$$

$$\frac{\partial g_m}{\partial T} = \frac{\partial g_m}{\partial \mu_N}\frac{\partial \mu_N}{\partial T} + \frac{\partial g_m}{\partial V_{th}}\frac{\partial V_{th}}{\partial T}. \tag{13}$$

It follows from (1) and (3) that:

$$\frac{\partial V_{th}}{\partial T} = \alpha_{VT} \quad \text{and} \quad \frac{\partial \mu_N}{\partial T} = \alpha_\mu \frac{\mu_N(T)}{T}, \tag{14}$$

where, α_μ is assumed to be a constant. It can be intuitively realized that both mobility and threshold voltage exhibit a negative dependence on temperature and the slope of V_{th} − T curve is a constant whereas the slope of the μ_{eff} − T curve itself is temperature dependent which justifies Fig. 1.

From (9) and (10), we get

$$\frac{\partial I_D}{\partial \mu_N} = \frac{C_{ox} W}{2L}\frac{(V_{GS} - V_{th})^2}{1 + \theta(V_{GS} - V_{th})}(1 + \lambda V_{DS}), \tag{15}$$

$$\frac{\partial I_D}{\partial V_{th}} = \frac{\mu_N C_{ox} W}{2L}\left\{\frac{-2(V_{GS} - V_{th})}{1 + \theta(V_{GS} - V_{th})} + \frac{\theta(V_{GS} - V_{th})^2}{[1 + \theta(V_{GS} - V_{th})]^2}\right\}(1 + \lambda V_{DS}). \tag{16}$$

Similarly from (11),

$$\frac{\partial g_m}{\partial \mu_N} = \frac{C_{ox} W}{2L}\left\{\frac{2(V_{GS} - V_{th})}{1 + \theta(V_{GS} - V_{th})} - \frac{\theta(V_{GS} - V_{th})^2}{[1 + \theta(V_{GS} - V_{th})]^2}\right\} \times (1 + \lambda V_{DS}), \tag{17}$$

$$\frac{\partial g_m}{\partial V_{th}} = \frac{\mu_N C_{ox} W}{2L}\left\{\frac{-2}{[1 + \theta(V_{GS} - V_{th})]^3}\right\}(1 + \lambda V_{DS}). \tag{18}$$

By putting the relations (14)–(18) in (12) and (13), the overall temperature models for I_D and g_m can be derived. These models are now used to obtain temperature relations for the various voltage references.

4.1 Constant voltage bias

The constant bias reference outputs a voltage that is independent of temperature i.e.,

$$\frac{\partial V_{ref}}{\partial T} = 0. \tag{19}$$

Such a reference can be constructed by forming a voltage divider using temperature independent resistors (TIRs). These TIRs consist of n+ and p+ polysilicon resistors combined in such a way that their overall temperature coefficient is practically negligible (Paily and Mahanta 2015).

4.2 Resistor-MOS voltage reference

The resistor-MOS reference consists of a divider formed using a TIR and a diode-connected MOS as shown in Fig. 2a. The reference voltage V_{ref} for this configuration is determined as:

$$V_{ref} = V_{DD} - RI_D. \tag{20}$$

Differentiating (20) w.r.t. temperature,

$$\frac{\partial V_{ref}}{\partial T} = -R\frac{\partial I_D}{\partial T} = -R\left(\frac{\partial I_D}{\partial V_{th}}\frac{\partial V_{th}}{\partial T}\right) - R\left(\frac{\partial I_D}{\partial \mu_N}\frac{\partial \mu_N}{\partial T}\right), \tag{21}$$

which can be obtained by substitutions from (14) to (16).

4.3 MOS-only voltage reference

The MOS only voltage divider (shown in Fig. 2c) consists of only active resistors and has the advantage of being compact as compared to R-MOS and resistor-only topologies (Baker 2010). The equivalent resistance (R_{out}) of an NMOS active resistor can be approximated as:

$$R_{out} = \frac{1}{g_m + g_{mbs} + g_{ds}} \approx \frac{1}{g_m}. \tag{22}$$

Hence, the output voltage V_{ref} of the MOS diode is equal to:

$$V_{ref} = R_{out} I_D = \frac{I_D}{g_m}. \tag{23}$$

The temperature relationship of the MOS-only voltage reference can be easily obtained by partially differentiating (23) w.r.t. temperature, to obtain

$$\frac{\partial V_{ref}}{\partial T} = \frac{1}{g_m}\frac{\partial I_D}{\partial T} - \frac{I_D}{(g_m)^2}\frac{\partial g_m}{\partial T}. \tag{24}$$

and substituting the suitable values from (14) to (18).

4.4 Constant-g_m voltage reference

A classical constant-g_m reference circuit consists of a self-biased quad of transistors and a TIR as shown in Fig. 2c. For this topology, it has been established that:

$$g_{m\,(MN2)} = \frac{2(1-\chi^{-0.5})}{R}, \tag{25}$$

where, χ is the ratio of channel widths of MN2 and MN1 and R is the resistance (Chu and Wang 2014). A simplified model for transconductance g_m as given below:

$$g_{m(MN2)} \approx \frac{\mu_N C_{ox} W_{MN2}(1+\lambda V_{DS})}{L_{MN2}}(V_{ref} - V_{th}), \tag{26}$$

can be used to obtain the value of the bias voltage V_{ref} by equating (25) and (26). It follows that:

$$V_{ref} = V_{th} + \frac{2(1-\chi^{-0.5})L_{MN2}}{RC_{ox}W_{MN2}\mu_N(1+\lambda V_{DS})}. \tag{27}$$

The sensitivity of this reference voltage to temperature can be determined as:

$$\frac{\partial V_{ref}}{\partial T} = \frac{\partial V_{th}}{\partial T} - \frac{2(1-\chi^{-0.5})L_{MN2}}{RC_{ox}W_{MN2}\mu_N^2(1+\lambda V_{DS})}\frac{\partial \mu_N}{\partial T}. \tag{28}$$

Now, since both mobility and threshold voltage exhibit negative temperature characteristics as observed from Fig. 1, they have opposing contributions in the expression of V_{ref} due to the presence of a negative sign. The change in V_{th} causes the bias voltage to drop with temperature, whereas the mobility μ has a positive impact on V_{ref}. Thus, this compensation phenomenon produces a bias voltage which is less sensitive to temperature (Wirnshofer 2013).

5 Proposed voltage reference

The proposed voltage reference (shown in Fig. 3) utilizes the self-bias transistor-quad configuration (MN1, MN2 and MP1, MP2) of the constant-g_m topology along with the active MOS diode (MN3). The self-biased transistor quad is sized to operate in the subthreshold region whereas the active MOS resistor operates in the super threshold region. The motivation behind this is reduction in power dissipation and greater increase in bias voltage with temperature due to exponential characteristics of drain current I_D in subthreshold region. Further, the active MOS diode is very compact and offers significant advantage over the polysilicon resistors in terms of die area requirement.

In subthreshold operation, I_D without taking channel length modulation into account can be expressed as Boser (2005):

$$I_D = \frac{\mu_N C_{ox} W (n-1) V_t^2}{L} e^{\left(\frac{V_{GS}-V_{th}}{nV_t}\right)}\left(1 - e^{\frac{-V_{DS}}{V_t}}\right). \tag{29}$$

Here, V_t is the thermal voltage defined as:

$$V_t = \frac{kT}{q}, \tag{30}$$

and has a value of about 26 mV at 300 K. The parameter n is:

$$n = \frac{C_{ox} + C_{depl}}{C_{ox}}, \tag{31}$$

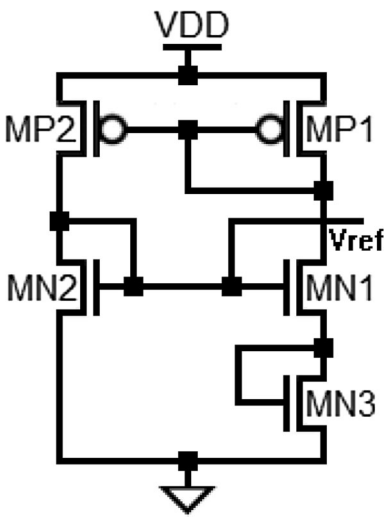

Fig. 3 Circuit level model of the proposed reference voltage generator

and is approximately equal to 1.5 in magnitude. C_{depl} is the depletion capacitance of the MOS device.

For $V_{DS} > 100$ mV, (29) can be reduced to:

$$I_D \approx \frac{\mu_N C_{ox} W(n-1)V_t^2}{L} e^{\left(\frac{V_{GS}-V_{th}}{nV_t}\right)}, \tag{32}$$

which can be used for calculating the transconductance of a MOS device operating in subthreshold as:

$$g_{mS} = \frac{\partial I_D}{\partial V_{GS}} = \frac{I_D}{nV_t}. \tag{33}$$

Finally, the above relations can be used to calculate the reference voltage for the proposed biasing topology. From (25) and (33):

$$\frac{I_D}{nV_t} = 2(1-\chi^{-0.5})g_m, \tag{34}$$

where, g_m is the transconductance of the MOS diode equal to the g_m of a saturated MOS device. After substitution of values from (32) and some algebraic manipulation, we get

$$V_{ref} = V_{th} + nV_t e^{\left(\frac{2nL(1-\chi^{-0.5})g_m}{\mu_N C_{ox} W(n-1)V_t}\right)} \tag{35}$$

where all the quantities have their usual meanings.

The fractional temperature coefficient for the proposed reference voltage can be calculated using:

$$\frac{\partial V_{ref}}{\partial T} = \frac{\partial V_{th}}{\partial T} + nV_t e^{\left(\frac{2nL(1-\chi^{-0.5})g_m}{\mu_N C_{ox} W(n-1)V_t}\right)} \left\{\frac{1}{T} + \Gamma\right\}, \tag{36}$$

where,

$$\Gamma = \frac{2nL(1-\chi^{-0.5})}{\mu_N C_{ox} W(n-1)V_t} \left\{\frac{\partial g_m}{\partial T} - \frac{g_m}{T}(1+\alpha_\mu)\right\}. \tag{37}$$

The final proposed topology of the Common Source amplifier is shown in Fig. 4.

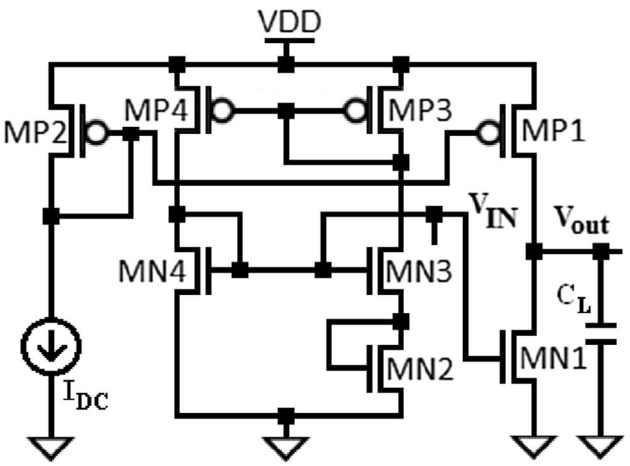

Fig. 4 Circuit level modal of the proposed CS amplifier

6 Dependence of amplifier performance on temperature

The open circuit voltage gain for CS amplifier is defined as:

$$A_V = -g_m\,(r_{o1}||r_{o2}), \tag{38}$$

where, the negative sign depicts the phase difference of 180° between the output and the input excitation. g_m is the transconductance of the amplifying device and r_{o1} and r_{o2} are the output resistances of the amplifying and load transistor respectively defined as:

$$r_o = \frac{|V_A|}{I_D} = \frac{1}{\lambda I_D}. \tag{39}$$

Here, I_D is the saturated drain current without taking channel length modulation into account, λ is the channel length modulation parameter and V_A is the early voltage characterized as:

$$V_A = \frac{I_D}{\partial I_D/\partial V_{DS}} = I_D\left[\frac{\partial I_D}{\partial V_{DS}}\right]^{-1}. \tag{40}$$

Different physical mechanisms such as channel length modulation (CLM), drain-induced barrier lowering (DIBL) and the substrate current induced body effect (SCBE) affect the Early voltage and in turn the output resistance in the saturation region. These mechanisms dominate in different regions of the operating V_{DS} (drain-to-source) as illustrated in Fig. 5. The different definitions of Early voltage V_A (and hence r_o) corresponding to different physical mechanisms is tabulated in Table 4.

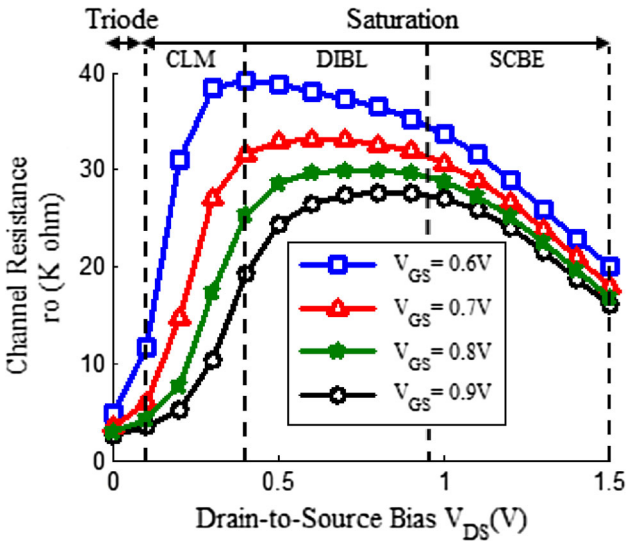

Fig. 5 Variation of channel resistance r_o with V_{DS} for different values of V_{GS}, V_{BS} = 0 V in different regions of operation

Table 4 Definitions of early voltage in the saturation region corresponding to different physical mechanisms

Channel length modulation (CLM)	Drain induced barrier lowering (DIBL)	Substrate current induced body effect (SCBE)
$I_D\left[\frac{\partial I_D}{\partial L_{eff}}\frac{\partial L_{eff}}{\partial V_{DS}}\right]^{-1}$	$I_D\left[\frac{\partial I_D}{\partial V_{th}}\frac{\partial V_{th}}{\partial V_{DS}}\right]^{-1}$	$\frac{L_{eff}}{\psi_2}e^{\frac{\psi_1\sigma}{V_{DS}-V_{Dsat}}}$

In Table 4,

$$\sigma = \sqrt{\frac{\varepsilon_{Si}\, t_{ox} X_J}{\varepsilon_G}}, \tag{41}$$

where, X_J is the junction depth, ψ_1 and ψ_2 are SCBE parameters, ε_{Si} and ε_G are the dielectric constant of silicon and gate dielectric constant relative to vacuum respectively and t_{ox} is the oxide thickness.

For derivation of temperature compensation models, channel length modulation (CLM) is assumed to be the dominant mechanism in the region of operation, hence from Table 4 and (9):

$$V_A = -L_{eff}\left(\frac{\partial L_{eff}}{\partial V_{DS}}\right)^{-1}. \tag{42}$$

Here, L_{eff} is the effective channel length of the MOS device which is defined as:

$$L_{eff} = L_{drwn} - 2L_d - X_d, \tag{43}$$

where, L_{drwn} is the drawn length of the polysilicon gate electrode, L_d is the lateral diffusion under the gate, assumed same for both source and drain and X_d is the drain depletion width. Since the drain depletion width X_d is the only bias dependent parameter in the expression of L_{eff},

$$r_o = \frac{L_{eff}}{I_D}\left(\frac{\partial X_d}{\partial V_{DS}}\right)^{-1}. \tag{44}$$

The drain depletion width X_d for the amplifying device MN1 assuming an abrupt junction is determined as Gray et al. (2009)

$$X_d = \sqrt{\frac{2\varepsilon_{Si}\,(V_{DS} - V_{ov})}{qN_A}}, \tag{45}$$

where, V_{DS} and V_{OV} are the drain-to-source and overdrive voltages respectively. N_A is the doping concentration of acceptor atoms, q is the electronic charge and ε_{Si} is the permittivity of silicon.

Partially differentiating (45) with respect to V_{DS}:

$$\frac{\partial X_d}{\partial V_{DS}} = \frac{1}{2X_d}\frac{2\varepsilon_{Si}}{qN_A} = \frac{\varepsilon_{Si}}{qN_A X_d}. \tag{46}$$

Therefore, from (44) the output resistance of the amplifying transistor MN1 can be expressed as:

$$r_{o1} = \frac{L_{eff}}{I_D}\cdot\frac{qN_A X_d}{\varepsilon_{Si}}, \tag{47}$$

where,

$$I_D = \frac{\mu_N C_{ox} W}{2L}\,\frac{(V_{GS} - V_{tn})^2}{1 + \theta(V_{GS} - V_{tn})}. \tag{48}$$

Similarly, the output resistance of MP1:

$$r_{o2} = \frac{L_{eff}}{I_D}\frac{qN_D X_d}{\varepsilon_{Si}}, \tag{49}$$

where,

$$I_D = \frac{\mu_P C_{ox} W}{2L}\,\frac{(V_{SG} - |V_{tp}|)^2}{1 + \theta(V_{SG} - |V_{tp}|)}. \tag{50}$$

The temperature relationship for A_V can be calculated using:

$$\frac{\partial A_V}{\partial T} = -\left\{g_m\frac{\partial(r_{o1}||r_{o2})}{\partial T} + (r_{o1}||r_{o2})\frac{\partial g_m}{\partial T}\right\}, \tag{51}$$

where,

$$\frac{\partial g_m}{\partial T} = \frac{\partial g_m}{\partial \mu_N}\frac{\partial \mu_N}{\partial T} + \frac{\partial g_m}{\partial V_{th}}\frac{\partial V_{th}}{\partial T} + \frac{\partial g_m}{\partial V_{GS}}\frac{\partial V_{ref}}{\partial T}, \tag{52}$$

since the total change in g_m is due to the contributions of the temperature dependent parameters of the amplifying transistor and its temperature dependent bias voltage. From (9),

$$\frac{\partial g_m}{\partial T} = \frac{\partial g_m}{\partial \mu_N}\frac{\partial \mu_N}{\partial T} + \left(\frac{\partial V_{th}}{\partial T} - \frac{\partial V_{ref}}{\partial T}\right)\frac{\partial g_m}{\partial V_{th}}. \tag{53}$$

Also,

$$\frac{\partial(r_{o1}||r_{o2})}{\partial T} = \left(\frac{r_{o1}}{r_{o1} + r_{o2}}\right)^2\frac{\partial r_{o2}}{\partial T} + \left(\frac{r_{o2}}{r_{o1} + r_{o2}}\right)^2\frac{\partial r_{o1}}{\partial T}, \tag{54}$$

which can be calculated using (47) and (49). It can be seen that:

$$\frac{\partial\, r_{o1(o2)}}{\partial T} = \frac{qN_{A(D)}}{\varepsilon_{Si}}\left\{\frac{I_D(L_{eff} - X_d)\frac{\partial X_d}{\partial T} - X_d L_{eff}\frac{\partial I_D}{\partial T}}{(I_D)^2}\right\}, \tag{55}$$

where,

$$\frac{\partial I_D}{\partial T} = \frac{\partial I_D}{\partial \mu_N}\frac{\partial \mu_N}{\partial T} + \left(\frac{\partial V_{th}}{\partial T} - \frac{\partial V_{ref}}{\partial T}\right)\frac{\partial I_D}{\partial V_{th}}, \tag{56}$$

$$\frac{\partial X_d}{\partial T} = \frac{\partial X_d}{\partial V_{th}}\frac{\partial V_{th}}{\partial T} + \frac{\partial X_d}{\partial V_{GS}}\frac{\partial V_{ref}}{\partial T}. \tag{57}$$

Substituting values from (45), gives:

$$\frac{\partial X_d}{\partial T} = \frac{\varepsilon_{Si}}{qN_A X_d}\left(\frac{\partial V_{th}}{\partial T} - \frac{\partial V_{ref}}{\partial T}\right). \tag{58}$$

Clearly, from (53), (56) and (58) a greater change in reference voltage with temperature implies a more temperature stable current, transconductance and hence gain. This is because greater the temperature dependence of V_{ref}, smaller the temperature dependence of g_{m}, I_{D}, X_{d} and hence A_{V}. Thereby, justifying the choice of subthreshold operation of the transistors of the biasing arrangement in addition to the added advantage of lower power dissipation. A similar explanation is true for other design metrics of the amplifier such as output voltage swing, bandwidth, slew rate etc. which are more or less dependent on the open circuit voltage gain.

The same relationships remain true even if drain induced barrier lowering (DIBL) is considered as the dominant one. However, in the DIBL region r_o can be expressed using (40) by substituting the value of Liu et al. (1993):

$$\frac{\partial V_{th}}{\partial V_{DS}} = -\psi_{th}(DIBL)\,(\chi_{DIBL} + \chi_B V_{BS})V_{DS}. \tag{59}$$

Here, χ_{DIBL} is the DIBL coefficient in the subthreshold region typically equal to 0.08 and χ_B is the body-bias coefficient for the subthreshold DIBL effect equal to $-0.07\ \mathrm{V}^{-1}$.

In (59),

$$\psi_{th}(DIBL) = \frac{1}{2\left[\cosh\left(\chi_{SUB}\,\frac{L_{eff}}{l_t}\right) - 1\right]} \tag{60}$$

where, χ_{SUB} is the DIBL coefficient exponent in the subthreshold region normally used as 0.56 and

$$l_t = \sqrt{\frac{\varepsilon_{Si} t_{ox} X_{dep}}{\varepsilon_{ox}}}. \tag{61}$$

In the above expression,

$$X_{dep} = \sqrt{\frac{2\,\varepsilon_{Si}\phi_S}{qN_{dep}}}, \tag{62}$$

where, N_{dep} is the channel doping concentration at depletion edge for zero body bias and Φ_S is the surface potential.

To validate the above theory, the variation of the reference voltage of the proposed biasing topology with temperature was studied and compared with other biasing topologies. The results are shown in Fig. 6. As observed, the variation of bias voltage with temperature in case of the proposed reference circuit is maximum as compared to its counterparts. Further, when this reference circuit is used to bias the amplifier, the drain current and transconductance of the amplifying device is found to be the most robust as shown in Figs. 7 and 8. The constant-g_m and constant bias references exhibit significant variations in I_D and g_m when used for biasing. However, the other three namely the proposed, diode-connected and resistor-MOS topologies

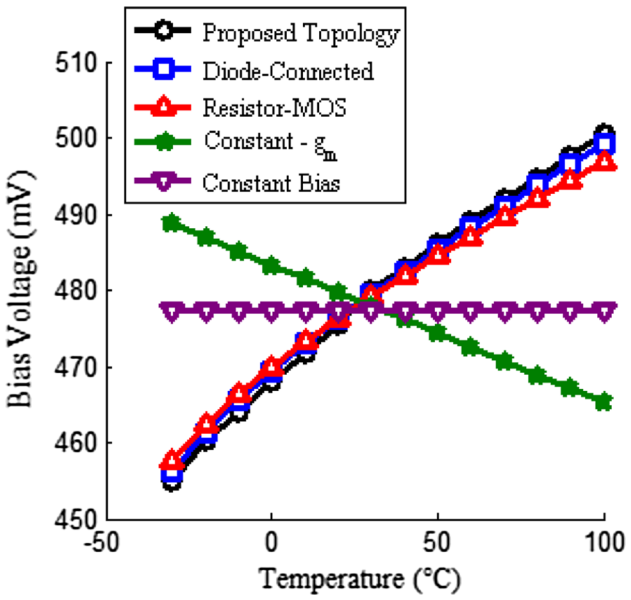

Fig. 6 Variation of reference voltage V_{ref} with temperature corresponding to different biasing topologies

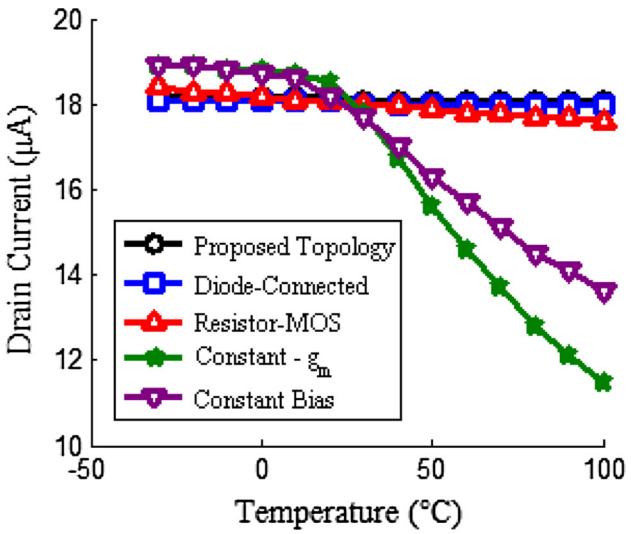

Fig. 7 Variation of drain current I_D of the amplifying device with temperature corresponding to different biasing topologies

have comparable performance. In case of drain current, the proposed topology has a maximum temperature sensitivity of about 0.55% which is 5.8× and 14× lesser than its MOS-only (3.2%) and resistor-MOS (7.7%) counterparts over a range of − 30 to 100 °C.

In addition, temperature sensitivities for transconductance g_m are 0.35, 0.39 and 0.41 respectively in absolute terms within the same temperature range. All these prove the suitability of the proposed design for realizing a temperature stable and robust amplifier.

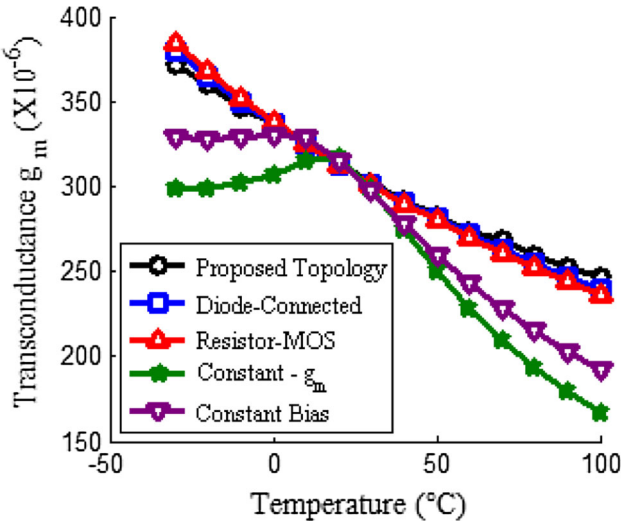

Fig. 8 Variation of transconductance g_m of the amplifying device with temperature corresponding to different biasing topologies

7 Simulation results and discussions

As established in the previous section, the proposed biasing topology is the most suitable for designing a temperature compensated and robust amplifier. This is because the parameters such as I_D and g_m, which largely govern the design metrics of an amplifier, are found to be the least temperature sensitive when the proposed biasing topology is adopted. The mathematical modelling and explanation for the same has also been discussed in the previous section. To further validate the above theory, the five voltage references are used to bias the amplifier and performance of each is studied separately.

The temperature characteristics of gain, output voltage swing and slew rate are calculated for each case and are depicted in Figs. 9, 10 and 11.

It can be seen from Figs. 9 and 10 that the proposed voltage reference enhances the reliability of the design by

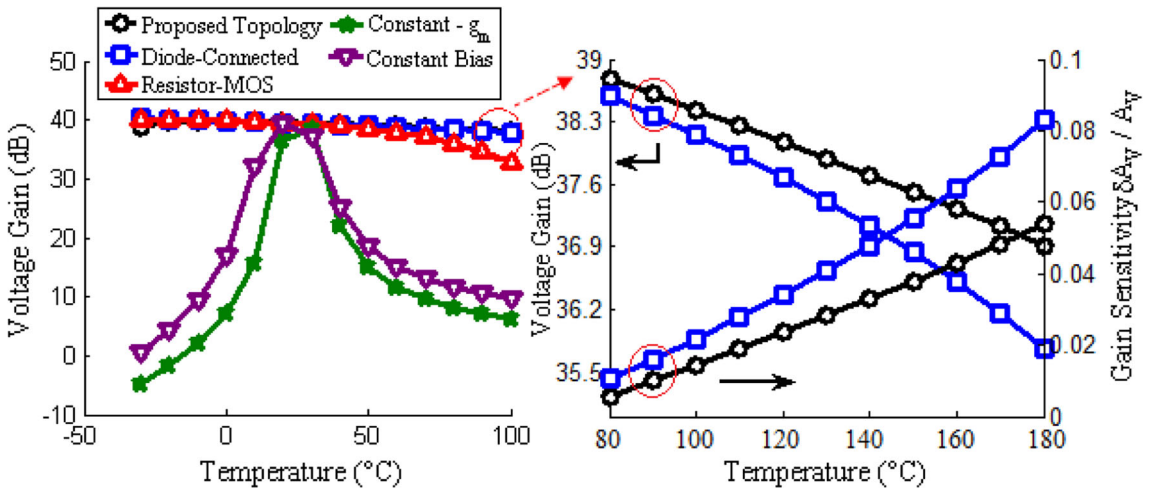

Fig. 9 Variation of voltage gain of the amplifier and gain sensitivity with temperature corresponding to different biasing topologies

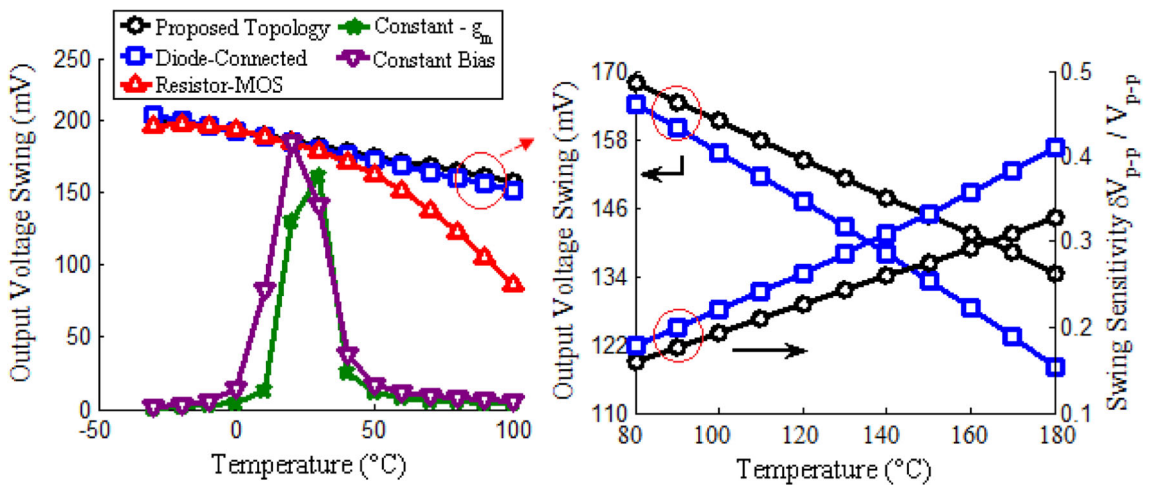

Fig. 10 Variation of voltage swing of the amplifier and swing sensitivity with temperature corresponding to different biasing topologies

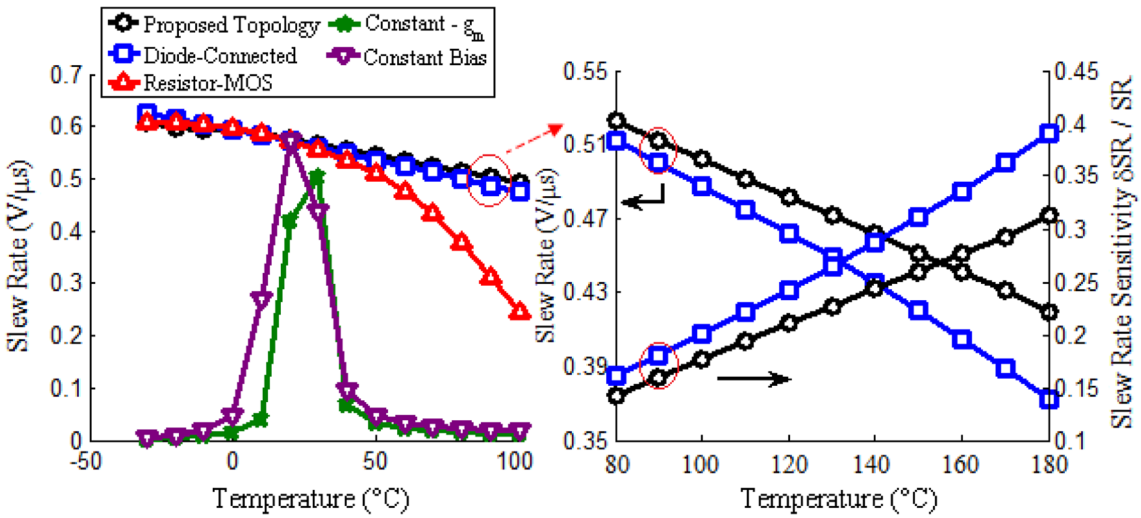

Fig. 11 Variation of slew rate of the amplifier and slew rate sensitivity with temperature corresponding to different biasing topologies

making the amplifier robust and less sensitive to temperature variations. It reduces the sensitivity of gain to 4.3% as compared to 5.2% (1.2× lesser) in case of the MOS-only divider and 18.1% (4.2× lesser) of the resistor-MOS divider over the temperature range from − 30 to 100 °C. This is because the MOS-only divider behaves like an adaptive voltage reference and its bias voltage increases more rapidly with temperature. This increase in V_{GS} provides greater compensation to the exponential degradation in mobility thereby minimizing the overall change in the circuit parameters. It has been observed in Figs. 7 and 8 that the variation in drain current I_D and transconductance g_m is the least in case of the proposed biasing methodology which leads to a more temperature-stable gain. The constant-g_m and constant bias reference circuits exhibit large variations and can be undoubtedly concluded as the least suitable for robust design. In addition, the proposed reference has significant advantage over the MOS-only divider as the temperature begins to exceed 100 °C. It can be observed from Fig. 9, that the sensitivity of the proposed circuit is 5.3% in comparison to 8.2% of its MOS-only counterpart at a temperature of 180 °C which is at least 1.54× lesser. Therefore, the amplifier designed using the proposed reference is also appropriate for extremely high temperature applications.

A similar trend is followed in case of the output voltage swing which can be observed from Fig. 10. The sensitivities of the proposed, MOS-only and resistor-MOS topologies are 0.215, 0.245 and 0.542 respectively in absolute terms over the temperature range of − 30 to 100 °C. Yet again, a 1.13× and 2.52× improvement has been recorded by the proposed circuit. Further, the output voltage swing for the proposed circuit is approximately 1.26× more stable in comparison to the diode-connected MOS divider at a temperature of 180 °C which is also depicted in Fig. 10. Similar conclusions from Fig. 11 can be drawn for the slew rate of the amplifier.

The slew rate of the proposed amplifier is found to be 1.17× and 3.22× more stable at 100 °C in comparison to the MOS-only and resistor-MOS topologies. Further, at 180 °C the slew rate sensitivity for the proposed circuit is 1.25× less than the MOS-only configuration. The temperature sensitivities for the design metrics of the amplifier corresponding to the biasing methodology adopted at 100 °C is tabulated in Table 5. Further, the sensitivities for

Table 5 Temperature sensitivities of design metrics of the amplifier at 100 °C corresponding to different biasing methodologies

Biasing scheme used	Gain sensitivity	Swing sensitivity	Bandwidth sensitivity	Slew rate sensitivity	Noise figure sensitivity	1-dB compression point sensitivity
Proposed topology	0.043	0.215	0.138	0.183	0.057	0.0085
Diode-connected	0.052	0.245	0.136	0.214	0.061	0.0094
Resistor-MOS	0.181	0.542	0.147	0.591	0.113	0.0108
Constant-g_m	0.831	0.975	0.189	0.978	0.350	0.0563
Constant bias	0.754	0.967	0.162	0.971	0.561	0.0771

Table 6 Temperature sensitivities at 180 °C for the proposed and MOS-only topology

Sensitivity (at T = 180 °C)	Proposed topology	Diode-connected
Gain sensitivity	0.053	0.082
Swing sensitivity	0.327	0.411
Bandwidth sensitivity	0.183	0.181
Slew rate sensitivity	0.312	0.391
Noise figure sensitivity	0.069	0.083
P_{1dB} sensitivity	0.0104	0.0123

the proposed and MOS-only topology at 180 °C are presented in Table 6.

In addition to the above design metrics, some of the other performance parameters which are very crucial in amplifier design are linearly and noise. The linearly of an amplifier can be quantified in terms of its 1-dB compression point P_{1dB} which is essentially the input power that causes the gain to decrease (compress by) 1 dB from the normal linear gain specification. The 1-dB compression point may be defined at the input level that produces it or the output power where the 1-dB drop occurs. The 1-dB compression point P_{1dB} of the proposed amplifier is found to be 1.10× and 1.27× more stable in comparison to the MOS-only and resistor-MOS topologies at 100 °C and 1.18× more stable in comparison with the MOS-only topology at 180 °C as tabulated in Tables 5 and 6. Similarly, the noise performance of an amplifier is measured in terms of its noise figure (NF). The NF sensitivities of the proposed, MOS-only and resistor-MOS topologies at 100 °C are 0.057, 0.061 and 0.113 respectively which translates into a 1.07× and 1.98× improvement. Further, the proposed design reports a 1.20× NF sensitivity improvement as compared to the MOS-only topology at 180 °C.

A summary of the design metrics of the common source amplifier namely gain, output voltage swing, bandwidth, slew rate, 1-dB compression point, noise figure and power dissipation at room temperature (27 °C) corresponding to the different biasing methodologies used is tabulated in Table 7.

All the voltage references are sized such that the bias voltage (V_{GS}) for the amplifying device is equal to 477.5 mV. As observed, the proposed topology has similar performance for each design metric and gives significant advantage in terms of power dissipation. It consumes 1.351×, 1.34×, 1.343× and 1.33× less power as compared to the diode-connected, resistor-MOS, constant-g_m and constant bias topology respectively. The variation of power dissipation of the amplifier with temperature is presented in Fig. 12. As observed, the amplifier when biased using the proposed voltage reference, consumes the least amount of power in comparison to the other voltage references. Since the drain current is the most stabilized in case of the proposed circuit, there is no significant variation (0.047 μW) in the power consumption with temperature. However, there is difference of 0.15, 0.8, 5.2 and 12.3 μW for the MOS-only, resistor-MOS, constant bias and constant-g_m configurations respectively over the temperature range of − 30 to 100 °C.

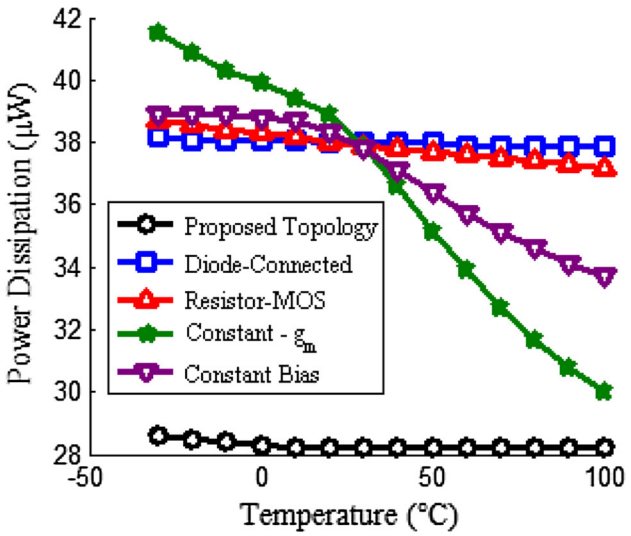

Fig. 12 Variation of power dissipated by the amplifier with temperature corresponding to different biasing topologies

Table 7 Summary of design metrics of the amplifier at 27 °C corresponding to different biasing methodologies

Biasing scheme used	Gain, dB	Output swing, mV	Bandwidth, MHz	Slew rate, V/μs	Power dissipation, μW	Noise figure NF, dB	1-dB compression point P_{1dB}, dBm
Proposed topology	39.45	182.19	788	0.565	28.2	18.53	− 2.18
Diode-connected	39.35	180.16	791	0.559	38.1	18.49	− 2.23
Resistor-MOS	39.28	178.45	786	0.554	37.8	18.55	− 2.31
Constant-g_m	38.44	160.82	783	0.502	37.9	18.61	− 2.18
Constant bias	37.35	141.64	782	0.438	37.5	18.42	− 2.35

It can be concluded from the above results, that the proposed voltage reference when used to bias the amplifier gives superior performance as compared to its counterparts available in literature both in terms of reliability and power consumption. The sensitivities of amplifier design metrics to temperature have been significantly reduced and power consumption has been reduced by at least 1.33 times.

8 Conclusion

A new biasing topology is proposed to enhance the reliability of design metrics of CS amplifier when subjected to temperature variations. The proposed design exhibits superior performance both in terms of robustness and power dissipation. The amplifier gain is less sensitive to temperature variations by 1.2× and 4.2× as compared to its MOS-only and resistor-MOS counterparts at 100 °C. Further, temperature sensitivity is improved significantly as the temperature increases beyond 100 °C, thereby supporting extremely high temperature applications. A similar trend is followed for output voltage swing, slew rate, 1-dB compression point and noise figure of the amplifier with respective sensitivity improvements of 1.13× and 2.52× for voltage swing, 1.17× and 3.22× for slew rate, 1.10× and 1.27× for 1-dB compression point and 1.07× and 1.98× for noise figure. In addition, the amplifier consumes at least 1.34× less power in comparison to the voltage references available in literature. This is due to the appropriate sizing of the devices which not only saves power due to subthreshold operation but also provides increased temperature compensation leading to a temperature stabilized drain current, transconductance and hence gain.

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