# Compact Model of Drain Current in Short-Channel Triple-Gate FinFETs

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***Abstract*—An analytical compact drain current model for undoped (or lightly doped) short-channel triple-gate fin-shaped field-effect transistors (finFETs) is presented, taking into account quantum-mechanical and short-channel effects such as threshold-voltage shifts, drain-induced barrier lowering, and subthreshold slope degradation. In the saturation region, the effects of series resistance, surface roughness scattering, channel length modulation, and saturation velocity were also considered. The proposed model has been validated by comparing the transfer and output characteristics with device simulations and with experimental results. The good accuracy and the symmetry of the model make it suitable for implementation in circuit simulation tools.**

***Index Terms*—Drain-current modeling, nanoscale finFETs.**

## I. Introduction

TRIPLE-GATE (TG) FETs such as fin-shaped field-effect transistors (finFETs) have been recognized as the best candidates for sub-100-nm scaling of MOSFETs due to their immunity to short-channel effects (SCEs) and proximity to standard bulk planar complementary metal–oxide–semiconductor processing [1]–[5]. However, as the FinFETs scale down, the fins need to be thinner for better control of the SCEs, resulting in difficulties for experimental realization of a specific doping profile in such thin fins. Lightly doped channels are preferred to reduce random dopant fluctuation [6], [7] and corner effects [8], [9].

For TG FinFETs, several analytical approaches have been developed for the calculation of the electrostatic potential within the channel [10]–[14]. Based on the potential analytical models, the threshold-voltage and the short-channel characteristics of the subthreshold slope and drain-induced barrier lowering (DIBL) were derived. However, for nanoscale FinFETs, most of the published drain-current models concern double-gate (DG) FinFETs, which include second-order effects such as DIBL, quantum-mechanical effects (QMEs), channel length modulation (CLM), and mobility degradation due to carrier velocity saturation [15]–[19].

To our knowledge, the studies published so far on drain-current modeling in TG FinFETs are very limited [20], [21]. In [20], the drain current was calculated from a charge-based equation of a long-channel DG MOSFET, which is a superposition of a standard bulk current equation above threshold and a 3-D model below threshold to predict the influence of the top gate on the subthreshold slope and threshold voltage. In this model, the threshold voltage was calculated from an analytical expression including the potential barrier at two different gate voltages and the inversion potential $\phi_i$ at the most leaky path [14]. Taking $\phi_i$ as a fitting parameter, comparison of the threshold-voltage model with numerical simulations yielded a fixed value of $\phi_i = 0.793$ V, independent of the channel geometry. However, it was not clarified if this value of $\phi_i$ is valid for any gate oxide thickness, whereas the model was verified only in transfer characteristics. More recently, in [21], an analytical drain-current model has been proposed in Π-shaped field effect transistor (ΠFET), using a suitable interpolation function that matches the weak and strong inversion modes near the threshold. However, this model is limited in the linear region of operation and was validated only in transfer characteristics for channel length down to 40 nm.

In this paper, based on analytical models for the threshold voltage and the subthreshold slope developed for undoped or lightly doped DG and TG MOSFETs [22] and relying on our previous analytical modeling of drain current in DG MOSFETs [23], we derive a fully analytical and compact drain-current model valid in all regions of operation for TG FinFETs, including SCEs, CLM, QMEs, and other secondary effects, such as mobility degradation and series resistance. The unique feature of the present model is the use of unified expressions for the inversion charge and drain current valid in all the regions of operation. The proposed compact model has been validated by comparing the transfer and output characteristics with simulation and experimental results.

## II. Compact Drain-Current Model

A schematic view of the TG FinFET is shown in Fig. 1, where $W_{\rm fin}$ is the fin width, $H_{\rm fin}$ is the fin height, and $L$ is the channel length. The gate electrode surrounds the silicon body on three sides with a gate oxide thickness $t_{\rm ox}$. The body of the silicon is lightly doped with acceptor concentration $N_A$ and the

Manuscript received December 9, 2011; accepted April 10, 2012. Date of publication May 18, 2012; date of current version June 15, 2012. This work was supported by the Greek Ministry of Education, Long Life Learning and Religious Affairs, General Secretariat for Research and Technology through the Program COOPERATION under Contract 09-ΣΥΝ-42-998. The review of this paper was arranged by Editor H. S. Momose.

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Digital Object Identifier 10.1109/TED.2012.2195318

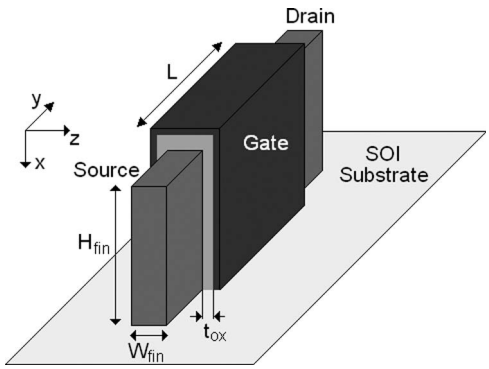


Fig. 1. Schematic 3-D representation of a TG FinFET.

gate material is metal with a proper work function to adjust the threshold voltage.

### A. Compact Drain-Current Equation

The drain-current equation of nanoscale TG FinFETs is defined by the unified charge-based equation of short-channel DG MOSFETs valid in all regions of operation [24], considering that each half of the top-gate width $W_{\rm fin}$ contributes to the side gate of width $H_{\rm fin}$. Therefore, the effective channel width of the TG FinFET is defined as $W = H_{\rm fin} + W_{\rm fin}/2$. However, the influence of the top gate on the SCEs is captured through the threshold voltage $V_t$ and the subthreshold swing coefficient $\eta_{\rm TG}$. As a result, the drain-current equation of TG FinFETs is similar to this of DG MOSFETs with increased channel width and modified parameters $V_t$ and $\eta_{\rm TG}$. The key features of the drain-current model and the improvements made in the threshold-voltage definition capable for predicting accurately the current–voltage characteristics of short-channel TG FinFETs will be presented in this section for brevity.

Under this light, the overall TG FinFET drain current is given by the following:

$$I_d = \mu_o \frac{2W}{L}\frac{\varepsilon_{\rm ox}}{t_{\rm ox}}(2V_{\rm th})^2\left[(q_{\rm is}-q_{\rm id}) + \frac{1}{2}\left(q_{\rm is}^2 - q_{\rm id}^2\right)\right] \quad (1)$$

where $\mu_o$ is the low-field electron mobility, $\varepsilon_{\rm ox}$ is the permittivity of the gate oxide, and $V_{\rm th} = {\rm kT/q}$ is the thermal voltage. The first charge term in the brackets of (1) dominates in the subthreshold region and the second charge term in the above-threshold region. $q_{\rm is}$ and $q_{\rm id}$ are the values of the normalized inversion sheet-charge densities calculated at the source and drain, respectively. Based on the unified normalized inversion sheet-charge density of DG MOSFETs [25], the modified one for TG FinFETs is described by the following relationship:

$$q_{\rm ix} = {\rm Lambert\ W}\left(e^{\frac{(V_g - V_t - V_x)}{2V_{\rm th}}}\frac{e^{\frac{(V_g - V_t - V_x)}{2\eta'_{\rm TG}V_{\rm th}}}}{A + e^{\frac{(V_g - V_t - V_x)}{2\eta'_{\rm TG}V_{\rm th}}}}\right) \quad (2)$$

where $V_x$ is the electron quasi-Fermi potential, which varies from the source voltage 0 to the drain voltage $V_d$. The first term of the Lambert W function dominates in the above-threshold region, whereas the second term dominates in the subthreshold region. The parameter $A$ in the Lambert W function is expressed as

$$A = 4e^{\frac{V_t + V_{\rm fb}}{V_o}}/e^{c_1} \quad (3)$$

where $V_o = 1$ V represents a normalizing factor, $V_{\rm fb} = \Delta\varphi - ({\rm kT/q})\ln(N_A/n_i)$ is the flatband voltage, $\Delta\varphi$ is the gate work function referenced to silicon, $N_A$ is the doping concentration of silicon, $n_i$ is the intrinsic carrier concentration, and $c_1$ is a fitting parameter for adjusting the transition from the below to the above-threshold region. The parameter $\eta'_{\rm TG} = \eta_{\rm TG}/(2 - \eta_{\rm TG})$ in (2) is a mathematical correction of the subthreshold swing coefficient $\eta_{\rm TG}$ for the TG FinFET reported in [22]. To improve the computational speed for the current calculation, we use a logarithmic approximation for the Lambert W$(x)$ function with good accuracy for positive $x$ [25].

In DG FinFETs, we have derived the threshold voltage from analysis in the subthreshold region using the minimum carrier sheet density $Q_{\rm th}$ as a fitting parameter [22]. The threshold voltage $V_t$ of the TG FinFET has been obtained by extending the DG FinFET threshold-voltage model to capture the electrostatic control of the top gate over the SCEs and using a fitting parameter that reflects the increase in the inversion carrier density in DG FinFETs needed in TG FinFETs to reach the threshold voltage [22]. However, this threshold-voltage model is not adequate to predict accurately the transfer and output characteristics of TG FinFETs since the obtained value of $V_t$ corresponds to the onset of the inversion-channel creation, and an increase in $V_t$ by few thermal voltages is needed to enter the strong inversion region. In this paper, we have improved our previous threshold-voltage model for both DG and TG FinFETs by deriving an analytical expression for $Q_{\rm th}$, leading to a threshold-voltage value that corresponds to the onset of strong inversion. The improved threshold-voltage model can be used to predict accurately the current–voltage characteristics of short-channel TG FinFETs. Starting from the strong inversion region in short-channel DG FinFETs, the normalized sheet-charge density is given in terms of the Lambert W function by

$$q_{ix1} = {\rm Lambert\ W}\left[\frac{qt_{\rm ox}}{\varepsilon_{\rm ox}}\sqrt{\frac{n_i^2\varepsilon_{\rm Si}}{2kTN_A}}e^{\frac{(V_g + \Delta V_t - V_{\rm fb} - V_x)}{2V_{\rm th}}}\right] \quad (4)$$

where $q$ is the electron charge, $\varepsilon_{\rm Si}$ is the permittivity of silicon and $\Delta V_t$ is the threshold-voltage roll-off [23]. The above equation can be rewritten as

$$q_{ix1} = {\rm LambertW} \times \left[e^{\frac{1}{2V_{\rm th}}\left[(V_g + \Delta V_t - V_{\rm fb} - V_x) + 2V_{\rm th}\ln\left(\frac{qt_{\rm ox}}{\varepsilon_{\rm ox}}\sqrt{\frac{n_i^2\varepsilon_{\rm Si}}{2kTN_A}}\right)\right]}\right]. \quad (5)$$

Equating (5) with (6)

$$q_{ix2} = {\rm Lambert\ W}\left[e^{\frac{1}{2V_{\rm th}}(V_g - V'_t - V_x)}\right] \quad (6)$$

we derive the threshold voltage $V_t'$ for DG FinFETs as follows:

$$V_t' = V_{\rm fb} - \frac{A_{1,DG}(V_{\rm bi}+V_d)+A_{2,DG}V_{\rm bi}}{1-(A_{1,DG}+A_{2,DG})} + \frac{V_{\rm th}}{1-(A_{1,DG}+A_{2,DG})}\ln\left(\frac{Q_{\rm th}N_A}{n_i^2 W_{\rm fin}}\right) \quad (7)$$

where $V_{\rm bi}$ is the built-in potential across the source/drain junctions and $A_{1,\rm DG}$ and $A_{2,\rm DG}$ are the parameters expressed as a function of the device natural length and channel length [22]. The obtained minimum carrier sheet density $Q_{\rm th}$, which is adequate to achieve the turn-on of the strong inversion condition, is given by the following analytical expression:

$$Q_{\rm th} = \left(\frac{2V_{\rm th}}{q}\right)\left(\frac{C_{\rm ox}^2}{C_{\rm Si}}\right) \quad (8)$$

where $C_{\rm Si} = \varepsilon_{\rm Si}/W_{\rm fin}$. The DG FinFET $V_t'$ model can be extended to the TG FinFET $V_t$ model by using effective parameters capturing the electrostatic control of the top gate over the SCEs and is described by the following expression:

$$V_t = V_{\rm fb} - \frac{A_{1,\rm TG}(V_{\rm bi}+V_d)+A_{2,\rm TG}V_{\rm bi}}{1-(A_{1,\rm TG}+A_{2,\rm TG})} + \frac{kT/q}{1-(A_{1,\rm TG}+A_{2,\rm TG})}\ln\left(\frac{Q_{\rm th}N_A}{n_i^2 W_{\rm fin}}\right) \quad (9)$$

where $Q_{\rm th}$ is given by (8). The parameters $A_{1,\rm TG}$ and $A_{2,\rm TG}$ are geometrical factors expressed as a function of $\lambda_{\rm sym}$ and $\lambda_{\rm asym}$, representing the natural lengths of the symmetric and asymmetric DG MOSFETs constituting the TG FinFETs [22]. These two characteristic lengths are associated with the conductive path of the "virtual cathode" in the silicon channel, which is expressed as

$$\lambda_{\rm sym} = \frac{1}{2}\sqrt{W_{\rm fin}\left(\frac{\varepsilon_{\rm Si}}{\varepsilon_{\rm ox}}t_{\rm ox}+\frac{3W_{\rm fin}}{16}\right)} \quad (10)$$

$$\lambda_{\rm asym} = \frac{1}{2}\sqrt{H_{\rm fin}\left(\frac{2\varepsilon_{\rm Si}}{\varepsilon_{\rm ox}}t_{\rm ox}+\frac{7H_{\rm fin}}{16}\right)}. \quad (11)$$

The analytical expression of (8) for $Q_{\rm th}$, which is extracted from the analysis of the sheet-charge density in the strong inversion region, leads to a threshold-voltage value corresponding to the onset of strong inversion, and it can be used for the calculation of the current–voltage characteristics. This finding explains the much higher fitting value of $Q_{\rm th}$, which is required to derive the current–voltage characteristics in DG MOSFETs [23], as compared with the $Q_{\rm th}$ value used to obtain the threshold voltage in the subthreshold region [26].

### B. CLM

When the drain–source voltage $V_d$ is increased beyond the saturation voltage $V_{\rm dsat} = V_g - V_t$, a pinchoff occurs in the channel moving from the drain toward the source. This displacement, known as the CLM effect, makes the channel shorter than the physical gate length $L$. The so-called electrical gate length $L'$ is given by

$$L' = L - \Delta L \quad (12)$$

where $\Delta L$ corresponds to the gap between $L$ and the channel pinchoff. Modifying the approach introduced in [27], we can model $\Delta L$ as

$$\Delta L = \lambda_{\rm eff}\ln\left[1+\frac{V_{\rm deff}-(V_g-V_t)}{V_E}\right]. \quad (13)$$

$V_E$ is a fitting parameter, and $\lambda_{\rm eff}$ corresponds to the effective natural length, which is the average of the two natural lengths $\lambda_{\rm sym}$ and $\lambda_{\rm asym}$, given for TG FinFETs by [28]

$$\lambda_{\rm eff} = \frac{1}{\sqrt{\left(\frac{1}{\lambda_{\rm sym}}\right)^2+\left(\frac{0.5}{\lambda_{\rm asym}}\right)^2}}. \quad (14)$$

In (13), $V_{\rm deff}$ is the effective drain voltage defined as

$$V_{\rm deff} = (V_g - V_t) + [V_d - (V_g - V_t) + 1]\tanh\left(\frac{V_d}{((V_g-V_t)+1)}\right)^2 \quad (15)$$

which is used to avoid discontinuity at $V_d = V_g - V_t$. Considering the CLM effect, the drain-current equation becomes

$$I_d = 2W\mu_o\frac{\varepsilon_{\rm ox}}{t_{\rm ox}}\left(\frac{2kT}{q}\right)^2\left[\frac{q_{\rm is}-q_{\rm id}}{L}+\frac{1}{2}\frac{q_{\rm is}^2-q_{\rm id}^2}{L-\Delta L}\right]. \quad (16)$$

### C. Mobility Degradation and Series Resistance

To compare the model with simulation and experimental results, the effects of series resistance and saturation velocity due to the horizontal drain field and surface roughness scattering due to the vertical gate field were considered in the above-threshold charge term of (16). These effects are included in the electron mobility expression in terms of the normalized inversion sheet-charge density at the source $q_{\rm is}$ given by

$$\mu = \frac{\mu_o}{1+\theta_1 V_{\rm th}q_{\rm is}} \quad (17)$$

where $\theta_1$ is the mobility attenuation factor of the first order. The charge $q_{\rm is}$ given by the associated Lambert equation generates secondary nonlinear effects around threshold; therefore, it is not required to consider the attenuation coefficient of the second order in the mobility expression reported in [29]. As in a conventional long-channel device, $\theta_1$ includes the linear mobility attenuation coefficient $\theta_{1,0}$, the high-field saturation velocity $\upsilon_{\rm sat}$, and the series resistance $R_{\rm sd}$ through the following relation:

$$\theta_1 = \theta_{1,0}\left(1+\frac{\mu_o V_d}{\upsilon_{\rm sat}(L-\Delta L)}\right)+\frac{\mu_o 2WC_{\rm ox}}{L-\Delta L}R_{\rm sd}. \quad (18)$$

It is mentioned that in FinFETs, the series resistance $R_{\rm sd}$ normalized with respect to the fin width $R_{\rm sd}W_{\rm fin}$, was found experimentally to be independent on the fin width [30], [31].

Substituting $\mu_o$ with $\mu$ in (16), the final compact equation for drain current becomes:

$$I_d = 2W\mu\frac{\varepsilon_{\rm ox}}{t_{\rm ox}}\left(\frac{2kT}{q}\right)^2\left[\frac{q_{\rm is}-q_{\rm id}}{L}+\frac{1}{2}\frac{q_{\rm is}^2-q_{\rm id}^2}{L-\Delta L}\right]. \quad (19)$$

### D. QMEs

In DG FinFETs, as the silicon fin width $W_{\rm fin}$ is scaled down to several nanometers ($<$ 10 nm), QMEs become significant since a quantum well is formed in the fin width between the two-side oxide layers (namely a structural confinement). Advanced analytical quantum-mechanical models have been developed accounting for arbitrary silicon film thickness, front- and back-gate charge coupling, and high transverse electric field confinement [32], or by incorporating the QMEs in a surface-potential-based compact model [33]. Furthermore, in addition to quantum threshold-voltage shift due to structural confinement, the gate capacitance degradation due to QMEs was considered, resulting in an enhanced value of the gate oxide thickness, which is bias dependent through the inversion charge density [34]. Although these models give insight into QMEs, the derived equations are very complicated and not straightforward for charge-based compact modeling in nanoscale FinFETs, requiring long computation time.

In the particular case of multiple-gate MOSFETs, for a compact modeling purpose, we use a simple model for QMEs by inserting the carrier-energy quantization caused by the structural confinement, as a widening of the band gap in thin films. In DG FinFETs, the minimum energy of the first subband above the conduction band is $E_{G1}=\hbar^2\pi^2/2m_{\rm eff}W_{\rm fin}^2$, where $\hbar$ is the reduced Plank's constant and $m_{\rm eff}$ is the effective mass of electrons along the confinement direction. This correction results in an increase in the threshold voltage $V_t$ of DG FinFETs by the following amount [35] [36]:

$$\Delta V_t^{\rm QM}=\frac{(\pi\hbar)^2}{2qm_{\rm eff}W_{\rm fin}^2}. \quad (20)$$

However, the energy of the first subband depends on the number of gates and is lower in devices where the electron distribution is more symmetrical, such as the DG FinFETs [37], [38]. In TG FinFETs ($W_{\rm fin}=H_{\rm fin}$), the value of $E_{G1}$ is twice the value obtained for DG FinFETs [37]. This modification in $E_{G1}$ introduces parameter $\alpha$ in the increase in $V_t$ due to QMEs as follows:

$$\Delta V_t^{\rm QM}=\alpha\frac{(\pi\hbar)^2}{2qm_{\rm eff}W_{\rm fin}^2} \quad (21)$$

where $\alpha=1$ for DG ($H_{\rm fin}\gg W_{\rm fin}$) and $\alpha=2$ for TG (square cross section) FinFETs.

The application of the compact model in simulation results of FinFETs demonstrates that the simple $V_t$ shift model due to structural confinement (21), including the second effect of bias-independent quantum degradation gate capacitance [35], [36], is sufficient to predict with good accuracy the current–voltage characteristics. The second effect arises from the quantum-mechanical distribution of the inversion charge, showing a peak inside the substrate at some distance away from the $SiO_2$-Si interface. This effect can be accounted for by considering two capacitance values connected in series: the oxide capacitance formed by the physical oxide layer and the capacitance developed within the average distance of $\Delta z$ inside the silicon from the interface [35], [36]. The QME results in an enhanced value of the gate oxide thickness given by

$$t_{\rm ox}^{\rm QM}=t_{\rm ox}+\Delta z\frac{\varepsilon_{\rm ox}}{\varepsilon_{\rm Si}}. \quad (22)$$

It was found that $\Delta z$ has a constant value of about 1.2 nm derived from the difference of the average inversion layer depths [35]. The modified value of the oxide thickness causes shift of the threshold voltage by $\Delta V_{t,{\rm tox}}^{\rm QM}$ calculated by replacing $t_{\rm ox}$ with $t_{\rm ox}^{\rm QM}$. Thus, including the QMEs in the drain-current equation, the classical threshold voltage $V_t$ is replaced by $V_t^{\rm QM}=V_t+\Delta V_t^{\rm QM}+\Delta V_{t,{\rm tox}}^{\rm QM}$ and $t_{\rm ox}$ with $t_{\rm ox}^{\rm QM}$.

## III. Model Validation With Simulation Results

Using the device simulator Silvaco (Atlas) and selecting the classical drift–diffusion approach, we have simulated the transfer and output characteristics of TG FinFETs with channel length, fin width, and fin height as parameters, satisfying the conditions $W_{\rm fin}<0.7$ L and $W_{\rm fin}<H_{\rm fin}/2$ in order to achieve realistic and operational FinFETs [22], [39]. When $W_{\rm fin}$ is much larger than $H_{\rm fin}$ or when the top-gate oxide is much thinner than the side oxides, the FinFET can be approximately treated as a single-gate fully depleted silicon-on-insulator (SOI) MOSFET as long as the silicon fin remains fully depleted. On the other hand, when $H_{\rm fin}$ is much larger than $W_{\rm fin}$, or the top-gate oxide is much thicker than the side oxides, the FinFET can be approximately treated as the DG FinFET.

We have considered the DG FinFET with parameters: fin width $W_{\rm fin}=5$ nm, fin height $H_{\rm fin}=30$ nm, channel length $L=30$ nm and equivalent gate oxide thickness $t_{\rm ox}=1$ nm; doping concentration of the silicon channel $N_A=1.45\times10^{10}$ cm$^{-3}$; doping concentration of the source/drain contact regions $N_D=10^{20}$ cm$^{-3}$; and a midgap metal gate with a work function of 4.71 eV. For QMEs, in Atlas 3-D simulations, the "Bohm quantum potential" (BQP) model was used with isotropic effective mass $m_x=0.7\times m_o$, where $m_o$ is the free electron mass.

In order to validate the model, in simulations and for simplicity, we keep constant the electron mobility ($\mu=200$ cm$^2$/V$\cdot$s) and saturation velocity ($\upsilon_{\rm sat}=10^7$ cm/s), whereas $\theta_{1,0}=0$ due to the absence of surface roughness scattering. In all cases, the verification was made using the complete model, which includes the QMEs. The parameter $\Delta z$, characterizing the oxide thickness enhancement due to QMEs, has a constant value of 0.7 nm in all devices. We compared the drain current computed with the model and the device simulator for DG FinFETs. Figs. 2(a) and 3(a) show the transfer characteristics in semi-logarithmic and linear plots for drain voltages $V_d=0.1$ and 1 V and the output characteristics for different $V_g$ values, respectively, for a DG FinFET ($\alpha=1$) with channel $L=30$ nm, $H_{\rm fin}=30$ nm, and $W_{\rm fin}=5$ nm. The model current–voltage characteristics were derived using the

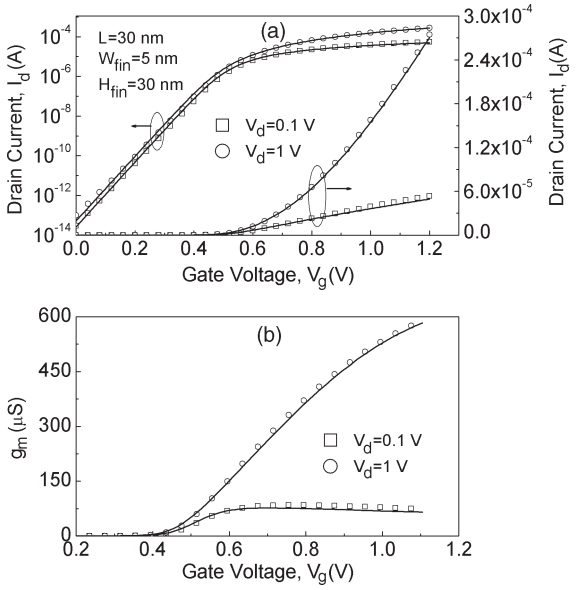


Fig. 2. Simulated (symbols) and modeled (solid lines): (a) Transfer characteristics in linear and semi-logarithmic representation and (b) $g_m$ versus $V_g$ plots of silicon DG FinFET with $W_{\rm fin} = 5$ nm, $H_{\rm fin} = 30$ nm, $L = 30$ nm, and $t_{\rm ox} = 1$ nm.

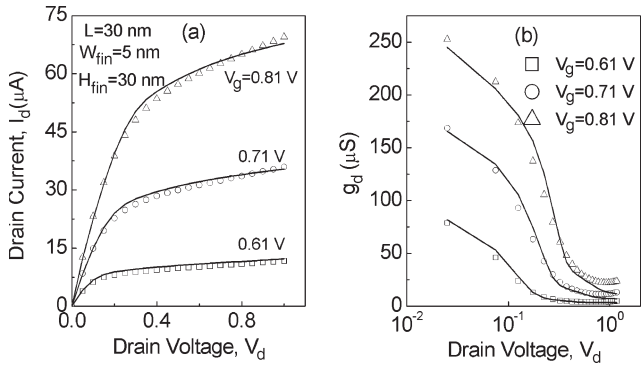


Fig. 3. Simulated (symbols) and modeled (solid lines): (a) output characteristics and (b) $g_d$ versus $V_d$ plots of the silicon DG FinFET with $W_{\rm fin} = 5$ nm, $H_{\rm fin} = 30$ nm, $L = 30$ nm, and $t_{\rm ox} = 1$ nm.

parameters: $V_E = 0.005$ V, $R_{\rm sd} \times W_{\rm fin} = 2.5 \times 10^{-4}\ \Omega \cdot$ cm, and $c_1 = 2$. It can be seen that the model describes very well the current–voltage characteristics in all regions of operation.

In order to check further the accuracy of the drain-current model, the small-signal parameters and, particularly, the transconductance $g_m$ and the drain conductance $g_d$ have been examined. A comparison of the model with the simulation values of $g_m$ for two different values of drain voltage ($V_d = 0.1$ and 1 V) is shown in Fig. 2(b), which is derived from the data in Fig. 2(a). Furthermore, a comparison of the model with the simulation values of $g_d$ for different values of gate voltage is shown in Fig. 3(b), derived from the data in Fig. 3(a). The agreement between the simulated and modeled results of the small-signal parameters supports further the good accuracy of the proposed compact model.

The model has been validated also for a TG FinFET with fin width equal to fin height ($H_{\rm fin} = W_{\rm fin} = 20$ nm), as shown in Figs. 4 and 5, giving accurate results for both static characteristics and small-signal parameters. The

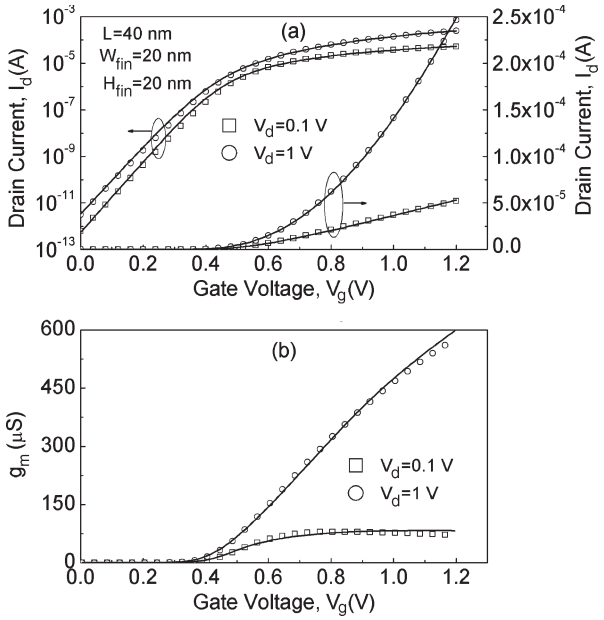


Fig. 4. Simulated (symbols) and modeled (solid lines): (a) transfer characteristics in linear and semi-logarithmic representation and (b) $g_m$ versus $V_g$ plots of the silicon TG FinFET with $W_{\rm fin} = 20$ nm, $H_{\rm fin} = 20$ nm, $L = 20$ nm, and $t_{\rm ox} = 1$ nm.

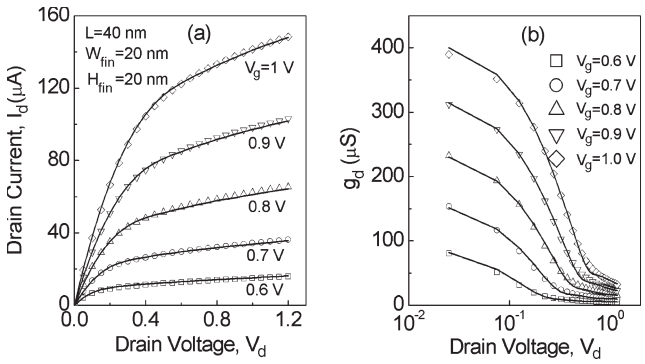


Fig. 5. Simulated (symbols) and modeled (solid lines): (a) output characteristics and (b) $g_d$ versus $V_d$ plots of silicon TG FinFET with $W_{\rm fin} = 20$ nm, $H_{\rm fin} = 20$ nm, $L = 20$ nm, and $t_{\rm ox} = 1$ nm.

model current–voltage characteristics were derived using the parameters: $V_E = 0.35$ V, $R_{\rm sd} \times W_{\rm fin} = 2.5 \times 10^{-4}\ \Omega \cdot$ cm, $c_1 = 3$. The good agreement between model and simulated results in both weak and strong inversion regimes is evident.

The validity of the compact drain-current model including the QMEs was verified for other channel dimensions. The unified expressions for the current and charge (2) and (21), respectively, can be used to derive analytical expressions for the total charges and capacitance values at the source, drain, and gate terminals of the device. Preliminary results have shown excellent agreement of the modeled capacitance values with numerical simulations (not presented). This will be the subject of our feature work.

## IV. Model Validation With Experimental Results

The analytic drain-current model has been verified also by comparing the model with the experimental transfer and output

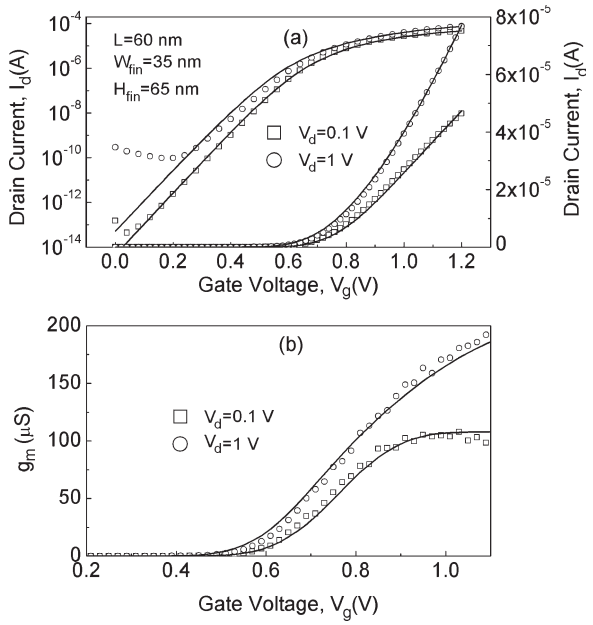


Fig. 6. Experimental (symbols) and modeled (solid lines): (a) transfer characteristics in linear and semi-logarithmic representation and (b) $g_m$ versus $V_g$ plots of silicon TG FinFET with $W_{\rm fin} = 35$ nm, $H_{\rm fin} = 65$ nm, $L = 60$ nm, and $t_{\rm ox} = 1.7$ nm.

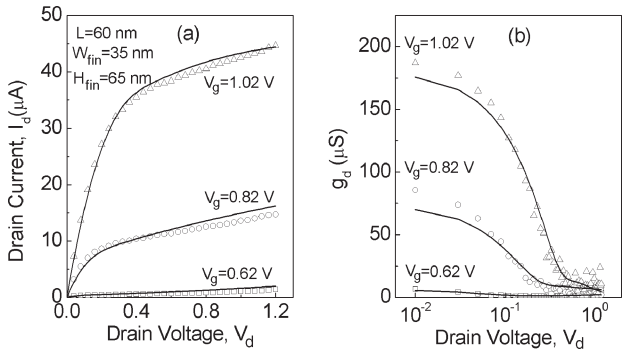


Fig. 7. Experimental (symbols) and modeled (solid lines): (a) output characteristics and (b) $g_d$ versus $V_d$ plots of silicon TG FinFET with $W_{\rm fin} = 35$ nm, $H_{\rm fin} = 65$ nm, $L = 60$ nm and $t_{\rm ox} = 1.7$ nm.

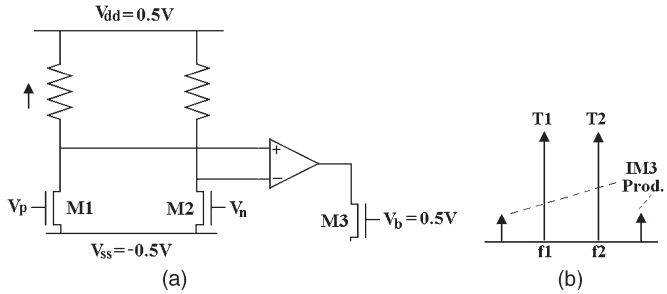


Fig. 8. (a) Analog gain stage for assessing the proposed compact model linearity behavior (b) with typical output behavior in the frequency domain.

characteristics of TG FinFETs, fabricated at Interuniversity MicroElectronics Center (IMEC) (Leuven) on SOI wafers with 145-nm buried oxide thickness [21]. The device parameters are: channel doping concentration $10^{15}$ cm$^{-3}$, TiN/HfO$_2$ gate insulator stack with equivalent gate oxide thickness $t_{\rm ox} = 1.7$ nm, fin width $W_{\rm fin} = 35$ nm, fin height $H_{\rm fin} = 65$ nm, and channel length $L = 60$ nm. Details for the device fabrication processes are presented elsewhere [39].

Figs. 6(a) and 7(a) present the measured transfer characteristics in linear and semi-logarithmic plots for $V_d = 0.1$ and 1 V and the output characteristics for different $V_g$ values. Good agreement between model results and experimental measurements in all operation regimes is obtained, using fixed values for the parameters: $c_1 = 3.5$, $\upsilon_{\rm sat} = 0.5 \times 10^7$ cm/s, $\theta_{1,0} = 0.26$, $V_E = 0.55$ V, $\Delta\varphi = 0.26$ V, $\mu_o = 150\,{\rm cm}^2/{\rm V}\cdot{\rm s}$, and $R_{\rm sd}W_{\rm fin} = 3.15 \times 10^{-4}\ \Omega\cdot{\rm cm}$. Figs. 6(b) and 7(b) show the $g_m$ versus $V_g$ and $g_d$ versus $V_d$ plots, respectively, derived from the experimental data of Figs. 6(a) and 7(b). The agreement between the experimental and modeled results is good, supporting the good accuracy of the compact model.

Summarizing all model parameters used to evaluate the predictive ability of the proposed unified drain-current model, in addition to the geometrical dimensions describing the device structure (see Fig. 1), a limited number of fitting parameters $(c_1, V_E, \mu_o, \theta_{1,0}, R_{\rm sd})$ is used. Generally, by comparing the model with simulation and experimental results, we found that the parameter $c_1$ controlling the transition from weak to strong inversion lies in the range of 2–3.5 in all devices and that $V_E$ controlling the CLM effect takes an average value of about 0.4 V for $L > 30$ nm and a much smaller value of about 0.005 V for $L \leq 30$ nm due to enhanced SCEs. It is mentioned that, based on the unified drain current (21) in the above-threshold region and at low drain voltage, the classical Y-function methodology [40] can be extended to extract the electrical parameters $V_t$, $\mu_o$, $\theta_{1,0}$ and $R_{\rm sd}$ of nanoscale TG FinFETs using the $I_d$–$V_g$ experimental data at low $V_d$. This will be the subject of our feature work. Using the extracted parameters $V_t$, $\mu_o$, $\theta_{1,0}$, and $R_{\rm sd}$ and the channel-length-dependent parameters $c_1$ and $V_E$, the transfer and output characteristics of short-channel FinFETs can be predicted with good accuracy.

## V. Assessing the Symmetry of the Compact Model

An important factor of any modern compact model is its continuous behavior in all regions of operation and its symmetry around $V_d = 0$ V. This behavior is important for analog design since it dictates the suitability of the device model for a plethora of circuit applications, which utilize the transistor in the linear region (filters, gain stages, and signal conditioning circuits). Old models (such as the BSIM model) lacked this symmetry, a limitation that was manifesting itself as an undesirable (and non physical) behavior of their intermodulation products (IM3) and an erroneous third point intercept (IIP3) estimation. Because this behavior is extremely important to any wideband system, as most of modern telecommunication standards operate, it is necessary to assess the models' linearity behavior. This is possible by implementing the circuit shown in Fig. 8(a). This includes three devices: M1 and M2 operate in saturation and form a differential stage while they produce the system-desired input gain together with the appropriate scaled resistors. While M3 is in the linear region acting as an output load (for example,

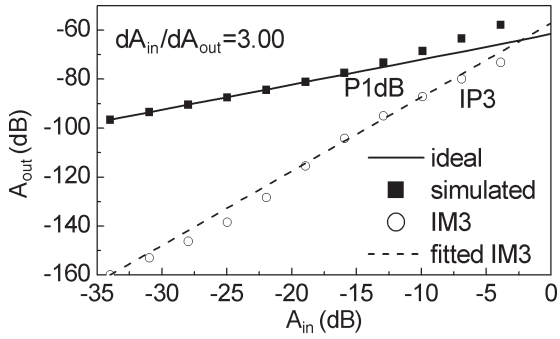


Fig. 9. IIP3 simulation response of the main and intermediation products for a sweep of input power, assessing the linearity of the model (good accordance to the IM3 slope being three times the slope of the main tones and a 9.6-dB difference of the P1dB point to the third intercept point).

the input resistance of a MOSFET-C filter), all other circuit components are of a passive nature, to ensure we assess the transistor linearity. The signal that drives the circuit consists of two sine waves of equal amplitude at two slightly different frequencies ($f1$ and $f2$). The output of this circuit is schematically shown in Fig. 8(b), where the output IM3 product tones are introduced because of the nonlinear ties of the system. Fig. 9 shows the simulated results of the output amplitude in decibels (T1 and T2 are equal due to the symmetry of the circuit and the frequency ranges used), whereas the IM3 products are also shown. The output signal shows the desired linear characteristic (until the system starts saturating, the P1dB point where the distance from the ideal response is 1 dB indicates the end of the circuit's usable range.

The IM3 products are following a linear behavior in decibels (although the devices move from weak to strong inversion) with a ratio of (exactly) 3, compared with the main products. This is the expected response of the IM3 products (and is not observable in a BSIM-based circuit), whereas third intercept point (IP3) is indeed 9.6 dB higher than the P1dB point, as it is expected. This shows that the proposed model is indeed linear for the desired simulation setup demanding such linearity.

## VI. Conclusion

An analytical and compact drain current–voltage model for undoped (or lightly doped) short-channel TG FinFETs, accounting for small-geometry effects and QMEs, is presented. The model is an extension of the compact model for DG FinFETs with increasing the channel width by the top-gate width and incorporating the effect of the top gate on the SCEs through the threshold-voltage modeling. The proposed model has been validated by device simulations in all regions of operation with simulated and experimental results. The symmetry of the model and its good level of accuracy make the model suitable for implementation in circuit simulation tools.

## Acknowledgment

The authors would like to thank N. Collaert from IMEC (Leuven) for providing the samples.

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