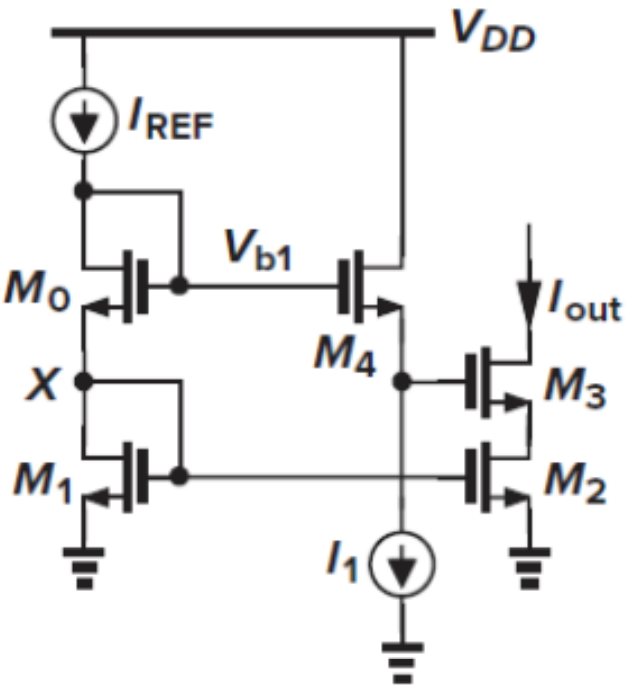
Q1.



(a)

Assume the body effect is ignored,

$$R_{out} = r_{o2} + r_{o3} + g_{m3} r_{o3} r_{o2}$$

(b)

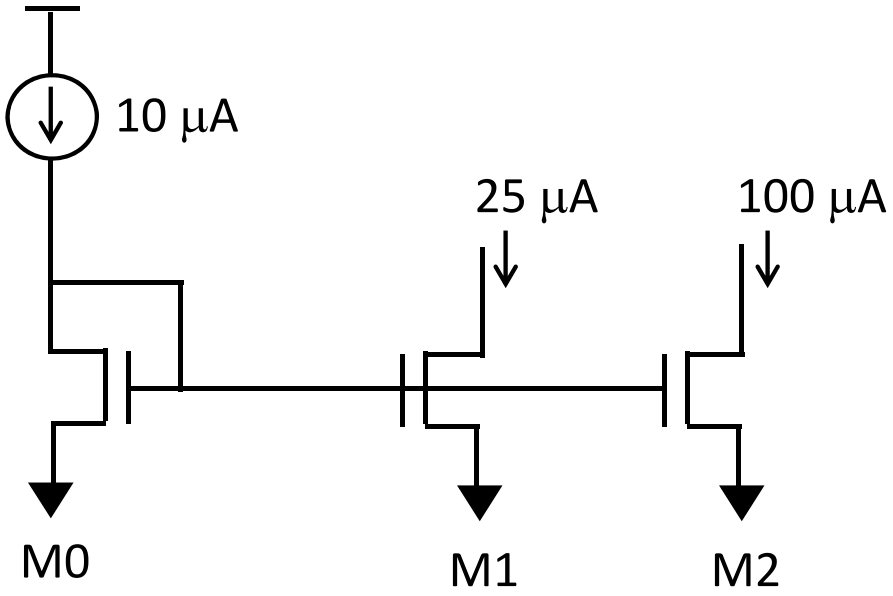
M4: 為了使Vout可以達到min(Vout)=2Vov，不能直接將V_{b1} (2Vth+2Vov)接到M3的gate node (Vout=Vth+2Vov)。故而使用M4提供一個level shift (Vth)，輸出即可低至2Vov。

I1: 即是提供M4偏壓所需的電流，通常是使Vgs4~Vth4

(c)

1. 使用通道很長的電晶體，但輸出寄生電容會大增
2. 使用更多個電晶體做疊接(cascode)，但Vout會增加
3. 使用回授電路，可以參考Lectures，但注意穩定性問題

Q2.



(a)

$$i_D = \frac{1}{2}K'\left(\frac{W}{L}\right)V_{ov}^2$$

$$10u = 0.5*100u*(0.2)^2*(\mathrm{W/L})_0$$

$$\Rightarrow (\mathrm{W/L})_0 = 5$$

Using L=4um for avoid CLM,

For M0, W=10u, L=4u, m=2

For M1, W=10u, L=4u, m=5

For M2, W=1ou, L=4u, m=20

(b)

Length很大，會使Width跟著增加，面積很大。另外，M1 and M2 drain node的寄生電容跟著增加，對頻率響應會有影響。

可以使用cascode方式疊接電晶體，雖然輸出電壓會上升，但輸出電阻可以增大許多，電晶體面積會縮小許多。

Q3.

(a)

$$V_{REF} = \alpha \cdot \left(V_{PTAT} + kV_{CTAT} \right)$$

$$\left. \frac{\partial V_{REF}}{\partial T} \right|_{T=T_0} = \frac{\partial V_{PTAT}}{\partial T} + k \frac{\partial V_{CTAT}}{\partial T} = 0$$

$$k = -\left(\frac{\partial V_{CTAT}}{\partial T} \right)^{-1} \left(\frac{\partial V_{PTAT}}{\partial T} \right) \Bigg|_{T=T_0}$$

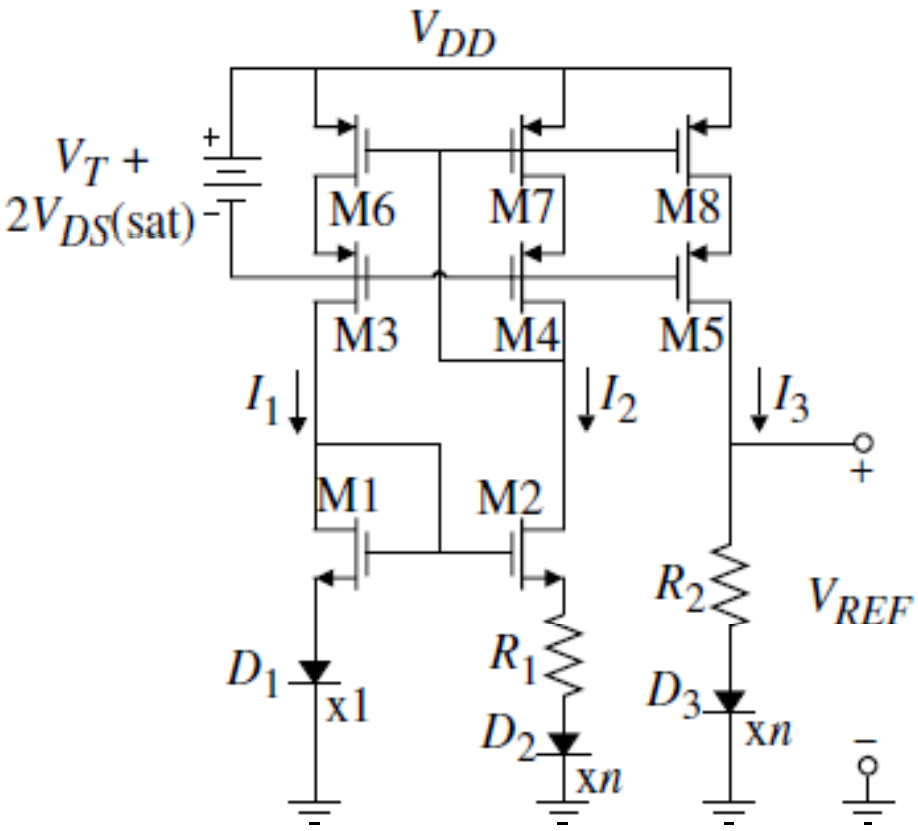
(b)

As the right schematic,

V_{CTAT} is the voltage across a diode

V_{PTAT} is the difference of two voltages across two diodes

(c)

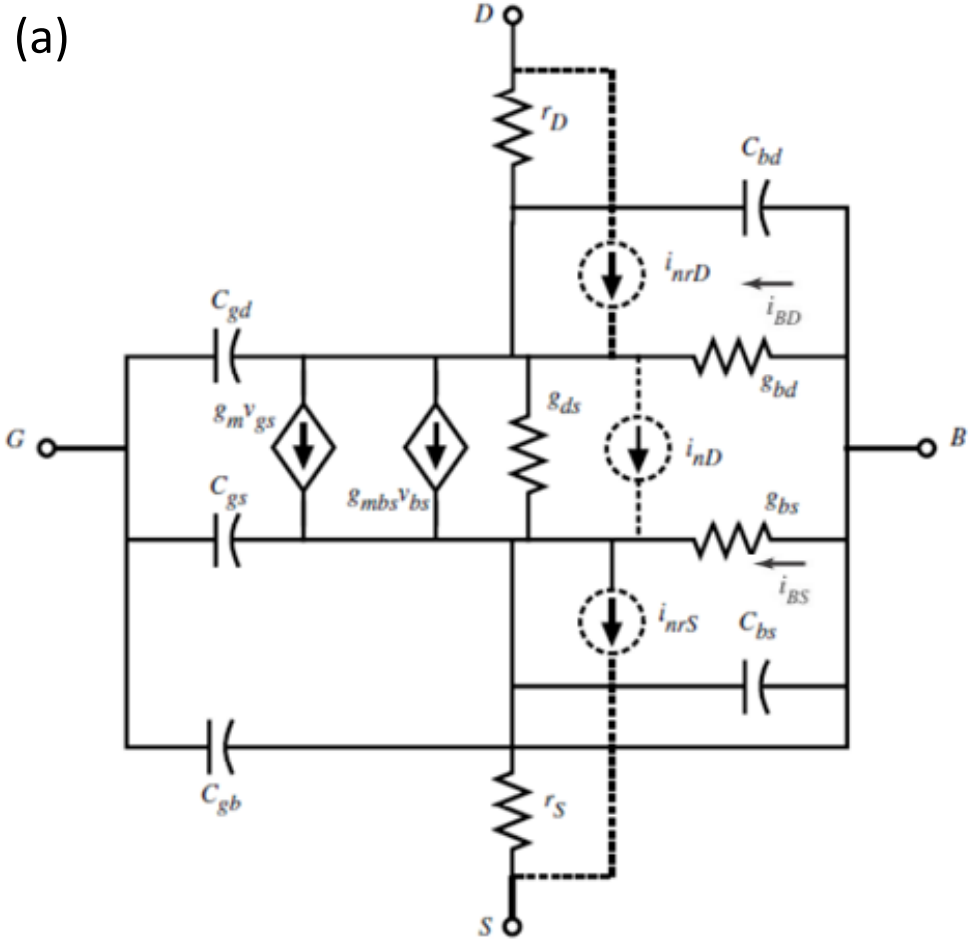


$$V_{REF} = V_{D3} + I_3 R_2 = V_{D3} + \frac{R_2}{R_1} V_t \, ln(n)$$

$$= V_{CTAT} + \frac{R_2}{R_1} ln(n) V_{PTAT}$$

Q4.

(a)



(b)

1. 通道調變效應 (channel length modulation)

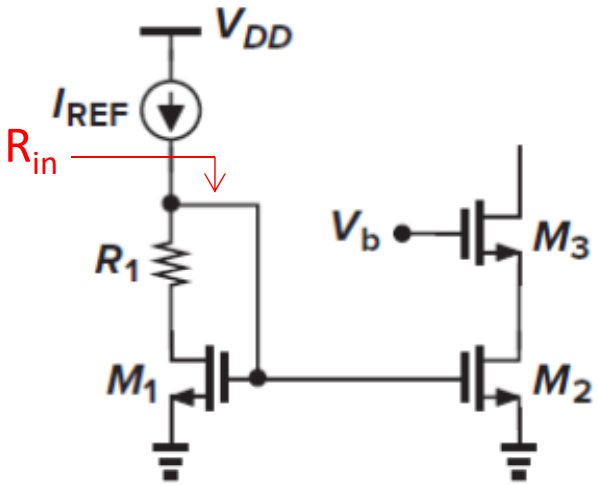
CLM is a shortening of the length of the inverted channel region with increase in drain bias for large drain biases. The result of CLM is an increase in current with drain bias and a reduction of output resistance.

2. 基底效應 (body effect)

The body effect is the change in the threshold voltage by an amount approximately equal to the change in the source-bulk voltage, V_{SB}, because the body influences the threshold voltage (when it is not tied to the source). Its root cause is that charges originally existed in the channel region are changed by V_{SB}.

Q5.

(a) R_1 是用來降低V_{DS} of M_1 來使M1與M2有相同的V_{DS} 進而減少通道長度調變效應對這個current mirror的影響



(b) Rin ~ $1/g_{m1}$。

(c) V_{b1} = 2Vth+2Vov
V_b = Vth+2Vov
Min(Vout) ~ 2Vov