2023 Computer Organization - ET3502701
Final Examination

Name: _____ ID: _____

1. (5%) Would you please explain why ARM proposes big-LITTLE technology in terms of power consumption?

2. (10%) Why do the control signals have to traverse through the following pipeline stages?

3. (10%) Please give an example to explain how the cache write-back policy can reduce the number of DRAM accesses.

4. (10%) Why should we employ dynamic scheduling in processor designs?

5. (10%) Please explain why a 2-bit predictor can reduce the misprediction rate for certain situations.

6. (10%) Why is the cache miss ratio of the I-cache always lower than that of the D-cache?

7. (5%) What is speculation, and how does it differ from prediction?

8. (5%) What are early restart and critical-word-first?

9. (5%) Why does Translation Lookaside Buffer (TLB) have a good locality?

10. (5%) What is superscalar and what is superpipeline?

11. (10%) Please explain the **write-through** and **write-back** for the cache mechanism. Will it be used for the case of a cache read miss?

12. (5%) Is it possible to have TLB miss, Page Table miss, and Cache hit? Please explain.

13. (5%) Will conflict misses occur in a fully associative cache? Please explain why.

14. (5%) Why do we need to increase associativity when there are more cores in a multiprocessor with shared L2 or L3 cache?