電子學 (二) 期末考 Chapter 10, 11, 12.2~3, 13.2　　2021.6.16　13:20-15:10pm

(if not specified, $v_d = v_1 - v_2$, $v_{cm} = (v_1 + v_2)/2$ for differential amplifiers)

必須要有計算過程。

1. (18%) Consider the Widlar current-source circuit with multiple output transistors shown in Figure 1. Assume $V_{BE1}(\text{on}) = 0.7$ V, $R_1 = 20$ kΩ, and all base currents are negligible . (a) Find the value of I_{REF}(4%). (b) Determine values of R_{E2} such that $I_{O2} = 20\ \mu$A (4%). (c) Determine the value of I_{O3} if $R_{E3} = 2$ kΩ(5%). (d) Assuming that $\beta = 120$ and $V_A = 100$ V, what is the output resistance of this circuit (equivalent resistance looking into the collector of transistor Q_3)(5%)?

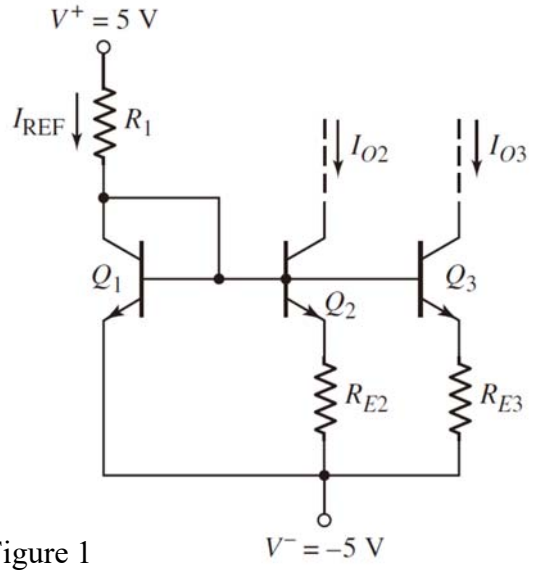

Figure 1

2. (15%) The parameters of the transistors in Figure 2 are $V_{TN} = 0.6$ V, $V_{TP} = -0.6$ V, $k_n' = 80\ \mu\text{A/V}^2$, $k_p' = 40\ \mu\text{A/V}^2$, and $\lambda_n = \lambda_p = 0.02\ \text{V}^{-1}$. The width-to-length ratios of M_1 and M_2 are 50, and those of all other transistors are 100. The values of V_{GSQ} is such that $I_{DQ1} = 80\ \mu$A, and all transistors are biased in saturation region. (a) Determine the effective resistance looking into the drain of M_3. (b) Determine the small signal voltage gain $A_v = v_o/v_i$. (c) What is the possible highest value of the output voltage V_O.

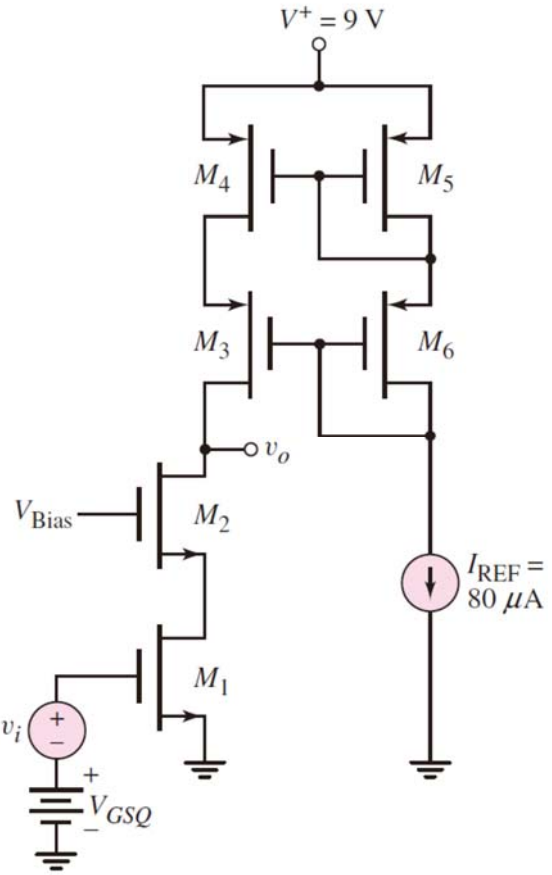

Figure 2

3. (17%) For the transistors in the circuit in Figure 3, the transistor parameters are $K_n = 0.2\ \text{mA/V}^2$, $V_{TN} = 2\ \text{V}$, and $\lambda = 0.02\ \text{V}^{-1}$. (a) Determine the value of bias current I_Q (3%) and the output resistance looking into current mirror (4%). (b) Determine $A_d = v_{o2}/v_d$ (5%). (c) Determine $A_{cm} = v_{o2}/v_{cm}$ (5%).

4. (12%) Simplified input stage of uA741is shown in Figure 4. (a) Use BJT small-signal parameters such as β_n, β_p, $r_{\pi1}$~$r_{\pi4}$, g_{m1}~g_{m4} to write the equation of differential-mode input resistance R_{id} (6%). (b) If the supply voltage (V^+&V^-) of uA741 is changed from $\pm 15V$ to $\pm 5V$, will R_{id} become larger, smaller, or unchanged (2%)? Why (4%)?

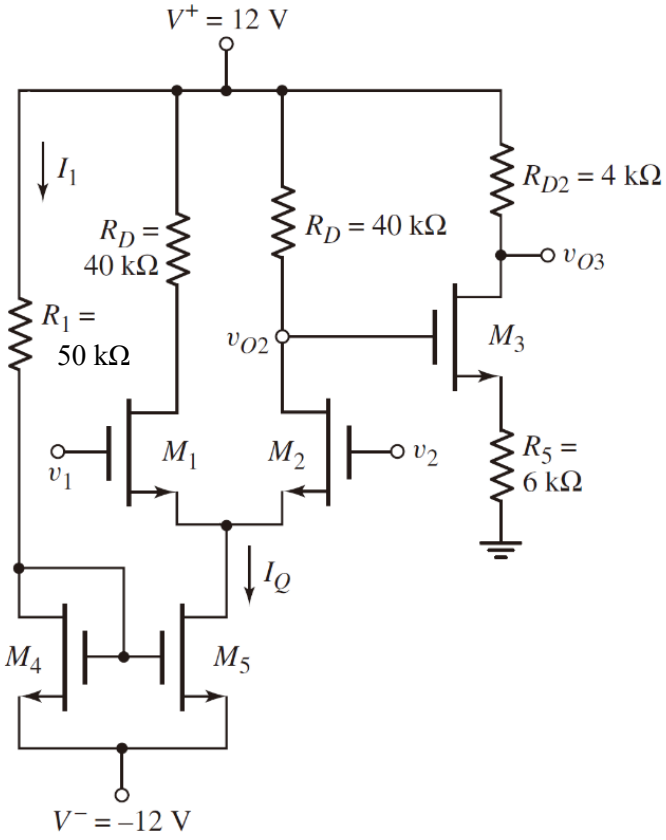

Figure 3

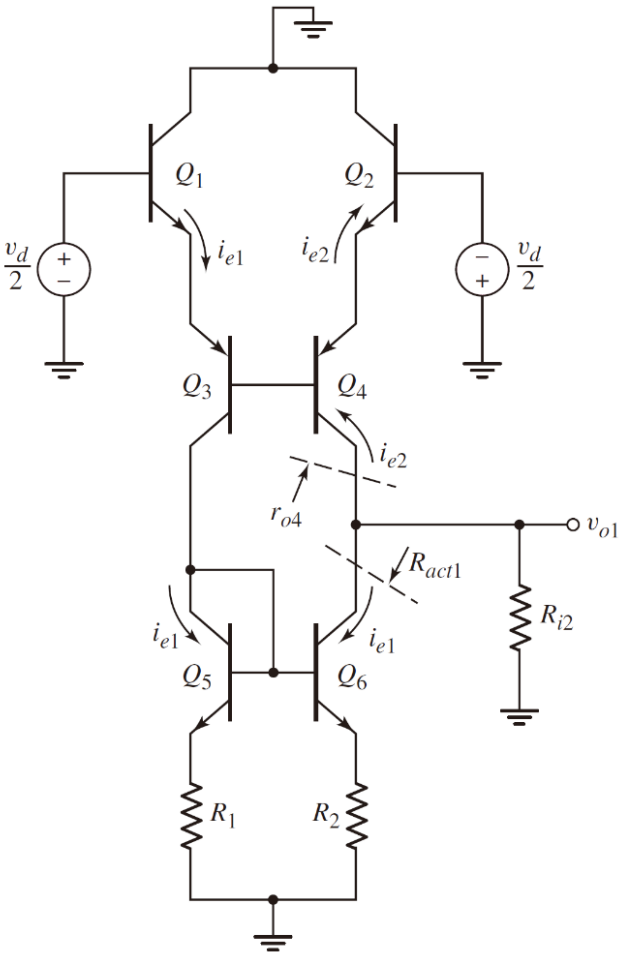

Figure 4

5. (20%) Consider the Darlington pair and output stage of the circuit in Figure 5. The parameters are $I_{C7} = I_Q = 0.4\ \text{mA}$, $I_{C8} = 2\ \text{mA}$, $R_4 = 5\ \text{k}\Omega$, $R_3 = 0.1\ \text{k}\Omega$, $\beta = 100$ for all transistors and early voltages $V_A = 80\ \text{V}$ for Q_1~ Q_7 and Q_{11}. (a) Calculate the small-signal voltage gain of the differential amplifier ($A_{v1} = v_{o2}/v_d$). (b) Determine the input resistance of the Darlington pair R_i. (c) Calculate the small-signal voltage gain of the Darlington pair ($A_{v2} = v_{o3}/v_{o2}$). (d) Find the output resistance (R_o).

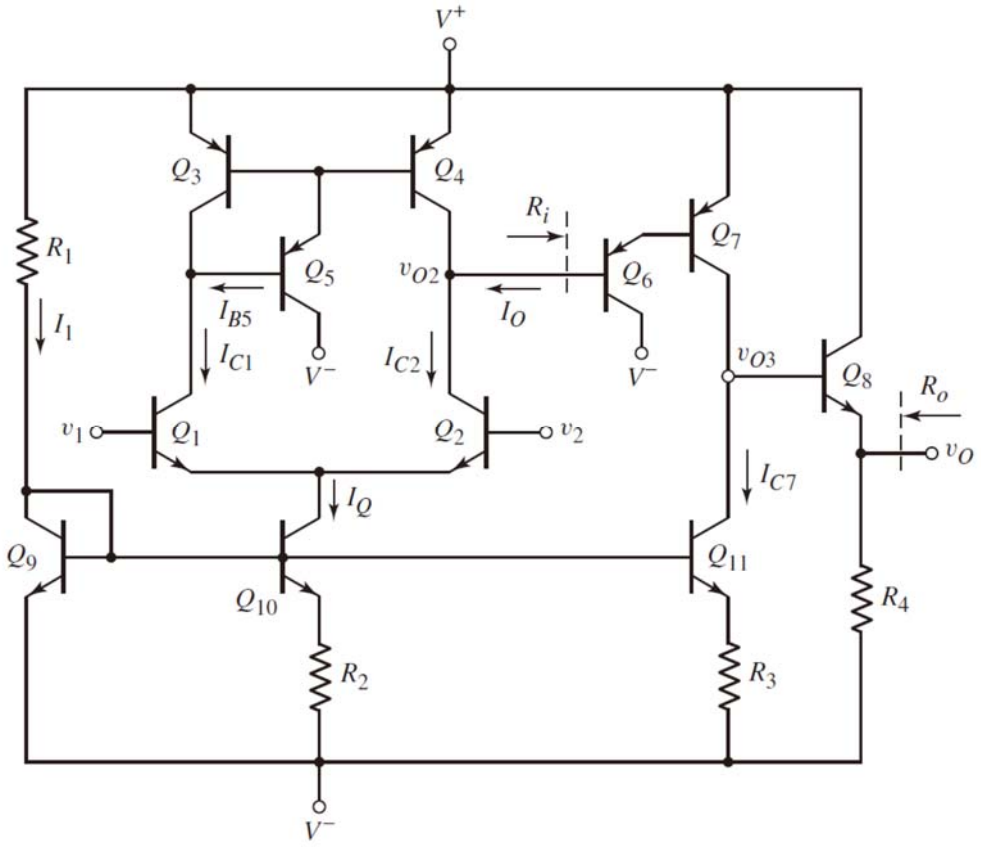

Figure 5

6. (12%) Two feedback configuration are shown in Figure 6. The close-loop gain is $A_{vf} = v_o/v_i = 20$ for both circuits. (a) Determine β_1 and β_2. (b) For both circuits, estimate the percent change in the close-loop gain for both configuration if A_2 is decreases by 10%.

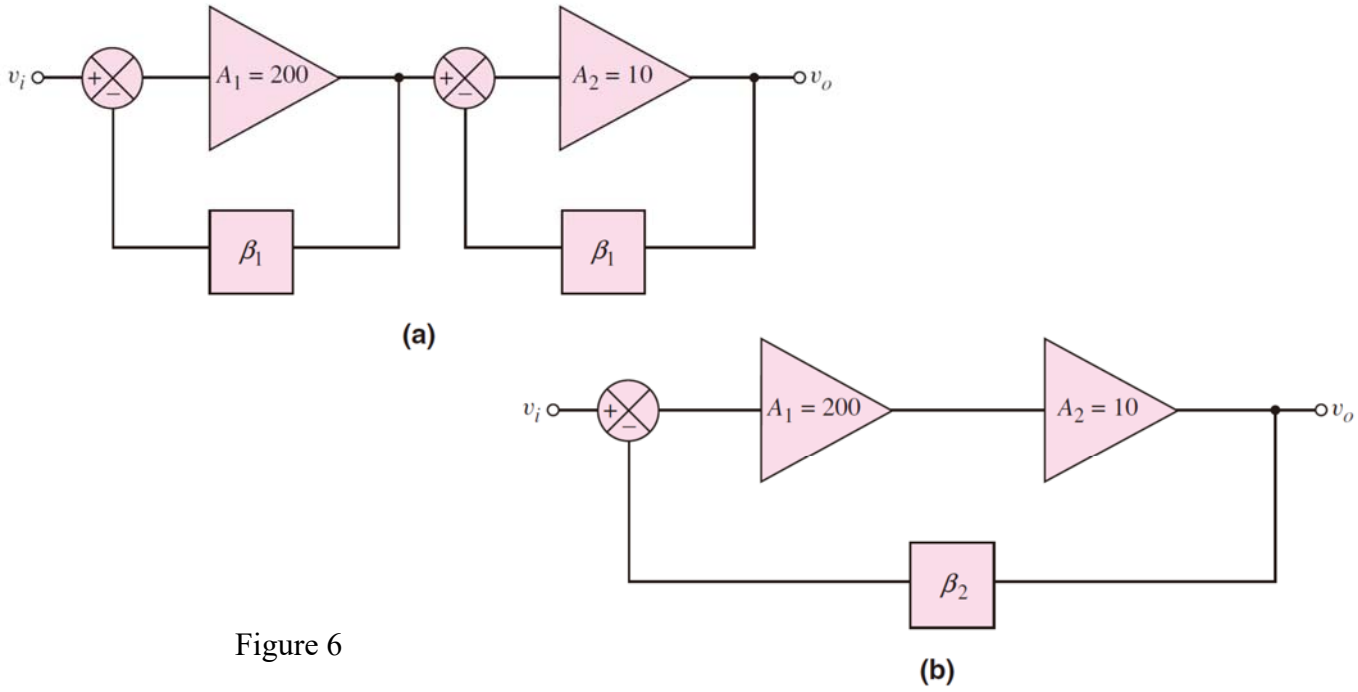

Figure 6

7. (6%) What kind of feedback configuration is this (2%)? Why (4%)?

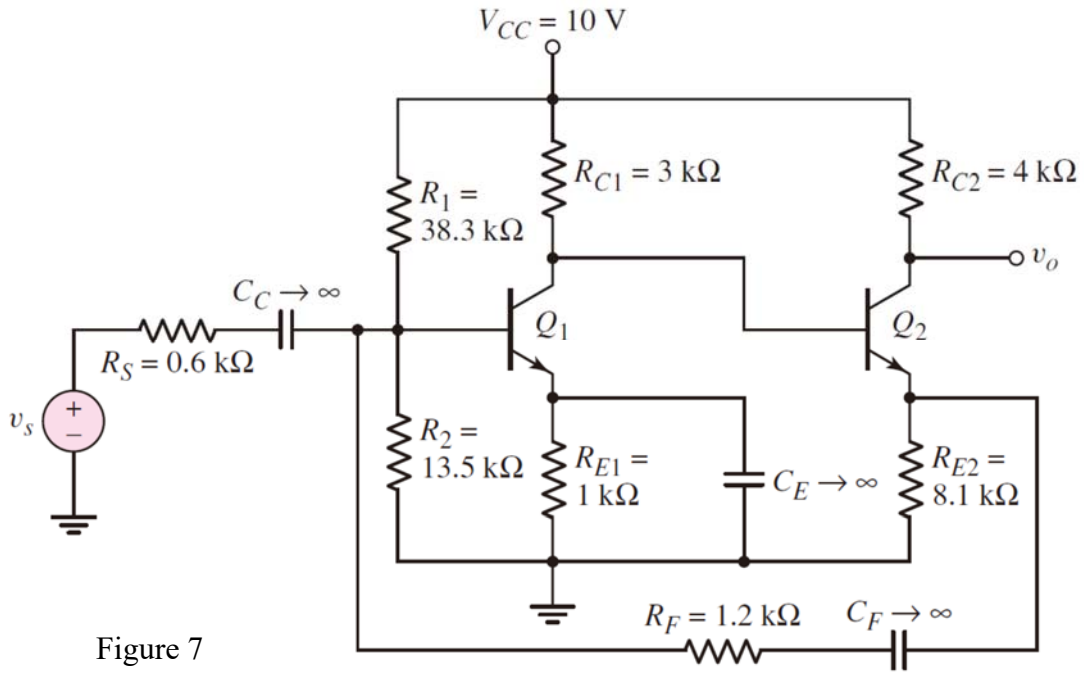

Figure 7

Stay home! Stay safe!