TAIWAN TECH National Taiwan University of Science and Technology

Analog Integrated Circuit Design and Applications

Spring 2024

Nanometer Design Studies

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Outline

- Transistor Design Considerations
- Deep-Submicron Effects
- Transconductance Scaling
- Design for Nanometer Transistors
- Opamp Design Examples
- Summary

- In chapter 17, we have studied some second order effects.
- In this lecture, we try to get something more!!

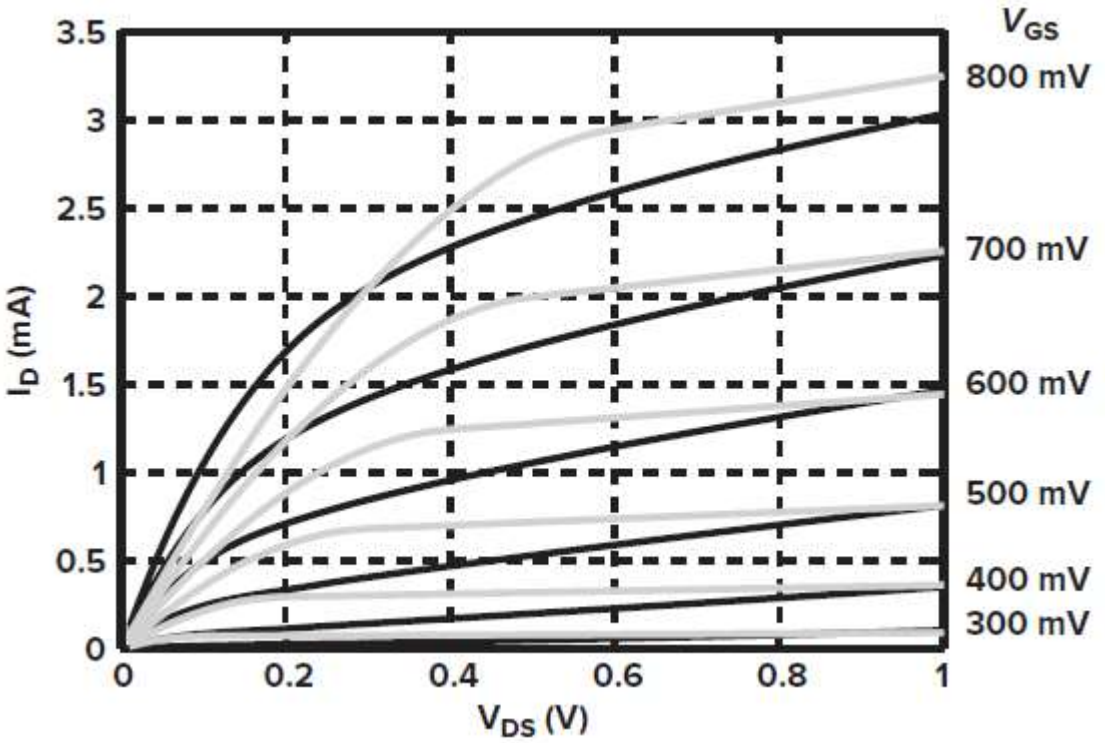
Nanometer Design Concept

- Conventional Design Concept
  - Using long-channel current equation to calculate the required bias and small-signal parameters
  - But, this is invalid for advanced CMOS process

- New Design Concept
  - Since current equation is not valid, only use it as a conceptual observation and direction
  - Using models in PDK to yield several curves for different conditions
  - For example, gm/Id design concept

Transistor Design Considerations

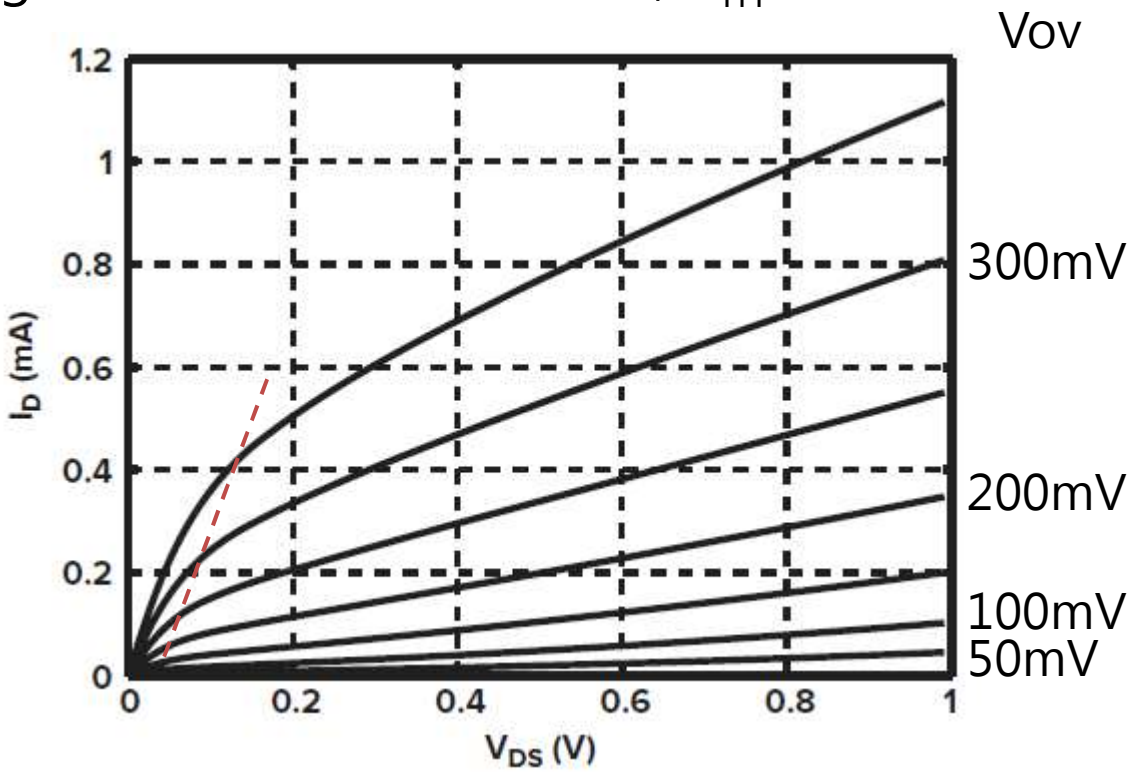
V_{GS} is ranged from 300mV to 800 mV, V_{TH}~300mV



- A 5μm/40nm device,
- **Black line**: Actual current model
- **Gray line**: Square-law current model

Transistor Design Considerations

V_{GS}-V_{TH} is ranged from 50mV to 350 mV, V_{TH}~200mV

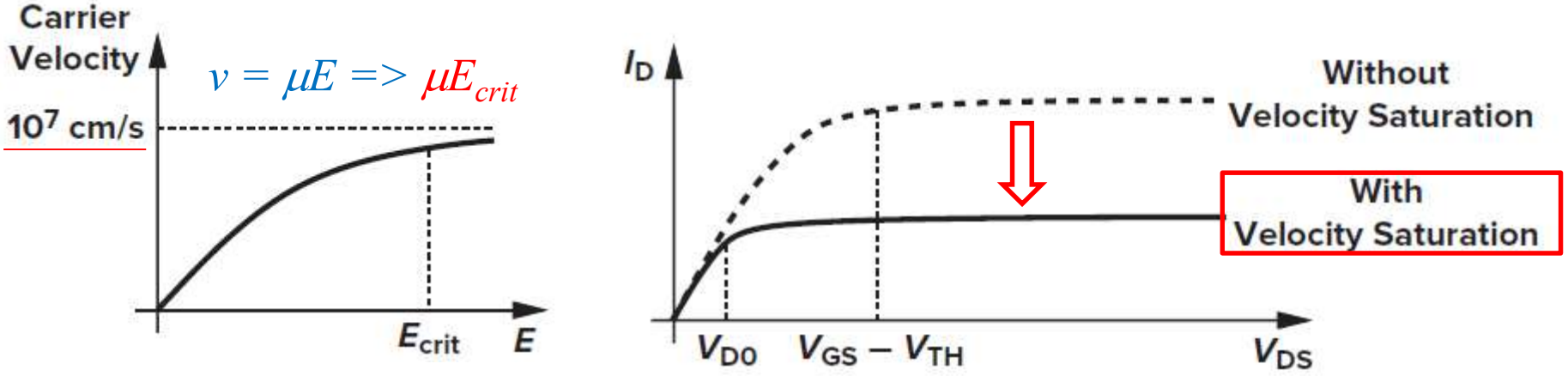


Triode or saturation region?

Deep-Submicron Effects

Velocity Saturation

Channel length: 1μm => 40nm (1/25), but VDD: 5V => 1V (1/5)



- **Velocity Saturation**: In a MOSFET, as V_{DS} and hence the electronic field along the source-drain path increase, the drift velocity (v) does not rise proportionally

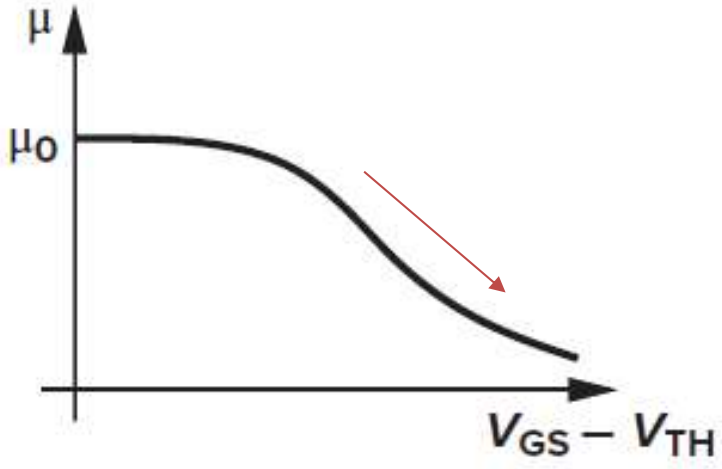
$$I = Q_d \cdot v = WC_{ox}\left(V_{GS} - V_{TH}\right)v_{sat}$$

Q_d is the charge density (per unit length)

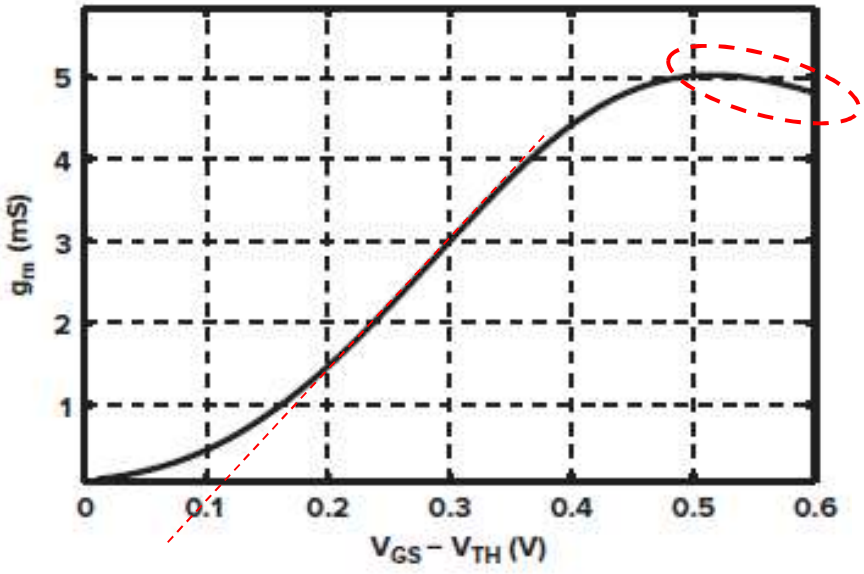
$$g_m = \left.\frac{\partial I}{\partial V_{GS}}\right|_{V_{DS},const} = WC_{ox}v_{sat}$$

Mobility Degradation with Vertical Field

– The mobility of the charge carriers in the channel also declines as the gate-source voltage and the vertical field increase



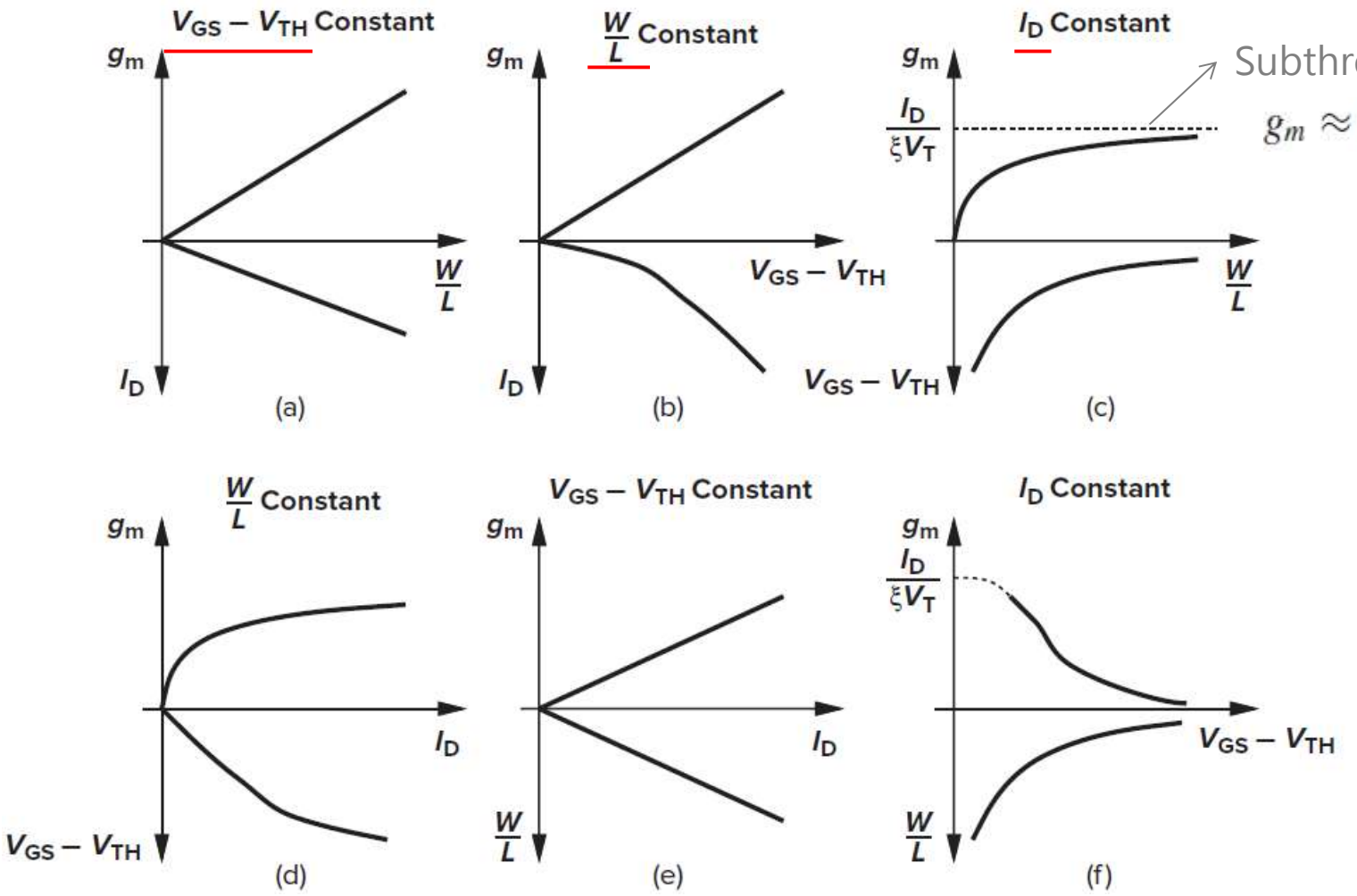
Example 11.1 shows the declined g_m for large V_{GS}-V_{TH}



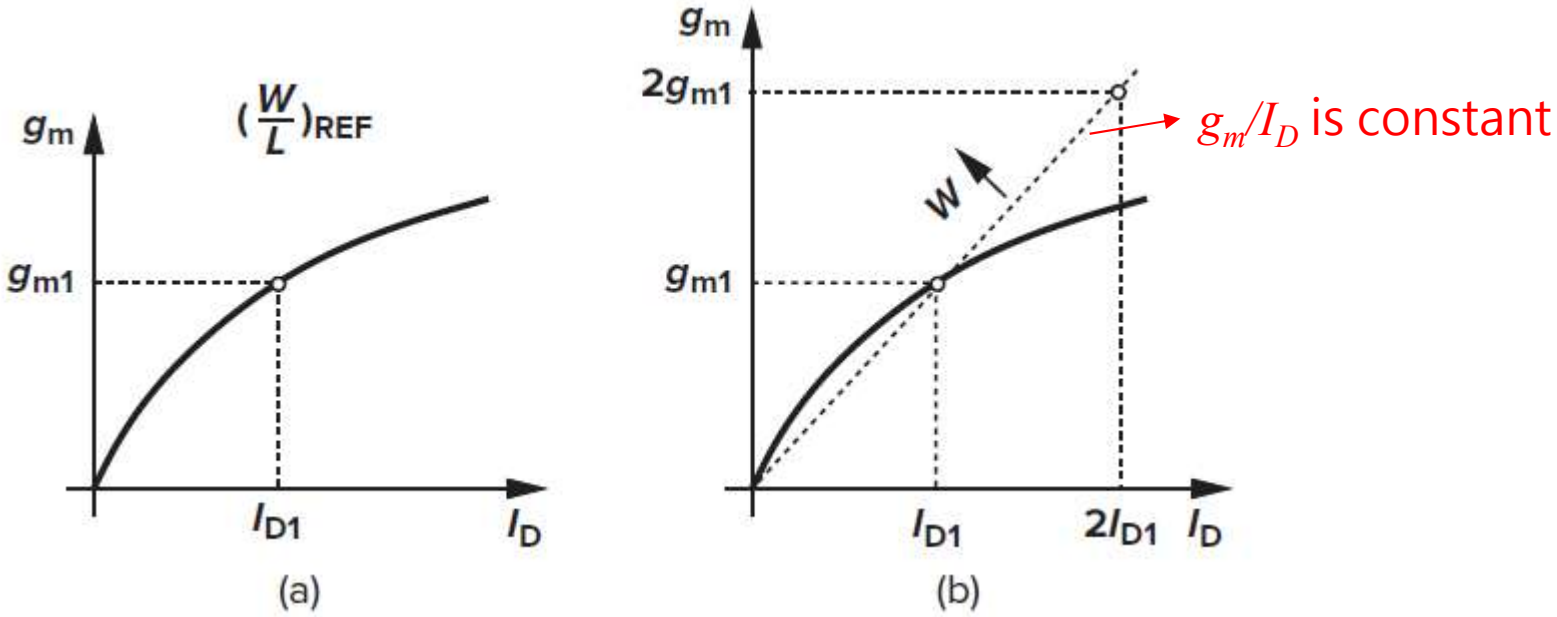
$$g_m = \mu_n C_{ox} \frac{W}{L}\left(V_{GS} - V_{TH}\right)$$

Transconductance Scaling

$$g_m = \mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{TH}) = \sqrt{2\mu_n C_{ox}\frac{W}{L}I_D} = \frac{2I_D}{V_{GS}-V_{TH}}$$

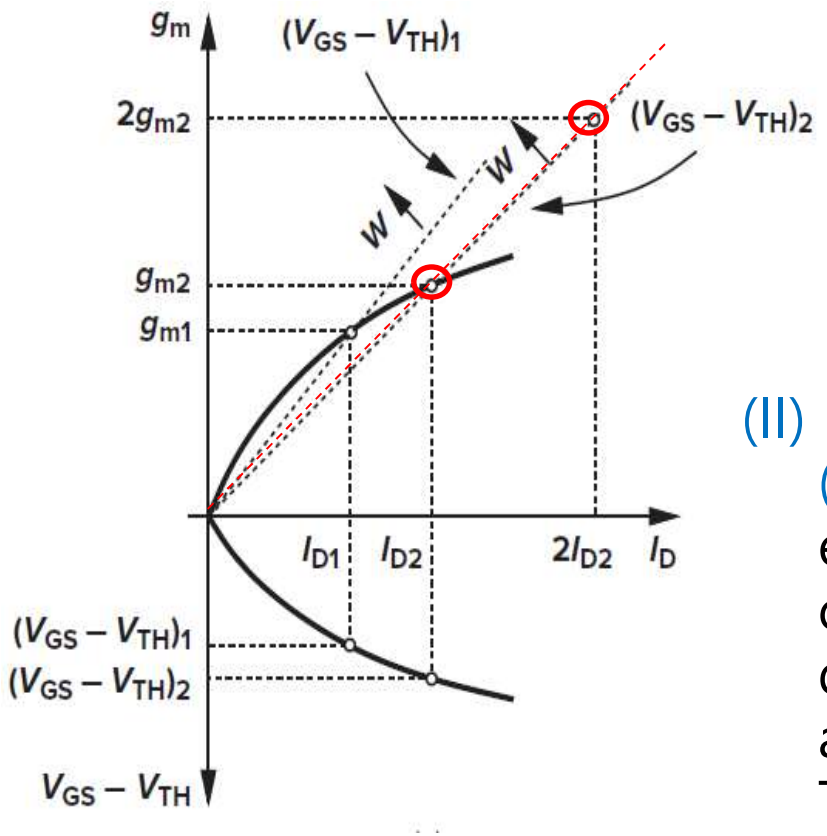


Example 11.3



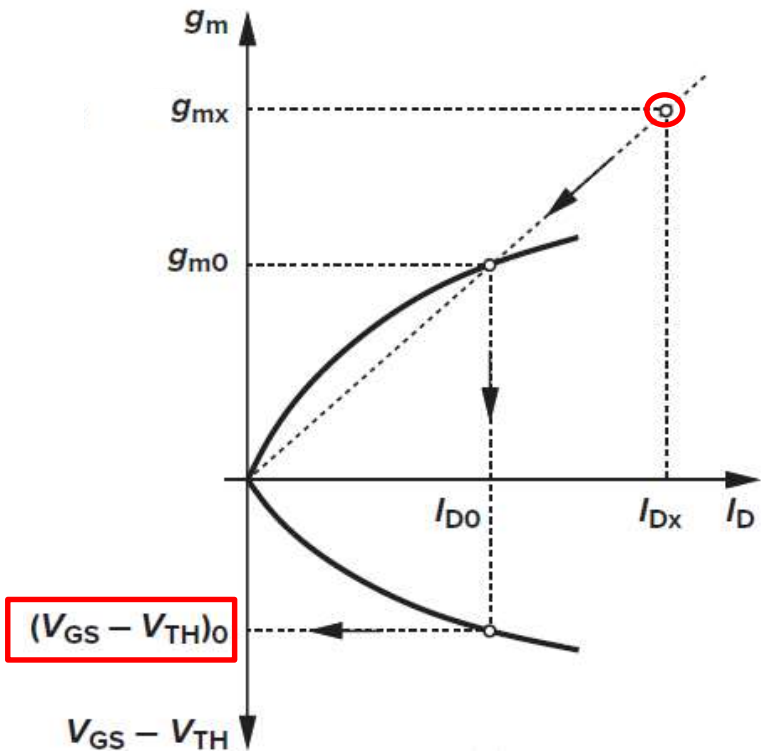
(I) With a constant $V_{GS}-V_{TH}$, doubling the width also doubles the transconductance and the drain current (Example 11.2). Since g_m/I_D is constant, to obtain this point on the g_m-I_D plane, we pass a straight line through the origin and (I_{D1}, g_{m1}), continuing to reach ($2I_{D1}$, $2g_{m1}$) [Fig. 11.9(b)]. Thus, all (I_D, g_m) combinations resulting from the scaling of W fall on this line if the overdrive is fixed.

Example 11.3



(II) If we begin with a greater overdrive, $(V_{GS}-V_{TH})_2$, (I_D, g_m) point is located elsewhere, at (I_{D2}, g_{m2}), on the characteristic [Fig. 11.9(c)]. We again draw a straight line through the origin and (I_{D2}, g_{m2}) and continue to $(2I_{D2}, 2g_{m2})$. Thus, each such line in the g_m-I_D plane represents the possible (I_D, g_m) combinations that can be obtained by scaling W for a given overdrive

Example 11.3



(III) We draw a line through the origin and the point (I_{Dx}, g_{mx}) [Fig. 11.9(d)]. The intersection of the line and the g_m plot yields a "reference" point specifying the proper overdrive voltage, $(V_{GS}-V_{TH})_0$, and an acceptable (I_D, g_m) combination, (I_{D0}, g_{m0}). If the width is scaled up by a factor of g_{mx}/g_{m0} $(=I_{Dx}/I_{D0})$, and the overdrive remains equal to $(V_{GS}-V_{TH})_0$, then the desired transconductance and current are obtained

Transistor Design

A typical transistor design problem specifies one of three (I_D, g_m and $V_{DS,min}$) and seeks the other two then **W/L**

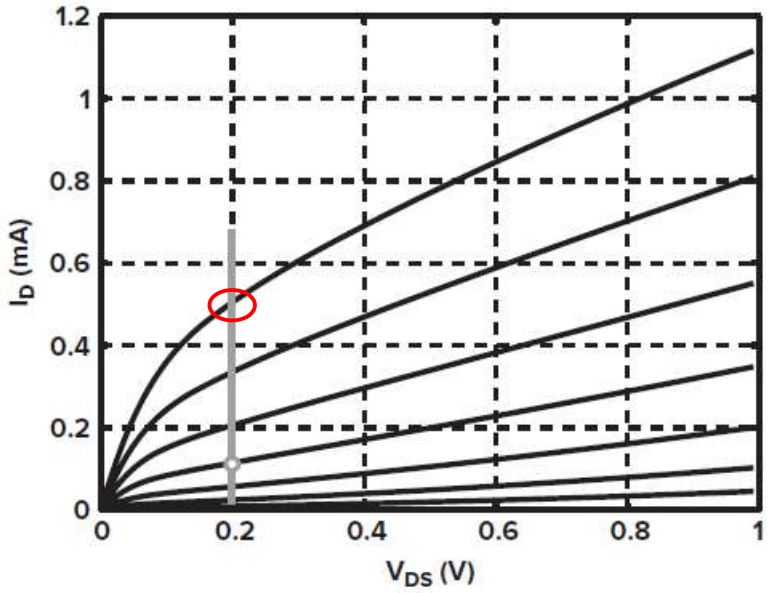
- Design for Given I_D and $V_{DS,min}$
- Design for Given I_D and g_m
- Design for Given g_m and $V_{DS,min}$
- Design for a Given g_m

$$g_m = \mu_n C_{ox}\left(\frac{W}{L}\right)V_{DS,min}$$
$$= \sqrt{2\mu_n C_{ox}\left(\frac{W}{L}\right)I_D}$$
$$= \frac{2I_D}{V_{DS,min}}$$

Table 11.1 Three scenarios encountered in transistor design.

	Case I	Case II	Case III
Given	I_D, $V_{DS,min}$	g_m, I_D	g_m, $V_{DS,min}$
To Be Determined	$\frac{W}{L}$, g_m	$\frac{W}{L}$, $V_{DS,min}$	$\frac{W}{L}$, I_D
Design Revision	g_m insufficient; Raise I_D and $\frac{W}{L}$	$V_{DS,min}$ too large; Raise $\frac{W}{L}$	I_D too large; Raise $\frac{W}{L}$; Lower $V_{GS} - V_{TH}$

1. Design for Given I_D and $V_{DS,min}$



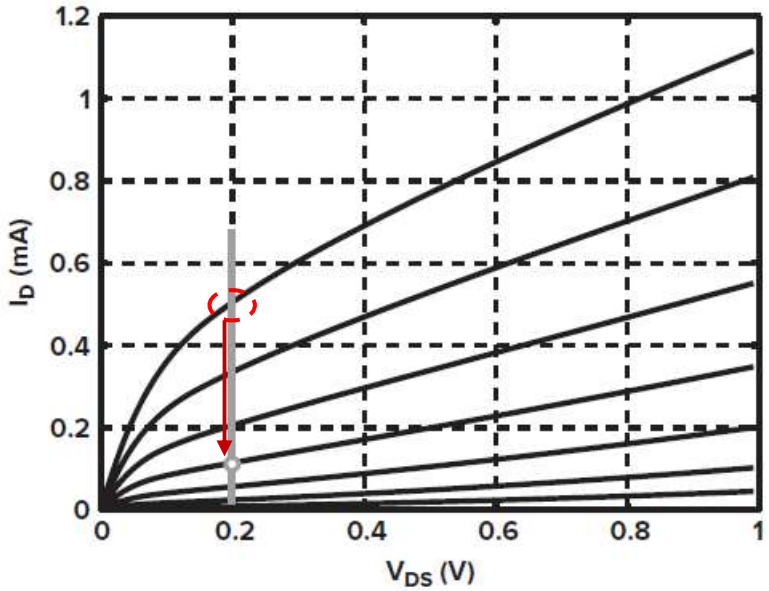
$I_D = 0.5$ mA and
$V_{DS,min} = 200$ mV

Step 1 Select a "reference" transistor, with a width W_{REF} and a length equal to the minimum allowable value, L_{min} (e.g., $L_{min} = 40$ nm). Let us choose $W_{REF} = 5\ \mu$m as an example.

Step 2 Using the actual device models and a circuit simulator, plot the I_D-V_{DS} characteristics of the reference transistor for different values of $V_{GS} - V_{TH}$. In typical analog circuits, $V_{GS} - V_{TH}$ ranges from about 50 mV to about 600 mV. We can therefore construct the characteristics with the overdrive incrementing in steps of 50 mV.[4] Figure 11.10 shows the results for $W_{REF}/L_{min} = 5\ \mu$m/40 nm. (Here, $V_{GS} - V_{TH}$ increments from 50 mV to 350 mV for clarity.)

在先進製程中，作圖是一件重要且必要的事!!

1. Design for Given I_D and $V_{DS,min}$



$I_D = 0.5$ mA and
$V_{DS,min} = 200$ mV

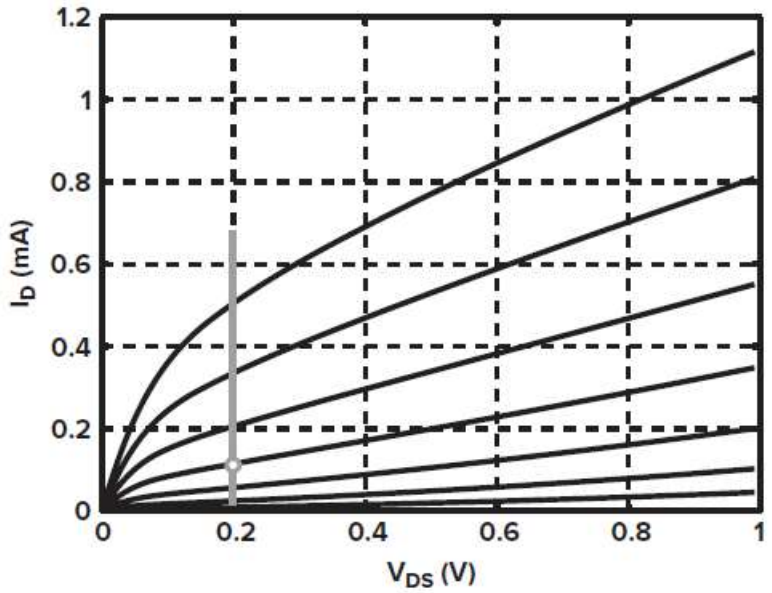
V_{GS}-V_{TH}=200mV

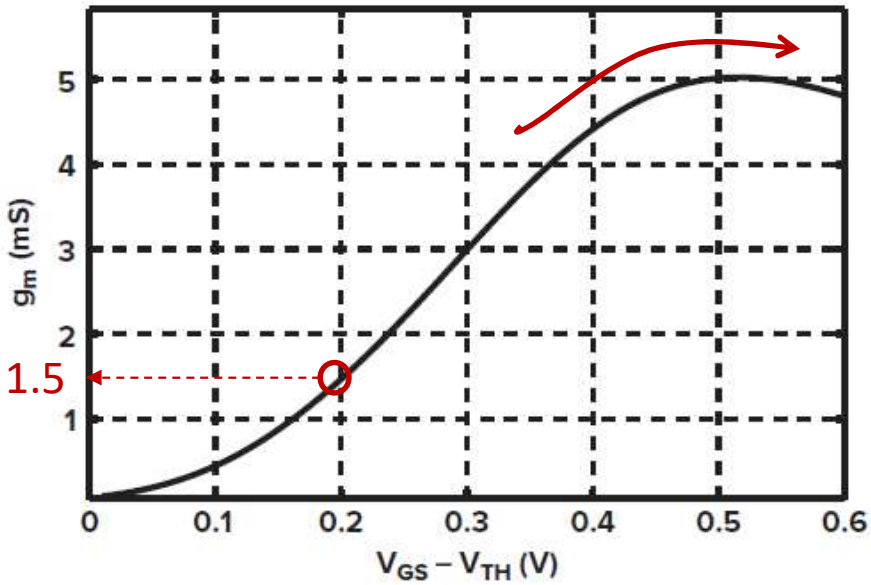
Step 3 Bearing in mind that our example specifies $I_D = 0.5$ mA and $V_{DS,min} = 200$ mV, we draw a vertical line at $V_{DS} = 200$ mV (Fig. 11.10) and find its intersection with the plots. Which plot should we select? If the device obeyed the square law, we would choose the plot for $V_{GS} - V_{TH} = V_{DS,min} = 200$ mV. However, the short-channel device remains in saturation even for $V_{GS} - V_{TH} = 350$ mV at $V_{DS} = 200$ mV. The situation is therefore more complex, but let us proceed with $V_{GS} - V_{TH} = 200$ mV for now.

Step 4 The foregoing procedure has yielded, for the reference transistor, one operating point that satisfies the V_{DS} requirement. The drain current, $I_{D,REF}$, however, may not be close to the necessary value, 0.5 mA in our example. What shall we do here? We must now *scale* the width of the transistor and hence its drain current. Since in Fig. 11.10, $I_{D,REF} \approx 100\ \mu$A, we choose a transistor width of $(500\ \mu\text{A}/100\ \mu\text{A}) \times W_{REF} = 5W_{REF} = 25\ \mu$m.

使用較小的參考電流產生偏壓!!

1. Design for Given I_D and $V_{DS,min}$

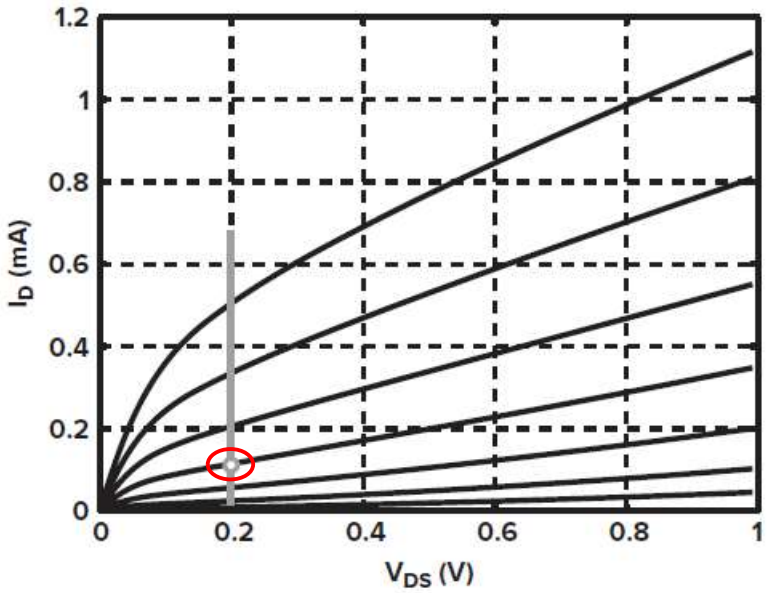


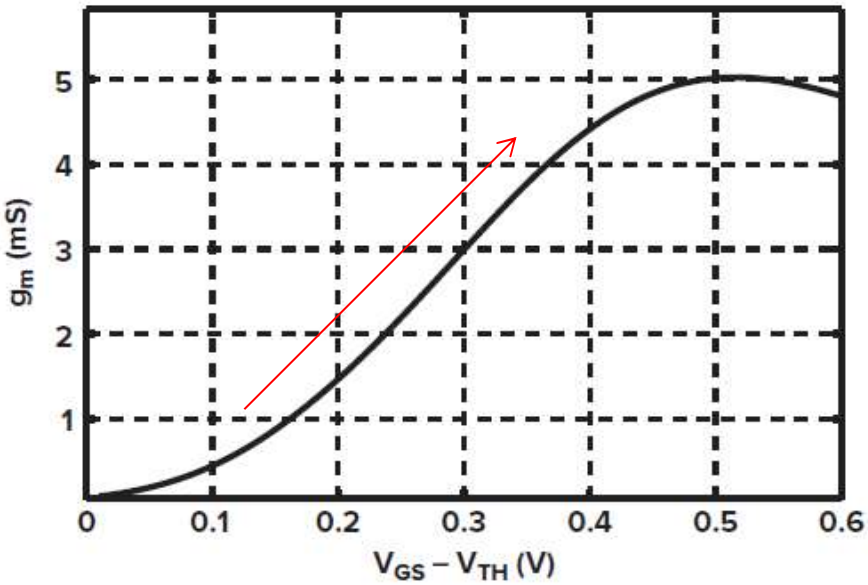


An Example: Current ↑, W↑ → g_m↑

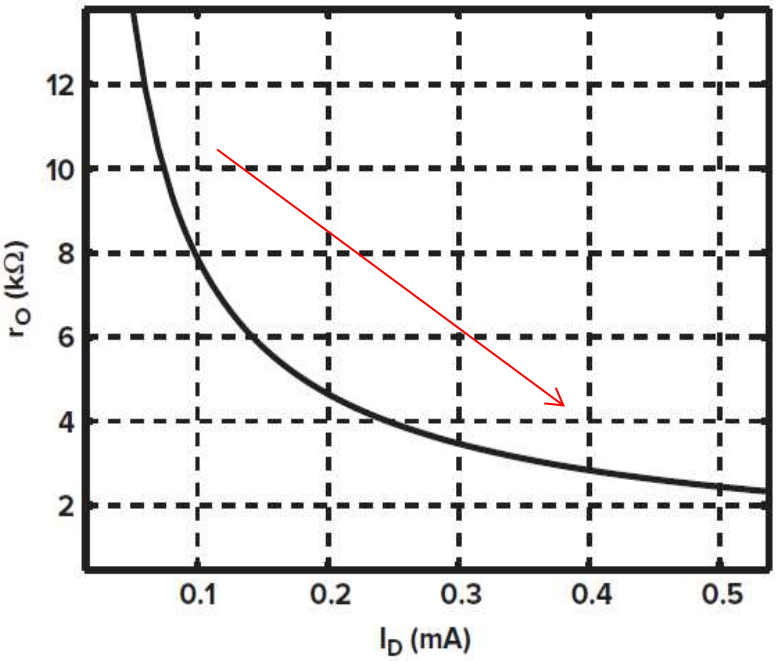
Can we choose a higher overdrive voltage in Fig. 11.10? Suppose we select $V_{GS} - V_{TH} = 250$ mV, obtaining $I_D = 200\ \mu$A for the reference transistor and a transconductance of about 2.3 mS from Fig. 11.11. If scaled up to 12.5 μm so as to carry 500 μA, the transistor exhibits a transconductance of 2.5×2.3 mS $= 5.75$ mS, a value *less* than that observed in the previous case (7.5 mS). This occurs because $g_m = 2I_D/(V_{GS} - V_{TH})$ in saturation. To obtain a high transconductance, therefore, we typically choose $V_{GS} - V_{TH} \approx V_{DS,min}$ even though it translates to a wider transistor.

1. Design for Given I_D and $V_{DS,min}$

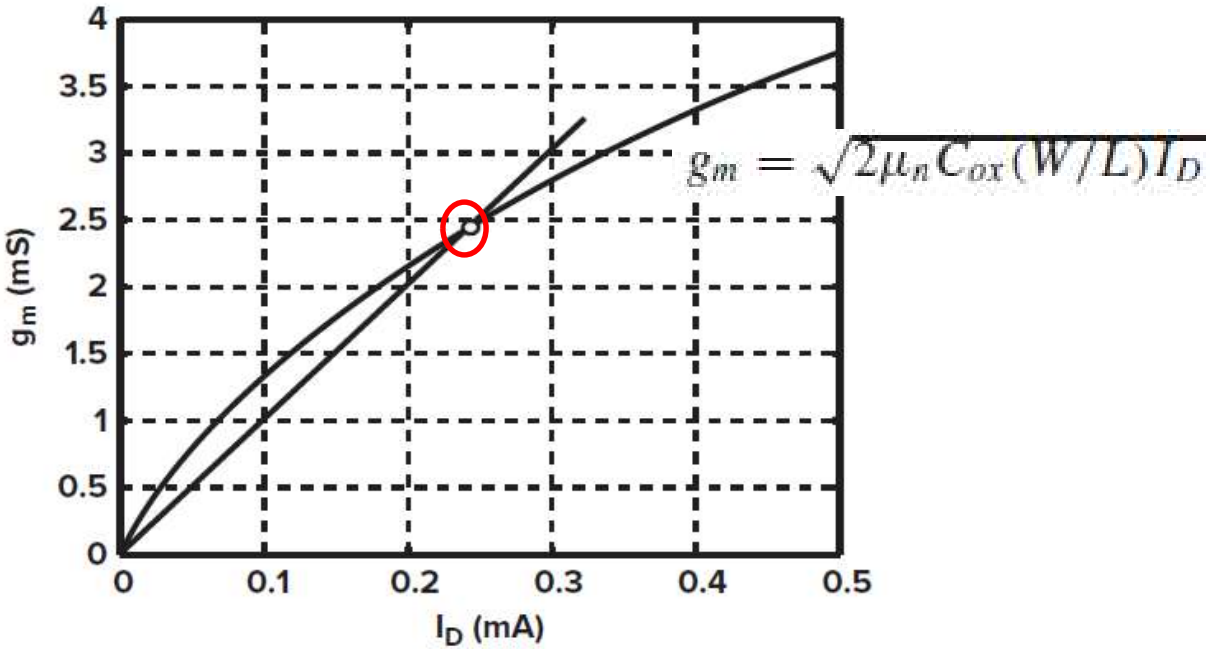




Things cannot be so simple. For analog design, there is no free lunch, generally!!



2. Design for Given I_D and g_m



$$g_{m1} = 10 \text{ mS}$$

$$I_{D1} = 1 \text{ mA}$$

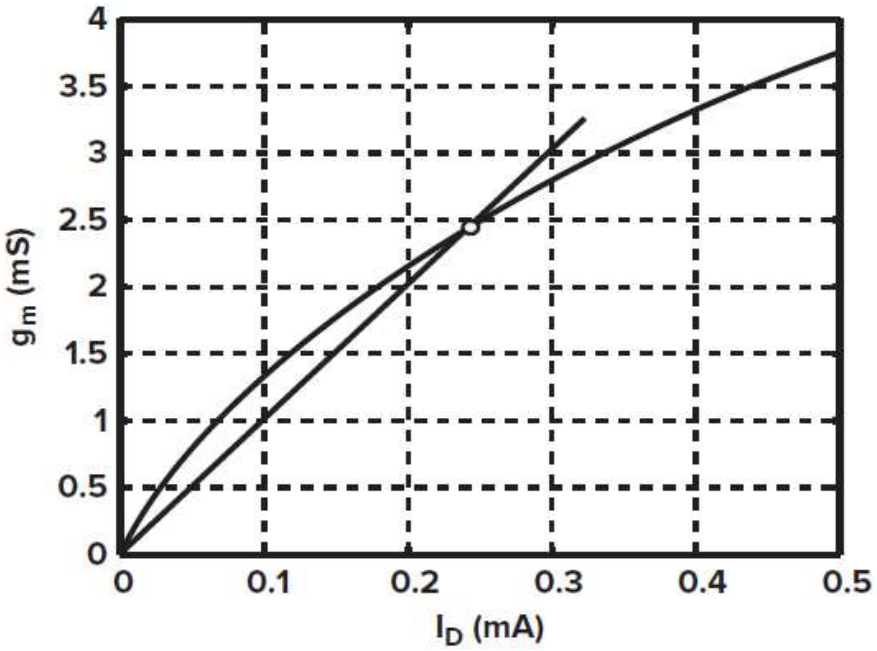
$$g_{m1} < \frac{I_{D1}}{\xi V_T}, \ \xi \approx 1.5$$

Step 1 Using simulations, we plot g_m as a function of I_D for a reference transistor, e.g., with $W_{REF}/L_{min} = 5\ \mu\text{m}/40\ \text{nm}$ (Fig. 11.14).

Step 2 We identify the point (I_{D1}, g_{m1}) on the g_m-I_D plane and draw a line through the origin and this point, obtaining the intersection at $(I_{D,REF}, g_{m,REF}) = (240\ \mu\text{A}, 2.4\ \text{mS})$ and a corresponding overdrive.

Step 3 We multiply W_{REF} by $g_{m1}/g_{m,REF} = 4.2$ so as to travel on the straight line to point (I_{D1}, g_{m1}) while maintaining the same overdrive (Example 11.3). This completes the design of the transistor.

2. Design for Given I_D and g_m

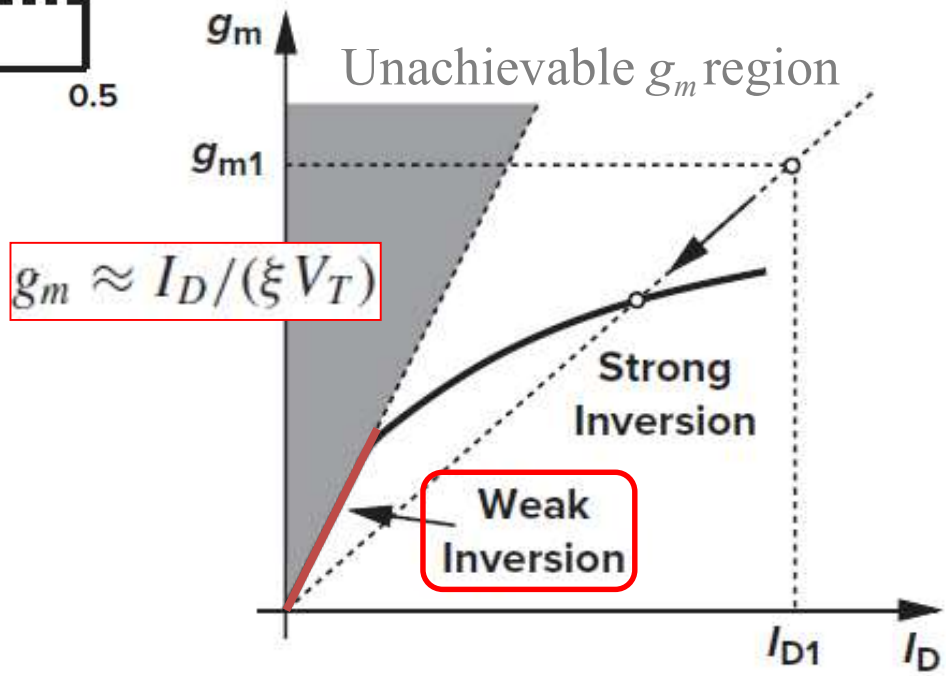


$$g_{m1} = 10\ \text{mS}$$

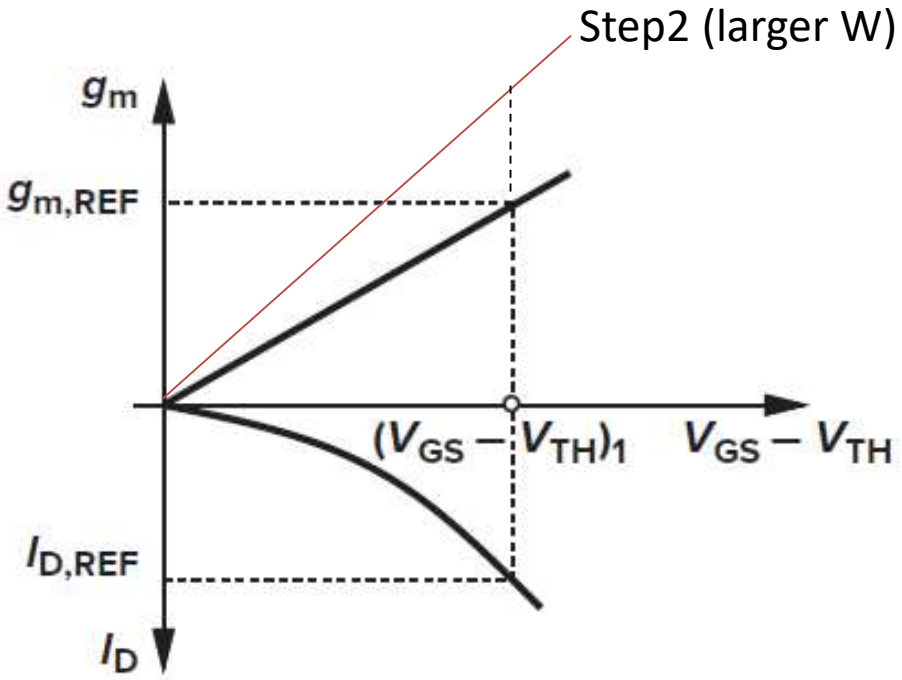
$$I_{D1} = 1\ \text{mA}$$

$$g_{m1} < \frac{I_{D1}}{\xi V_T},\ \xi \approx 1.5$$

$$\Rightarrow g_{m,max} = 26\text{mS at } 27°\text{C}$$



3. Design for Given g_m and $V_{DS,min}$



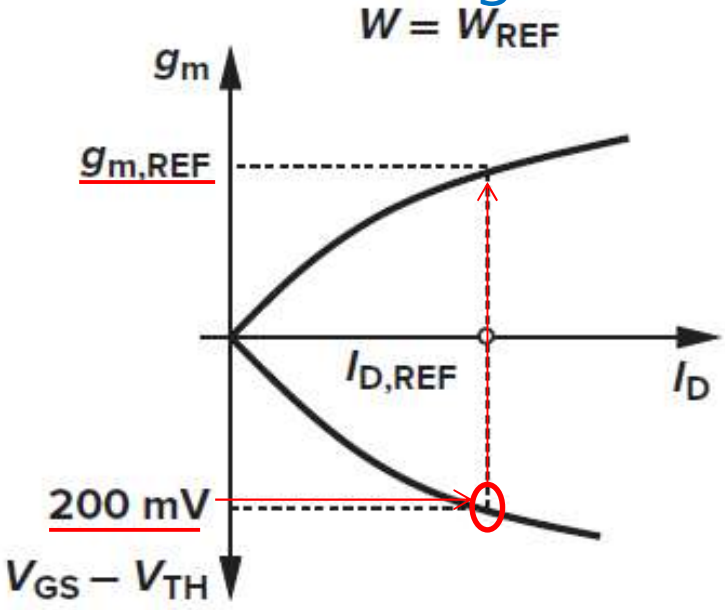
$(V_{GS} - V_{TH})_1 = V_{DS,min}$

Step 1 We use simulations to plot the g_m as a function of $V_{GS} - V_{TH}$ for the reference transistor (Fig. 11.17). Now, we select $(V_{GS} - V_{TH})_1 = V_{DS,min}$ and obtain the corresponding transconductance, $g_{m,REF}$. In this case, it is helpful to plot I_D on the same plane and find $I_{D,REF}$ at $(V_{GS} - V_{TH})_1$.

Step 2 To reach the required transconductance, g_{m1}, we scale the transistor width up by a factor of $g_{m1}/g_{m,REF}$. Note that I_D scales by the same factor.

4. Design for Given g_m

Q: How do we select the transistor's drain current, overdrive voltage, and dimensions?



Two scenarios:

(1) We select a certain W/L and raise I_D until we obtain the desired transconductance, g_{m1}.

(2) We select a reasonable value for I_D (perhaps according to a power budget) and increase W/L to obtain g_{m1}.

(1) In this case, the required I_D, and hence the power consumption, may be excessive. More important, the overdrive voltage may be unacceptably large, leaving little headroom for voltage swings.

(2) In this case, however, we may not be able to reach g_{m1}; increasing W/L (and hence decreasing V_{GS}) eventually drives the device into the subthreshold region, where gm cannot exceed $I_D/(\xi V_T)$.

Opamp Design Examples

- Three Opamp design in the textbook
  - Opamp design example 1: a telescopic opamp
  - Opamp design example 2: a two-stage opamp
  - Opamp design example 3: a high-speed amplifier

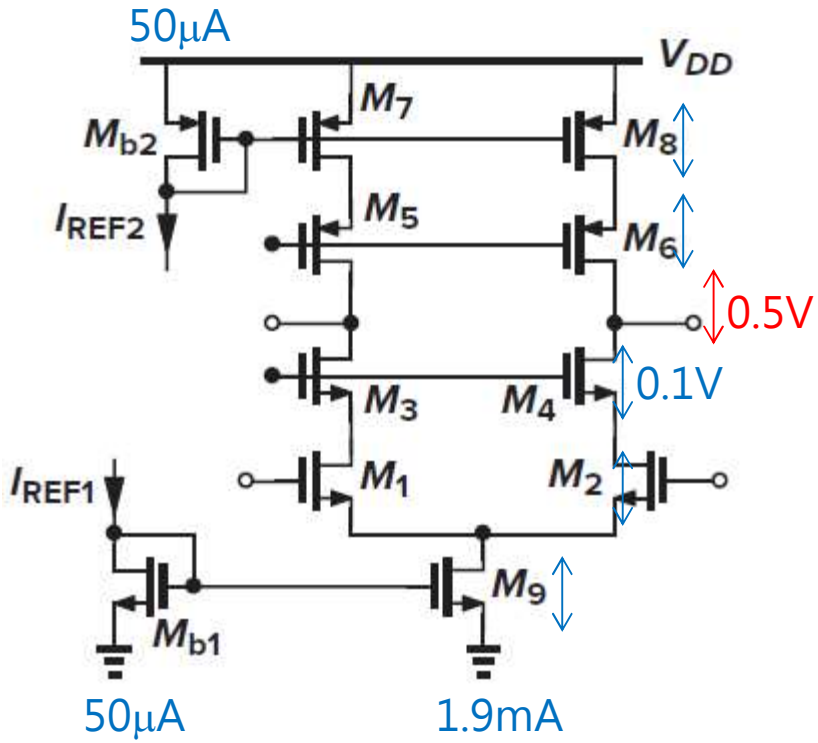
Opamp Design Example 1

Target specifications:

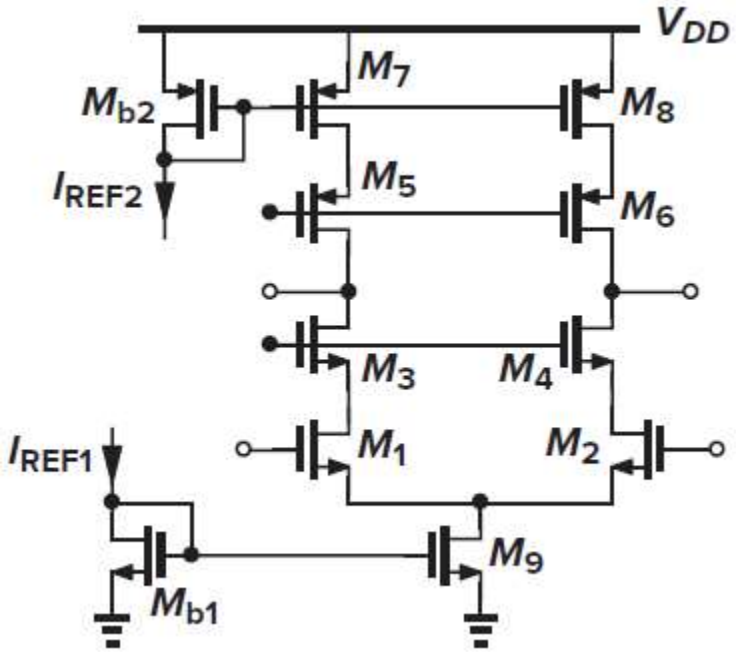
- Differential Output Voltage Swing = 1 V*pp*
- Power Consumption = 2 mW
- Voltage Gain = 500
- Supply Voltage = 1 V

Design Concept:

1. Current arrangement
2. Output Swing => $V_{DS,min}$
3. ICMR => Vicm
4. Small-signal: DC => AC



Opamp Design Example 1



Three observations:

(1) $g_m r_o$ for L=40nm MOSTs,

- pMOST: 5~7; nMOST: 7~10

(2) Longer *L*, lower speed

(3) $g_{m1}=2I_{D1}/(V_{GS1}-V_{TH1})$ = 19mS; it means r_o is about 530Ω

For this telescopic opamp,

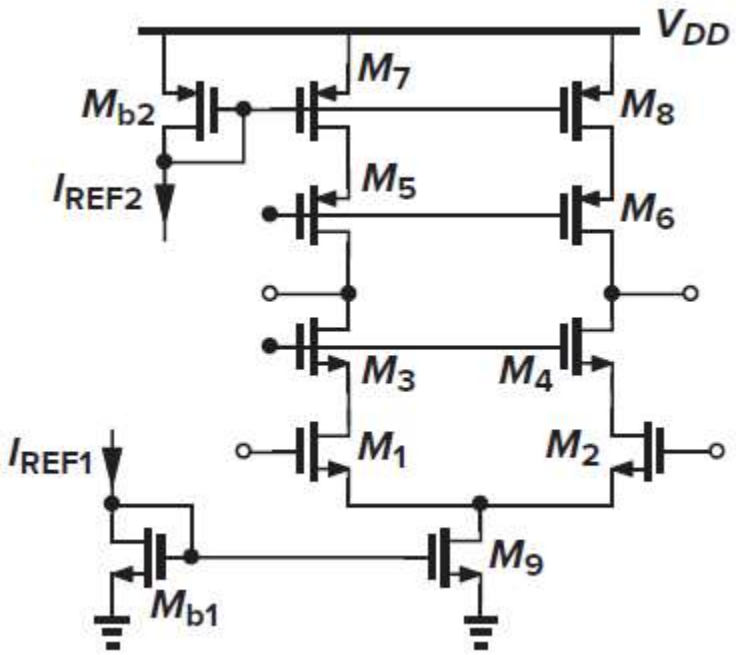
A= Gm*Rout = 1000 => Rout~50kΩ

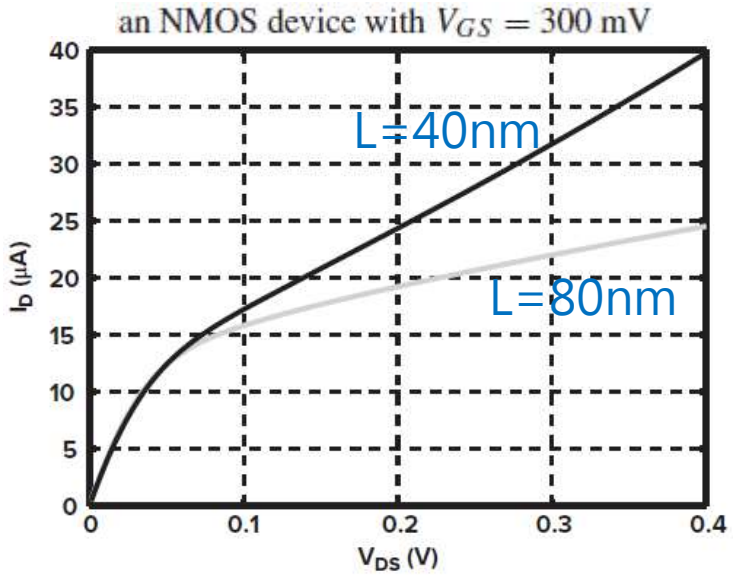
Rout= $(g_{m5,6}r_{o5,6})r_{o7,8}$ // $(g_{m3,4}r_{o3,4})r_{o1,2}$

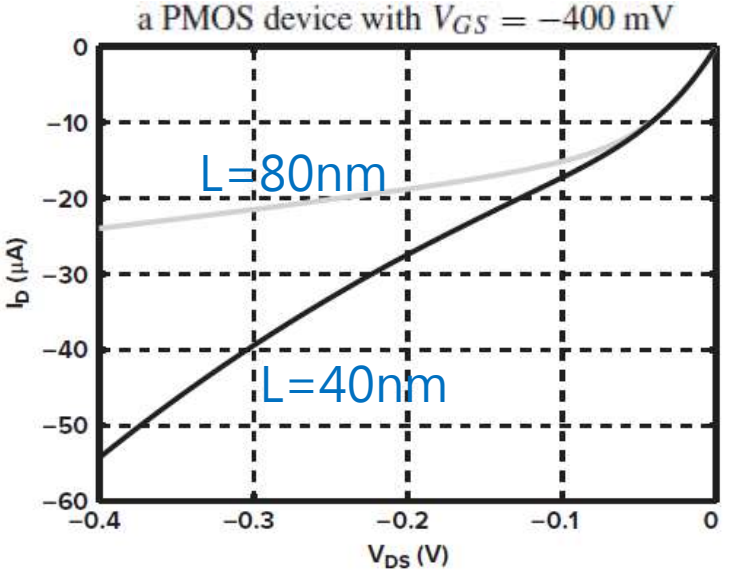
=> $(g_{m5,6}r_{o5,6})r_{o7,8}$ ~ 100kΩ

=> $g_{m5,6}r_{o5,6}$ ~ 200, hard to achieve!!

Opamp Design Example 1

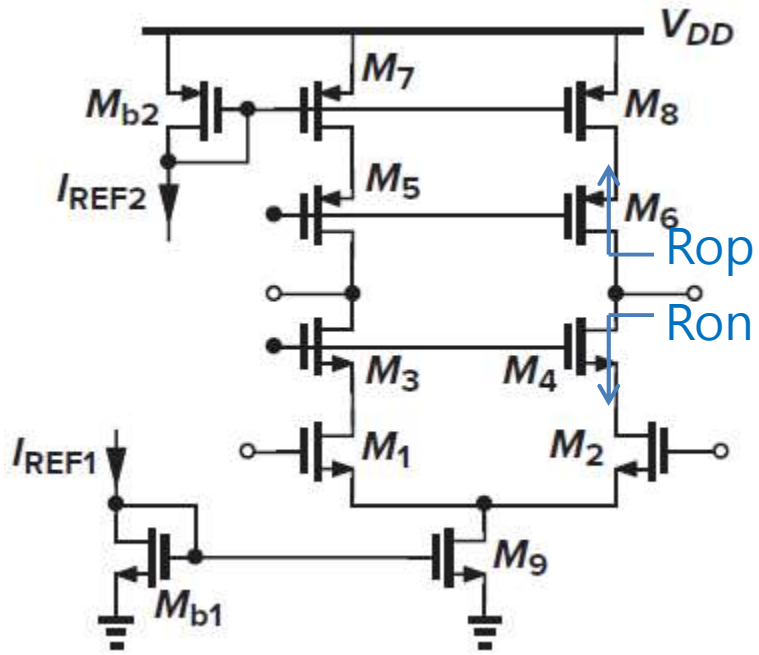


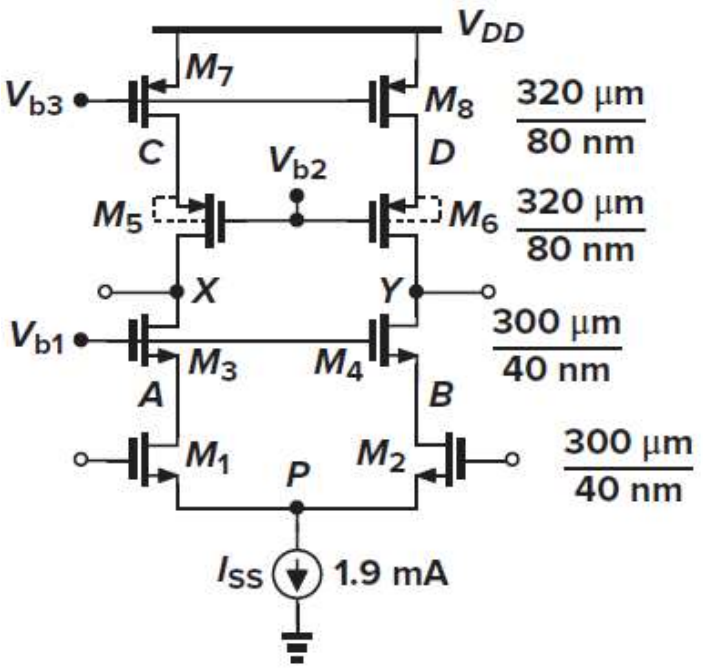




Try some Longer MOSTs!!

Opamp Design Example 1





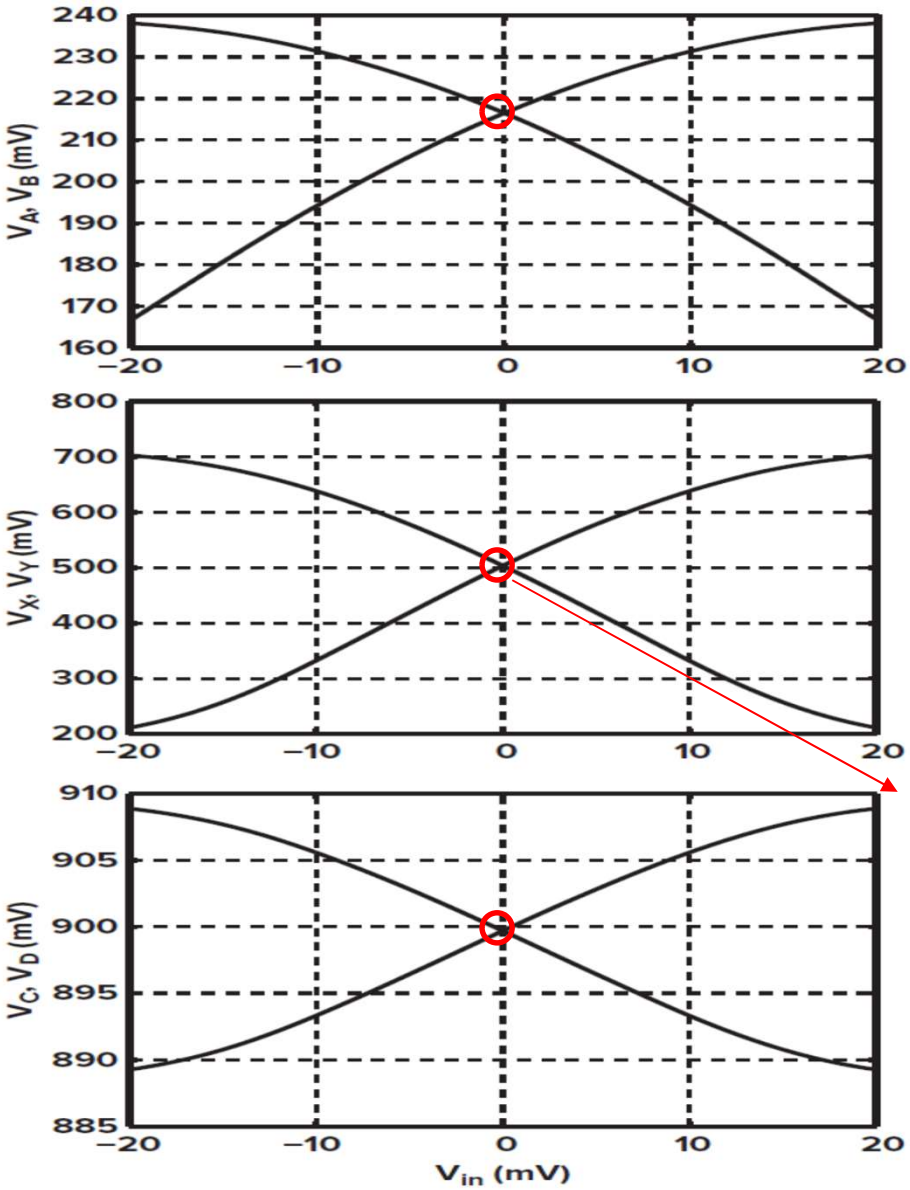
Why do we design like above?

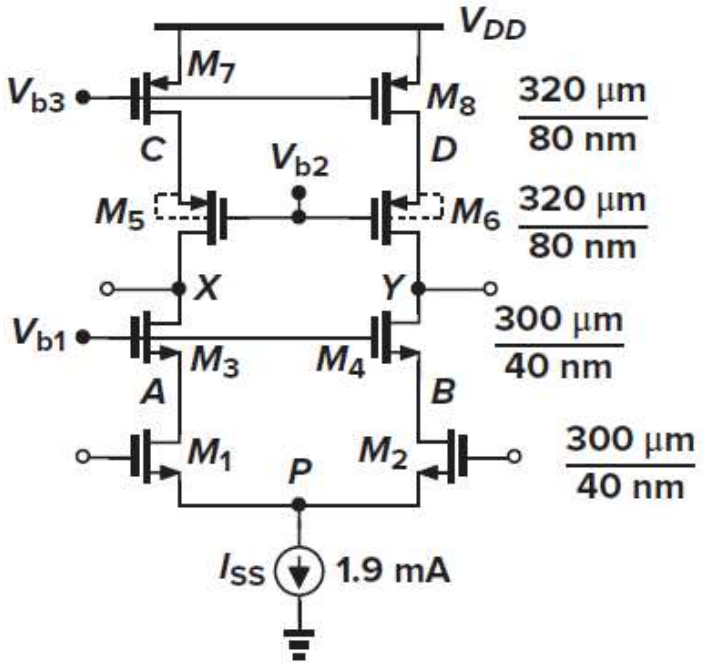
⇒Based on two reasons:

(1) Higher speed

(2) Ro balance (Rop~Ron)

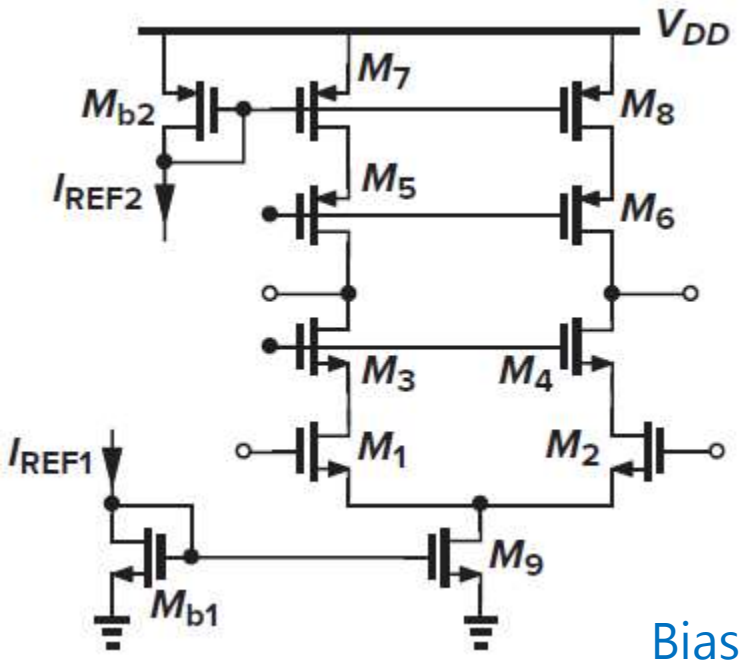
Opamp Design Example 1

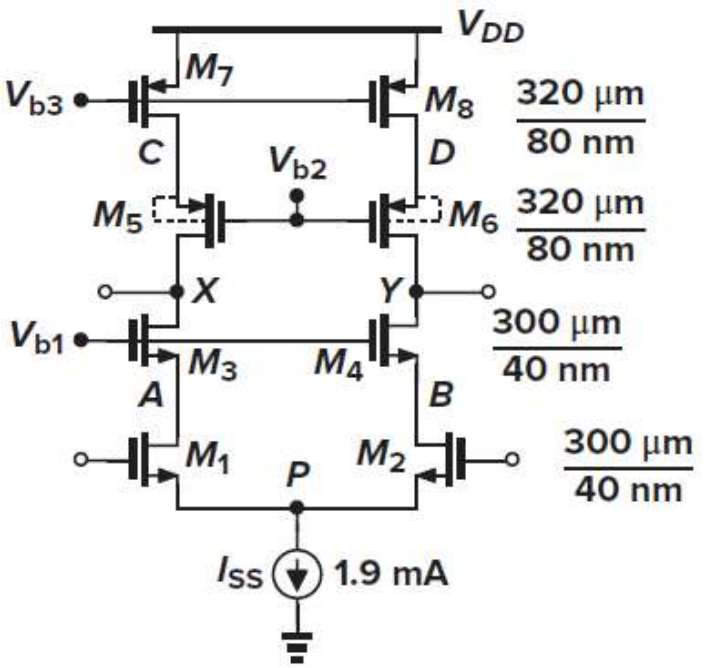




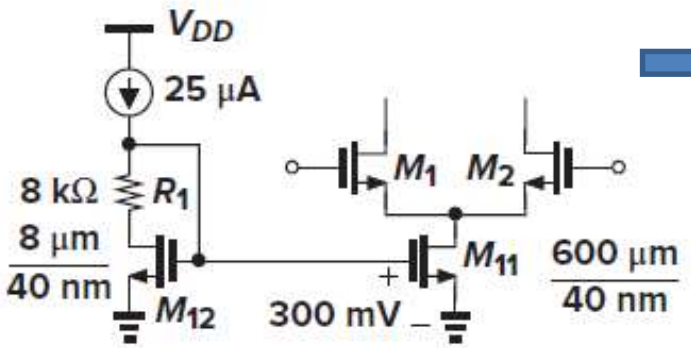
- The slope of each single-ended output is approximately equal to 15 in the vicinity of *Vin* = 0, yielding a differential gain of 30, far below our target.
- Diff. gain is low to only 6.4 for max. output
- Fail to meet the target spec. But, we keep looking

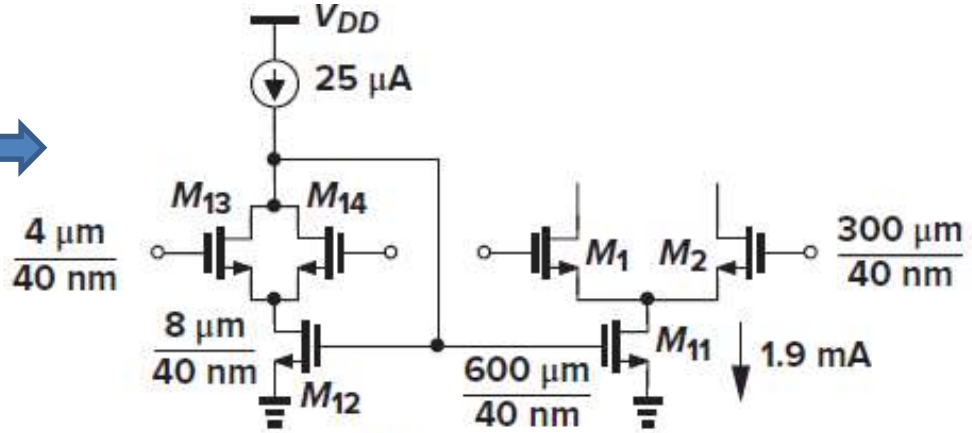
Opamp Design Example 1





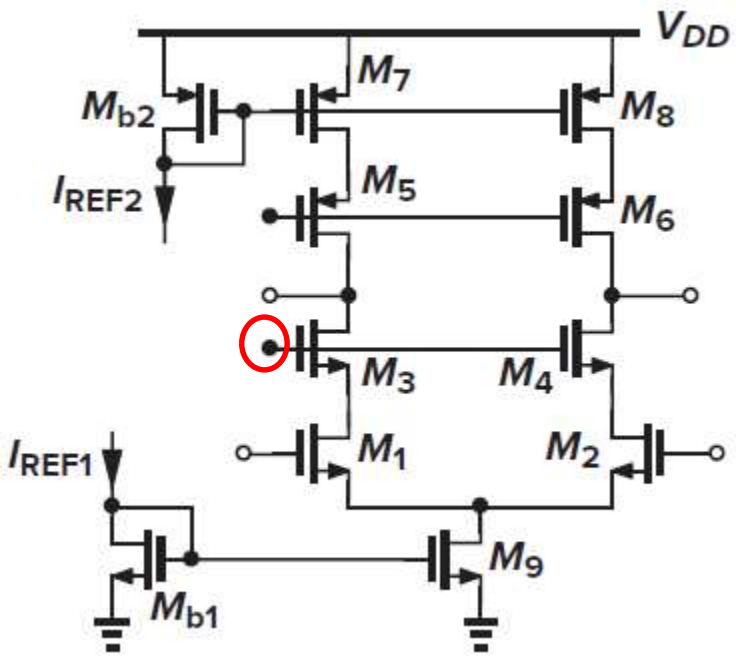
Bias Circuits



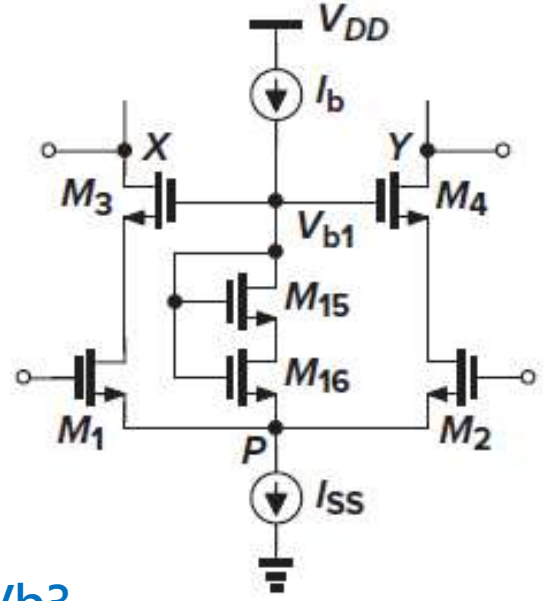


Q: What's the difference?

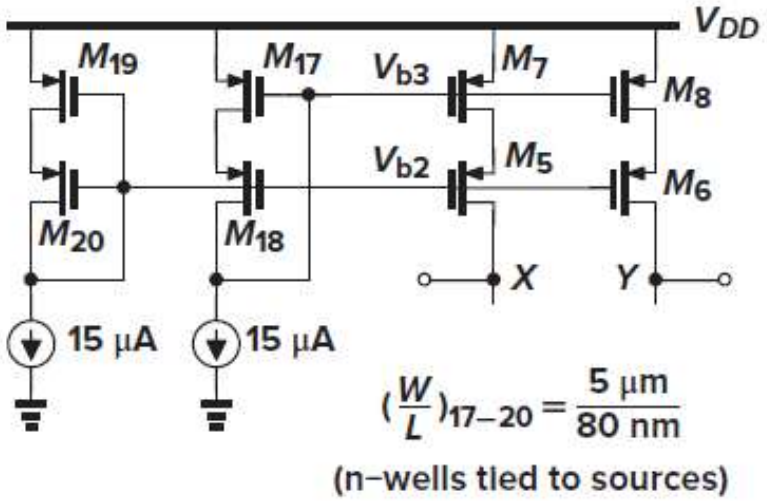
Opamp Design Example 1



Vb1

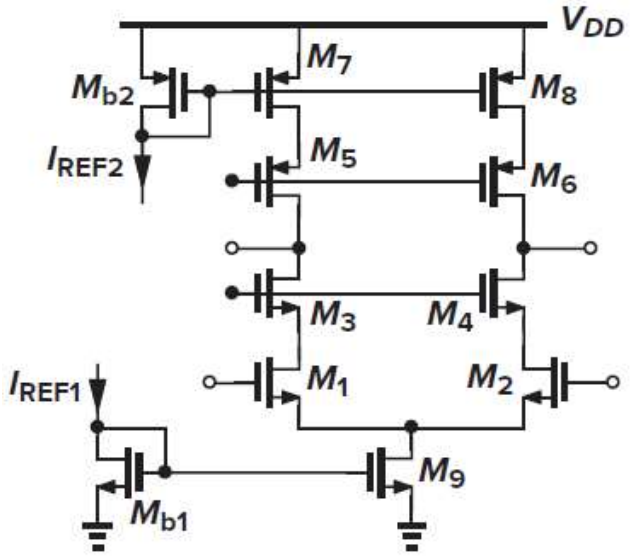


Vb2, Vb3

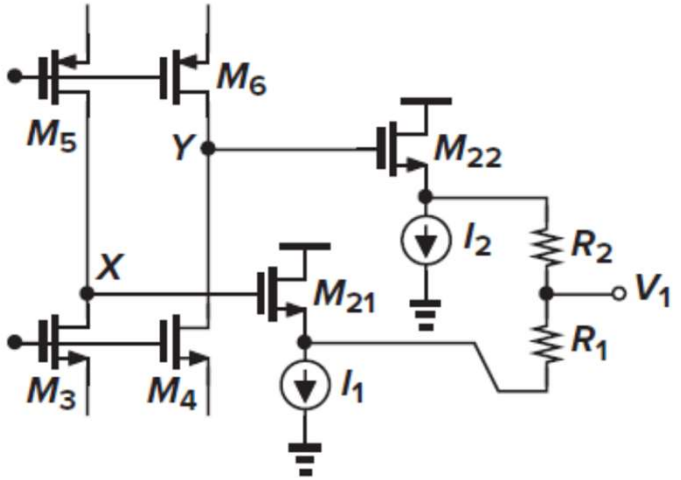


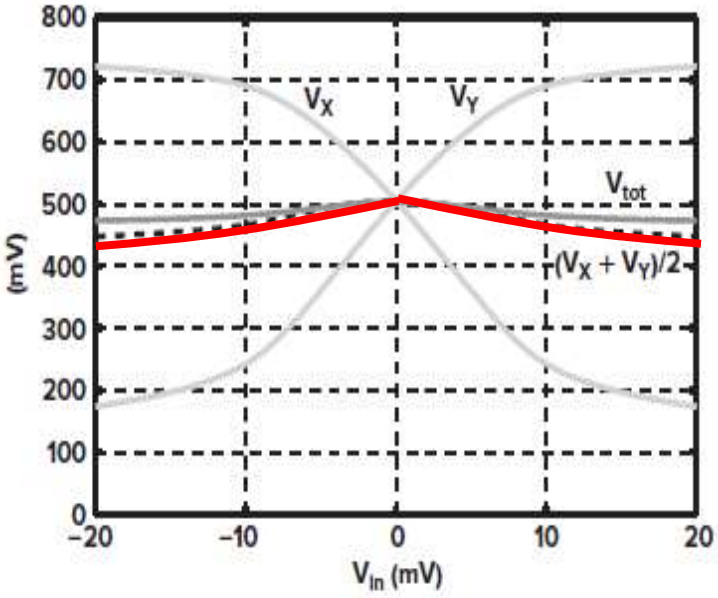
Bias Circuits

Opamp Design Example 1



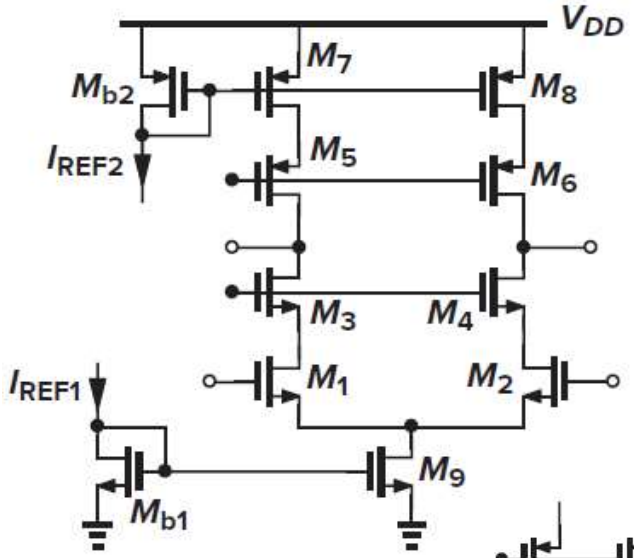
CMFB Circuit





- CMFB sensing: Resistor, Triode MOST, Source Follower
- Simple source follower cannot maintain a large output swing (shown in the right figure)
- Vocm cannot be a constant over the full-scale output range

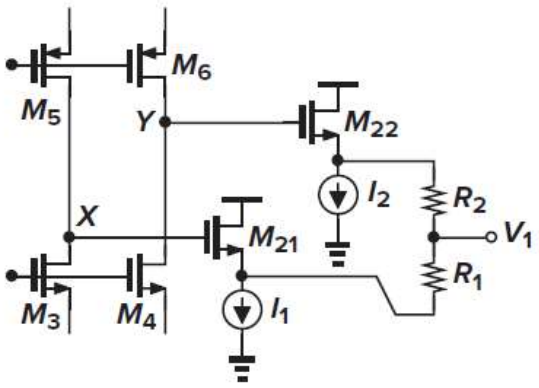
Opamp Design Example 1



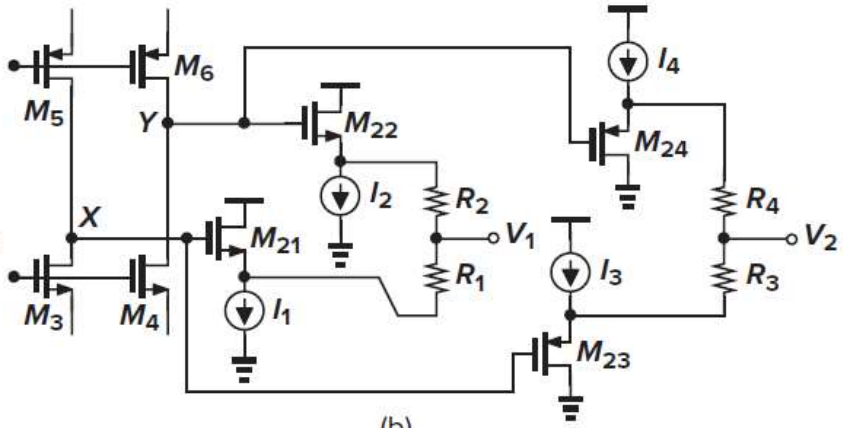
CMFB Circuits

(a) Single source follower (P or N-SF)

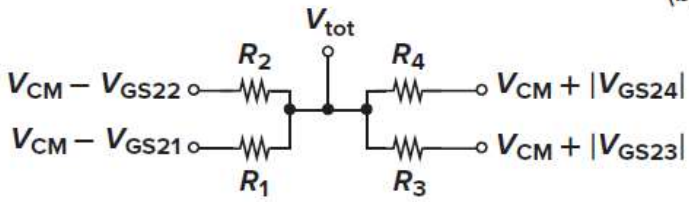
(b) Composite source followers (P+N-SFs)



(a)



(b)



(c)

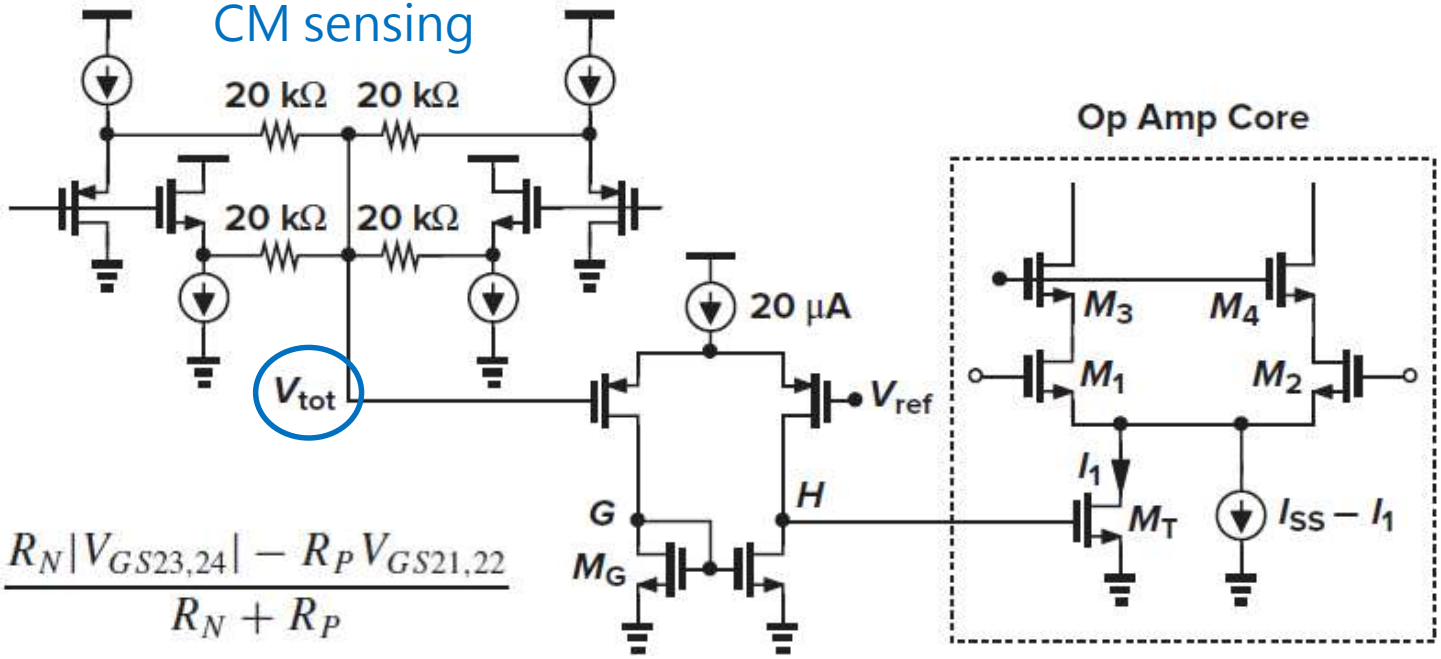
Opamp Design Example 1

CMFB Loop: Concept

$$V_1 = V_{CM} - V_{GS21,22}$$

$$V_2 = V_{CM} + |V_{GS23,24}|$$

$$\alpha V_1 + \beta V_2 = (\alpha + \beta) V_{CM} - \alpha V_{GS21,22} + \beta |V_{GS23,24}|$$



$$V_{tot} = V_{CM} + \frac{R_N |V_{GS23,24}| - R_P V_{GS21,22}}{R_N + R_P}$$

where $R_N = R_1 = R_2$ and $R_P = R_3 = R_4$.

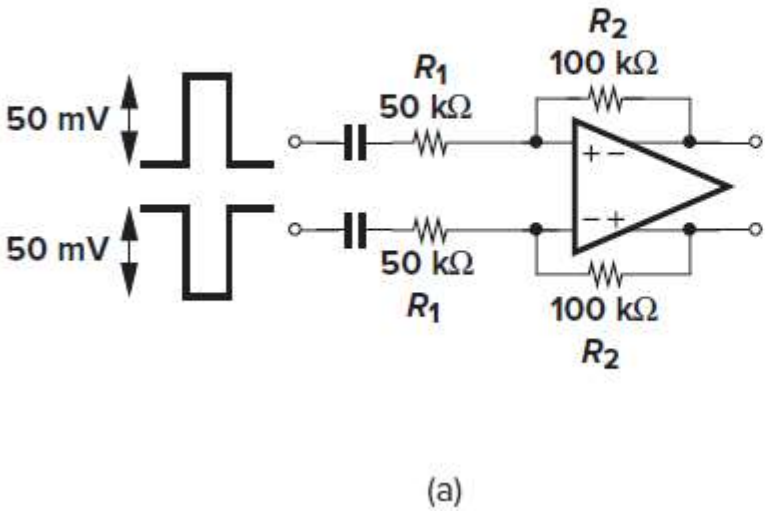
Error Amplifier (Err. Amp.)

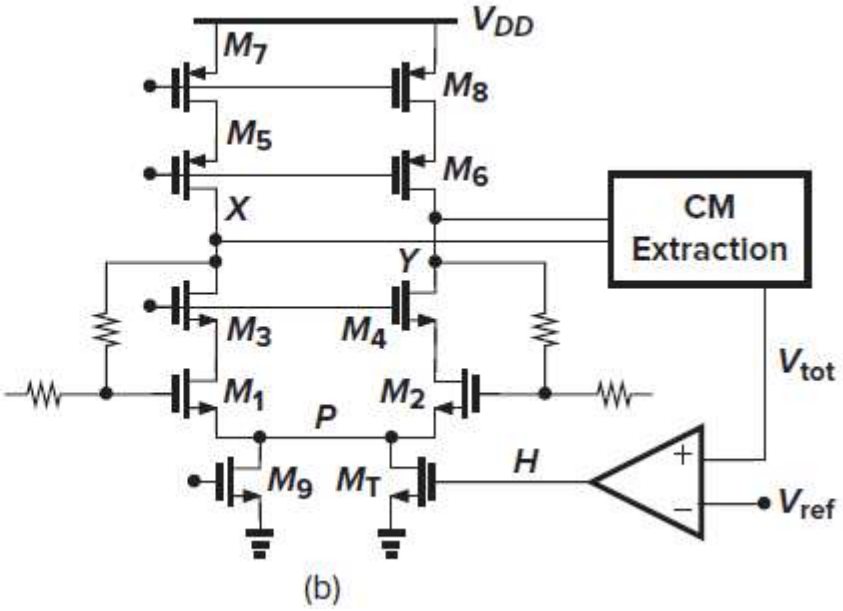
Current Control (M_T)

Q: Explain why the OTA employs PMOS (rather than NMOS) input devices.

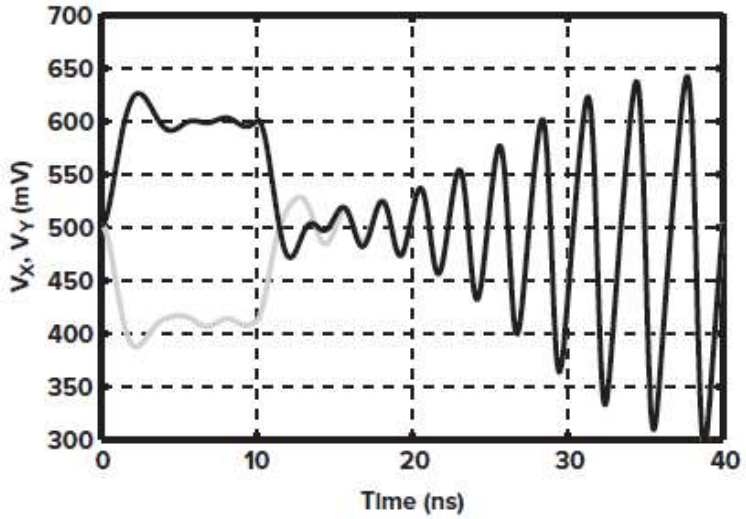
Opamp Design Example 1

CMFB Loop: Simulation



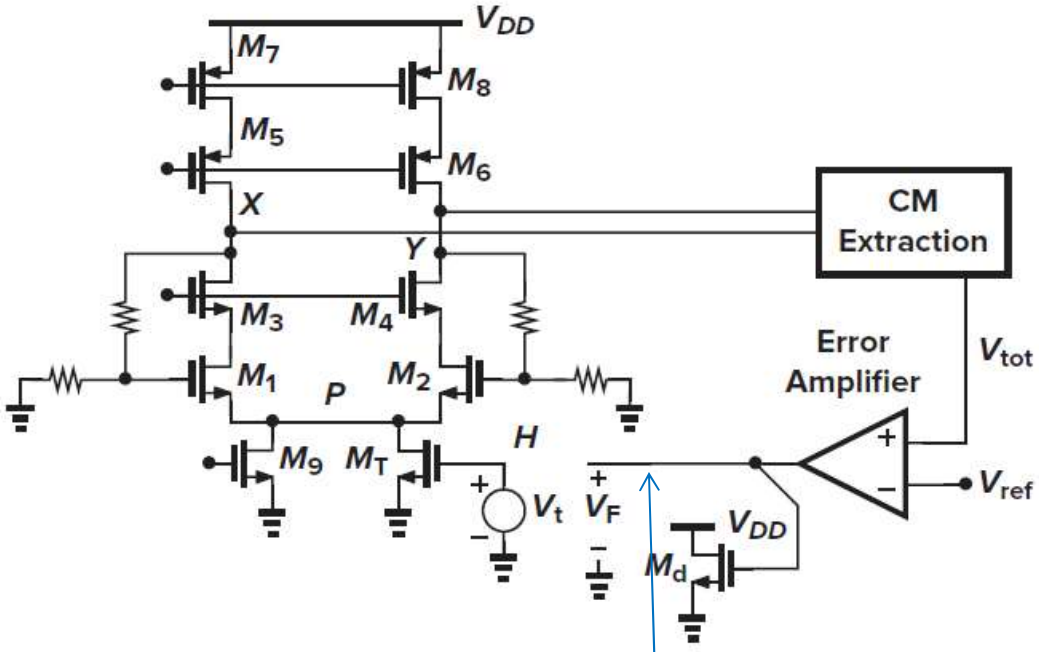


Transient response revealing CM loop instability. Why?

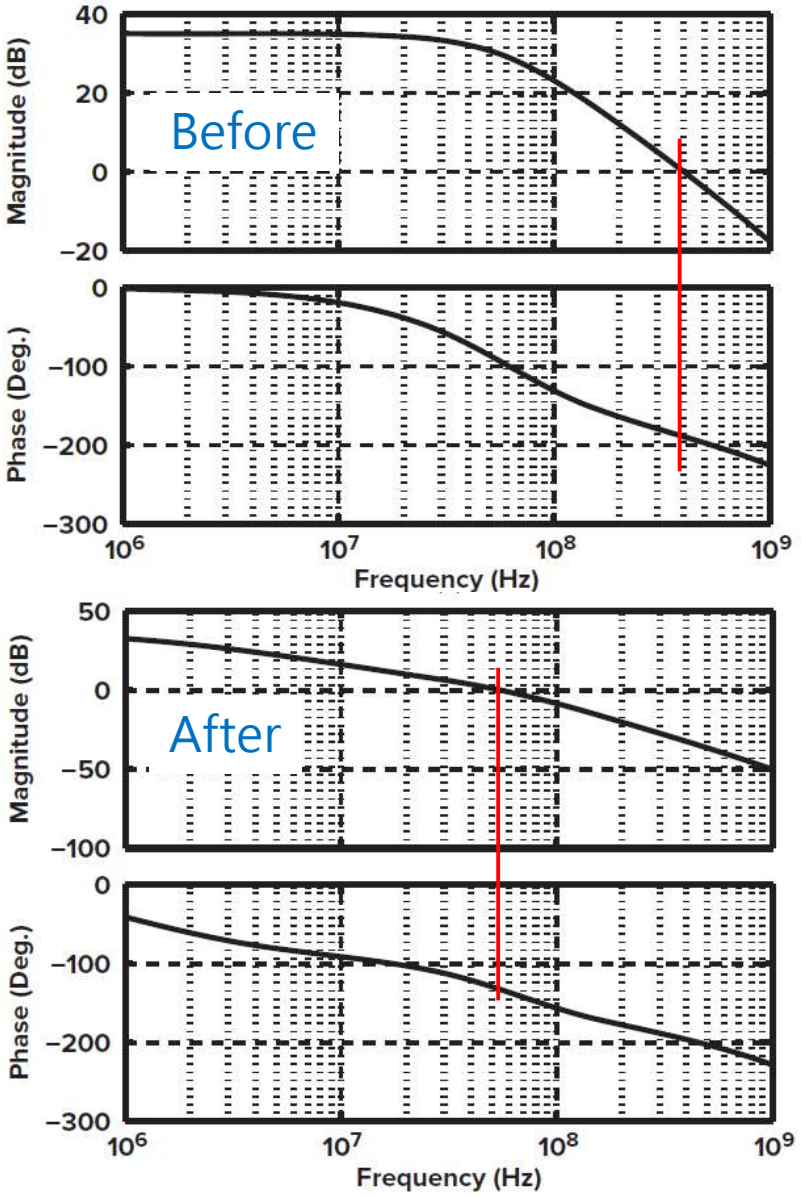


Opamp Design Example 1

CMFB Loop: Compensation

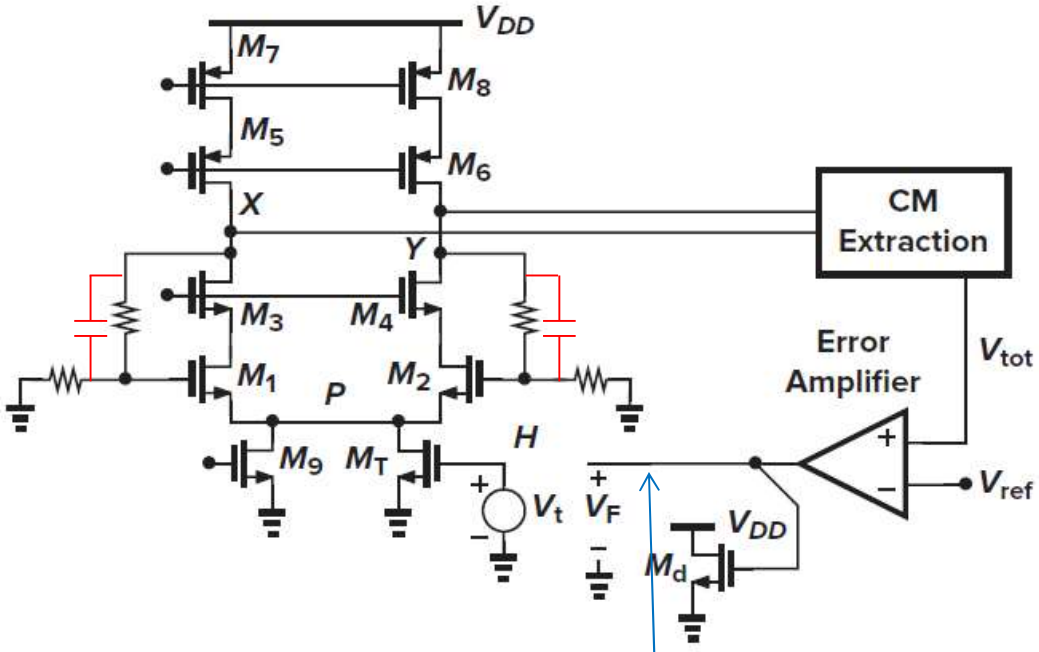


3pF Cap at the output node of the Err. Amp.



Opamp Design Example 1

CMFB Loop: Compensation

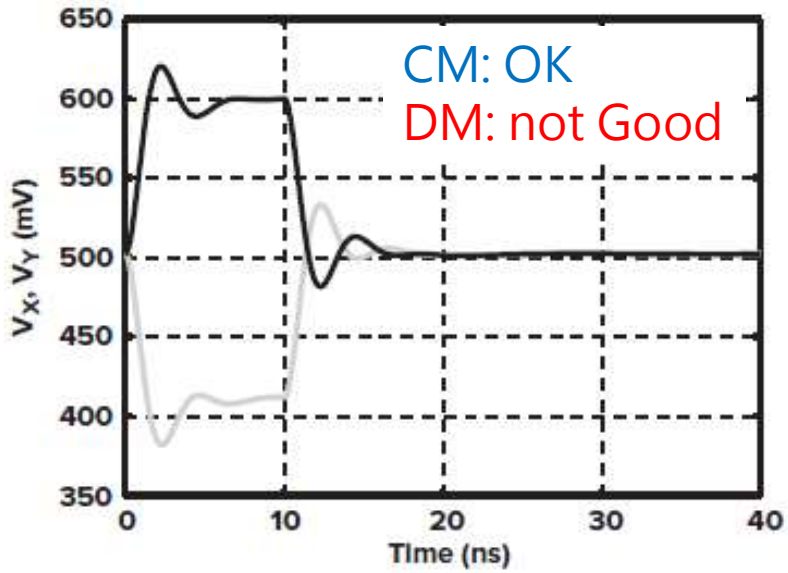


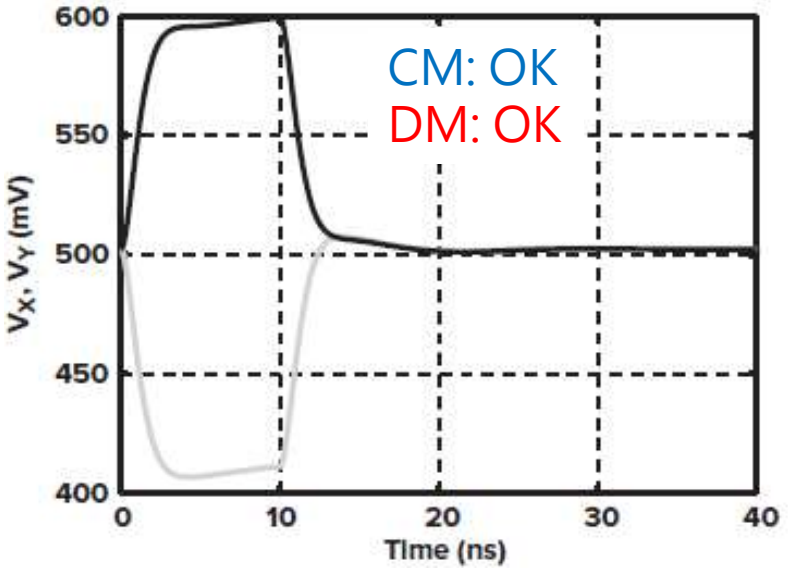
CM

3pF Cap at the output node of the Err Amp

DM

7fF miller cap connected from output to input





Opamp Design Example 1

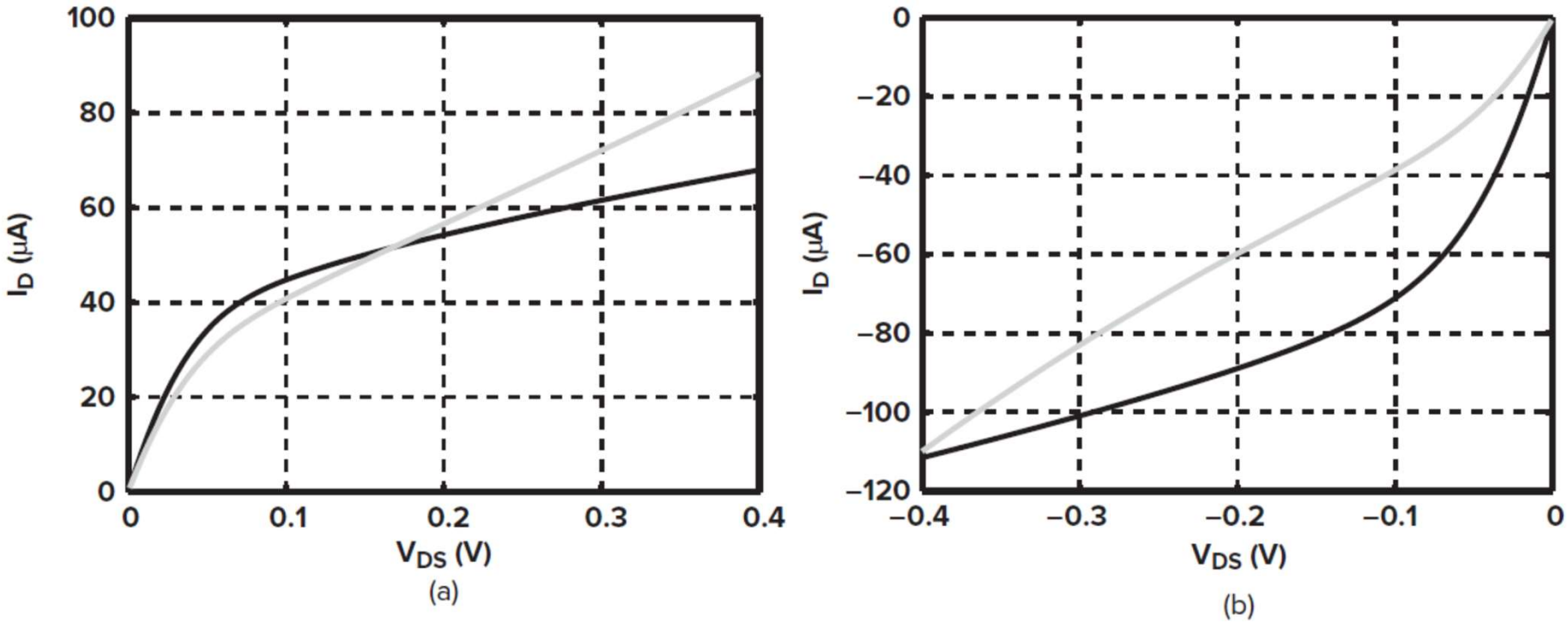
Design Summary

We have attempted to design a telescopic-cascode op amp for a voltage gain of 500 and a differential output swing of 1 Vpp. Neither specification could be met with a 1-V supply, but we have established the steps that one must complete in order to arrive at the final design. Specifically, we have dealt with the following general principles:

1. Allocation of V_{DS} and I_D to transistors according to required swings and power dissipation, respectively
2. Characterization and scaling of MOSFETs for allowable V_{DS} and desired current level (page 24)
3. Quick estimate of the achievable voltage gain
4. Use of dc sweep to study bias conditions and nonlinearity
5. Design of bias circuitry using current mirrors and low-voltage cascodes
6. Common-mode feedback design and compensation
7. Use of closed-loop transient analysis to study CM and differential stability

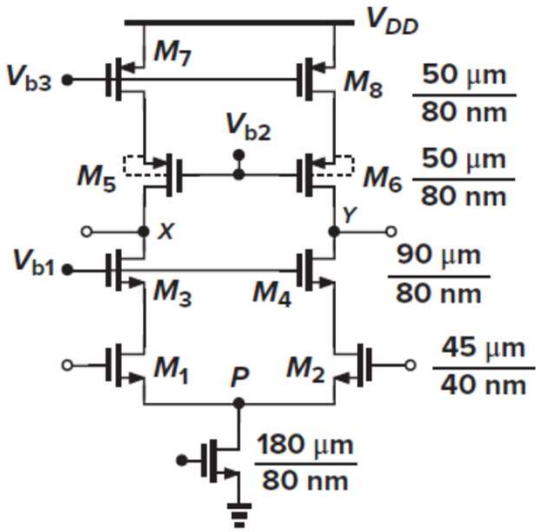
Opamp Design Example 2

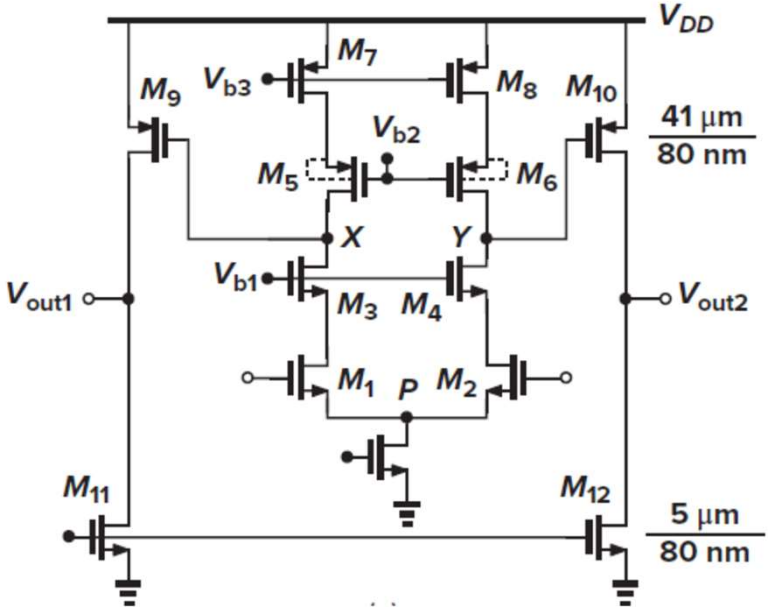
Two-Stage Opamp Design Flow (Textbook, pp. 487~495)



At the beginning, try to get your MOSFET plots, simulated using Hspice/Spectre models

Two-Stage Opamp





Total bias branch current:100 μA

Branch current: <1.9 mA/4 = 450 μA

I=50 μA => (W/L)n =10μm/80nm

First stage output, $V_{xy,pp}$ = 50mV

$V_{DS,N}$ = 150 mV and $V_{DS,P}$ = 200 mV

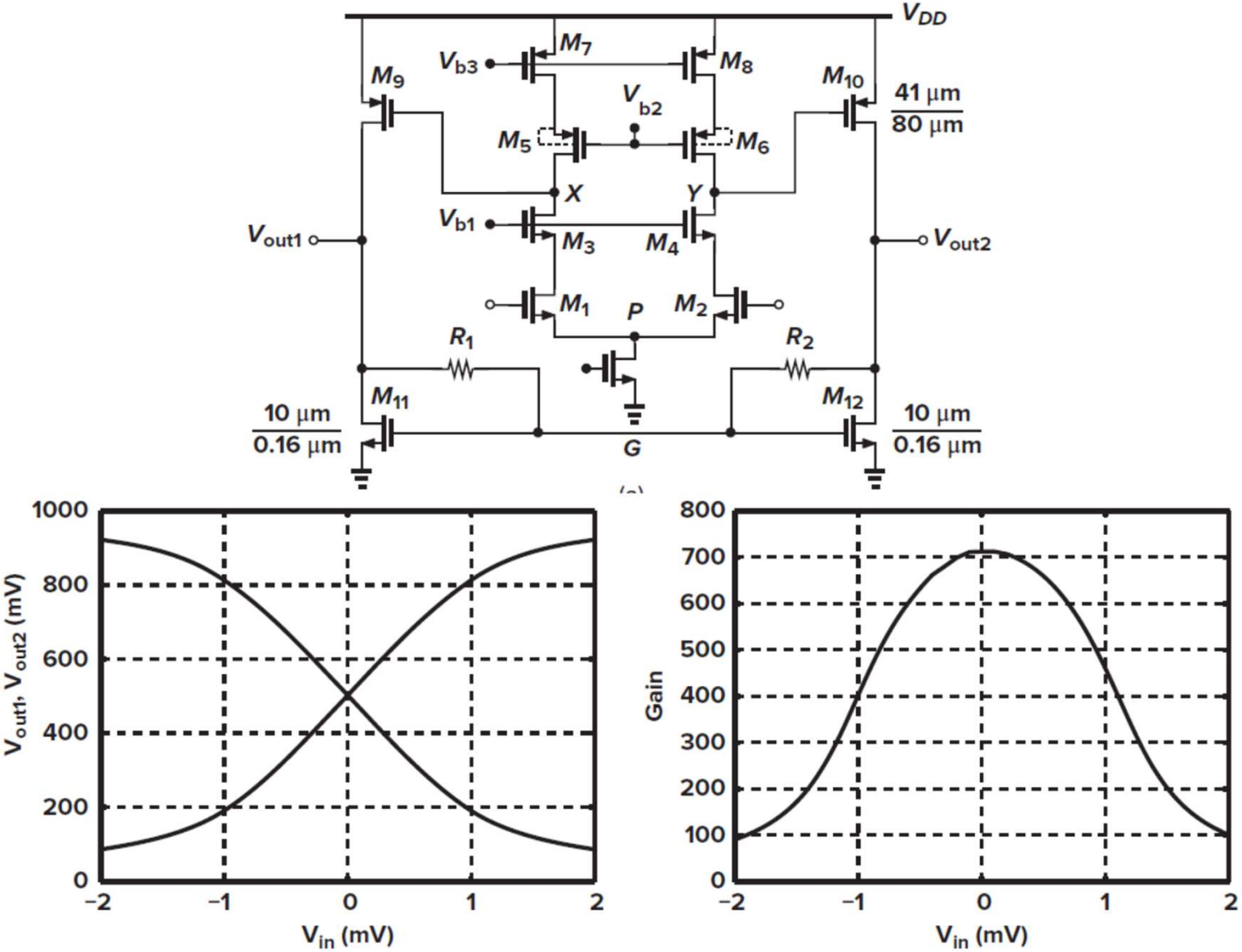
First stage gain = 50

Second stage gain = 10

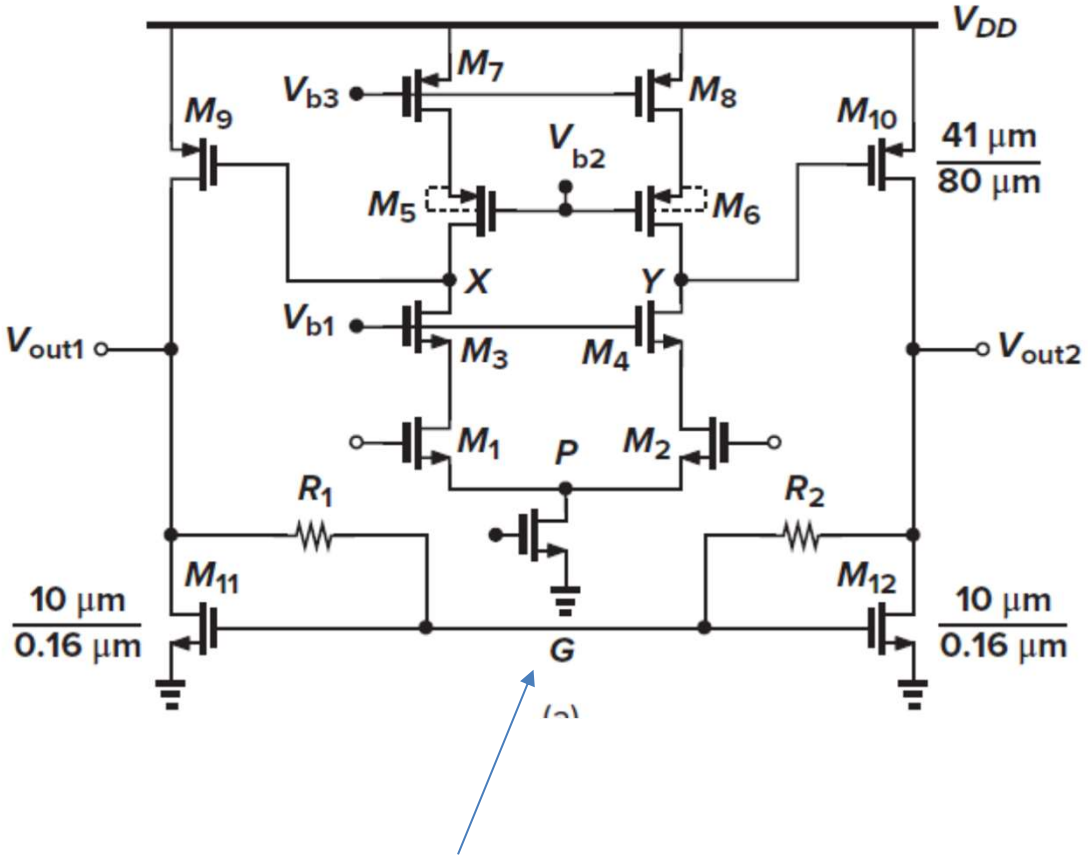
$A_{V2} = g_{m10}*(r_{o10}//r_{o12}) > 10$

$V_{out1,2}$: 0.5V output range

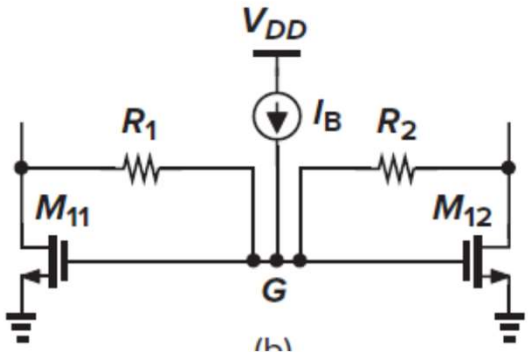
Two-Stage Opamp



Two-Stage Opamp



CMFB

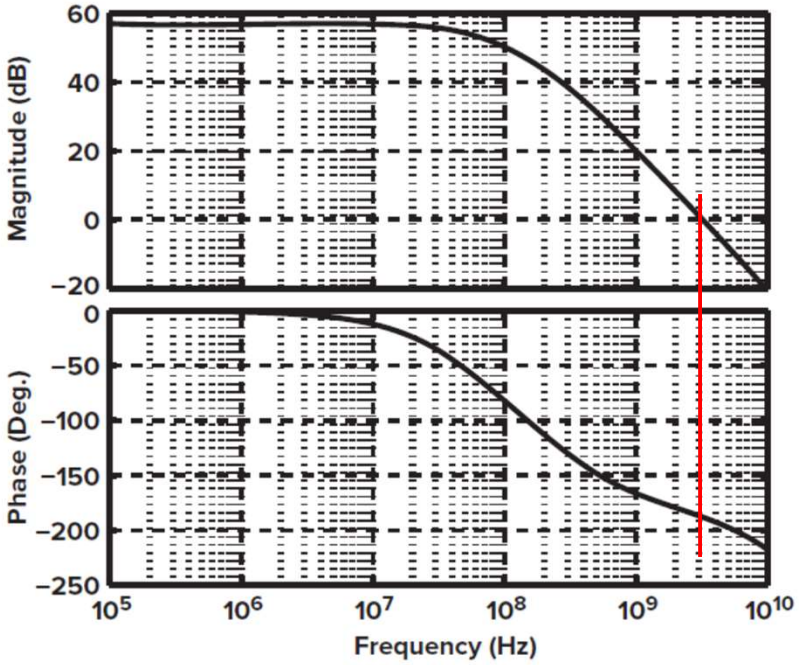


R_1 and R_2 ($\approx$30 kΩ)

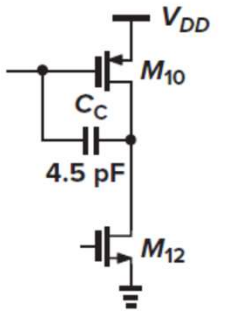
- Common-mode of Vx and Vy are not maintained
- The first stage needs a CMFB loop

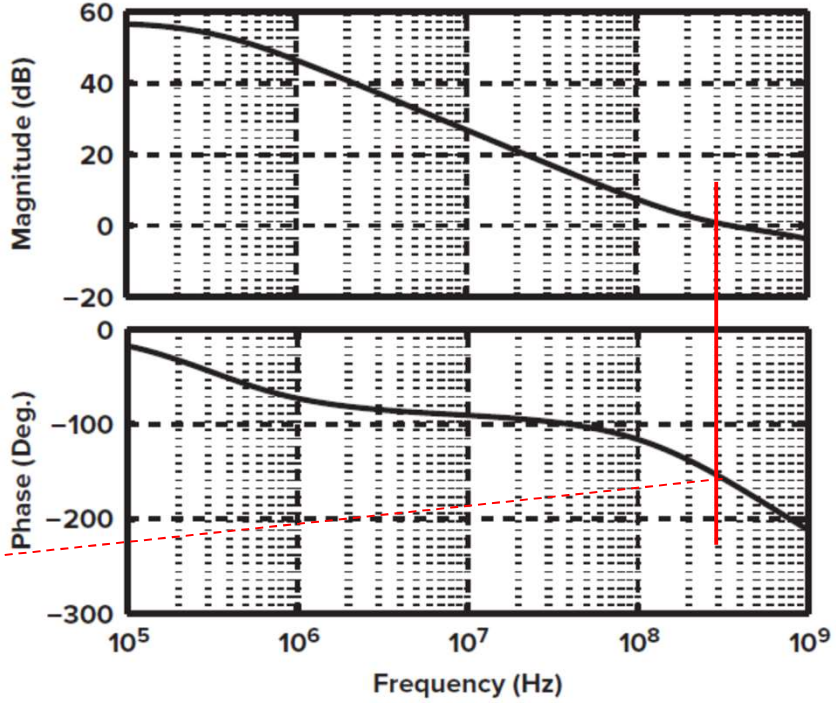
Adding I_B to shift CM level

Two-Stage Opamp



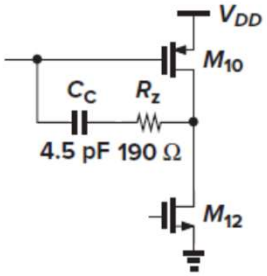
Frequency Compensation

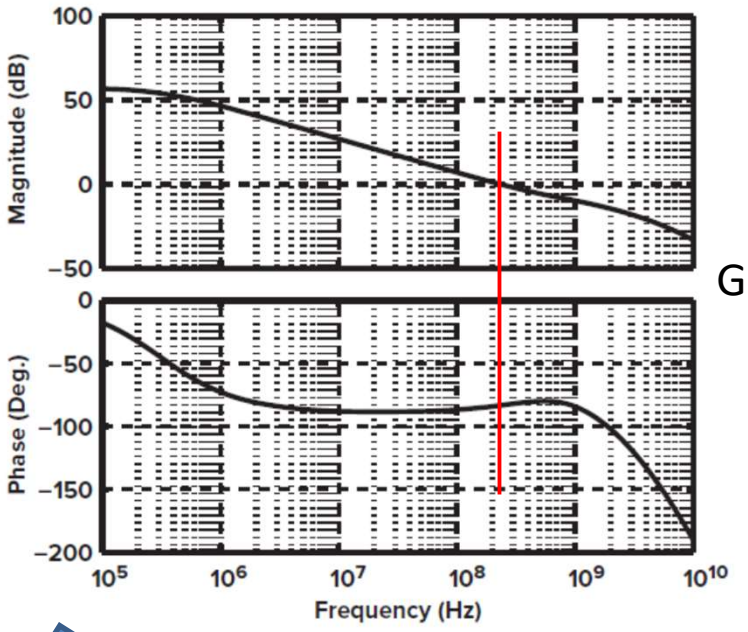




Only a miller cap is not enough!!

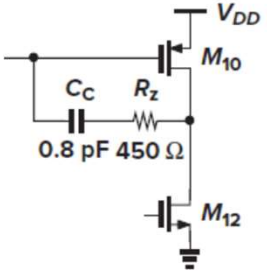
Two-Stage Opamp

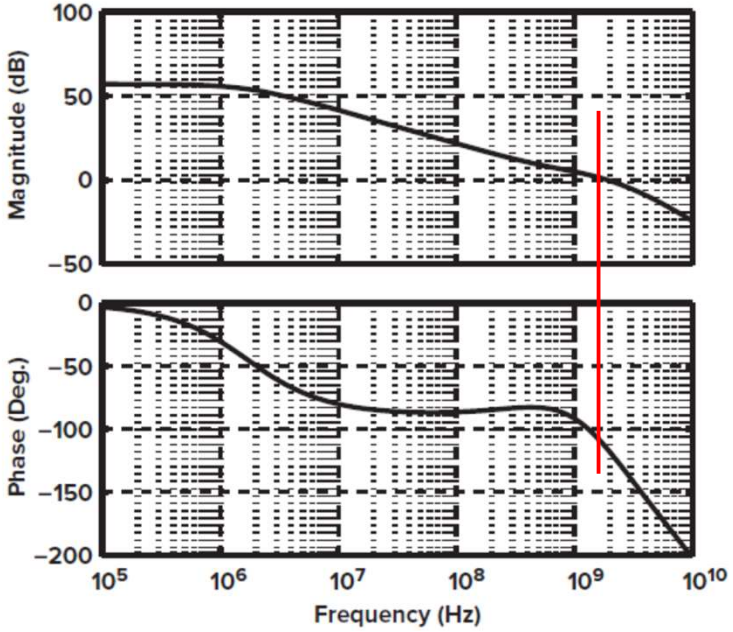




Frequency Compensation

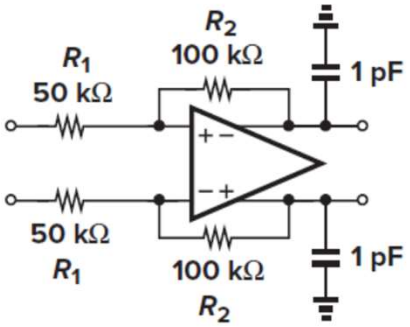
GBW is not good enough!!

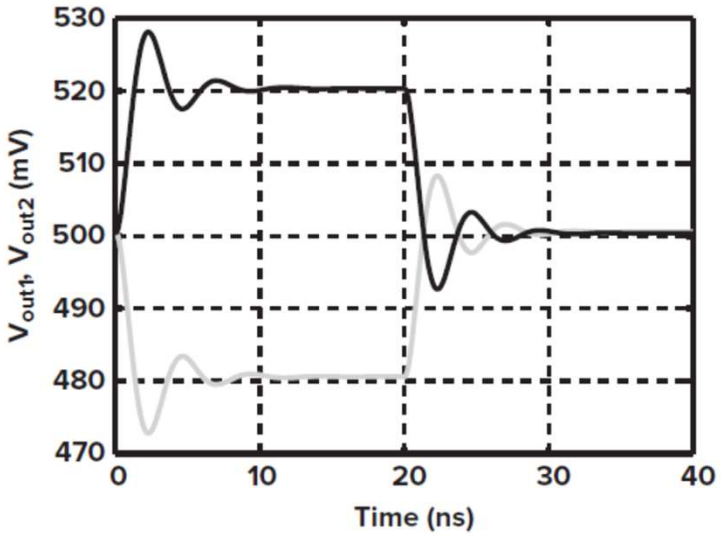




Two-Stage Opamp

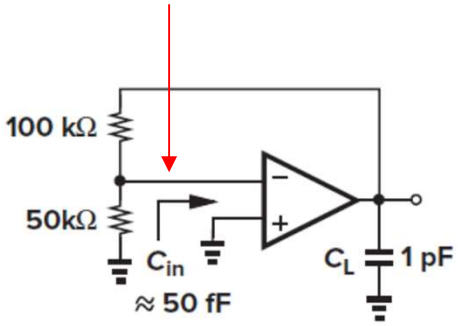
Closed-Loop Behavior

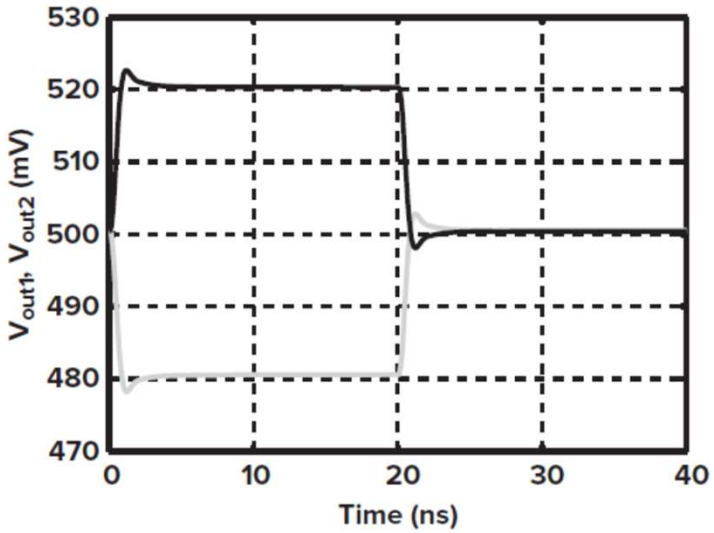




Rz = 1500ohm

An **open-loop pole** around $[2\pi(100k||50k)C_{in}]^{-1} \approx 95$ MHz is formed at the input of the op amp





Opamp Design Example 3

High-Speed Amplifier Design Flow (Textbook, pp. 495~507)