

Analog Integrated Circuit Design and Applications

Spring 2024

Bandgap References

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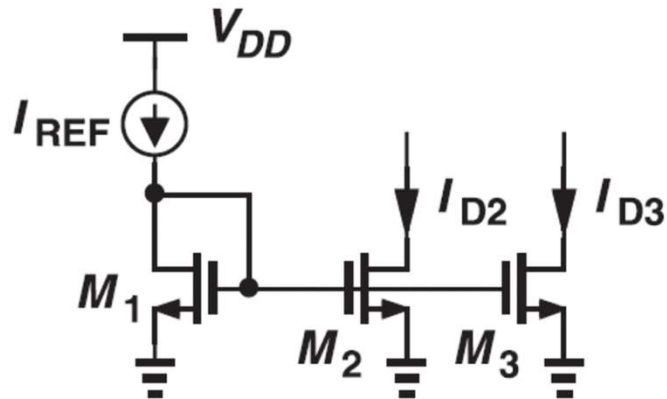
MSIC Lab
DECE, NTUST

Mixed-Signal
IC Laboratory 
NTUST

Outline

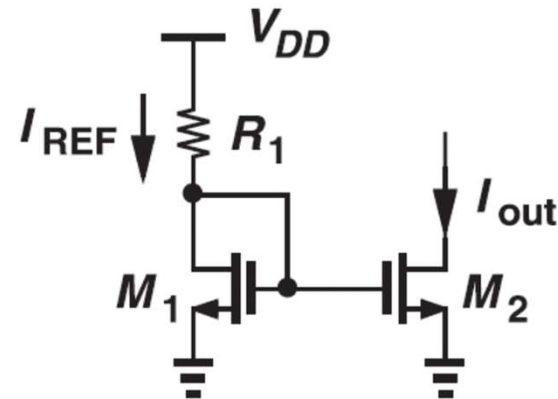
- Supply-Independent Biasing
- Temperature-Independent References
- PTAT Current Generation
- Constant- G_m Biasing
- Speed and Noise Issues
- Low-Voltage Bandgap References
- Case Study

電流鏡偏壓



(a)

(a)理想電流源



(b)

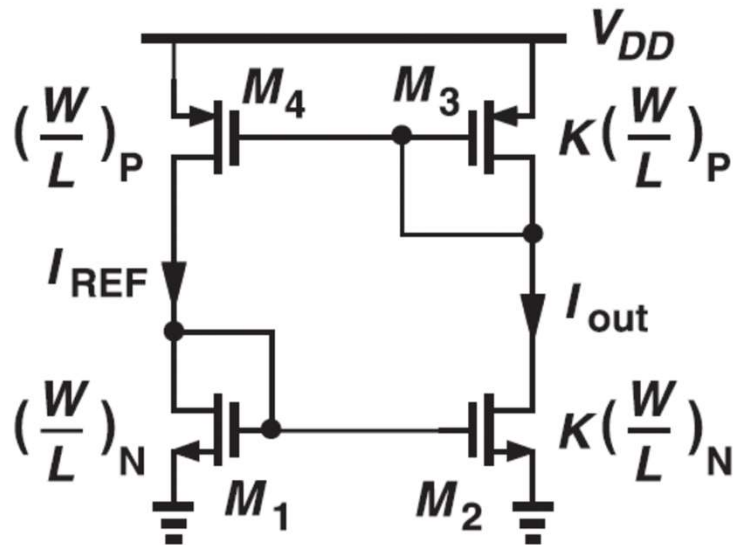
(b)電阻之電流鏡偏壓

如果 I_{REF} 不會隨著 V_{DD} 而改變且 M_2 和 M_3 之通道長度調變可忽略時，則 I_{D2} 和 I_{D3} 和供應電壓無關。

$$\Delta I_{out} = \frac{\Delta V_{DD}}{R_1 + 1/g_{m1}} \cdot \frac{(W/L)_2}{(W/L)_1}$$

Supply-Independent Biasing

建立和供應電源無關之電流的簡單電路



如果通道長度調變可忽略時

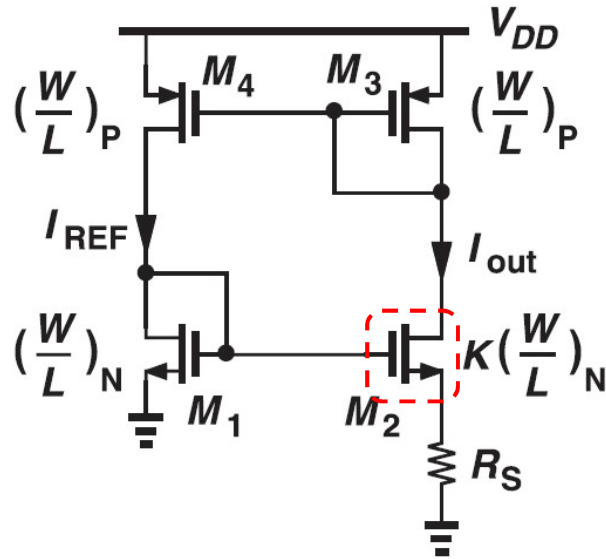
$$I_{out} = KI_{REF}$$

I_{REF} is still process-dependent, not **well-controlled**

Is there any problem for this circuit?

- It needs a start-up circuit to make it alive ($I_{out}=0$ or ?)

Supply-Independent Biasing



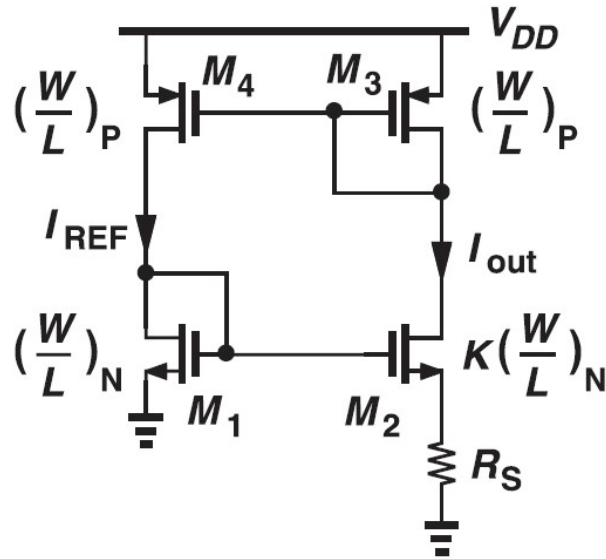
(a)

(a) 加入 R_S 以定義電流

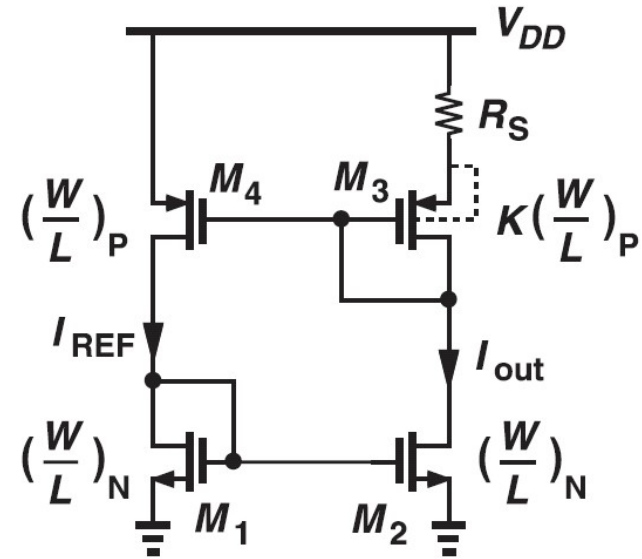
$$V_{GS1} = V_{GS2} + I_{D2} R_S$$

$$\sqrt{\frac{2I_{out}}{\mu_n C_{ox} (W/L)_N}} + V_{TH1} = \sqrt{\frac{2I_{out}}{\mu_n C_{ox} K(W/L)_N}} + V_{TH2} + I_{out} R_S$$

Supply-Independent Biasing



(a)



(b)

忽略基板效應

$$\sqrt{\frac{2I_{out}}{\mu_n C_{ox} (W/L)_N}} \left(1 - \frac{1}{\sqrt{K}}\right) = I_{out} R_S$$

$$I_{out} = \frac{2}{\mu_n C_{ox} (W/L)_N} \cdot \frac{1}{R_S^2} \left(1 - \frac{1}{\sqrt{K}}\right)^2$$



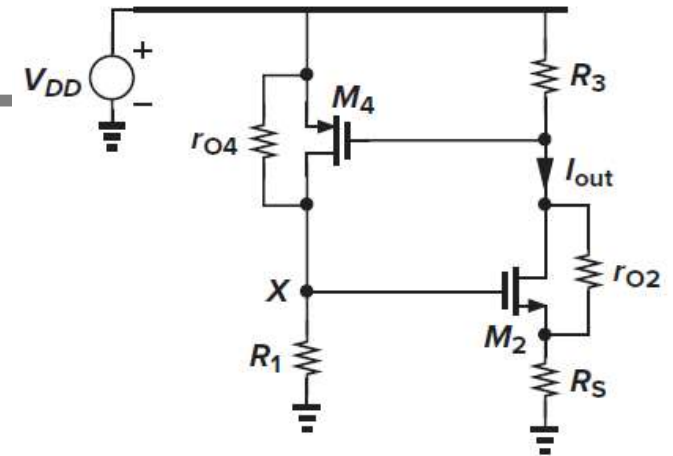
I_{out} 與 V_{DD} 無關!!

If more non-ideal effects, ...

例題 12.1

假設在圖12.3(a)中 $\lambda \neq 0$ ，當供應電壓改變 ΔV_{DD} 時，
計算 I_{out} 之變化為何？

答：



將電路簡化為圖12.4所示之電路，其中 $R_1 = r_{O1} \parallel (1/g_{m1})$ 且 $R_3 = r_{O3} \parallel (1/g_{m3})$ ，
我們計算由 V_{DD} 至 I_{out} 的增益， M_4 之小信號閘極-源極電壓為 $-I_{out}R_3$ 且
流經 r_{O4} 之電流為 $(V_{DD} - V_X)/r_{O4}$ 。因此，
$$\frac{V_{DD} - V_X}{r_{O4}} + I_{out}R_3g_{m4} = \frac{V_X}{R_1}$$

如果我們以 $G_m = I_{out}/V_X$ 來象徵 M_2 的

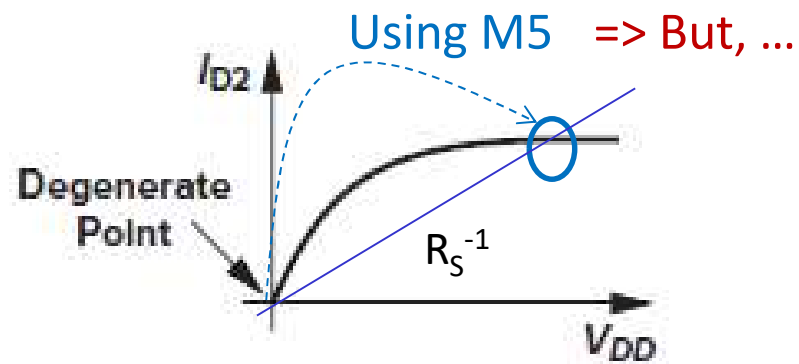
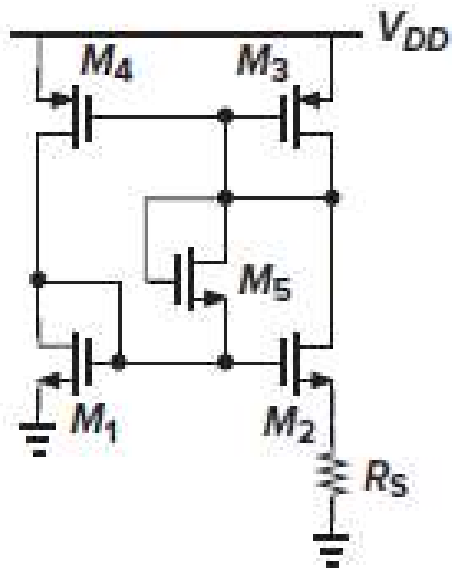
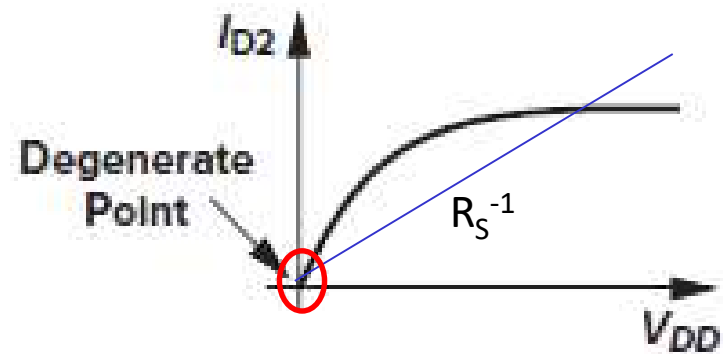
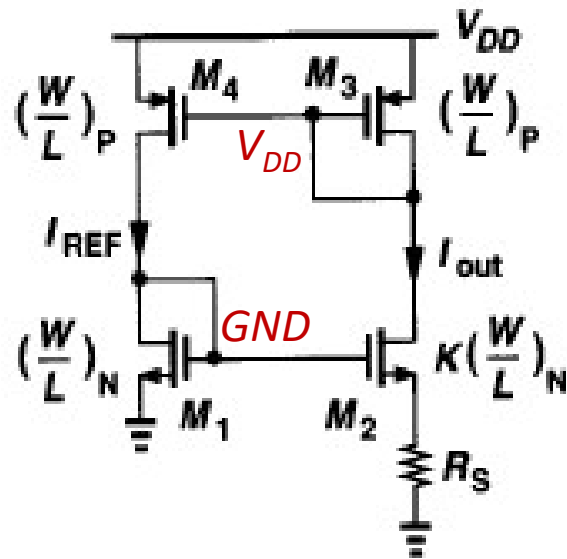
等效轉導時，則

$$\frac{I_{out}}{V_{DD}} = \frac{1}{r_{O4}} \left[\frac{1}{G_{m2}(r_{O4} \parallel R_1)} - g_{m4}R_3 \right]^{-1}$$

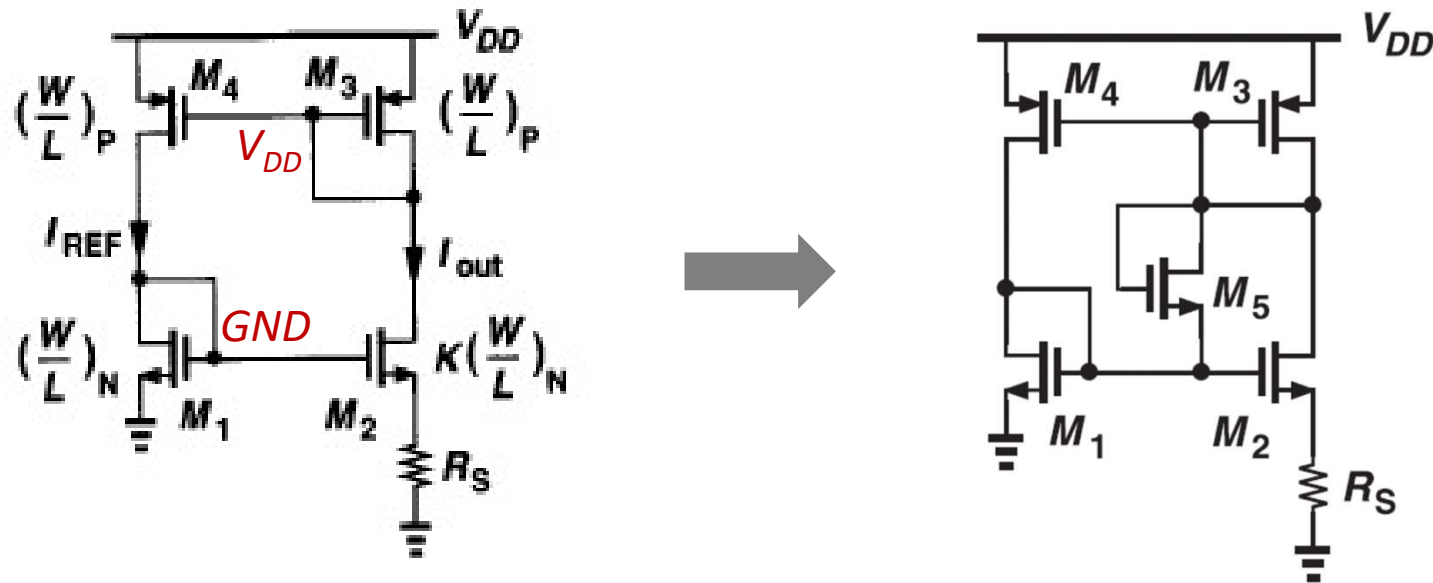
注意從第三章中得知 $G_{m2} = \frac{g_{m2}}{1 + (g_{m2} + g_{mb2})R_S}$

有趣地是，如果 $r_{O4} = \infty$ ，靈敏度將會消失(Ideal case!!)。

起始問題



起始問題



Major considerations for a feedback circuit:

- 加入一個驅動電路離開退化偏壓點之機制來解決起始問題
- 驅動電路本身不應在偏壓正常後繼續動作 (*)

與溫度無關的參考電壓

- 如何產生一個與溫度無關的參考電壓，供晶片做為電壓基準使用？
- 為什麼我們在意：參考電壓要與溫度無關？
- 與溫度有關之物理量(幾乎所有材料)
 - V_T : kT/q (positive TC)
 - V_{BE} : $\partial V_{BE}/\partial T \sim -2\text{mV}/^\circ\text{C}$ (negative TC)
 - $\Delta V_{BE} \propto T$ (positive TC)
 - Resistors (positive or negative TC)
 - MOSFETs in Subthreshold region

負溫度係數電壓 (Negative-TC)

對一個雙載子元件而言， $I_C = I_S \exp(V_{BE}/V_T)$ 。其中 $V_T = kT/q$ ，

$$I_S = bT^{4+m} \exp \frac{-E_g}{kT} \quad (\text{課本有推導!!}) \quad E_g \sim 1.12 \text{ eV}$$

$$V_{BE} = V_T \ln(I_C/I_S), \quad \frac{\partial V_{BE}}{\partial T} = \frac{\partial V_T}{\partial T} \ln \frac{I_C}{I_S} - \frac{V_T}{I_S} \frac{\partial I_S}{\partial T} \quad (\text{Assume } I_C \text{ is constant?})$$

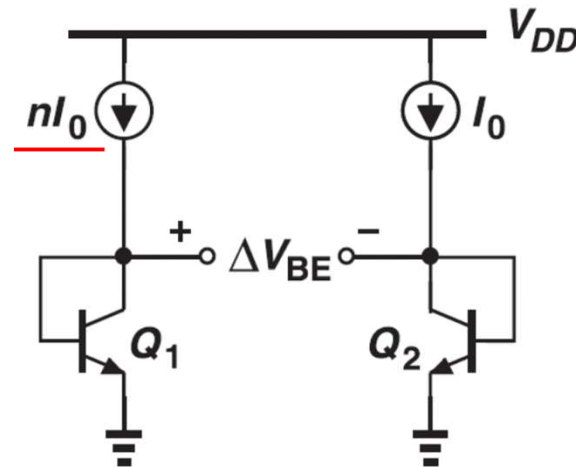
$$\frac{\partial I_S}{\partial T} = b(4+m)T^{3+m} \exp \frac{-E_g}{kT} + bT^{4+m} \left(\exp \frac{-E_g}{kT} \right) \left(\frac{E_g}{kT^2} \right)$$

$$\frac{V_T}{I_S} \frac{\partial I_S}{\partial T} = (4+m) \frac{V_T}{T} + \frac{E_g}{kT^2} V_T$$

$$\frac{\partial V_{BE}}{\partial T} = \frac{V_T}{T} \ln \frac{I_C}{I_S} - (4+m) \frac{V_T}{T} - \frac{E_g}{kT^2} V_T = \underline{\underline{\frac{V_{BE} - (4+m)V_T - E_g/q}{T}}}$$

假設 $V_{BE} \doteq 750 \text{ mV}$ 且在 $T = 300^\circ \text{K}$ 時， $\underline{\underline{\partial V_{BE} / \partial T \approx -1.5 \text{ mV} / \text{K}}}$

正溫度係數電壓 (Positive-TC)



PTAT電壓的產生

$$\Delta V_{BE} = V_{BE1} - V_{BE2} = V_T \ln \frac{nI_0}{I_{S1}} - V_T \ln \frac{I_0}{I_{S2}} = V_T \ln n$$

$$\frac{\partial \Delta V_{BE}}{\partial T} = \frac{k}{q} \ln n$$

Too small!!

例題 12.3

計算圖11.7電路之 ΔV_{BE} 。

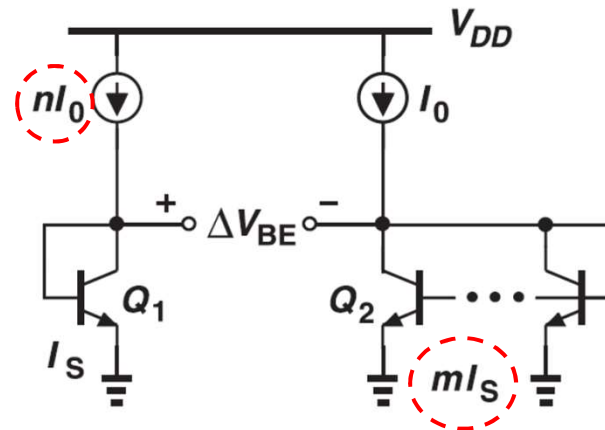


圖 11.7

答：

忽略基極電流，我們寫成

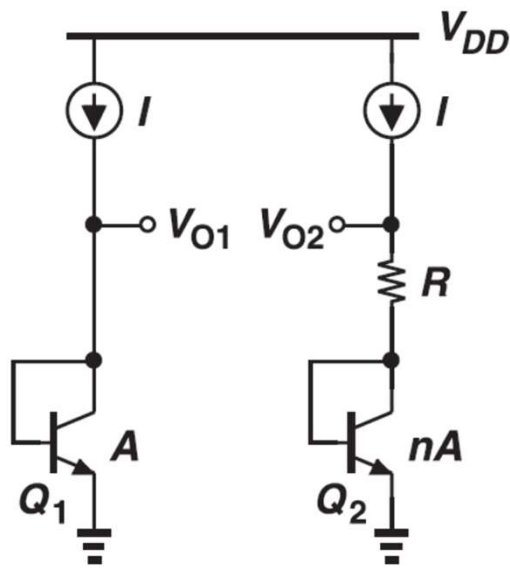
$$\Delta V_{BE} = V_T \ln \frac{nI_0}{I_S} - V_T \ln \frac{I_0}{mI_S} = V_T \ln(nm)$$

因此溫度係數為 $(k/q)\ln(nm)$ 。

→ Larger than that on the last page

與溫度無關之電壓概念生成圖

$$V_{REF} = \alpha_1 V_{BE} + \alpha_2 (V_T \ln n) \Rightarrow \text{To meet } \partial V_{REF} / \partial T = 0$$



If $V_{O1} \sim V_{O2}$,

$$V_{BE1} = RI + V_{BE2}$$

$$RI = V_{BE1} - V_{BE2} = V_T \ln(n)$$

$$V_{O2} = V_{BE2} + IR = V_{BE2} + V_T \ln(n)$$

To get V_{O2} is T-independent

$$\ln(n) = 17.2$$

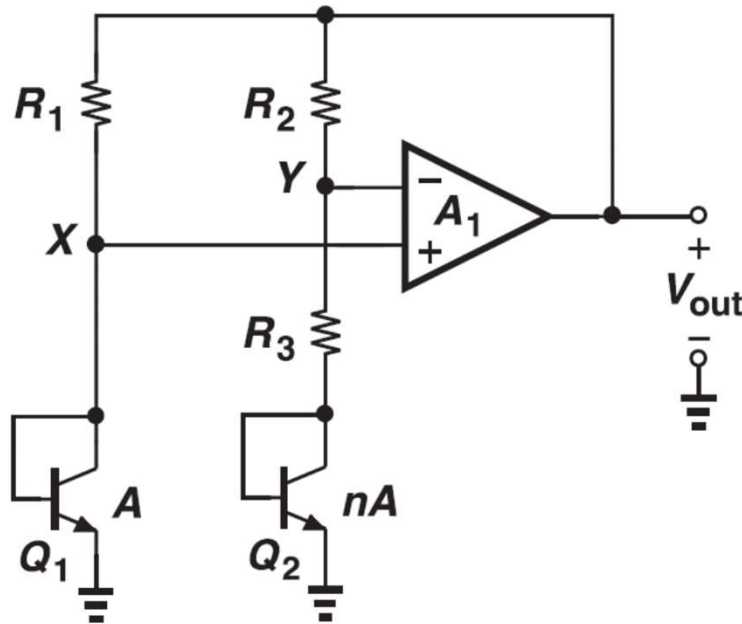
因為 $\alpha_1 = \alpha_2 = 1$ ，選擇 $\ln(n)$ 使得 $(\alpha_2 \ln n)(0.087 \text{ mV/K}) = 1.5 \text{ mV/K}$ 。

$n = 3 \times 10^7$ (quite large!!) \rightarrow We need a smaller $\ln(n)$

$$V_{REF} = V_{BE} + 17.2 V_T \approx 1.25 V$$

與溫度無關電壓觀念電路的實現

A conventional *Bandgap reference* circuit



If $V_{O1} \sim V_{O2} \Rightarrow$ using opamp!!

$$V_{out} = V_{BE2} + \frac{V_T \ln n}{R_3} (R_3 + R_2) = V_{BE2} + (V_T \ln n) \left(1 + \frac{R_2}{R_3} \right)$$

To achieve a smaller n !!

與溫度無關電壓觀念電路的實現

$$V_{BE} = V_T \ln(I_C / I_S) \rightarrow \frac{\partial V_{BE}}{\partial T} = \frac{\partial V_T}{\partial T} \ln \frac{I_C}{I_S} - \frac{V_T}{I_S} \frac{\partial I_S}{\partial T}$$

假設 $I_{C1} = I_{C2} \approx (V_T \ln(n)) / R_3$ (I_C is not constant, we need to modify)

$$\frac{\partial V_{BE}}{\partial T} = \frac{\partial V_T}{\partial T} \ln \frac{I_C}{I_S} + V_T \left(\frac{1}{I_C} \frac{\partial I_C}{\partial T} - \frac{1}{I_S} \frac{\partial I_S}{\partial T} \right)$$

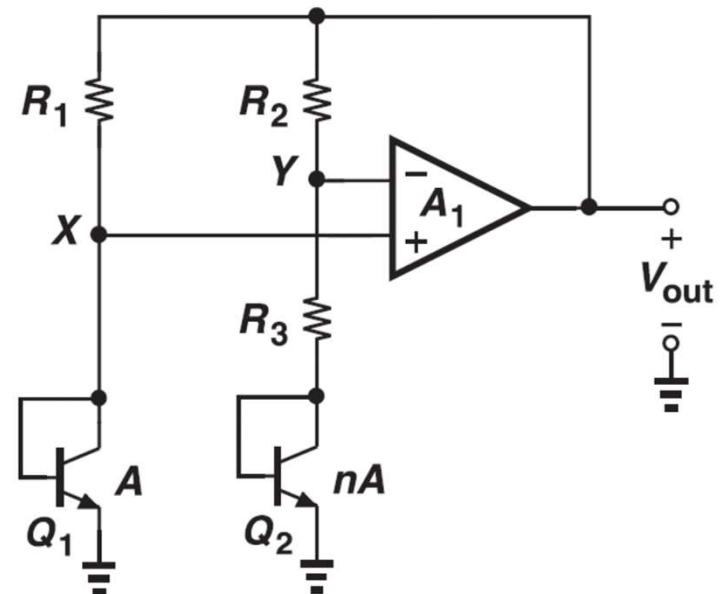
因為 $\partial I_C / \partial T \approx (V_T \ln n) / (R_3 T) = I_C / T$

$$\frac{\partial V_{BE}}{\partial T} = \frac{\partial V_T}{\partial T} \ln \frac{I_C}{I_S} + \boxed{\frac{V_T}{T}} - \frac{1}{I_S} \frac{\partial I_S}{\partial T}$$

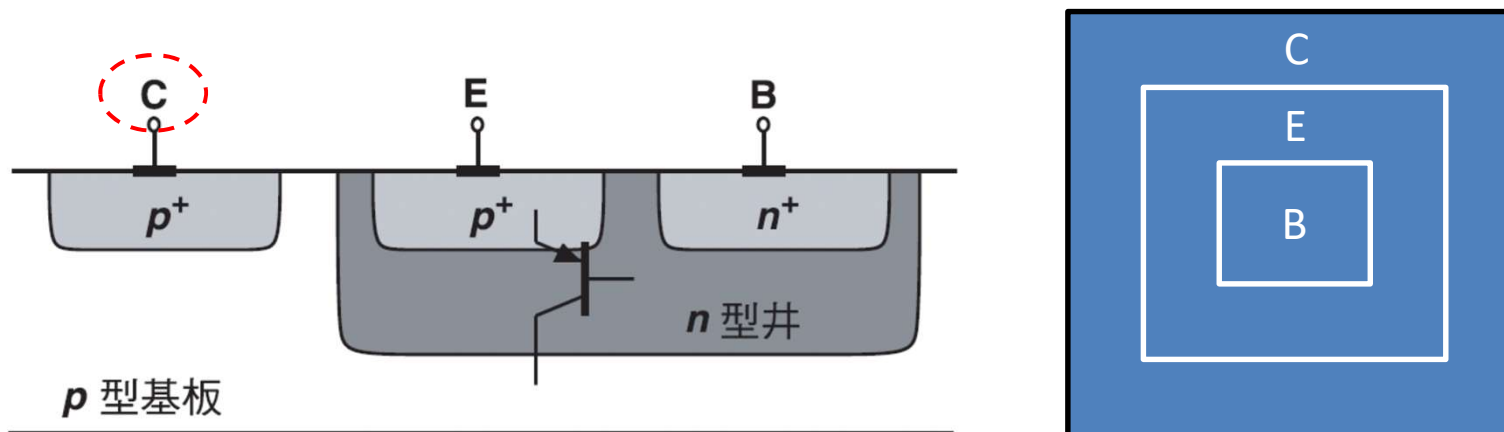
$$\frac{\partial V_{BE}}{\partial T} = \frac{V_{BE} - (3 + m)V_T - E_g / q}{T}$$

not (4+m)

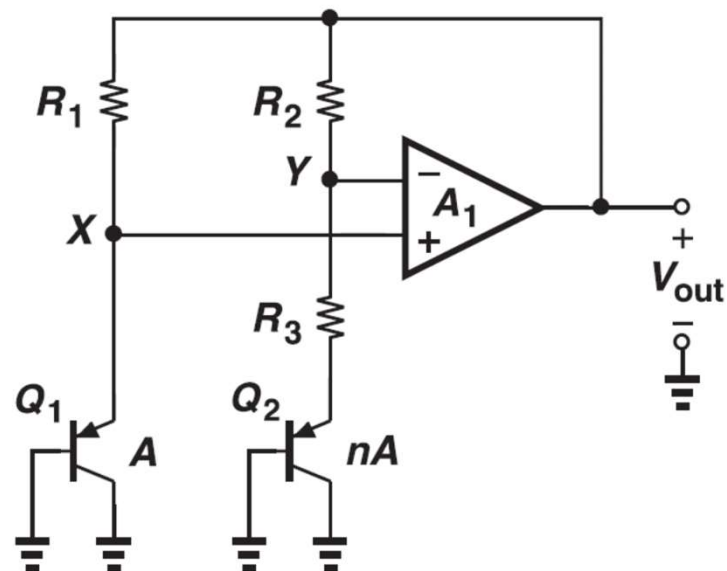
顯示出 TC 比 $-1.5\text{mV}/^\circ\text{K}$ 略小。



BJT與CMOS技術之相容性

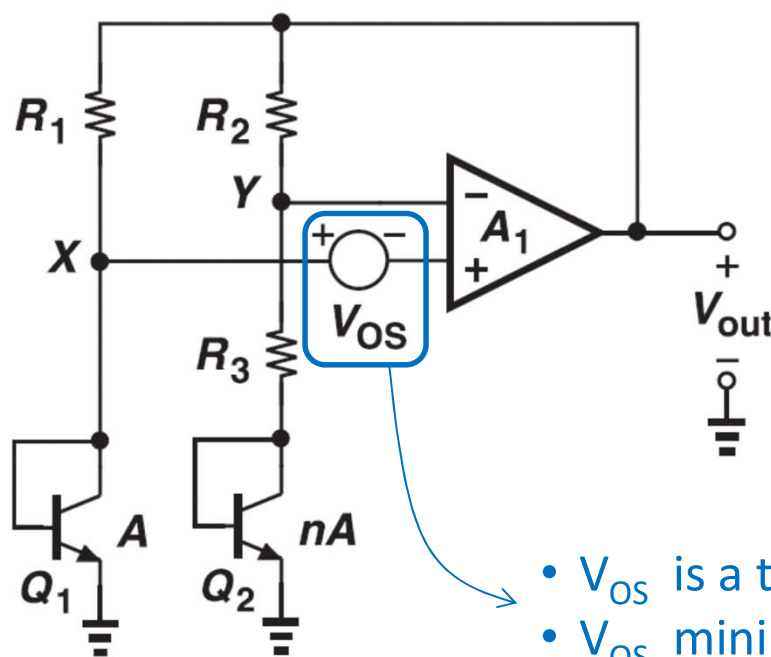


在CMOS技術中實現一 *pnp* 雙載子電晶體(from PDK)



PDK: Process Design Kit

運算放大器偏移和輸出阻抗



A: area of unit BJT
Larger area => larger I_s
 $V_{BE} = V_T \ln(I_c/I_s)$

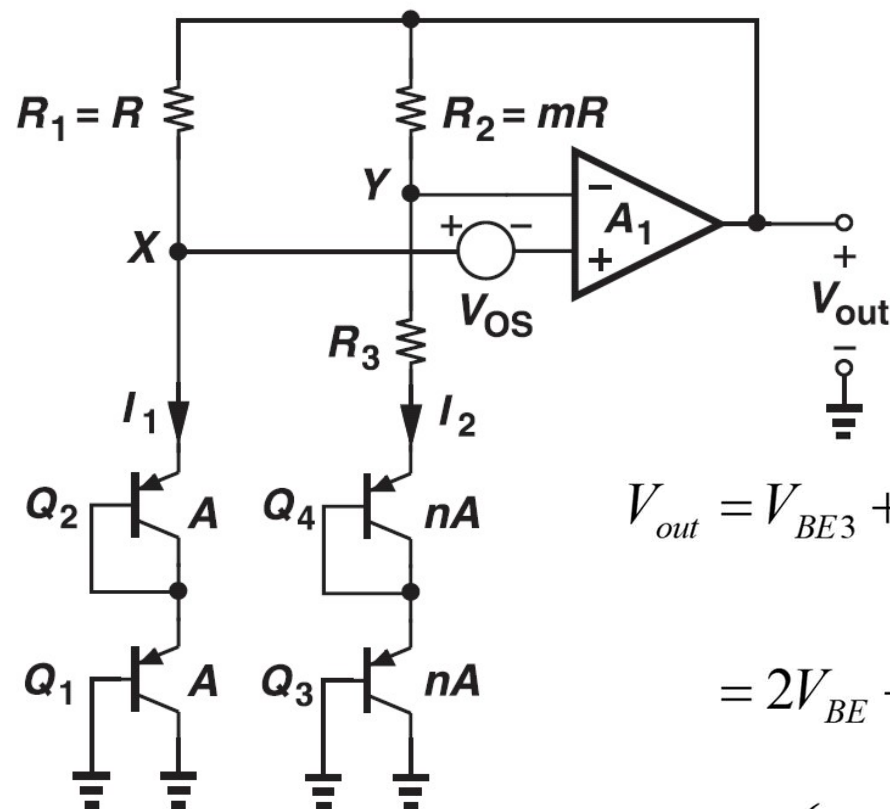
- V_{OS} is a temp-dependent factor
- V_{OS} minimization is necessary

運算放大器偏移對參考電壓的影響。

$$V_{BE1} - V_{OS} \approx V_{BE2} + R_3 I_{C2} \quad \text{且} \quad V_{out} = V_{BE2} + (R_3 + R_2) I_{C2}$$

$$V_{out} = V_{BE2} + (R_3 + R_2) \frac{V_{BE1} - V_{BE2} - V_{OS}}{R_3} = V_{BE2} + \left(1 + \frac{R_2}{R_3}\right) (V_T \ln n - \underline{V_{OS}})$$

運算放大器偏移效應的降低



Correction ($V_{BE} \Rightarrow V_{EB}$)

$$V_{BE1} + V_{BE2} - V_{OS} = V_{BE3} + V_{BE4} + R_3 I_2$$

$$V_{out} = V_{BE3} + V_{BE4} + (R_3 + R_2) I_2$$

$$V_{out} = V_{BE3} + V_{BE4} + (R_3 + R_2) \frac{2V_T \ln(mn) - V_{OS}}{R_3}$$

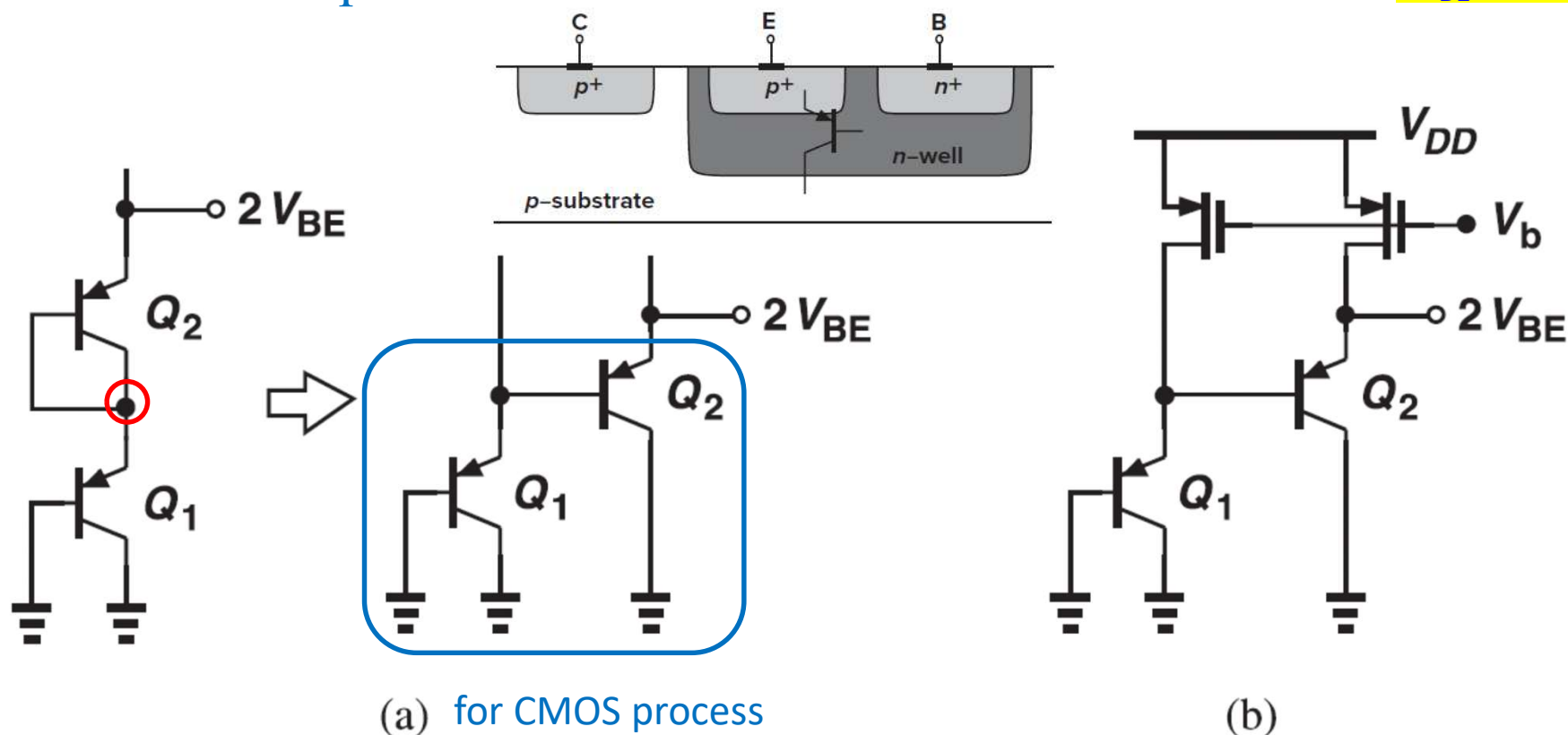
$$= 2V_{BE} + \left(1 + \frac{R_2}{R_3}\right) [2V_T \ln(mn) - V_{OS}]$$

$$= 2 \left(V_{BE} + \left(1 + \frac{R_2}{R_3}\right) \left[V_T \ln(mn) - \frac{V_{OS}}{2} \right] \right) \text{ Only half!!}$$

- V_{out} will be 2.5V, not a good solution
- A better solution is using the offset-compensated opamp (using auto-zero, chopper or else)

運算放大器偏移和輸出阻抗

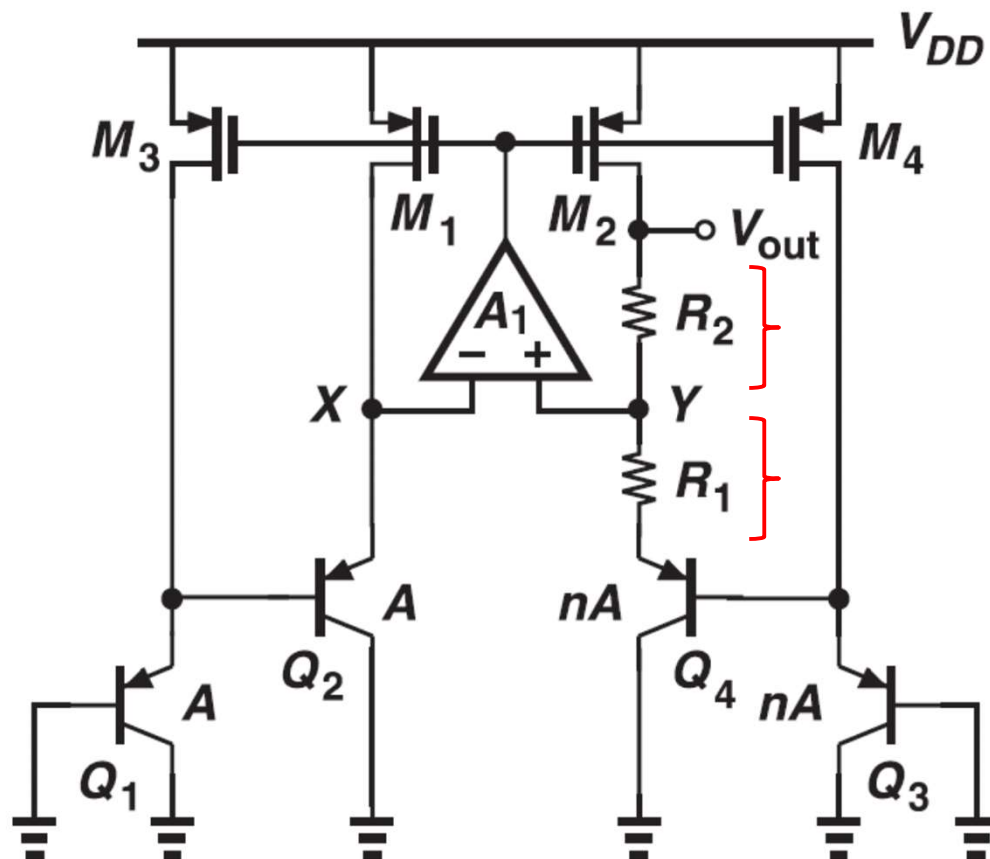
BJTs in CMOS process: the E-B-C structure

$$(V_{BE} \Rightarrow V_{EB})$$


(a) 串聯二極體轉換為一集極接地之組態；

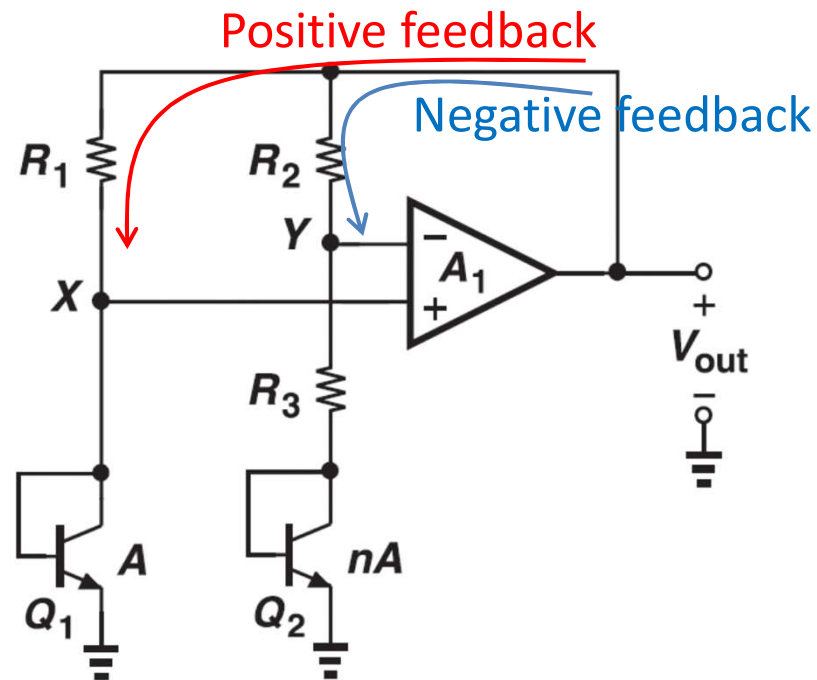
(b) 以PMOS電流源偏壓(a)中的電路。

運算放大器偏移和輸出阻抗



利用二個串聯基極-射極電壓之參考電路產生器

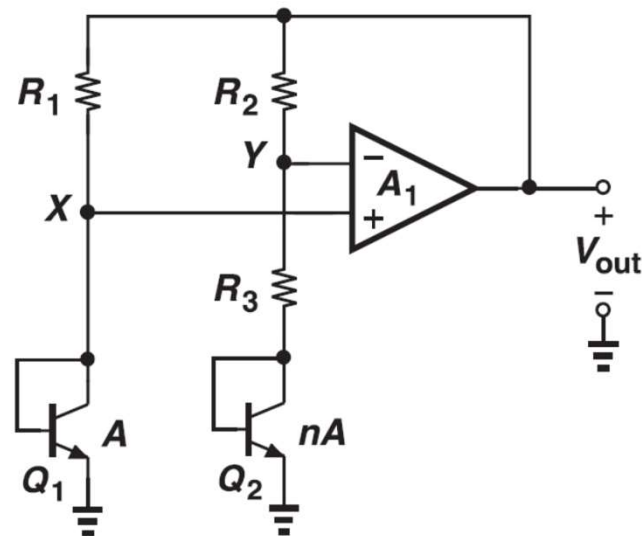
回授極性



Q: We have both positive and negative loops.
What is the stability? Is it stable or not?

A: Of course, it must be stable

回授極性



運算放大器所產生之回授信號將會回傳至其輸入端，

負回授因子給定為
$$\beta_N = \frac{1/g_{m2} + R_3}{1/g_{m2} + R_3 + R_2}$$

而正回授因子為
$$\beta_P = \frac{1/g_{m1}}{1/g_{m1} + R_1}$$

為確保整體回授為負， β_P 必須小於 β_N 。

帶差參考電壓 (Bandgap Voltage)

$$V_{REF} = V_{BE} + V_T \ln n$$

$$I_S = bT^{4+m} \exp \frac{-E_g}{kT}$$

$$\frac{\partial V_{REF}}{\partial T} = \frac{\partial V_{BE}}{\partial T} + \frac{V_T}{T} \ln n$$

$$\frac{\partial V_{BE}}{\partial T} = \frac{V_{BE} - (4+m)V_T - E_g / q}{T}$$

如果 $\frac{\partial V_{REF}}{\partial T}$ 為零

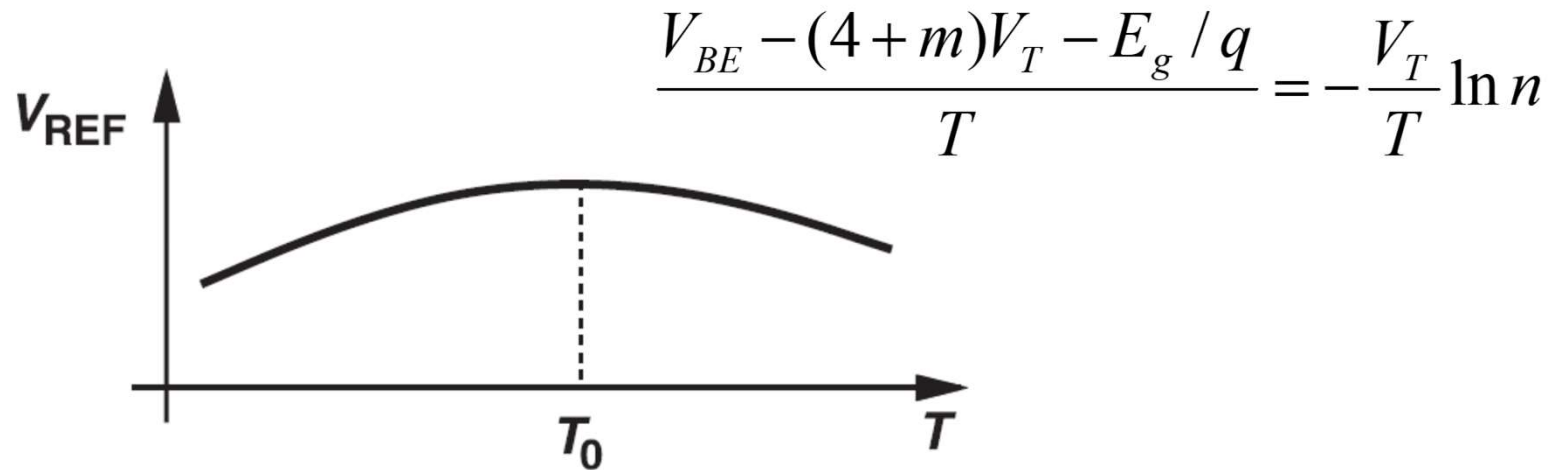
$$\frac{V_{BE} - (4+m)V_T - E_g / q}{T} = -\frac{V_T}{T} \ln n$$

$$\rightarrow V_{REF} = \frac{E_g}{q} + (4+m)V_T$$

$$T \rightarrow 0 \Rightarrow V_{REF} \rightarrow E_g / q$$

$E_g \sim 1.12\text{eV}$, called the bandgap energy of *Silicon*

帶差參考電壓:曲率校正



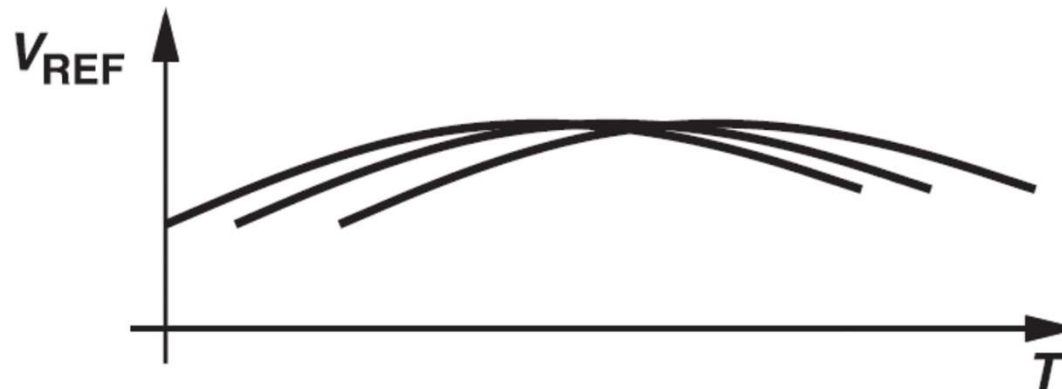
帶差電壓對於溫度相關性之曲率



單點校正

or

多點校正

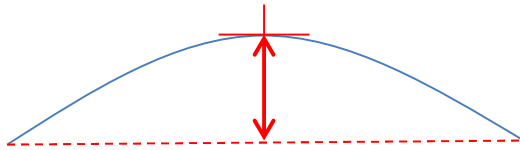


對不同範例而言，零 TC 溫度的變化

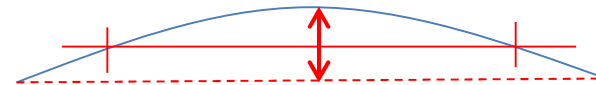
帶差參考電壓:曲率校正

單點校正 or 多點校正

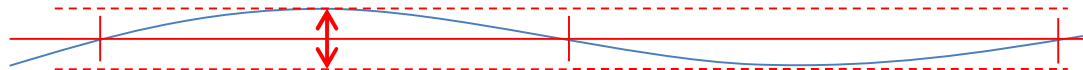
單點校正



兩點校正

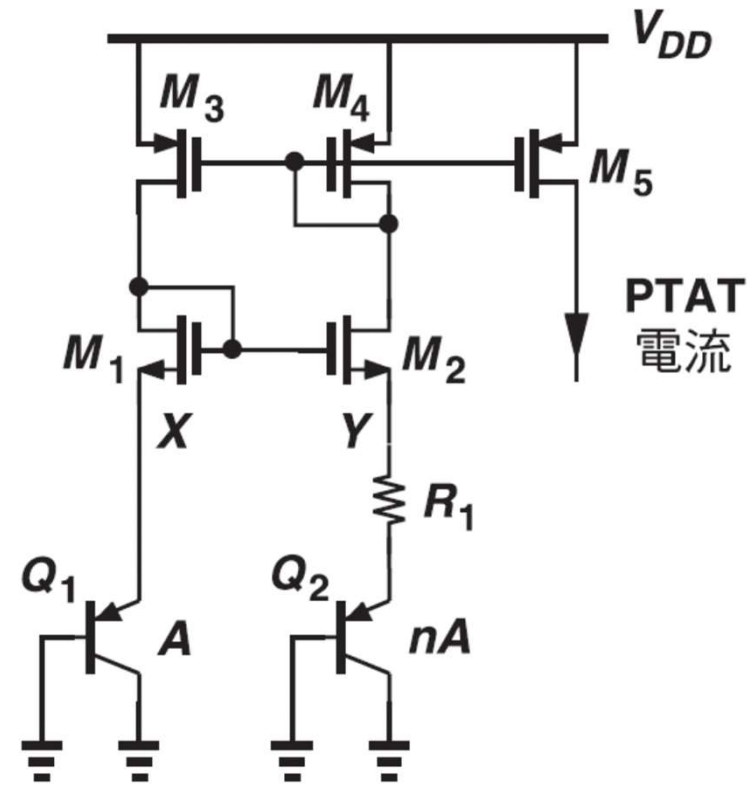
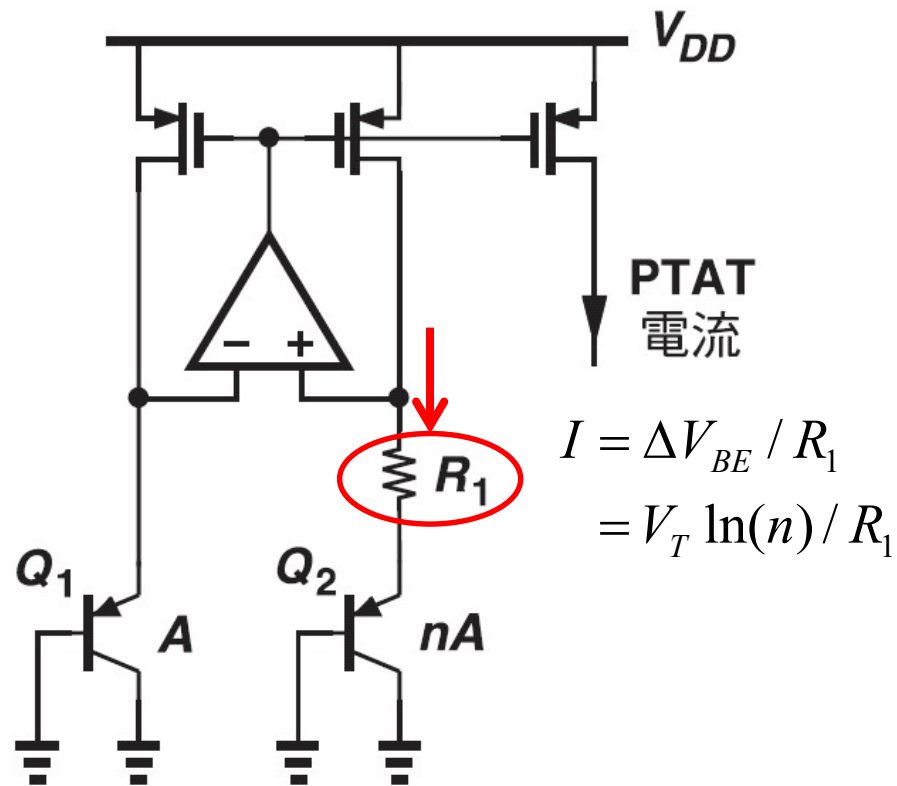


三點校正



對一般產品來說，最好 V_{ref} 是可以被調整到一個固定值!!
即便在溫度範圍內有些微變化，其絕對值是最重要的!!

PTAT 電流生成

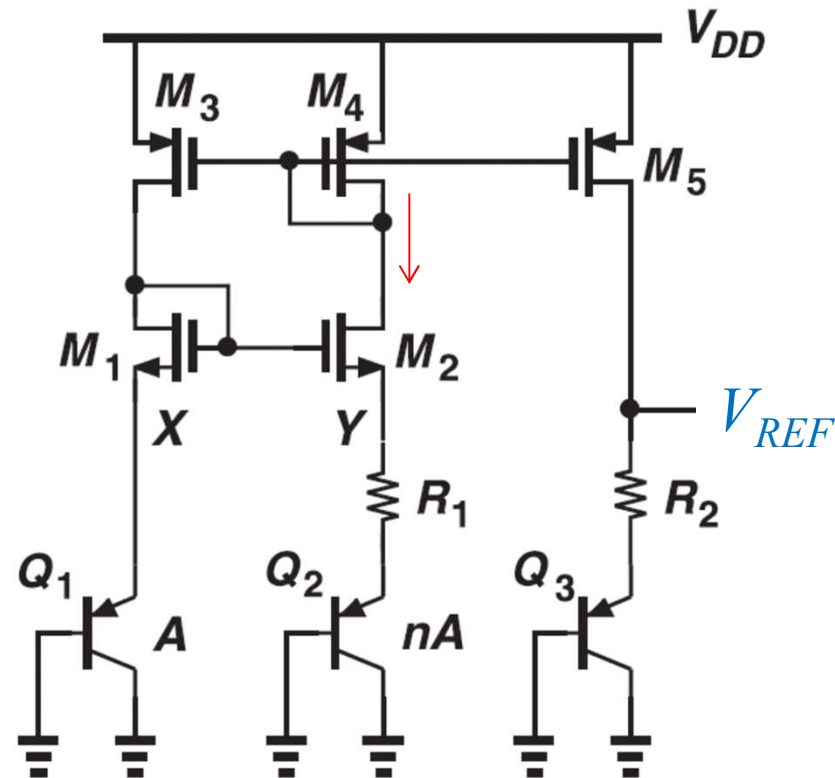


PTAT 電流之生成 (溫度感測)

利用一簡單放大器產生 PTAT 電流

Q: How about R_1 ?

與溫度無關電壓的另一實現

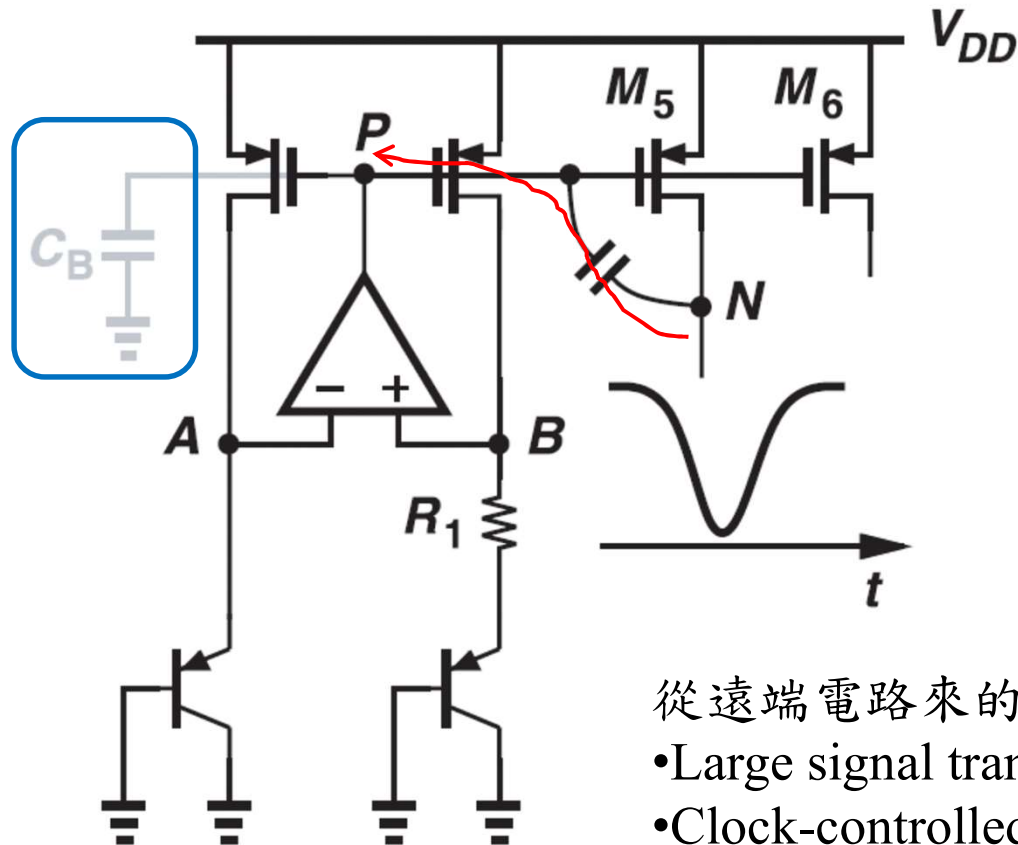


產生與溫度無關之電壓。

$$V_{REF} = V_{BE3} + \frac{R_2}{R_1} V_T \ln n$$

速度和雜訊問題

Bypass cap
But,

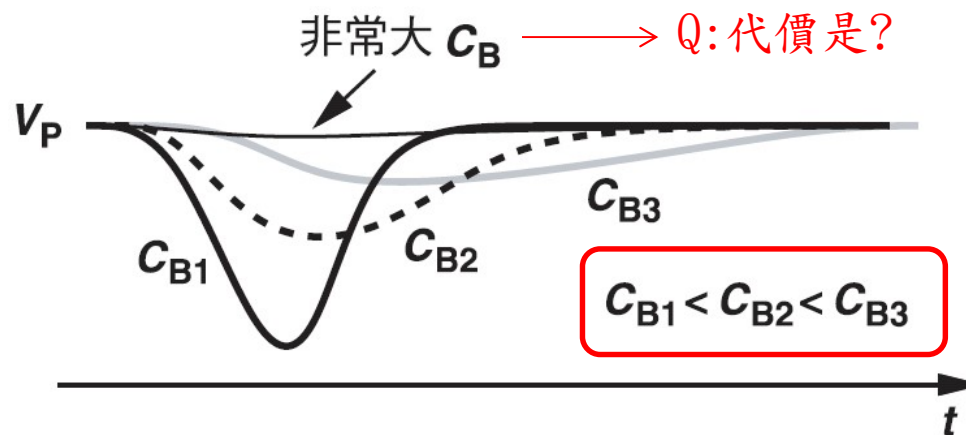


從遠端電路來的kickback noise:

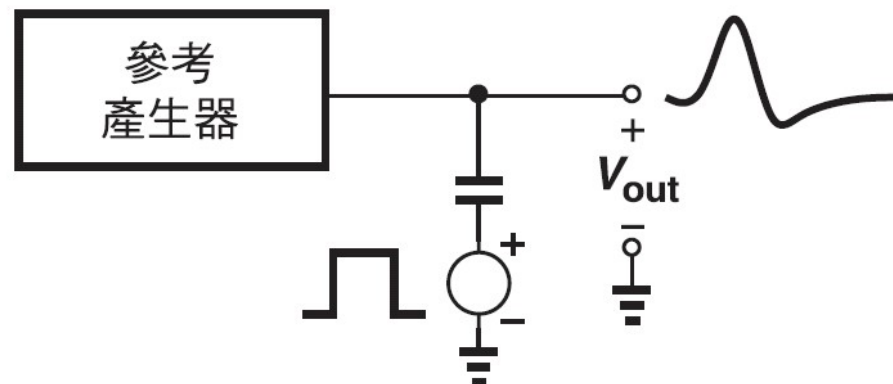
- Large signal transition
- Clock-controlled signal (switch-capacitor circuit)

電路的暫態行為對參考電壓和電流的影響

速度和雜訊問題



增加旁路電容對參考產生器響應的影響



測試參考產生器暫態響應的機制 (Test bench)

例題 12.7

決定圖12.23所示之帶差參考電路的小信號輸出阻抗並檢查其隨著頻率變化的特性。

答：

圖12.26

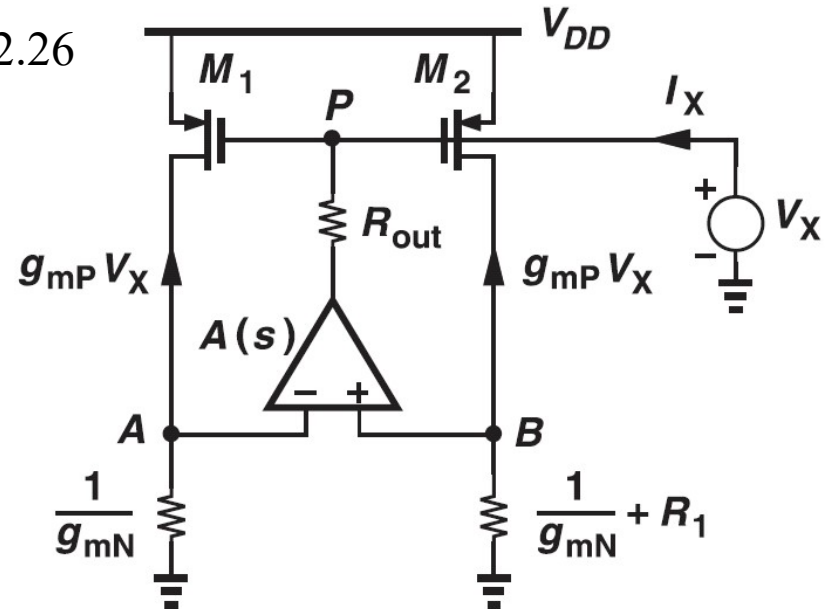


圖12.26顯示其等效電路，並以一單極點轉移函數 $A(s)=A_0/(1+s/\omega_0)$ 和輸出電阻 R_{out} 建立開路迴路運算放大器之模型，以及以電阻 $1/g_{mN}$ 建立每個BJT的模型。如果 M_1 和 M_2 相同，其轉導皆為 g_{mP} ，則其汲極電流為 $g_{mP}V_X$ ，在運算放大器之輸入端產生一差動電壓為

$$V_{AB} = -g_{mP}V_X \frac{1}{g_{mN}} + g_{mP}V_X \left(\frac{1}{g_{mN}} + R_1 \right) = g_{mP}V_X R_1$$

例題 12.7 〈續〉

答：

流經 R_{out} 之電流為

$$I_X = \frac{V_X + g_{mP} V_X R_1 A(s)}{R_{out}}$$

產生

$$\begin{aligned} \frac{V_X}{I_X} &= \frac{R_{out}}{1 + g_{mP} R_1 A(s)} = \frac{R_{out}}{1 + g_{mP} R_1 \frac{A_0}{1 + s/\omega_0}} \\ &= \frac{R_{out}}{\underline{1 + g_{mP} R_1 A_0}} \cdot \frac{1 + \frac{s}{\omega_0}}{1 + \frac{s}{(1 + g_{mP} R_1 A_0)\omega_0}} \end{aligned}$$

因此，輸出阻抗顯示了一位於 ω_0 之零點和一極點位於 $(1 + g_{mP} R_1 A_0)\omega_0$ 。

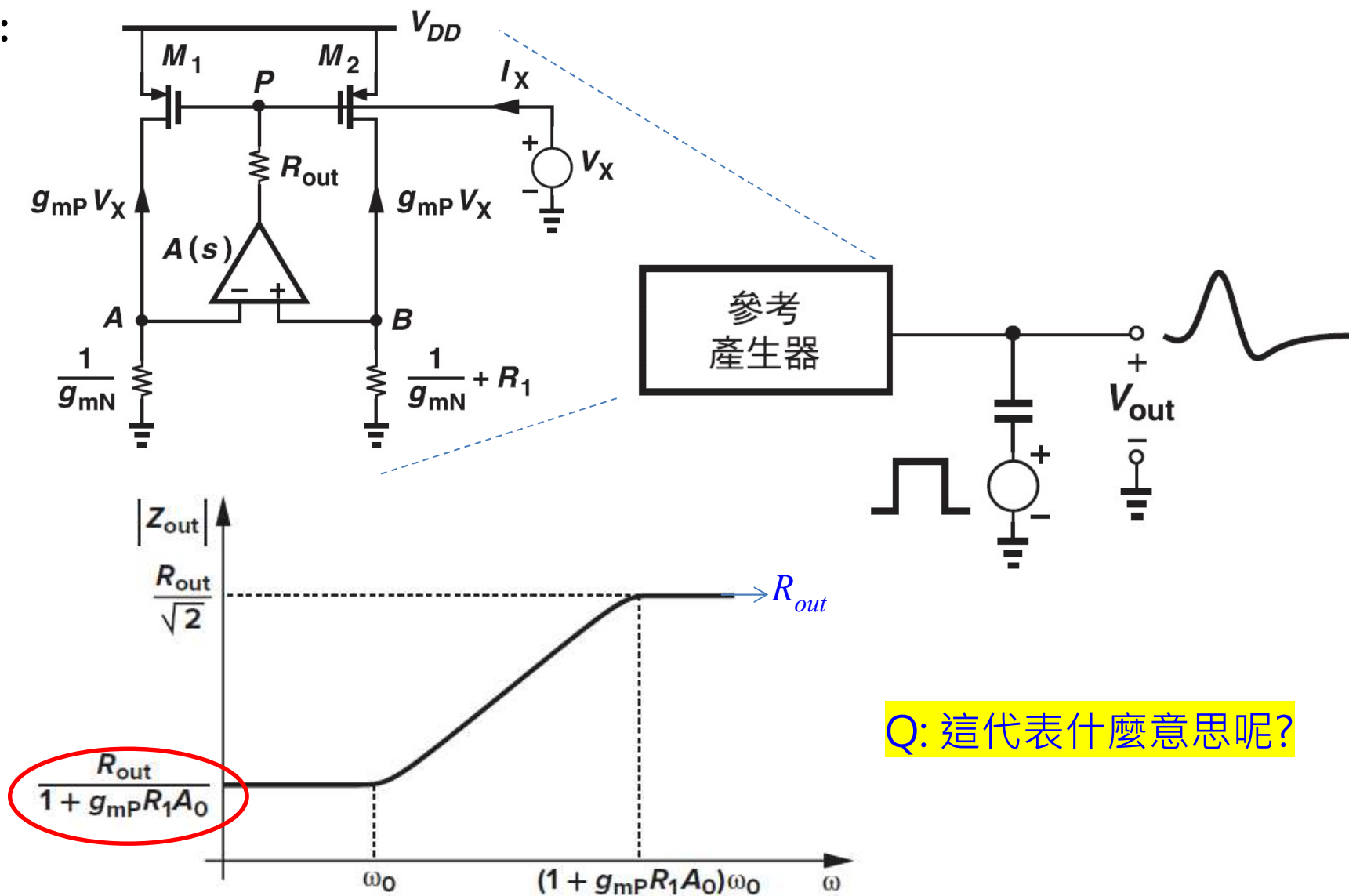
注意對 $\omega \ll \omega_0$ 而言， $|Z_{out}|$ 相當低，但是當頻率接近極點頻率時將會上升至一很高的值。事實上，設定 $\omega = (1 + g_{mP} R_1 A_0)\omega_0$ 並假設 $g_{mP} R_1 A_0 \gg 1$ ，我們得到

$$|Z_{out}| = \frac{R_{out}}{1 + g_{mP} R_1 A_0} \left| \frac{1 + j(1 + g_{mP} R_1 A_0)}{1 + j} \right| = \frac{R_{out}}{\underline{\sqrt{2}}}$$

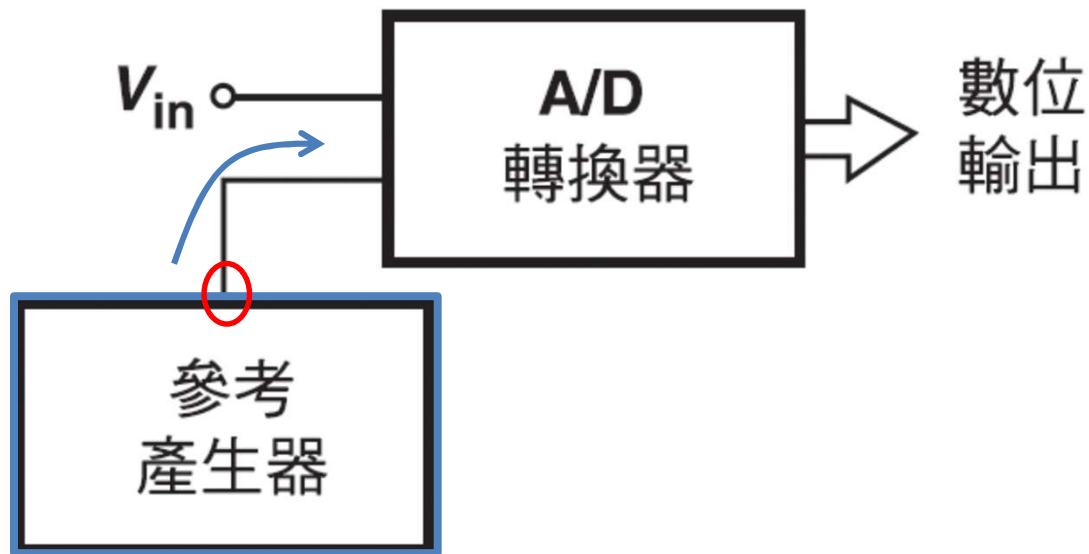
只比開路迴路值低 30%。

例題 12.7 〈續〉

答：



使用參考產生器之 A/D 轉換器



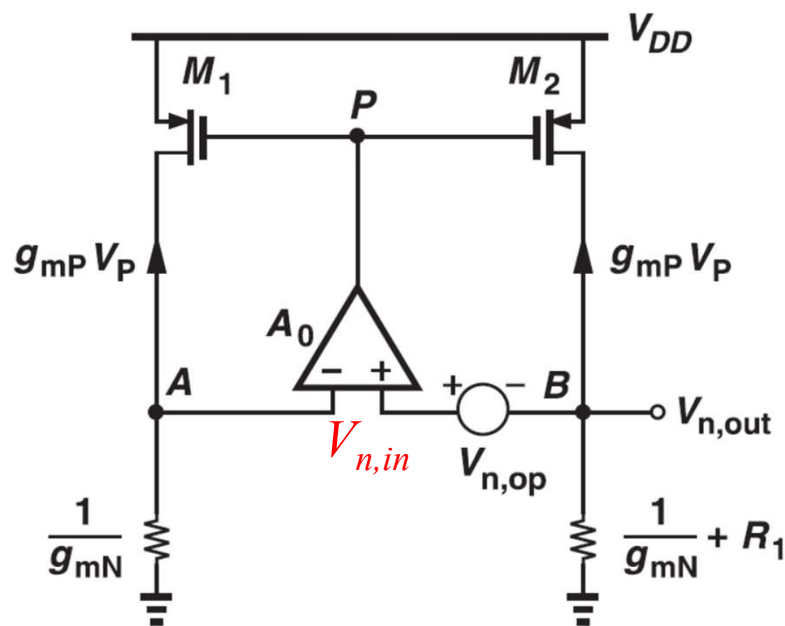
如果高精確 A/D 轉換器使用一帶差電壓作為與類比電路相比較之參考電壓，則在參考電路之雜訊將直接加入輸入端。

⇒ Output referred noise!!

⇒ A reference buffer is necessary

計算參考產生器中雜訊的電路

Firstly, we consider the opamp noise



$$V_{n,in} = -\frac{V_{n,out}}{g_{mP} A_0 (R_1 + g_{mN}^{-1})}$$

$$= (V_{n,op} + V_{n,out}) - \frac{V_{n,out}}{R_1 + g_{mN}^{-1}} \cdot \frac{1}{g_{mN}}$$

V_A

$$V_{n,out} \left[\frac{1}{R_1 + g_{mN}^{-1}} \cdot \left(\frac{1}{g_{mN}} - \frac{1}{g_{mP} A_0} \right) - 1 \right] = V_{n,op}$$

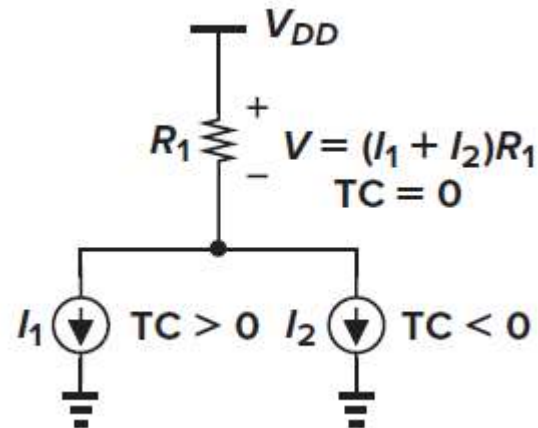
一般來說, $g_{mP} A_0 \gg g_{mN} \gg R_1^{-1}$, $|V_{n,out}| \approx V_{n,op}$

Then, we consider *other components* in the circuit

Appendix

- Low-Voltage Bandgap Reference
- High-Precision Bandgap Reference

Low-Voltage Bandgap Reference

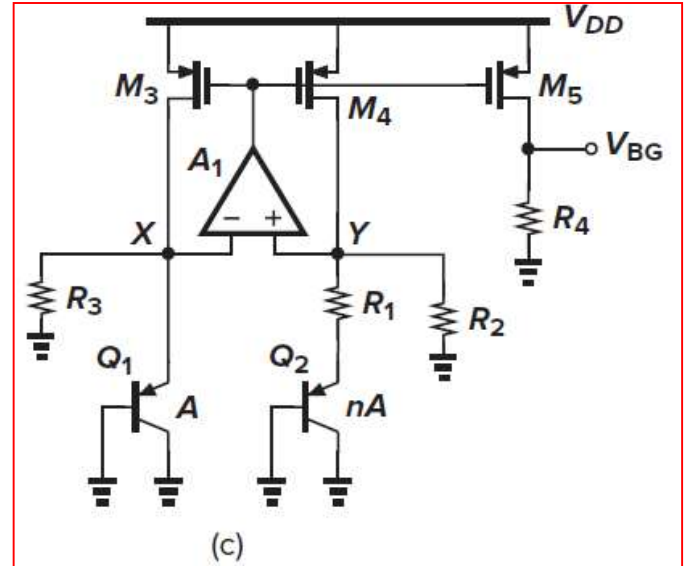
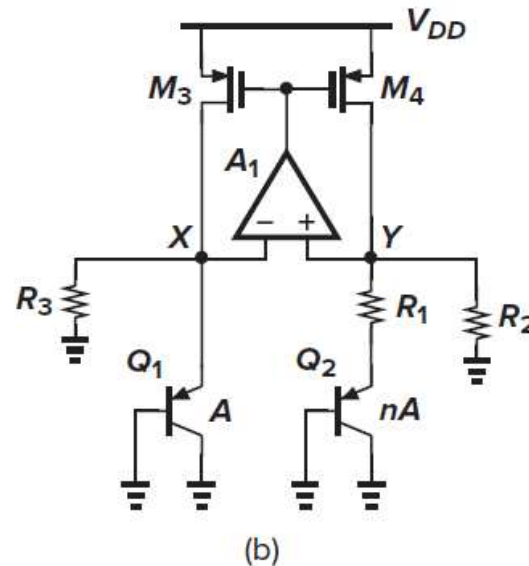
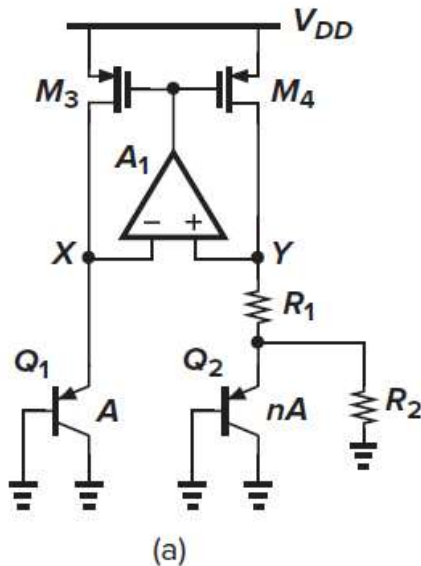


$$I_{C1} + \frac{|V_{BE1}|}{R_3} = I_{C2} + \frac{|V_{BE1}|}{R_2}$$

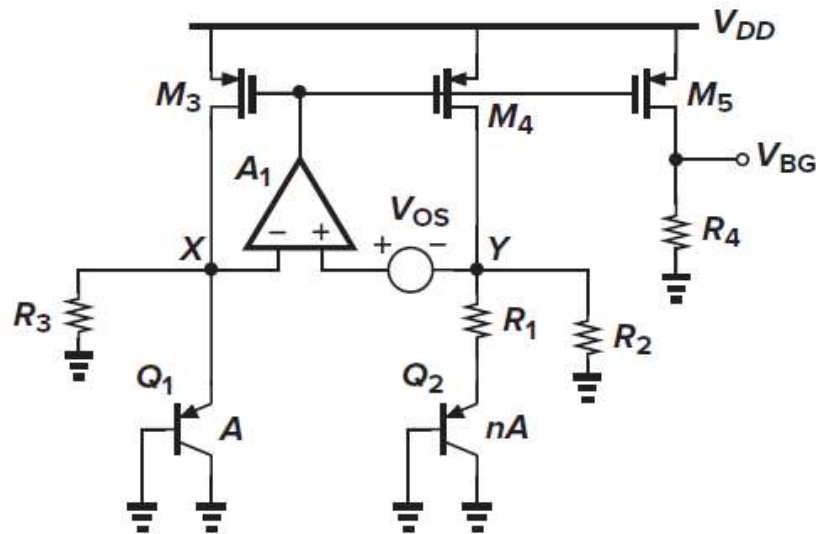
$$|I_{D4}| = \frac{V_T \ln n}{R_1} + \frac{|V_{BE1}|}{R_2}$$

$$= \frac{1}{R_2} \left(|V_{BE1}| + \frac{R_2}{R_1} V_T \ln n \right)$$

$$V_{BG} = \frac{R_4}{R_2} \left(|V_{BE1}| + \frac{R_2}{R_1} V_T \ln n \right)$$



Low-Voltage Bandgap Reference



$$V_X \approx V_Y + V_{OS} \approx |V_{BE1}|$$

$$I_{C1} + \frac{|V_{BE1}|}{R_3} = I_{C2} + \frac{|V_{BE1}| - V_{OS}}{R_2}$$

$$|V_{BE1}| = |V_{BE2}| + R_1 I_{C2} + V_{OS}$$

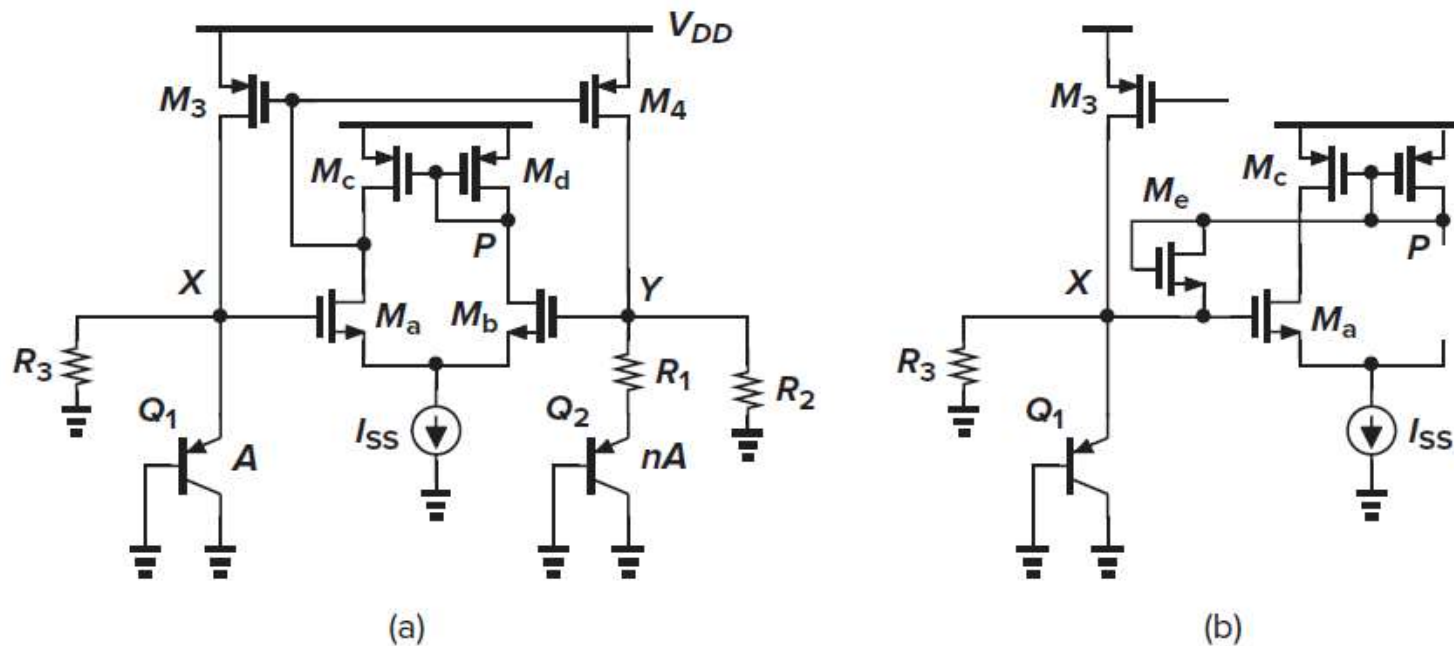
$$I_{C2} = V_T \ln n / R_1 - V_{OS} / R_1$$

$$|I_{D4}| = \frac{V_T \ln n - V_{OS}}{R_1} + \frac{|V_{BE1}| - V_{OS}}{R_2}$$

$$V_{BG} = \frac{R_4}{R_2} \left(|V_{BE1}| + \frac{R_2}{R_1} V_T \ln n \right) - \frac{R_4}{R_1 || R_2} V_{OS}$$

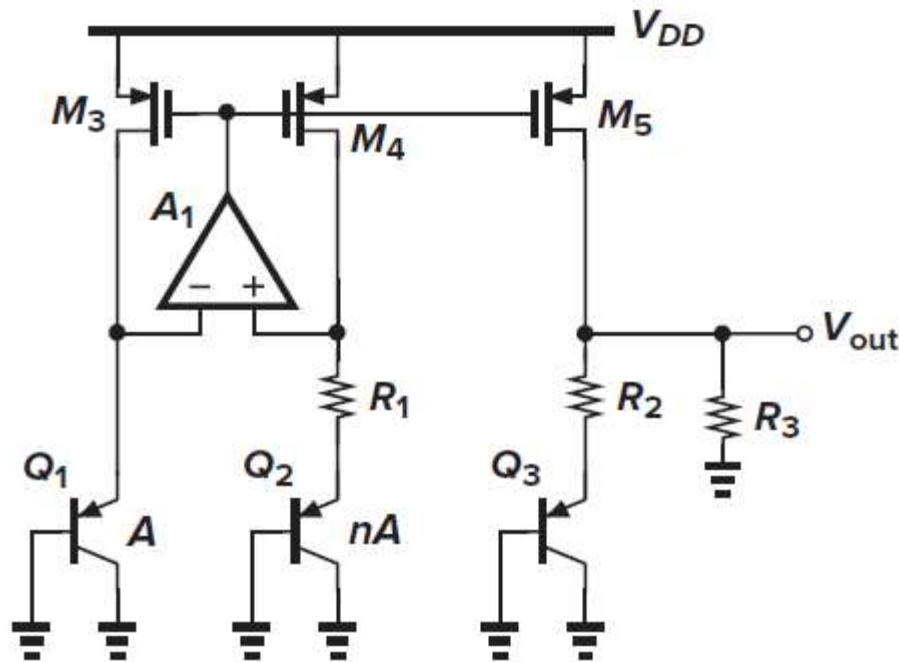
$$V_{BG} = \frac{R_4}{R_2} \left[|V_{BE1}| + \frac{R_2}{R_1} V_T \ln n - \left(1 + \frac{R_2}{R_1} \right) V_{OS} \right] \Rightarrow \text{Larger } n \text{ is used to reduce } V_{OS} \\ \text{But, ...}$$

Low-Voltage Bandgap Reference



- (1) Large transistor dimensions are chosen so as to minimize their **flicker noise and offset**
- (2) The gate-source voltage of M_a and M_b plus the headroom required by I_{SS} *must not exceed* $|V_{BE1}|$
- (3) The transistors are chosen long enough to yield a reasonable loop gain (a smaller loop gain gets more error)
- (4) It needs a start-up circuit

Low-Voltage Bandgap Reference



$$|I_{D5}| = \frac{V_{out}}{R_3} + \frac{V_{out} - |V_{BE3}|}{R_2}$$

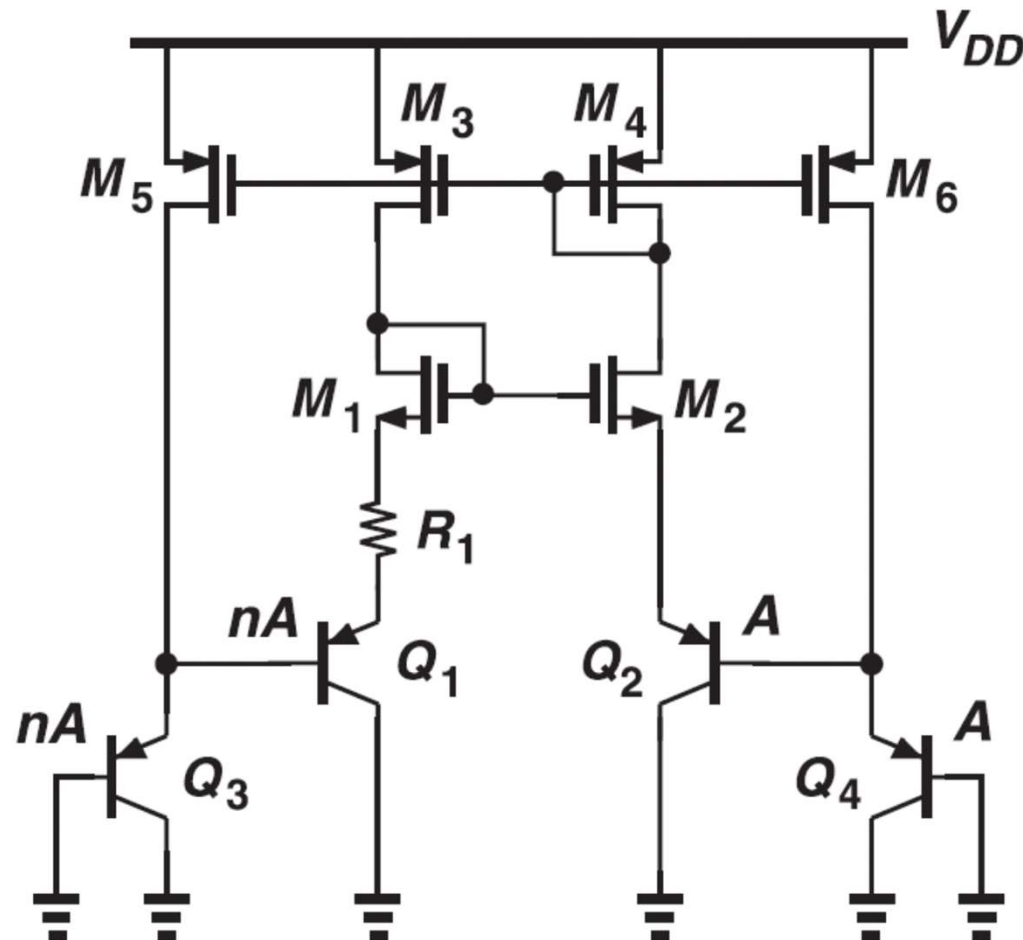
$$|I_{D5}| = V_T \ln n / R_1$$

$$V_{out} = \frac{R_3}{R_2 + R_3} \left(|V_{BE3}| + \frac{R_2}{R_1} V_T \ln n \right)$$

What do we get, if ...

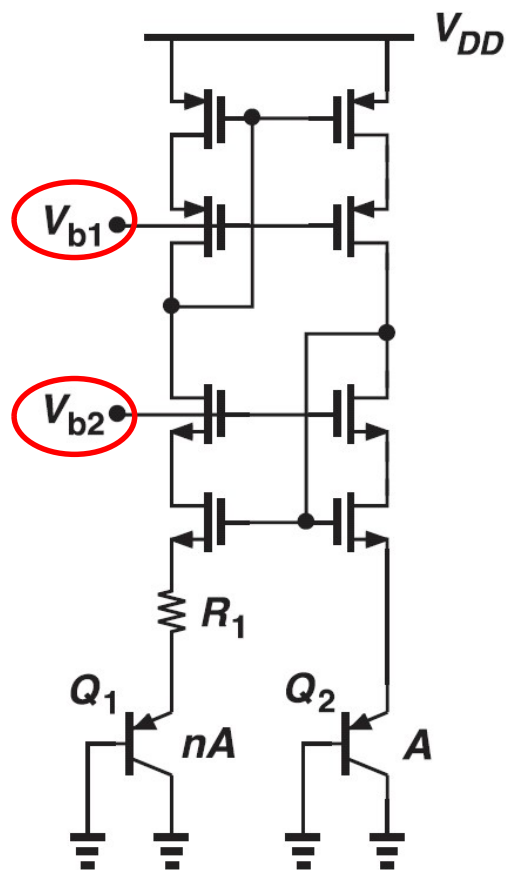
=> Using resistance ratio is better

(High-Precision) Bandgap Reference

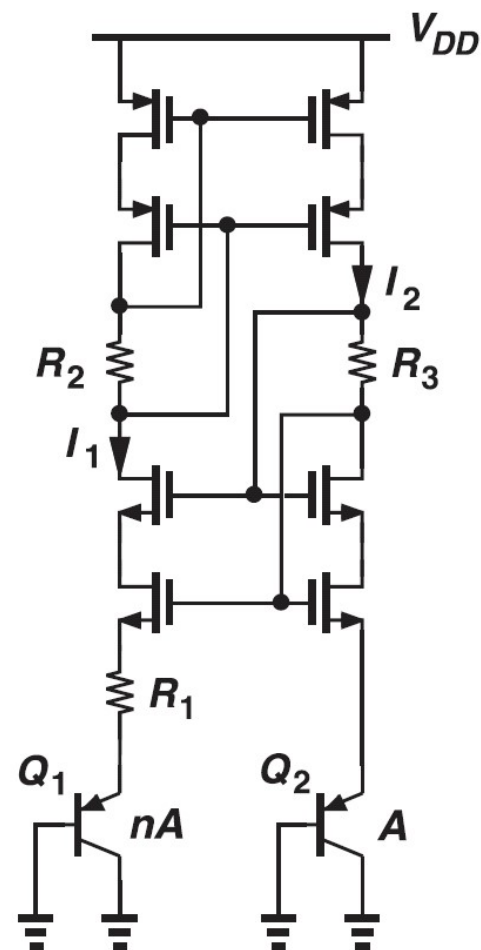


帶差電路之簡化核心部份 => How to get more precise?

High-Precision Bandgap Reference



(a)

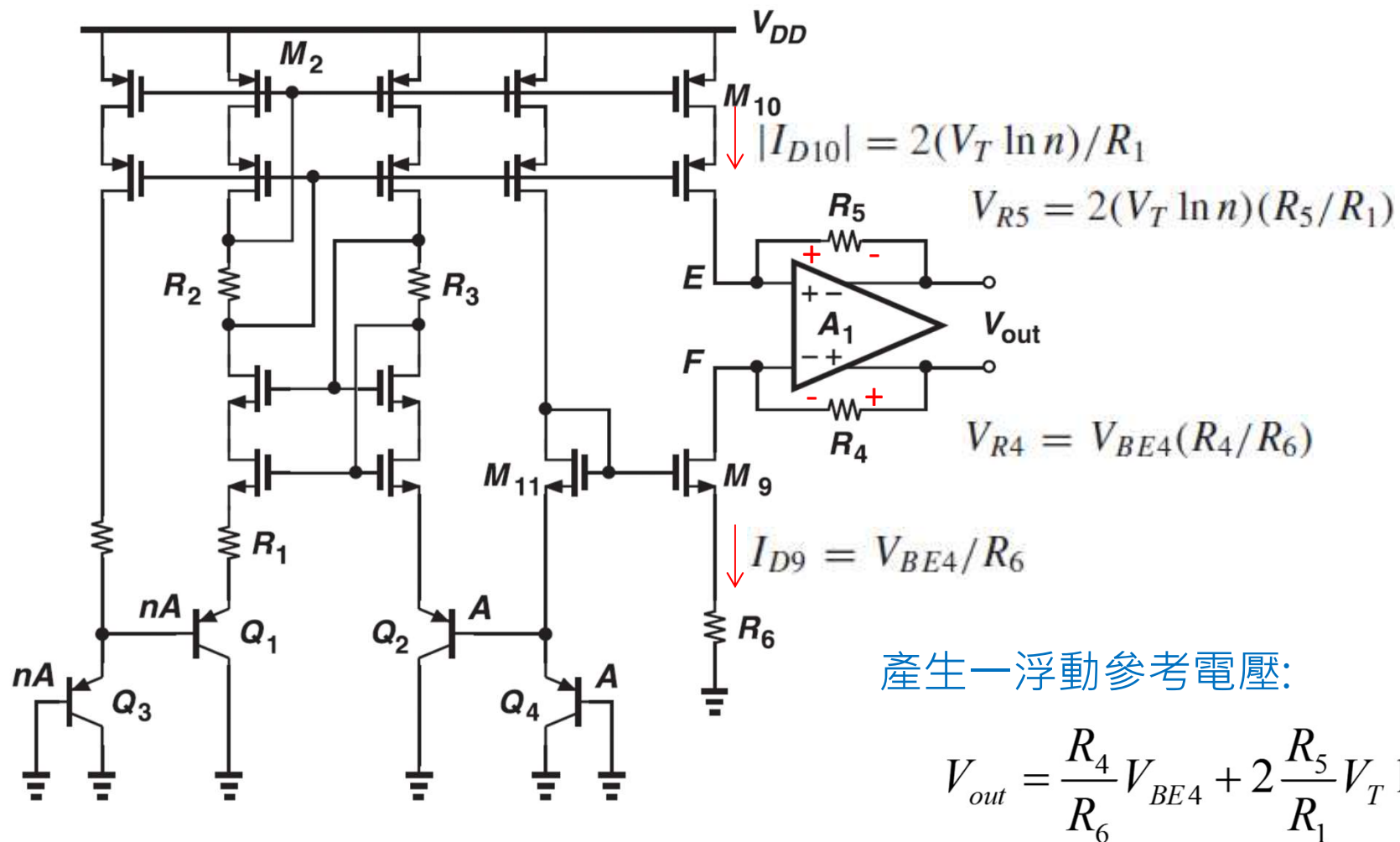


(b)

(a) 加入疊接元件以改善供應電源排斥現象；

(b) 使用自我偏壓疊接組態以消除 V_{b1} 和 V_{b2} 。

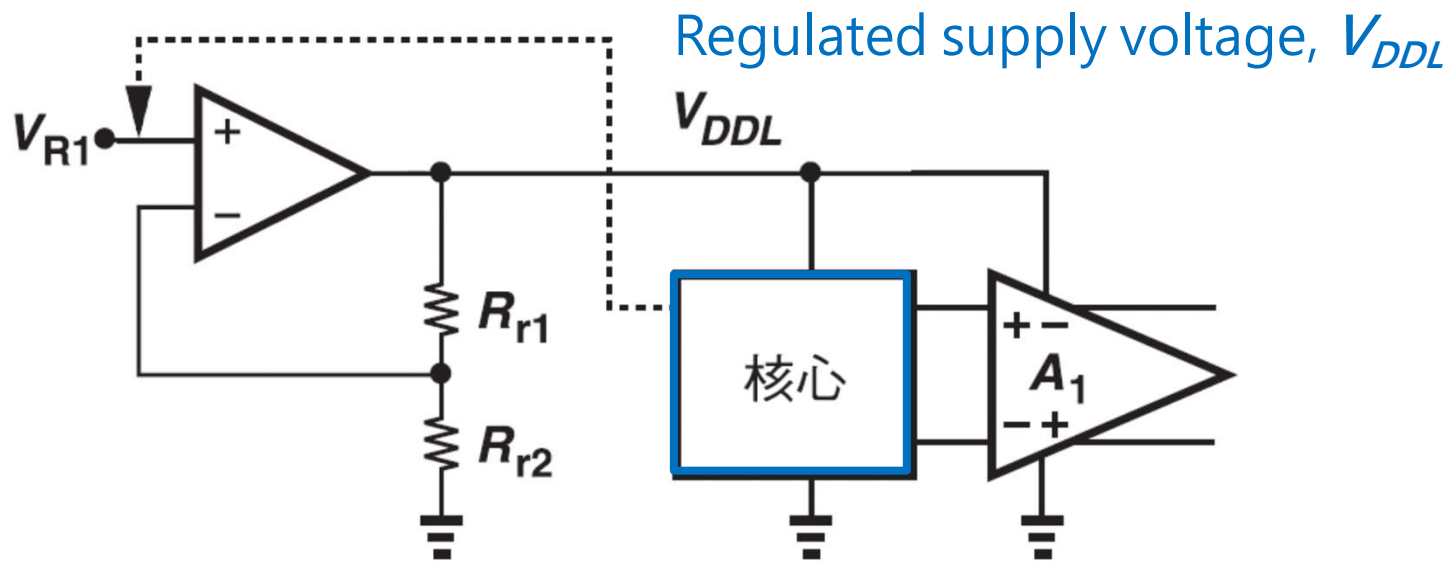
High-Precision Bandgap Reference



T. Brooks and A. L. Westwisk, "A Low-Power Differential CMOS Bandgap Reference," *ISSCC Dig. of Tech. Papers*, pp. 248–249, February 1994.

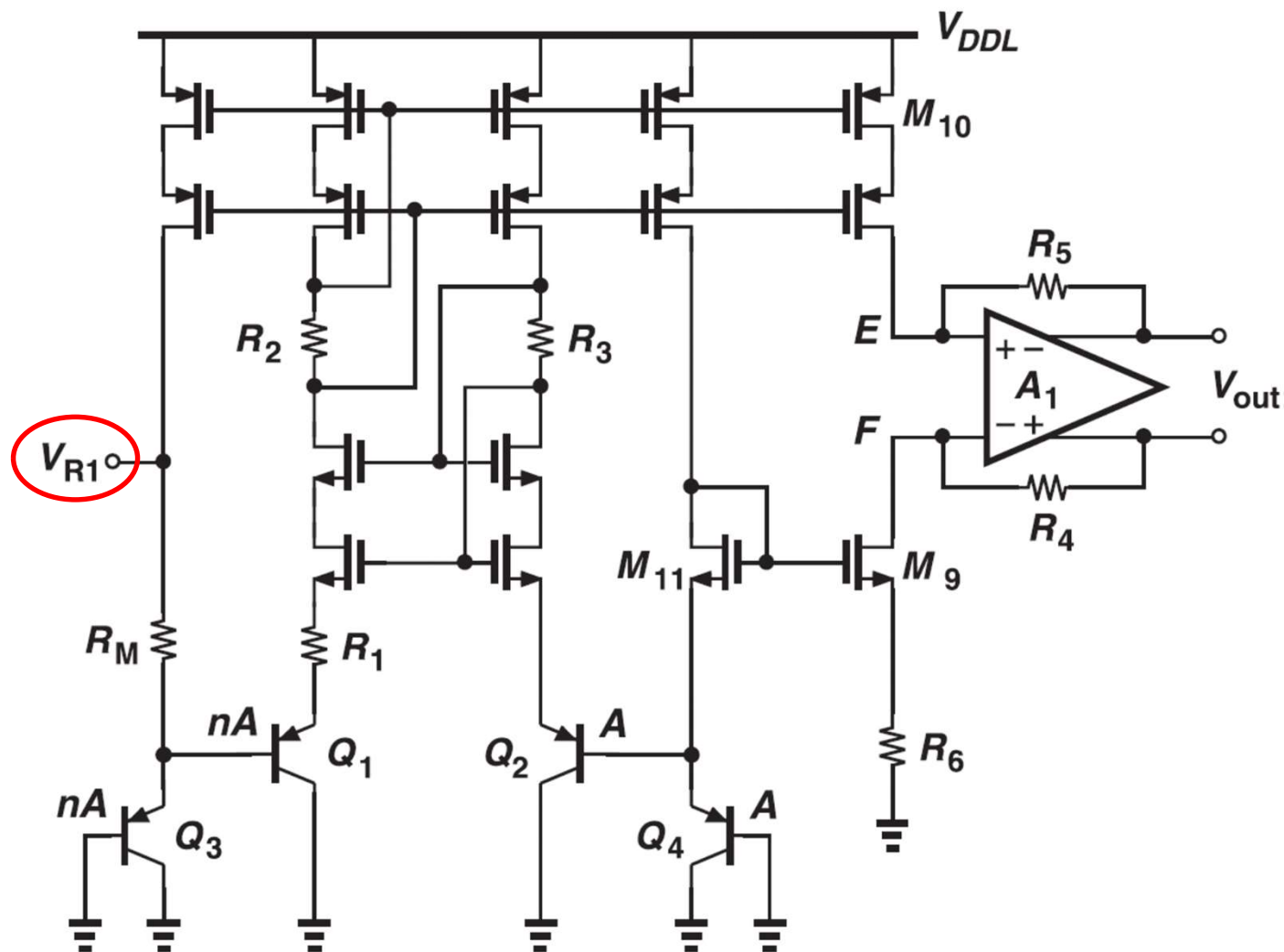
High-Precision Bandgap Reference

限制運算放大器及核心的供應電壓以改善PSRR



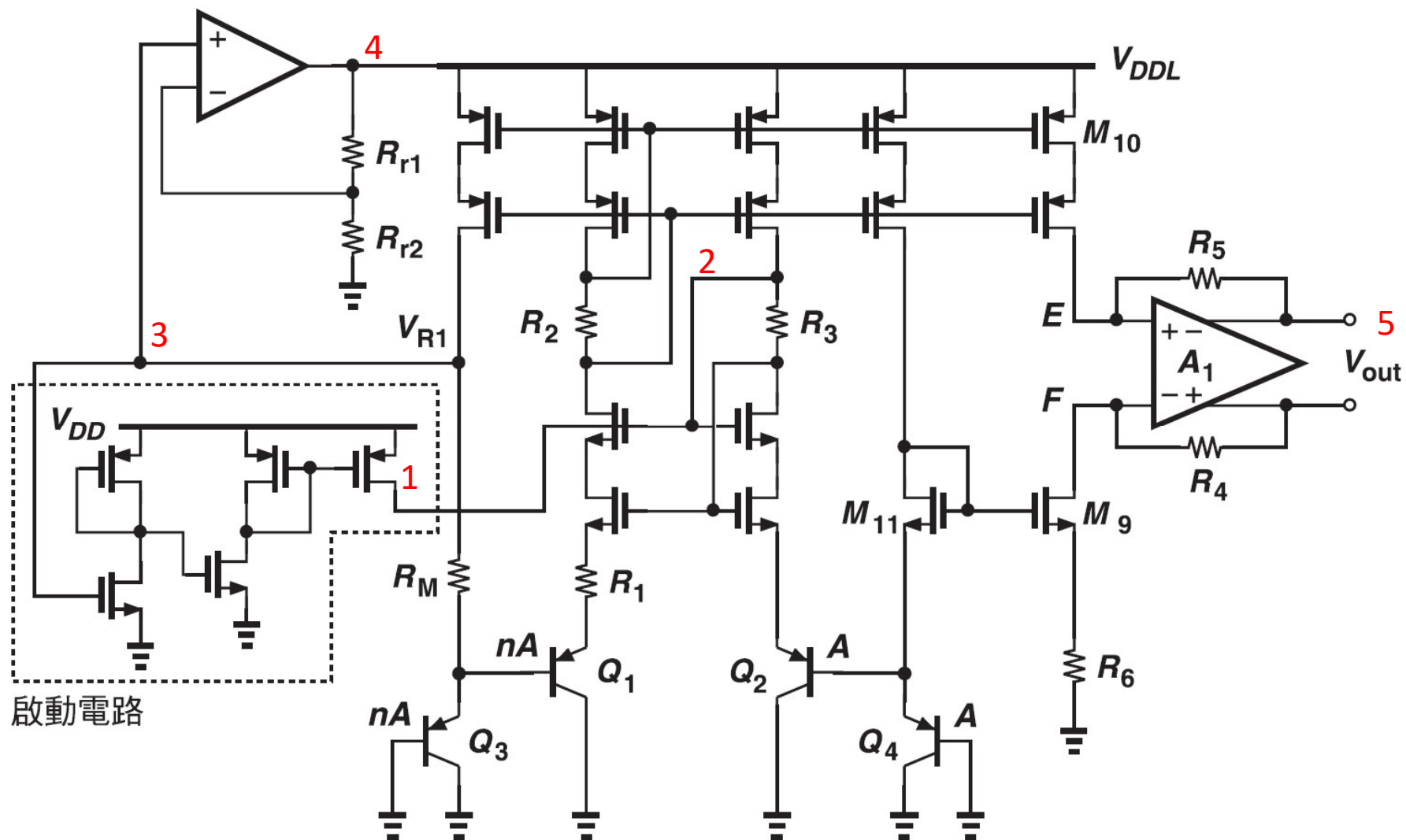
- Be careful, the startup circuit is necessary or not?

High-Precision Bandgap Reference



產生 V_{R1} 之電路

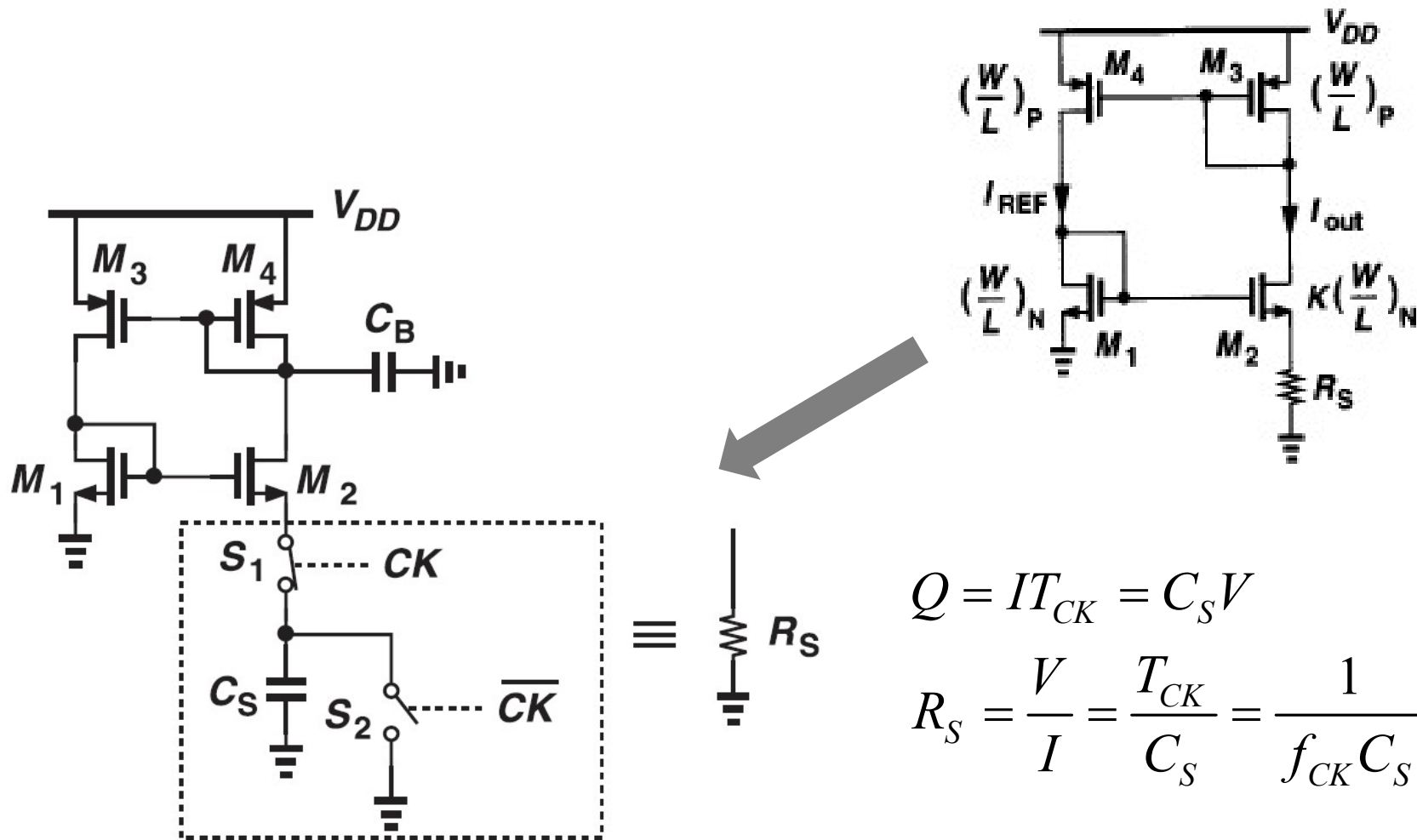
High-Precision Bandgap Reference



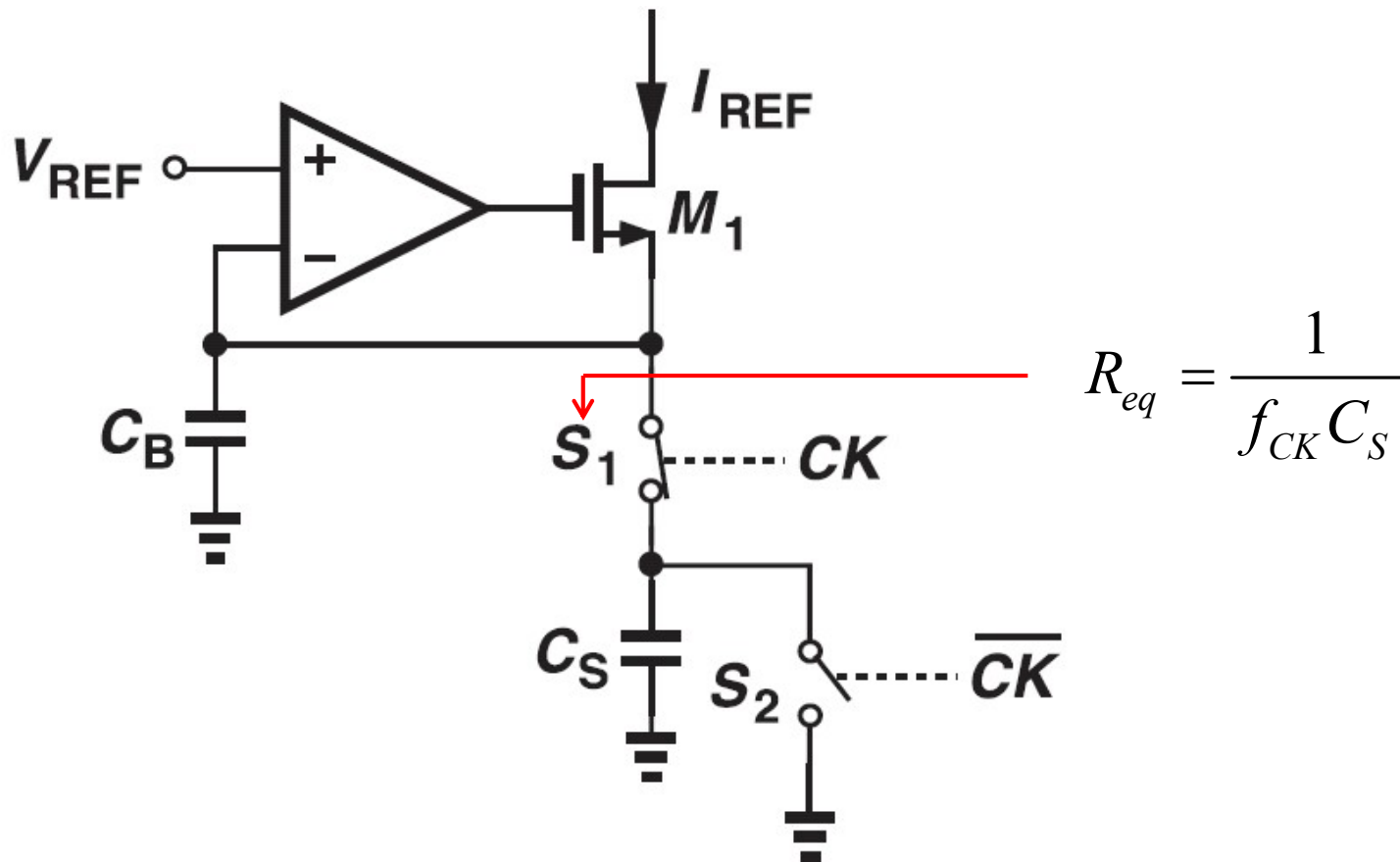
帶差電壓產生器的整體電路圖

SC Constant-Gm Biasing

利用交換電容式電阻以達到常數 G_m 偏壓



SC Constant-Gm Biasing



利用交換電容式電阻以達到電壓-電流轉換