

A PHYSICAL MODEL FOR MOSFET OUTPUT RESISTANCE

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Abstract— The output resistance (R_{out}) is one of the most important device parameters for analog applications. However, it has been difficult to model R_{out} correctly. In this paper, we present a physical and accurate output resistance model that can be applied to both long-channel and submicrometer MOSFETs. Major short channel effects and hot-carrier effect, such as channel-length modulation (CLM) [1], drain-induced-barrier-lowering (DIBL) [2] [3] [4] and substrate current induced output resistance reduction [5] [6], are all included in this model, and it is scalable with respect to different channel length L , gate oxide thickness T_{ox} and power supply V_{dd} . This model can be incorporated into existing MOSFET's model without introducing discontinuity.

I. INTRODUCTION

In analog circuit applications, the voltage gain is directly proportional to R_{out} . Existing analytical models for MOSFET R_{out} are not adequate [7], because only channel-length modulation effect is included. The empirical model [6] is more accurate, however it lacks scalability. To achieve high accuracy and scalability, R_{out} model must be analytical and include all the major physical mechanisms that affect R_{out} . The typical MOSFET I-V characteristic and output resistance are shown in Fig. 1.

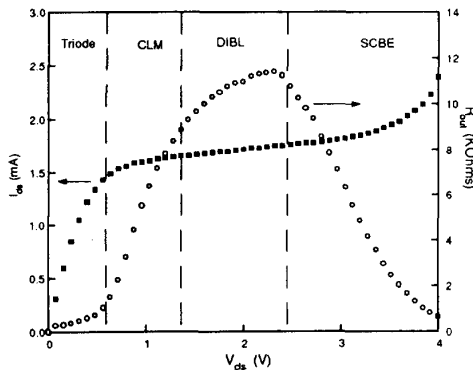


Fig. 1. Typical drain current and output resistance.
 $W/L = 10/0.43$. $T_{ox} = 75 \text{ \AA}$.

The R_{out} curve can be clearly divided into four regions with each region dominated by a mechanism. The first region is the triode region. As will be shown, the second region is the near-saturation region dominated by CLM. The third region is dominated by DIBL and the fourth is the high field region in which R_{out} is greatly reduced by the substrate current induced body effect (SCBE). Because MOSFET model in the triode region is fairly well understood, we will concentrate only on the saturation region in this paper.

II. PHYSICAL OUTPUT RESISTANCE MODEL

To smoothly and easily incorporate the various mechanisms into any drain current equation, the concept of Early voltage V_A which is widely used in BJT models, is adopted. In saturation region, V_A is introduced as follows

$$I_{ds}(V_{gs}, V_{ds}) = I_{ds}(V_{gs}, V_{dsat}) + \frac{\partial I_{ds}(V_{gs}, V_{ds})}{\partial V_{ds}} (V_{ds} - V_{dsat}) \quad (1)$$

$$\equiv I_{dsat} (1 + (V_{ds} - V_{dsat})/V_A)$$

where V_{dsat} is the saturation voltage and is given by $V_{dsat} = E_{sat} L V_{gst} / (E_{sat} L + V_{gst})$ [1], and $E_{sat} = 2v_{sat}/\mu_{eff}$, v_{sat} and μ_{eff} are saturation velocity and mobility, respectively.

$I_{dsat} = I_{ds}(V_{gs}, V_{dsat}) = v_{sat} W C_{ox} (V_{gst} - V_{dsat})$ [1] [8]. W is the width, and C_{ox} is gate oxide capacitance. V_A has three components, i.e., V_{ACLM} , V_{ADIBL} and V_{ASCBE} , corresponding to CLM, DIBL and SCBE, respectively. Each component can be evaluated separately.

$$\frac{1}{V_A} = \frac{1}{I_{dsat}} \left[\left(\frac{\partial I_{ds}}{\partial V_{ds}} \right)_{CLM} + \left(\frac{\partial I_{ds}}{\partial V_{ds}} \right)_{DIBL} + \left(\frac{\partial I_{ds}}{\partial V_{ds}} \right)_{SCBE} \right] \quad (2)$$

$$= \frac{1}{V_{ACLM}} + \frac{1}{V_{ADIBL}} + \frac{1}{V_{ASCBE}}$$

(i) Channel Length Modulation (CLM)

As $V_{ds} > V_{dsat}$, the velocity saturation region near the drain extends toward the source, which reduces the effective channel length and in turn increases the drain current. The channel length reduction ΔL satisfies $V_{ds} = V_{dsat} + I_{E_{sat}} \sin(\Delta L/l)$ [1], where $l = \sqrt{3T_{ox}X_j}$. X_j is the channel depth. V_{dsat} is a

function of $L-\Delta L$, therefore is a function of V_{ds} . V_{ACLM} can be calculated by

$$\frac{1}{V_{ACLM}} = \frac{1}{I_{dsat}} \left(\frac{\partial I_{ds}}{\partial V_{ds}} \right)_{CLM} = \frac{1}{I_{dsat}} \left(\frac{\partial I_{ds}}{\partial V_{dsat}} \frac{\partial V_{dsat}}{\partial L} \frac{\partial L}{\partial V_{ds}} \right) \quad (3)$$

We can obtain

$$V_{ACLM} = (E_{sat}L + V_{gst})(V_{ds} - V_{dsat})/E_{sat}l \quad (4)$$

where $V_{gst} = V_{gs} - V_{th}$.

(ii) Drain Induced Barrier Lowering (DIBL)

As V_{ds} is applied to the drain, the barrier height between the source and drain will be lowered [2] [4] [6], therefore the threshold voltage V_{th} is reduced and in turn the drain current increases. It has been shown [4] that threshold voltage reduction due to DIBL is given by $-\theta(L)V_{ds}$. $\theta(L)$ is the DIBL coefficient which has strong dependence on the channel length and is given by

$$\theta(L) = \exp(-L/2l_i) + 2\exp(-L/l_i) \quad (5)$$

where $l_i = \sqrt{3T_{ox}X_{dep}/\eta}$ and X_{dep} is the depletion width at the source, and X_{dep}/η is the average depletion width along the channel, where η is determined by experimental data. V_{ADIBL} can be evaluated by

$$\frac{1}{V_{ADIBL}} = \frac{1}{I_{dsat}} \left(\frac{\partial I_{ds}}{\partial V_{ds}} \right)_{DIBL} = \frac{1}{I_{dsat}} \left(\frac{\partial I_{ds}}{\partial V_{dsat}} \frac{\partial V_{dsat}}{\partial V_{th}} \frac{\partial V_{th}}{\partial V_{ds}} \right) \quad (6)$$

From the above argument, we obtain

$$V_{ADIBL} = (E_{sat}L + V_{gst})/\theta(L)(1 + 2E_{sat}L/V_{gst}) \quad (7)$$

(iii) Substrate Current Induced Body Effect (SCBE)

At even higher V_{ds} , the electrical field near the drain becomes very high ($>0.1\text{MV/cm}$). some electrons traveling through this region will acquire enough energy to cause impact ionization and result in substrate current. The substrate current will flow through the substrate, produce an ohmic drop across the substrate resistance R_{sub} , and increase the substrate potential. This substrate potential will reduce V_{th} and hence increases the drain current. On the other hand the electrons (in NMOS) created during impact ionization will go into the drain directly. Therefore we have

$$V_{ASCBE} = \sqrt{\left| \frac{A_i}{B_i} \right| \left(1 + g_m \frac{\gamma}{2\sqrt{\phi_s - V_{bi}}} R_{sub} \left(1 + \frac{B_l l}{V_{ds} - V_{dsat}} \right) \exp\left(-\frac{B_l l}{V_{ds} - V_{dsat}}\right) \right)} \quad (8)$$

where A_i and B_i are the parameters associated with the substrate current determined by experimental data [5]. g_m is the transconductance, γ is the coefficient of body effect, ϕ_s is the surface potential. V_{ASCBE} has very strong dependence on V_{ds} ,

this is because substrate current depends on V_{ds} exponentially [5]. In order to make the drain current and the first order derivative continuous at $V_{ds} = V_{dsat}$, and also take into account LDD structure effect on R_{out} , Eq. (2) is modified as

$$V_A = V_{Asat} + (1 + \alpha L_n/l)/(1/V_{ACLM} + 1/V_{ADIBL} + 1/V_{ASCBE}) \quad (9)$$

where V_{Asat} is the Early voltage at $V_{ds} = V_{dsat}$, which can be obtained from the triode region. L_n is the length of LDD region. The term $\alpha L_n/l$ take into account the LDD structure effect on R_{out} [4]. α will be extracted from experimental data. If the triode region current model in [1] [8] is used, then $V_{Asat} = E_{sat}L + V_{dsat}$. The formulation ensures that R_{out} is continuous throughout all regions, which is an important property for robust circuit simulations. Because the Early voltage approach for modeling R_{out} does not depend on the specific form of the drain current. This methodology is suitable to any MOSFET's model.

III. RESULTS AND DISCUSSION

The individual component of V_A together with the resultant V_A are shown in Fig. 2. The dominant mechanism is the one with the smallest Early voltage in each region.

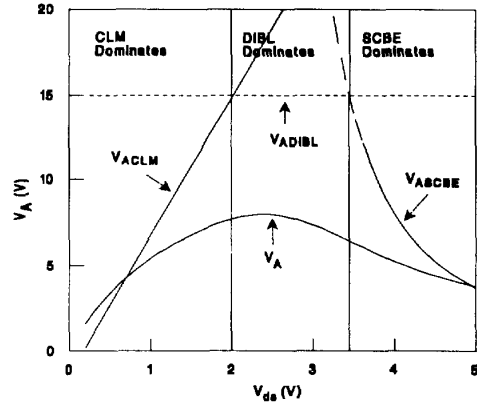


Fig. 2. Early voltage and its components versus V_{ds}

Fig. 3 shows measured R_{out} and the model at different gate voltages. The good agreement between experimental data and modeling results makes the model highly suitable for analog applications. Quantitatively predicting the scaling effects on R_{out} can also be done. Figs. 4 and 5 show R_{out} versus V_{ds} for various channel lengths and gate oxide thicknesses, respectively. The most important characteristics of R_{out} in circuit designs are the maximum R_{out} which determines the maximum available gain from the device, and the onsets of drain voltage at which R_{out} starts

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decreasing on both sides of the maximum R_{out} , which determines the dynamic swing of the drain voltage.

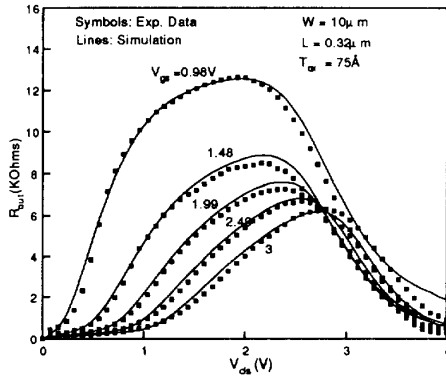


Fig. 3. NMOS R_{out} versus V_{ds} at different gate voltage

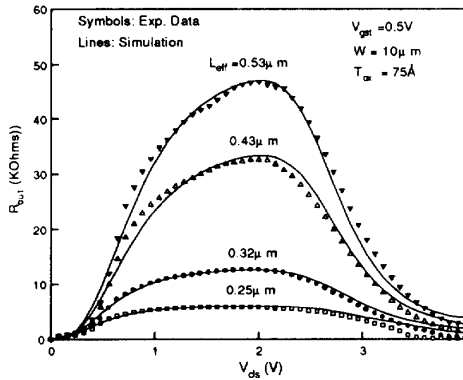


Fig. 4. R_{out} versus V_{ds} for different channel length. Gate voltage is 0.5V above threshold voltage.

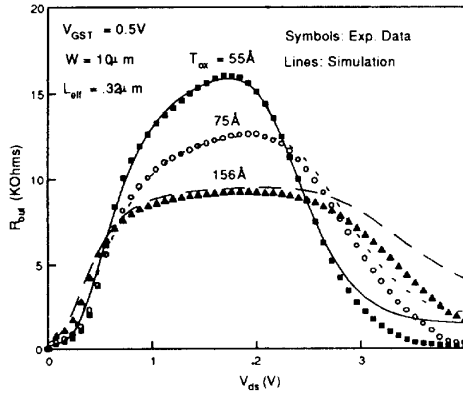


Fig. 5. R_{out} versus V_{ds} for different gate oxide thickness.

Among the three mechanisms stated above, *DIBL* has the greatest impact on the maximum R_{out} , while *SCBE*

and V_{dsat} limit the dynamic range of V_{ds} . Fig. 4 shows that maximum R_{out} is reduced as channel length decreases, this is because *CLM* and *DIBL* effects become more severe as channel length is reduced. The channel length sensitivity of maximum R_{out} is mainly due to the exponential dependence of $\theta(L)$ on channel length [4]. $\theta(L)$ and maximum R_{out} versus channel length and gate oxide thickness are shown in Fig. 6 and 7, respectively.

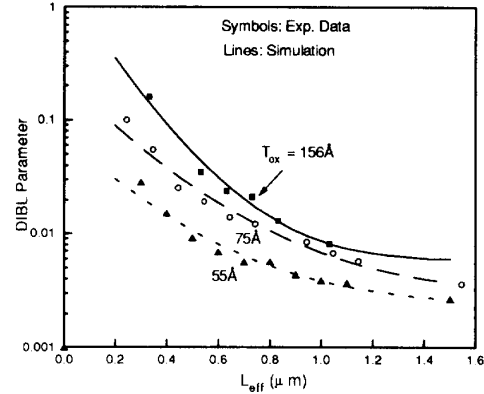


Fig. 6. *DIBL* coefficient $\theta(L)$ versus channel length. $W = 10\mu m$

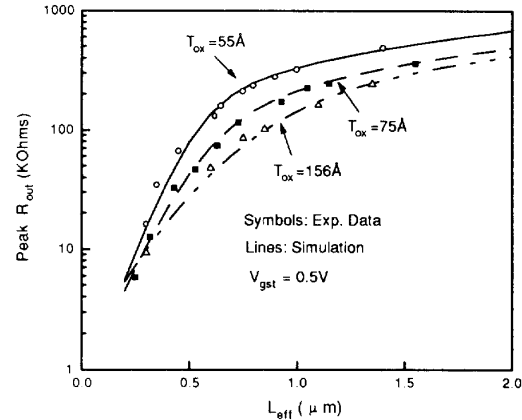


Fig. 7. Maximum R_{out} versus channel length. $W = 10\mu m$

As gate oxide thickness decreases, short channel effects are suppressed and maximum R_{out} increases, as shown in Fig. 5. However, the substrate current induced body effect (*SCBE*) is also enhanced as indicated by the faster R_{out} decreasing in the high field region for device with thinner T_{ox} . It is interesting to note that, for a given technology, the hot-carrier effects (e.g. *SCBE*) will be enhanced when the short channel effects (e.g. *CLM* & *DIBL*) are suppressed, or

vice versa, except for the introduction of LDD which improves both. This is because when the short channel effects are to be suppressed, the high field region has to be shortened. Therefore the maximum lateral electrical field is increased and hot-carrier effects is enhanced.

If we assume that the minimum R_{out} required in a design is 120 kohms, a contour of the drain voltage and channel length at which $R_{out}=120\text{ kohms}$ can be plotted as shown in Fig. 8. The regions enclosed by the contour represent the acceptable design windows. The dynamic swing for any given channel length can be clearly determined from Fig. 8. As expected, devices with thicker gate oxide will provide larger voltage swing, because of weaker SCBE, but the minimum channel length which can be used is also longer due to worse short-channel effects. With this model, families of plots similar to Fig. 8 at different V_{gst} can be generated and used by analog circuit designer in choosing the optimal device dimensions and bias conditions.

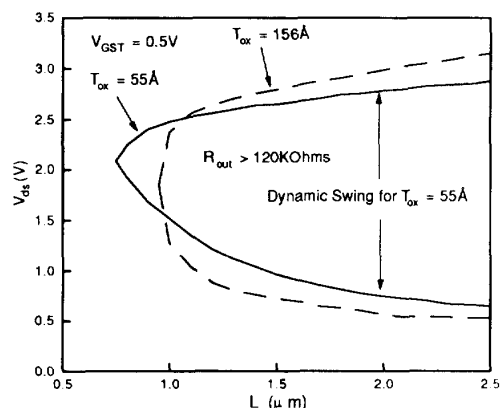


Fig. 8. Contours of R_{out} equal to 120KΩ.

Figs. 9 and 10 show that R_{out} model also has capability of modeling PMOS and LDD MOSFET.

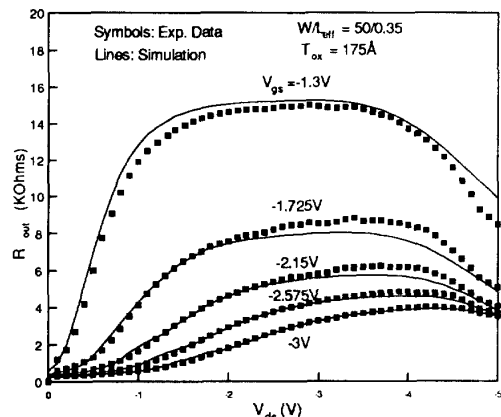


Fig. 9. Output resistance modeling for PMOS.

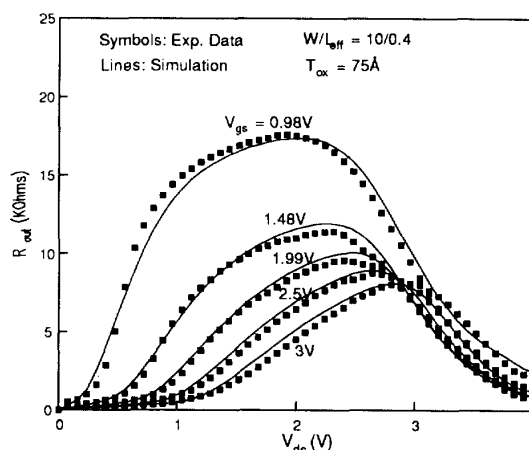


Fig. 10. Output resistance for LDD device.

IV. CONCLUSIONS

A physical-based analytical model for MOSFET output resistance is presented. Major physical mechanisms important to the output resistance are considered and analyzed. Scaling effects of channel length, gate oxide thickness and power supply on the output resistance are also investigated. This model can be incorporated into any exist MOSFET's model without introducing discontinuity.

ACKNOWLEDGMENT

This work is supported by SRC under contract 92-DC-008. J. H. Huang was also partially supported by K. C. Wong Education Foundation in Hong Kong.

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