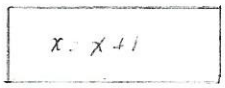
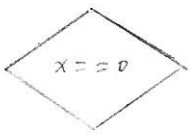
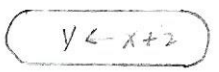
1.



state block



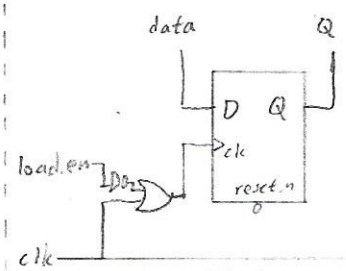
decision block



conditional output block

when load_en = 1

Q = data, every clk positive edge.

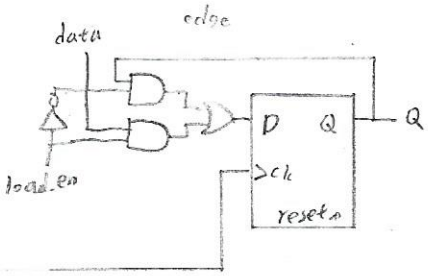


clk = load_en + clk

when load_en = 0, Q = Q

when load_en = 1

Q = data, every clk positive edge



$D = \overline{load\_en} \cdot Q + load\_en \cdot data$

when load_en = 0, Q = Q every clk positive edge

2.

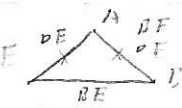
PS	NS, Z x=0	NS, Z x=1
A	B, 0	E, 0
B	F, 0	D, 0
C	D, 1	A, 0
D	C, 1	F, 0
E	B, 0	D, 0

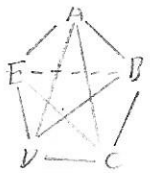
	A	B	C	D
B	BE, DE x			
C	x	x		
D	x	x	ED, AE x	
E	DE x	✓	x	x

D: Non

C: Non

B: BF





PS	NS, Z x=0	NS, Z x=1
A	E, 0	B, 1
B	G, 0	A, 1
C	B, 0	C, 1
D	C, 0	B, 1
E	D, 0	A, 1
F	F, 1	F, 1
G	E, 1	G, 1

$P_0 = (ABC \vee EFG)$

$P_1 = (AB \vee C \vee EF)(CFG)$

$= (AB)(C \vee DE)(CFG)$

$= (AB)(C)(CD)(E)(CFG)$

$P_2 = P_1$

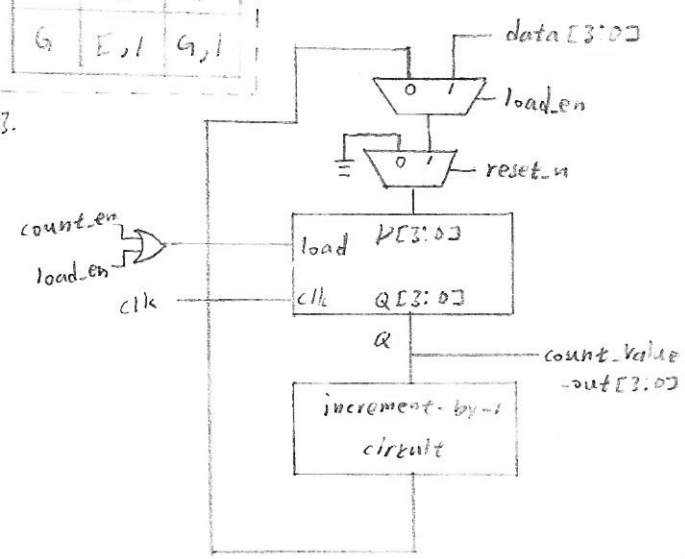
E → A, G → F

PS	NS, Z x=0	NS, Z x=1
A	F, 0	A, 1
C	A, 0	C, 1
D	C, 0	A, 1
E	D, 0	A, 1
F	E, 1	F, 1

PS	NS, Z x=0	NS, Z x=1
A → V	Z, 0	V, 1
C → W	V, 0	W, 1
V → X	W, 0	V, 1
E → Y	X, 0	V, 1
F → Z	Y, 1	Z, 1

PS	NS, Z x=0	NS, Z x=1
A	E, 0	A, 1
B	A, 0	B, 1
C	B, 0	A, 1
D	C, 0	A, 1
E	D, 1	E, 0

3.



(1) counter will increase 1 when load_en = 0 reset_n = 1, and count_en = 1 per clk positive edge. counter will load external value data every clk positive edge when loaden = 1 and reset_n = 1 counter will reset itself every clock when reset_n = 0

if count_en or load_en is 0, then the counter stop it motion

(1) use a 2 to 1 mux to choose register input value source. it is synchronously reset

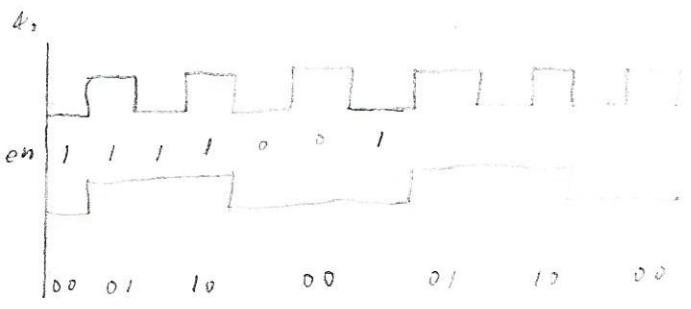
(3) also use a 2 to 1 mux circuit, it is synchronously load circuit.

測 驗 用 紙

測驗日期____年____月____日

科 目_____ 班 級_____ 評 分 | 教師簽章 | 家長簽章

4.



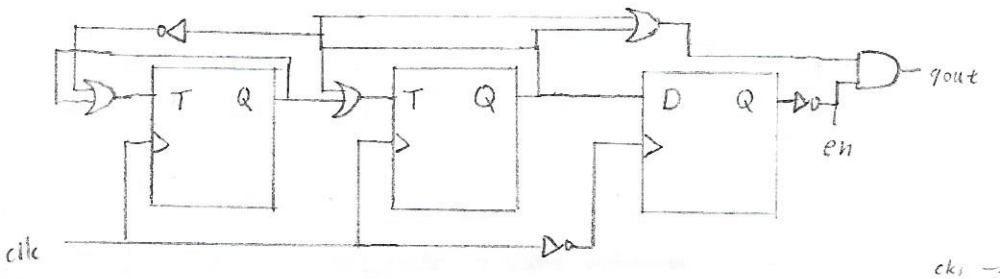
y	N	T_2	T_1
00	01	0	1
01	10	1	1
10	00	1	0
11	00	1	1

$Q_2 \backslash Q_1$	0	1
0	0	1
1	1	1

$Q_2 \backslash Q_1$	0	1
0	1	1
1	0	1

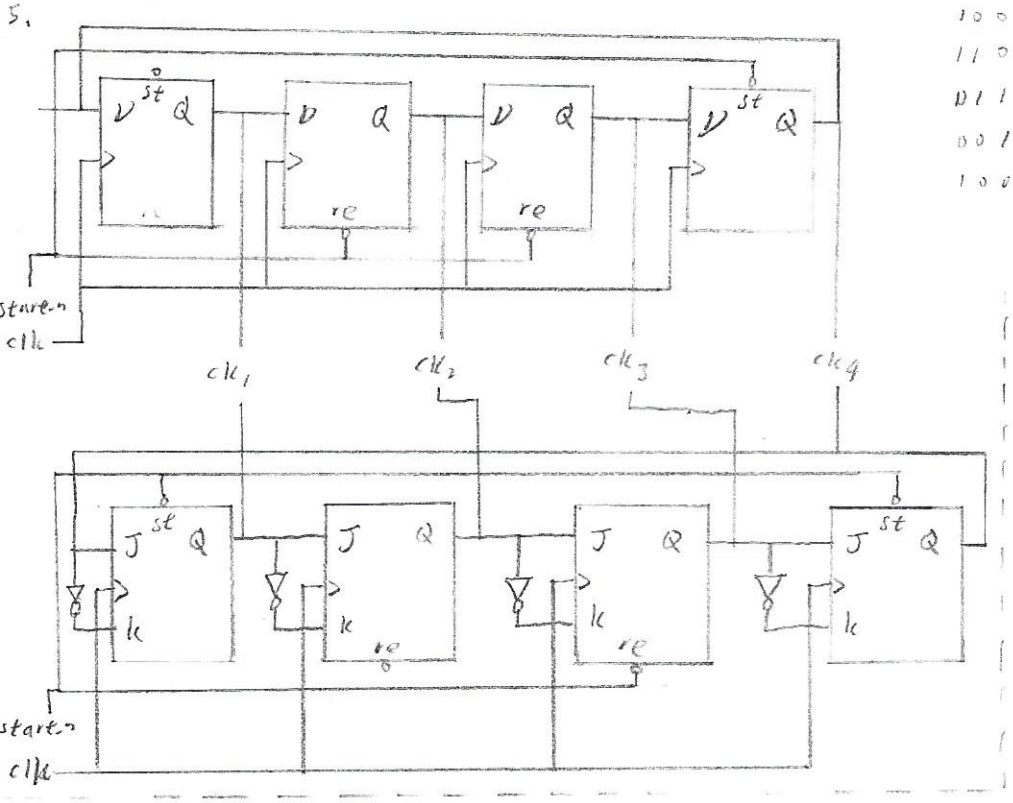
$T_2 = Q_1 + Q_2$ $T_1 = Q_1 + \overline{Q_2}$

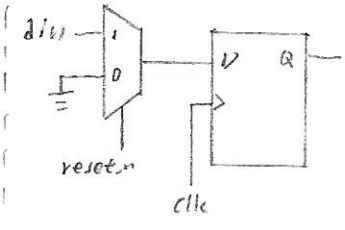
P	N	in
0	0	0
0	1	1
1	0	0



5.

ck_1	→	ck_4
1	0	0
1	1	0
0	1	1
0	0	1
1	0	0





typical synchronous reset circuit.

6.

synchronous reset along with clock, when clock at positive edge, the circuit will reset. usually use mux to implement synchronous reset.

asynchoronous reset not affected with clock, if reset is trigger, the circuit will reset immediate.