TAIWAN TECH National Taiwan University of Science and Technology

Introduction to Analog Integrated Circuit Design

Fall 2023

Current Source and Biasing

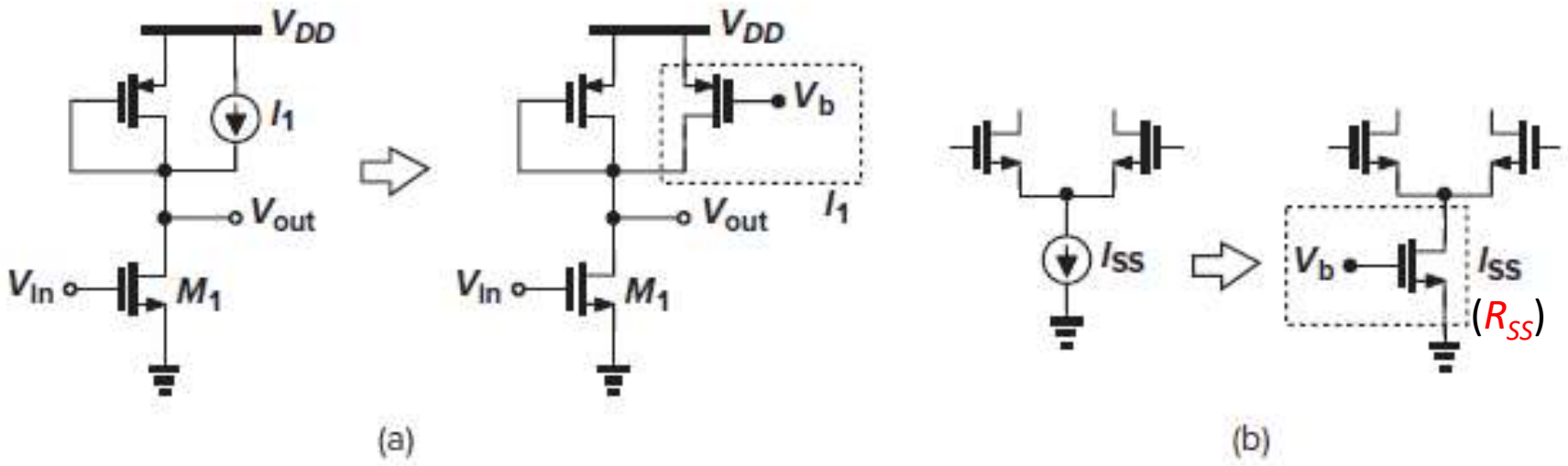
Yung-Hui Chung

MSIC Lab

DECE, NTUST

Mixed-Signal IC Laboratory NTUST

Current Sources



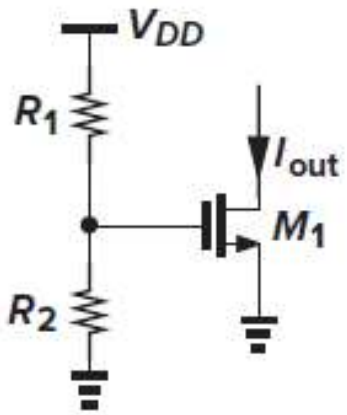
- Current sources are widely used in analog circuits
- By now, current source is not considered in the small-signal model of analog circuits
- But, we have seen its effect on **CMRR**

$$\text{CMRR} = \left| \frac{A_{DM}}{A_{CM-DM}} \right|$$

$$\text{CMRR} = \frac{g_{m1} + g_{m2} + 4g_{m1}g_{m2}R_{SS}}{2\Delta g_m}$$

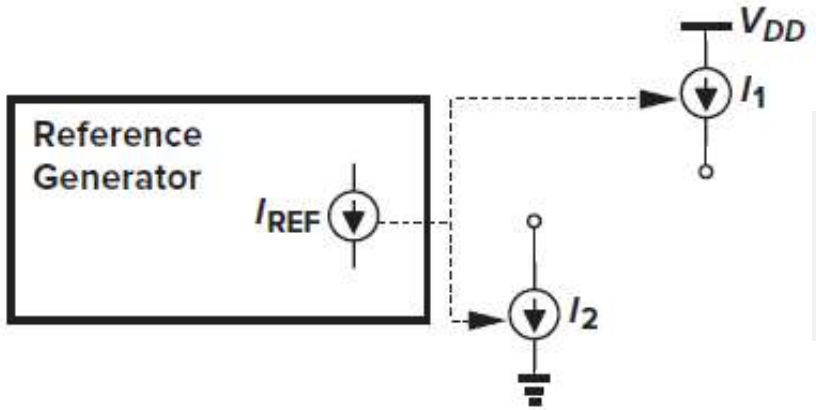
$$\approx \frac{g_m}{\Delta g_m}(1 + 2g_m R_{SS})$$

Current Sources



$$I_{out} \approx \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(\frac{R_2}{R_1+R_2}V_{DD}-V_{TH}\right)^2$$

- Some questions about the bias voltage:
  - How to get a stable current source?
  - How to define "stable"?
    - By PVT* variations, V_{TH} can have 50mV variation

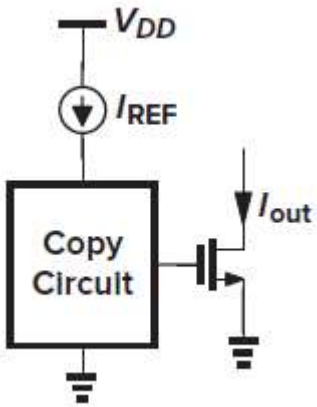


Current mirror is a good way, but ….

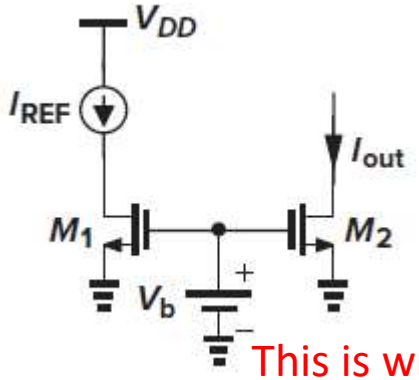
Q: Using voltage or current to transfer the current?

*PVT: **P**rocess, **V**oltage and **T**emperature

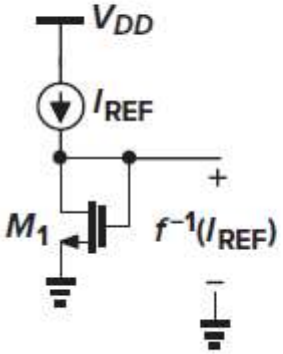
Current Sources



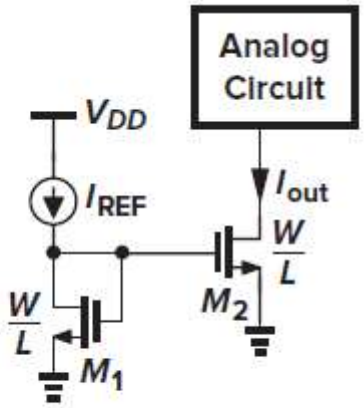
$I_{out} = I_{REF}$?



This is wrong!!



(a)



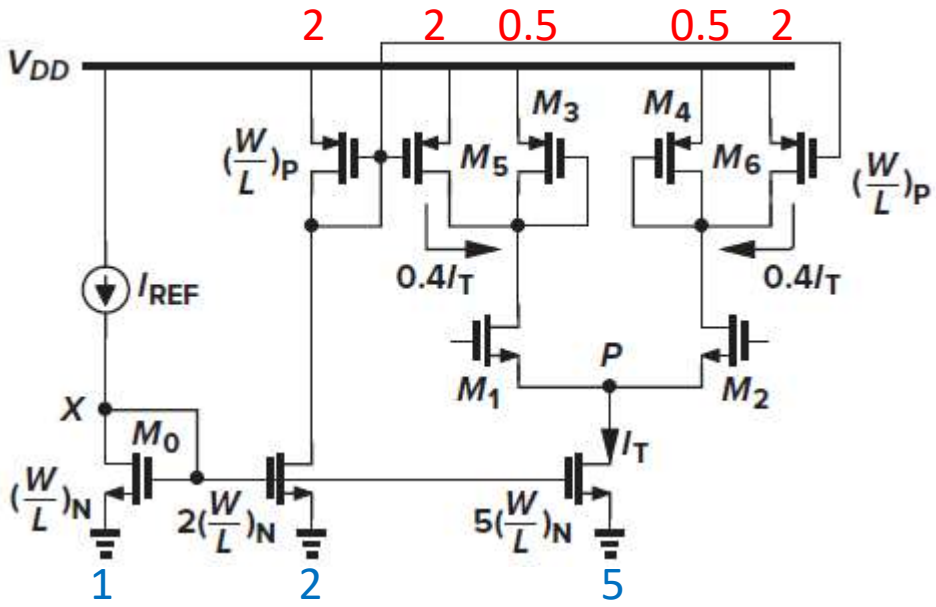
(b)

$$I_{REF} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_{GS} - V_{TH})^2$$

$$I_{out} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_2 (V_{GS} - V_{TH})^2$$

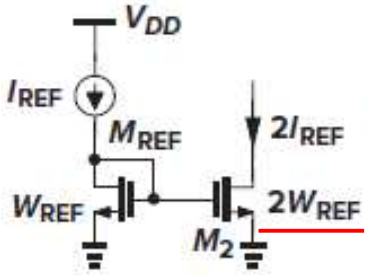
$$I_{out} = \frac{(W/L)_2}{(W/L)_1} I_{REF}$$ (but …)

Bias of a Diff-Amp

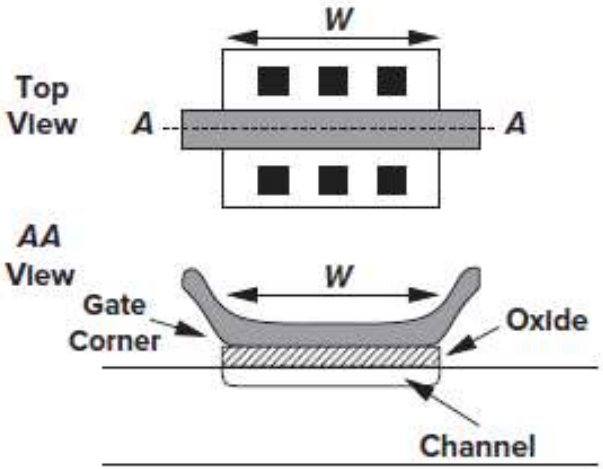


Q: How do we adjust the sizing?

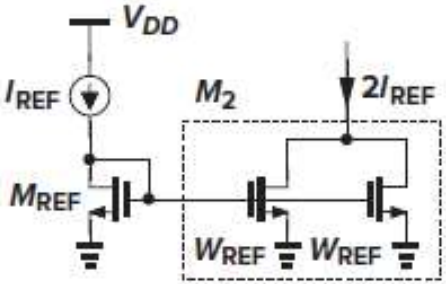
The first rule:
使用相同大小的電晶體



(a)



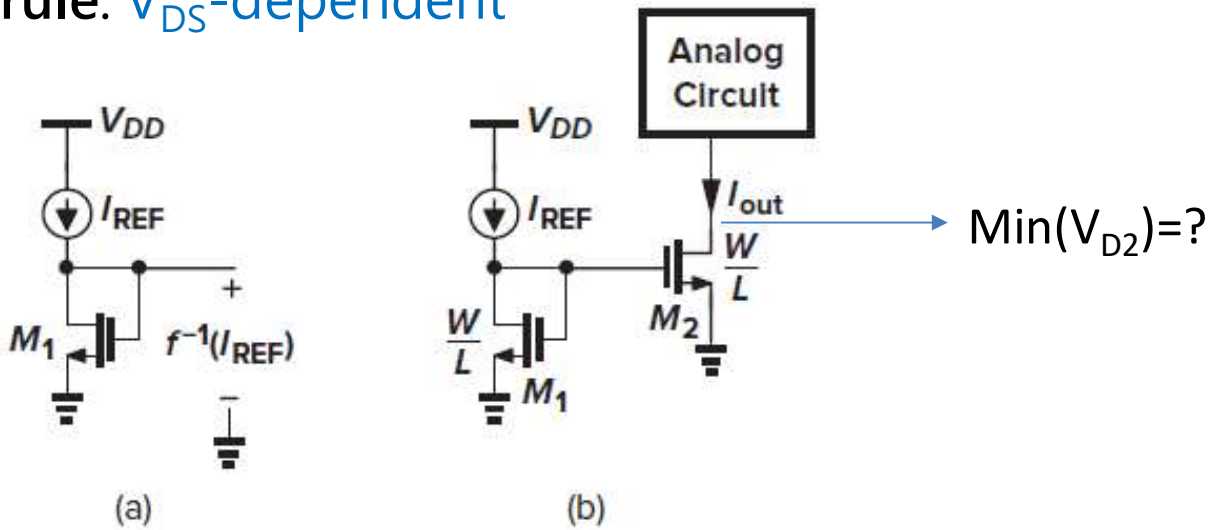
(b)



(c)

V_{DS} Dependence

The second rule: V_{DS}-dependent



$$I_{D1} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_{GS} - V_{TH})^2(1 + \lambda V_{DS1})$$

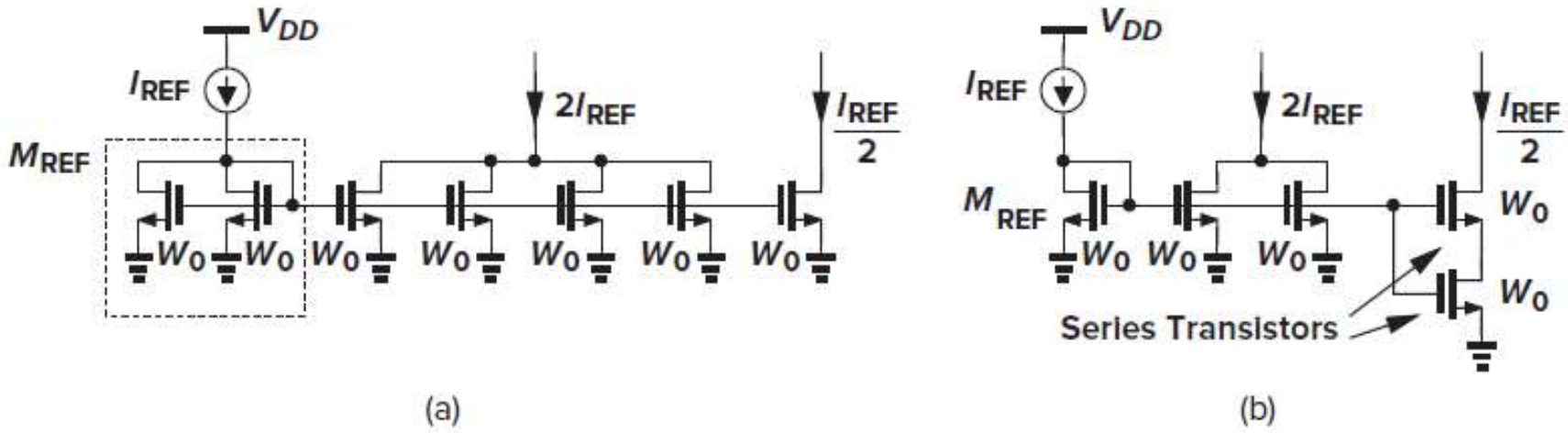
$$I_{D2} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_2 (V_{GS} - V_{TH})^2(1 + \lambda V_{DS2})$$

$$\frac{I_{D2}}{I_{D1}} = \frac{(W/L)_2}{(W/L)_1} \cdot \frac{1 + \lambda V_{DS2}}{1 + \lambda V_{DS1}}$$

(V_{DS}-dependent)

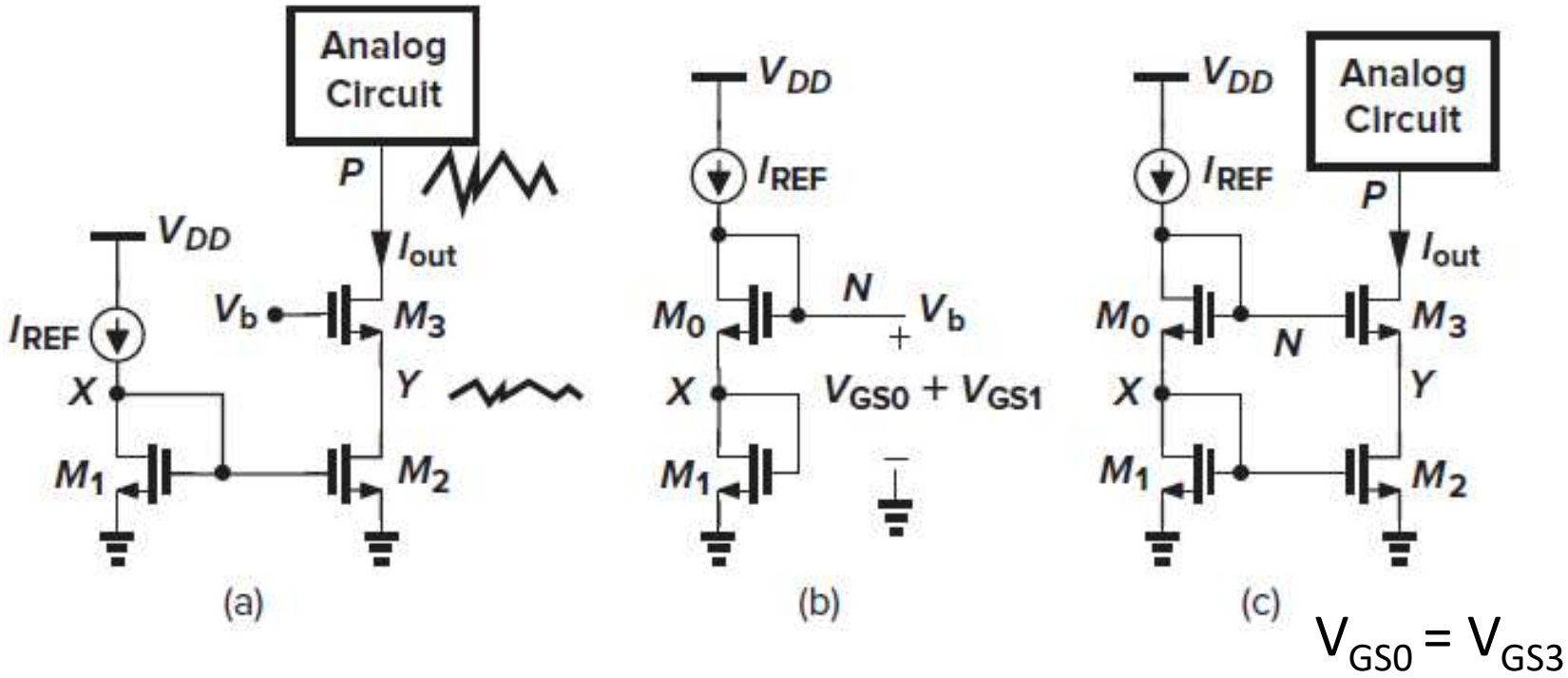
Comment: To avoid long current mirror chain (1=>2=>4=>8)!!

Current Multiplication and Division



- Transistors with same dimension (積木的概念)
- Similar V_{DS} (相同的操作環境)
- Mismatch issue (chapter 14) ⇒1112_AIC2
- Layout issue (chapter 19) ⇒1112_IC Layout Practice
  - Same current direction
  - Common-centroid layout

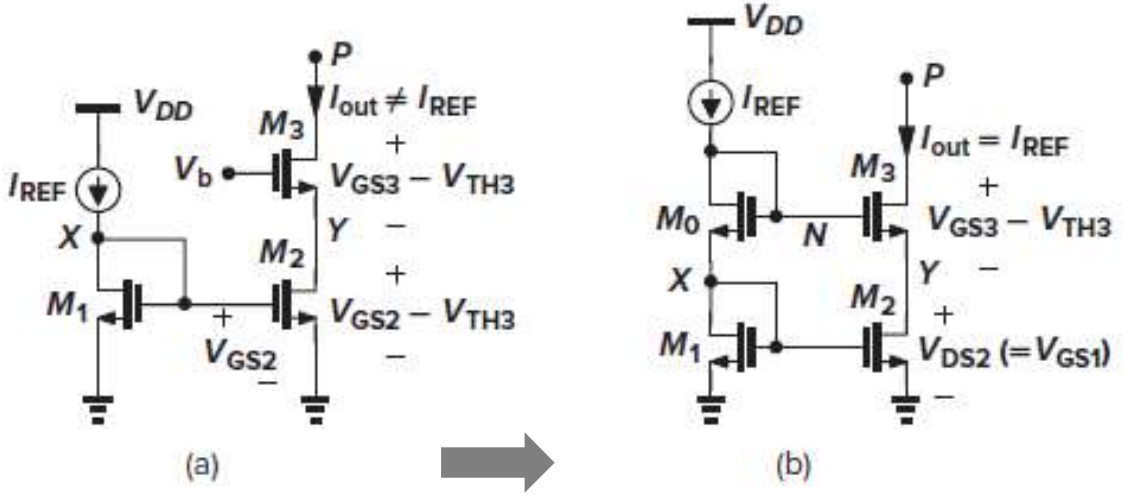
Precision of Current Mirrors



$V_{GS0} = V_{GS3}$

- How to get a precise current multiplication?
  - Design Concept (channel length, V_{GS} and V_{DS})
  - Layout Concept (Physical errors by layout)
  - Manufacture Concept (design for manufacture, DFM)

Precision of Current Mirrors

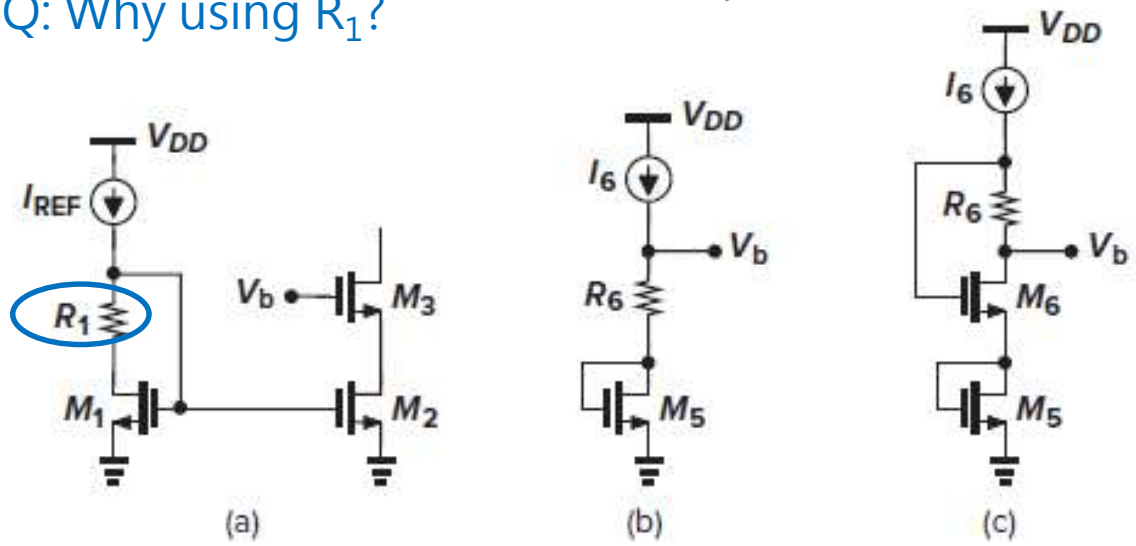


V_Y=?

Drawbacks?

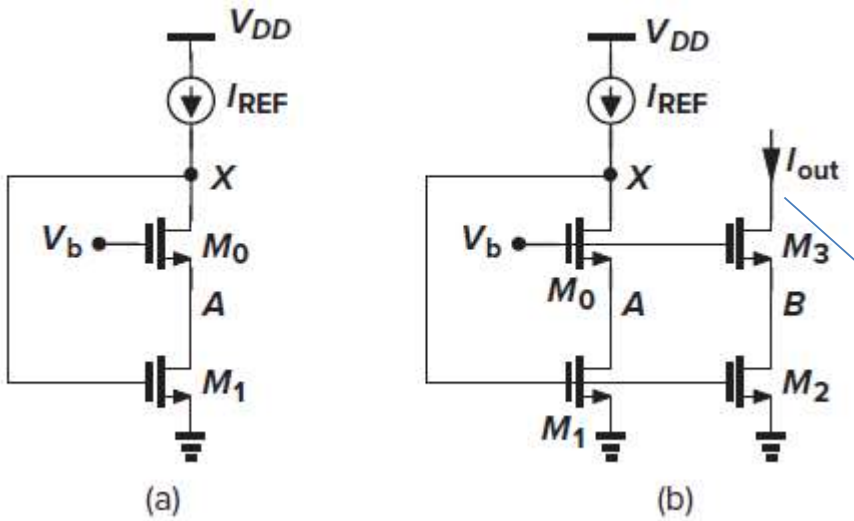
Try to improve!!

Q: Why using R_1?



V_b is a bias voltage which is needed to bias M3 properly!!

Precision of Current Mirrors

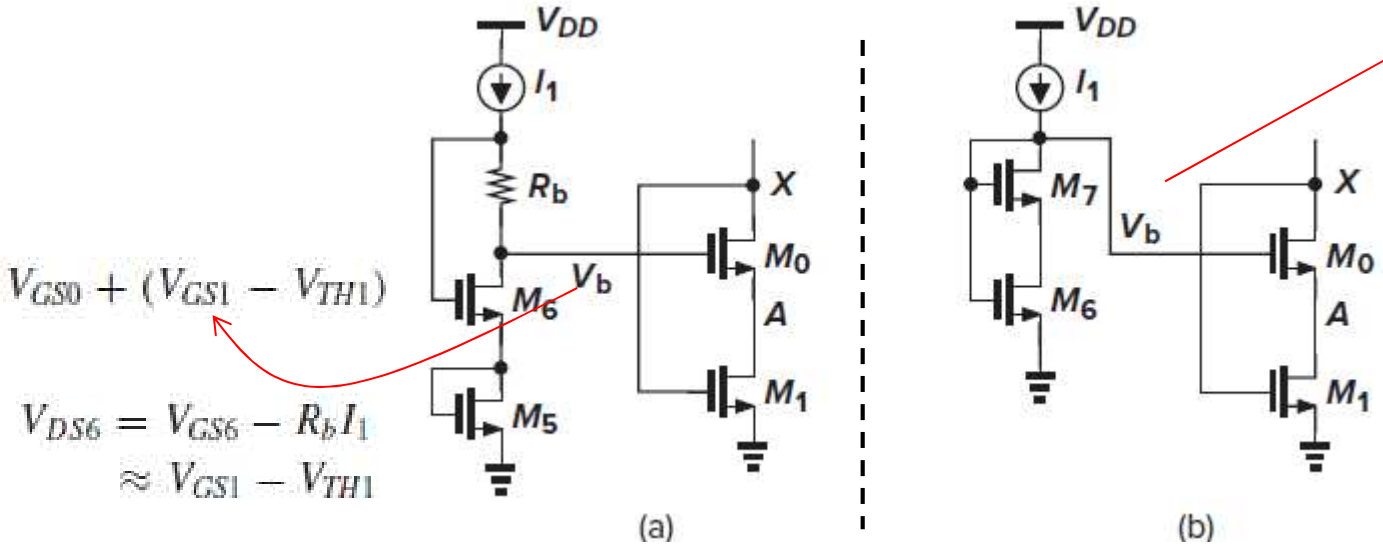


Low voltage self-bias

$$V_{GS0} + (V_{GS1} - V_{TH1}) \le V_b \le V_{GS1} + V_{TH0}$$

$$V_{GS0} - V_{TH0} < V_{TH1}$$

If $V_b = V_{TH3}+V_{ov3}+V_{ov2}$,
V_{d3} can be as low as "$V_{ov3}+V_{ov2}$"



$$V_{GS0} + (V_{GS1} - V_{TH1})$$

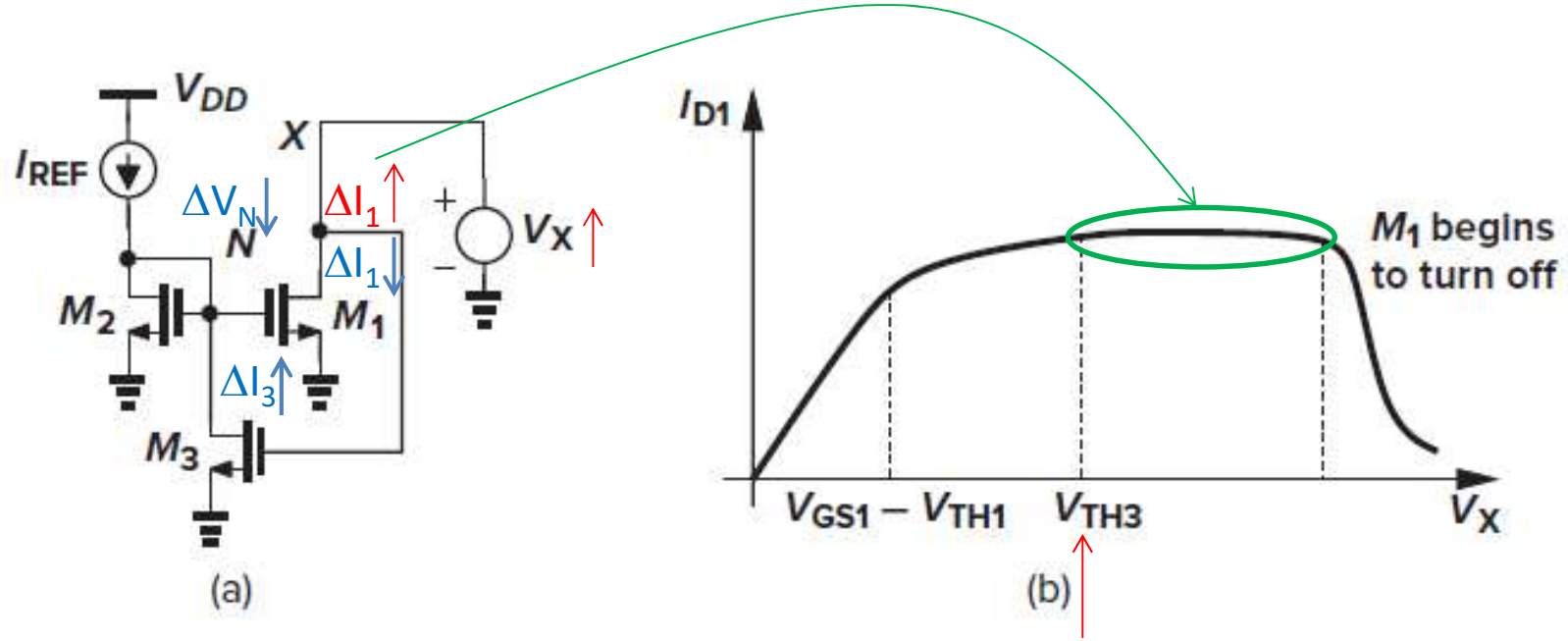
$$V_{DS6} = V_{GS6} - R_b I_1 \approx V_{GS1} - V_{TH1}$$

A simple way

$V_b = V_{GS5} + V_{GS1} - V_{TH1}$ ⇒ $V_{GS5} = V_{GS0}$ But, are you sure?

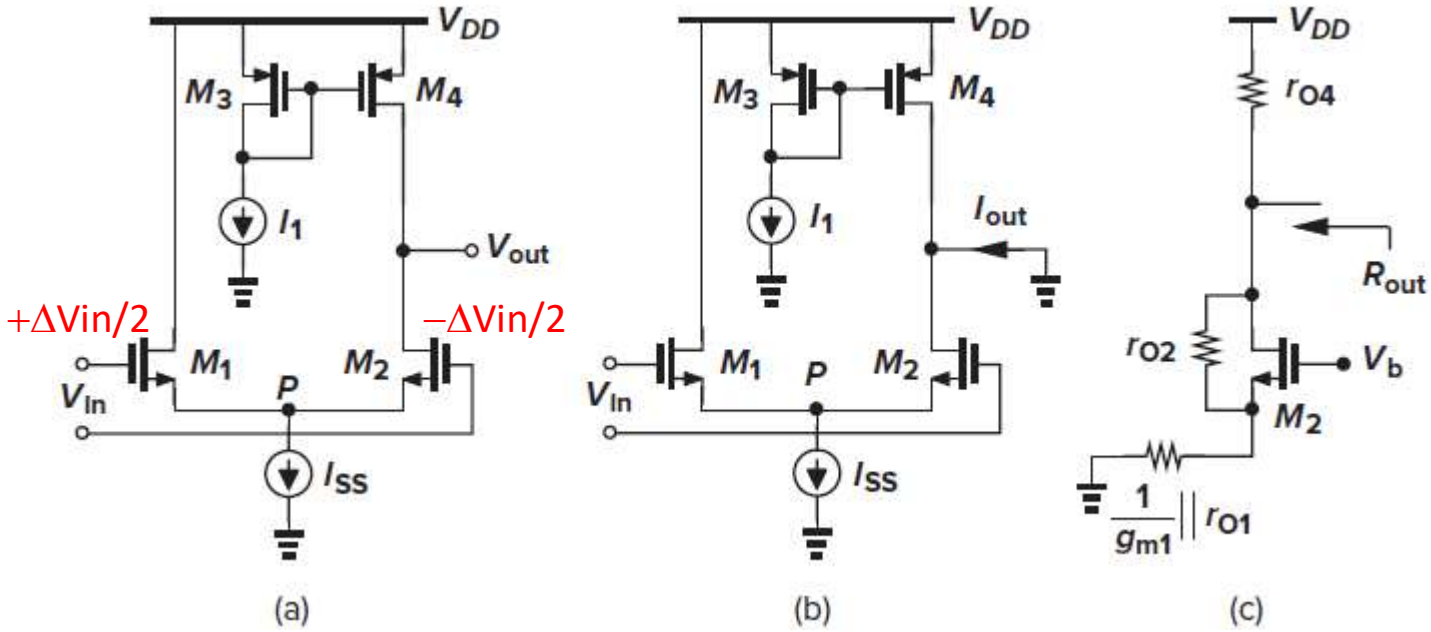
Precision of Current Mirrors

Another way: using a feedback loop



- If cascode current source is not allowed, the feedback loop also helps to improve the output resistance
- But, Vx is not low enough. Why?

Operational Transductance Amplifier



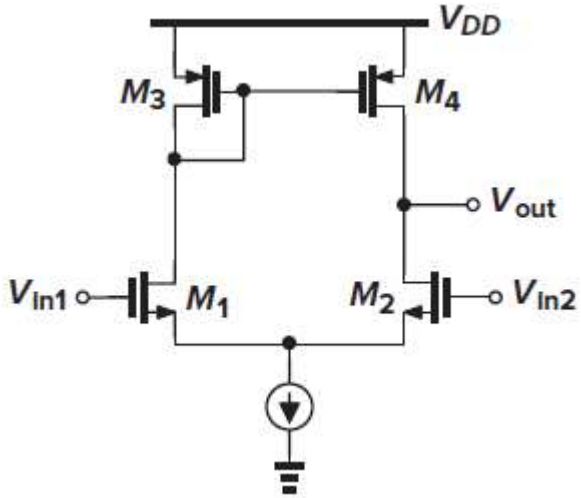
$$|A_v| = \frac{g_{m1}}{2}[(2r_{O2})\|r_{O4}]$$

Q: Why "2"?

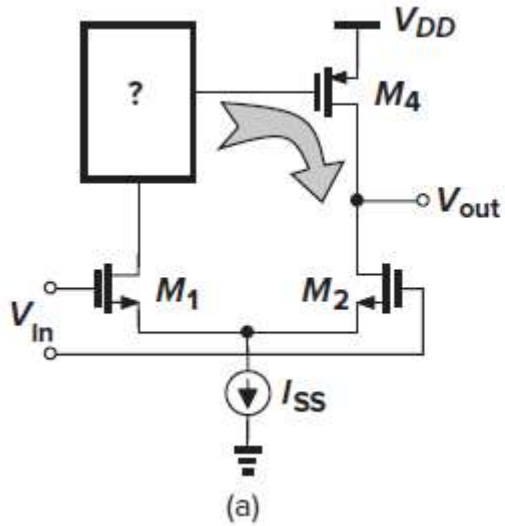
if $r_{O4} \to \infty$, then $A_v \to -g_{m1}r_{O2}$.

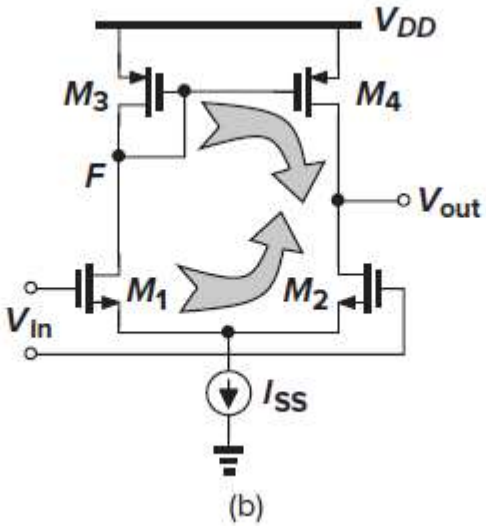
(There is another way to conduct this. In textbook, page 147)

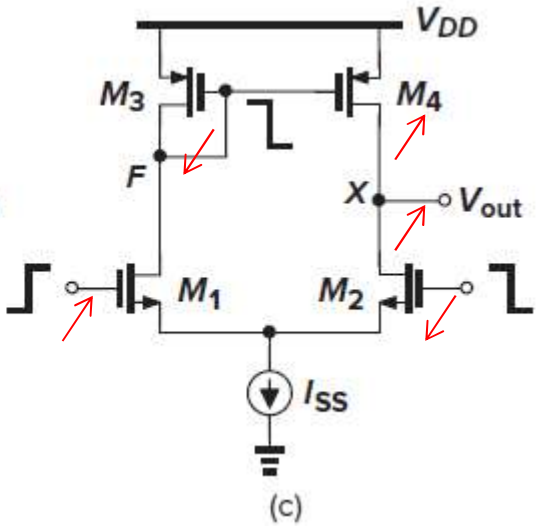
OTA



The five-transistor OTA is also called a differential pair with active load

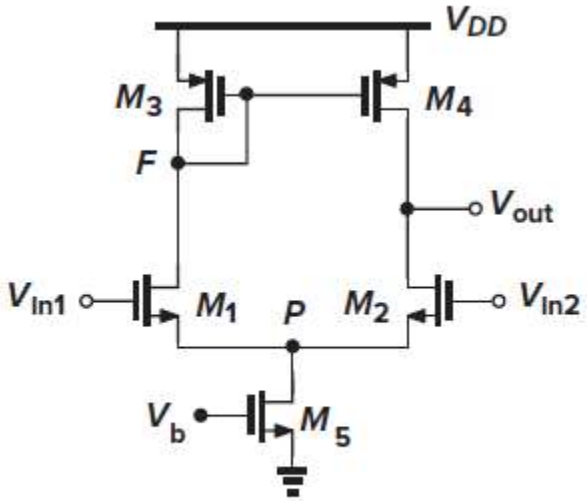




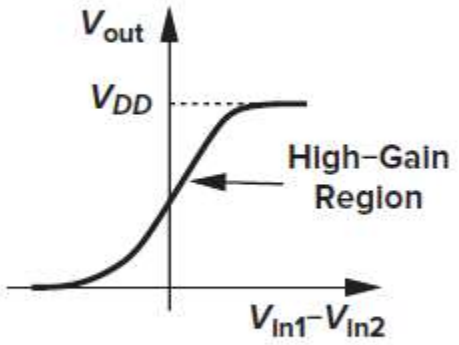


Analysis of OTA: DC gain

Large-signal analysis

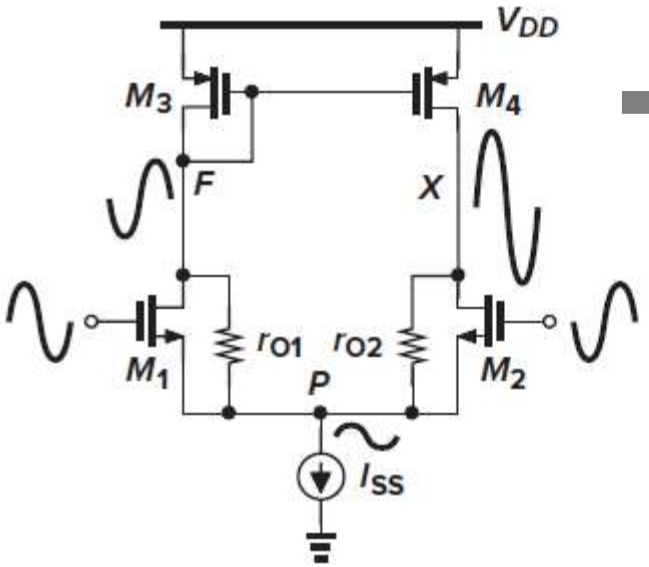


(a)



(b)

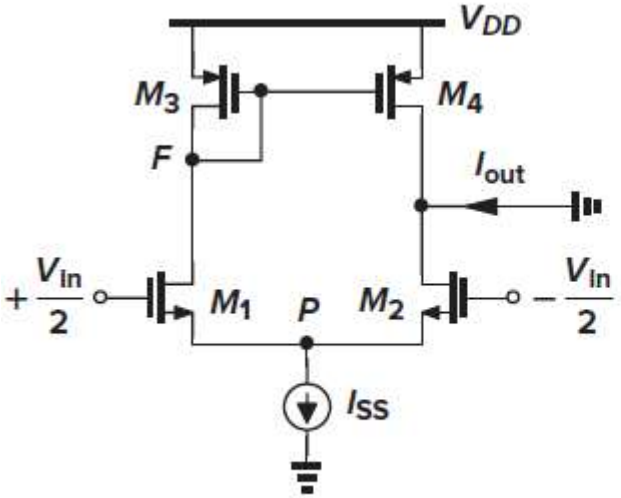
Small-signal analysis



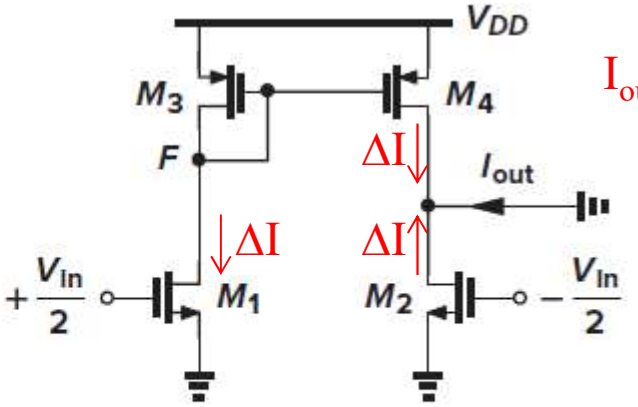
➡ Is there something you find?

Figure 5.31 Asymmetric swings in a differential pair with active current mirror.

Analysis of OTA: DC gain



(a)

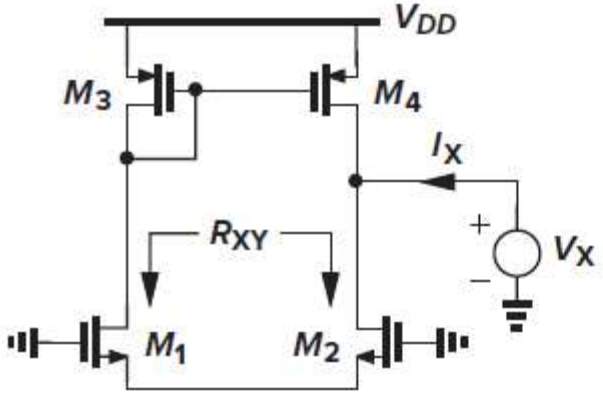


$I_{out} = -2\Delta I$

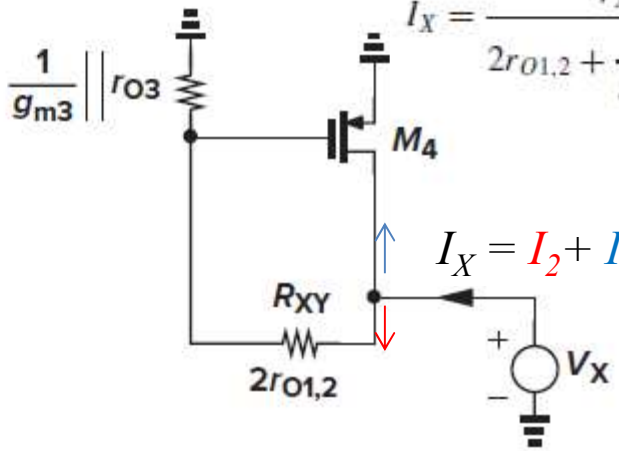
$= -g_m * \Delta V_{in}$

$\Delta I = g_m * \Delta V_{in}/2$

(b)



(a)

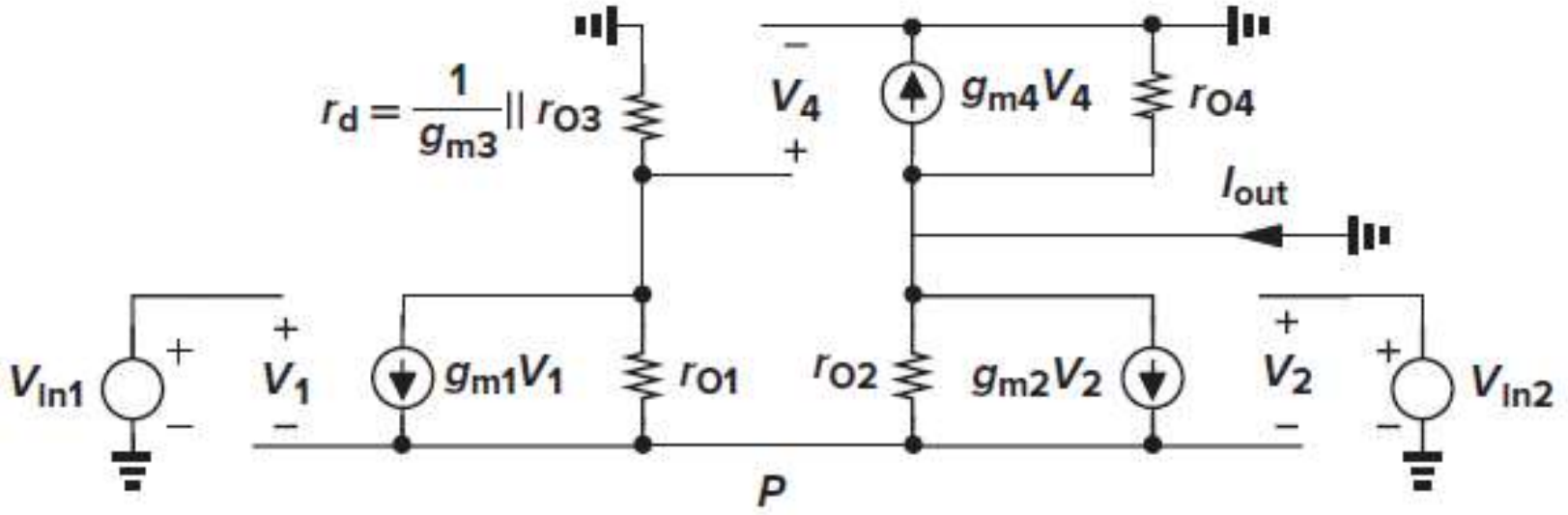


$$I_X = \frac{V_X}{2r_{O1,2} + \frac{1}{g_{m3}} \| r_{O3}} \left[1 + \left(\frac{1}{g_{m3}} \| r_{O3}\right) g_{m4}\right] + \frac{V_X}{r_{O4}}$$

$$R_{out} \approx r_{O2} \| r_{O4}$$

(b)

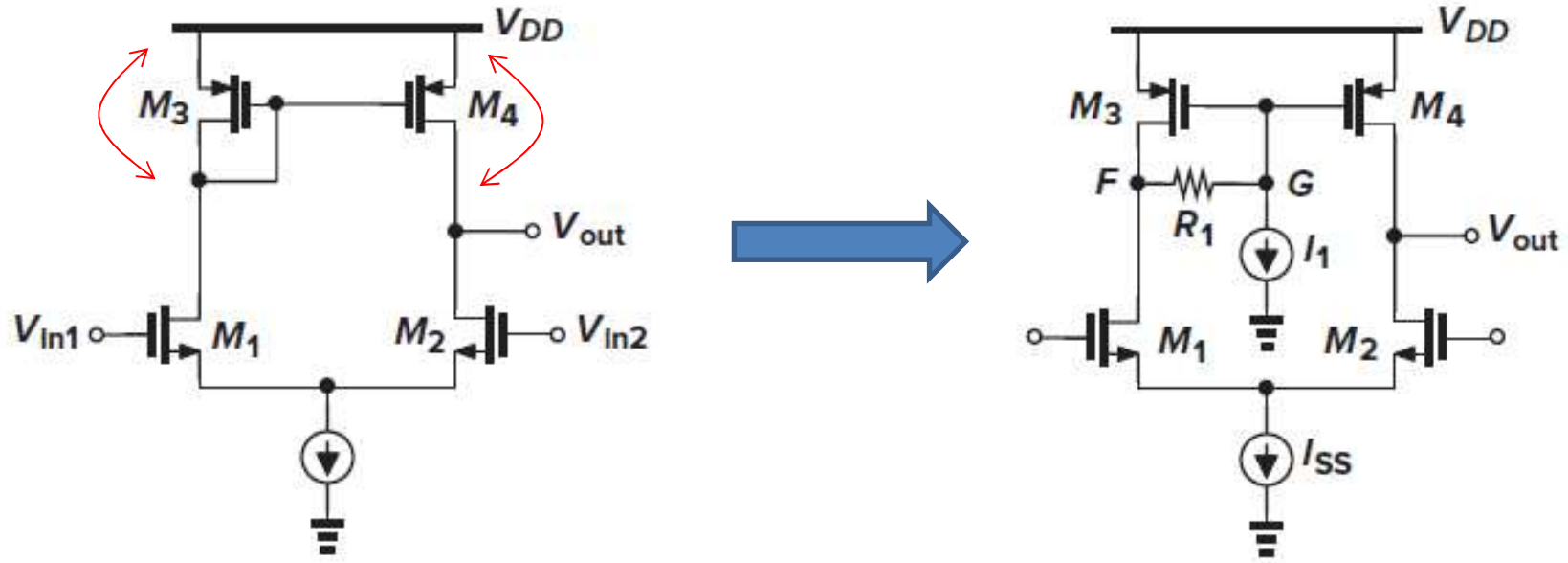
Exact Analysis: DC gain



(in the textbook, page 154)

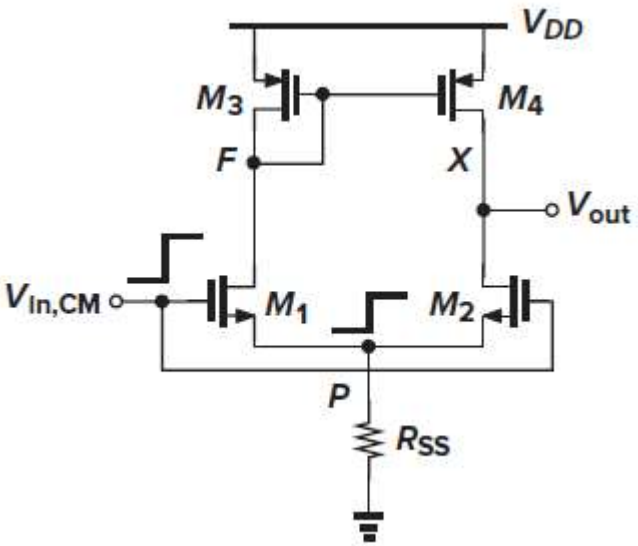
$$|A_v| = g_{m1}(r_{O1} \| r_{O4}) \frac{2g_{m4}r_{O4} + 1}{2(g_{m4}r_{O4} + 1)}$$

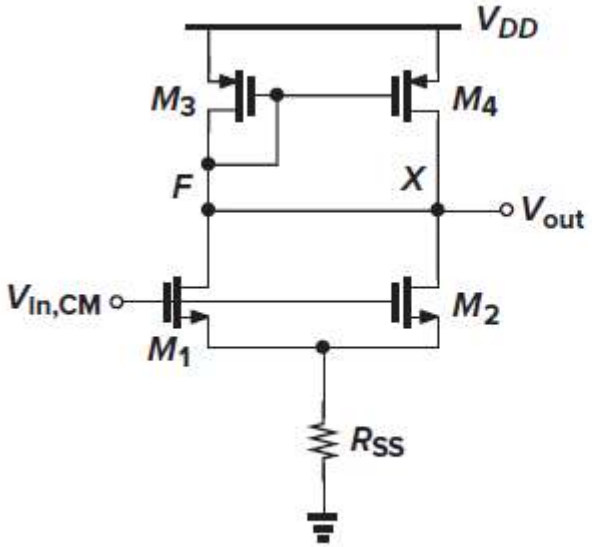
Improvement of OTA



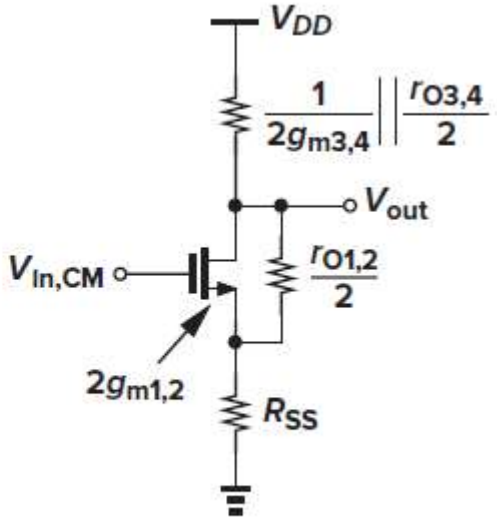
- The above schematic shows an imbalance
- M_3 is diode-connected, $V_{DS3} = V_{GS3} \neq V_{DS4}$
- Add R_1 between nodes F and G to decouple V_{DS3} and V_{GS3}
- Is "$V_{DS3} \neq V_{DS4}$" a big issue? The answer is "No", but …

CMRR of OTA (No Mismatch)





(a)



(b)

$$\text{CMRR} = \left|\frac{A_{DM}}{A_{CM}}\right|$$

$$= g_{m1,2}(r_{O1,2} \| r_{O3,4}) \frac{g_{m3,4}(1 + 2g_{m1,2}R_{SS})}{g_{m1,2}}$$

$$= (1 + 2g_{m1,2}R_{SS}) g_{m3,4}(r_{O1,2} \| r_{O3,4})$$

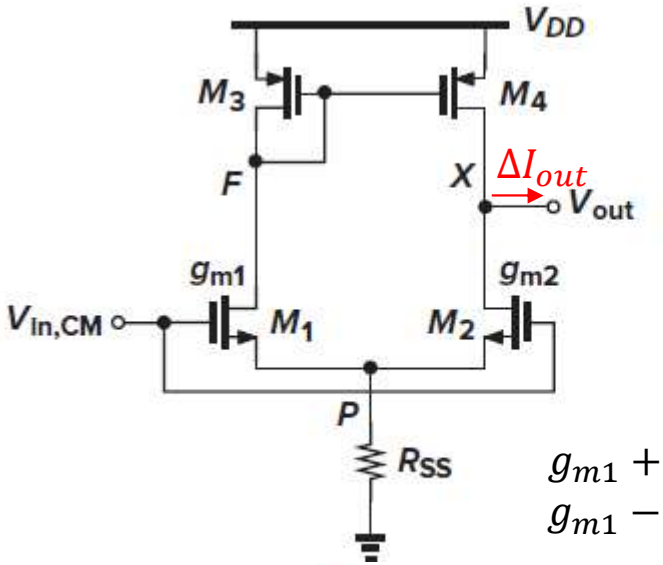
$$A_{CM} = \frac{\Delta V_{out}}{\Delta V_{in,CM}}$$

$$A_{CM} \approx \frac{-\frac{1}{2g_{m3,4}} \| \frac{r_{O3,4}}{2}}{\frac{1}{2g_{m1,2}} + R_{SS}}$$

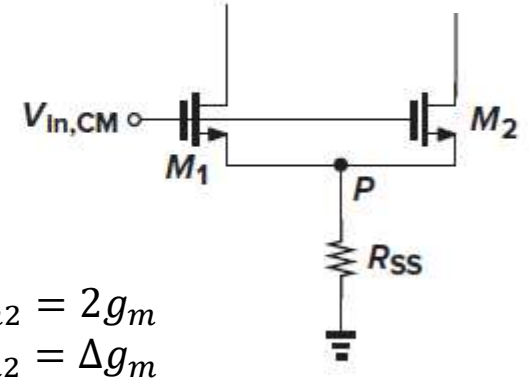
$$= \frac{-1}{1 + 2g_{m1,2}R_{SS}} \frac{g_{m1,2}}{g_{m3,4}}$$

CMRR of OTA – g_m Mismatch

Case 1:



$$\Delta V_P = \Delta V_{in,CM}\frac{R_{SS}}{R_{SS}+\dfrac{1}{g_{m1}+g_{m2}}}$$



$$g_{m1}+g_{m2}=2g_m$$
$$g_{m1}-g_{m2}=\Delta g_m$$

$$\Delta I_{D1}=g_{m1}(\Delta V_{in,CM}-\Delta V_P)$$

$$=\frac{\Delta V_{in,CM}}{R_{SS}+\dfrac{1}{g_{m1}+g_{m2}}}\frac{g_{m1}}{g_{m1}+g_{m2}}$$

$$\Delta I_{D2}=g_{m2}(\Delta V_{in,CM}-\Delta V_P)$$

$$=\frac{\Delta V_{in,CM}}{R_{SS}+\dfrac{1}{g_{m1}+g_{m2}}}\frac{g_{m2}}{g_{m1}+g_{m2}}$$

(b)

$$\Delta I_{out}=\Delta I_{D4}-\Delta I_{D2}\approx\Delta I_{D1}-\Delta I_{D2}$$

$$\Delta I_{out}=\frac{\Delta V_{in,CM}}{1+2g_mR_{SS}}(g_{m1}-g_{m2})$$

$$=\frac{\Delta g_m}{1+2g_mR_{SS}}\Delta V_{in,CM}$$

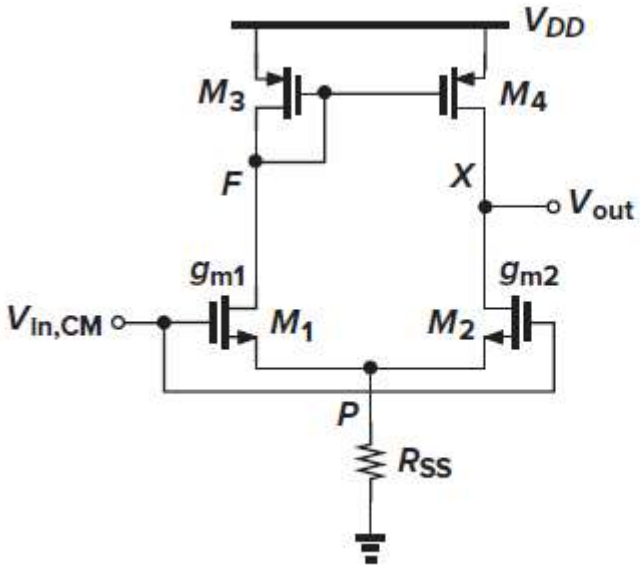
$$\Delta V_{out}=\Delta I_{out}R_{out}$$

$$A_{CM}=\frac{\Delta V_{out}}{\Delta V_{in,CM}}=\frac{\Delta g_mR_{out}}{1+2g_mR_{SS}}$$

$$\text{CMRR}=\left|\frac{A_{DM}}{A_{CM}}\right|=\frac{g_m}{\Delta g_m}(1+2g_mR_{SS})$$

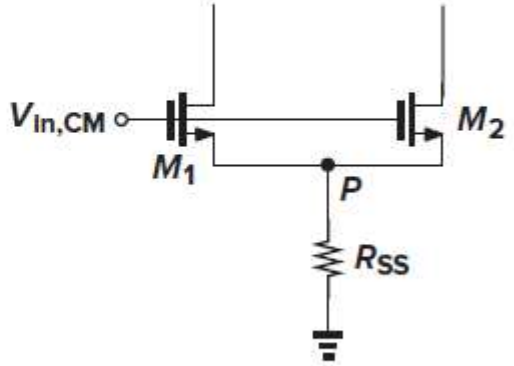
CMRR of OTA – g_m Mismatch

Case 2:



(a)

$$A_{DM} = g_m(r_{o2}||r_{o4})$$



(b)

(ΔI_{D4})

$$\Delta V_{out} = \left[\frac{g_{m1}\Delta V_{in,CM}}{1+(g_{m1}+g_{m2})R_{SS}} \frac{r_{O3}}{r_{O3}+\frac{1}{g_{m3}}} - \frac{g_{m2}\Delta V_{in,CM}}{1+(g_{m1}+g_{m2})R_{SS}} \right] (r_{o2}||r_{o4})$$

(ΔI_{D1}) (ΔI_{D2})

$$= \frac{\Delta V_{in,CM}}{1+(g_{m1}+g_{m2})R_{SS}} \frac{(g_{m1}-g_{m2})r_{O3}-g_{m2}/g_{m3}}{r_{O3}+\frac{1}{g_{m3}}} (r_{o2}||r_{o4})$$

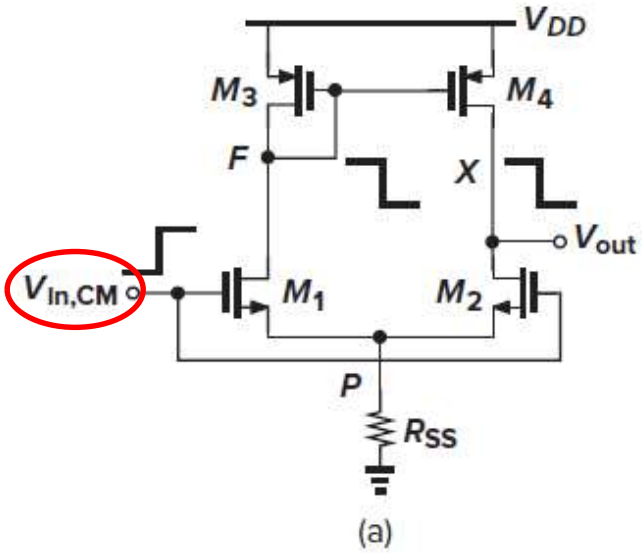
$$\frac{\Delta V_{out}}{\Delta V_{in,CM}} \approx \frac{\Delta g_m g_{m3} r_{o3} - g_{m2}}{1+2g_m R_{SS}} \frac{r_{o2}||r_{o4}}{1+g_{m3}r_{o3}} \approx \frac{\Delta g_m}{1+2g_m R_{SS}} (r_{o2}||r_{o4})$$

$$\text{CMRR} \approx \frac{g_m}{\Delta g_m}(1+2g_m R_{SS})$$

Common-Mode Errors

- Check anything by their definitions

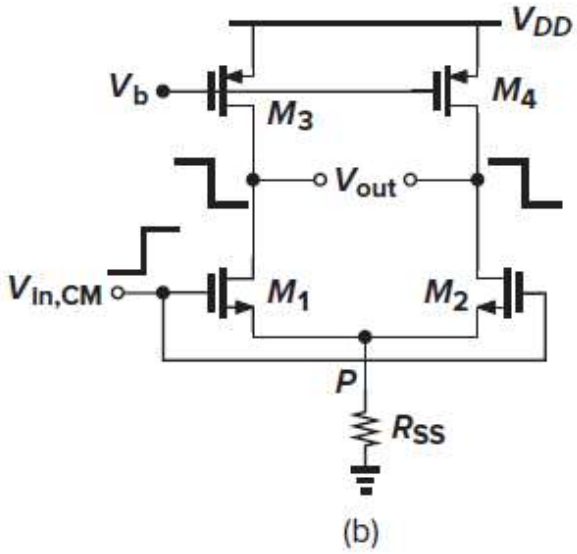
Single-ended output



(a)

$$A_{CM} = \frac{-1}{1+2g_{m1,2}R_{SS}} \frac{g_{m1,2}}{g_{m3,4}}$$

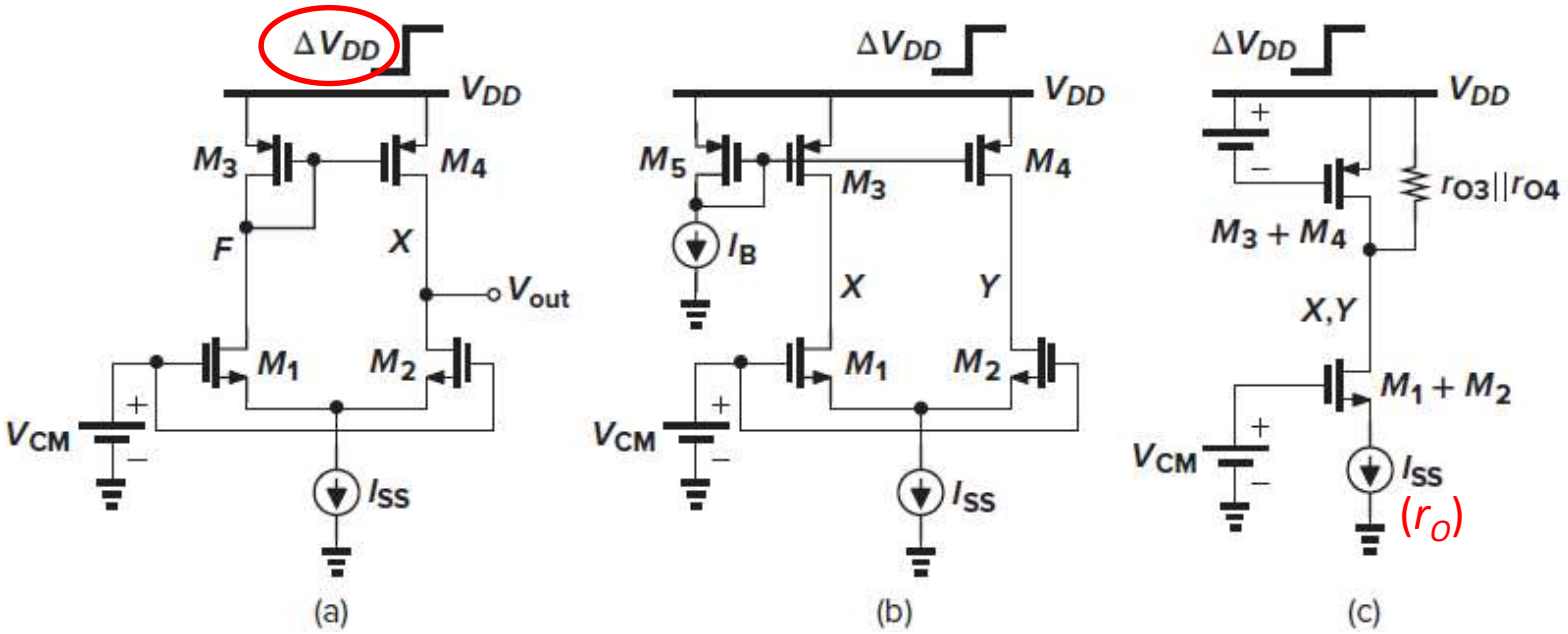
Differential output



(b)

No errors on Vout (= Vop-Von)

Supply Noise



$\Delta V_F \approx \Delta V_{DD}$

$A_{CM} \approx 1$

$\Delta V_X = \Delta V_Y$

$A_{CM} \approx 0$ (if)

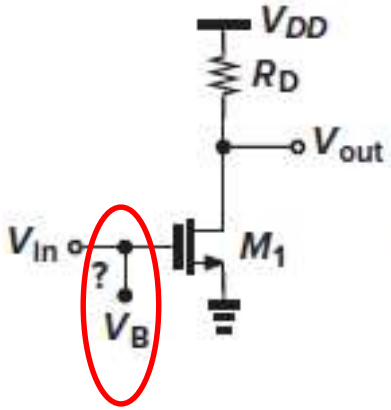
$\Delta V_X = \Delta V_Y \approx \Delta V_{DD}$

if all r_O are much higher

Biasing Techniques

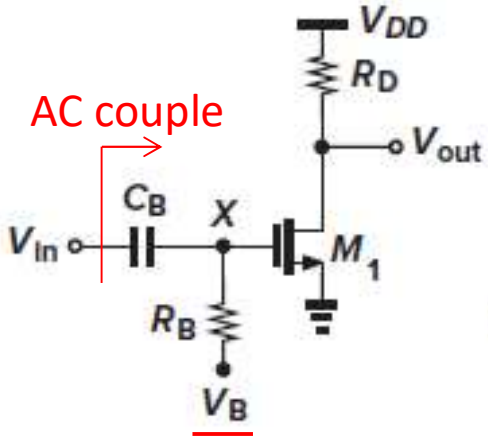
- Common-Source Biasing
- Common-Gate Biasing
- Source Follower Biasing
- Differential Pair Biasing

CS Biasing



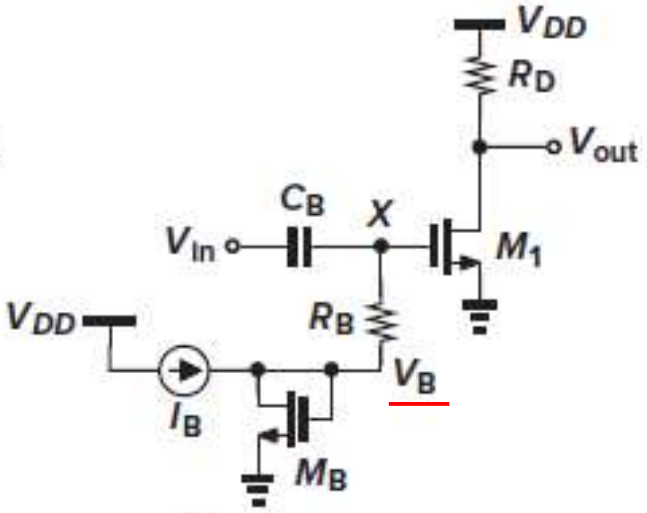
=> DC + AC

(a)

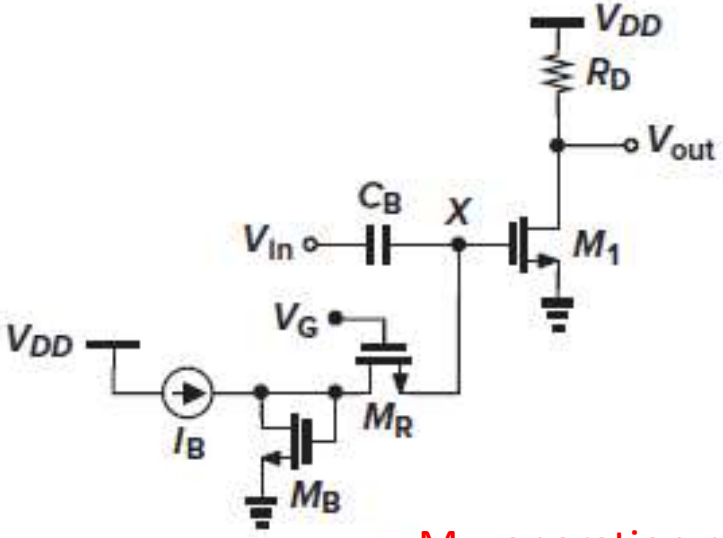


DC set

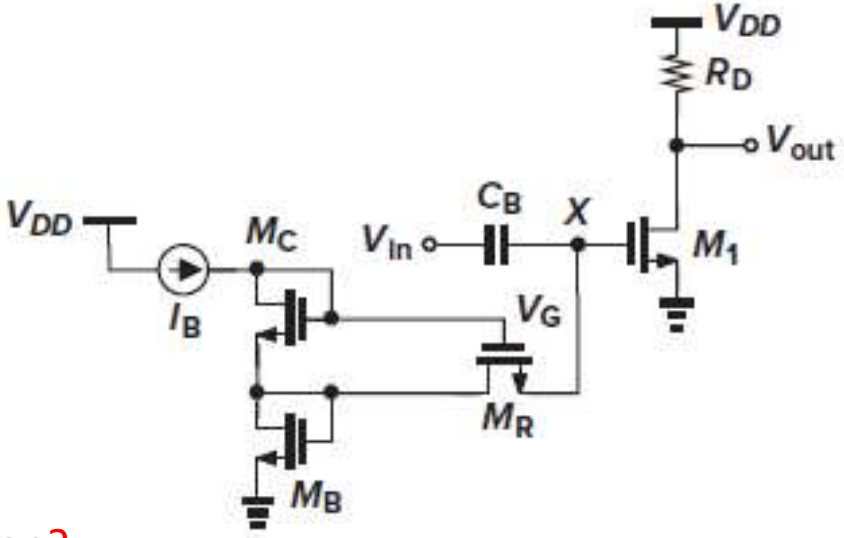
(b)



(c) I_B=? How to determine V_B?

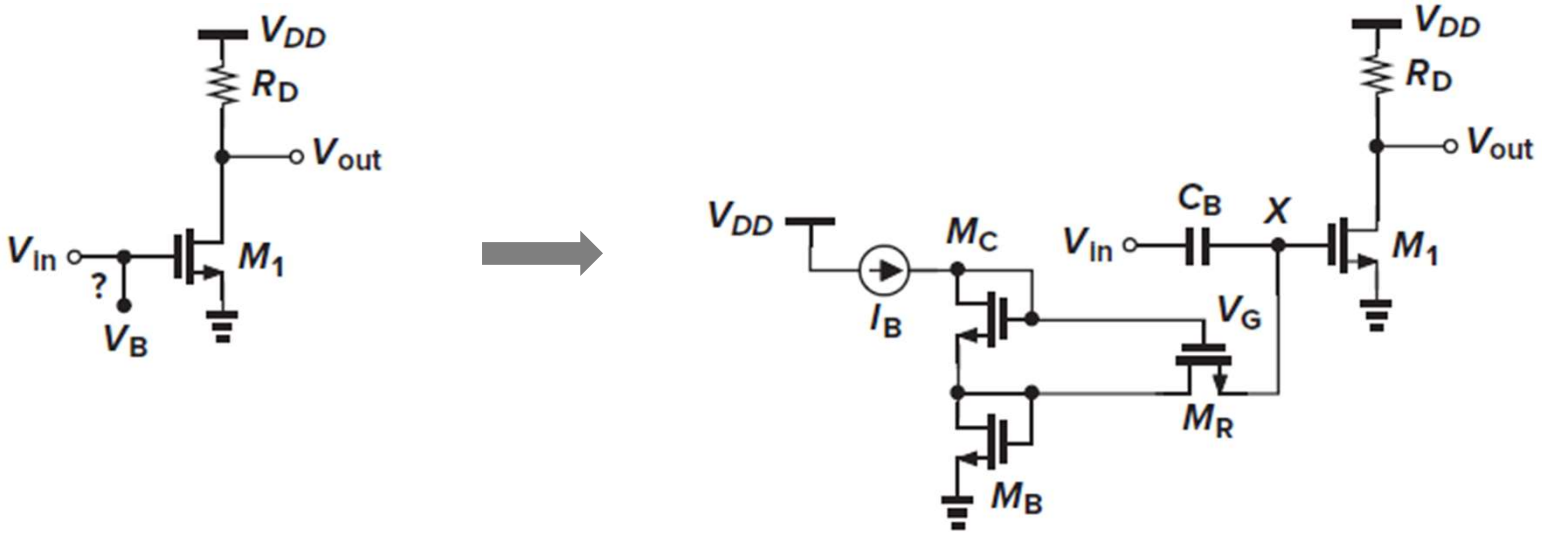


(d) M_R: operation region?



(e)

CS Biasing

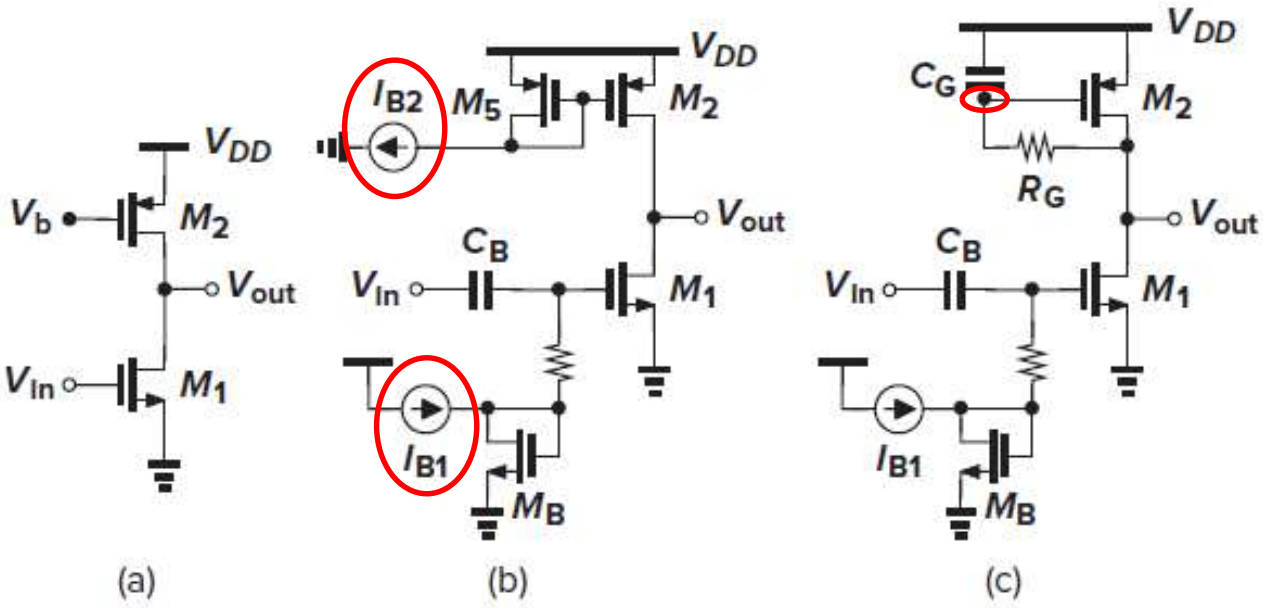


If $(W/L)_C$ is large, $V_{GS,C} \approx V_{TH}$, producing a high resistance in M_R. Using a long-channel model, you can prove that, in strong inversion,

$$R_{on,R} = \frac{(W/L)_C}{(W/L)_R}\frac{1}{g_{m,C}}$$

The proof is assigned as HW4.1

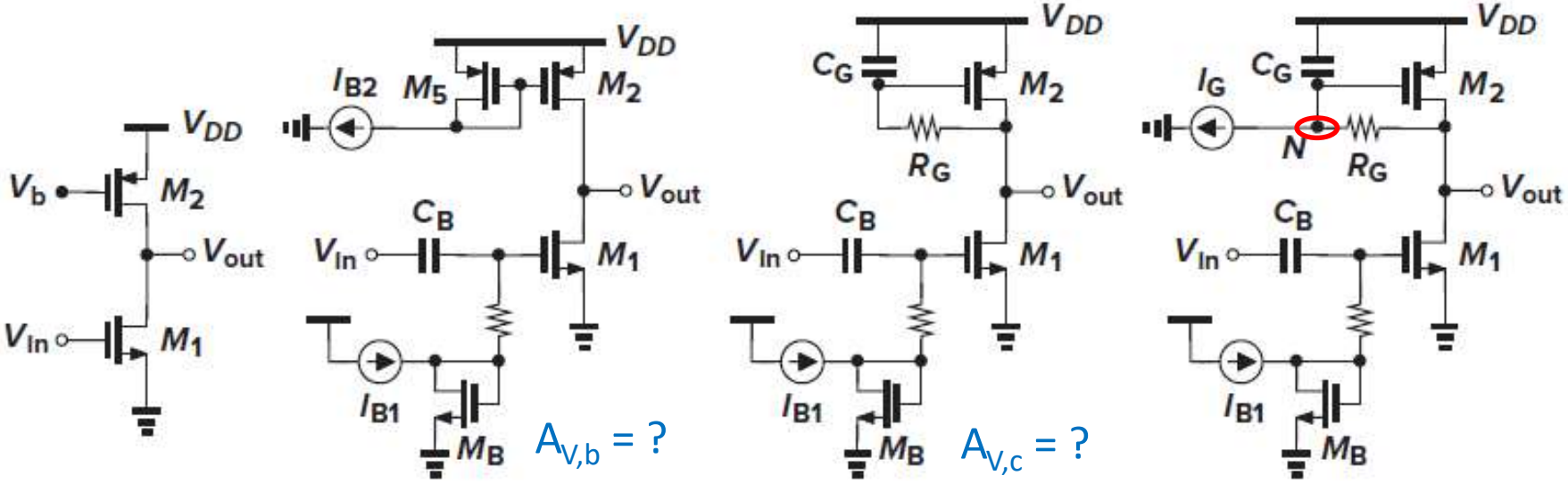
CS Stage with Current-Source Load



$R_G >> r_{O1} \| r_{O2}$

- If the copied currents in Fig. 5.45(b), I_{D1} and I_{D2}, are not exactly equal, each transistor wants to impose its own current. But, …
- But, if $I_{D1} \neq I_{D2}$
- Therefore, self-biasing in Fig. 5.45(c) is necessary!!
- R_G introduce a large area cost and $1/(2\pi R_G C_G)$ is less than the lowest signal frequency of interest (Vout's ac term does not affect the bias!!)

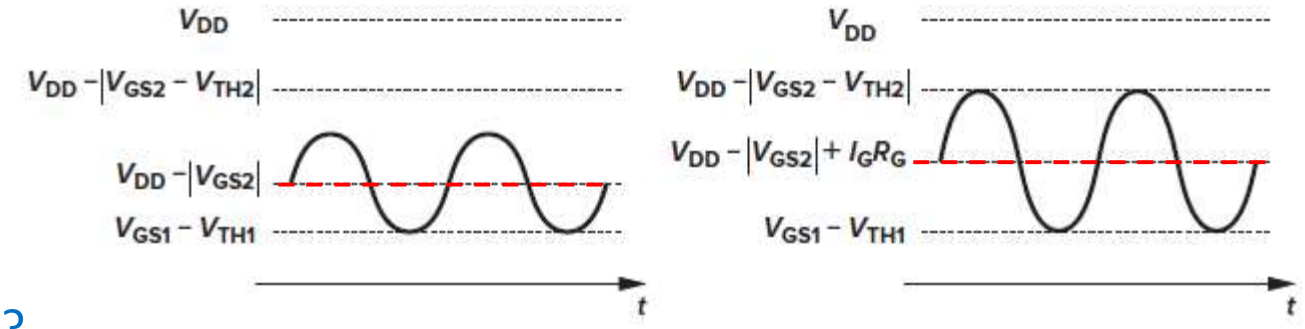
CS Stage with Current-Source Load



$A_{V,b}$ = ?

$A_{V,c}$ = ?

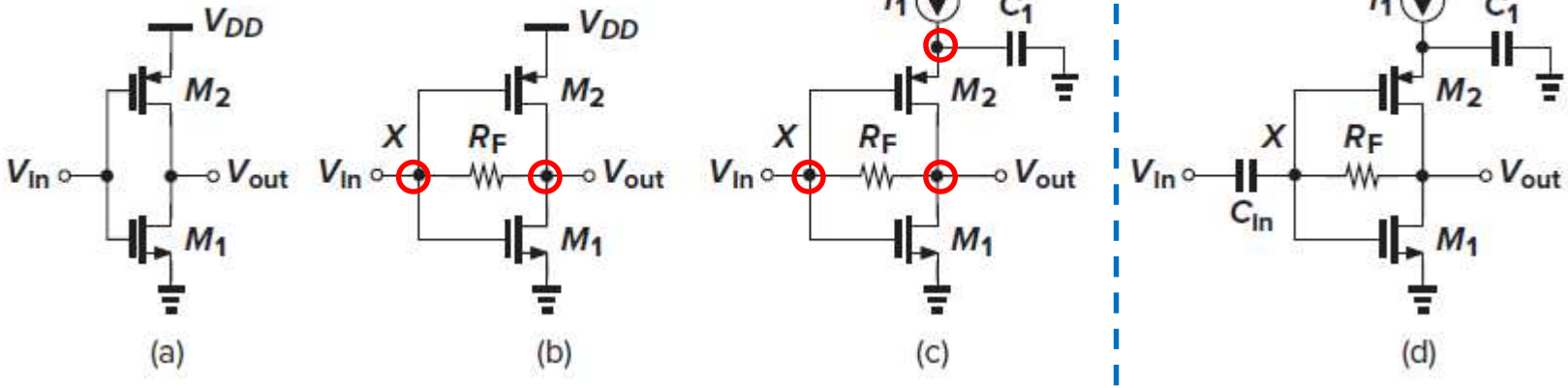
(R_G, C_G)



Q1: For (b) and (c), A_V = ?

Q2: Why using I_G?

Complementary CS Stage



A worse amplifier

A self-biased amplifier

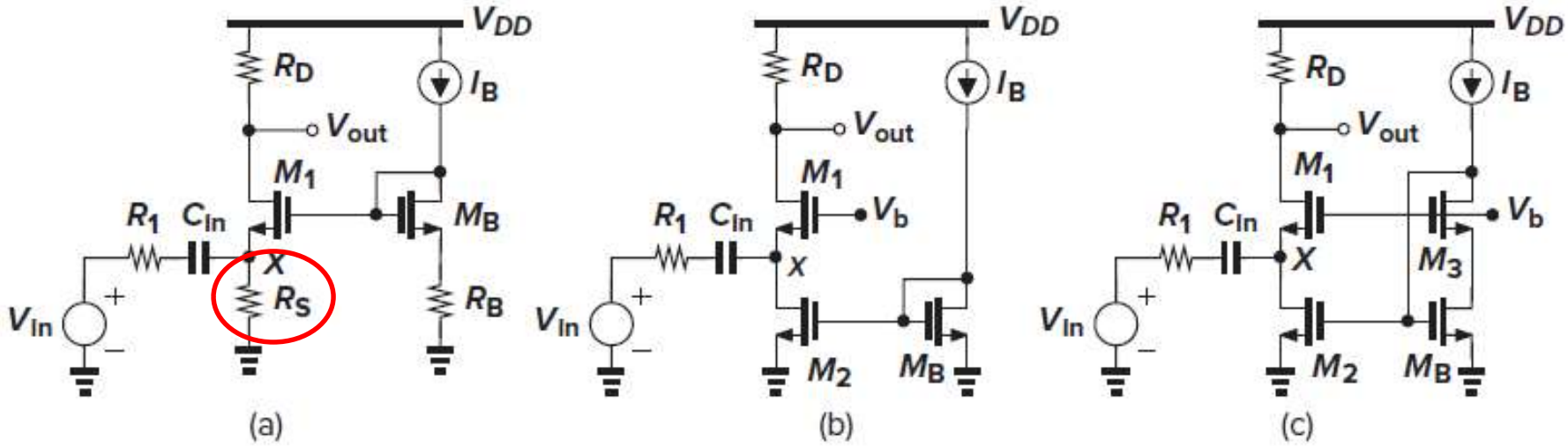
An amplifier with constant current

An amplifier with constant current and input isolation

$$\frac{1}{C_1\omega_{min}} \ll \frac{1}{g_{m2}}$$

- How to define these node voltages?

Common-Gate Biasing



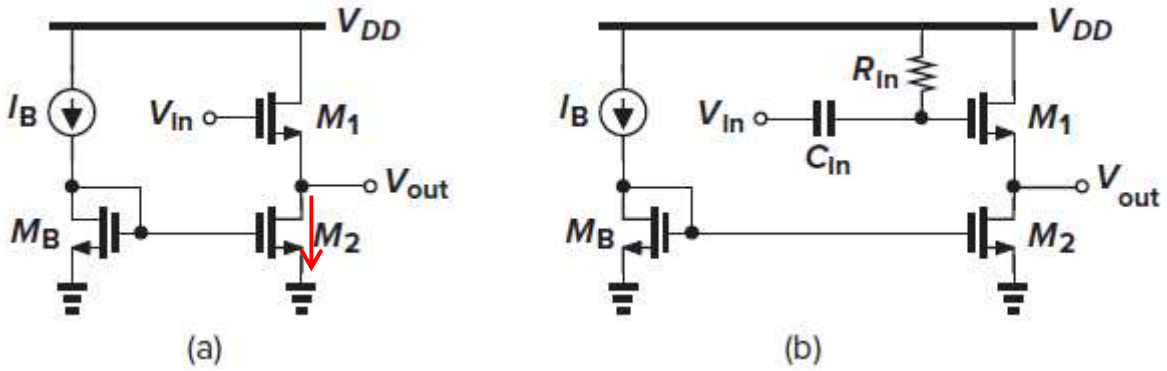
- R_S has input attenuation
- Why R_B?

➡ To remove the input attenuation, but a worse current mirror

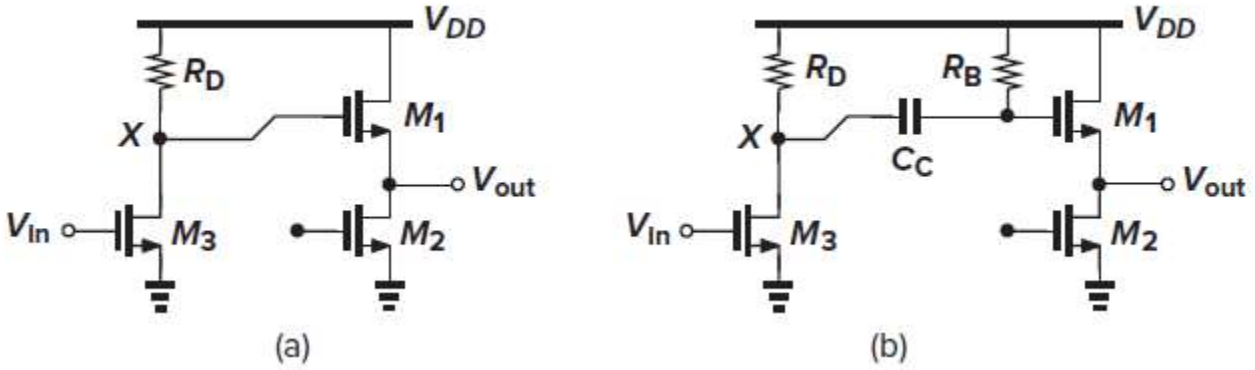
➡ To remove the input attenuation and a good current mirror

$$\frac{V_X}{V_{in}} = \frac{\frac{1}{g_{m1}+g_{mb1}}||R_S}{\frac{1}{g_{m1}+g_{mb1}}||R_S + R_1}$$

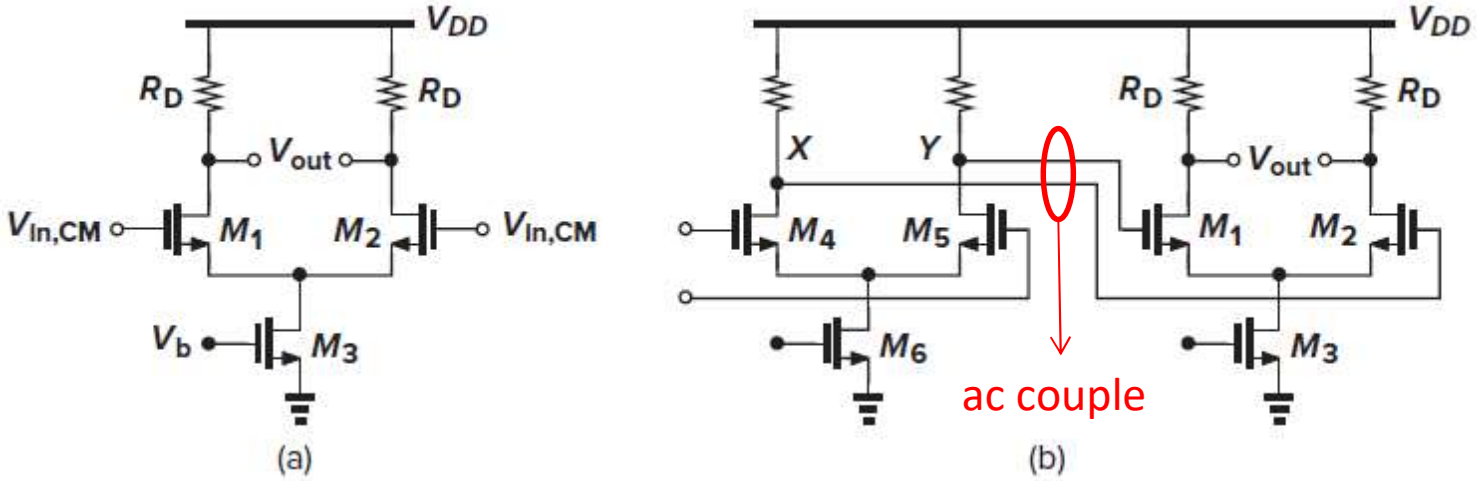
Source Follower Biasing



Example 5.15



Differential Pair Biasing



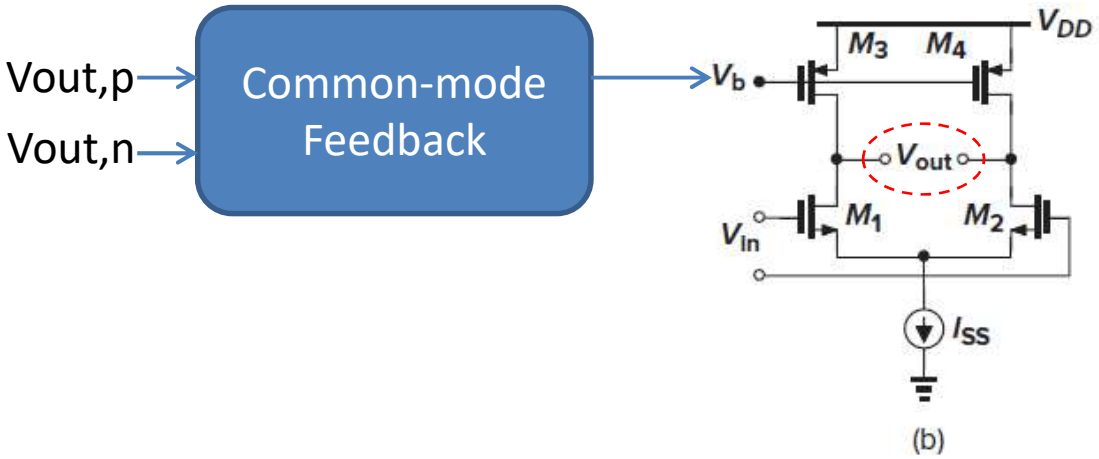
The first stage gain limits …

Better to use ac couple between two stages. If using active current load, what do we need?

OR, …

Do you have a better idea?

Common-Mode FeedBack



- Common-mode feedback (CMFB) loop is a feedback control to suppress the output stage p/n current mismatch
- Vout,p = Vocm+ΔVo/2; Vout,n = Vocm-ΔVo/2
- Only common-mode term (Vocm) is processed for better operating points
- The root cause is the output nodes are high impedance
- Even a small current mismatch can cause a large DC shift
- For example, ΔI=1uA, Rout=1Mohm => IR drop is 1V!!