Introduction to Analog Integrated Circuits (111), DECE, NTUST

Homework 3 (Due date: 10/19)

HW3.1: (20 points)

Fig. 3.1 shows a fully differential amplifier and its transfer curves. Assume Vin1 and Vin2 are differential signals, for $I_{D1}=I_{D2}=I_{SS}/2$, $V_{GS1} = V_{GS2} = V_{TH}+200mV$. ΔVin1 is a specified voltage means M1 or M2 is turned off. Please identify ΔVin1 and describe Gm = *f*(ΔVin). Note: *channel length modulation* and *body effect* are ignored.

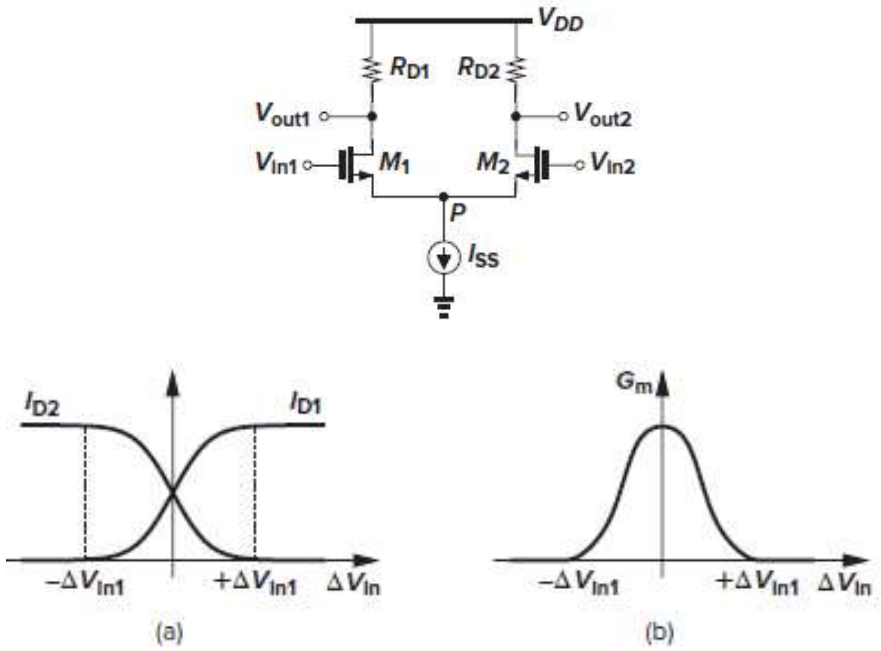

Fig. 3.1

HW3.2: (30 points)

Assuming that all the transistors in the circuits of Figs. 3.2 are saturated and $\lambda \neq 0$, calculate the small-signal differential voltage gain. Please specify their positive and negative input and output nodes.

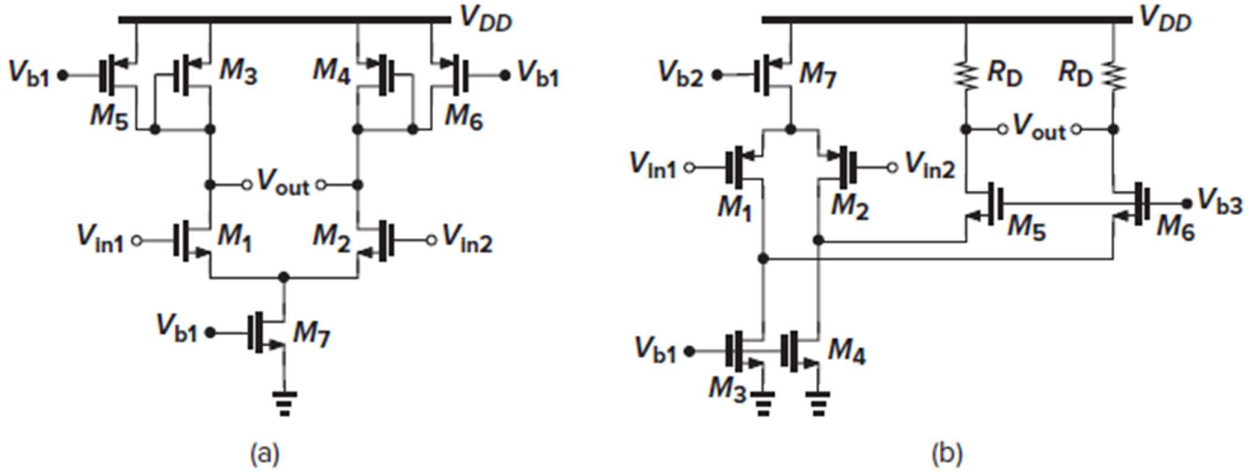

Fig. 3.2

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HW3.3 (30 points)

Table 2.1 Level 1 SPICE models for NMOS and PMOS devices.

NMOS Model			
LEVEL = 1	VTO = 0.7	GAMMA = 0.45	PHI = 0.9
NSUB = 9e+14	LD = 0.08e−6	UO = 350	LAMBDA = 0.1
TOX = 9e−9	PB = 0.9	CJ = 0.56e−3	CJSW = 0.35e−11
MJ = 0.45	MJSW = 0.2	CGDO = 0.4e−9	JS = 1.0e−8
PMOS Model			
LEVEL = 1	VTO = −0.8	GAMMA = 0.4	PHI = 0.8
NSUB = 5e+14	LD = 0.09e−6	UO = 100	LAMBDA = 0.2
TOX = 9e−9	PB = 0.9	CJ = 0.94e−3	CJSW = 0.32e−11
MJ = 0.5	MJSW = 0.3	CGDO = 0.3e−9	JS = 0.5e−8

$\varepsilon_{ox} = \varepsilon_{SiO2} \cdot \varepsilon_0$, $\varepsilon_{SiO2} = 3.9$, $\varepsilon_0 = 8.85*10^{-14}$ F/cm

VDD=3.3V; VSS=0V

Suppose the differential pair of Fig. 3.3 is designed with $(W/L)_{1,2}$=50/0.5, $(W/L)_{3,4}$=10/0.5, R_1=R_2=1MΩ, and I_{SS} = 0.5 mA. Also, I_{SS} is implemented with an NMOS device having $(W/L)_{SS}$=50/0.5.

(a) What are the maximum and minimum allowable input common-mode levels if the differential swing at the input and output are small? (10 points)

(b) For $V_{in,CM}$ = 1.2V, calculate the small-signal differential voltage gain. (10 points)

(c) Suppose M_1 and M_2 have a threshold voltage mismatch of 1mV. What is the CMRR? (10 points)

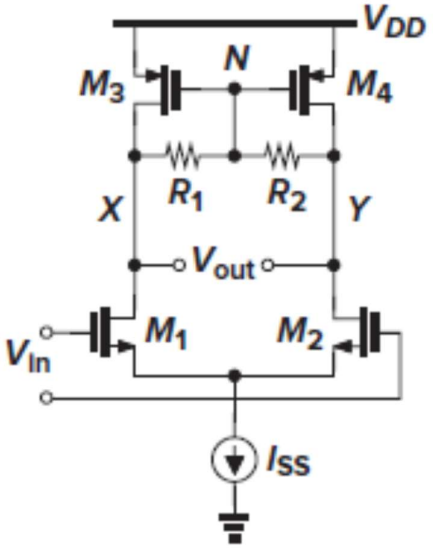

Fig. 3.3

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HW3.4: (20 points)

Consider the circuit shown in Fig. 3.4. VDD=3.3V and VSS=0.

(a) Sketch V_{out} as V_{in1} and V_{in2} vary differentially from zero to VDD.

(b) If $\lambda = 0$, obtain an expression for the voltage gain. What is the voltage gain if $W_{3,4} = 0.8W_{5,6}$?

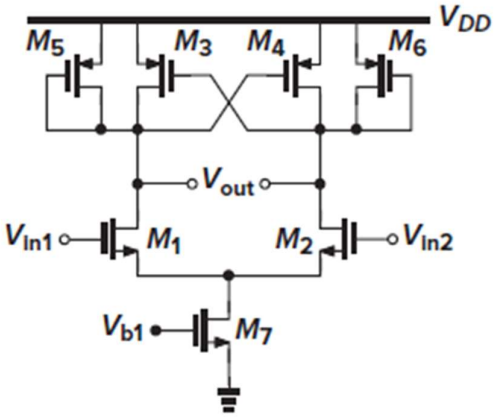

Fig. 3.4