Digital Logic Design

(ET3305302)

Exam #2 — Closed books

Date: June 6, 2023
Time limit: 100 minutes

This exam has five problems in total. Please read each problem carefully and write down your answers on the answer sheet.

1. (20%) Answer each of the following questions:

   (a) Explain the differences among the bistable device, latch, and flip-flop.

   (b) In using a flip-flop, what are the three timing parameters that must be considered?

   (c) What is a self-correcting (also called self-starting) circuit?

   (d) How would you allow to input data into a D flip-flop as desired but also to be able of keeping the output of the D flip-flop unchanged if necessary? Give at least two methods and explain their operation.

2. (20%) Analyzing the sequential circuit shown in Figure 1, answer each of the following questions:

   (a) Derive the excitation functions of flip-flops from the sequential circuit.

   (b) Derive the transition table from the excitation functions.

   (c) Is the sequential circuit self-starting? Explain it. If not, try to modify it so that it may become self-starting.

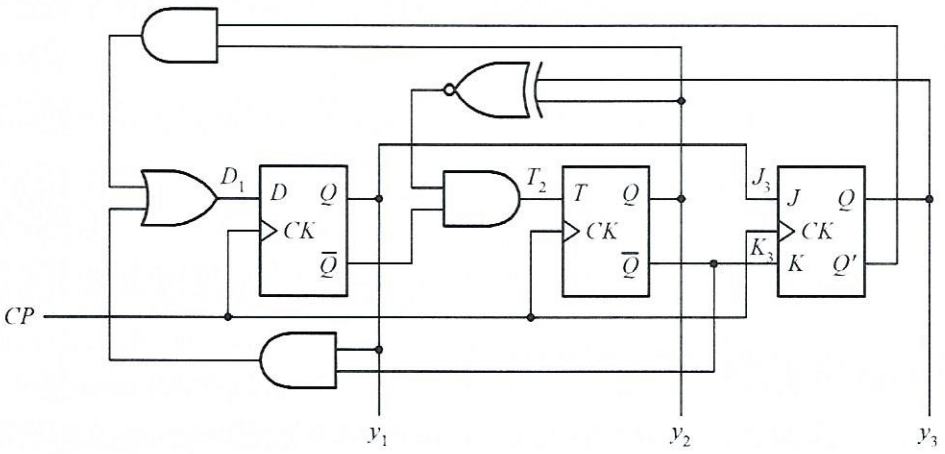

Figure 1: State table of Problem 2.

3. (20%) Considering the state tables shown in Figure 2, answer each of the following questions:

   (a) Use the compatibility method to simplify the state table shown in Figure 2(a). What is the minimal state table? Represent the minimal state table in standard form.

   (b) Use the k-partition method to simplify the state table depicted in Figure 2(b). What is the minimal state table? Represent the minimal state table in standard form.

PS	x = 0	x = 1
A	D,0	C,0
B	F,0	A,1
C	D,0	A,0
D	C,0	E,0
E	F,0	C,1
F	E,0	D,1

(a)

PS	x = 0	x = 1
A	B,0	C,1
B	B,0	D,0
C	E,1	C,1
D	B,0	F,0
E	G,1	C,1
F	B,0	C,1
G	B,0	C,1

(b)

Figure 2: State tables of Problem 3.

4. (20%) Considering the state diagram shown in Figure 3, answer each of the following questions:

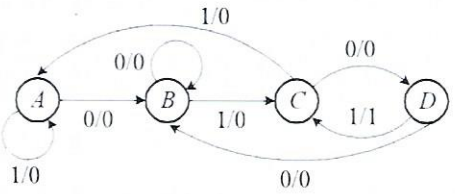

Figure 3: State table of Problem 4.

   (a) Draw its equivalent ASM chart.

   (b) Using the one-hot method, implement the ASM chart you obtained.

5. (20%) Design a sequential circuit to generate the following output sequence ($wxyz$) repeatedly:

$$0 \longrightarrow 8 \longrightarrow 12 \longrightarrow 14 \longrightarrow 15 \longrightarrow 7 \longrightarrow 3 \longrightarrow 1 \longrightarrow 0...$$

   (a) Write your design procedure, assuming that a 4-stage shift register is employed along with a combinational logic circuit.

   (b) Draw the logic circuit with D flip-flops and necessary logic gates if necessary.

   (c) Draw the logic circuit with JK flip-flops and necessary logic gates if necessary.