Digital Logic Design

(ET3305302)

Exam #1 — Closed books

Date: April 18, 2023
Place: IB410-2
Time limit: 100 minutes

This exam has five problems in total. Please read each problem very carefully and write your answers on the answer sheet clearly.

1. (20%) Answer each of the following questions:

   (a) Carry out the calculation of $32_{10} - 28_{10}$ in binary number system.

   (b) Carry out the calculation of $27_{10} - 37_{10}$ in binary number system.

   (c) What is the meaning of a self-complementing code? Define it.

   (d) Assuming that the weight of a weighted code is (6, 2, -2, 3), list the codewords representing the decimal digits on condition that your code must be self-complementing.

2. (20%) Answer each of the following questions:

   (a) Prove the following equality (consensus theorem):
   $x \cdot y + x' \cdot z + y \cdot z = x \cdot y + x' \cdot z$

   (b) Use the consensus theorem in (a) to simplify the following switching expression:
   $f(v, w, x, y, z) = vwxy + w'xyz + v'w' + wxz' + vxyz$

3. (20%) Simplify the following switching function with the tabulation method:

   $$f(w, x, y, z) = \Sigma(1, 3, 4, 5, 10, 11, 12, 14)$$

   (a) Find all prime implicants with the tabulation method. Note that *you will get no credit of this problem if you do not apply the tabulation method.*

   (b) Construct a prime implicant (PI) chart based on the prime implicants obtained from (a).

   (c) Find the minimal expression with Petrick's method from the PI chart obtained in (b).

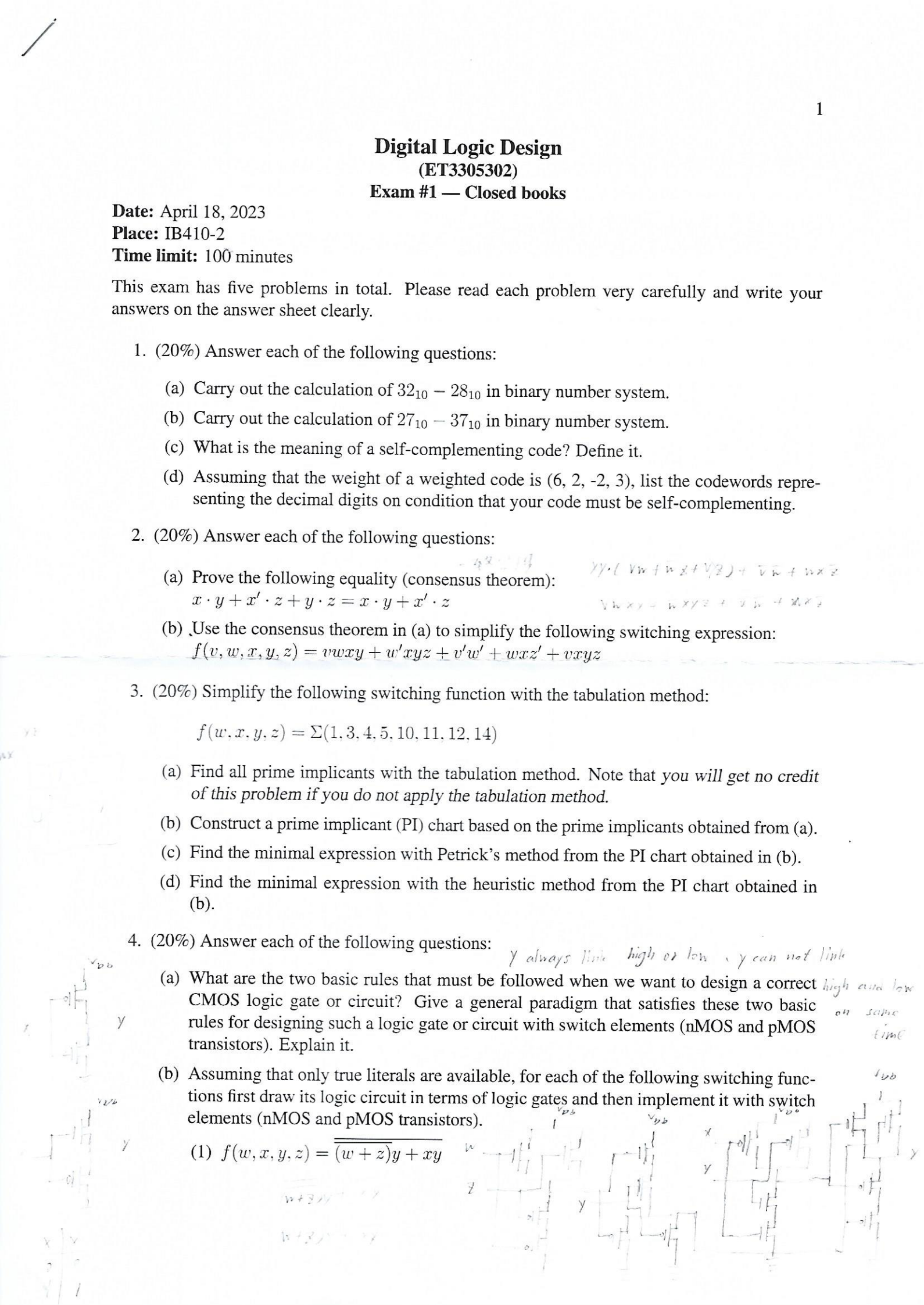
   (d) Find the minimal expression with the heuristic method from the PI chart obtained in (b).

4. (20%) Answer each of the following questions:

   (a) What are the two basic rules that must be followed when we want to design a correct CMOS logic gate or circuit? Give a general paradigm that satisfies these two basic rules for designing such a logic gate or circuit with switch elements (nMOS and pMOS transistors). Explain it.

   (b) Assuming that only true literals are available, for each of the following switching functions first draw its logic circuit in terms of logic gates and then implement it with switch elements (nMOS and pMOS transistors).

   (1) $f(w, x, y, z) = \overline{\overline{(w + z)}y + xy}$



(2) $f(w,x,y,z) = \overline{\overline{(wy)}z + xyz}$

You do not need to further simplify them but you need to use the minimum number of MOSFETs in each case. In addition, you are not allowed to use any inverter to convert a literal into its complement form.

5. (20%) Assume that we want to design a transmission system capable of detecting and correcting any single-bit error. The messages to be transmitted are BCD codes. At the transmitter, the incoming BCD codeword is first encoded into the Hamming code and then transmitted to the receiver. At the receiver, the incoming Hamming code is decoded back into its correct BCD codeword. The communication channel between the transmitter and the receiver may encounter noise and hence the message passing through it may be corrupted at most one bit of each Hamming codeword.

   (a) Design and draw the resulting block diagram of the system.

   (b) Explain the operation of your system.

   (c) How many parity bits are required?

   (d) Describe how to verify the correction of your system, meaning that how would you add an erroneous single-bit to the communication channel.