TAIWAN TECH National Taiwan University of Science and Technology

Analog Integrated Circuit Design and Applications

Spring 2023

Yung-Hui Chung

MSIC Lab

DECE, NTUST

Mixed-Signal IC Laboratory NTUST

Instructor and Grading

- **Instructor: Yung-Hui Chung (鍾勇輝)**
  - Course time: T6, T7, W6
  - Classroom: T6/T7 (IB-304); W6 (EE-503)
  - Office hours: Tue. 10:00~12:00 (by email)
  - Office: **EE-601-2**
  - TEL: 02-27376394 (#6394)
  - Email: yhchung@mail.ntust.edu.tw
  - TA: 張凱棋、郭駿浩 (Lab: **EE-601-2**, #7138)

- **Grading**
  - Homework & Lab: 40%
  - Mid-Exam: 30%
  - Final Project: 30%

Textbooks and References

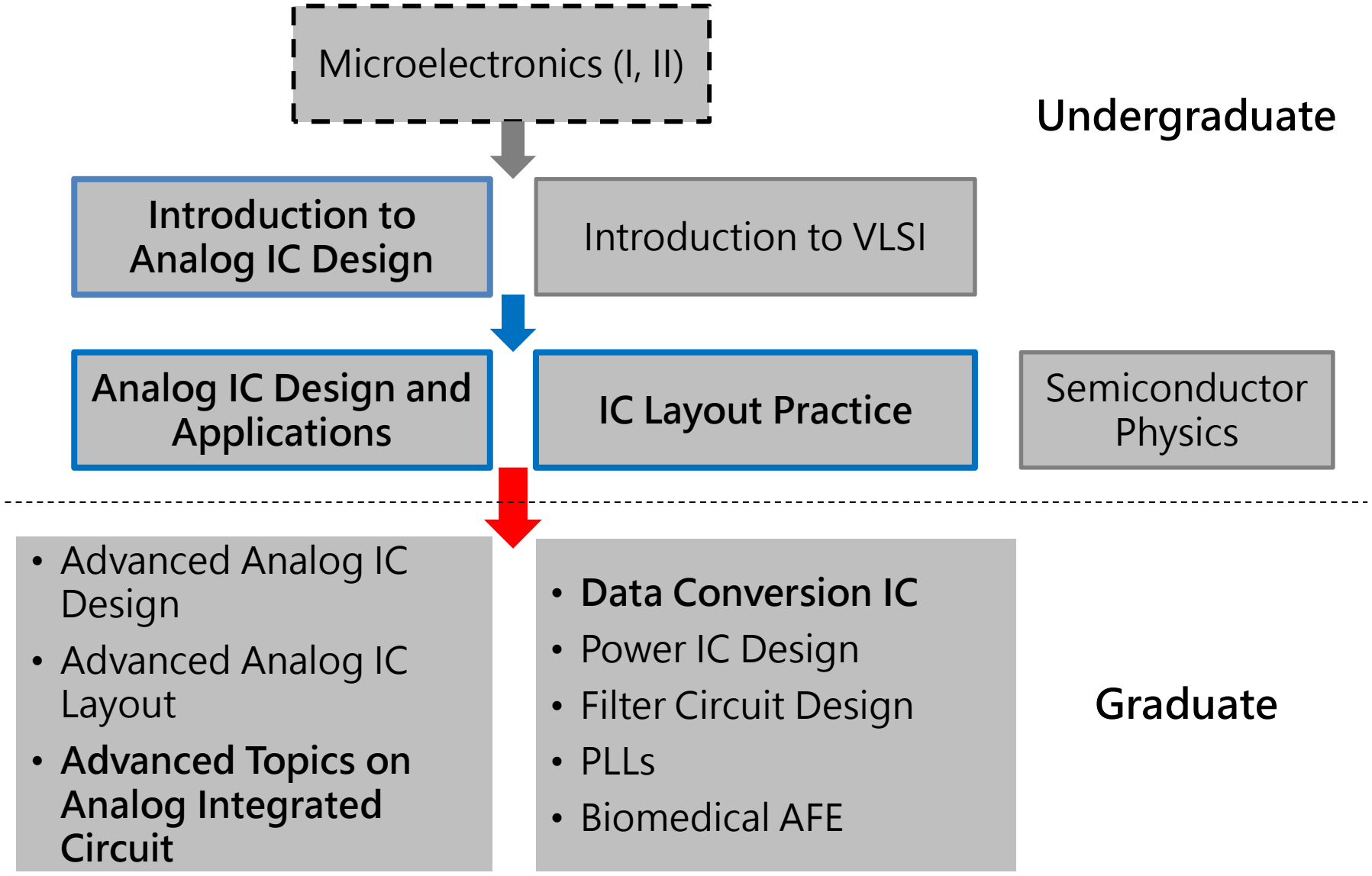
- **Textbook:**
  - Behzad Razavi, **Design of Analog CMOS Integrated Circuits**, McGraw-Hill, 2nd Edition, 2017

- **References:**
  - Phillip E. Allen, Douglas E. Holberg, **CMOS Analog Circuit Design**, 3rd Edition, Oxford, 2011
  - Tony Chan Carusone, David A. Johns and Kenneth W. Martin, **Analog Integrated Circuit Design**, 2nd Edition, Wiley, 2011
  - Gray, Hurst, Lewis and Meyer, **Analysis and Design of Analog Integrated Circuits**, 5th Edition, Wiley, 2008
  - Willy M. C. Sansen, **Analog Design Essentials**, Springer, 2006

Course Content

- AIC1 (Introduction to Analog IC Design)
  - MOS Device Physics and Modeling
  - Short Channel Effects
  - Review of Amplifiers
  - Current Mirrors and Biasing Techniques
  - Frequency Response
  - Stability and Frequency Compensation
- **AIC2 (Analog IC Design and Applications)**
  - Noise
  - Operational Amplifiers (Basic Opamp)
  - Bandgap References
  - Advanced Opamp
  - Switched-Capacitor Circuits
  - Nonlinearity and Mismatch
  - Nanometer Design

Analog IC Courses



Lab Introduction

- Lab0: CAD Setup Introduction
- Lab1: MOS simulation (g_m/I_d)
- Lab2: Current Mirrors
  - Accuracy check for different type CMs
- Lab3: Single-Stage Opamps
  - Telescopic
  - Folded-cascode
- Lab4: Two-Stage Opamp
  - Folded-cascode + CS + …
- Lab5: LDO
  - Opamp applications

Final Project

- Choose one of the following both topics

- A Bandgap Reference Circuit (lecture 13)
  - Reference paper:
    -

- A Switch-Capacitor Circuit (lecture 15)
  - A Fully-Differential Flip-Around Track-and-Hold Circuit
  - Using switched-capacitor operation

Analog Design Challenges

- Transistor Imperfections
- Declining Supply Voltages
  - $5V \rightarrow 2.5V \rightarrow 1.8V \rightarrow 1.2V \rightarrow 0.9V \rightarrow \ldots \rightarrow 0.5V$
- Low Power Request
- Less Circuit Complexity
- Sensitive to PVT Variations
  - Process Corner: TT, FF, SS, SNFP, FNSP
  - Supply Voltage: VDD +/- 10%
  - Temperature: -40°C ~ +125°C

Abstraction Levels in Circuit Design

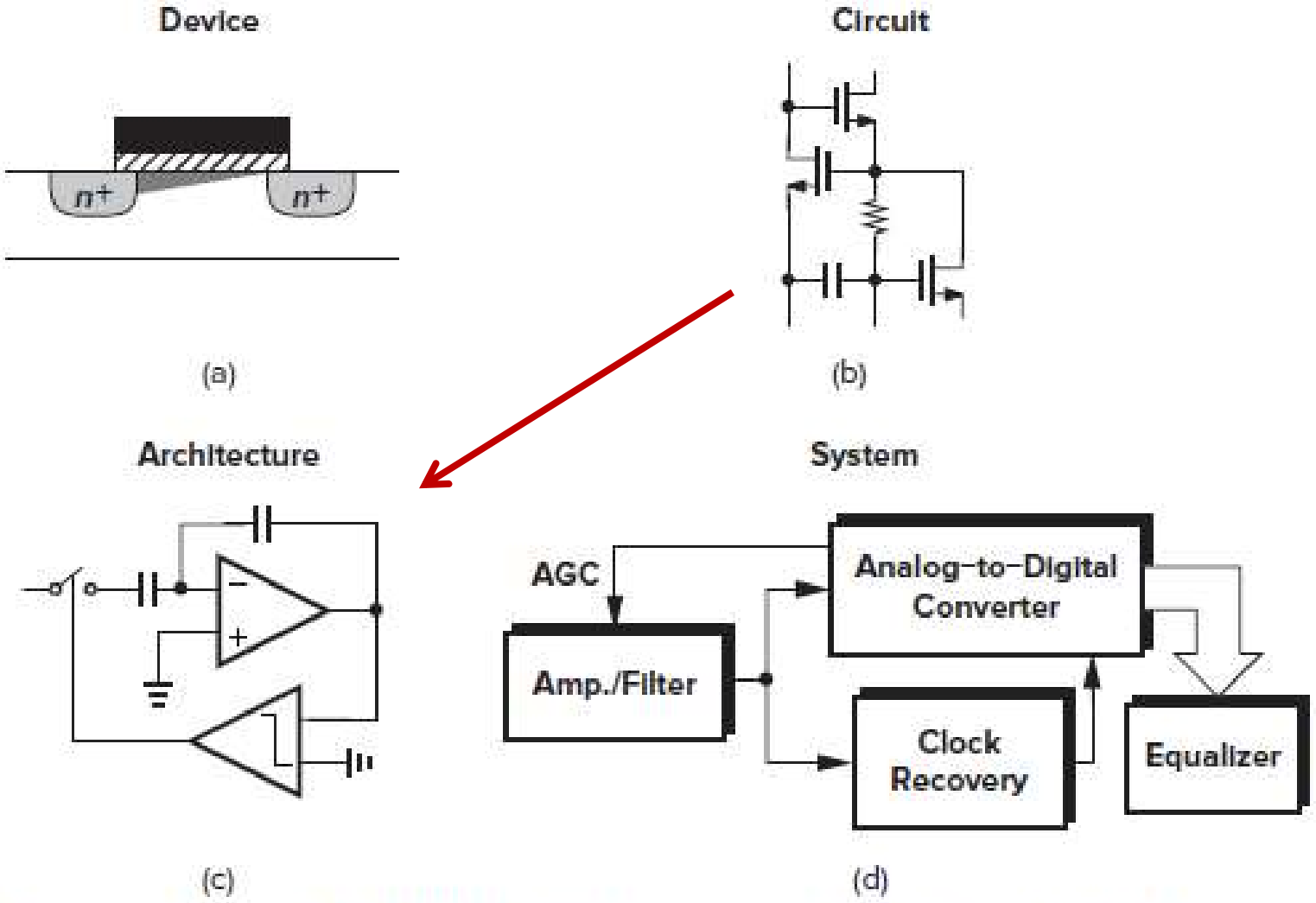
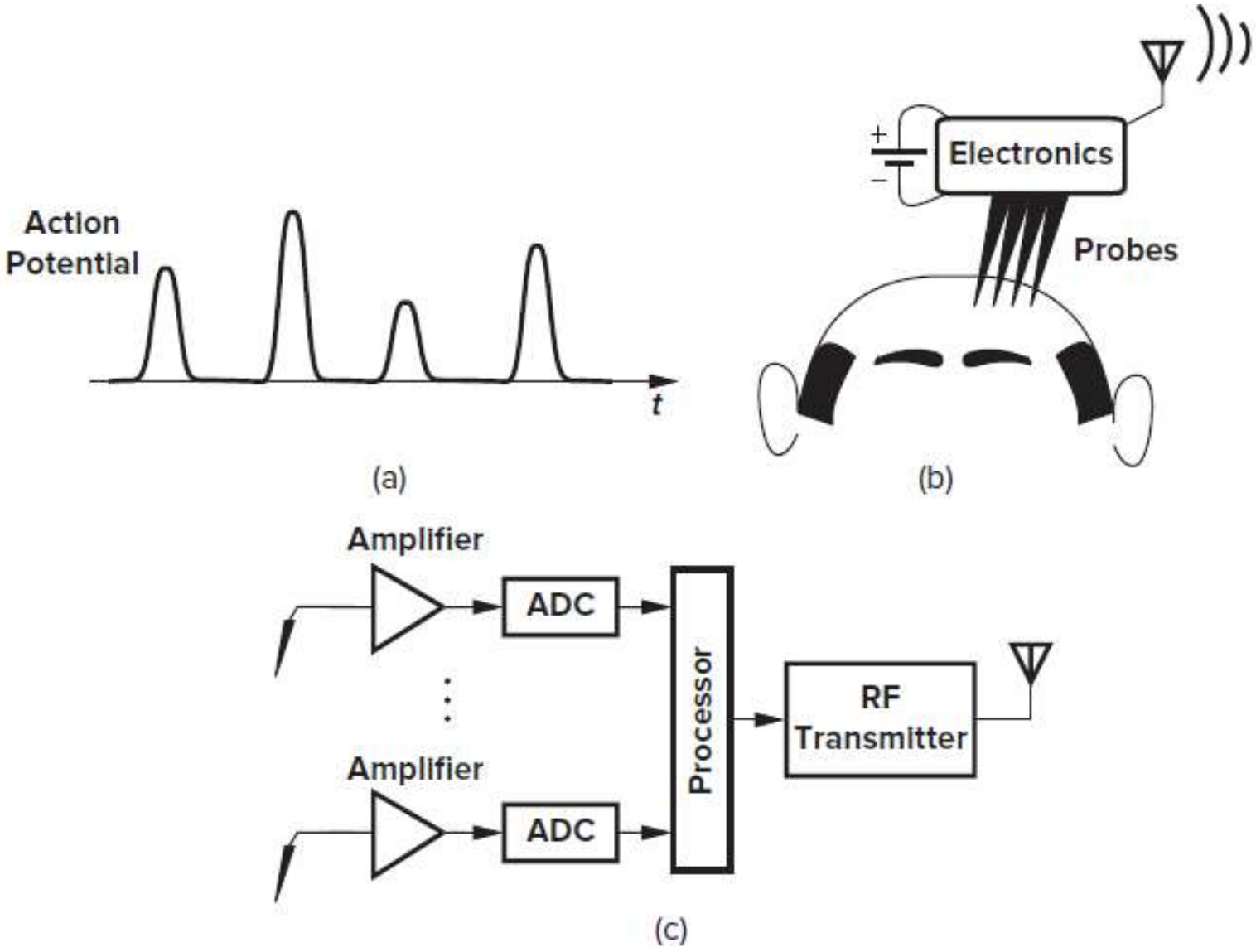
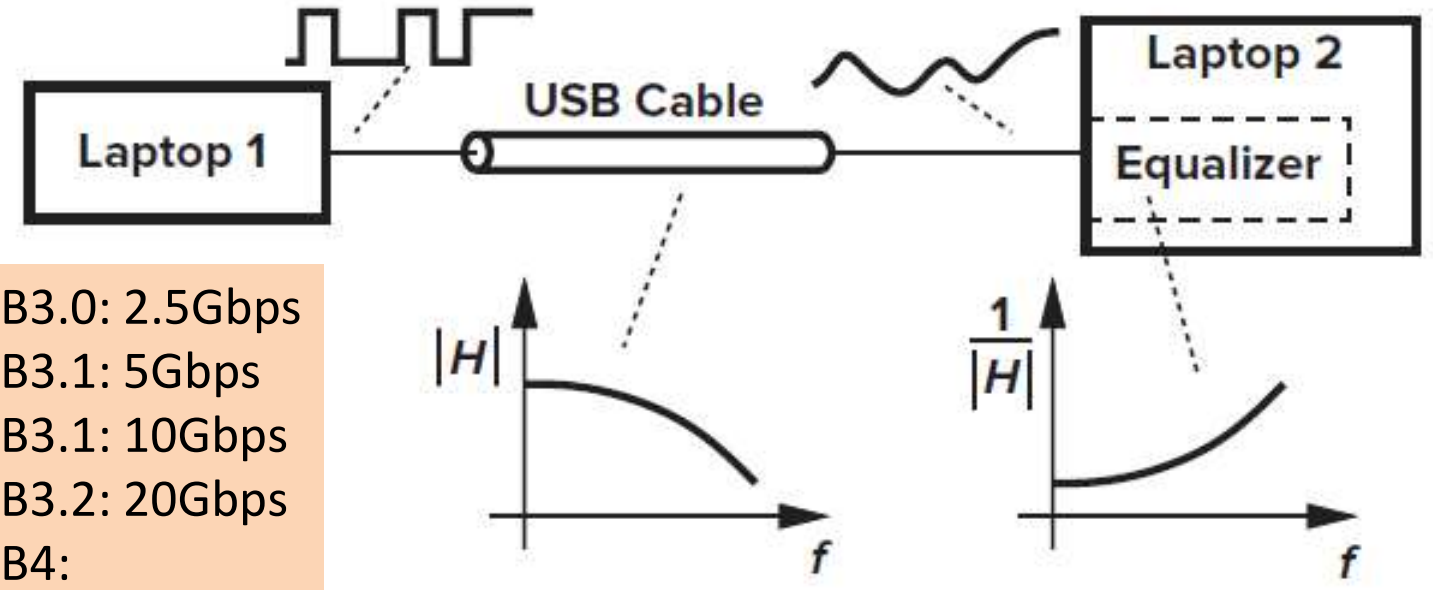


Figure 1.5 Abstraction levels in circuit design: (a) device level, (b) circuit level, (c) architecture level, (d) system level.

Biomedical Analog Front-End



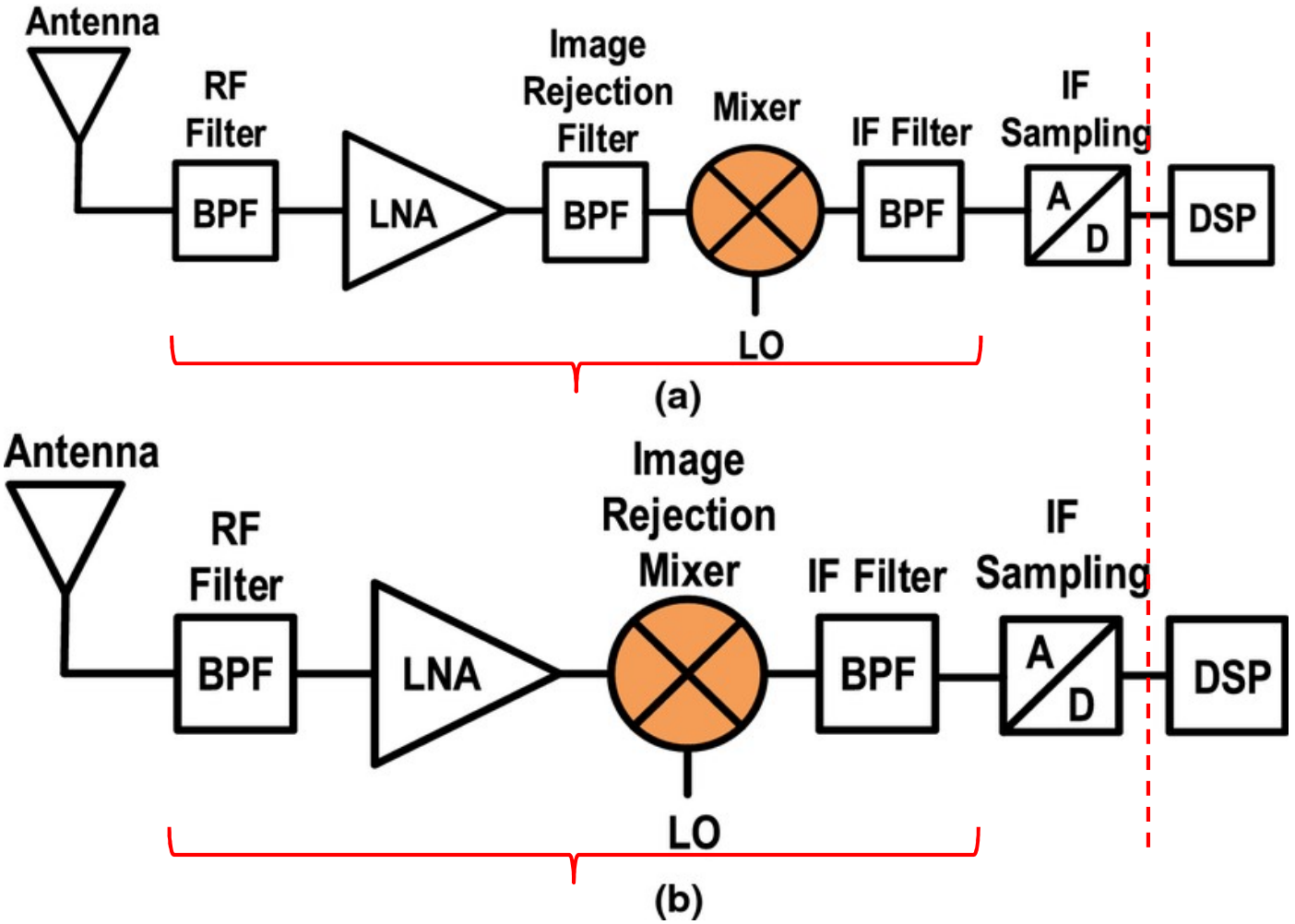
USB 3.0 (Serdes Applications)



USB3.0: 2.5Gbps
USB3.1: 5Gbps
USB3.1: 10Gbps
USB3.2: 20Gbps
USB4:

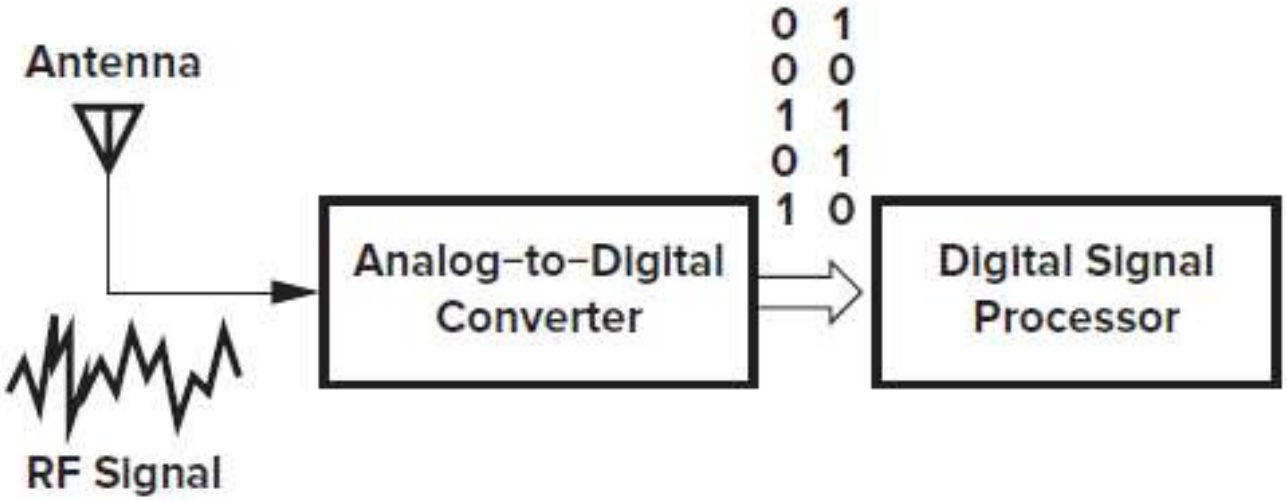
- Laptop 1 delivers the data to the cable in the form of a sequence of ONEs and ZEROs
- Since the cable attenuates high frequencies, we may design the equalizer to amplify such frequencies
- Serdes: Serializer and Deserializer (USB, PCIE, SATA, …)

Conventional RF Communication



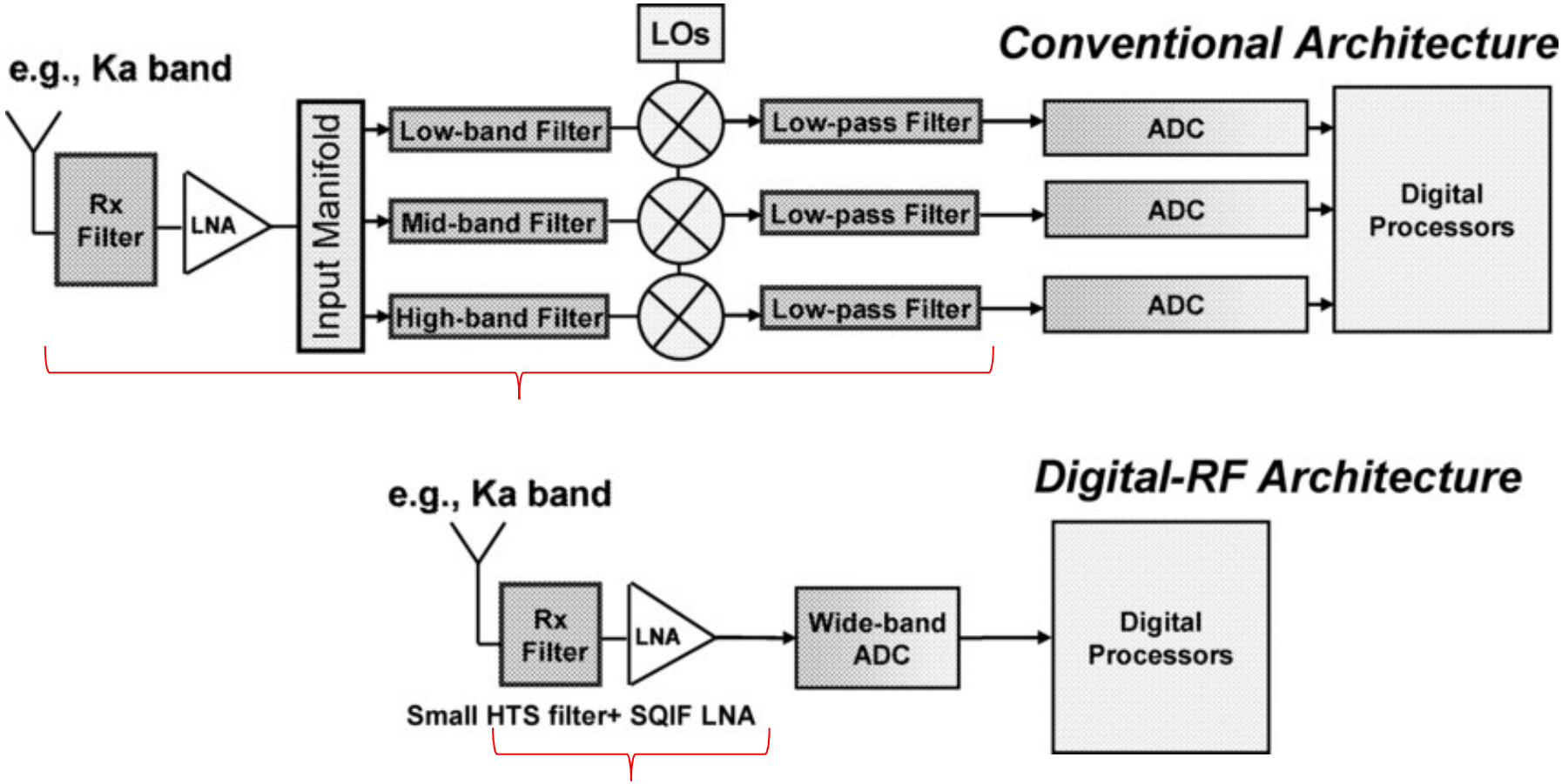
- May 2021, Circuits Systems and Signal Processing 40(7): 1-17
- DOI: 10.1007/s00034-020-01579-4

Advanced RF Receiver



- Direct RF Sampling to save more analog circuits (LNA, mixer, PLL, AAF, …) before ADCs
- As advanced CMOS technologies developed, ADC can be fast enough to directly sampling the RF signal (2.5GHz or higher)

RF Receiver Comparison



- March 2008, IEICE Transactions on Electronics 91-C(3):306-317
- DOI: 10.1093/ietele/e91-c.3.306