

Open Source GF180 Tapeout

Open Source Template Chip Frame For 2023 GF180 Chipathon

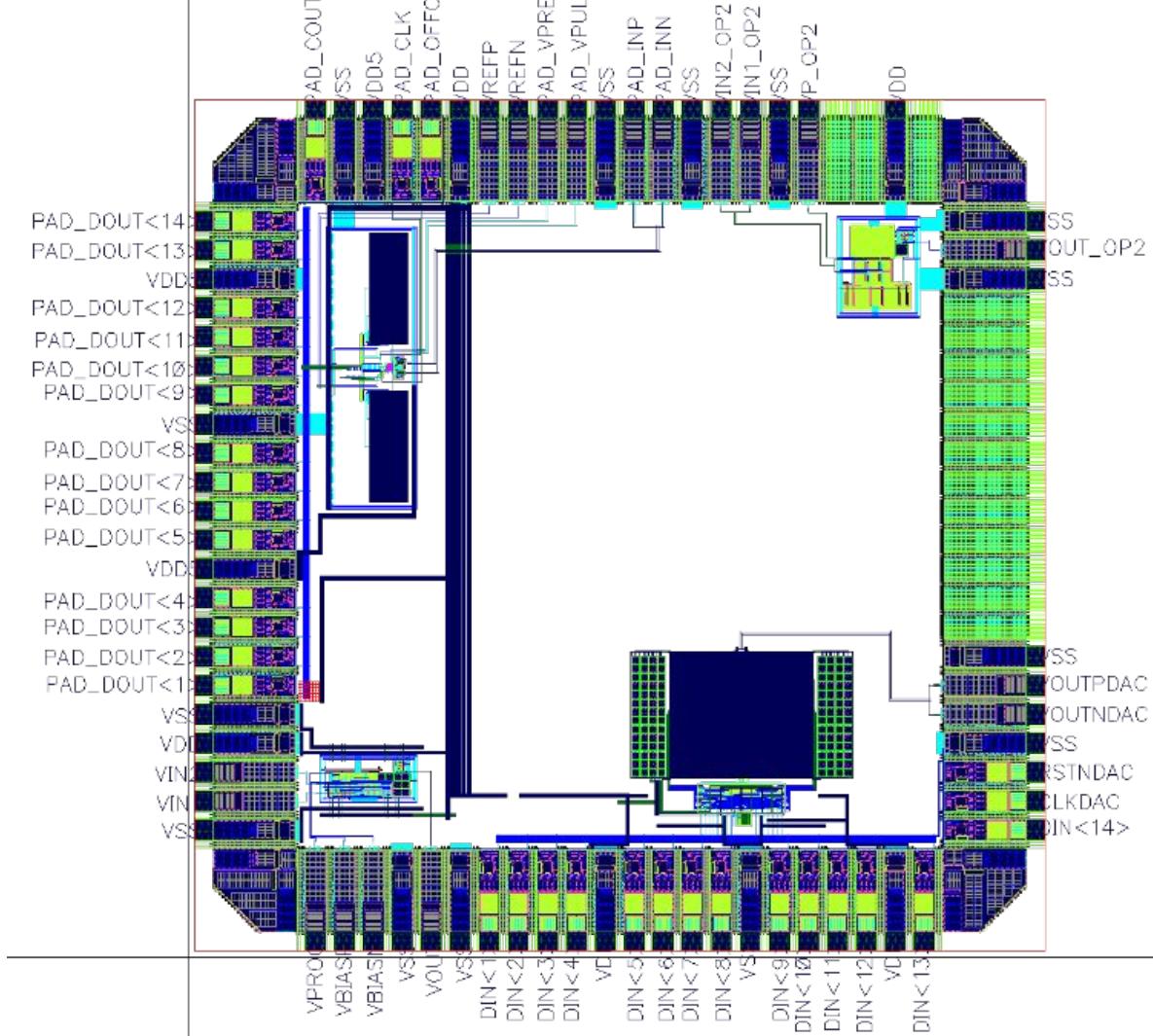
Overview

A chip designed for general-purpose sensor characterization.

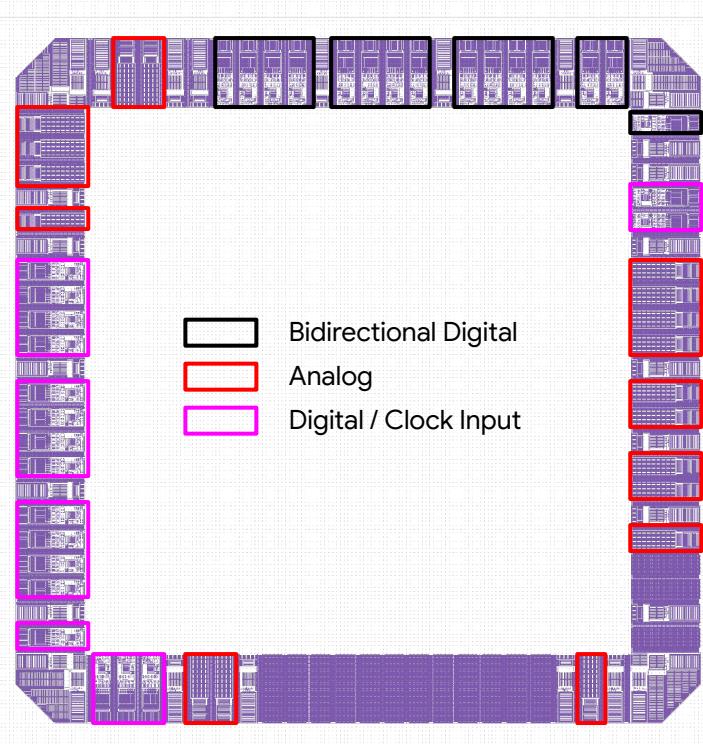
1x 15MSps 14bit ADC

1x 30MSps 13bit DAC

2x Low Noise OPAMPs



Overview



1 Power Domain

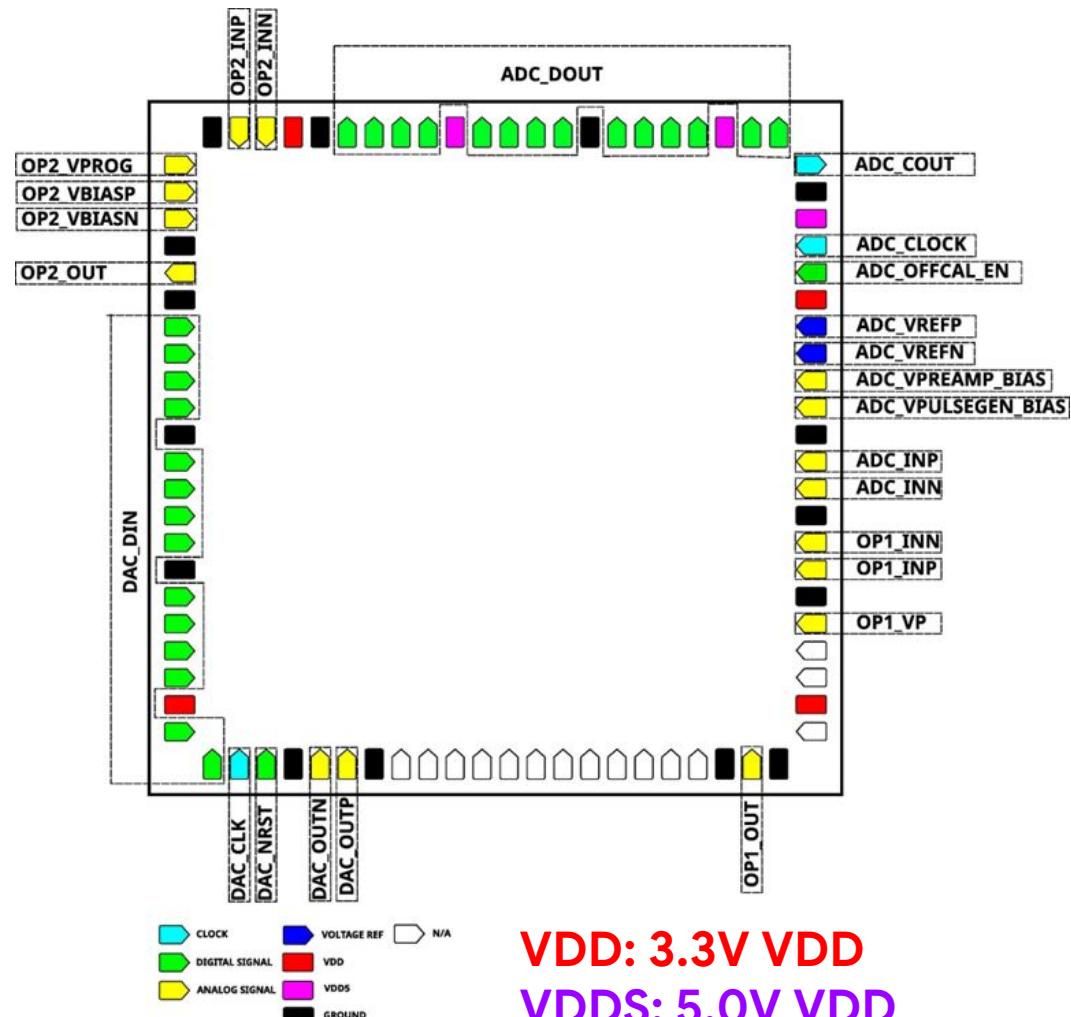
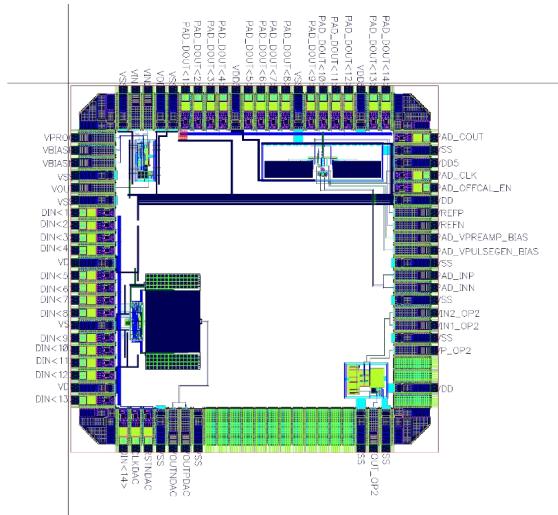
15 Bidirectional Digital GPIO (bi_t)

18 Analog IO (asig_5p0)

18 Digital Input (in_c)

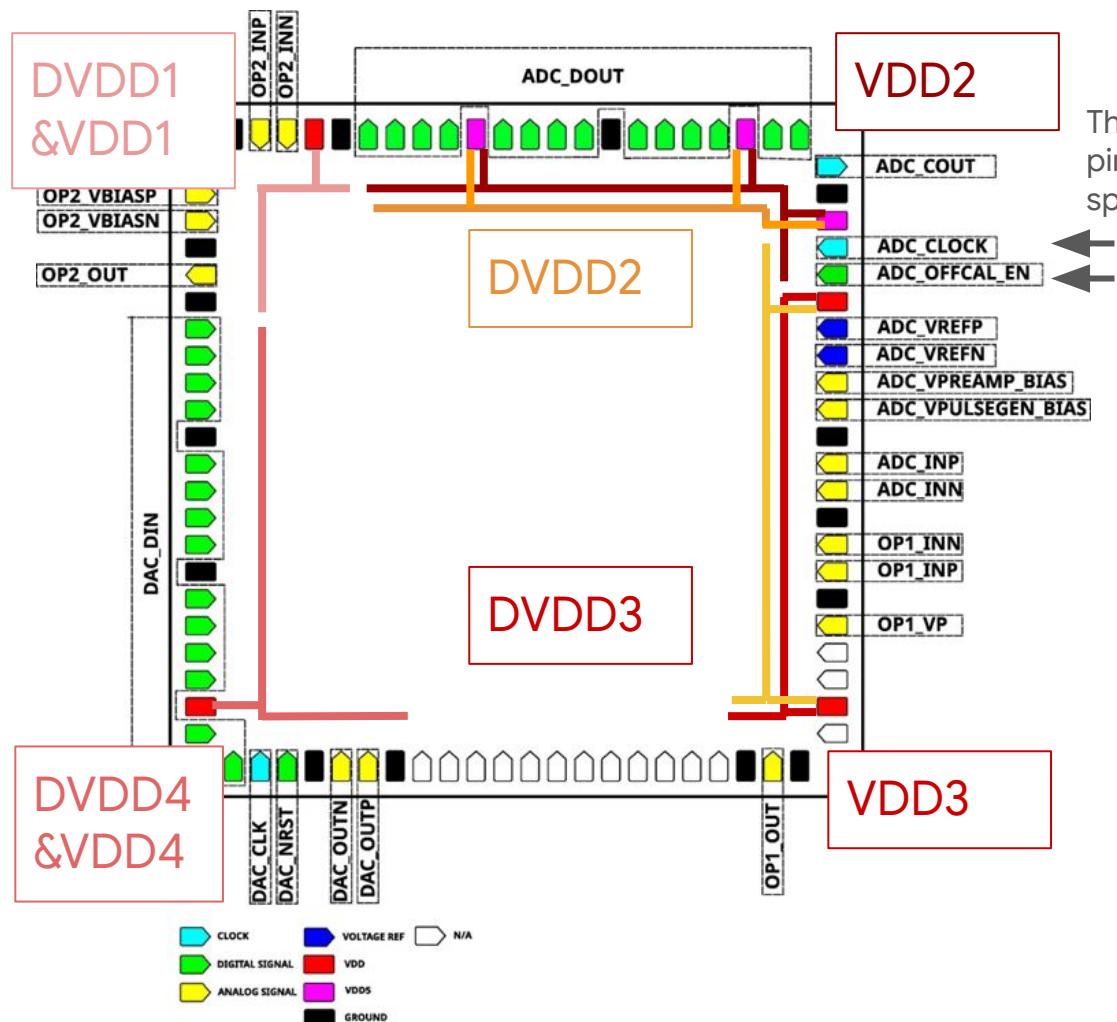
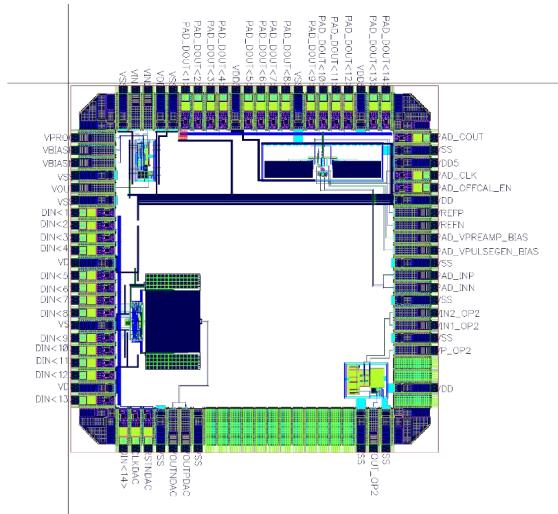
All IO cells are 5V capable

Overview



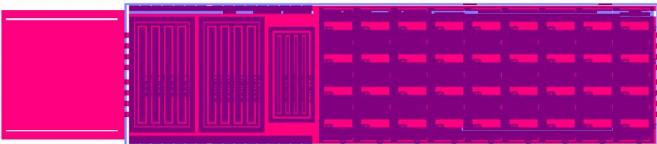
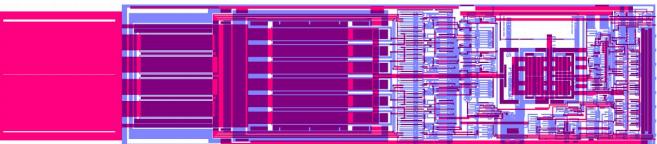
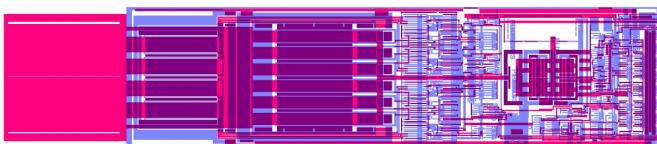
VDD: 3.3V VDD
VDDS: 5.0V VDD

Overview



Those IO
pins are
special

IO Cell Types



gf180mcu_fd_io.bi_t:

5V Bidirectional/Tristate IO pad with internal pull-up / down, programmable drive strength, Selectable Schmitt mode

gf180mcu_fd_io.in_c:

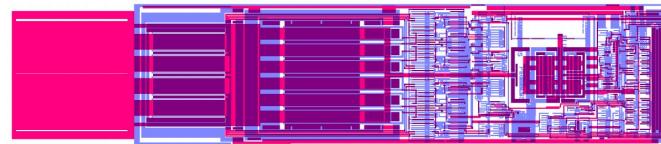
5V digital input only pad with internal pull-up / down

gf180mcu_fd_io.asig_5p0:

5V analog pad with double diode protection (DC current carrying capability 10mA)

Reference: https://gf180mcu-pdk.readthedocs.io/en/latest/IPs/IO/gf180mcu_fd_io/datasheet.html

gf180mcu_fd_io_bit

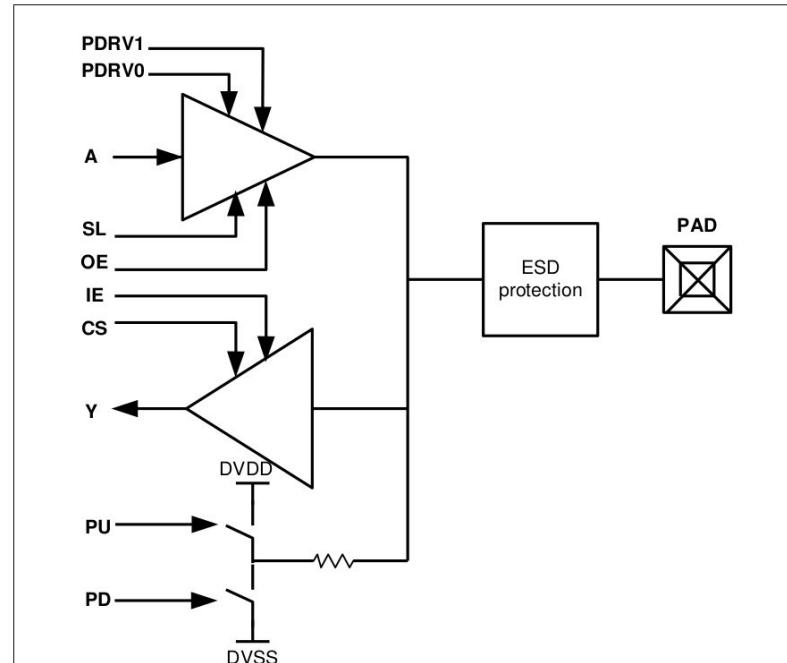


Driver Function

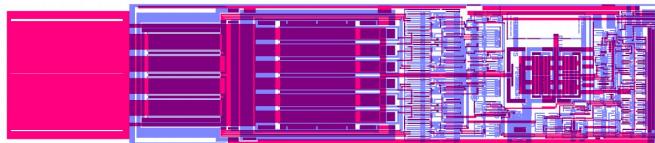
| Input | | | Output | |
|-------|----|----|--------|--------|
| OE | PU | PD | A | PAD |
| 0 | 0 | 0 | X | Hi-Z |
| 0 | 0 | 1 | X | weak 0 |
| 0 | 1 | 0 | X | weak 1 |
| 0 | 1 | 1 | X | Hi-Z |
| 1 | X | X | 0 | 0 |
| 1 | X | X | 1 | 1 |

Receiver Function

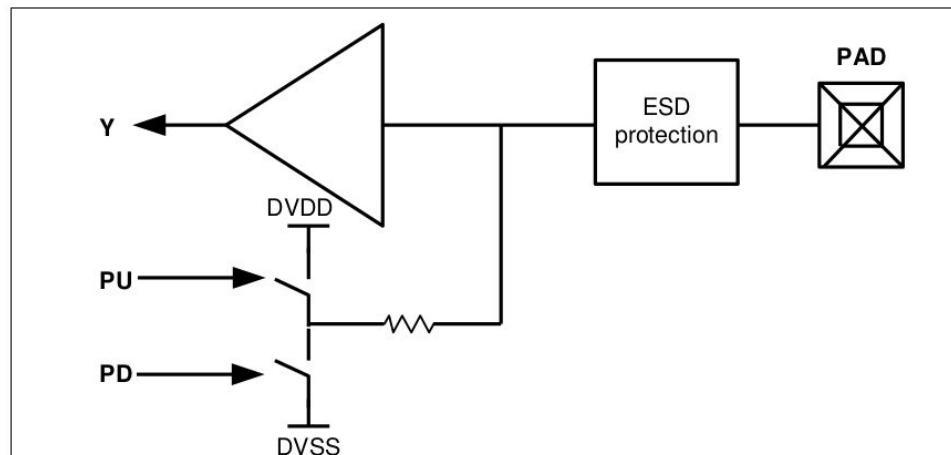
| Input | | | Output | |
|-------|----|----|--------|---|
| IE | PU | PD | PAD | Y |
| 0 | X | X | X | 0 |
| 1 | X | X | 0 | 0 |
| 1 | X | X | 1 | 1 |
| 1 | 0 | 1 | weak 0 | 0 |
| 1 | 1 | 0 | weak 1 | 1 |



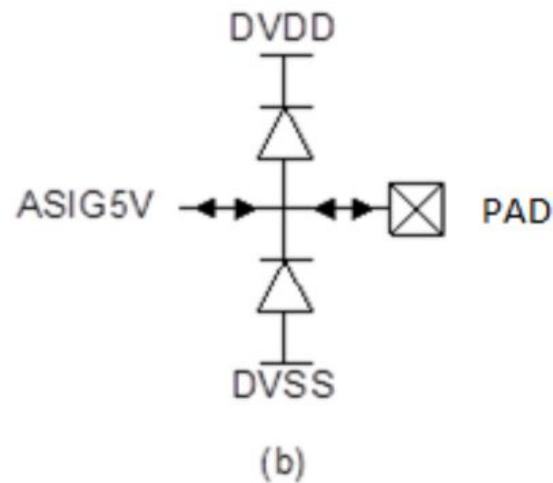
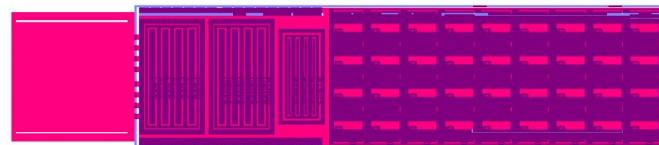
gf180mcu_fd_io_in_c



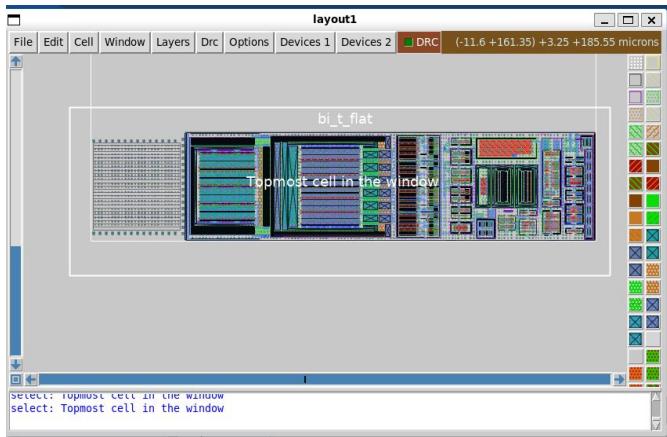
| Input | | | Output |
|-------|----|--------|--------|
| PU | PD | PAD | Y |
| X | X | 0 | 0 |
| X | X | 1 | 1 |
| 0 | 1 | weak 0 | 0 |
| 1 | 0 | weak 1 | 1 |



gf180mcu_fd_io_asig_5p0



Extracted Spice Simulation Support



s2

Instantiate DUT

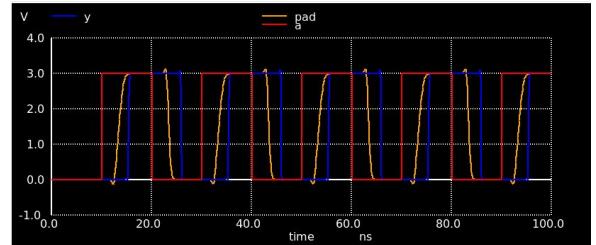
```
.include ../../mag/bi_t_flat.spice
XDUT vdd GND pad pu $l a y pdrv0 pdrv1 pd cs oe ie vddio GND bi_t_flat
```

Power Connections & Stimulus

Import GF180 Device Libraries

```
.include $::180MCU_MODELS/design.ngspice
.lib $::180MCU_MODELS/sm141064_ngspice_typical
.lib $::180MCU_MODELS/sm141064_ngspice_diode_typical
.lib $::180MCU_MODELS/sm141064_ngspice_res_typical
.lib $::180MCU_MODELS/sm141064_ngspice_mincap_typical
.lib $::180MCU_MODELS/sm141064_ngspice_moscap_typical

s1
.tran 10p 200n
.save all
.control
run
display
plot a y pad
.endc
```



List of Resources

Cell Detailed Description:

https://gf180mcu-pdk.readthedocs.io/en/latest/IPs/IO/gf180mcu_fd_io/

GDS, LEF, Netlist, Synthesis Library, Verilog Model :

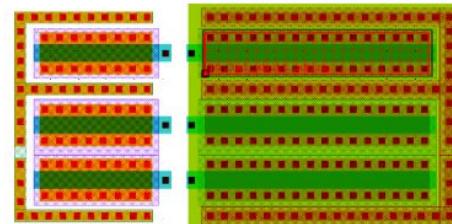
https://github.com/google/globalfoundries-pdk-libs-gf180mcu_fd_io/

Frame is available here:

<https://github.com/idea-fasoc/openfasoc-tapeouts>

Caution: IO Latch-up Rules

| Rules | DRC Description |
|--------------------|---|
| IO.1a1_xbutt_xRing | NCOMP in PSub directly connected to I/O pad must be surrounded by Psub tap inside the Psub without any PCOMP in NWELL in between |
| IO.1a2 | It should also be directly surrounded by an Nwell guard ring (Non broken NCOMP ring inside Nwell!). |
| IO.1b | Within 15um from the edge of the NCOMP connected to I/O pad (marked by Latchup_MK) |
| IO.3a1_xbutt_xRing | PCOMP in Nwell directly connected to I/O pad must be surrounded by Nwell tap inside the Nwell |
| IO.3a2 | It should also be directly surrounded by PCOMP guard ring outside NWELL. PCOMP guardring shall be connected to the lowest potential |
| IO.3b | Within 10um from the edge of the PCOMP connected to I/O Pad (marked by Latchup_MK) |



- [IO.3a1_xbutt_xRing] Observed PCOMP not completely surrounded by Nwell tap, potential leakage/current injection into substrate;
- Multiple IO violations may lead to latch-up risk;

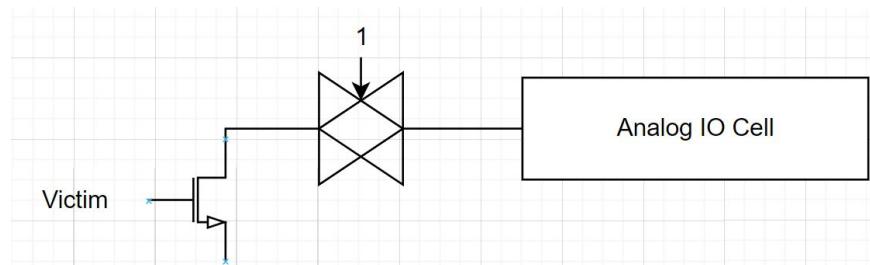
There're special rules that applies to the transistors directly exposed to the IO.

This check is not yet available in the open-source PDK release.

Caution: IO Latch-up Rules

A few ways to deal with this issue:

1. Do thorough chip-level DRC check using commercial tools before submitting for tapeout.
2. Add full guard rings for all transistors exposed to IO, and keep at least 15um distance between those transistors and other circuits.
3. Add a pass gate between those transistors and the IO pads. (Not recommended, but works as the last resort).



Compiling New Issues

We can use this platform to issues (we still have to file issues on tool owner's repos):

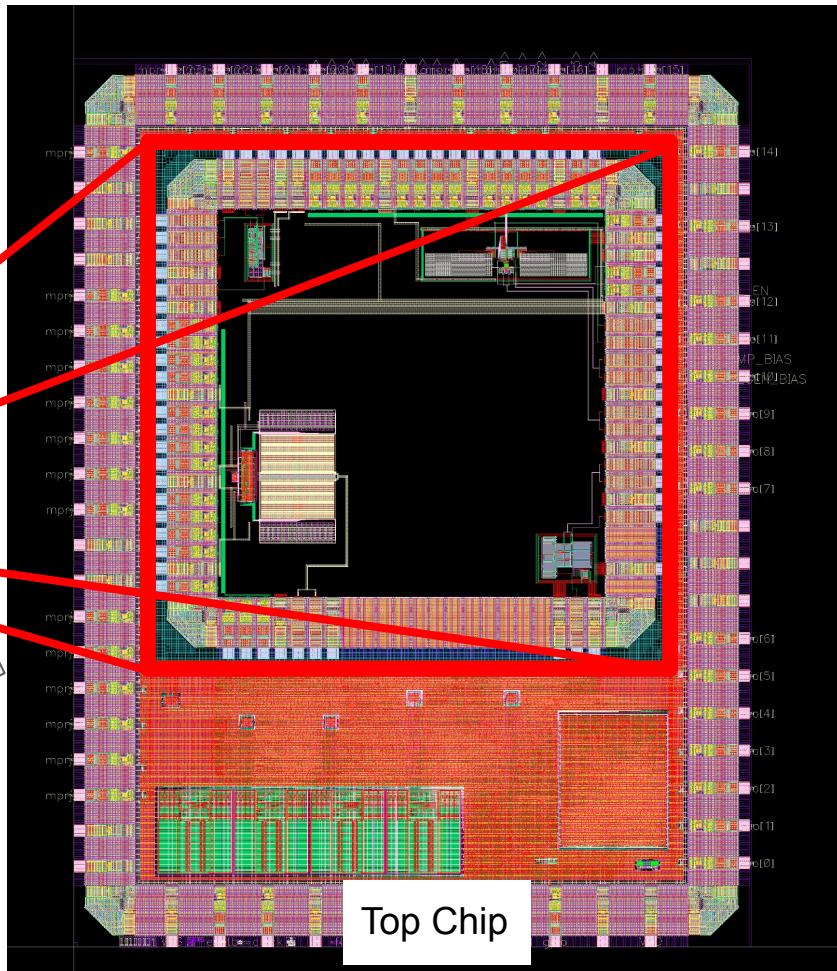
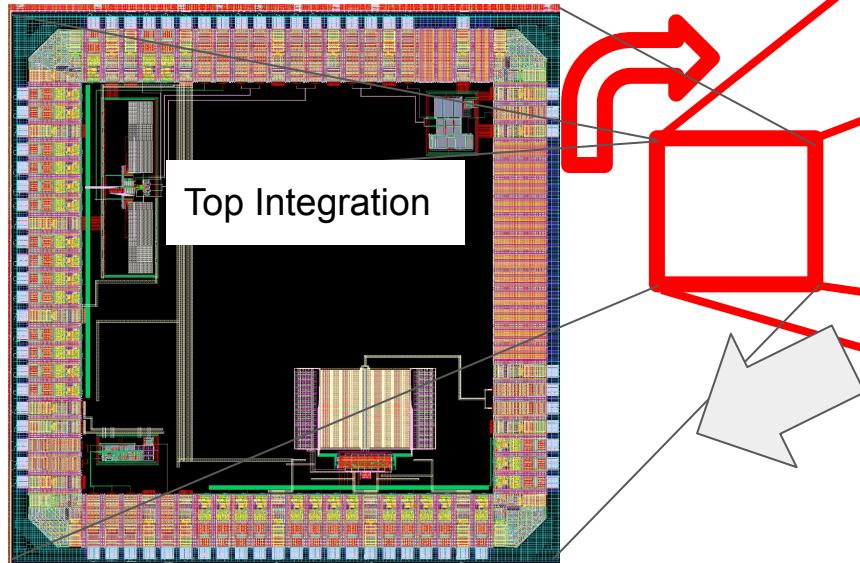
<https://github.com/orgs/idea-fasoc/projects/1/views/1>

Backup Slides

GF180 TO - PAD Name

Top Chip Caravel

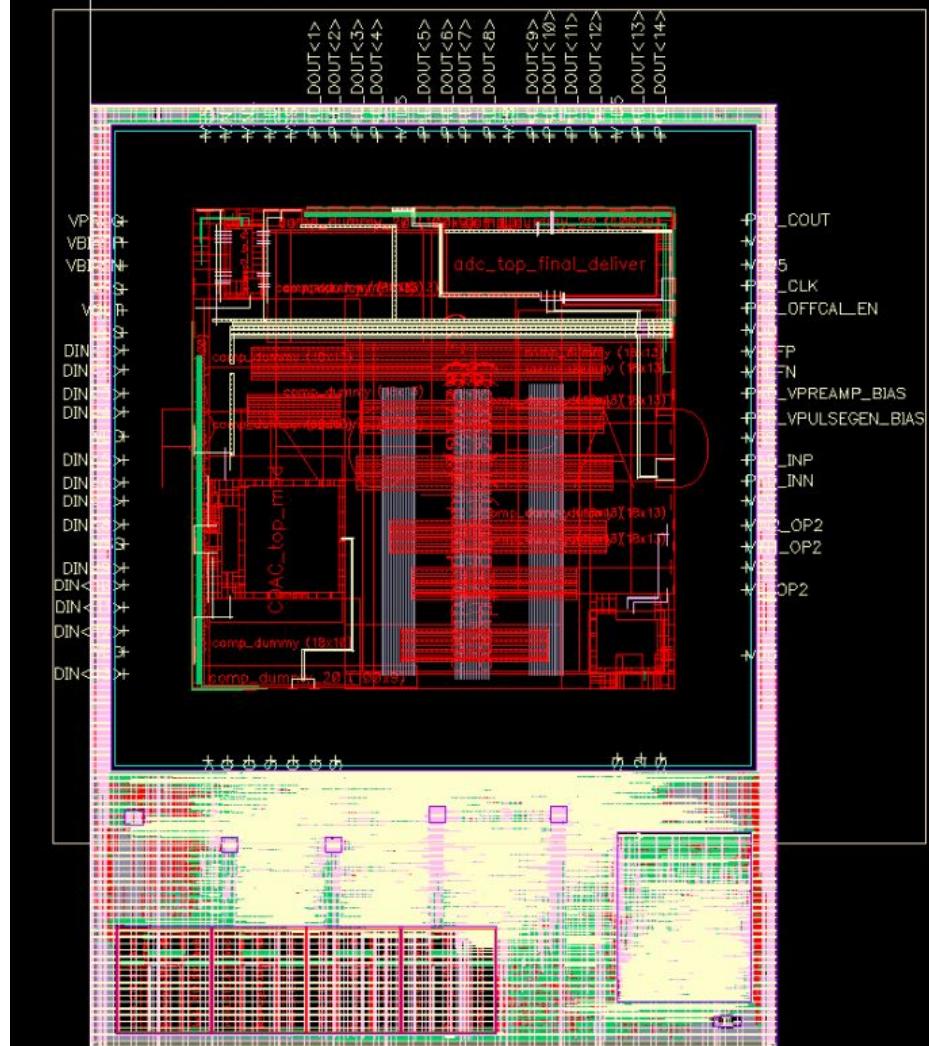
Top Integration is 90 degree CW
rotated from Top Chip



Size of the chip

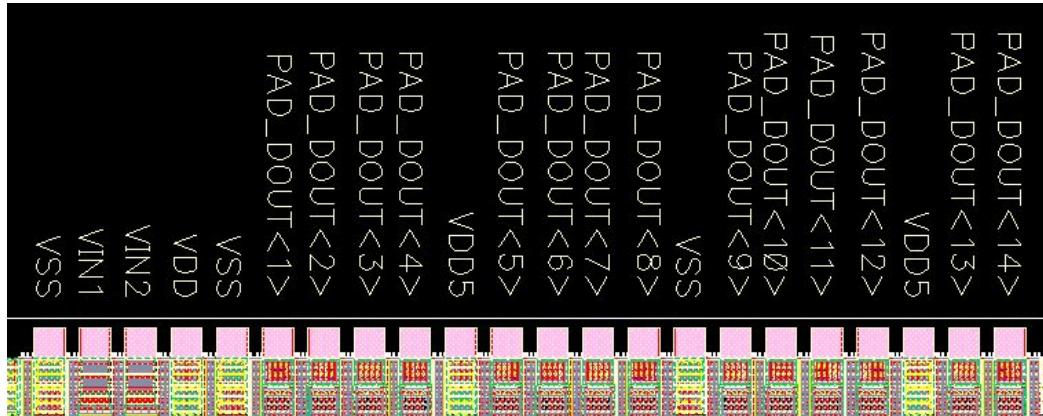
Total: 3890um x 5100um

Inside: 2935um x 2935um



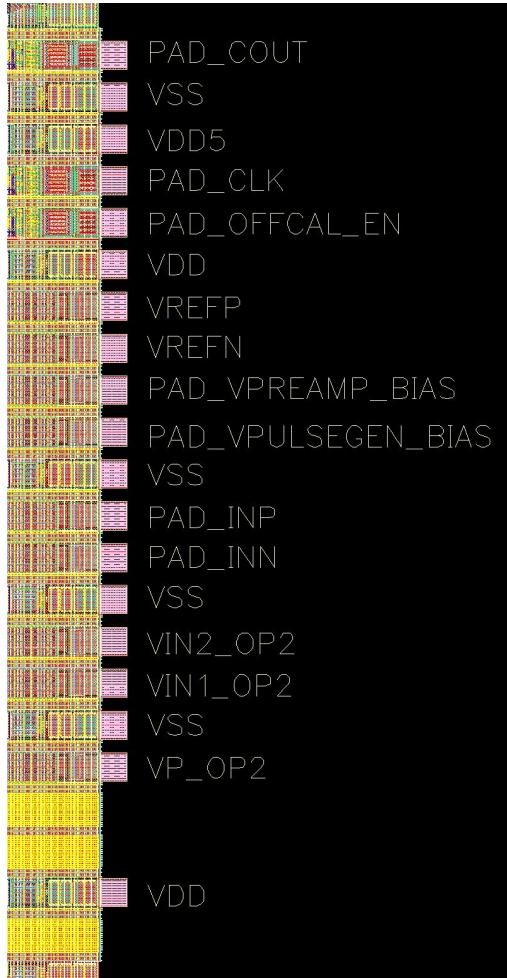
North Pad

22



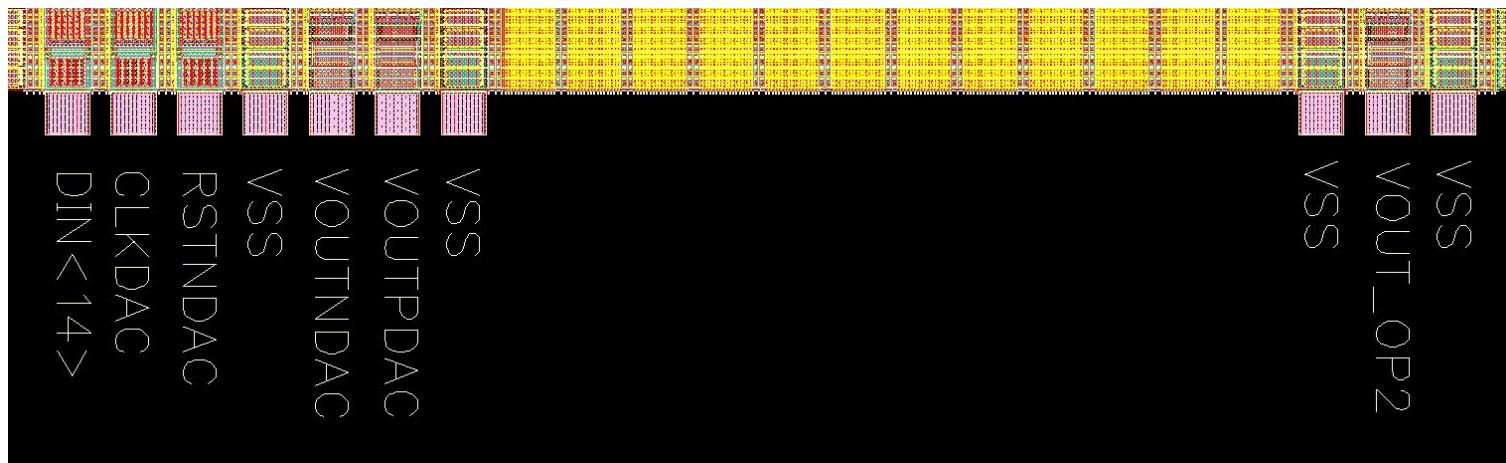
East Pad

19



South PAD

10



West Pad

22

