

# Landon Hering

7636004761 | 1108landon@gmail.com | Minnetonka, MN

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## Education

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**Massachusetts Institute of Technology | Cambridge, MA**  
**Computer Science and Engineering | 05/2028**

- 5.0/5.0 GPA

### *Prominent Coursework:*

- Discrete Mathematics for Computer Science
- Fundamentals of Programming
- Introduction to Algorithms
- Computation Structures

**Hopkins High School | Minnetonka, Minnesota**  
**05/2024**

- 4.0/4.0 GPA

### *Honors:*

- National Merit Finalist
- National Honor Society
- All State Cross Country and Track

### *Leadership Positions:*

- Captain of Cross Country team (led and organized practices over the summer for a group of around 30 boys)
- Captain of the Track Team (led and organized practices over the winter for a group of around 20 distance boys)
- Captain of the Math League (created mini-lectures to prepare teammates for the topics relevant to upcoming competitions)

**University of Minnesota Twin Cities | Minneapolis, MN**  
**05/2024**

- 4.0/4.0 GPA
- Dean's List: Fall 2023, Spring 2024

### *Prominent Coursework:*

- Introduction to Algorithms and Data Structures
- Machine Architecture and Organization
- Applied Linear Algebra
- Statistics for Engineers

## Work Experience

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**01/2025 - 06/2025:** Full time software development for research with the Tomas Palacios Group. Created full-stack applications like a QR code generator, QR code reader, and structured database to usefully encode position at microscopic scales on silicon wafers. Utilized a dynamic SQL-based database allowing sample images to be sorted and displayed according to the QR codes contained in the image.

**06/2025-08/2025:** Full time software developer for Evolve BGS, a start-up building a virtual power plant in Cape Town. Working primarily on creating tools to analyze our logger data from our Postgresql database, including noise reduction, fitting optimal solar curves, and organizing all the incoming data on the back end.

## Projects

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### **4-Stage Processor**

**03/2025 - 05/2025**

Created a 4 stage Risc-V fully pipelined processor described in minispec (a hardware description language). Processor was divided into fetch, decode, execute, and writeback stages with full bypassing from fetch and decode to writeback, along with

branch prediction (and annulment) and stall logic. This processor was later optimized for matrix multiplication thorough creation of a custom packmul instruction (multiply 4 8 bit numbers and add the sum) along with other smaller improvements.

### **Flask Project**

**08/2024**

Created a website that stored books and book reviews using a SQL database and the flask framework. Also, included different user logins and the ability to add new books into the system.

### **Malloc Implementation**

**04/2024**

Malloc implementation to correctly allocate and free memory from the heap using blocks storing the size, state, and next and previous block pointers for an arbitrary sized heap.