

# The Rule of Three: Triple Modular Redundancy

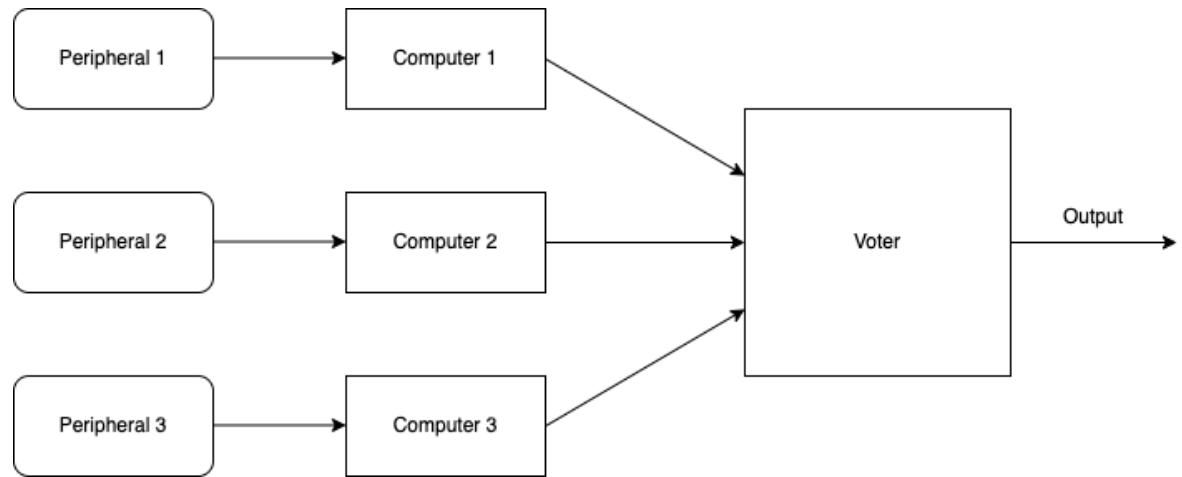
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# What is Triple Modular Redundancy?

Triple Modular Redundancy is a form of redundant computing where 3 computers run in parallel



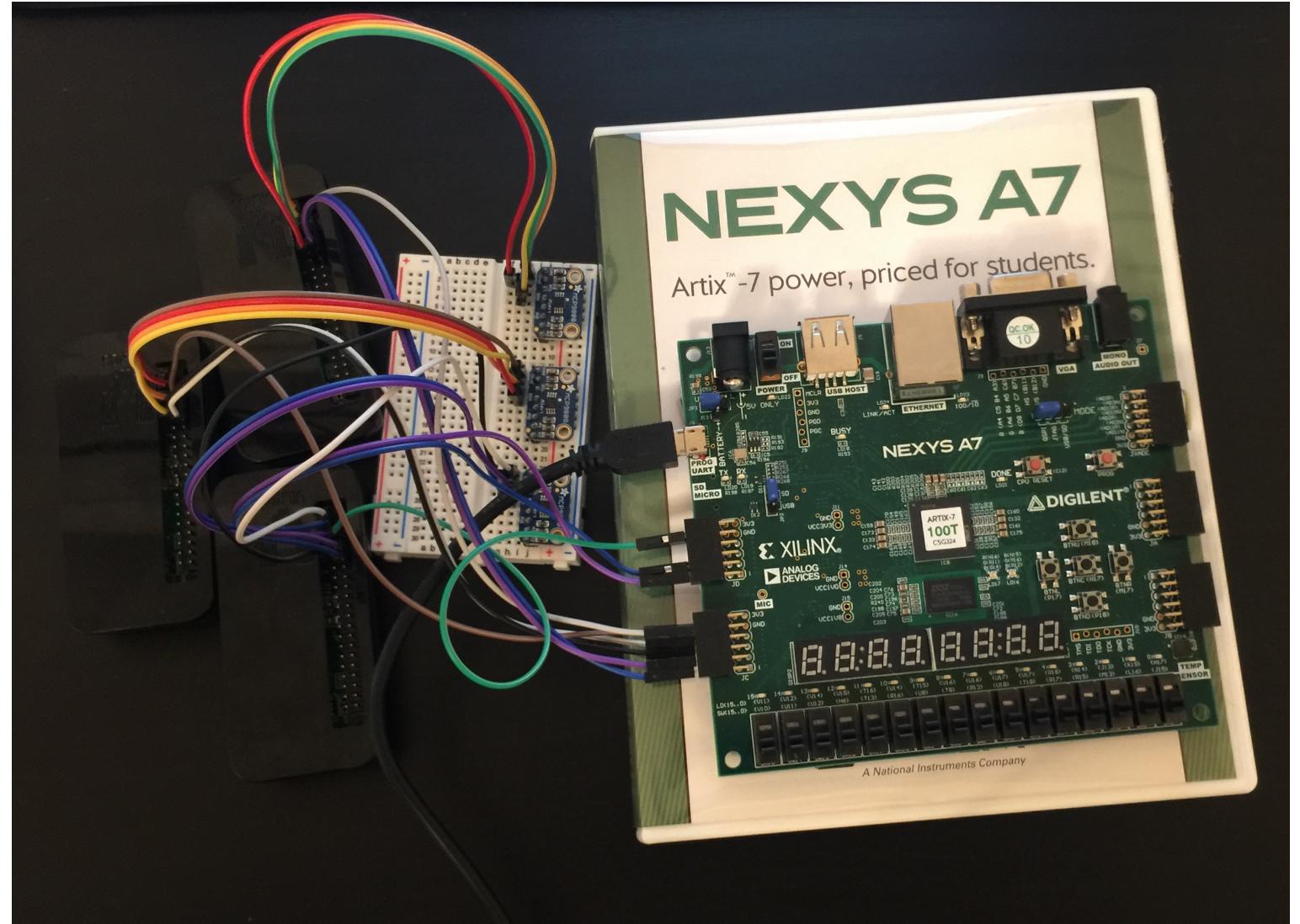
# Standard Design and Features of TMR

- All TMR Systems have a voting system, with an actuator or voter that checks the response from each of the computers and compares them
- The voter ignores an outlier (or performs majority vote), which in the case of a TMR is 2 out of 3 majority
- Most systems have error detection and masking (described above), and some even have error correction, where there may be software countermeasures to correct faults on a single computer
- Some systems also have synchronization and intercommunication across all components in the TMR system

# Our TMR System (Asynchronous Voter)

- Peripherals: 3 MCP9808 Temperature Sensors
- Computers: 3 Raspberry Pi Zeros
- Actuator: 1 Digilent Nexys Artix-7 FPGA Board
- Our TMR System computers send temperature data to the actuator every 0.5 seconds, so there was no need for synchronization
- The actuator will measure differences in all three reported temperatures and determine if one is an outlier

# Physical Layout



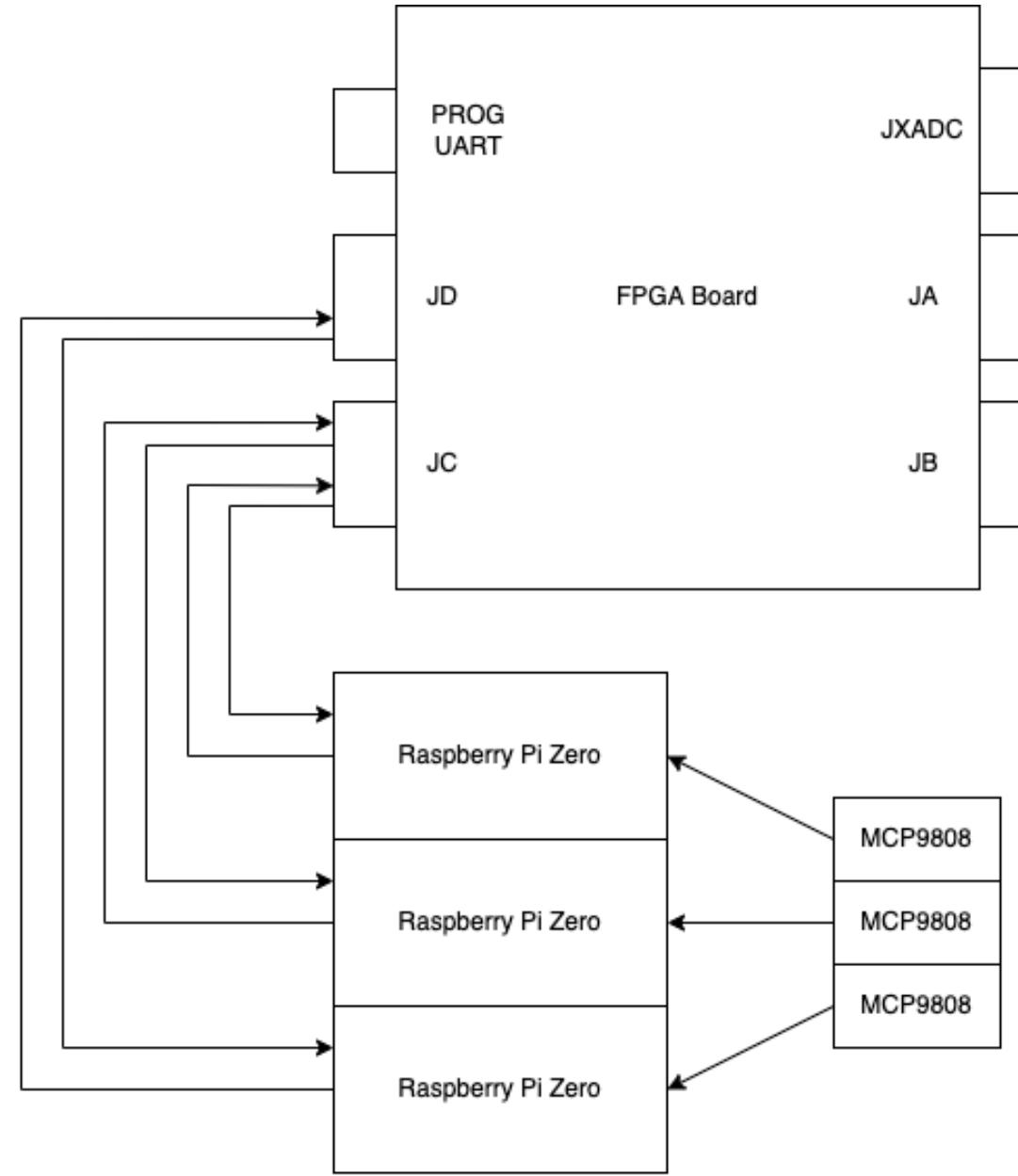
# Initial Challenges

- Initially, we tried to use a pure Verilog approach, only using hardware-description language to program the FPGA
- This wound up to be quite difficult because each time we made changes to the Verilog code, it would take a long time to reprogram the FPGA, making debugging a very costly task
- Later on, we found a very useful way to use the FPGA board as a microcontroller, from the book "FPGA Prototyping by SystemVerilog Examples" by Pong Chu, which made development a lot quicker

# MicroBlaze FPGA Microcontroller

- By using the FPGA board as a microcontroller, we get all the benefits of using microcontrollers and FPGA
- Microcontrollers are a lot easier and quicker to program
- FPGA boards have a high amount of versatile I/O, and we can still modify the hardware programming with SystemVerilog
- For the hardware, we just need to access UART over some pins in the PMOD ports
- While we have full control of every aspect of the hardware up through the software, we can primarily focus on the software now

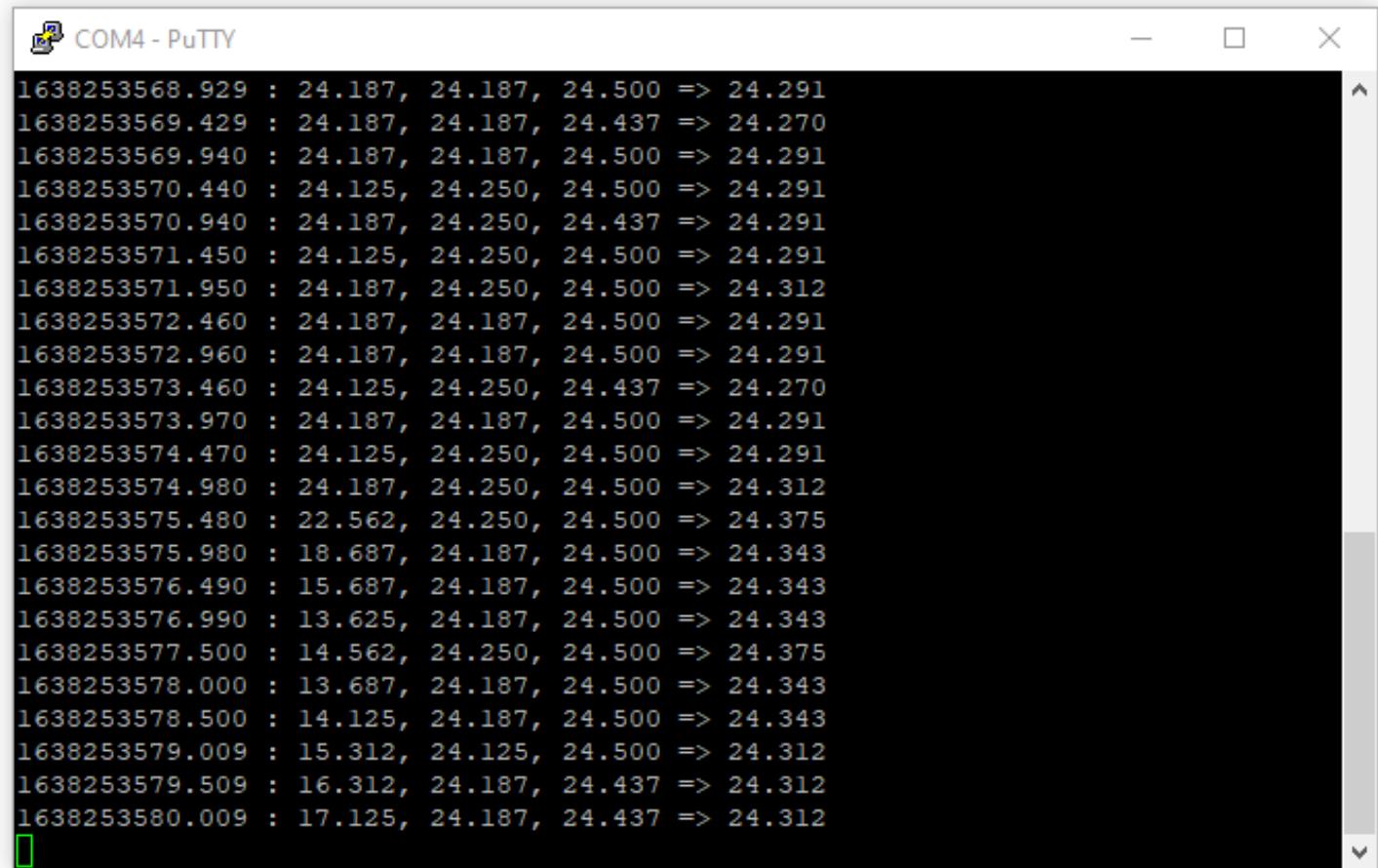
# Physical Layout



# TMR Software

- There are two software components of the TMR: the computers and the actuator
- Computer Software: each computer reads temperature from the MCP9808 Temperature Sensor and sends that data to the FPGA Board every 0.5 seconds
- Actuator Software: the FPGA board waits for input from all 3 computers, compares the input to see if there are outliers, and then displays the individual temperature from each computer, as well as the average temperature of the computers deemed to not be outliers

# Final Build



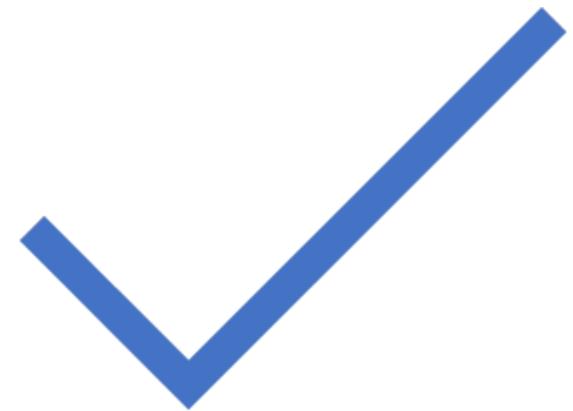
A screenshot of a PuTTY terminal window titled "COM4 - PuTTY". The window displays a list of 24 entries, each consisting of a timestamp followed by three numerical values and an assignment operator (=>) followed by another value. The entries are as follows:

```
1638253568.929 : 24.187, 24.187, 24.500 => 24.291
1638253569.429 : 24.187, 24.187, 24.437 => 24.270
1638253569.940 : 24.187, 24.187, 24.500 => 24.291
1638253570.440 : 24.125, 24.250, 24.500 => 24.291
1638253570.940 : 24.187, 24.250, 24.437 => 24.291
1638253571.450 : 24.125, 24.250, 24.500 => 24.291
1638253571.950 : 24.187, 24.250, 24.500 => 24.312
1638253572.460 : 24.187, 24.187, 24.500 => 24.291
1638253572.960 : 24.187, 24.187, 24.500 => 24.291
1638253573.460 : 24.125, 24.250, 24.437 => 24.270
1638253573.970 : 24.187, 24.187, 24.500 => 24.291
1638253574.470 : 24.125, 24.250, 24.500 => 24.291
1638253574.980 : 24.187, 24.250, 24.500 => 24.312
1638253575.480 : 22.562, 24.250, 24.500 => 24.375
1638253575.980 : 18.687, 24.187, 24.500 => 24.343
1638253576.490 : 15.687, 24.187, 24.500 => 24.343
1638253576.990 : 13.625, 24.187, 24.500 => 24.343
1638253577.500 : 14.562, 24.250, 24.500 => 24.375
1638253578.000 : 13.687, 24.187, 24.500 => 24.343
1638253578.500 : 14.125, 24.187, 24.500 => 24.343
1638253579.009 : 15.312, 24.125, 24.500 => 24.312
1638253579.509 : 16.312, 24.187, 24.437 => 24.312
1638253580.009 : 17.125, 24.187, 24.437 => 24.312
```

Current Time, T1, T2, T3, Voter

# Thank You

This concludes my presentation



# Demo

- I'll now show a live demo of the system in real-time operation
- Step 1: Run TMR Program on all computers
- Step 2: Show Normal Operation
- Step 3: Use Air Compressor on 1 or more Temperature Sensors
- Step 4: Show Majority Vote working as intended

# Work Cited

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P. Chu, *FPGA Prototyping by SystemVerilog Examples: Xilinx MicroBlaze MCS SoC*, New Jersey: Wiley, 2018.