FPL Demo: SERVE: Agile Hardware Development Platform with Cloud IDE and Cloud FPGAs

Zelin Wang, Ke Zhang, Yisong Chang, Yanlong Yin†, Yuxiao Chen,
Ran Zhao, Songyue Wang, Mingyu Chen, Yungang Bao
State Key Laboratory of Processor, ICT, CAS, Beijing, China
University of Chinese Academy of Sciences, Beijing, China
Email: {wangzelin20s, zhangke, changyisong, chenyuxiao20g, zhaoran, wangsongyue22s, cmy, baoyg}@ict.ac.cn
†yyin@bosc.ac.cn

***Abstract*—We introduce SERVE, a cloud platform for agile hardware software co-design, with cloud IDE and cloud FPGAs integrated. SERVE enables users to focus on logic designs, without facing the hassle of setting up FPGA tools and development environment. Users can write and simulate hardware logic in the cloud IDE and then generate bitstream files through a Continuous Integration (CI) pipeline. Finally, the bitstream files are deployed on an FPGA board. A great amount of testbenches will be executed to ensure the correctness of the hardware logic.**

We will demo a workflow of modifying a RISC-V processor and getting the design change quickly evaluated using SERVE.

I. Introduction

The importance of the capabilities for hardware and software co-design has emerged in recent years. Configuring development environment for HW/SW co-design can be frustrating for a beginner, and a solution to this problem is moving the whole hardware development process to the cloud, including coding, simulation, implementation, and on-FPGA evaluation of the design under test(DUT). To achieve this, we design and implement SERVE, an agile hardware development platform leveraging existing cloud FPGA hardware [1] and CI platform [2].

Figure 1 illustrates a typical flow of hardware development in SERVE. Each of these steps can be completed in web browsers on a normal laptop, requiring no extra environmental configuration. When a user completed hardware logic design in cloud IDE, he or she can push source files of the design to the project repository hosted in SERVE. After that, a series of CI processes for simulation and FPGA implementation will be launched automatically. If all CI processes are passed, a bitstream file will be generated and deployed in the cloud FPGA cluster. Finally, a large number of evaluation programs will be run for automatic examination and grading.

Figure 2 shows details of the cloud FPGA equipped in SERVE. We design our FPGA board based on Xilinx UltraScale+ ZU19EG MPSoC FPGA. Each FPGA has a shell design including five partial reconfiguration regions (PRR), each containing a 32-bit AXI4-lite slave interface for MMIO access from ARM and a 64-bit AXI4 master interface for access to dedicated 2GB of memory from the DUT. On each chassis that accommodates 32 such FPGA boards, SERVE can perform examination on 160 DUTs simultaneously.

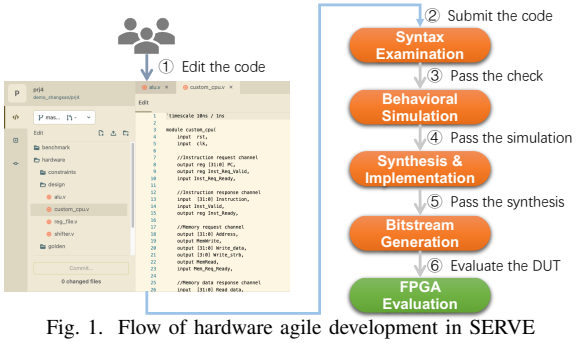

Fig. 1. Flow of hardware agile development in SERVE

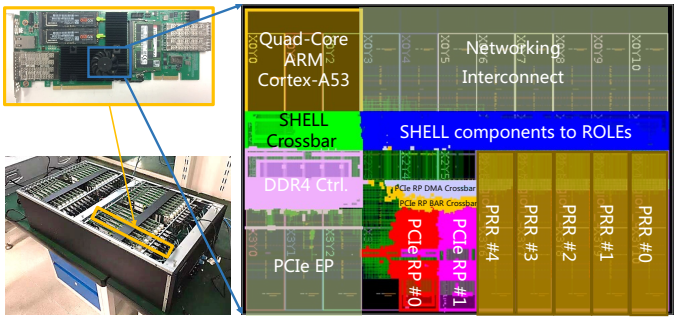

Fig. 2. The cloud FPGA behind SERVE

II. Demo-Setup

The demo includes scenarios for designing a basic RISC-V processor, as shown in Figure 1, including steps 1 through 6. The users can modify a five-stage pipelined RISC-V processor, submit the code change, run tests, and check test results. Extensive simulations and evaluations on SERVE platform will examine the correctness of the modified processor.

References

[1] K. Zhang, Y. Chang, M. Chen, Y. Bao, and Z. Xu, "Computer Organization and Design Course with FPGA Cloud," in *Proceedings of the 50th ACM Technical Symposium on Computer Science Education*, ser. SIGCSE '19. New York, NY, USA: Association for Computing Machinery, 2019, p. 927–933. [Online]. Available: https://doi.org/10.1145/3287324.3287475

[2] K. Zhang, Y. Chang, R. Zhao, Z. Wang, M. Chen, Y. Bao, and Z. Xu, "EdUCAS: An In-House CI/CD Platform with Cloud FPGAs for Agilely Conducting Computer Systems Course Projects," in *Proceedings of the 26th ACM Conference on Innovation and Technology in Computer Science Education V. 2*, ser. ITiCSE '21. New York, NY, USA: Association for Computing Machinery, 2021, p. 662. [Online]. Available: https://doi.org/10.1145/3456565.3460060