Lab/Assignment 2: Digital design for a given scenario (Patient ward display system).

Due Date 17th of February 2020 @ 3am

Objective:

- Design and test combinational logic design using the VHDL program.
- Design practice based on a specification.

Design Scenario and Specification

Eastern Health Rural Avalon (EHRA) plans to build and develop modern ward facilities to improve their services. Each floor in a hospital consists of 7 patients, wards nurses' room, and a doctor's room.

Improve the nursing services in the hospital; management decided to install a switch inside every ward. Therefore patients can use this switch to alert the nursing staff whenever service is required. In response, the patient will get a quick service.

You are recruited by the project team as an Electronic Engineer to develop this project using the digital system and solve this problem.

Specification

1. When the switch is pressed in the ward, the ward number should be displayed in the nurse's room display (7-segment display). If no button is pressed, the display remains off.
2. If more than one patient presses the switch at the same time, priority should be given for the first press.
3. Design must include only combinational logic devices, such as mux, de-mux, decoders, encoders etc.
4. The design must use FPGA/SoC and VHDL program to develop the system.

Task 1 (10 Marks)

Evaluate and describe the top-level functional block diagram for the above scenario. This should include and describe the **Combinational Logic Devices** that can be used in the design implementation.

Task 2 (30 Marks)

Develop a VHDL code for the complete scenario. You must use separate modules for each device described in Task 1.

Task 3 (20 Marks)

Write a test bench and test the design. You must provide a test bench and waveform.

Task 4 (40 Marks)

If a design specification required for 15 patient wards, what are the changes / modification that helps to full fill the requirement without redesign?

Provide the modified top-level functional block diagram.

Develop and test the modified system using the VHDL program.

Deliverable

1. Design functional block diagram
2. VHDL code
3. Test bench if required
4. Output waveform.