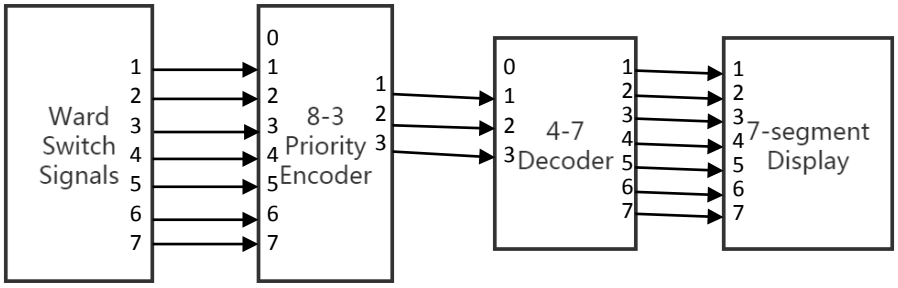
Assignment 2

Task 1

Block diagram



Task 2

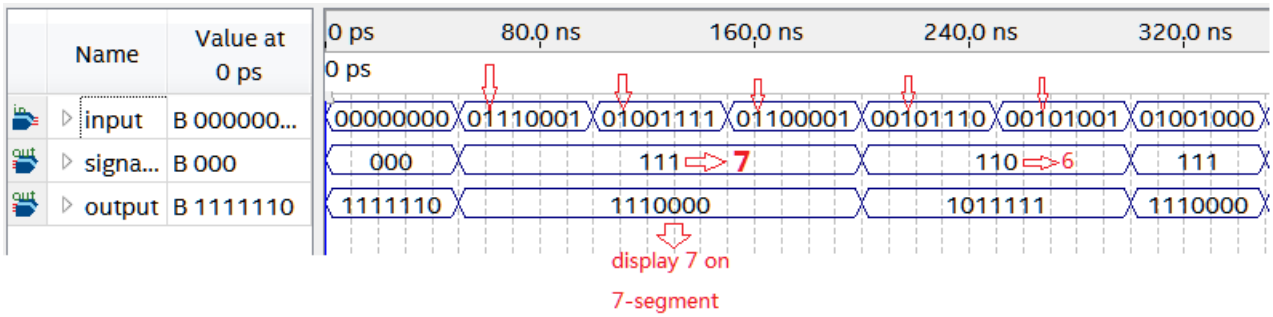
VHDL code

```
1   library ieee;
2   use ieee.std_logic_1164.all;
3
4   entity encoder_8_3 is
5      port (encoder_in:    in    std_logic_vector(7 downto 0);
6            encoder_out:   out   std_logic_vector(2 downto 0));
7   end encoder_8_3;
8
9   architecture design_encoder_8_3 of encoder_8_3 is
10  begin
11
12        encoder_out <= "000" when encoder_in(7) = '1' else
13                       "111" when encoder_in(6) = '1' else
14                       "110" when encoder_in(5) = '1' else
15                       "101" when encoder_in(4) = '1' else
16                       "100" when encoder_in(3) = '1' else
17                       "011" when encoder_in(2) = '1' else
18                       "010" when encoder_in(1) = '1' else
19                       "001" when encoder_in(0) = '1' else
20                       "000";
21
22  end design_encoder_8_3;
23
24  library ieee;
25  use ieee.std_logic_1164.all;
26
27  entity decoder_4_7 is
28     port (decoder_in:    in    std_logic_vector(3 downto 0);
29           decoder_out:   out   std_logic_vector(6 downto 0));
30  end decoder_4_7;
31
32  architecture design_decoder_4_7 of decoder_4_7 is
33  begin
34   with decoder_in select
35      decoder_out <= "1111110" when "0000",
36                     "0110000" when "0001",
37                     "1101101" when "0010",
38                     "1111001" when "0011",
39                     "0110011" when "0100",
40                     "1011011" when "0101",
41                     "1011111" when "0110",
42                     "1110000" when "0111",
43                     "1111111" when "1000",
44                     "1111011" when "1001",
45                     "0000000" when others;
46   end design_decoder_4_7;
47
48   library ieee;
49   use ieee.std_logic_1164.all;
50
```

```
50
51  entity ward_switch_7 is
52      port( input:   in    std_logic_vector(7 downto 0);
53            output:  out   std_logic_vector(6 downto 0);
54            signal_3: out  std_logic_vector(2 downto 0));
55  end ward_switch_7;
56
57  architecture design_ward of ward_switch_7 is
58
59  component encoder_8_3 is
60      port (encoder_in:    in    std_logic_vector(7 downto 0);
61            encoder_out:   out   std_logic_vector(2 downto 0));
62  end component;
63
64  component decoder_4_7 is
65      port (decoder_in:    in    std_logic_vector(3 downto 0);
66            decoder_out:   out   std_logic_vector(6 downto 0));
67  end component;
68
69  signal encoder_3  :  std_logic_vector(2 downto 0);
70
71  begin
72  encoder: encoder_8_3 port map (input, encoder_3);
73  decoder: decoder_4_7 port map ('0' & encoder_3, output);
74
75  signal_3 <= encoder_3;
76
77  end design_ward;
```

Task 3

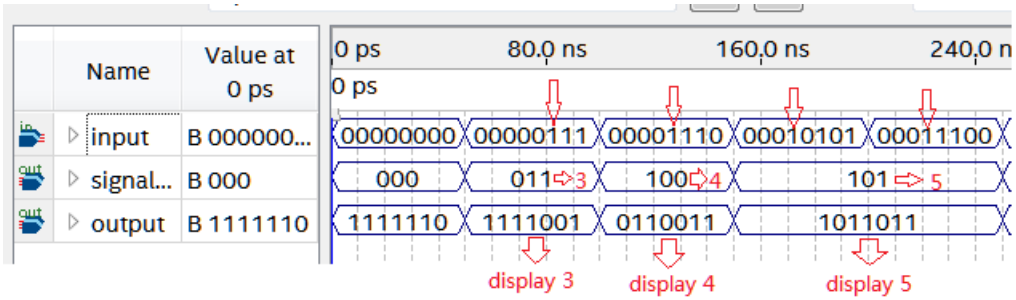
Test



As shown, “input” is an 8-bit signal that shows which wards have alerted. The most left bit represents ward number 1.

“signal” is a 3-bit signal produced by 8-3 encoder. It shows the priority number of wards.

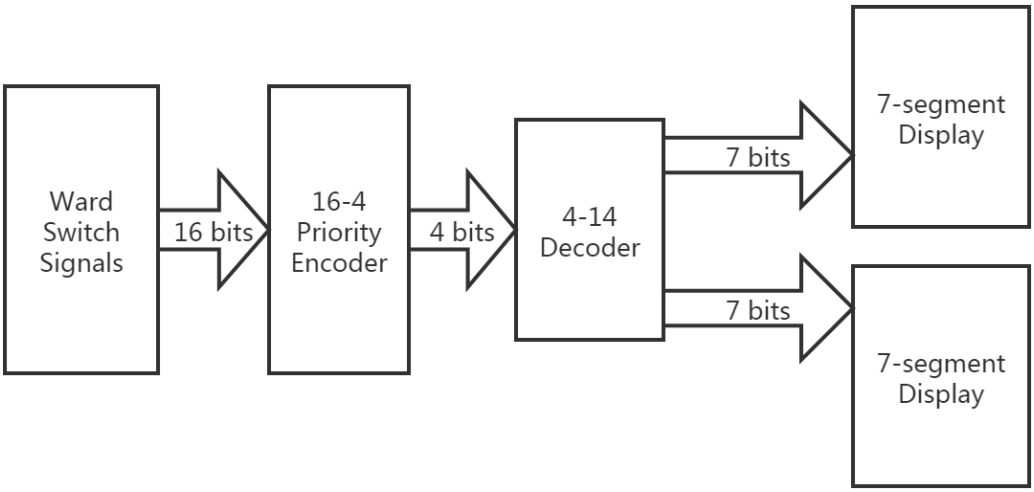
“output” is a 7-bit signal which can be sent to 7-segment display to show the corresponding number.



More test result.

Task 4

diagram



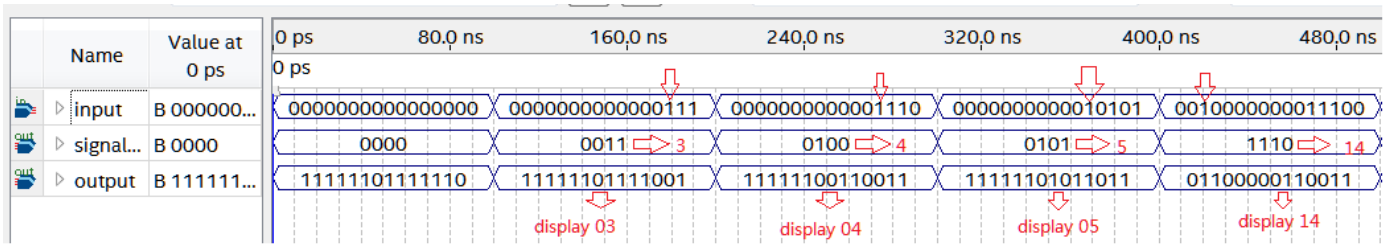
Code

```
1   library ieee;
2   use ieee.std_logic_1164.all;
3
4   entity encoder_16_4 is
5      port (encoder_in:    in    std_logic_vector(15 downto 0);
6            encoder_out:   out   std_logic_vector(3 downto 0));
7   end encoder_16_4;
8
9   architecture design_encoder_16_4 of encoder_16_4 is
10  begin
11
12        encoder_out <= "0000" when encoder_in(15) = '1' else
13                       "1111" when encoder_in(14) = '1' else
14                       "1110" when encoder_in(13) = '1' else
15                       "1101" when encoder_in(12) = '1' else
16                       "1100" when encoder_in(11) = '1' else
17                       "1011" when encoder_in(10) = '1' else
18                       "1010" when encoder_in(9) = '1' else
19                       "1001" when encoder_in(8) = '1' else
20                       "1000" when encoder_in(7) = '1' else
21                       "0111" when encoder_in(6) = '1' else
22                       "0110" when encoder_in(5) = '1' else
23                       "0101" when encoder_in(4) = '1' else
24                       "0100" when encoder_in(3) = '1' else
25                       "0011" when encoder_in(2) = '1' else
26                       "0010" when encoder_in(1) = '1' else
27                       "0001" when encoder_in(0) = '1' else
28                       "0000";
29
30  end design_encoder_16_4;
```

```
32  library ieee;
33  use ieee.std_logic_1164.all;
34
35  entity decoder_4_14 is
36     port (decoder_in:    in    std_logic_vector(3 downto 0);
37           decoder_out:   out   std_logic_vector(13 downto 0));
38  end decoder_4_14;
39
40  architecture design_decoder_4_14 of decoder_4_14 is
41  begin
42  with decoder_in select
43     decoder_out <= "11111101111110" when "0000",
44                    "11111100110000" when "0001",
45                    "11111101101101" when "0010",
46                    "11111101111001" when "0011",
47                    "11111100110011" when "0100",
48                    "11111101011011" when "0101",
49                    "11111101011111" when "0110",
50                    "11111101110000" when "0111",
51                    "11111101111111" when "1000",
52                    "11111101111011" when "1001",
53
54                    "01100001111110" when "1010",
55                    "01100000110000" when "1011",
56                    "01100001101101" when "1100",
57                    "01100001111001" when "1101",
58                    "01100000110011" when "1110",
59                    "01100001011011" when "1111",
60
61                    "00000000000000" when others;
62  end design_decoder_4_14;
```

```
64  library ieee;
65  use ieee.std_logic_1164.all;
66
67  entity ward_switch_15 is
68     port( input:   in    std_logic_vector(15 downto 0);
69           output:  out   std_logic_vector(13 downto 0);
70           signal_4: out  std_logic_vector(3 downto 0));
71  end ward_switch_15;
72
73  architecture design_ward of ward_switch_15 is
74
75  component encoder_16_4 is
76     port (encoder_in:    in    std_logic_vector(15 downto 0);
77           encoder_out:   out   std_logic_vector(3 downto 0));
78  end component;
79
80  component decoder_4_14 is
81     port (decoder_in:    in    std_logic_vector(3 downto 0);
82           decoder_out:   out   std_logic_vector(13 downto 0));
83  end component;
84
85  signal encoder_4  :  std_logic_vector(3 downto 0);
86
87  begin
88  encoder: encoder_16_4 port map (input, encoder_4);
89  decoder: decoder_4_14 port map (encoder_4, output);
90
91  signal_4 <= encoder_4;
92
93  end design_ward;
```

Test



As shown, “input” is an 16-bit signal that shows which wards have alerted. The most left bit represents ward number 1.

“signal” is a 4-bit signal produced by 16-4 encoder. It shows the priority number of wards.

“output” is a 14-bit signal which can be separate to two 7-bits parts and be sent to two 7-segment displays to show the corresponding number.