ENGI 9865 Advanced Digital Design

Lab/Assignment 4: Digital design for a given scenario (RTMD).

Due Date 3rd of April 2020 @ 3am

Contribute 10% of final grading

Aim of the assignment

Design, simulation and implementation of a Remote Temperature Monitoring Device (RTMD).

Objectives:

- To make use of the Altera/Modelsim development system to create a working FPGA based design.
- To create an Algorithmic State Machine (ASM) diagram, describing the behaviour of the design.
- To create register transfer level (RTL) design descriptions (based upon the ASM diagram) of the main controller and associated blocks.
- To create a top level description (HDL) of the complete design, including an existing bit-serial transmitter module. (complete in the class laboratory)
- To verify correct operation of the system using functional simulation, fully documenting the results.
- To perform logic synthesis and implementation of the RTL design description, targeting a FPGA.
- To document, in detail, the work carried out toward meeting the objectives.

Software Resources:

- Quarts II Development software or Modelsim.

Design specification of the RTMD

Figure 1 shows the block diagram of the RTMD. The design comprises a number of functional blocks, initially student must design following modules for serial transmission and timer (you may follow the lecture notes).

- TySysRTL – bit serial data transmitter.
- Timer – generates a continues steam of trigger pulses at time interval determined by a parameter. Each pulse lasts for one clock cycle.

One new block is required to complete RTMD system,

- RTMD_Controller – the main control block of the system, this module response to the pulses out from the timer module. At each time pulse (input on 'Trigger') the controller module reads the temperature sensor and activates the alarm if the rate of change or level exceeds the limits set by the user via input switches. The temperature, along with an identity number, is also transmitted to a base station via the serial transmitter.

RTMD inputs and outputs

At the top level of the system has the following ports,

- RST – Achieve high asynchronous reset.
- CLK – 32768 Hz crystal clock (will be change based on selected FPGA)
- Temp[7:0] – 8 bit temperature value supplied from a transducer continuously measuring ambient temperature. Supplies an unsigned output calibrated directly in degree Celsius. (0^oC to 255^oC).
- DetNo[7:0] – Supplied from 8bit DIP switch, this input represent the identity number or address of the RTMD. Given the possibility to having several RTMDs in a building, each one must have a unique 'detect number'.
- MaxRate[7..0] – An 8 bit value supplied from DIP switches specifying the maximum allowed rate of change of the measured in ^oC/second.
- RstAlarm – The RstAlarm input clears the alarm output until the next temperature measurement.
- TxData – Asynchronous Serial Data output at a rate of approximately 1800 bits-per-second. Format is 8 data bits, 1 stop bit and single bit odd parity.

- Alarm – The Alarm output is set to logic 1 when the measured temperature exceeds the limit set by the ‘MaxTemp’ input and/or the rate of rise of the measured temperature exceeds the limit set by the ‘MaxRate’.

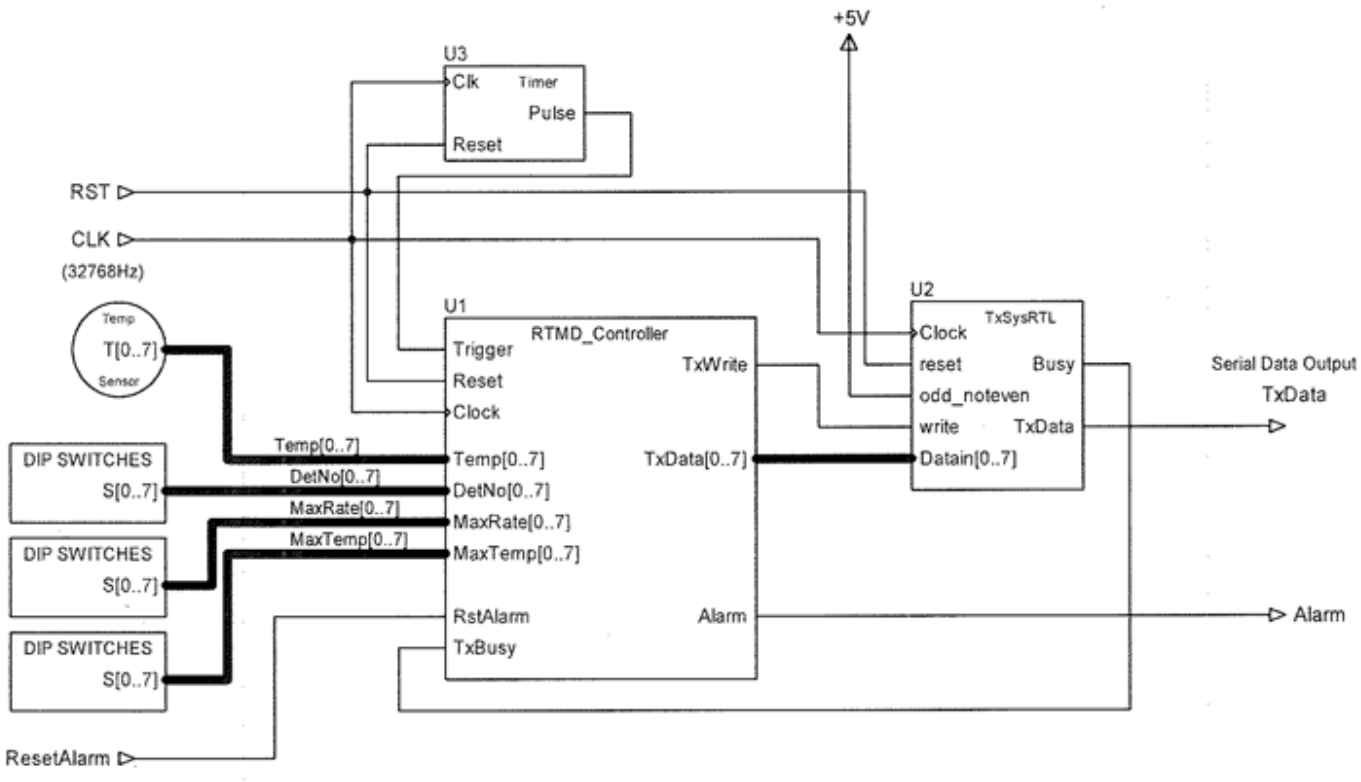

Figure 1 : FPGA Based Remote temperature monitoring device

The RTMD system is to operate as follows:

Following a reset, the system enters an initial state where the alarm output is inactive and the serial data output is set to logic 1. The timer block will start to output pulses at intervals set by the timer parameter (for example 5 seconds, however for simulation purpose timer interval can be reduced). When the controller receives a trigger pulse it responds by reading the input value from the temperature sensor.

Assuming the measured temperature is within acceptable limits, the controller then transmits two characters, using the serial format specified above, detector number followed immediately by temperature value to base station via a wireless radio link connected to the TxData output of the serial transmitter (note that the wireless radio link and the base station are not part of this assignment). Having sent the message, the RTMD then returns to an initial state until the next pulse is received from the timer, and the above ‘measure/transmit’ process is repeated.

If the measured temperature value exceeds either, or both, of the maximum rate of change or level settings, the following is to take place. The controller goes into an alarm state and activates

the alarm output, while simultaneously transmitting a fixed ‘alarm character’ of <8’hF0>. The serial transmission of the alarm character is to be repeated contiguously (stop bit followed immediately by start bit of next character), until the ‘RstAlarm’ input is asserted. Note that each transmission is begin with the detector number character.

Once the ‘RstAlarm’ input is asserted, the controller is to return to the initial state, reset the alarm output and wait for the next timer pulse.

Student Activity

To develop the above given system, student has to follow the guidelines below,

Source creation and functional simulation of the RTMD

1. Create individual ASM diagram and VHDL modules for the RTMD controller block. Prior to incorporating the blocks into the RTMD system, perform individual simulations to verify correct operation. Document and comment all the result.

2. Using HDL language, crate a design module for the complete RTMD system described in figure 1.

3. Crete a test module for the RTMD system. Design the test module so that the simulation clearly shows the response of the system to changing temperature measurements. Include test values to demonstrate normal measurement and alarm conditions. Document and comment all the results.

Deliverables

The following list indicates what must be included in the assignment report.

1. Design method

   Block and schematics diagrams, ASM diagrams and logics diagrams where appropriate, along with brief textual descriptions fully explaining how your design implements the required functionality of the RTMD.

   [4 Marks]

2. VHDL Source Develop and Describe

   Listing all VHDL source descriptions, correctly indented with reserved words **boldface** font (use an appropriate font such as MS reference Sans Serif or Courier New). The sources should be adequately commented (comment in italics) and each module should be preceded by a header comment containing basic information about the design, such as the student name and ID number, date of the creation etc.

   [6 Marks]

3. Module test

Printouts or screen dumps showing simulation waveforms for individual modules were appropriate. These should be annotated with notes and comments clearly indicating how the waveform show correct operation.

[4 Marks]

4. System test

Printouts or screen dumps of simulation waveforms for the top-level test-bench for the RTMD, these should also be annotated with notes and comments and measurements clearly indicated how the waveforms show correct operation of the overall system.

[6 Marks]