Job Posting:165694 - Position: S25 Digital Design Verification Engineering Intern 165694

Co-op Work Term Posted:	2025 - Summer
App Deadline	02/05/2025 09:00 AM
Application Method:	Through Employer Website
Posting Goes Live:	01/16/2025 04:06 PM
Job Posting Status:	Expired

ORGANIZATION INFORMATION

Organization	Synopsys
Country	Canada

JOB POSTING INFORMATION

Placement Term	2025 - Summer
<b> Job Title <b>	S25 Digital Design Verification Engineering Intern 165694
Position Type	Co-op Position
Job Location	Mississauga, ON
Country	Canada
Duration	16 months
Salary Currency	CAD
Salary	Salary Not Available, 0 Major List

Job Description

Job Title: Digital Design Verification Engineering Intern

Job ID: 4674

We Are: Drive technology innovations that shape the way we live and connect. Our technology drives the Era of Pervasive Intelligence, where smart tech and AI are seamlessly woven into daily life. From self-driving cars and health-monitoring smartwatches to renewable energy systems that efficiently distribute clean power, Synopsys creates high-performance silicon chips that help build a healthier, safer, and more sustainable world.

At Synopsys, interns dive into real-world projects, gaining hands-on experience while collaborating with our passionate teams worldwide-and having fun in the process! You'll have the freedom to share your ideas, unleash your creativity, and explore your interests. This is your opportunity to bring your solutions to life and work with cutting-edge technology that shapes not only the future of innovation but also your own career path. Join us and start shaping your future today!

Our mission is to fuel today's innovations and spark tomorrow's creativity. Together, we embrace a growth mindset, empower one another, and collaborate to achieve our shared goals. Every day, we live by our values of Integrity, Excellence, Leadership, and Passion, fostering an inclusive culture where everyone can thrive-both at work and beyond.

What You'll Be Doing:

• Defining and tracking Verification Testplans
•Designing and writing constrained-random SystemVerilog testbenches using a Verification Methodology such as UVM (Universal Verification Methodology)
•Creating and examining Functional Coverage
•Writing SystemVerilog assertions
•Debugging RTL and gate-level simulation failures
•Firmware Debug
•Bug Tracking using Software Tools such as Jira
•Code Coverage Analysis

Job Requirements

What You'll Need:

• Experience writing scripts in languages such as Perl, Unix shell, or Python
•Experience with any object-oriented programming language (C++, Java, Python, etc.)
•Familiar with Verilog or SystemVerilog
•Enrolled in Computer Engineering or Electrical Engineering program, or similar

Citizenship Requirement N/A

APPLICATION INFORMATION

Application Procedure Through Employer Website
Cover Letter Required? Yes
Address Cover Letter to Hiring Manager
Special Application Instructions

Application Link:

https://careers.synopsys.com/job/mississauga/digital-design-verification-engineering-intern/44408/74034245488
Please click the "I intend to apply to this position" button on SCOPE and also submit your application via the employer's website. Applications are accepted on a rolling basis and the posting may be expired at any time by the employer as submissions are received. Students should submit their applications as soon as they are ready.