Job Posting:165952 - Position: S25 FPGA Digital Design Engineering Intern 165952 E2

Co-op Work Term Posted:	2025 - Summer
App Deadline	03/26/2025 09:00 AM
Application Method:	Through Employer Website
Posting Goes Live:	03/05/2025 10:16 AM
Job Posting Status:	Approved

ORGANIZATION INFORMATION

Organization	Kepler Communications Inc.
Address Line 1	355 ADELAIDE ST W, SUITE 500
City	Toronto
Postal Code / Zip Code	M5V 1S2
Province / State	ON
Country	Canada

JOB POSTING INFORMATION

Placement Term	2025 - Summer
<b> Job Title <b>	S25 FPGA Digital Design Engineering Intern 165952 E2
Position Type	Co-op Position
Job Location	Toronto, ON
Country	Canada
Duration	4 or 8 months
Work Mode	Hybrid
Salary Currency	CAD
Salary	Salary Not Available, 0 Major List

Job Description

FPGA Digital Design Engineering Intern

Kepler is on an audacious mission: to bring the internet to space. Founded in 2015, our ambition is to provide internet connectivity in space, whether in LEO, MEO, GEO, or beyond. With an expanding base of early customers and our first 23 satellites in orbit, Kepler is continuing to grow and expand its most important asset - the Team!

This position requires candidates to be available for 4-16 months starting May or September 2025.

We invest heavily to deliver the best products to our customers, and so we're on the hunt for a top-tier FPGA Digital Designer Engineer Intern. The RTL code you write will contribute to our new generation of satellites and earth stations.

Responsibilities

- Maintain and add new functionality to our FPGA code base, including code to control and test our SDR (software-defined radio) and SDN (software-defined network);
- Design custom IP for new features of both Kepler's satellites and ground stations;
- Add support for new sensors/communication interfaces (such as SPI, I2C, UART);
- Work with high-speed FPGA interfaces (e.g. JESD204b, 10G Ethernet, Aurora).

Job Requirements

Requirements

• 2+ years in an Electrical or Computer Engineering degree program, or equivalent;
•Experience with Verilog, SystemVerilog, or VHDL. (You will be working in SystemVerilog).
•Bonus Points
•Acceptance into a Masters in Electrical or Computer Engineering, or equivalent;
•Experience with DSP (digital signal processing) algorithms;
•Strong skills with C++ and embedded programming;
•Strong scripting experience (e.g. bash, Python, Tcl, etc.);
•Relevant experience through hobbies or a university design team.
•This position requires candidates to be available for 4-16 months starting May or September 2025.
This position can be on-site, hybrid, or remote and is based out of Kepler's Toronto Office located at 24 Ward Street, Toronto ON M6H 4A6.
Please note: This job is funded by the Government of Canada's Student Work Placement Program (SWPP) or Canada Summer Jobs. These programs require that candidates be a Canadian citizen, permanent resident or a protected person defined by the Immigration and Refugee Protection Act.

Citizenship Requirement N/A

APPLICATION INFORMATION

Application Procedure Through Employer Website
Cover Letter Required? Optional
Special Application Instructions

Please apply via the link here: https://jobs.lever.co/kepler/8ee064a3-cb35-437d-8355-721fe18184cd
Please click the "I intend to apply to this position" button on SCOPE and also submit your application via the employer's website.
Applications are accepted on a rolling basis and the posting may be expired at any time by the employer as submissions are received.
Students should submit their applications as soon as they are ready.