# Deep Reinforcement Learning-based Decoupling Capacitor Optimization Method for Multi-Power Domain considering Transfer Noise in 3D-ICs

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Abstract-In this paper, we propose a deep reinforcement learning (DRL)-based multi-power distribution network (PDN) decoupling capacitor design optimization method considering transfer noise in 3D-ICs. The transfer noise from multi-PDN with vertical structures could cause system failure, the entire simultaneous switching noise (SSN) with the combined transfer noise should be considered. To address the multi-PDN problem, we use reinforcement learning suitable for solving complex optimization problems. The input dataset and Markov decision process (MDP) were designed to optimize various multi-PDN cases. The 5x4 size of two PDNs with a vertically stacked structure was used for verification. The proposed method successfully optimizes the decoupling capacitors of multi-PDN. In addition, the proposed method was compared to genetic algorithm (GA), the proposed method perfored better optimization and reduced the time by about 99% compared to GA to 0.08 seconds.

Index Terms—Deep reinforcement learning (DRL), Deep Q network (DQN), Markov decision process (MDP) Power distribution network (PDN), Simultaneous switching noise (SSN)

#### I. INTRODUCTION

Recently, integrated circuit (IC) chips are getting smaller and closer according to the demand for high-performance semiconductors. Therefore, in order to integrate several systems in a limited space, a 3D-IC in which several systems are vertically stacked was developed. The 3D-ICs needs a multi-power domain, and the power distribution network (PDN) for supplying multiple power exists vertically [1]. As the current is rapidly switched, an undesirable noise called simultaneous switching noise (SSN) is generated in PDN. Because SSN causes power integrity problems, the PDN selfimpedance should be lowered below a specific value called target impedance using the decoupling capacitor (decap). The decaps should be optimized due to different impedance changes depending on location and number. There have been researches to optimize decaps with genetic algorithm (GA) and deep reinforcement learning (DRL) [2], [3].

However, PDNs with vertical structures cause large transfer noise as well as self-noise due to the coupling between PDNs of different domains as shown in Fig.1 (a). Because the entire SSN is the summation of transfer noise and the self-noise, the system could fail in a design that considers only the existing

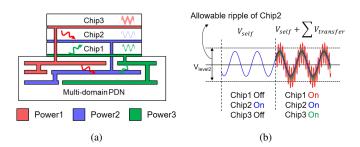


Fig. 1. Multi-PDN of 3D-ICs with vertical structure (a) Cross-section view (b) Supply voltage of chip2 depending on chip operations.

self-noise [2], [3], as shown in Fig.1 (b). Therefore, when designing the PDN of 3D-ICs, the entire SSN with transfer noise should be considered. The self and transfer noise are generated by the product of the switching current and the impedances. To reduce the entire SSN, it is assumed that target impedances of exist for self and transfer impedance. Therefore, when designing two power domains, we need to consider three factors: self-impedance of domain1, self-impedance of domain2, and transfer impedance of domains 1 and 2. However, since 3D-IC has many power domains, it is more difficult to optimize decaps.

In this paper, we propose a deep reinforcement learning-based multi-PDN decoupling capacitor design optimization method considering transfer noise in 3D-IC. The Markov decision process (MDP) and environment were designed with input datasets for various cases. The deep Q-network (DQN), a representative value-based algorithm was used for training, the proposed method could optimize decap of multi-PDN with different observation ports and target impedances. For the verification, the proposed method is compared to a genetic algorithm with random 12 cases.

# II. PROPOSAL OF DRL-BASED MULTI PDN DECOUPLING CAPACITOR OPTIMIZATION METHOD

In this section, we focus on designing an input dataset to learn reusable policy when the location of ports and target impedances are different. Then, we describe MDP for

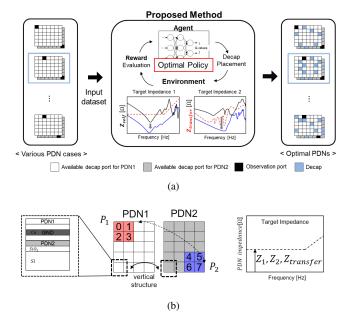


Fig. 2. Overview of proposed method using DRL (a) Proposed DRL-based deacp optimization method for multi-PDN. (b) Structure of two PDNs and definition of input dataset.

optimization of multi-PDN. The conceptual image of proposed method is as shown in Fig. 2(a).

# A. Definition of Input dataset for different port locations and target impedances

Depending on property of various system, the locations of ports and target impedance are designed differently. Therefore, we design dataset with different locations of the ports and the value of the target impedances as an input, as shown in (1) and Fig. 2(b).

$$Dataset_{input} = [P_1, P_2, Z_1, Z_2, Z_T]$$
 (1)

where  $P_1$  and  $P_2$  are the port locations of PDN1 and PDN2.  $Z_1$  and  $Z_2$  are the magnitude of target self-impedances of  $P_1$  and  $P_2$ .  $Z_T$  is the magnitude of target transfer-impedance between  $P_1$  and  $P_2$ . By configuring the environment for multi-PDN through Input dataset, it is possible to learn for various cases.

# B. Definition of Markov decision process for Multi-PDN

Based on the input dataset, the state of the initial PDN including the port locations, and the reward that is a function of target impedances are determined. Fig. 3 shows detail about MDP and the definition of MDP is as follows:

- State  $S_t$  is a matrix of the PDN and impedance states. The elements of PDN state : available decap port, decap, observation port.
  - The elements of impedance state : under target impedance, over target impedance
- Action A<sub>t</sub> is an assignment of the decap at a certain position. The assignment is limited when the self-impedance of PDN is satisfied the target self-impedance.
- Reward R<sub>t</sub> is combination of the number of frequency points at which each impedance does not satisfy the target impedance as formulated in (2).

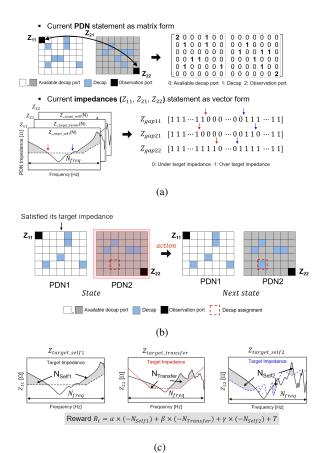


Fig. 3. Definition of MDP (a) State  $S_t$  is expressed by a matrix of the PDNs with port locations. (b) Action  $A_t$  is an assignment the decaps at a certain position. (c) Reward  $R_t$  is is combination of numbers of frequency points at which each impedance does not satisfy the target impedance.

$$R_t = -(\alpha * N_{self1} + \beta * N_{Transfer} + \gamma * N_{self2}) + T$$
 (2)

where  $N_{self1}$ ,  $N_{self2}$  and  $N_{Transfer}$  are the number of frequency points that do not satisfy the target impedance at states.  $\alpha$ ,  $\beta$  and  $\gamma$  are the weights that determine the importance of rewards. They were determined empipically. T is termination reward at the end of the episode. In order to calculate the reward changed by decap assignment, impedance matrix was obtained by using the segmentation method [4]. The episode ends when all impedance satisfies the target impedances or when there is no area to place the decap. With the defined MDP above, the DRL model learns the policy and optimizes the decap.

# III. VERIFICATION OF THE PROPOSED METHOD

For verification, the 5x4 size of two different PDNs with a vertically stacked structure and decoupling capacitor were used [5]. And we assumed that the structure of PDNs is fixed. The parameters for training are shown in Table I. The input dataset was arbitrarily selected as a combination within the range possible by the parameters in Table I.

Fig. 4 shows the training loss and average reward of each step. As the episode progresses, it can be seen that the reinforcement learning model builds experience while exploring, and the loss converges as the 500 episodes pass. Since the loss

TABLE I PARAMETERS FOR VERIFICATION

Parameter	Value	Parameter	Value	
Hidden layers	256,512,128	$P_1$	[0,1,2,3]	
Loss	MSE	$P_2$	[4,5,6,7]	
Learning rate	1e-04	$Z_1$	[2,2.5,3,3.5]	
Epsilon	1→0.001	$Z_2$	[2,2.5,3,3.5]	
Total episode	5000	$Z_T$	[0.1,0.2,0.3,0.4]	

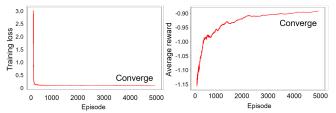


Fig. 4. Convergence of the training loss and average reward of each step.

converges to learn the optimal policy, the average reward is maximized.

The proposed method was compared with GA, which finds the best solution through variant algorithms in several initial populations. A total of 12 cases were conducted, and case 1 was selected as a validation case, and other cases were randomly selected. A narrower interval value was used, not the value used for learning. In the validation case, we confirmed that the proposed method was fast at 10/0.07 sec and found a global optimum. Table II compares the optimization results of proposed method and GA using 100 populations and 20 generations. Table II shows that the proposed method performed better in most cases than GA, and faster the optimization time excluded learning time. It was verified that it is the best method for fast and reusable use

The decap assignment results of validation case are shown in Fig. 5, a total of 10 decaps were used, 5 each for PDN1 and PDN2 respectively. The target impedance of PDN1 and PDN2 is same, displaying them on one graph. As shown in the graph, self-impedance for PDN1 (solid blue line) and self-impedance for PDN2 (dotted blue line) satisfied the target impedance in all frequency regions at the initial impedance, respectively, and transfer impedance also satisfied the target impedance in all frequency regions.

### IV. CONCLUSION

In this paper, we proposed a deep reinforcement learning-based multi-PDN decoupling capacitor design optimization method considering transfer noise in 3D IC. The input dataset and Markov decision process were designed to optimize various multi-PDN cases. For the verification, the proposed method was applied to a 5x4x2 size initial PDN. The proposed method successfully optimizes the multi-PDN decaps with a minimum number of decap by satisfying the target impedances. Also, the proposed method was compared to genetic algorithm of 100 populations and 20 generations. A total 12 cases were randomly selected, the proposed method performed better and faster than GA. It was verified that it is an appropriate method to optimize decaps in 3D-ICs in terms of reusablity and time consumption by reducing 99% simulation

 $\label{thm:table II} \text{Optimization results compared to genetic algorithm.}$ 

	Input dataset					GA (100/20)	Ours
	$P_1$	$P_2$	$Z_1$	$Z_2$	$Z_T$	Number of decaps / Time	
Case1	0	7	3.3	3.3	0.1	11 / 5mins	10 / 0.07sec
Case2	0	7	2	2	0.1	18 / 5mins	16 / 0.08sec
Case3	0	7	3.5	3.5	0.4	10 / 5mins	10 / 0.07sec
Case4	3	4	2	2	0.1	16 / 5mins	16 / 0.08sec
Case5	3	4	3.5	3.5	0.4	10 / 5mins	10 / 0.07sec
Case6	3	4	2.3	2.8	0.1	14 / 5mins	13 / 0.07sec
Case7	1	7	3.1	2	0.1	Fail / 5mins	13 / 0.07sec
Case8	1	5	2.3	2.8	0.25	13 / 5mins	11 / 0.07sec
Case9	3	7	3.2	3.2	0.3	10 / 5mins	11 / 0.07sec
Case10	0	6	2.6	2.6	0.15	14 / 5mins	14 / 0.08sec
Case11	2	5	2.7	3.2	0.35	11 / 5mins	11 / 0.07sec
Case12	3	6	2.4	2.1	0.2	14 / 5mins	13 / 0.07sec

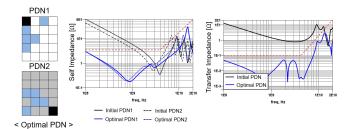


Fig. 5. Decap assignment and PDN impdances of validation case.

time. Currently, the decaps of two PDNs are optimized in this paper, but it is expected that this method can be extended to research that optimizes more than three multi-PDN of 3D-ICs.

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### REFERENCES

- R. Mahajan and B. Sankman, "3D packaging architectures and assembly process design," in 3D Microelectronic Packaging (Springer Series in Advanced Microelectronics), vol. 57, Y. Li and D. Goyal, Eds. Cham, Switzerland: Springer, 2017.
- [2] S. Piersanti, F. de Paulis, C. Olivieri and A. Orlandi, "Decoupling Capacitors Placement for a Multichip PDN by a Nature-Inspired Algorithm," in IEEE Transactions on Electromagnetic Compatibility, vol. 60, no. 6, pp. 1678-1685, Dec. 2018
- [3] H. Park et al., "Deep Reinforcement Learning-Based Optimal Decoupling Capacitor Design Method for Silicon Interposer-Based 2.5-D/3-D ICs," in IEEE Transactions on Components, Packaging and Manufacturing Technology (TCPMT), vol. 10, no. 3, pp. 467-478, Mar. 2020.
- [4] B. Bae et al., "Modeling and Measurement of Power Supply Noise Effects on an Analog-to-Digital Converter Based on a Chip-PCB Hierarchical Power Distribution Network Analysis," in IEEE Transactions on Electromagnetic Compatibility, vol. 55, no. 6, pp. 1260-1270, Dec. 2013.
- [5] K. Cho et al., "Fast and Accurate Power Distribution Network Modeling of a Silicon Interposer for 2.5-D/3-D ICs With Multiarray TSVs," in IEEE Transactions on Components, Packaging and Manufacturing Technology, vol. 9, no. 9, pp. 1835-1846, Sept. 2019