# 7 Register description

The device contains a set of registers which are used to control its behavior and to retrieve acceleration data. The registers address, made of 7 bits, is used to identify them and to write the data through serial interface.

## 7.1 WHO_AM_I (0Fh)

**Table 16. WHO_AM_I register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |

Device identification register.

This register contains the device identifier that for LIS331DLH is set to 32h.

## 7.2 CTRL_REG1 (20h)

**Table 17. CTRL_REG1 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| PM2 | PM1 | PM0 | DR1 | DR0 | Zen | Yen | Xen |

**Table 18. CTRL_REG1 description**

| | |
|---|---|
| PM2 - PM0 | Power mode selection. Default value: 000<br>(000: Power-down; Others: refer to *Table 19*) |
| DR1, DR0 | Data rate selection. Default value: 00<br>(00:50 Hz; Others: refer to *Table 20*) |
| Zen | Z axis enable. Default value: 1<br>(0: Z axis disabled; 1: Z axis enabled) |
| Yen | Y axis enable. Default value: 1<br>(0: Y axis disabled; 1: Y axis enabled) |
| Xen | X axis enable. Default value: 1<br>(0: X axis disabled; 1: X axis enabled) |

**PM** bits allow to select between power-down and two operating active modes. The device is in power-down mode when PD bits are set to “000” (default value after boot). *Table 19* shows all the possible power mode configurations and respective output data rates. Output data in the low-power modes are computed with low-pass filter cut-off frequency defined by DR1, DR0 bits.

**DR** bits, in the normal-mode operation, select the data rate at which acceleration samples are produced. In low-power mode they define the output data resolution. *Table 20* shows all the possible configuration for DR1 and DR0 bits.

Table 19. Power mode and low-power output data rate configurations

| PM2 | PM1 | PM0 | Power mode selection | Output data rate [Hz] $ODR_{LP}$ |
|---|---|---|---|---|
| 0 | 0 | 0 | Power-down | -- |
| 0 | 0 | 1 | Normal mode | ODR |
| 0 | 1 | 0 | Low-power | 0.5 |
| 0 | 1 | 1 | Low-power | 1 |
| 1 | 0 | 0 | Low-power | 2 |
| 1 | 0 | 1 | Low-power | 5 |
| 1 | 1 | 0 | Low-power | 10 |

Table 20. Normal-mode output data rate configurations and low-pass cut-off frequencies

| DR1 | DR0 | Output Data Rate [Hz] ODR | Low-pass filter cut-off frequency [Hz] |
|---|---|---|---|
| 0 | 0 | 50 | 37 |
| 0 | 1 | 100 | 74 |
| 1 | 0 | 400 | 292 |
| 1 | 1 | 1000 | 780 |

## 7.3 CTRL_REG2 (21h)

Table 21. CTRL_REG2 register

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| BOOT | HPM1 | HPM0 | FDS | HPen2 | HPen1 | HPCF1 | HPCF0 |

Table 22. CTRL_REG2 description

| | |
|---|---|
| BOOT | Reboot memory content. Default value: 0<br>(0: normal mode; 1: reboot memory content) |
| HPM1, HPM0 | High pass filter mode selection. Default value: 00<br>(00: normal mode; Others: refer to *Table 23*) |
| FDS | Filtered data selection. Default value: 0<br>(0: internal filter bypassed; 1: data from internal filter sent to output register) |
| HPen2 | High pass filter enabled for interrupt 2 source. Default value: 0<br>(0: filter bypassed; 1: filter enabled) |

Table 22. CTRL_REG2 description (continued)

| | |
|---|---|
| HPen1 | High pass filter enabled for interrupt 1 source. Default value: 0<br>(0: filter bypassed; 1: filter enabled) |
| HPCF1,<br>HPCF0 | High pass filter cut-off frequency configuration. Default value: 00<br>(00: HPc=8; 01: HPc=16; 10: HPc=32; 11: HPc=64) |

**BOOT** bit is used to refresh the content of internal registers stored in the flash memory block. At the device power up the content of the flash memory block is transferred to the internal registers related to trimming functions to permit a good behavior of the device itself. If for any reason the content of trimming registers was changed it is sufficient to use this bit to restore correct values. When BOOT bit is set to '1' the content of internal flash is copied inside corresponding internal registers and it is used to calibrate the device. These values are factory trimmed and they are different for every accelerometer. They permit a good behavior of the device and normally they have not to be changed. At the end of the boot process the BOOT bit is set again to '0'.

Table 23. High-pass filter mode configuration

| HPM1 | HPM0 | High-pass filter mode |
|---|---|---|
| 0 | 0 | Normal mode (reset reading HP_RESET_FILTER) |
| 0 | 1 | Reference signal for filtering |
| 1 | 0 | Normal mode (reset reading HP_RESET_FILTER) |

**HPCF[1:0]**. These bits are used to configure high-pass filter cut-off frequency $f_t$ which is given by:

$$f_t = \ln\left(1 - \frac{1}{HPc}\right) \cdot \frac{f_s}{2\pi}$$

The equation can be simplified to the following approximated equation:

$$f_t = \frac{f_s}{6 \cdot HPc}$$

Table 24. High-pass filter cut-off frequency configuration

| HPcoeff2,1 | $f_t$ [Hz]<br>Data rate = 50 Hz | $f_t$ [Hz]<br>Data rate = 100 Hz | $f_t$ [Hz]<br>Data rate = 400 Hz | $f_t$ [Hz]<br>Data rate = 1000 Hz |
|---|---|---|---|---|
| 00 | 1 | 2 | 8 | 20 |
| 01 | 0.5 | 1 | 4 | 10 |
| 10 | 0.25 | 0.5 | 2 | 5 |
| 11 | 0.125 | 0.25 | 1 | 2.5 |

## 7.4 CTRL_REG3 [Interrupt CTRL register] (22h)

**Table 25. CTRL_REG3 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| IHL | PP_OD | LIR2 | I2_CFG1 | I2_CFG0 | LIR1 | I1_CFG1 | I1_CFG0 |

**Table 26. CTRL_REG3 description**

| | |
|---|---|
| IHL | Interrupt active high, low. Default value: 0<br>(0: active high; 1:active low) |
| PP_OD | Push-pull/Open drain selection on interrupt pad. Default value 0.<br>(0: push-pull; 1: open drain) |
| LIR2 | Latch interrupt request on INT2_SRC register, with INT2_SRC register cleared by reading INT2_SRC itself. Default value: 0.<br>(0: interrupt request not latched; 1: interrupt request latched) |
| I2_CFG1, I2_CFG0 | Data signal on INT 2 pad control bits. Default value: 00.<br>(see table below) |
| LIR1 | Latch interrupt request on INT1_SRC register, with INT1_SRC register cleared by reading INT1_SRC register. Default value: 0.<br>(0: interrupt request not latched; 1: interrupt request latched) |
| I1_CFG1, I1_CFG0 | Data signal on INT 1 pad control bits. Default value: 00.<br>(see table below) |

**Table 27. Data signal on INT 1 and INT 2 pad**

| I1(2)_CFG1 | I1(2)_CFG0 | INT 1(2) Pad |
|---|---|---|
| 0 | 0 | Interrupt 1 (2) source |
| 0 | 1 | Interrupt 1 source OR interrupt 2 source |
| 1 | 0 | Data ready |
| 1 | 1 | Boot running |

## 7.5 CTRL_REG4 (23h)

**Table 28. CTRL_REG4 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| BDU | BLE | FS1 | FS0 | STsign | 0 | ST | SIM |

**Table 29. CTRL_REG4 description**

| | |
|---|---|
| BDU | Block data update. Default value: 0<br>(0: continuos update; 1: output registers not updated between MSB and LSB reading) |
| BLE | Big/little endian data selection. Default value 0.<br>(0: data LSB @ lower address; 1: data MSB @ lower address) |

Table 29. CTRL_REG4 description (continued)

| | |
|---|---|
| FS1, FS0 | Full-scale selection. Default value: 00.<br>(00: ±2 *g*; 01: ±4 *g*; 11: ±8 *g*) |
| STsign | Self-test sign. Default value: 00.<br>(0: self-test plus; 1 self-test minus) |
| ST | Self-test enable. Default value: 0.<br>(0: self-test disabled; 1: self-test enabled) |
| SIM | SPI serial interface mode selection. Default value: 0.<br>(0: 4-wire interface; 1: 3-wire interface) |

**BDU** bit is used to inhibit output registers update between the reading of upper and lower register parts. In default mode (BDU = '0') the lower and upper register parts are updated continuously. If it is not sure to read faster than output data rate, it is recommended to set BDU bit to '1'. In this way, after the reading of the lower (upper) register part, the content of that output registers is not updated until the upper (lower) part is read too.
This feature avoids reading LSB and MSB related to different samples.

## 7.6 CTRL_REG5 (24h)

Table 30. CTRL_REG5 register

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | TurnOn1 | TurnOn0 |

Table 31. CTRL_REG5 description

| | |
|---|---|
| TurnOn1, TurnOn0 | Turn-on mode selection for sleep to wake function. Default value: 00. |

**TurnOn** bits are used for turning on the **sleep to wake** function.

Table 32. Sleep to wake configuration

| TurnOn1 | TurnOn0 | Sleep to wake status |
|---|---|---|
| 0 | 0 | Sleep to wake function is disabled |
| 1 | 1 | Turned on: The device is in low power mode (ODR is defined in CTRL_REG1) |

Setting TurnOn[1:0] bits to 11 the "sleep to wake" function is enabled. When an interrupt event occurs the device is turned to normal mode increasing the ODR to the value defined in CTRL_REG1. Although the device is in normal mode, CTRL_REG1 content is not automatically changed to "normal mode" configuration.

## 7.7 HP_FILTER_RESET (25h)

Dummy register. Reading at this address zeroes instantaneously the content of the internal high pass-filter. If the high pass filter is enabled all three axes are instantaneously set to 0*g*. This allows to overcome the settling time of the high pass filter.

## 7.8 REFERENCE (26h)

**Table 33. REFERENCE register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Ref7 | Ref6 | Ref5 | Ref4 | Ref3 | Ref2 | Ref1 | Ref0 |

**Table 34. REFERENCE description**

| | |
|---|---|
| Ref7 - Ref0 | Reference value for high-pass filter. Default value: 00h. |

This register sets the acceleration value taken as a reference for the high-pass filter output.

When filter is turned on (at least one of FDS, HPen2, or HPen1 bit is equal to ‘1’) and HPM bits are set to “01”, filter out is generated taking this value as a reference.

## 7.9 STATUS_REG (27h)

**Table 35. STATUS_REG register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| ZYXOR | ZOR | YOR | XOR | ZYXDA | ZDA | YDA | XDA |

**Table 36. STATUS_REG description**

| | |
|---|---|
| ZYXOR | X, Y and Z axis data overrun. Default value: 0<br>(0: no overrun has occurred;<br>1: new data has overwritten the previous one before it was read) |
| ZOR | Z axis data overrun. Default value: 0<br>(0: no overrun has occurred;<br>1: a new data for the Z-axis has overwritten the previous one) |
| YOR | Y axis data overrun. Default value: 0<br>(0: no overrun has occurred;<br>1: a new data for the Y-axis has overwritten the previous one) |
| XOR | X axis data overrun. Default value: 0<br>(0: no overrun has occurred;<br>1: a new data for the X-axis has overwritten the previous one) |
| ZYXDA | X, Y and Z axis new data available. Default value: 0<br>(0: a new set of data is not yet available; 1: a new set of data is available) |

Table 36. STATUS_REG description (continued)

| | |
|---|---|
| ZDA | Z axis new data available. Default value: 0<br>(0: a new data for the Z-axis is not yet available;<br>1: a new data for the Z-axis is available) |
| YDA | Y axis new data available. Default value: 0<br>(0: a new data for the Y-axis is not yet available;<br>1: a new data for the Y-axis is available) |
| XDA | X axis new data available. Default value: 0<br>(0: a new data for the X-axis is not yet available;<br>1: a new data for the X-axis is available) |

## 7.10 OUT_X_L (28h), OUT_X_H (29)

X-axis acceleration data. The value is expressed as two's complement.

## 7.11 OUT_Y_L (2Ah), OUT_Y_H (2Bh)

Y-axis acceleration data. The value is expressed as two's complement.

## 7.12 OUT_Z_L (2Ch), OUT_Z_H (2Dh)

Z-axis acceleration data. The value is expressed as two's complement.

## 7.13 INT1_CFG (30h)

Table 37. INT1_CFG register

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| AOI | 6D | ZHIE | ZLIE | YHIE | YLIE | XHIE | XLIE |

Table 38. INT1_CFG description

| | |
|---|---|
| AOI | AND/OR combination of Interrupt events. Default value: 0.<br>(See *Table 39*) |
| 6D | 6 direction detection function enable. Default value: 0.<br>(See *Table 39*) |
| ZHIE | Enable interrupt generation on Z high event. Default value: 0<br>(0: disable interrupt request;<br>1: enable interrupt request on measured accel. value higher than preset threshold) |
| ZLIE | Enable interrupt generation on Z low event. Default value: 0<br>(0: disable interrupt request;<br>1: enable interrupt request on measured accel. value lower than preset threshold) |
| YHIE | Enable interrupt generation on Y high event. Default value: 0<br>(0: disable interrupt request;<br>1: enable interrupt request on measured accel. value higher than preset threshold) |

**Table 38. INT1_CFG description**

| | |
|---|---|
| YLIE | Enable interrupt generation on Y low event. Default value: 0<br>(0: disable interrupt request;<br>1: enable interrupt request on measured accel. value lower than preset threshold) |
| XHIE | Enable interrupt generation on X high event. Default value: 0<br>(0: disable interrupt request;<br>1: enable interrupt request on measured accel. value higher than preset threshold) |
| XLIE | Enable interrupt generation on X low event. Default value: 0<br>(0: disable interrupt request;<br>1: enable interrupt request on measured accel. value lower than preset threshold) |

Configuration register for Interrupt 1 source.

**Table 39. Interrupt 1 source configurations**

| AOI | 6D | Interrupt mode |
|---|---|---|
| 0 | 0 | OR combination of interrupt events |
| 0 | 1 | 6 direction movement recognition |
| 1 | 0 | AND combination of interrupt events |
| 1 | 1 | 6 direction position recognition |

## 7.14 INT1_SRC (31h)

**Table 40. INT1_SRC register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0 | IA | ZH | ZL | YH | YL | XH | XL |

**Table 41. INT1_SRC description**

| | |
|---|---|
| IA | Interrupt active. Default value: 0<br>(0: no interrupt has been generated; 1: one or more interrupts have been generated) |
| ZH | Z high. Default value: 0<br>(0: no interrupt, 1: Z High event has occurred) |
| ZL | Z low. Default value: 0<br>(0: no interrupt; 1: Z Low event has occurred) |
| YH | Y high. Default value: 0<br>(0: no interrupt, 1: Y High event has occurred) |
| YL | Y low. Default value: 0<br>(0: no interrupt, 1: Y Low event has occurred) |
| XH | X high. Default value: 0<br>(0: no interrupt, 1: X High event has occurred) |
| XL | X low. Default value: 0<br>(0: no interrupt, 1: X Low event has occurred) |

Interrupt 1 source register. Read only register.

Reading at this address clears INT1_SRC IA bit (and the interrupt signal on INT 1 pin) and allows the refreshment of data in the INT1_SRC register if the latched option was chosen.

## 7.15 INT1_THS (32h)

**Table 42. INT1_THS register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0 | THS6 | THS5 | THS4 | THS3 | THS2 | THS1 | THS0 |

**Table 43. INT1_THS description**

| | |
|---|---|
| THS6 - THS0 | Interrupt 1 threshold. Default value: 000 0000 |

## 7.16 INT1_DURATION (33h)

**Table 44. INT1_DURATION register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

**Table 45. INT2_DURATION description**

| | |
|---|---|
| D6 - D0 | Duration value. Default value: 000 0000 |

**D6 - D0** bits set the minimum duration of the Interrupt 2 event to be recognized. Duration steps and maximum values depend on the ODR chosen.

## 7.17 INT2_CFG (34h)

**Table 46. INT2_CFG register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| AOI | 6D | ZHIE | ZLIE | YHIE | YLIE | XHIE | XLIE |

**Table 47. INT2_CFG description**

| | |
|---|---|
| AOI | AND/OR combination of interrupt events. Default value: 0.<br>(See table below) |
| 6D | 6 direction detection function enable. Default value: 0.<br>(See table below) |
| ZHIE | Enable interrupt generation on Z high event. Default value: 0<br>(0: disable interrupt request;<br>1: enable interrupt request on measured accel. value higher than preset threshold) |
| ZLIE | Enable interrupt generation on Z low event. Default value: 0<br>(0: disable interrupt request;<br>1: enable interrupt request on measured accel. value lower than preset threshold) |

Table 47. INT2_CFG description (continued)

| | |
|---|---|
| YHIE | Enable interrupt generation on Y high event. Default value: 0<br>(0: disable interrupt request;<br>1: enable interrupt request on measured accel. value higher than preset threshold) |
| YLIE | Enable interrupt generation on Y low event. Default value: 0<br>(0: disable interrupt request;<br>1: enable interrupt request on measured accel. value lower than preset threshold) |
| XHIE | Enable interrupt generation on X high event. Default value: 0<br>(0: disable interrupt request;<br>1: enable interrupt request on measured accel. value higher than preset threshold) |
| XLIE | Enable interrupt generation on X low event. Default value: 0<br>(0: disable interrupt request;<br>1: enable interrupt request on measured accel. value lower than preset threshold) |

Configuration register for Interrupt 2 source.

Table 48. Interrupt mode configuration

| AOI | 6D | Interrupt mode |
|---|---|---|
| 0 | 0 | OR combination of interrupt events |
| 0 | 1 | 6 direction movement recognition |
| 1 | 0 | AND combination of interrupt events |
| 1 | 1 | 6 direction position recognition |

## 7.18 INT2_SRC (35h)

Table 49. INT2_SRC register

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0 | IA | ZH | ZL | YH | YL | XH | XL |

Table 50. INT2_SRC description

| | |
|---|---|
| IA | Interrupt active. Default value: 0<br>(0: no interrupt has been generated; 1: one or more interrupts have been generated) |
| ZH | Z high. Default value: 0<br>(0: no interrupt, 1: Z high event has occurred) |
| ZL | Z low. Default value: 0<br>(0: no interrupt; 1: Z low event has occurred) |
| YH | Y high. Default value: 0<br>(0: no interrupt, 1: Y high event has occurred) |
| YL | Y low. Default value: 0<br>(0: no interrupt, 1: Y low event has occurred) |

**Table 50. INT2_SRC description**

| | |
|---|---|
| XH | X high. Default value: 0<br>(0: no interrupt, 1: X high event has occurred) |
| XL | X Low. Default value: 0<br>(0: no interrupt, 1: X low event has occurred) |

Interrupt 2 source register. Read only register.

Reading at this address clears INT2_SRC IA bit (and the interrupt signal on INT 2 pin) and allows the refreshment of data in the INT2_SRC register if the latched option was chosen.

## 7.19 INT2_THS (36h)

**Table 51. INT2_THS register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0 | THS6 | THS5 | THS4 | THS3 | THS2 | THS1 | THS0 |

**Table 52. INT2_THS description**

| | |
|---|---|
| THS6 - THS0 | Interrupt 1 threshold. Default value: 000 0000 |

## 7.20 INT2_DURATION (37h)

**Table 53. INT2_DURATION register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

**Table 54. INT2_DURATION description**

| | |
|---|---|
| D6 - D0 | Duration value. Default value: 000 0000 |

**D6 - D0** bits set the minimum duration of the Interrupt 2 event to be recognized. Duration time steps and maximum values depend on the ODR chosen.