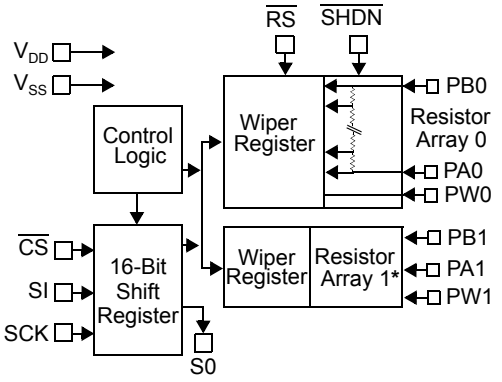
MCP41XXX/42XXX

Single/Dual Digital Potentiometer with SPI™ Interface

Features

- 256 taps for each potentiometer
- Potentiometer values for 10 kΩ, 50 kΩ and 100 kΩ
- Single and dual versions
- SPI™ serial interface (mode 0,0 and 1,1)
- ±1 LSB max INL & DNL
- Low power CMOS technology
- 1 µA maximum supply current in static operation
- Multiple devices can be daisy-chained together (MCP42XXX only)
- Shutdown feature open circuits of all resistors for maximum power savings
- Hardware shutdown pin available on MCP42XXX only
- Single supply operation (2.7V - 5.5V)
- Industrial temperature range: -40°C to +85°C
- Extended temperature range: -40°C to +125°C

Block Diagram



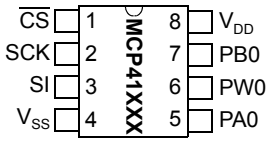
*Potentiometer P1 is only available on the dual MCP42XXX version.

Description

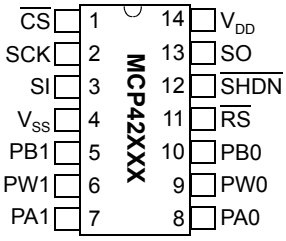
The MCP41XXX and MCP42XXX devices are 256-position, digital potentiometers available in 10 kΩ, 50 kΩ and 100 kΩ resistance versions. The MCP41XXX is a single-channel device and is offered in an 8-pin PDIP or SOIC package. The MCP42XXX contains two independent channels in a 14-pin PDIP, SOIC or TSSOP package. The wiper position of the MCP41XXX/42XXX varies linearly and is controlled via an industry-standard SPI interface. The devices consume <1 µA during static operation. A software shutdown feature is provided that disconnects the "A" terminal from the resistor stack and simultaneously connects the wiper to the "B" terminal. In addition, the dual MCP42XXX has a $\overline{SHDN}$ pin that performs the same function in hardware. During shutdown mode, the contents of the wiper register can be changed and the potentiometer returns from shutdown to the new value. The wiper is reset to the mid-scale position (80h) upon power-up. The $\overline{RS}$ (reset) pin implements a hardware reset and also returns the wiper to mid-scale. The MCP42XXX SPI interface includes both the SI and SO pins, allowing daisy-chaining of multiple devices. Channel-to-channel resistance matching on the MCP42XXX varies by less than 1%. These devices operate from a single 2.7 - 5.5V supply and are specified over the extended and industrial temperature ranges.

Package Types

PDIP/SOIC



PDIP/SOIC/TSSOP



1.0 ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS: 10 kΩ VERSION

Electrical Characteristics: Unless otherwise indicated, V_{DD} = +2.7V to 5.5V, T_A = -40°C to +85°C (TSSOP devices are only specified at +25°C and +85°C). Typical specifications represent values for V_{DD} = 5V, V_{SS} = 0V, V_B = 0V, T_A = +25°C.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Rheostat Mode						
Nominal Resistance	R	8	10	12	kΩ	T_A = +25°C **(Note 1)**
Rheostat Differential Non Linearity	R-DNL	-1	±1/4	+1	LSB	**Note 2**
Rheostat Integral Non Linearity	R-INL	-1	±1/4	+1	LSB	**Note 2**
Rheostat Tempco	$\Delta R_{AB}/\Delta T$	—	800	—	ppm/°C	
Wiper Resistance	R_W	—	52	100	Ω	V_{DD} = 5.5V, I_W = 1 mA, code 00h
	R_W	—	73	125	Ω	V_{DD} = 2.7V, I_W = 1 mA, code 00h
Wiper Current	I_W	-1	—	+1	mA	
Nominal Resistance Match	ΔR/R	—	0.2	1	%	**MCP42010 only**, P0 to P1; T_A = +25°C
Potentiometer Divider						
Resolution	N	8	—	—	Bits	
Monotonicity	N	8	—	—	Bits	
Differential Non-Linearity	DNL	-1	±1/4	+1	LSB	**Note 3**
Integral Non-Linearity	INL	-1	±1/4	+1	LSB	**Note 3**
Voltage Divider Tempco	$\Delta V_W/\Delta T$	—	1	—	ppm/°C	Code 80h
Full Scale Error	V_{WFSE}	-2	-0.7	0	LSB	Code FFh, V_{DD} = 5V, see Figure 2-25
	V_{WFSE}	-2	-0.7	0	LSB	Code FFh, V_{DD} = 3V, see Figure 2-25
Zero Scale Error	V_{WZSE}	0	+0.7	+2	LSB	Code 00h, V_{DD} = 5V, see Figure 2-25
	V_{WZSE}	0	+0.7	+2	LSB	Code 00h, V_{DD} = 3V, see Figure 2-25
Resistor Terminals						
Voltage Range	$V_{A,B,W}$	0	—	V_{DD}		**Note 4**
Capacitance (C_A or C_B)		—	15	—	pF	f = 1 MHz, Code = 80h, see Figure 2-30
Capacitance	C_W	—	5.6	—	pF	f = 1 MHz, Code = 80h, see Figure 2-30
Dynamic Characteristics (All dynamic characteristics use V_{DD} = 5V)						
Bandwidth -3dB	BW	—	1	—	MHz	V_B = 0V, Measured at Code 80h, Output Load = 30 pF
Settling Time	t_S	—	2	—	µS	V_A = V_{DD},V_B = 0V, ±1% Error Band, Transition from Code 00h to Code 80h, Output Load = 30 pF
Resistor Noise Voltage	e_{NWB}	—	9	—	nV/√Hz	V_A = Open, Code 80h, f =1 kHz
Crosstalk	C_T	—	-95	—	dB	V_A = V_{DD}, V_B = 0V **(Note 5)**
Digital Inputs/Outputs ($\overline{CS}$, SCK, SI, SO) See Figure 2-12 for $\overline{RS}$ and $\overline{SHDN}$ pin operation						
Schmitt Trigger High-Level Input Voltage	V_{IH}	0.7V_{DD}	—	—	V	
Schmitt Trigger Low-Level Input Voltage	V_{IL}	—	—	0.3V_{DD}	V	
Hysteresis of Schmitt Trigger Inputs	V_{HYS}	—	0.05V_{DD}	—		
Low-Level Output Voltage	V_{OL}	—	—	0.40	V	I_{OL} = 2.1 mA, V_{DD} = 5V
High-Level Output Voltage	V_{OH}	V_{DD} - 0.5	—	—	V	I_{OH} = -400 µA, V_{DD} = 5V
Input Leakage Current	I_{LI}	-1	—	+1	µA	$\overline{CS}$ = V_{DD}, V_{IN} = V_{SS} or V_{DD}, includes V_A $\overline{SHDN}$=0
Pin Capacitance (All inputs/outputs)	C_{IN}, C_{OUT}	—	10	—	pF	V_{DD} = 5.0V, T_A = +25°C, f_c = 1 MHz
Power Requirements						
Operating Voltage Range	V_{DD}	2.7	—	5.5	V	
Supply Current, Active	I_{DDA}	—	340	500	µA	V_{DD} = 5.5V, $\overline{CS}$ = V_{SS}, f_{SCK} = 10 MHz, SO = Open, Code FFh **(Note 6)**
Supply Current, Static	I_{DDS}	—	0.01	1	µA	$\overline{CS}$, $\overline{SHDN}$, $\overline{RS}$ = V_{DD} = 5.5V, SO = Open **(Note 6)**
Power Supply Sensitivity	PSS	—	0.0015	0.0035	%/%	V_{DD} = 4.5V - 5.5V, V_A = 4.5V, Code 80h
	PSS	—	0.0015	0.0035	%/%	V_{DD} = 2.7V - 3.3V, V_A = 2.7V, Code 80h

Note 1: V_{AB} = V_{DD}, no connection on wiper.

2: Rheostat position non-linearity R-INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from the ideal between successive tap positions. I_W = 50 µA for V_{DD} = 3V and I_W = 400 µA for V_{DD} = 5V for 10 kΩ version. See Figure 2-26 for test circuit.

3: INL and DNL are measured at V_W with the device configured in the voltage divider or potentiometer mode. V_A = V_{DD} and V_B = 0V. DNL specification limits of ±1 LSB max are specified monotonic operating conditions. See Figure 2-25 for test circuit.

4: Resistor terminals A,B and W have no restrictions on polarity with respect to each other. Full-scale and zero-scale error were measured using Figure 2-25.

5: Measured at V_W pin where the voltage on the adjacent V_W pin is swinging full-scale.

6: Supply current is independent of current through the potentiometers.

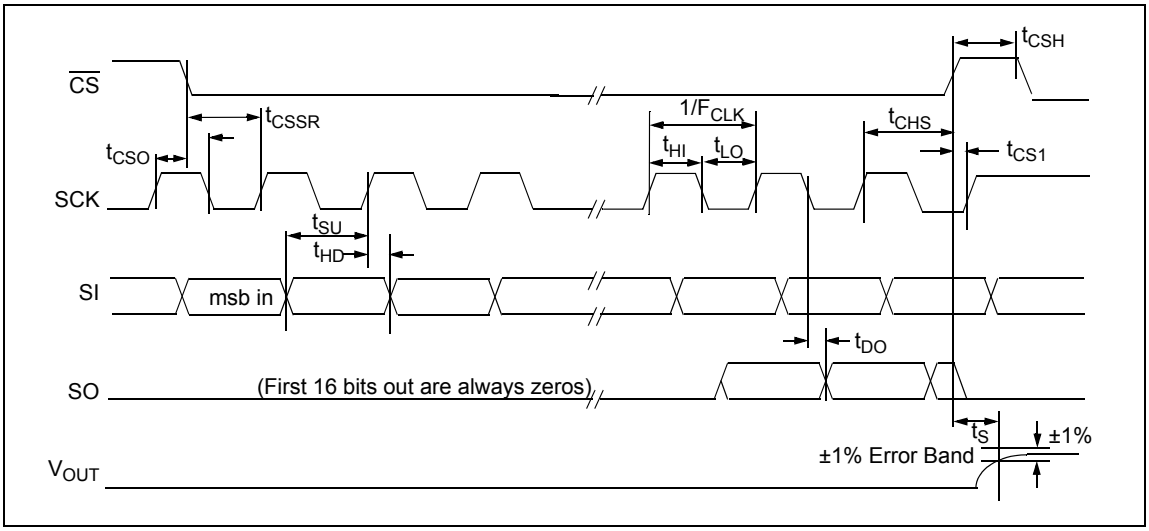


FIGURE 1-1: *Detailed Serial interface Timing.*

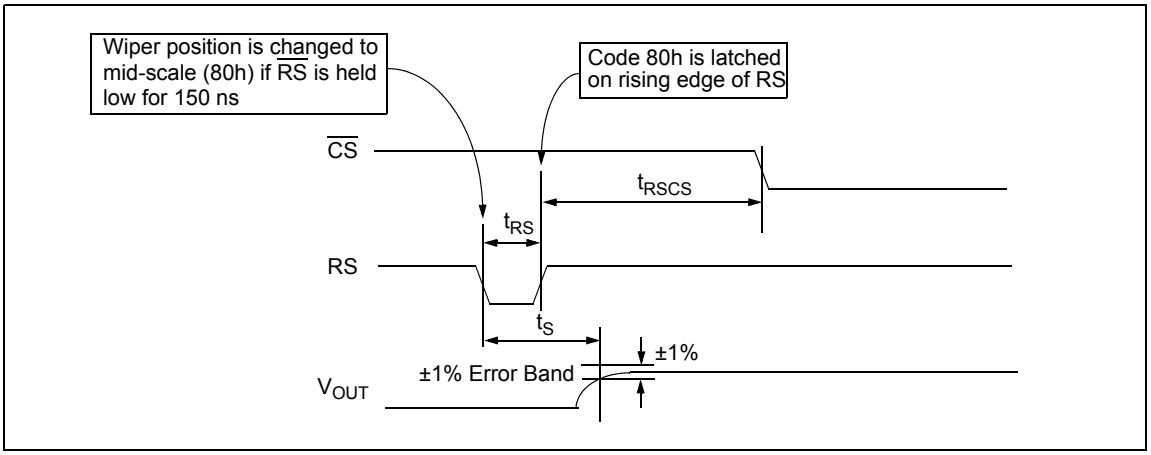


FIGURE 1-2: *Reset Timing.*

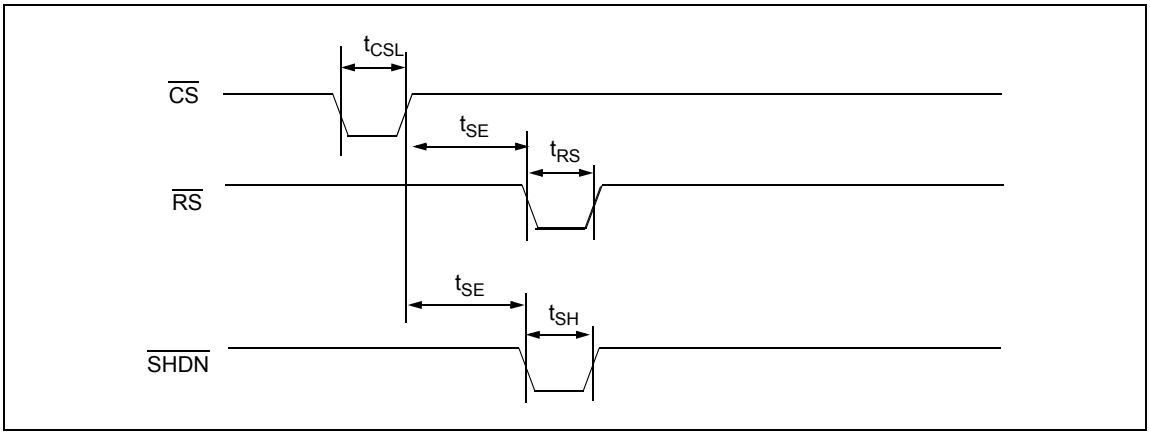


FIGURE 1-3: *Software Shutdown Exit Timing.*

2.0 TYPICAL PERFORMANCE CURVES

Note:	The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, curve represents 10 kΩ, 50 kΩ and 100 kΩ devices, V_{DD} = 5V, V_{SS} = 0V, T_A = +25°C, V_B = 0V.

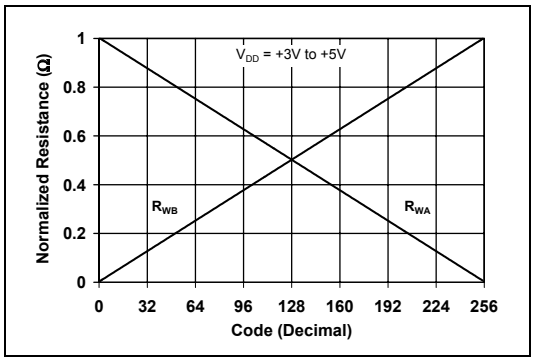


FIGURE 2-1: *Normalized Wiper to End Terminal Resistance vs. Code.*

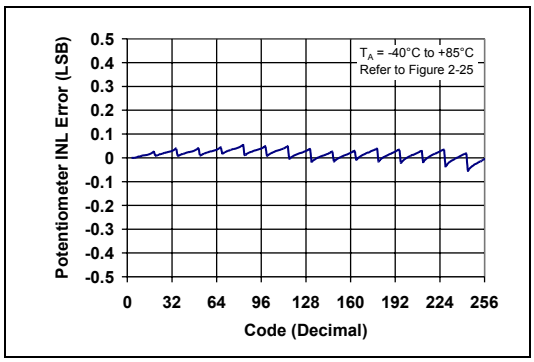


FIGURE 2-2: *Potentiometer INL Error vs. Code.*

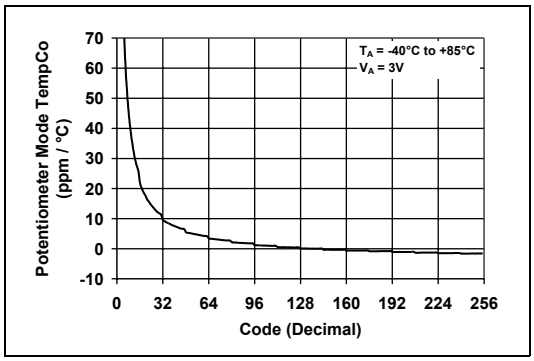


FIGURE 2-3: *Potentiometer Mode Tempco vs. Code.*

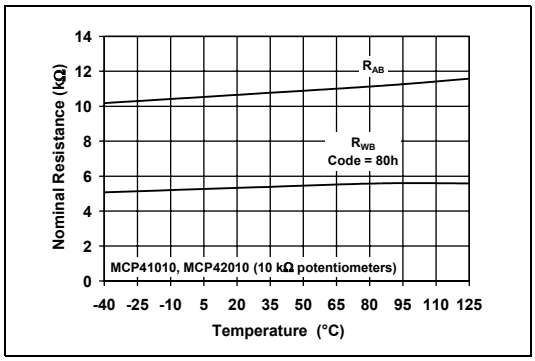


FIGURE 2-4: *Nominal Resistance 10 kΩ vs. Temperature.*

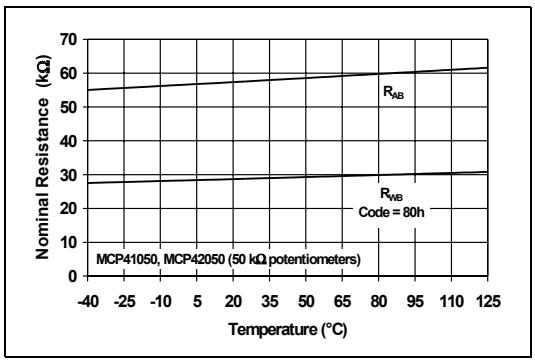


FIGURE 2-5: *Nominal Resistance 50 kΩ vs. Temperature.*

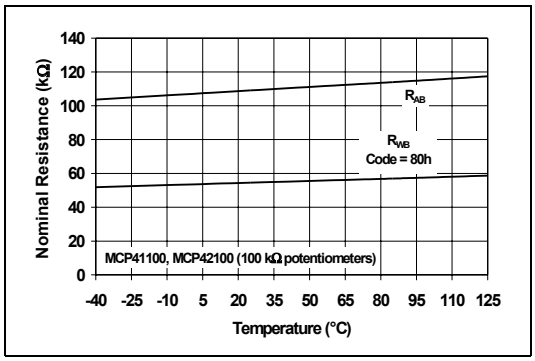


FIGURE 2-6: *Nominal Resistance 100 kΩ vs. Temperature.*

3.0 PIN DESCRIPTIONS

3.1 PA0, PA1

Potentiometer Terminal A Connection.

3.2 PB0, PB1

Potentiometer Terminal B Connection.

3.3 PW0, PW1

Potentiometer Wiper Connection.

3.4 Chip Select ($\overline{CS}$)

This is the SPI port chip select pin and is used to execute a new command after it has been loaded into the shift register. This pin has a Schmitt Trigger input.

3.5 Serial Clock (SCK)

This is the SPI port clock pin and is used to clock-in new register data. Data is clocked into the SI pin on the rising edge of the clock and out the SO pin on the falling edge of the clock. This pin is gated to the $\overline{CS}$ pin (i.e., the device will not draw any more current if the SCK pin is toggling when the $\overline{CS}$ pin is high). This pin has a Schmitt Trigger input.

3.6 Serial Data Input (SI)

This is the SPI port serial data input pin. The command and data bytes are clocked into the shift register using this pin. This pin is gated to the $\overline{CS}$ pin (i.e., the device will not draw any more current if the SI pin is toggling when the $\overline{CS}$ pin is high). This pin has a Schmitt Trigger input.

3.7 Serial Data Output (SO) (MCP42XXX devices only)

This is the SPI port serial data output pin used for daisy-chaining more than one device. Data is clocked out of the SO pin on the falling edge of clock. This is a push-pull output and **does not** go to a high-impedance state when $\overline{CS}$ is high. It will drive a logic-low when $\overline{CS}$ is high.

3.8 Reset ($\overline{RS}$) (MCP42XXX devices only)

The Reset pin will set all potentiometers to mid-scale (Code 80h) if this pin is brought low for at least 150 ns. This pin should not be toggled low when the $\overline{CS}$ pin is low. It is possible to toggle this pin when the $\overline{SHDN}$ pin is low. In order to minimize power consumption, this pin has an active pull-up circuit. The performance of this circuit is shown in Figure 2-12. This pin will draw negligible current at logic level '0' and logic level '1'. Do not leave this pin floating.

3.9 Shutdown ($\overline{SHDN}$) (MCP42XXX devices only)

The Shutdown pin has a Schmitt Trigger input. Pulling this pin low will put the device in a power-saving mode where A terminal is opened and the B and W terminals are connected for all potentiometers. This pin should not be toggled low when the $\overline{CS}$ pin is low. In order to minimize power consumption, this pin has an active pull-up circuit. The performance of this circuit is shown in Figure 2-12. This pin will draw negligible current at logic level '0' and logic level '1'. Do not leave this pin floating.

TABLE 3-1: MCP41XXX Pins

Pin #	Name	Function
1	$\overline{CS}$	Chip Select
2	SCK	Serial Clock
3	SI	Serial Data Input
4	V_{SS}	Ground
5	PA0	Terminal A Connection For Pot 0
6	PW0	Wiper Connection For Pot 0
7	PB0	Terminal B Connection For Pot 0
8	V_{DD}	Power

TABLE 3-2: MCP42XXX Pins

Pin #	Name	Function
1	$\overline{CS}$	Chip Select
2	SCK	Serial Clock
3	SI	Serial Data Input
4	V_{SS}	Ground
5	PB1	Terminal B Connection For Pot 1
6	PW1	Wiper Connection For Pot 1
7	PA1	Terminal A Connection For Pot 1
8	PA0	Terminal A Connection For Pot 0
9	PW0	Wiper Connection For Pot 0
10	PB0	Terminal B Connection For Pot 0
11	$\overline{RS}$	Reset Input
12	$\overline{SHDN}$	Shutdown Input
13	SO	Data Out for Daisy-Chaining
14	V_{DD}	Power

4.1 Modes of Operation

Digital potentiometer applications can be divided into two categories: rheostat mode and potentiometer, or voltage divider, mode.

4.1.1 RHEOSTAT MODE

In the rheostat mode, the potentiometer is used as a two-terminal resistive element. The unused terminal should be tied to the wiper, as shown in Figure 4-2. Note that reversing the polarity of the A and B terminals will not affect operation.

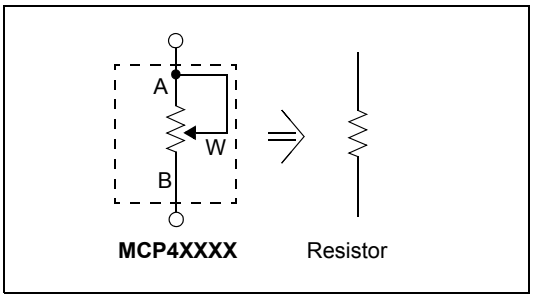


FIGURE 4-2: *Two-terminal or rheostat configuration for the digital potentiometer. Acting as a resistive element in the circuit, resistance is controlled by changing the wiper setting.*

Using the device in this mode allows control of the total resistance between the two nodes. The total measured resistance would be the least at code 00h, where the wiper is tied to the B terminal. The resistance at this code is equal to the wiper resistance, typically 52Ω for the 10 kΩ MCP4X010 devices, 125Ω for the 50 kΩ (MCP4X050), and 100 kΩ (MCP4X100) devices. For the 10 kΩ device, the LSB size would be 39.0625Ω (assuming 10 kΩ total resistance). The resistance would then increase with this LSB size until the total measured resistance at code FFh would be 9985.94Ω. The wiper will never directly connect to the A terminal of the resistor stack.

In the 00h state, the total resistance is the wiper resistance. To avoid damage to the internal wiper circuitry in this configuration, care should be taken to ensure the current flow never exceeds 1 mA.

For dual devices, the variation of channel-to-channel matching of the total resistance from A to B is less than 1%. The device-to-device matching, however, can vary up to 30%. In the rheostat mode, the resistance has a positive temperature coefficient. The change in wiper-to-end terminal resistance over temperature is shown in Figure 2-8. The most variation over temperature will occur in the first 6% of codes (code 00h to 0Fh) due to the wiper resistance coefficient affecting the total resistance. The remaining codes are dominated by the total resistance tempco R_{AB}, typically 800 ppm/°C.

4.1.2 POTENTIOMETER MODE

In the potentiometer mode, all three terminals of the device are tied to different nodes in the circuit. This allows the potentiometer to output a voltage proportional to the input voltage. This mode is sometimes called voltage divider mode. The potentiometer is used to provide a variable voltage by adjusting the wiper position between the two endpoints as shown in Figure 4-3. Note that reversing the polarity of the A and B terminals will not affect operation.

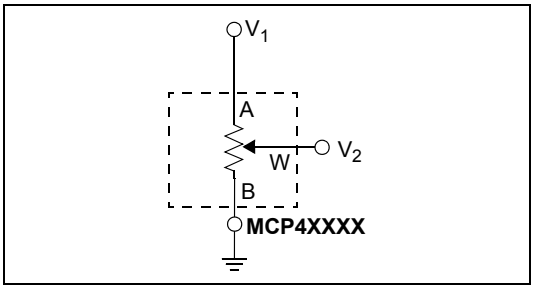


FIGURE 4-3: *Three terminal or voltage divider mode.*

In this configuration, the ratio of the internal resistance defines the temperature coefficient of the device. The resistor matching of the R_{WB} resistor to the R_{AB} resistor performs with a typical temperature coefficient of 1 ppm/°C (measured at code 80h). At lower codes, the wiper resistance temperature coefficient will dominate. Figure 2-3 shows the effect of the wiper. Above the lower codes, this figure shows that 70% of the states will typically have a temperature coefficient of less than 5 ppm/°C. 30% of the states will typically have a ppm/°C of less than 1.

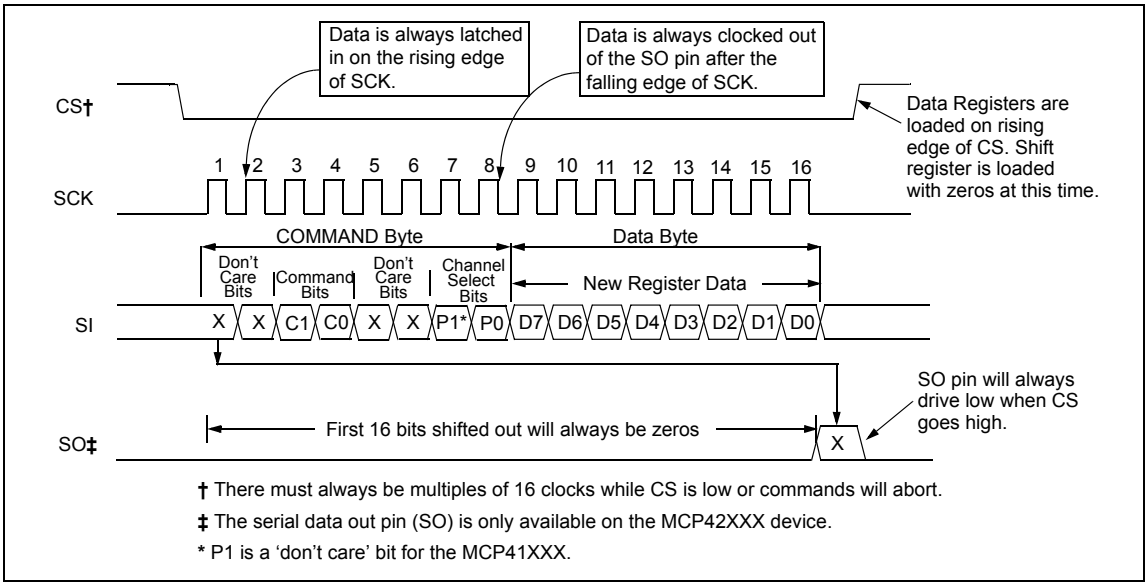
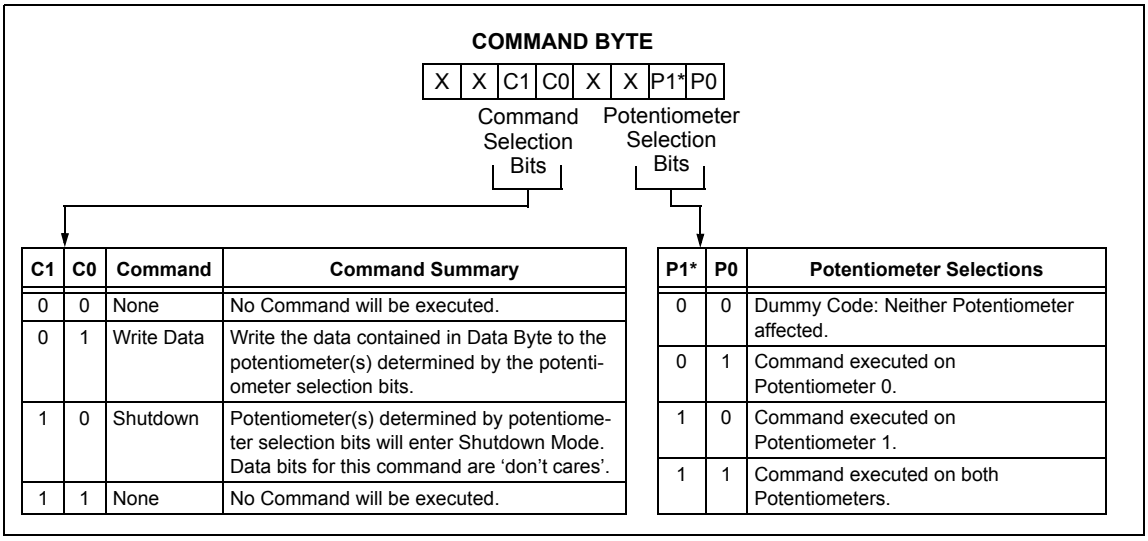


FIGURE 5-1: *Timing Diagram for Writing Instructions or Data to a Digital Potentiometer.*



C1	C0	Command	Command Summary
0	0	None	No Command will be executed.
0	1	Write Data	Write the data contained in Data Byte to the potentiometer(s) determined by the potentiometer selection bits.
1	0	Shutdown	Potentiometer(s) determined by potentiometer selection bits will enter Shutdown Mode. Data bits for this command are 'don't cares'.
1	1	None	No Command will be executed.

P1*	P0	Potentiometer Selections
0	0	Dummy Code: Neither Potentiometer affected.
0	1	Command executed on Potentiometer 0.
1	0	Command executed on Potentiometer 1.
1	1	Command executed on both Potentiometers.

FIGURE 5-2: *Command Byte Format.*