Simulation # 2

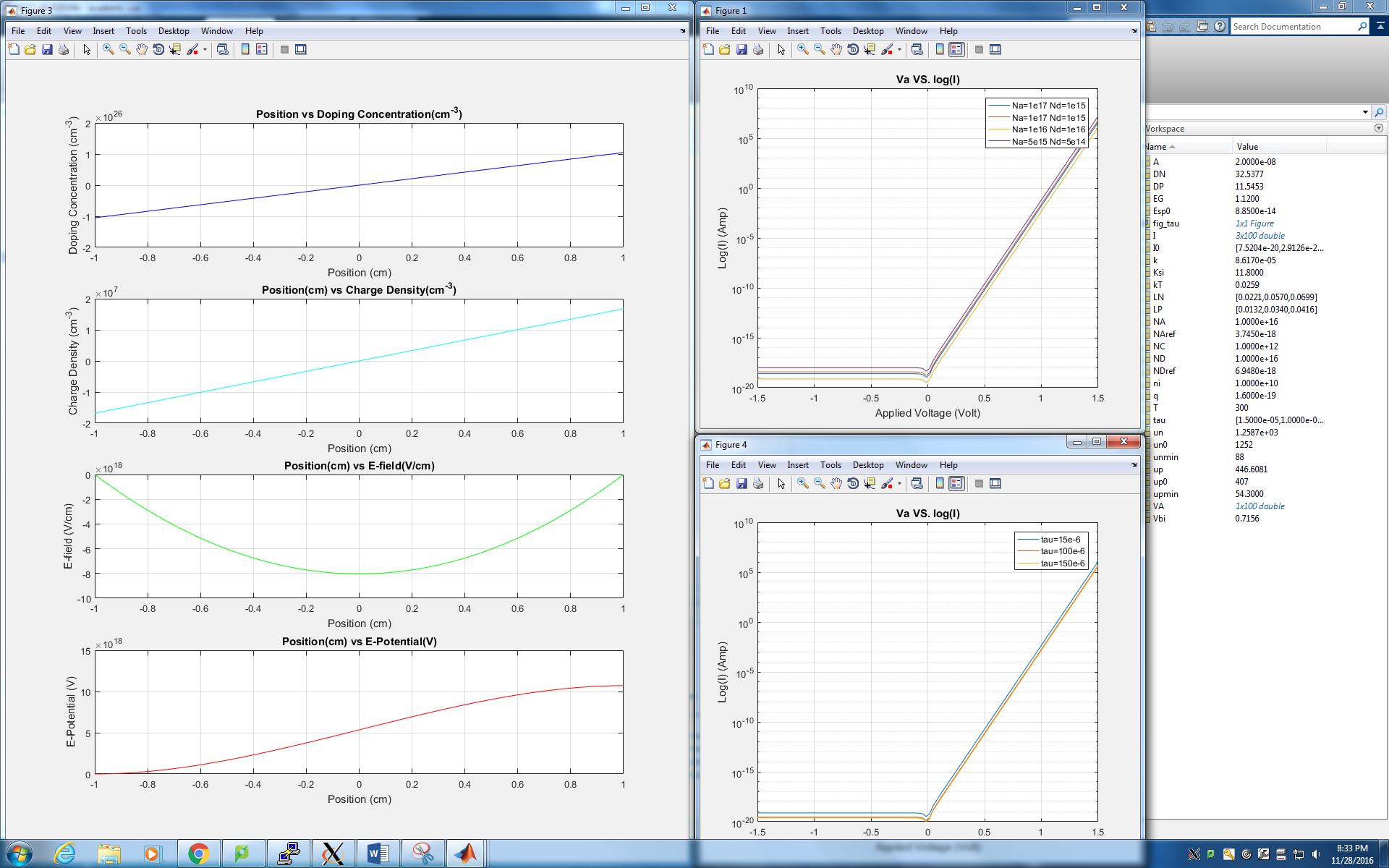
ECE416

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***Matlab***



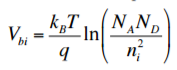
In portion of the simulation, an ideal diode is assumed. Its behaviors are mathematically derived as referred by the textbook. The image above shows a screenshot of the *Matlab* ­simulation output figures.

**A)**

Reverse Saturation Current, Zero-bias Junction Capacitance, Junction Capacitance at   
-3V Bias, and Built-in Voltage of four different unique ideal diodes are investigated via *Matlab* simulation.

All the mentioned properties are a unique constant to a doping profile. A relationship between a doping profile and a property can be mathematically represented by the following set of equations:

Build-in Voltage:



A Built-in voltage results from juxtaposition of a N-type and a P-type which causes the loss of charge neutrality at the junction creating a “depletion region.”

Capacitance

A capacitance of a semiconductor device is a direct reverse proportion to a width of depletion region which causes by the defect of charge carrier around the P-N junction.  
A capacitance can be calculated using

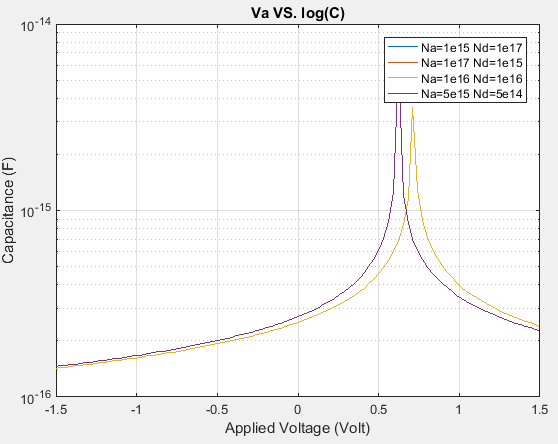


And a width of depletion region can be calculated by



Where Vbi is a Built-In voltage; Va is an Applied Voltage

To calculate for a capacitance at a different bias, you can simply replace Va with the desire applied voltage. Va = 0 volts for a zero-bias junction capacitance and Va = -3 volts for a 3V reverse bias.



Saturation Current

From the first simulation assignment, we recall that a current in a semiconductor device depends on the charge carrier mobility which is a function of dopant concentrations. In our case, a semiconductor mobility expressions are

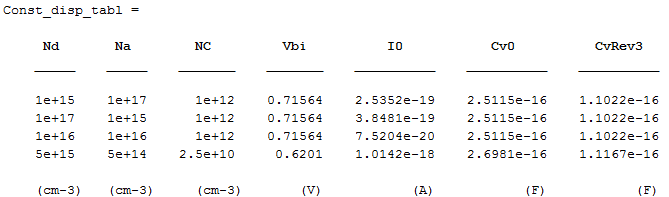
Hence, we can calculate the Saturation Current using an equation:



Where

 (Einstein Equation) (Minority Carrier Diffusion Length)

*Result of the computations:*



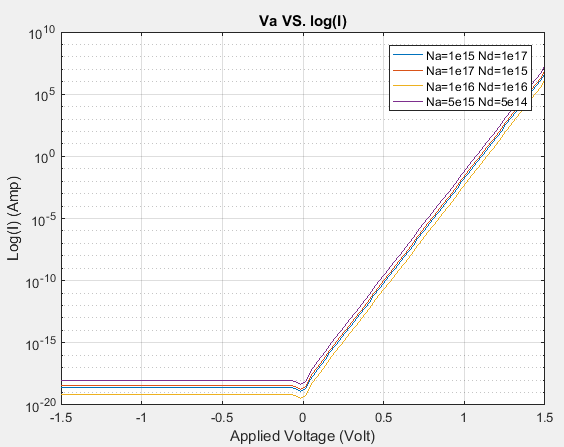
**B)**

This section of *Matlab* simulation a relationship between a bias voltage and a device current is going to be investigated. Four different ideal diodes each with a different doping profile are undergone a simulation and observed to obtain relationship.

We obtain the saturation current from part A, we can find a junction current using



When we put it all together, we obtain a relationship between Applied Voltage and Device Current. A figure below shows the Va-I relationship of a different doping profile.



The current of the is not solely determined by the net dopant concentrations but also the charge carrier mobility and the average minority carrier lifetime. As you can observe from the first three dopant profiles where all the net dopant concentrations and average minority carrier lifetime are the same, the device current varies in respond to a different charge carrier mobility. Thus, it results in different non-overlapping lines each represents a different doping profile. In the reverse bias region (Va < 0), the current flow in the device is not impacted by the applied voltage because the minority charge carrier cannot be depleted below zero. As a result, Va remains a constant at the magnitude of reverse saturation current. On the other hand, in response to forward bias (Va > 0), the current responds to an increasing applied voltage exponentially which results in a linear positive slop in V-log(I) graph with the slop of .

It is worth notetaking that the V-log(I) graph above takes an absolute value of the current to do the log-plot due to a negative current when a negative voltage is applied – a log() cannot handle a negative input value.

**C)**

In the earlier sections of the *Matlab* simulation, we assume semiconductors are doped uniformly, but in reality uniformly doped can be very difficult to achieve. In this section of *Matlab* simulation, we are investigating in a gradian doped silicon and how its properties reflect the change in dopant concentrations. The given problem has a gradian doped silicon with a gradian constant of 2020 cm -4 (a = 2020 cm -4 )

From the Linearly Graded Junction equation:

We can obtain the graded doping profile; hence, we can determine the charge density with respect to position.

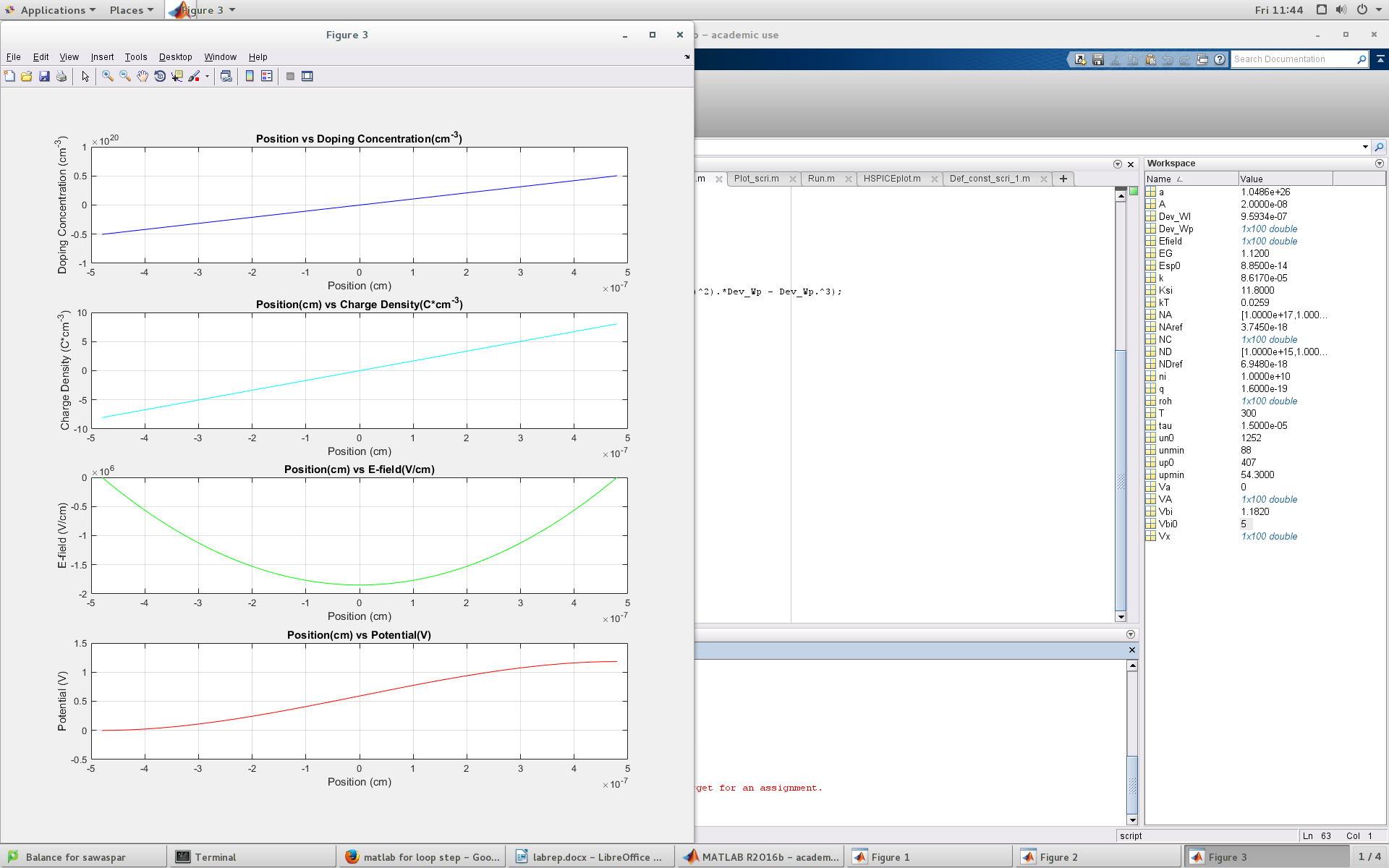
The width of the depletion region changes due to the doping grading on a piece of silicon. By referring to book page 223, one can obtain the width and built-in voltage of the device. From there, we use Poisson’s equation to obtain the relationship between charge density and Electric field given the charge density is symmetric at x=0.

Recall that E-field is defined as

We can take an integral with respect to x to obtain a relationship between E-field and potential in term of position.

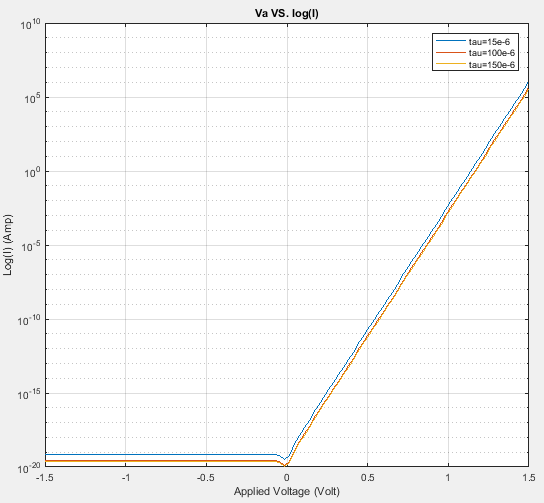
The graph on the next page shows the relationship between each of the properties with respect to position.

Where is referred as “Doping Concentration” (cm-3)  
 is referred as “Charge Density” (C/cm-3)   
 is referred as “Electric Field” (V/cm)   
 is referred as “Potential” (V)



**D)**

In this portion of *Matlab*, the effect of average minority carrier lifetime on current is investigated over a sweep of voltage. To do so, the silicon is doped with the third doping profile (Na=1e-16, Nd=1e-16) and measure the current in respond to a sweep of voltage range. The graph below show the result of a simulation.



As one can recognize, the graph retains the same shape as the graph (1.B) which is a plot of



Recall:

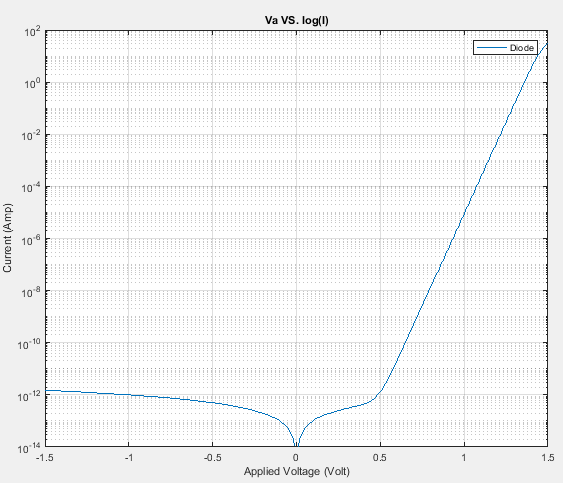
 

Hypothetically, the reverse saturation current should decrease as the value of minority carrier lifetime increases (). From our graph inspection, the least tau value, =15e-6, has the highest saturation current among all the value of which agrees with our hypothesis. The smaller minority carrier lifetime, the faster the minority carrier gets absorbed, the shorter a diffusion length, the lesser minority carrier gets to piled up, the lesser increase in net current.

***SPICE***

To further investigate in our V-log(I) relationship, we use “hspice” and a diode netlist to observe V-I behavior of a diode with the third doping profile (Na=1e-16, Nd=1e-16). Assumptively, the V-I graph should be the same for the same material regardless of the simulators. The result of hspice proves the assumption to be wrong.

Hspice simulates the V-I behavior using recursion method. It computes the initial values, use them to calculate for the output, then use the output values as initial conditions for the next stage. This method of calculation allows hspice to closely mimic a real physical device. Thus, the hspice simulates a NONE-ideal diode in contrast to an ideal diode which simulated using Matlab.



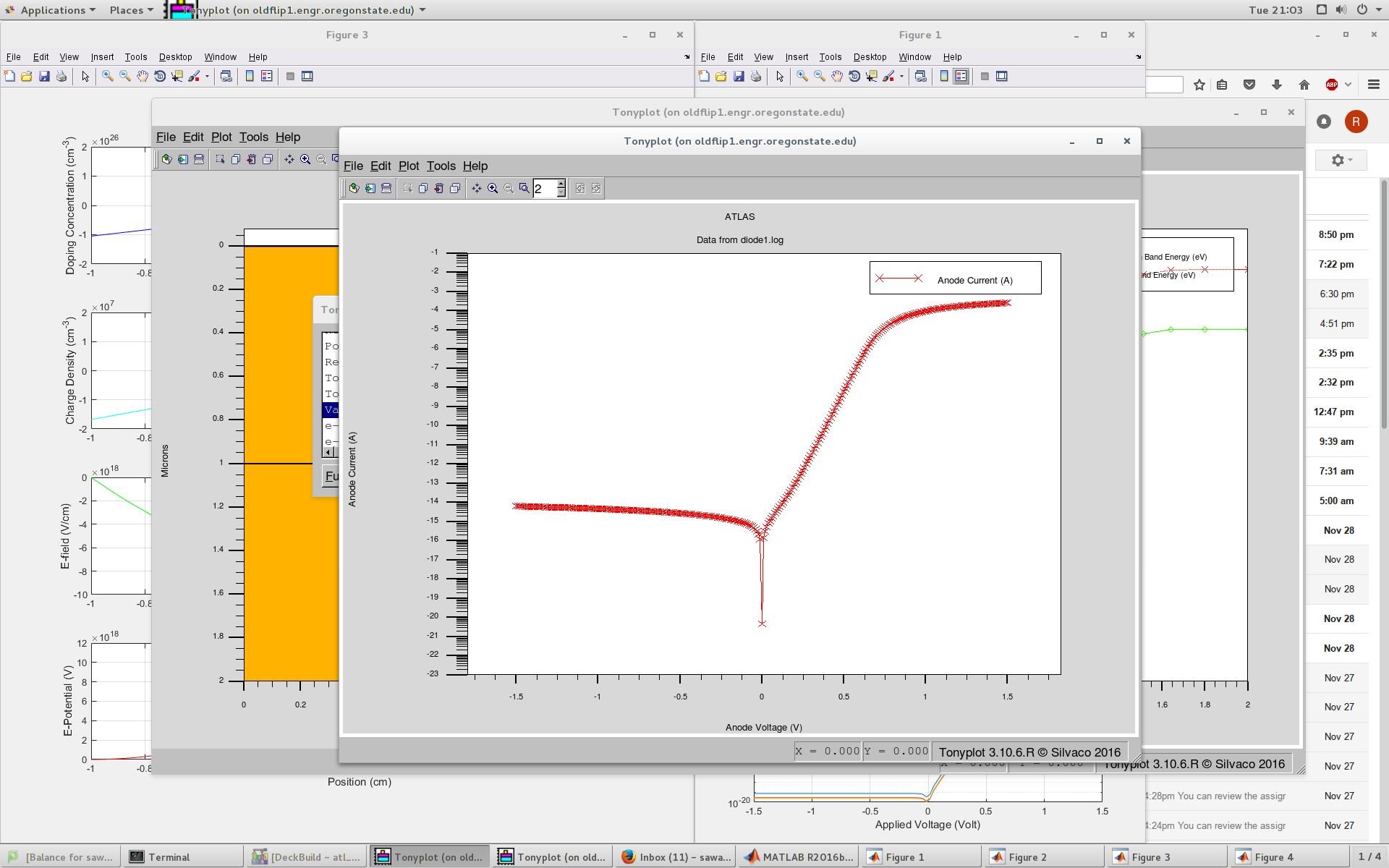
The current of hspice none-ideal diode simulation has an order of magnitude higher than a Matlab ideal diode. It is because the Matlab script assumed an ideal diode without carrier generation and recombination. The carrier RG affects the device current. In the reverse bias region (Va < 0), the PN-junction is in a great deficit of a carriers; the carrier generation takes place which increases the reverse current. While in the forward bias region (Va > 0), the PN-junction has a great excess carrier; the carrier recombination takes place which increases the forward current. Thus, the RG process increases the current magnitude in a semiconductor.

***ATLAS***

**A)**

This is another V-I plot from another simulator: Atlas. It still has the same plot shape with a very similar value. Notice the saturation current is slightly less than the one from hpsice. It is due to the sensitivity of the simulator. Hspice takes in only three parameters (I­o, C0v, and Vj) and tries its best to create the V-log(I) relationship which may cause an overshoot in the saturation current. On the other hand, ATLAS uses a very complex, high fidelity simulation method which takes in account of other factoring variables resulting in a slightly different order of magnitude in the saturation current.

The plot below shows a relationship between Anode Voltage (V) and Log of Anode Current (Amp) generated from ATLAS simulator.



Ideal region

Forward Bias

High Doping Effect

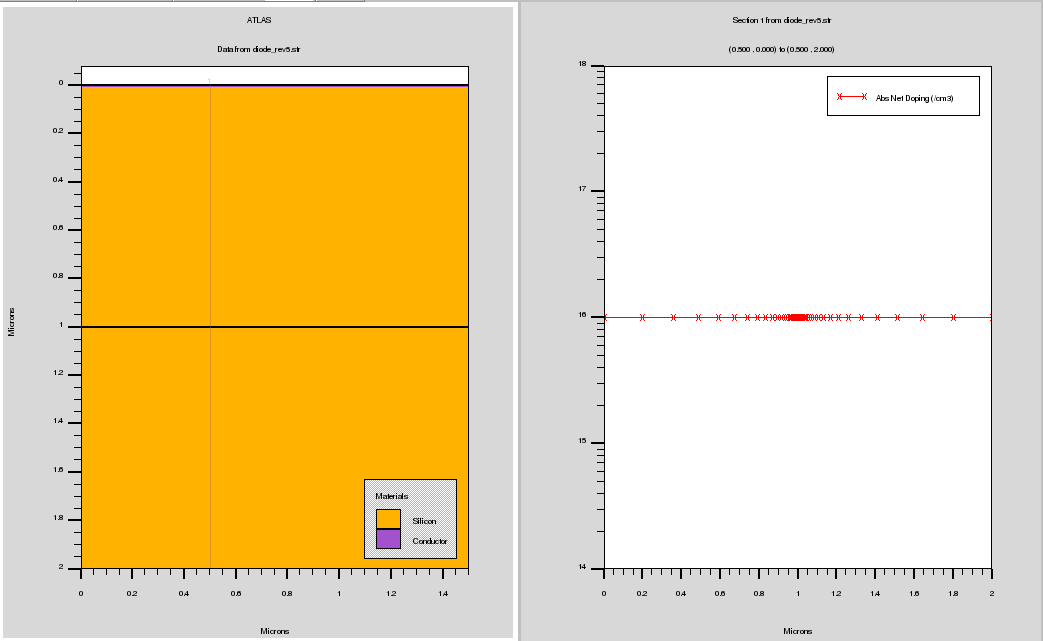
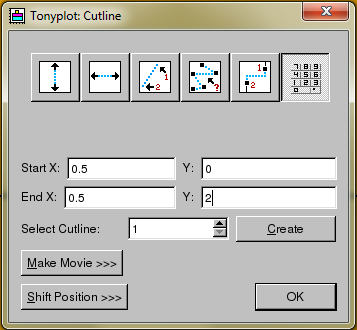
Series R

Reverse Bias

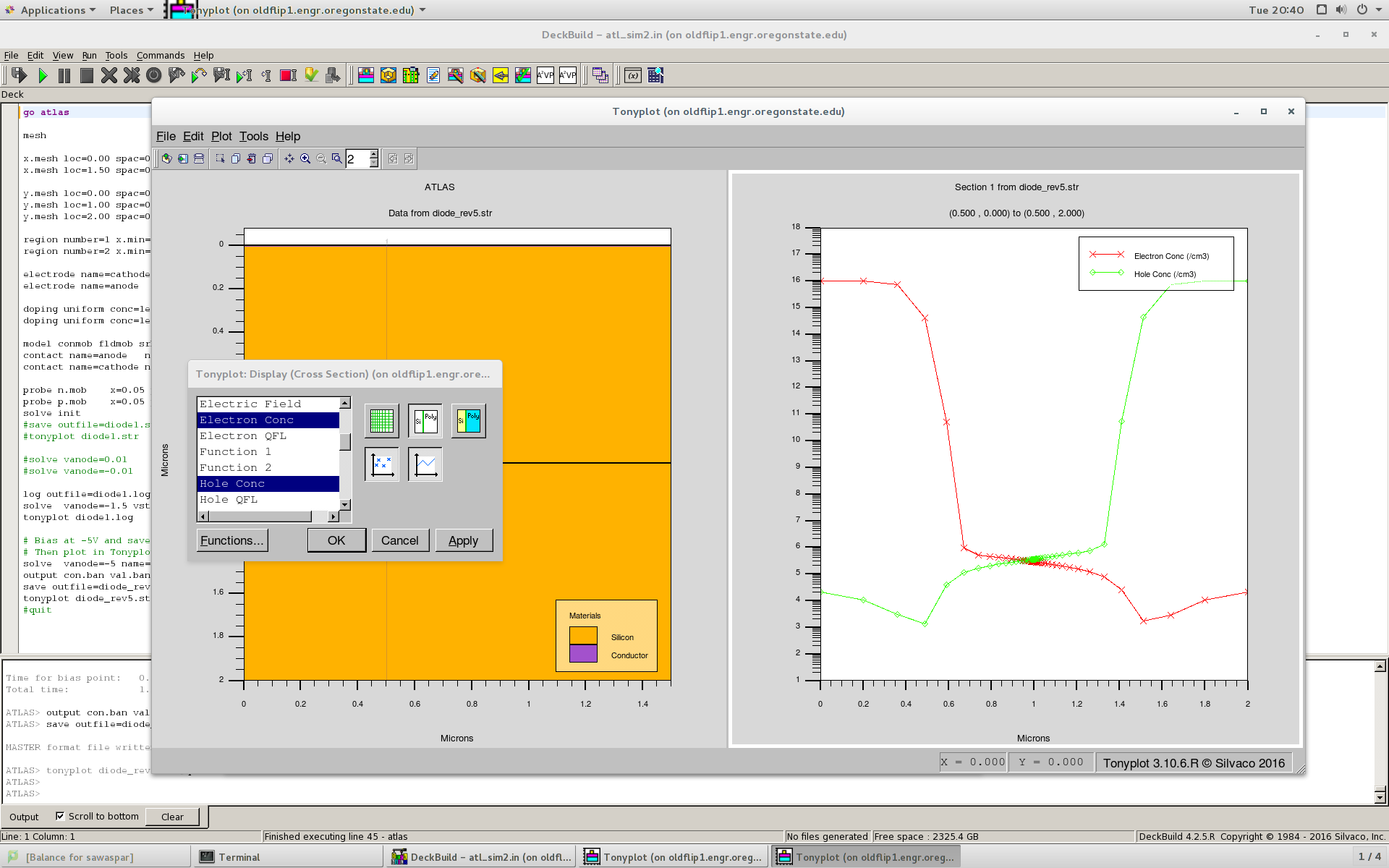
Avalanche

The graph is labelled with different state of the device in response to an applied voltage. The V-I curve starts off with Avalanche region in an area with a high negative applied voltage. The high negative Va causes drop between band gap to be very high and when a charge carrier jump over, it falls hard that it causes the nearby dopants to be ionized. The Reverse Bias region is a result from negative Va causing the junction to be severely lacked of mobile charge carrier. The Forward Bias region results from positive applied voltage making the junction to have excess minority carrier piling up. The Ideal diode region is where the PN-junction behaves like an ideal diode. Once the voltage starts to get higher, we get into High Doping Effect where the mobile carriers are going crazy and starting to ionized others around it. Lastly, our diode burnt out becoming a resistor.

**B)** Atlas has a cool feature that allows you to cut-up a piece of doped silicon and measure a different parameter values. So we cut the Si at x=0.5 from y=[0,2]



*Mobile Carrier Concentrations vs Position:*

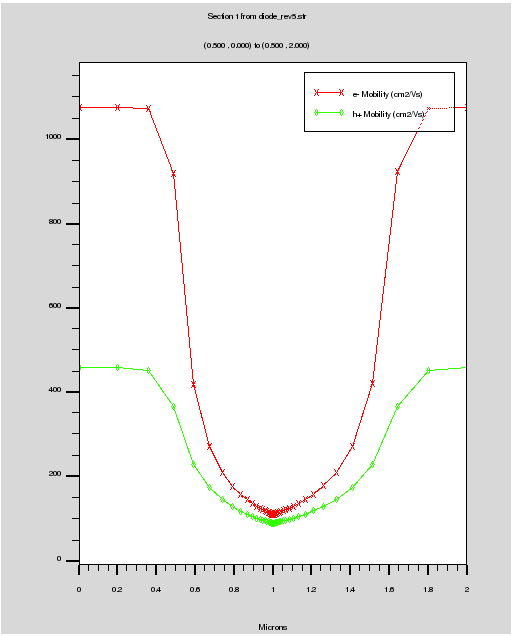


After cutting the silicon open, we have ATLAS plotted the concentrations of mobile carriers which are concentration of holes and electrons. They are NOT donor/acceptor concentrations because the dopants are not mobile.

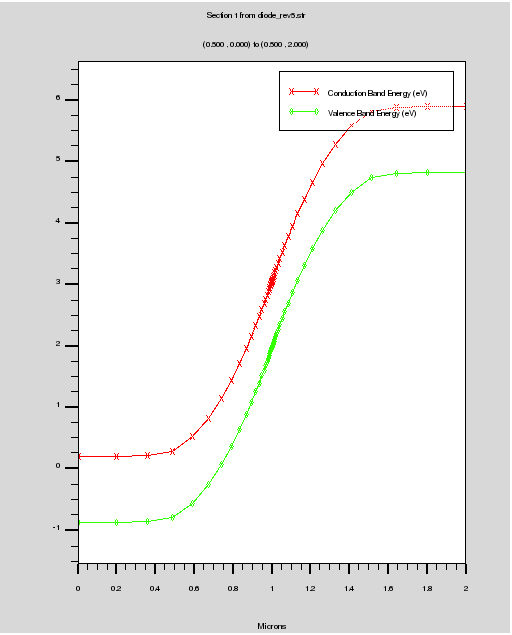
From looking at the carrier concentration graph, you can tell that the device is undergoing a reverse bias because there is a severe lack of carrier at the depletion region (at the junction) of the device – both e- and h+ concentrations drop. Furthermore, you can also tell the device has its N-type on the left-hand side and P-type on the right-hand side. e- concentration is higher than h+ concentration on the left-hand side indicates an N-type semiconductor. Likewise, for P-type when h+ concentration is higher than e- concentration.

Further analysis can be done to determine the applied voltage:

*Carrier Mobility: [NOT PART OF THE PROBLEM BUT COOL TO LOOK AT]*

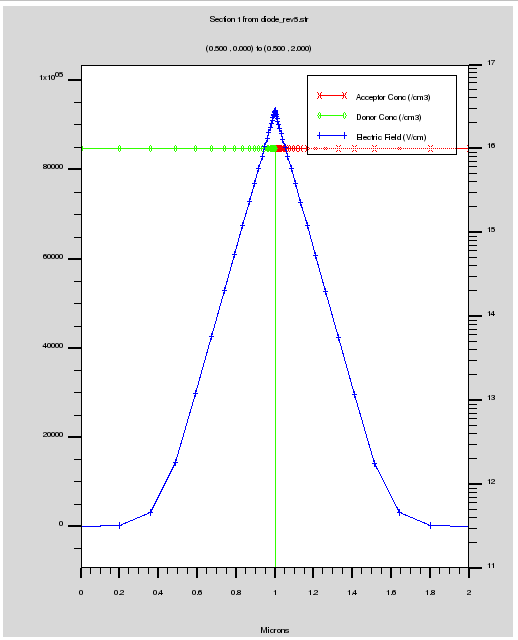


They are having a rough time going across the depletion region while undergoing a reverse bias. [It’s a trap!]



*Energy Bands VS Position:*

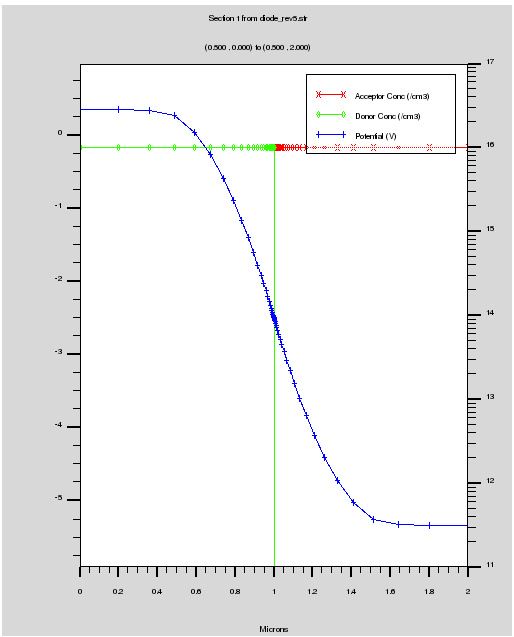
The graph shows a stretch out gap between the energy level of conduction/valance band between the N-type and P-type. The gap is enlarged as the device is undergoing a reverse bias. More specifically, the energy gap increases from to be   
 which is an increase with the magnitude of 5q.



*Electric Field VS Position:*

As mathematically shown in Matlab part 1.C,  
the electric field is directly proportion to the charge density within the depletion region.   
  
Since the device is undergoing a reverse bias, the depletion region behaves like a sinkhole and pulling in a great amount of charge carrier causing a spike of the electric field at the junction.

Note the green line and the red line are Donor (N-type) and Acceptor(P-type) concentration respectively. They are meant to provide you with a relative position.

*Potential VS Position:*

Recall:

To obtain an electric potential you simply integrate the given equation and solve for V.

Notice that across the depletion region, the voltage across the device is slightly greater than 5V – [0.3, -5.3]. We recall that any doped semiconductor device has a built-in voltage of Vbi. Incorporating the Vbi=0.7 V with our biasing voltage of -5 V, we get the net voltage drop across our device of approximately 5.7 V. The graph reflects the phenomenon in the overall voltage drop.