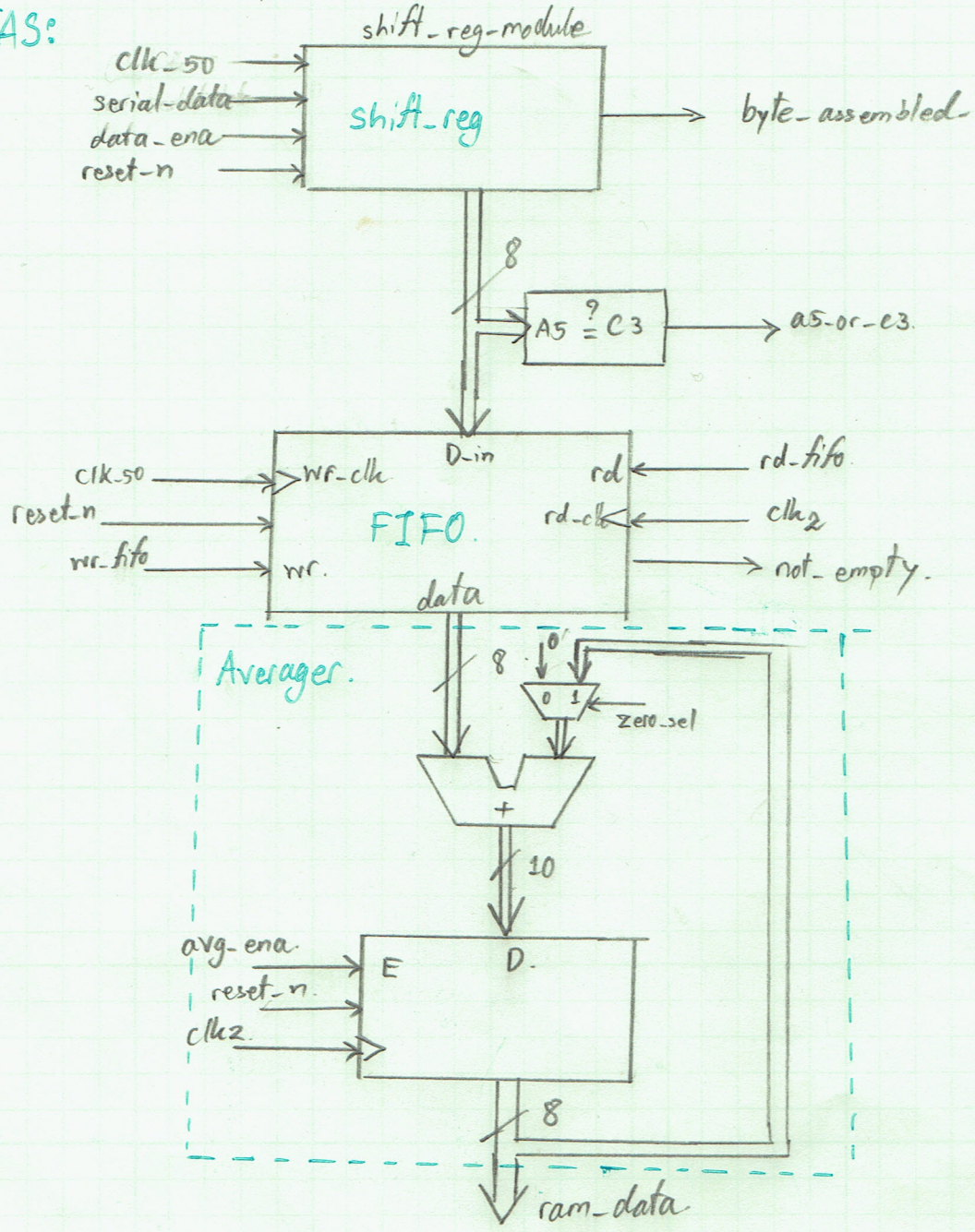
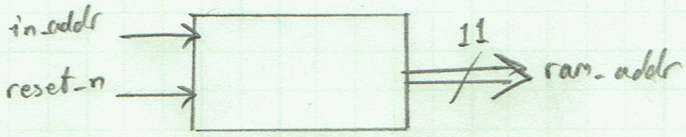
Block Diagram.

TAS:

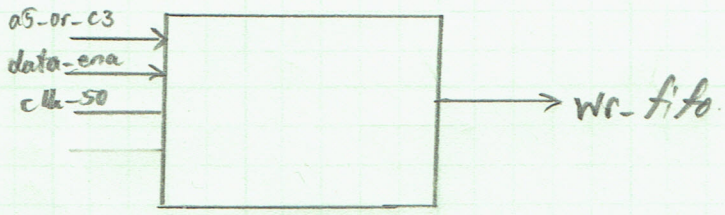


ram_addr:

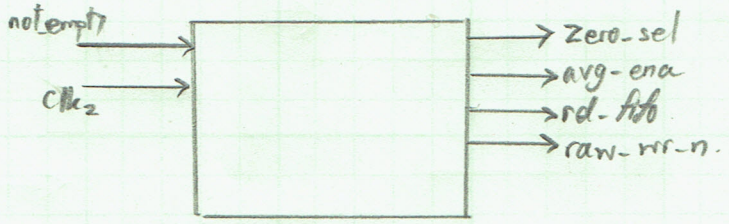


Control Block:

ctrl_50MHz:



ctrl_2MHz:



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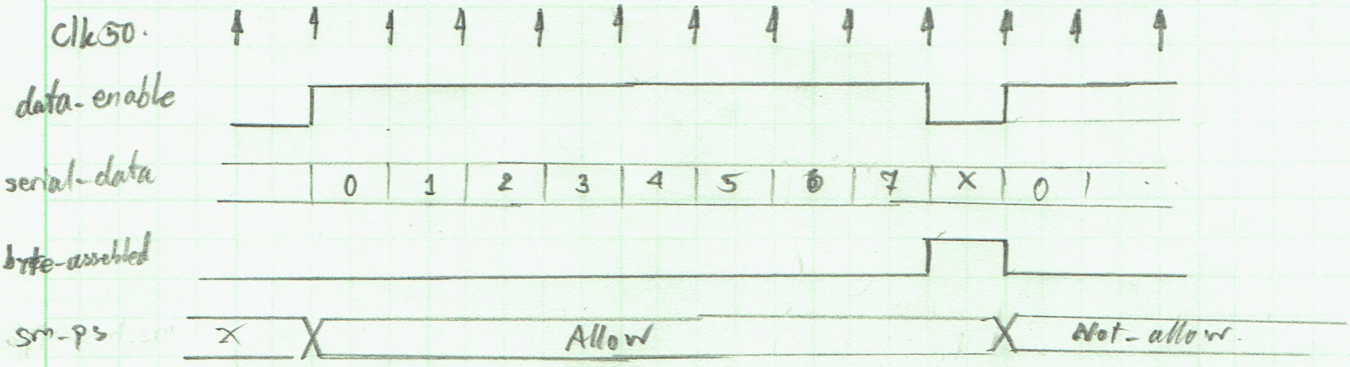
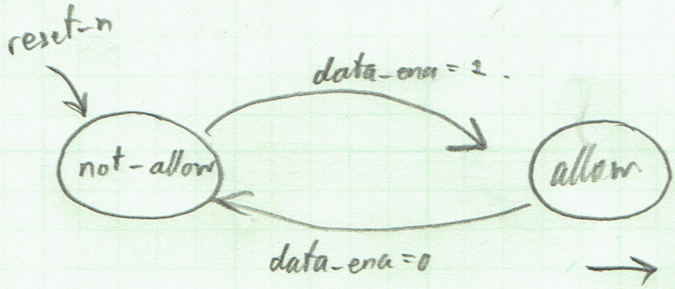


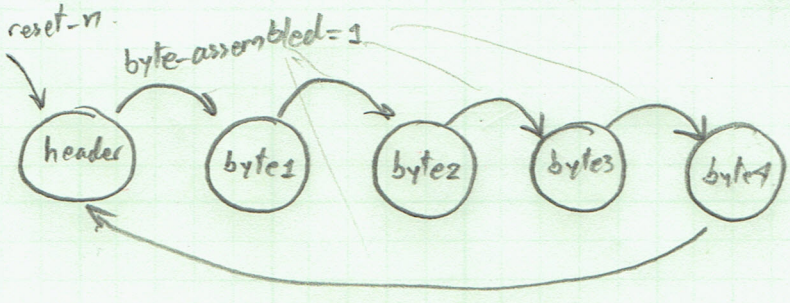
State Machine.

sm:

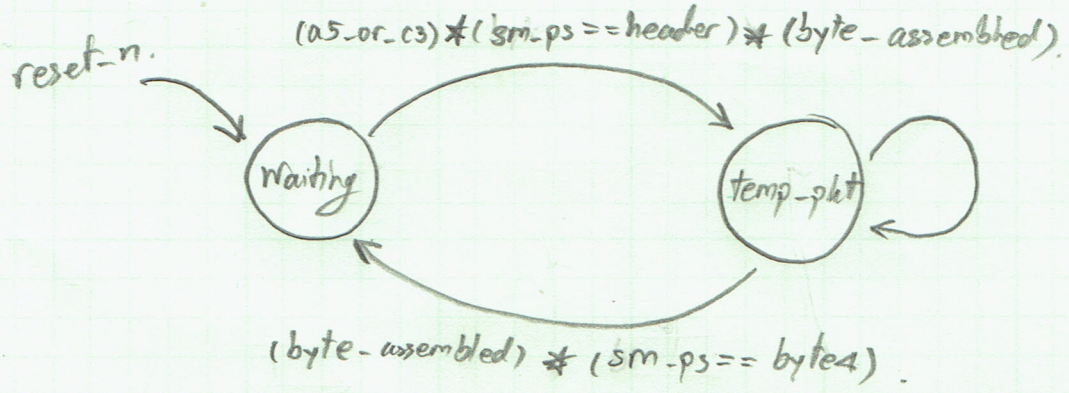


→ byte_assembled
= (sm_ps == Allow)
* (data_ena == 0)

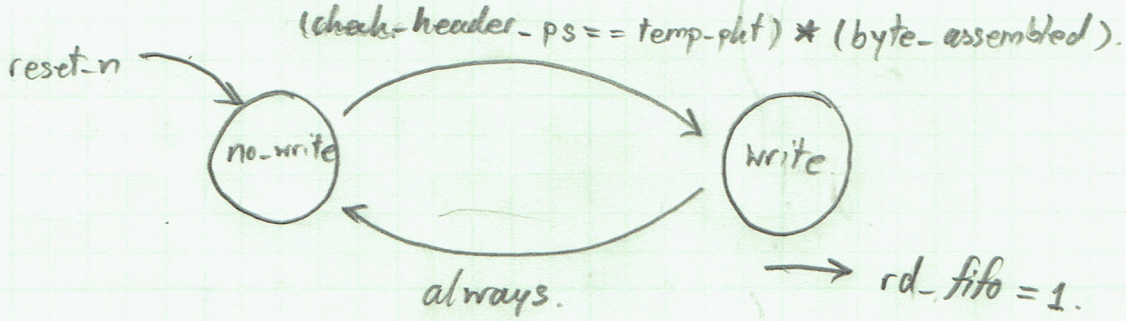
byte_count_sm:



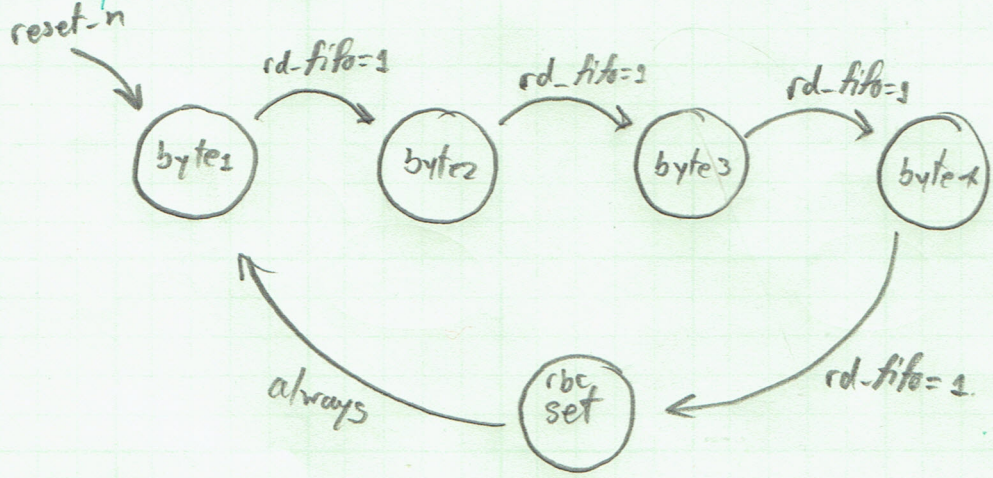
check_header_sm:



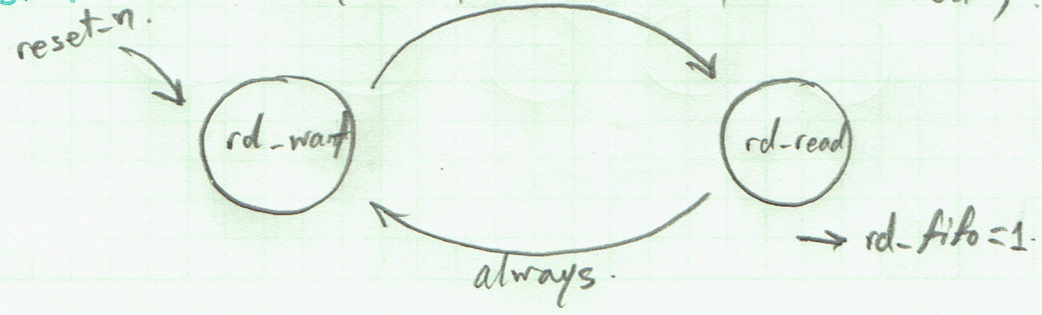
wr_sm:



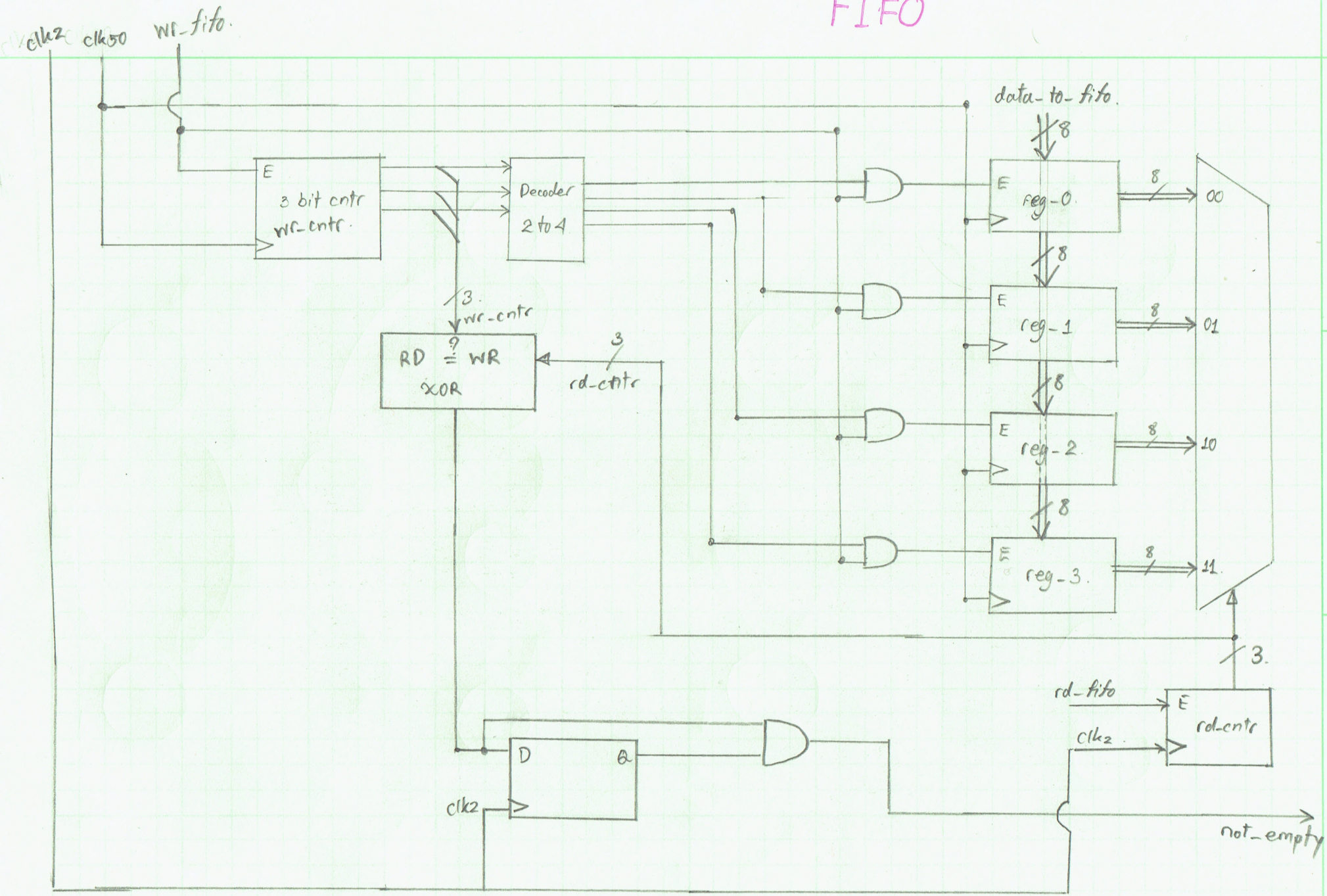
read_byte_sm: rbc



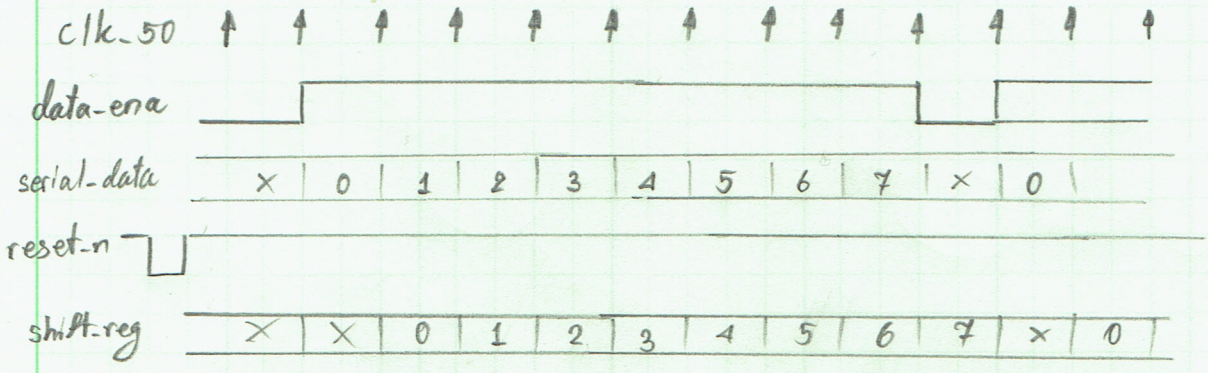
rd_wt_sm:



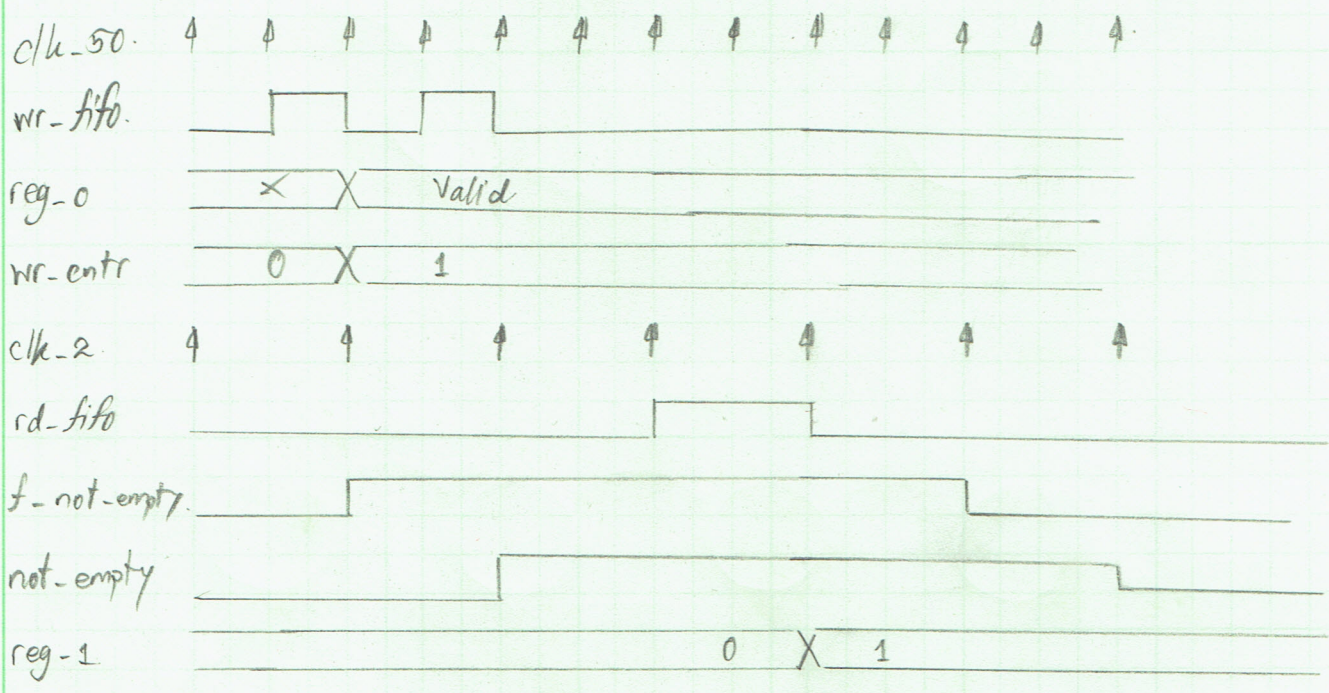
FIFO


clk2
clk50
wr_fifo
data_to_fifo
8
E
3 bit cntr
wr_cntr
Decoder
2 to 4
3
wr_cntr
RD = ? WR
XOR
3
rd_cntr
E
reg_0
reg_1
reg_2
reg_3
8
00
01
10
11
3
rd_fifo
clk2
E
rd_cntr
D
Q
clk2
not_empty

Shift_reg_module. Timing.



FIFO Timing.



Ctrl_2MHz Timing.