Manamania	Instruction code		Clocks	/instruct	on (42ns	/clock)	Evalenation
Mnemonic	D7 D6 D5 D4 D3 D2	D1 D0	8051	0 WAIT	1 WAIT	PAR.	Explanation
ADD A,Rn	0 0 1 0 1 n2	n1 n0	12	2	4	2 or 4	(A)<(A)+(Rn)
ADD A,direct	0 0 1 0 0 1	0 1	12	2	6	4	(A)<(A)+(direct)
	a7 a6 a5 a4 a3 a2	a1 a0					
ADD A,@Ri	0 0 1 0 0 1	1 i	12	2	4	2 or 4	(A)<(A)+((Ri))
ADD A,#data	0 0 1 0 0 1	0 0	12	2	6	4	(A)<(A)+#data
	d7 d6 d5 d4 d3 d2	d1 d0					
ADDC A,Rn	0 0 1 1 1 n2	n1 n0	12	2	4	2 or 4	(A)<(A)+(Rn)+(C)
ADDC A,direct	0 0 1 1 0 1	0 1	12	2	6	4	(A)<(A)+(direct)+(C)
	a7 a6 a5 a4 a3 a2	a1 a0					
ADDC A,@Ri	0 0 1 1 0 1	1 i	12	2	4	2 or 4	(A)<(A)+((Ri))+(C)
ADDC A,#data	0 0 1 1 0 1	0 0	12	2	6	4	(A)<(A)+#data+(C)
	d7 d6 d5 d4 d3 d2	d1 d0					
SUBB A,Rn	1 0 0 1 1 n2	n1 n0	12	2	4	2 or 4	(A)<(A)-(Rn)-(C)
SUBB A,direct	1 0 0 1 0 1	0 1	12	2	6	4	(A)<(A)-(direct)-(C)
	a7 a6 a5 a4 a3 a2	a1 a0					
SUBB A,@Ri	1 0 0 1 0 1	1 i	12	2	4	2 or 4	(A)<(A)-((Ri))-(C)
SUBB A,@Ri SUBB A,#data	1 0 0 1 0 1	0 0	12	2	6	4	(A)<(A)-#data-(C)
	d7 d6 d5 d4 d3 d2	d1 d0					
INC A	0 0 0 0 0 1	0 0	12	2	4	2 or 4	(A)<(A)+1
INC Rn	0 0 0 0 1 n2	n1 n0	12	2	4	2 or 4	(Rn)<(Rn)+1
INC direct	0 0 0 0 0 1	0 1	12	2	6	4	(direct)<(direct)+1
	a7 a6 a5 a4 a3 a2	a1 a0					
INC @Ri	0 0 0 0 0 1	1 i	12	2	4	2 or 4	((Ri))<((Ri))+1
INC DPTR	1 0 1 0 0 0	1 1	24	4	4	4	(DPTR)<(DPTR)+1
DEC A	0 0 0 1 0 1	0 0	12	2	4	2 or 4	(A)<(A)-1
DEC Rn	0 0 0 1 1 n2	n1 n0	12	2	4	2 or 4	(Rn)<(Rn)-1
DEC direct	0 0 0 1 0 1	0 1	12	2	6	4	(direct)<(direct)-1
	a7 a6 a5 a4 a3 a2	a1 a0					
DEC @Ri	0 0 0 1 0 1	1 i	12	2	4	2 or 4	((Ri))<((Ri))-1
MUL AB	1 0 1 0 0 1	0 0	96	8	8	8	(B),(A)<(A)x(B) B <msb a<lsb<="" td=""></msb>
DIV AB	1 0 0 0 0 1	0 0	96	8	8	8	(A),(B)<(A)/(B) A <q b<r<="" td=""></q>
DA A	1 1 0 1 0 1	0 0	12	2	4	2 or 4	Contents A=BCD , use ADD or ADDC with BC
							If flags not modified DA A will adjust
							result to BCD
ANL A,Rn	0 1 0 1 1 n2	n1 n0	12	2	4	2 or 4	(A)<(A) AND (Rn)
ANL A,direct	0 1 0 1 0 1	0 1	12	2	6	4	(A)<(A) AND (direct)
	a7 a6 a5 a4 a3 a2	a1 a0					
ANL A,@Ri	0 1 0 1 0 1	1 i	12	2	4	2 or 4	(A)<(A) AND ((Ri))
ANL A,#data	0 1 0 1 0 1	0 0	12	2	6	4	(A)<(A) AND #data
	d7 d6 d5 d4 d3 d2	d1 d0					
ANL direct,A	0 1 0 1 0 0	1 0	12	2	6	4	(direct)<(direct) AND (A)
<u> </u>	a7 a6 a5 a4 a3 a2	a1 a0					
ANL direct,#data	0 1 0 1 0 0	1 1	24	4	10	6 or 8	(direct)<(direct) AND #data
	a7 a6 a5 a4 a3 a2	a1 a0					
	d7 d6 d5 d4 d3 d2	d1 d0					
ORL A,Rn	0 1 0 0 1 n2	n1 n0	12	2	4	2 or 4	(A)<(A) OR (Rn)
ORL A,direct	0 1 0 0 0 1	0 1	12	2	6	4	(A)<(A) OR (direct)
1	a7 a6 a5 a4 a3 a2	-1 -0	I				

					Inst	ruct	ion	cod	e		Cloc	ks/ins	truct	ion (42ns	/clock)	
	Mnemonic	D7	7 D	6	D5	D4	D3	B D	2 [	D1 D0	805	1 0\	WAIT	1 WAIT	PAR.	Explanation
	ORL A,@Ri	0	:	1	0	0	0	1		1 i	12		2	4	2 or 4	(A)<(A) OR ((Ri))
	ORL A,#data	0	:	1	0	0	0	1		0 0	12		2	6	4	(A)<(A) OR #data
		d7	7 d	6	d5	d4	d3	d d	2 (	d1 d0	)					
	ORL direct,A	0	:	1	0	0	0	C	)	1 0	12		2	6	4	(direct)<(direct) OR (A)
		a7	' a	6	a5	a4	a3	a	2 a	a1 a0	)					
	ORL direct,#data	0	:	1	0	0	0	C	)	1 1	24		4	10	6 or 8	(direct)<(direct) OR #data
		a7	' a		a5	a4				a1 a0						
		d7			d5	d4		3 d		d1 d0	-		_			4.1 4.1
	XRL A,Rn	0		1	1	0	1		2 r		+	-	2	4	2 or 4	(A)<(A) XOR (Rn)
	XRL A,direct	0		1	1	0	0	1		0 1			2	6	4	(A)<(A) XOR (direct)
	VDL A @D:	a7			a5	a4				a1 a0	+	+	2	4	2 - 11 4	(A) (A) VOD ((Bi))
	XRL A,@Ri XRL A,#data	0		1	1	0	0	1		1 i 0 0	+	+	2	4	2 or 4	(A)<-(A) XOR ((Ri))
	XKL A,#data	d7		1	1 d5	d4				0 0 d1 d0			2	6	4	(A)<(A) XOR #data
suc	XRL direct,A	0		1	u5 1	0	0	, u		1 0			2	6	4	(direct)<(direct) XOR (A)
ructi	ARE direct,A	a7			т a5	a4				1 0 a1 a0			2	0	4	(unect)<(unect) XOK (A)
Logical instructions	XRL direct,#data	0		1	1	0	0	C		1 1	24	+	4	10	6 or 8	(direct)<(direct) XOR #data
gical	Ante an eec, naded	a7			ъ а5	a4				a1 a0			•		0 01 0	(direct) (direct) Northadta
2		d7			d5	d4				d1 d0						
	CLR A	1		1	1	0	0			0 0	+	+	2	4	2 or 4	(A)<0
	CPL A	1	:	1	1	1	0	1		0 0	+		2	4	2 or 4	ONES COMPLEMENT OF (A)
	RL A	0	(	)	1	0	0	C	)	1 1	12	+	2	4	2 or 4	rotate 1 bit left
																A7   A6   A5   A4   A3   A2   A1   A0
	RLC A	0	(	)	1	1	0	C	)	1 1	12		2	4	2 or 4	rotate 1 bit left
																C A7 A6 A5 A4 A3 A2 A1 A0
	RR A	0	(	)	0	0	0	C	)	1 1	12		2	4	2 or 4	rotate 1 bit right
																A7   A6   A5   A4   A3   A2   A1   A0
	RRC A	0	(	)	0	1	0	C	)	1 1	12		2	4	2 or 4	rotate 1 bit right
																C A7 A6 A5 A4 A3 A2 A1 A0
	SWAP A	1	:	1	0	0	0	1	_	0 0	12		2	4	2 or 4	A7 A6 A5 A4 A3 A2 A1 A0
		-														A7 A6 A5 A4 A3 A2 A1 A0
	MOV A,Rn	1		1	1	0	1			n1 n(	+		2	4	2 or 4	(A)<(Rn)
	MOV A,direct	1		1	1	0	0	. 1		0 1			2	6	4	(A)<(direct)
	MAON A OD:	a7			a5	a4				a1 a0			2	4	2 - 11 4	(A) c ((D;))
	MOV A,@Ri	1		1	1	0	0	1		1 i 0 0	+		2	4	2 or 4	(A)<((Ri)) (A)<#data
ions	MOV A,#data	0 d7		1  6	1 d5	1 d4	0 d3			0 0 d1 d0			2	6	4	(A)<#add
truct	MOV Rn,A	1		1	1	1	1			n1 n(	+		2	4	2 or 4	(Rn)<(A)
Data transfer instructions	MOV Rn,direct	1		)	1	0	1			n1 n0	+	+	4	8	6	(Rn)<(direct)
ansfe	= 1, a cot	a7			ъ а5					a1 a0			-			(, - (225)
ta trė	MOV Rn,#data	0		1	1	1	1			n1 n(	+	+	2	6	4	(Rn)<#data
Dat			7 d		d5	d4				d1 d0						(,
	MOV direct,A	1		1	1	1	0			0 1	-	+	2	6	4	(direct)<(A)
		a7			a5		a3			a1 a0						. , , ,
	MOV direct,Rn	1	(	)	0	0	1			n1 n0	+		4	8	6	(direct)<(Rn)
		a7		_	a5					a1 a0	.1			Ī		I

Mnemonic	Instruction code	Clocks	/instruct	ion (42ns	/clock)	Explanation
Willemonic	D7 D6 D5 D4 D3 D2 D1 C	0 8051	0 WAIT	1 WAIT	PAR.	Explanation
MOV direct1, direct2	1 0 0 0 0 1 0	24	4	10	6 or 8	(direct1)<(direct2)
	2a7 a6 a5 a4 a3 a2 a1 a	0				
	1a7 a6 a5 a4 a3 a2 a1 a	0				
MOV direct,@Ri	1 0 0 0 0 1 1	24	4	8	6	(direct)<((Ri))
	a7 a6 a5 a4 a3 a2 a1 a	0				
MOV direct,#data	0 1 1 1 0 1 0	L 24	4	10	6 or 8	(direct)<#data
	a7 a6 a5 a4 a3 a2 a1 a	0				
	d7 d6 d5 d4 d3 d2 d1 c	0				
MOV @Ri,A	1 1 1 1 0 1 1	12	2	4	2 or 4	((Ri))<(A)
MOV @Ri,direct	1 0 1 0 0 1 1	24	4	8	6	((Ri))<(direct)
	a7 a6 a5 a4 a3 a2 a1 a	0				
MOV @Ri,#data	0 1 1 1 0 1 1	12	2	6	4	((Ri))<#data
	d7 d6 d5 d4 d3 d2 d1 c	0				
MOV DPTR,#data	1 0 0 1 0 0 0	24	4	10	6 or 8	(DPTR)<#data16
	d15 d14 d13 d12 d11 d10 d9 d	8				or: (DPH) <high #data16="" and<="" td=""></high>
	d7 d6 d5 d4 d3 d2 d1 c	0				(DPL) <low #data16<="" td=""></low>
MOVC A,@A+DPTR	1 0 0 1 0 0 1	L 24	4	6	4 6 8	(A)<((A)+(DPTR)) <b>FLASH</b>
MOVC @(DPTR++),A	1 0 1 0 0 1 0	ERROR	4	4	4 or 6	((DPTR))<(A) and DPTR+1 FLASH DO NOT USE
MOVC A,@A+PC	1 0 0 0 0 0 1	L 24	4	6	4 6 8	(A)<((A)+(PC+1)) <b>FLASH</b>
MOVX A,@Ri	1 1 1 0 0 0 1	24	4	6	4 or 6	(A)<((Ri)) XRAM (XADDRH <f0h-f5h)< td=""></f0h-f5h)<>
MOVX A,@DPTR	1 1 1 0 0 0 0	24	4	6	4 or 6	(A)<((DPTR)) <b>XRAM</b>
MOVX @Ri,A	1 1 1 1 0 0 1	24	4	6	4 or 6	((Ri))<(A) XRAM (XADDRH <f0h-f5h)< td=""></f0h-f5h)<>
MOVX @DPTR,A	1 1 1 1 0 0 0	24	4	6	4 or 6	((DPTR))<(A) <b>XRAM</b>
PUSH direct	1 1 0 0 0 0 0	24	4	8	6	(SP)<(SP)+1
	a7 a6 a5 a4 a3 a2 a1 a	0				((SP))<(direct)
POP direct	1 1 0 1 0 0 0	24	4	8	6	(direct)<((SP))
	a7 a6 a5 a4 a3 a2 a1 a	0				(SP)<(SP)-1
XCH A,Rn	1 1 0 0 1 n2 n1 r	0 12	2	4	2 or 4	(A)<>(Rn)
XCH A,direct	1 1 0 0 0 1 0	12	2	6	4	(A)<>(direct)
	a7 a6 a5 a4 a3 a2 a1 a	0				
XCH A,@Ri	1 1 0 0 0 1 1	12	2	4	2 or 4	(A)<>((Ri))
XCHD A,@Ri	1 1 0 1 0 1 1	12	2	4	2 or 4	(A)<>((Ri)) (low nibble only)
CLR C	1 1 0 0 0 0 1	1 12	2	4	2 or 4	(C)<0
CLR bit	1 1 0 0 0 0 1	12	2	6	4	(bit)<0
	b7 b6 b5 b4 b3 b2 b1 b	-				
SETB C		12	2	4	2 or 4	(C)<1
SETB bit		12	2	6	4	(bit)<1
	b7 b6 b5 b4 b3 b2 b1 b	-				
CPL C		l 12	2	4	2 or 4	complement carry flag
CPL bit	1 0 1 1 0 0 1	12	2	6	4	complement (bit)
	b7 b6 b5 b4 b3 b2 b1 b	0				
ANL C,bit	1 0 0 0 0 0 1	24	4	8	6	(C)<(C) AND (bit)
	b7 b6 b5 b4 b3 b2 b1 b	0				
ANL C,/bit	1 0 1 1 0 0 0	24	4	8	6	(C)<(C) AND NOT(BIT)
	b7 b6 b5 b4 b3 b2 b1 b	0				
ORL C,bit	0 1 1 1 0 0 1	24	4	8	6	(C)<(C) OR (bit)
	b7 b6 b5 b4 b3 b2 b1 b	0				

	Instruction code	Clocks	/instruct	ion (42ns	/clock)	- I .:
Mnemonic	D7 D6 D5 D4 D3 D2 D1 D0	8051	0 WAIT	1 WAIT	PAR.	Explanation
ORL C,/BIT	1 0 1 0 0 0 0 0 0 0 b7 b6 b5 b4 b3 b2 b1 b0	24	4	8	6	(C)<(C) OR NOT (bit)
MOV C,bit  MOV bit,C	1 0 1 0 0 0 1 0 b7 b6 b5 b4 b3 b2 b1 b0	12	2	6	4	(C)<(bit)
MOV bit,C	1 0 0 1 0 0 1 0 b7 b6 b5 b4 b3 b2 b1 b0	24	4	8	6	(bit)<(C)
ACALL addr11	a10 a9 a8 1 0 0 0 1 a7 a6 a5 a4 a3 a2 a1 a0	24	4	8	6 or 8	call subroutine (2KByte page) save return address on stack
LCALL addr16	0 0 0 1 0 0 1 0 a15 a14 a13 a12 a11 a10 a9 a8 a7 a6 a5 a4 a3 a2 a1 a0	24	4	10	8	call subroutine (64KByte range) save return address on stack
RET	0 0 1 0 0 0 1 0	24	4	4	4 or 6	pop return address and jump
RETI	0 0 1 1 0 0 1 0	24	4	4	4 or 6	pop return address and jump restore interrupt scanning
AJMP addr11	a10 a9 a8 0 0 0 0 1 a7 a6 a5 a4 a3 a2 a1 a0	24	4	8	6 or 8	jump to address (2KByte page)
LJMP addr16	0 0 0 0 0 0 0 1 0 a15 a14 a13 a12 a11 a10 a9 a8 a7 a6 a5 a4 a3 a2 a1 a0	24	4	10	8	jump to address (64KByte range)
SJMP rel	1 0 0 0 0 0 0 0 0 0 r7 r6 r5 r4 r3 r2 r1 r0	24	4	8	6 or 8	jump rel
JMP @A+DPTR	0 1 1 1 0 0 1 1	24	4	4	4 or 6	(PC)<(A)+(DPTR)
JZ rel	0 1 1 0 0 0 0 0 0 r7 r6 r5 r4 r3 r2 r1 r0	24	4	8	6 or 8	If (A)<0 jump rel
JNZ rel	0 1 1 1 0 0 0 0 0 r7 r6 r5 r4 r3 r2 r1 r0	24	4	8	6 or 8	If (A) ≠0 jump rel
JC rel JNC rel	0 1 0 0 0 0 0 0 0 0 r7 r6 r5 r4 r3 r2 r1 r0	24	4	8	6 or 8	If (C)<1 jump rel
JNC rel	0 1 0 1 0 0 0 0 r7 r6 r5 r4 r3 r2 r1 r0	24	4	8	6 or 8	If (C)<0 jump rel
JB bit,rel	0 0 1 0 0 0 0 0 b7 b6 b5 b4 b3 b2 b1 b0 r7 r6 r5 r4 r3 r2 r1 r0	24	4	10	6 or 8	If (bit)<1 jump rel
JNB bit,rel	0 0 1 1 0 0 0 0 b7 b6 b5 b4 b3 b2 b1 b0 r7 r6 r5 r4 r3 r2 r1 r0	24	4	10	6 or 8	If (bit)<0 jump rel
JBC bit,rel	0 0 0 1 0 0 0 0 b7 b6 b5 b4 b3 b2 b1 b0 r7 r6 r5 r4 r3 r2 r1 r0	24	4	10	6 or 8	If (bit)<1 jump rel and clear (bit)
CJNE A,direct,re	1 0 1 1 0 1 0 1 a7 a6 a5 a4 a3 a2 a1 a0 r7 r6 r5 r4 r3 r2 r1 r0	24	4	10	6 or 8	If (A)≠(direct) jump rel If (A) <direct (c)<1<="" td=""></direct>
CJNE A,#data,re	1 0 1 1 0 1 0 0 d7 d6 d5 d4 d3 d2 d1 d0 r7 r6 r5 r4 r3 r2 r1 r0	24	4	10	6 or 8	If (A)≠ #data jump rel If (A)<#data (C)<1
CJNE Rn,#data,r	1 0 1 1 1 n2 n1 n0 d7 d6 d5 d4 d3 d2 d1 d0 r7 r6 r5 r4 r3 r2 r1 r0	24	4	10	6 or 8	If (Rn)≠ #data jump rel If (Rn)<#data (C)<1

	Mnemonic			Inst	tructi	ion c	ode			Clocks	/instruct	ion (42ns	/clock)	Explanation
	winemonic	D7	D6	D5	D4	D3	D2	D1	D0	8051	0 WAIT	1 WAIT	PAR.	Ехріанаціон
	CJNE @Ri,#data,rel	1	0	1	1	0	1	1	i	24	4	10	6 or 8	If ((Ri))≠ #data jump rel
bo		d7	d6	d5	d4	d3	d2	d1	d0					If ((Ri))<#data (C)<1
nching		r7	r6	r5	r4	r3	r2	r1	r0					
branc	DJNZ Rn,rel	1	1	0	1	1	n2	n1	n0	24	4	8	6 or 8	(Rn)<(Rn)-1
ram		r7	r6	r5	r4	r3	r2	r1	r0					If (Rn)≠ 0 jump rel
Progr	DJNZ direct,rel	1	1	0	1	0	1	0	1	24	4	10	6 or 8	(direct)<(direct)-1
ш.		а7	a6	a5	a4	а3	a2	a1	a0					If (direct)≠ 0 jump rel
		r7	r6	r5	r4	r3	r2	r1	r0					
	NOP	0	0	0	0	0	0	0	0	12	2	4	2 or 4	No OPeration (does nothing)

PAR: parallel read flash is default memory access method (disable: LCALL DFFCh, enable LCALL DFFFh build in routines)

## Notes on instruction set and the adressing modes

Rn Register R7-R0 of currently selected register bank (RS0 and RS1 in PSW SFR)

direct 8 bit GPR address (00h-7fh and 80h-ffh SFR register space)

@Ri Ri is a 8 bit pointer to indirect addressable GPR's (00h-ffh) (i=0 or i=1)

#data 8 bit constant included in instruction (range 00h-ffh)
#data16 16 bit constant included in instruction (range 0000h-ffffh)

addr16 16 bit destination address (range 64KByte)

addr11 11 bit destination address (range within current 2Kbyte page)

rel 8 bit two's complement jump offset (relative to first byte next instruction)

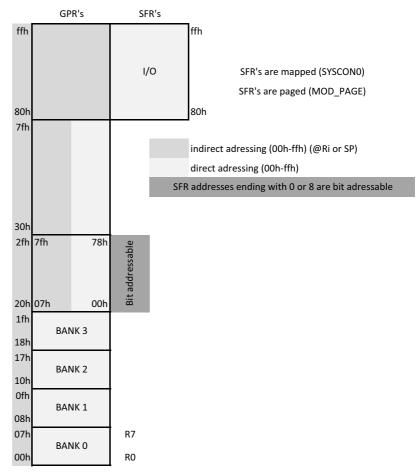
bit 8 bit address of a direct adressable bit

## Instructions that affec flag settings

Instruction		Flag	
	С	ov	AC
ADD	х	х	х
ADDC	х	х	х
SUBB	х	х	х
MUL	0	х	
DIV	0	х	
DA A	х		
RRC	х		
RLC	х		
SETB C	1		
CLR C	0		
CPL C	х		
ANL C,bit	х		
ANL C,/bit	х		
ORL C,bit	х		
ORL C,/bit	х		
MOV C,bit	х		
CJNE	х		

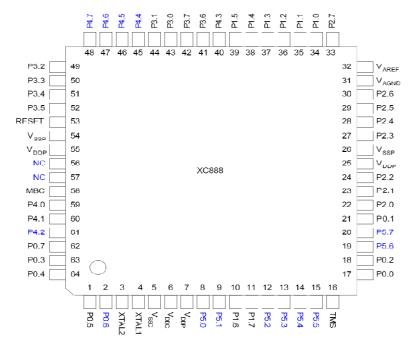
XRAM: f000h-f5ffh
Boot ROM: c000h-efffh
FLASH: 0000h-7fffh

## Register map



SFR ADDR BIT access	PAGE 0	PAGE 1	PAGE 2	NOT MAPPED (RMAP=0 PAGE 3	PAGE 4	PAGE 5	PAGE 6	RMAP=1 NO PAGE
FF FE	CCU6_CC62SRH CCU6_CC62SRL	CCU6_CC62RH CCU6_CC62RL	CCU6_TRPCTRH CCU6_TRPCTRL	CCU6_CMPSTATH CCU6_CMPSTATL				
FD FC	CCU6_CC61SRH CCU6_CC61SRL	CCU6_CC61RH CCU6_CC61RL	CCU6_MODCTRH CCU6_MODCTRL	CCU6_T13H CCU6_T13L				
FB	CCU6_CC60SRH	CCU6_CC60RH	CCU6_TCTR2H	CCU6_T12H				
FA F9	CCU6_CC60SRL	CCU6_CC60RL	CCU6_TCTR2L	CCU6_T12L	PH1			
F8 F7	T				P1		ī	HWBPDR
F6								HWBPSR
F5 F4								MMDR MMICR
F3 F2								MMBPCR MMSR
F1								MMCR2
F0 EF	Т				В	ı	ı	
EE								
ED EC								MMWR2
EB EA	FDRES FDSTEP							MMWR1
E9	FDCON	MISC_CON			N1			MMCR2
E8 E7					_141			
E6 E5								
E4								
E3 E2								
E1 E0				ACC ( A ONLY IF	USED IN OPCODE)			
DF								
DE DD				DATA3 DATA2				
DC DB				DATA1 DATA0				
DA				ADH				
D9 D8	_	_		ADL ADCON				
D7 D6								
D5 D4								
D3		ADC_CHCTR7	ADC_RESR3H	ADC_RESRA3H		ADC_EVINPR	ADC_QINR0	
D2 D1		ADC_CHCTR6	ADC_RESR3L	ADC_RESRA3L ADC_PAGE		ADC_EVINSR	ADC_QBUR0	
D0 CF	ADC_ETRCR	ADC_CHCTR5	ADC_RESR2H		SW	ADC_EVINCR	ADC_Q0R0	
CE	ADC_INPCR0	ADC_CHCTR4	ADC_RESR2L	ADC_RESRA2L	ADC_VFCR	ADC_EVINFR	ADC_QSR0	
CC	ADC_LCBR ADC_PRAR	ADC_CHCTR3 ADC_CHCTR2	ADC_RESR1H ADC_RESR1L	ADC_RESRA1H ADC_RESRA1L	ADC_RCR3 ADC_RCR2	ADC_CHINPR ADC_CHINSR	ADC_QMR0 ADC_CRMR1	FDRES1 FDSTEP1
CB CA	ADC_GLOBSTR ADC_GLOBCTR	ADC_CHCTR1 ADC_CHCTR0	ADC_RESR0H ADC_RESR0L	ADC_RESRA0H ADC_RESRA0L	ADC_RCR1 ADC_RCR0	ADC_CHINCR ADC_CHINFR	ADC_CRPR1 ADC_CRCR1	FDCON1 BG1
C9	P4_DIR	P4_PUDEN	P4_ALTSEL1		ADO_NONO	ADO_CHINITI	ABO_CHOTT	SBUF1
C8 C7	P4_DATA	P4_PUDSEL	P4_ALTSEL0	P4_OD				SCON1
C6				T2 T2H		<u> </u>		Tot Tou
C6 C5 C4				T2_T2H T2_T2L		<u> </u>		T21_T2H T21_T2L
C6 C5 C4 C3 C2				T2_T2L T2_RC2H T2_RC2L				T21_T2L T21_RC2H T21_RCL2
C6 C5 C4 C3 C2 C1				T2_T2L T2_RC2H				T21_T2L T21_RC2H T21_RCL2 T21_T2MOD
C6 C5 C4 C3 C2 C1 C0 BF	BG	COCON		T2_T2L T2_RC2H T2_RC2L T2_T2MOD				T21_T2L T21_RC2H T21_RCL2 T21_T2MOD T21_T2CON WDTH
C6 C5 C4 C3 C2 C1 C0 BF BE BD	BG BCON	COCON FEAH		T2_T2L T2_RC2H T2_RC2L T2_T2MOD T2_T2CON				T21_T2L  T21_RC2H  T21_RCL2  T21_T2MOD  T21_T2CON  WDTH  WDTL  WDTWINB
C6 C5 C4 C3 C2 C1 C0 BF BE BD BC BB	BCON NMISR NMICON	FEAH FEAL PASSWD		T2_T2L T2_RC2H T2_RC2L T2_T2MOD T2_T2CON SCU_PAGE  MODSUSP  PMCON2				T21_T2L T21_RC2H T21_RCL2 T21_T2MOD T21_T2CON WDTH WDTL
C6 C5 C4 C3 C2 C1 C0 BF BE BD BC	BCON NMISR	FEAH FEAL		T2_T2L T2_RC2H T2_RC2L T2_T2MOD T2_T2CON SCU_PAGE MODSUSP PMCON2 MODPISEL2	РН			T21_T2L  T21_RC2H  T21_RCL2  T21_T2MOD  T21_T2CON  WDTH  WDTL  WDTWINB  WDTREL
C6 C5 C4 C3 C2 C1 C0 BF BE BD BC BB BA B9 B8	BCON NMISR NMICON EXICON1	FEAH FEAL PASSWD CMCON		T2_T2L T2_RC2H T2_RC2L T2_T2MOD T2_T2CON SCU_PAGE MODSUSP PMCON2 MODPISEL2	PH  P			T21 T2L T21 RC2H T21 RC2H T21 RC12 T21 T2MOD T21 T2CON WDTH WDTL WDTWINB WDTREL WDTCON
C6 C5 C4 C3 C2 C1 C0 BF BE BD BC BB	BCON NMISR NMICON EXICON1  EXICON0 IRCON2	FEAH FEAL PASSWD CMCON  PLL_CON OSC_CON		T2, T2L T2, RC2H T2, RC2L T2, T2MOD T2, T2CON SCU_PAGE MODSUSP PMCON2 MODPISEL2				T21_T2L T21_RC2H T21_RC2H T21_RC1P T21_T2MOD T21_T2CON WDTH WDTL WDTL WDTL WDTCON WDTCON MD5_MR5 MD6_MR6
C6 C5 C4 C3 C2 C1 C0 BF BE BD BC BB	BCON NMISR NMICON EXICON1  EXICON0 IRCON2 IRCON1 IRCON0	FEAH FEAL PASSWD CMCON  PLL_CON OSC_CON PMCON1 PMCON0		T2, T2L T2, RC2H T2, RC2H T2, RC2L T2, T2MOD T2, T2CON SCU_PAGE MODSUSP PMCON2 MODPISEL2 MODPISEL1 IRCON4 IRCON4				T21 T2L T21 R02H T21 R02H T21 R01E T21 T2MOD T21 T2CON WDTH WOTWNB WDTHEL WDTCON  MOS MRS MD4 MR4 M03 MR3 M02 MR2
C6 C5 C4 C3 C2 C1 C1 C0 BF BE BB BB BB BA B9 B8 B7 B6 B5 B6 B5 B8	BCON NMISR NMICON EXICON1  EXICON0 IRCON2 IRCON1	FEAH FEAL PASSWD CMCON  PLL_CON OSC_CON PMCON1		T2, T2L T2, RC2H T2, RC2L T2, T2MOD T2, T2CON SCU_PAGE MODSUSP PMCON2 MODPISEL2 MODPISEL1 IRCON4 IRCON3 XADDRH				T21 T2L T21 R02H T21 R02H T21 R02H T21 R02H T21 T2MOD T21 T2GON WDTH WDTL WDTWINB WDTREL WDTCON  MD5 MR5 MD4 MR4 M03 MR3 M02 MR2 M01 MR1
C6 C5 C4 C3 C2 C1 C0 BF BE BD BC BB BB BA BB	BCON NMISR NMICON EXICON1  EXICON0 IRCON2 IRCON1 IRCON0 MODPISEL  P3_DIR	FEAH FEAL PASSWD CMCON  PLL_CON OSC_CON PMCON1 PMCON0 ID  P3_PUDEN	P3 ALTSEL1	T2, T2L T2, RC2H T2, RC2H T2, RC2L T2, T2MOD T2, T2CON SCU_PAGE MODSUSP MODSUSP MODPISEL2 MODPISEL1 IRCON4 IRCON4 IRCON3 XADDRH PORT_PAGE				T21 T2L T21 R02H T21 R02H T21 R02H T21 R02H T21 T2MOD T21 T2CON WDTH WDTH WDTWINB WDTREL WDTCON  MD5 MR5 MD4 MR4 MD3 MR3 MD2 MR2 MD1 MR1 MD0 MR0 MD0 MR0 MDUCON
C6 C5 C4 C3 C2 C1 C0 BF BE BD BC BB	BCON NMISR NMICON EXICON1  EXICON0 IRCON2 IRCON1 IRCON0 MODPISEL	FEAH FEAL PASSWD CMCON  PLL CON OSC_CON PMCON1 PMCON0 ID	P3 ALTSEL1 P3_ALTSEL0	T2, T2L T2, RC2H T2, RC2H T2, RC2L T2, T2MOD T2, T2CON SCU_PAGE MODSUSP  PMCON2 MODPISEL2  MODPISEL1  IRCON4 IRCON4 IRCON3 XADDRH PORT_PAGE P3_OD SSC_BRH				T21 T2L T21 RC2H T21 RC2H T21 RCL2 T21 T2MOD T21 T2CON WDTH WDTWNB WDTWNB WDTGN WDTCON MD5 MR5 MD4 MR4 MD3 MR3 MD2 MR2 MD1 MR1 MD0 MR1
C6 C5 C4 C3 C2 C1 C0 BF BE BB BD BC BB BA B9 BA B9 B8 B7 B6 B8 B7 B6 B8 B8 B7 B6 B8 B8 B7 B6 B8 B8 B7 B8 B8 B8 B8 B7 B8 B8 B8 B8 B8 B7 B8	BCON NMISR NMICON EXICON1  EXICON0 IRCON2 IRCON1 IRCON0 MODPISEL  P3_DIR	FEAH FEAL PASSWD CMCON  PLL_CON OSC_CON PMCON1 PMCON0 ID  P3_PUDEN		T2, T2L T2, RC2H T2, RC2L T2, T2MOD T2, T2CON SCU_PAGE MODSUSP PMCON2 MODPISEL2 MODPISEL1 IRCON4 IRC				T21 T2L T21 RC24 T21 RC24 T21 RC24 T21 RC24 T21 T2MOD T21 T2CON WOTH WOTH WOTH WOTREL WDTCON  MD5 MR5 M04 MR4 M03 MR3 M02 MR2 M01 MR1 M00 MR0 MD0 MR0 MDUCON
C6 C5 C4 C3 C2 C1 C0 BF BB	BCON NMISR NMICON EXICON1  EXICON0 IRCON2 IRCON1 IRCON0 MODPISEL  P3_DIR	FEAH FEAL PASSWD CMCON  PLL_CON OSC_CON PMCON1 PMCON0 ID  P3_PUDEN		T2, T2L T2, RC2H T2, RC2H T2, RC2L T2, T2MOD T2, T2CON SCU_PAGE MODSUSP MODSUSP MODPISEL2 MODPISEL1 IRCON4 IRCON4 IRCON3 XADDRH PORT_PAGE P3_OD SSC_BRH SSC_BRL SSC_TBL				T21 T2L T21 RC24 T21 RC24 T21 RC24 T21 RC24 T21 T2MOD T21 T2CON WOTH WOTH WOTH WOTREL WDTCON  MD5 MR5 M04 MR4 M03 MR3 M02 MR2 M01 MR1 M00 MR0 MD0 MR0 MDUCON
C6 C5 C4 C3 C2 C1 C1 C0 BF BE BD BC BB	BCON NMISR NMICON EXICON1  EXICON0 IRCON2 IRCON1 IRCON0 MODPISEL  P3_DIR	FEAH FEAL PASSWD CMCON  PLL_CON OSC_CON PMCON1 PMCON0 ID  P3_PUDEN		T2, T2L T2, RC2H T2, RC2H T2, RC2L T2, T2MOD T2, T2CON SCU_PAGE MODSUSP  MODSUSP  MODPISEL2  MODPISEL1  IRCON4 IRCON4 IRCON3 XADDRH PORT_PAGE P3_OD SSC_BRH SSC_BRL SSC_TBL SSC_TBL SSC_CONH				T21 T2L T21 R02H T21 R02H T21 R02H T21 R02H T21 T2MOD T21 T2CON WDTH WDTH WDTWINB WDTREL WDTCON  MD5 MR5 MD4 MR4 MD3 MR3 MD2 MR2 MD1 MR1 MD0 MR0 MD0 MR0 MDUCON
C6 C5 C4 C3 C2 C1 C0 BF BE BD BC BB	BCON NMISR NMICON EXICON1  EXICON0 IRCON2 IRCON1 IRCON0 MODPISEL P3_DATA	FEAH FEAL PASSWD CMCON  PLL CON OSC CON PMCON1 PMCON0 ID  P3 PUDEN P3 PUDSEL	P3_ALTSEL0	T2, T2L T2, RC2H T2, RC2H T2, RC2L T2_TZMOD T2, T2CON SCU_PAGE MODSUSP PMCON2 MODPISEL1 IRCON4 IRCON3 XADDRH PORT_PAGE P3_OD SSC_BRH SSC_BRL SSC_CONH SSC_CONH SSC_CONL SSC_PISEL				T21 T2L T21 R02H T21 R02H T21 R02H T21 R02H T21 T2MOD T21 T2CON WDTH WDTH WDTWINB WDTREL WDTCON  MD5 MR5 MD4 MR4 MD3 MR3 MD2 MR2 MD1 MR1 MD0 MR0 MD0 MR0 MD0 MR0 MDUCON
C6 C5 C4 C3 C2 C1 C1 C0 BF BB BB BB BA BB BA BB BA BB BB BB BA BB BB	BCON NMISR NMICON EXICON1  EXICON0 IRCON2 IRCON1 IRCON0 MODPISEL  P3_DIR	FEAH FEAL PASSWD CMCON  PLL_CON OSC_CON PMCON1 PMCON0 ID  P3_PUDEN		T2, T2L T2, RC2H T2, RC2H T2, RC2L T2_TZMOD T2, T2CON SCU_PAGE MODSUSP PMCON2 MODPISEL1 IRCON4 IRCON3 XADDRH PORT_PAGE P3_OD SSC_BRH SSC_BRL SSC_CONH SSC_CONH SSC_CONL SSC_PISEL	IP			T21 T2L T21 R02H T21 R02H T21 R02H T21 R02H T21 T2MOD T21 T2CON WDTH WDTH WDTWINB WDTREL WDTCON  MD5 MR5 MD4 MR4 MD3 MR3 MD2 MR2 MD1 MR1 MD0 MR0 MD0 MR0 MD0 MR0 MDUCON
C6 C5 C4 C3 C2 C1 C1 C0 BF BE BB	BCON NMISR NMICON EXICON1  EXICON0 IRCON2 IRCON2 IRCON0 IRCON0 MODPISEL  P3_DIR P3_DATA  CCU8_CMPMODIFH CCU6_CMPMODIFH CCU6_CMPMIDIFC CCU6_ISRH	FEAH FEAL PASSWD CMCON  PLL CON OSC_CON PMCON1 PMCON0 ID  P3_PUDEN P3_PUDSEL  CCU6_TCTR0H CCU6_TCTR0L CCU6_TCTR0L CCU6_TCTR0L CCU6_TCTR0L	P3_ALTSEL0  CCU6_MCMCTR CCU6_PSLR CCU6_ISSH	T2, T2L T2, RC2H T2, RC2H T2, RC2L T2_TZMOD T2_TZCON SCU_PAGE MODSUSP MODSUSP PMCON2 MODPISEL2 MODPISEL1 IRCON4 IRCON4 IRCON4 IRCON5 XADDRH PORT_PAGE P3_OD SSC_BRH SSC_BRH SSC_BRL SSC_TBL SSC_TBL SSC_TBL SSC_FBL II	IP			T21 T2L T21 RC24 T21 RC24 T21 RC24 T21 RC24 T21 T2MOD T21 T2CON WOTH WOTH WOTH WOTREL WDTCON  MD5 MR5 M04 MR4 M03 MR3 M02 MR2 M01 MR1 M00 MR0 MD0 MR0 MDUCON
C6 C5 C4 C3 C2 C1 C0 BF BE BD BC BB BB BA B9 B8 B7 B6 B8 B7 B8 B7 B8 B8 B8 B8 B9 B8 B8 B8 B7 B8	BCON NMISR NMICON EXICON1  EXICON0 IRCON2 IRCON1 IRCON0 MODPISEL  P3_DIR P3_DATA  CCU6_CMPMODIFH CCU6_CMPMODIFIEL	FEAH FEAL PASSWD CMCON  PLL CON OSC CON PMCON1 PMCON0 ID  P3_PUDEN P3_PUDSEL  CCUe_TCTR0H CCUe_TCTR0L	P3_ALTSEL0  CCU6_MCMCTR CCU6_PSLR	T2 T2L T2 RC2H T2 RC2H T2 RC2L T2_TZMOD T2_TZCON SCU_PAGE MODSUSP  MODSUSP  MODPISEL1  IRCON4 IRCON3 XADDRH PORT_PAGE P3_OD SSC_BRH SSC_BRL SSC_TBL SSC_TBL SSC_TBL SSC_TBL SSC_CONL SSC_PISEL  IRCON4 IRCON5	P P P P P P P P P P P P P P P P P P P			T21 T2L T21 R02H T21 R02H T21 R02H T21 R02H T21 T2MOD T21 T2CON WDTH WDTH WDTWINB WDTREL WDTCON  MD5 MR5 MD4 MR4 MD3 MR3 MD2 MR2 MD1 MR1 MD0 MR0 MD0 MR0 MD0 MR0 MDUCON
C6 C6 C5 C4 C3 C1 C2 C1 C0 BF BE BB	BCON NMISR NMICON EXICON1  EXICON0 IRCON2 IRCON1 IRCON0 MODPISEL  P3_DIR P3_DATA  CCU6_CMPMODIFH CCU6_ISRH CCU6_ISRL	FEAH FEAL PASSWD CMCON  PLL CON OSC CON PMCON1 PMCON0 ID  P3_PUDEN P3_PUDSEL  CCU6_TCTR0H CCU6_T12DTCL  P2_PUDEN P2_PUDEN	P3_ALTSEL0  CCU6_MCMCTR CCU6_PSLR CCU6_ISSH	T2 T2L T2 RC2H T2 RC2H T2 RC2L T2_TZMOD T2_TZCON SCU_PAGE MODSUSP  MODSUSP  MODPISEL1  IRCON4 IRCON3 XADDRH PORT_PAGE P3_OD SSC_BRH SSC_BRL SSC_TBL SSC_TBL SSC_TBL SSC_TBL SSC_CONL SSC_PISEL  IRCON4 IRCON5	IP			T21 T2L T21 RC24 T21 RC24 T21 RC24 T21 RC24 T21 T2MOD T21 T2CON WOTH WOTH WOTH WOTREL WDTCON  MD5 MR5 M04 MR4 M03 MR3 M02 MR2 M01 MR1 M00 MR0 MD0 MR0 MDUCON
C6 C5 C5 C4 C3 C2 C1 C1 C0 BF BE BB	BCON NMISR NMICON EXICON1  EXICON0 IRCON2 IRCON2 IRCON1 IRCON0 MODPISEL  P3_DIR P3_DATA  CCU8_CMPMODIFH CCU8_CMPMODIFH CCU8_ISRH CCU6_ISRL  P2_DIR P2_DIR P2_DATA	FEAH FEAL PASSWD CMCON  PLL CON OSC_CON PMCON1 PMCON0 ID  P3_PUDEN P3_PUDSEL  CCU6_TCTR0H CCU6_TCTR0H CCU6_T12DTCH CCU6_T12DTCL  P2_PUDEN P3_PUDSEL	P3_ALTSEL0  CCU6_MCMCTR CCU6_PSLR CCU6_ISSH CCU6_ISSL	T2, T2L T2, RC2H T2, RC2H T2, RC2L T2, T2MOD T2, T2CON SCU_PAGE MODSUSP MODSUSP PMCON2 MODPISEL1 IRCON4 IRCON4 IRCON4 IRCON4 IRCON4 IRCON5 SSC_BRL SSC_BRL SSC_BRL SSC_BRL SSC_FBL SSC_FBL SSC_FBL SSC_CONL SSC_PISEL I	P P P P P P P P P P P P P P P P P P P			T21 T2L T21 RC24 T21 RC24 T21 RC24 T21 RC24 T21 T2MOD T21 T2CON WOTH WOTH WOTH WOTH WOTH WOTH WOTHON MD5 MR5 M04 MR4 M03 MR3 M02 MR2 M01 MR1 M00 MR0 M0DUSTAT
C6 C5 C4 C3 C2 C1 C1 C0 BF BE BB	BCON NMISR NMICON EXICON1  EXICON0 IRCON2 IRCON1 IRCON0 IRCON0 MODPISEL  P3_DIR P3_DATA  CCU6_CMPMODIFH CCU6_ISRL  P2_DIR P2_DATA  CCU6_MCMOUTSL  CCU6_MCMOUTSL  CCU6_MCMOUTSL  CCU6_MCMOUTSL  CCU6_MCMOUTSL	FEAH FEAL PASSWD CMCON  PLL CON OSC CON PMCON1 PMCON0 ID  P3 PUDEN P3 PUDSEL  CCU6 TCTR0H CCU6 T12DTCH CCU6_T12DTCL  P2_PUDEN P2_PUDEN P2_PUDSEL CCU6_T13PRH CCU6_T13PRH CCU6_T13PRH CCU6_T13PRH CCU6_T13PRH CCU6_T13PRH	P3_ALTSEL0  CCU6_MCMCTR CCU6_PSLR CCU6_ISSL  CCU6_ISSL	T2 T2L T2 RC2H T2 RC2H T2 RC2L T2_TZMOD T2_TZCON SCU_PAGE MODSUSP  MODSUSP  PMCON2 MODPISEL2  MODPISEL1 IRCON4 IRCON3 XADDRH PORT_PAGE P3_OD SSC_BRH SSC_BRL SSC_TBL SSC_TBL SSC_TBL SSC_TBL SSC_TBL SSC_TBL SSC_TBL SSC_CONL SSC_PISEL  CCU6_PISEL2  CCU6_PISEL0  CCU6_PISEL0H CCU6_PISEL0H CCU6_PISEL0H	P P P P P P P P P P P P P P P P P P P			T21 T2L T21 R24 T21 R612 T21 R24 T21 R612 T21 T2MOD T21 T2CON WOTH WOTHWOTH WOTHCON WOTHON WOTHCON MD5 MR5 M04 MR4 M03 MR3 M02 MR2 M01 MR1 M0 MR0 M0
C6 C5 C4 C3 C2 C1 C0 BF BE BD BC BB	BCON NMISR NMICON EXICON1  EXICON0 IRCON2 IRCON1 IRCON0 IRCON1 IRCON0 MODPISEL  P3 DIR P3 DATA  CCUB_CMPMODIFL CCUB_ISRH CCUB_ISRH CCUB_ISRL  P2 DATA CCUB_MCMOUTSH CCUB_MCMOUTSH CCUB_TCTR4H CCUB_TCTR4H CCUB_TCTF44L	FEAH FEAL PASSWD CMCON  PLL CON OSC CON PMCON1 PMCON0 ID  P3_PUDEN P3_PUDEN COU6_T12DTCH CCU6_T12DTCH CCU6_T12PTCH CCU6_T1	P3_ALTSEL0  CCU6_MCMCTR CCU6_PSLR CCU6_ISSH CCU6_ISSL  CCU6_INPL CCU6_INPL CCU6_IENH CCU6_IENH CCU6_IENH	T2, T2L T2, T2L T2, T2CH T2, T2CH T2, T2CH T2, T2CON SCU_PAGE  MODSUSP  PMCON2 MODPISEL2  MODPISEL1  IRCON4 IRCON3 XADDRH PORT_PAGE P3_OD SSC_BRH SSC_BRL SSC_TBL SSC_TBL SSC_TBL SSC_TBL SSC_TBL SSC_TBL SSC_CONL SSC_PISEL	P P P P P P P P P P P P P P P P P P P			T21 T2L T21 R2L T21 R2C2 T21 R2C2 T21 T2MOD T21 T2CON WDTH WDTWINS WDTREL WDTCON  MOS MRS MD4 MR4 MD3 MR3 MD2 MR2 MD1 MR1 MD MR0 MDUCON MDUCON MDUSTAT
C6 C5 C4 C3 C4 C3 C2 C1 C1 C0 BF BE BB BB BA BB BA BB BB BB BB BB BB BB BB	BCON NMISR NMICON EXICONI  EXICONO IRCON2 IRCON0 IRCON0 MODPISEL  P3 DIR P3 DATA  CCU6 CMPMODIFH CCU6 CMPMODIFL CCU6 ISRH CCU6 ISRH CCU6 CMPMODIFL CCU6 MCMOUTSH CCU6 MCM CCU6 MCM CCU6 MCM CCU6 MCM C	FEAH FEAL PASSWD CMGON  PLL CON OSC CON PMCONI PMCONI ID P3_PUDEN P3_PUDEN CU6_TCTR0H CCU6_TCTR0L CCU6_TT2DTCL CCU6_T12DTCL CCU6_T12PTCL CCU6_T13PRL CCU6_T13PRH	P3_ALTSEL0  CCU6_MCMCTR CCU6_PSLR CCU6_ISSH CCU6_ISSL  CCU6_INPH CCU6_INPL CCU6_INPL CCU6_INPL	T2. T2L T2. RC2H T2. RC2H T2. RC2H T2. RC2H T2. RC2H T2. T2MOD T2. T2CON SOU_PAGE MODSUSP  MODSUSP  PMCON2 MODPISEL2  MODPISEL1  IRCON4 IRCON3 XADDRH PORT_PAGE P3 OD SSC_BRH SSC_BRH SSC_BRH SSC_FIBL SSC_CONL SSC_CONL SSC_CONL SSC_CONL SSC_CONL CCUG_PISEL2 CCUG_PISEL2 CCUG_PISELOH CCUG_PISELOH CCUG_ISH	P P P P P P P P P P P P P P P P P P P			T21 T2L T21 RC2H T21 RC2H T21 RC12 T21 RC12 T21 T2ROD T21 T2CON WDTH WDTWNB WDTREL WDTCON  MD5 MR5 MD4 MR4 M03 MR3 M02 MR2 M01 MR1 M00 MR0 MUCON MUUCON CD STATC CD CORDZH CD CO
C6 C5 C4 C3 C2 C1 C1 C0 BF BE BB	BCON NMISR NMICON EXICON1  EXICON0 IRCON2 IRCON2 IRCON1 IRCON0 MODPISEL  P3_DIR P3_DATA  CCU8_CMPMODIFH CCU6_CMPMODIFH CCU6_ISRL  P2_DIR P2_DATA CCU8_MCMOUTSH CCU6_ISRL  CCU6_ITCTR4H CCU6_TCTF4H CCU6_ICCU6_ICCSSRH	FEAH FEAL PASSWD CMCON  PLL CON OSC_CON PMCON1 PMCON0 ID  P3_PUDEN P3_PUDEN P3_PUDSEL  CCU6_TCTR0H CCU6_TCTR0H CCU6_T12DTCH CCU6_T12DTCH CCU6_T12PTCH CCU6_CCGSRH	P3_ALTSEL0  CCU6_MCMCTR CCU6_PSLR CCU6_ISSL	T2 T2L T2 RC2H T2 RC2H T2 RC2L T2_TZMOD T2_TZCON SCU_PAGE MODSUSP MODSUSP PMCON2 MODPISEL2  MODPISEL1 IRCON4 IRCON3 XADDRH PORT_PAGE P3_OD SSC_BRH SSC_BRL SSC_TBL SSC	ENO EO			T21 T2L T21 RC24 T21 RC24 T21 RC24 T21 RC24 T21 T2NOD T21 T2CON WOTH WOTH WOTH WOTH WOTH WOTH WOTH WOTH
C6 C6 C5 C4 C3 C2 C1 C1 C0 BF BE BB	BCON NMISR NMICON EXICON1  EXICON0 IRCON2 IRCON2 IRCON1 IRCON0 MODPISEL  P3_DIR P3_DATA  CCU8_CMPMODIFH CCU6_CMPMODIFH CCU6_ISRL  P2_DIR P2_DATA CCU8_MCMOUTSH CCU6_ISRL  CCU6_ITCTR4H CCU6_TCTF4H CCU6_ICCU6_ICCSSRH	FEAH FEAL PASSWD CMCON  PLL CON OSC_CON PMCON1 PMCON0 ID  P3_PUDEN P3_PUDEN P3_PUDSEL  CCU6_TCTR0H CCU6_TCTR0H CCU6_T12DTCH CCU6_T12DTCH CCU6_T12PTCH CCU6_CCGSRH	P3_ALTSEL0  CCU6_MCMCTR CCU6_PSLR CCU6_ISSL	T2 T2L T2 RC2H T2 RC2H T2 RC2L T2_TZMOD T2_TZCON SCU_PAGE MODSUSP MODSUSP PMCON2 MODPISEL2  MODPISEL1 IRCON4 IRCON3 XADDRH PORT_PAGE P3_OD SSC_BRH SSC_BRL SSC_TBL SSC	ENO EO			T21 T2L T21 RC24 T21 RC24 T21 RC24 T21 RC24 T21 T2NOD T21 T2CON WOTH WOTH WOTH WOTH WOTH WOTH WOTH WOTH
C6 C6 C5 C4 C3 C2 C1 C1 C0 BF BE BB	BCON NMISR NMICON EXICON1  EXICON0 IRCON2 IRCON2 IRCON1 IRCON0 MODPISEL  P3_DIR P3_DATA  CCU8_CMPMODIFH CCU6_CMPMODIFH CCU6_ISRL  P2_DIR P2_DATA CCU8_MCMOUTSH CCU6_ISRL  CCU6_ITCTR4H CCU6_TCTF4H CCU6_ICCU6_ICCSSRH	FEAH FEAL PASSWD CMCON  PLL CON OSC_CON PMCON1 PMCON0 ID  P3_PUDEN P3_PUDEN P3_PUDSEL  CCU6_TCTR0H CCU6_TCTR0H CCU6_T12DTCH CCU6_T12DTCH CCU6_T12PTCH CCU6_CCGSRH	P3_ALTSEL0  CCU6_MCMCTR CCU6_PSLR CCU6_ISSL	T2 T2L T2 RC2H T2 RC2H T2 RC2L T2_TZMOD T2_TZCON SCU_PAGE MODSUSP MODSUSP PMCON2 MODPISEL2  MODPISEL1 IRCON4 IRCON3 XADDRH PORT_PAGE P3_OD SSC_BRH SSC_BRL SSC_TBL SSC	ENO EO			T21 T2L T21 RC24 T21 RC24 T21 RC24 T21 RC24 T21 T2NOD T21 T2CON WOTH WOTH WOTH WOTH WOTH WOTH WOTH WOTH
C6 C6 C5 C4 C3 C2 C1 C1 C0 BF BE BB	BCON NMISR NMICON EXICON1  EXICON0 IRCON2 IRCON2 IRCON1 IRCON0 MODPISEL  P3_DIR P3_DATA  CCU6_CMPMODIFH CCU6_ISRH CCU6_ISRL  P2_DIR P2_DATA CCU6_MCMOUTSL CCU6_ISRL	FEAH FEAL PASSWD CMCON  PLL CON OSC CON PMCON1 PMCON0 ID  P3_PUDEN P3_PUDEN P3_PUDSEL  CCU6_TCTR0H CCU6_T12DTCH CCU6_T12DTCH CCU6_T13PRH CCU6_T13PRH CCU6_T12PRH CCU6_CC63RH CCU6_CC63RH CCU6_CC63RL	P3_ALTSEL0  CCU6_MCMCTR CCU6_PSLR CCU6_ISSH CCU6_ISSH CCU6_ISSL  CCU6_INPH CCU6_IENH CCU6_IENH CCU6_IENH CCU6_IT2MSELH CCU6_T12MSELL	T2 T2L T2 RC2H T2 RC2H T2 RC2L T2_TZMOD T2_TZCON SCU_PAGE MODSUSP MODSUSP PMCON2 MODPISEL2  MODPISEL1 IRCON4 IRCON3 XADDRH PORT_PAGE P3_OD SSC_BRH SSC_BRL SSC_TBL SSC	ENO EO			T21 T2L T21 RC24 T21 RC24 T21 RC24 T21 RC24 T21 T2NOD T21 T2CON WOTH WOTH WOTH WOTH WOTH WOTH WOTH WOTH
C6 C6 C5 C4 C3 C2 C1 C1 C0 BF BE BB	BCON NMISR NMICON EXICON1  EXICON0 IRCON2 IRCON1 IRCON2 IRCON1 IRCON0 MODPISEL  P3_DIR P3_DATA  CUG_CMPMODIFH CCUG_SRH CCUG_ISRH CCUG_ISRL  P2_DIR P2_DATA CCUG_MOMOUTSH CCUG_MOMOUTSH CCUG_CGSSRH CCUG_CCGSSRH CCUG_CCGSSRH CCUG_CCGSSRL	FEAH FEAL PASSWD CMCON  PLL CON OSC CON PMCON1 PMCON1 PMCON0 ID  P3 PUDEN P3 PUDEN P3 PUDSEL  CCU6 TCTR0H CCU6 T12DTCH CCU6_T12DTCH CCU6_T12PTL CCU6_T13PRL CCU6_T13PRL CCU6_T13PRL CCU6_CC63RL  P5_PUDEN	P3_ALTSEL0  CCU6_MCMCTR CCU6_PSLR CCU6_ISSH CCU6_ISSH CCU6_ISSL  CCU6_INPH CCU6_INPL C	T2 T2L T2 RC2H T2 RC2H T2 RC2L T2_TZMOD T2_TZCON SCU_PAGE MODSUSP MODSUSP PMCON2 MODPISEL2  MODPISEL1 IRCON4 IRCON3 XADDRH PORT_PAGE P3_OD SSC_BRH SSC_BRL SSC_TBL SSC	ENO EO			T21 T2L T21 R024 T21 R024 T21 R024 T21 R024 T21 R024 T21 T2MOD T21 T2CON WDTH WDTL WDTWINB WDTREL WDTCON  MD5 MR5 MD4 MR4 MD3 MR3 MD2 MR2 MD1 MR1 MD0 MR0 MD0 MR0 MDUSTAT  CD CON CD STATC CD CORD2L CD CORD2H CD CD CORD2H CD C
C6 C6 C6 C5 C4 C3 C2 C1 C1 C0 BF BE BB	BCON NMISR NMICON EXICON1  EXICON0 IRCON2 IRCON0 IRCON1 IRCON0 MODPISEL  P3_DIR P3_DATA  CCU6_CMPMODIFH CCU6_ISRH CC	FEAH FEAL PASSWD CMCON  PLL CON OSC CON PMCON1 PMCON0 ID  P3 PUDEN P3 PUDSEL  CCU6_TCTR0H CCU6_T12DTCL  P2_PUDEN P2_PUDSEL CCU6_T12DTCL  P2_PUDSEL CCU6_T12PTC CCU6_CCGSRT CCU6_CCGSRT  P5_PUDEN	P3_ALTSEL0  CCU8_MCMCTR CCU8_PSLR CCU8_ISSH CCU8_ISSL  CCU8_INPH CCU8_INPL CCU8_INPL CCU8_IENH CCU8_IENH CCU8_IENH CCU8_IENH CCU8_IENH CCU8_IENH CCU8_IENH CCU8_IENH CCU8_IENH	T2, T2L T2, RC2H T2, RC2H T2, RC2H T2, RC2L T2, T2MOD T2, T2CON SCU_PAGE  MODSUSP  PMCON2 MODPISEL2  MODPISEL1  IRCON4 IRCON3 XADDRH PORT_PAGE P3 OD SSC_BRH SSC_BRL SSC_TBL S	EN0  EO  BUF  CON			T21 T2L T21 RC24 T21 RC24 T21 RC24 T21 RC24 T21 T2NOD T21 T2CON WOTH WOTH WOTH WOTH WOTH WOTH WOTH WOTH
C6 C5 C5 C4 C3 C2 C1 C1 C2 C1 C6 BF BE BB	BCON NMISR NMICON EXICONI  EXICONO IRCON2 IRCON2 IRCON0 IRCON0 IRCON0 MODPISEL  P3_DIR P3_DATA  CCU6_CMPMODIFL CCU6_ISRH CCU6_ISRH CCU6_ISRH CCU6_ISRL  P2_DIR P2_DATA CCU6_MCMOUTSL CCU6_TCTA4H CCU6_CC63SRL  P5_DIR P5_DATA CCU6_CC63SRL	FEAH FEAL PASSWD CMCON  PLL CON OSC CON PMCON1 PMCON0 ID P3_PUDEN P3_PUDEN P3_PUDSEL  CCU6_TCTR0H CCU6_TT2DTCH CCU6_TT2DTCH CCU6_TT2PTH CCU6_TT3PRH CCU6_TT3PRH CCU6_TT3PRH CCU6_TCU6_TCU6_TCU6_TCU6_TCU6_TCU6_TCU6_	P3_ALTSEL0  CCU6_MCMCTR CCU6_PSLR CCU6_ISSL  P5_ALTSEL1 P5_ALTSEL1 P5_ALTSEL1 P5_ALTSEL1	T2, T2L T2, RC2H T2, RC2H T2, RC2H T2, RC2L T2, T2MOD T2, T2CON SCU_PAGE  MODSUSP  PMCON2 MODPISEL2  MODPISEL1  IRCON4 IRCON3 XADDRH PORT_PAGE P3 OD SSC_BRH SSC_BRL SSC_TBL S	ENO EO			T21 T2L T21 RC24 T21 RC24 T21 RC24 T21 RC24 T21 T2NOD T21 T2CON WOTH WOTH WOTH WOTH WOTH WOTH WOTH WOTH
C6 C6 C6 C5 C4 C3 C2 C1 C1 C0 BF BE BB	BCON NMISR NMICON EXICONI  EXICONO IRCON2 IRCON2 IRCON0 IRCON0 IRCON0 MODPISEL  P3_DIR P3_DATA  CCU6_CMPMODIFL CCU6_ISRH CCU6_ISRH CCU6_ISRH CCU6_ISRL  P2_DIR P2_DATA CCU6_MCMOUTSL CCU6_TCTA4H CCU6_CC63SRL  P5_DIR P5_DATA CCU6_CC63SRL	FEAH FEAL PASSWD CMCON  PLL CON OSC CON PMCON1 PMCON0 ID P3_PUDEN P3_PUDEN P3_PUDSEL  CCU6_TCTR0H CCU6_TT2DTCH CCU6_TT2DTCH CCU6_TT2PTH CCU6_TT3PRH CCU6_TT3PRH CCU6_TT3PRH CCU6_TCU6_TCU6_TCU6_TCU6_TCU6_TCU6_TCU6_	P3_ALTSEL0  CCU6_MCMCTR CCU6_PSLR CCU6_ISSL  P5_ALTSEL1 P5_ALTSEL1 P5_ALTSEL1 P5_ALTSEL1	T2 T2L T2 RC2H T2 RC2H T2 RC2L T2_TZMOD T2_TZCON SCU_PAGE MODSUSP  PMCON2 MODPISEL2  MODPISEL2  MODPISEL1 IRCON4 IRCON3 XADDRH PORT_PAGE P3_OD SSC_BRH SSC_BRL SSC_TBL	ENO  EO  CONO  TH			T21 T2L T21 RC24 T21 RC24 T21 RC24 T21 RC24 T21 T2NOD T21 T2CON WOTH WOTH WOTH WOTH WOTH WOTH WOTH WOTH
C6 C6 C6 C5 C4 C3 C2 C1 C1 C0 BF BE BB	BCON NMISR NMICON EXICONI  EXICONO IRCON2 IRCON2 IRCON0 IRCON0 IRCON0 MODPISEL  P3_DIR P3_DATA  CCU6_CMPMODIFL CCU6_ISRH CCU6_ISRH CCU6_ISRH CCU6_ISRL  P2_DIR P2_DATA CCU6_MCMOUTSL CCU6_TCTA4H CCU6_CC63SRL  P5_DIR P5_DATA CCU6_CC63SRL	FEAH FEAL PASSWD CMCON  PLL CON OSC CON PMCON1 PMCON0 ID P3_PUDEN P3_PUDEN P3_PUDSEL  CCU6_TCTR0H CCU6_TT2DTCH CCU6_TT2DTCH CCU6_TT2PTH CCU6_TT3PRH CCU6_TT3PRH CCU6_TT3PRH CCU6_TCU6_TCU6_TCU6_TCU6_TCU6_TCU6_TCU6_	P3_ALTSEL0  CCU6_MCMCTR CCU6_PSLR CCU6_ISSL  P5_ALTSEL1 P5_ALTSEL1 P5_ALTSEL1 P5_ALTSEL1	T2, T2L T2, T2L T2, T2CH T2, T2CH T2, T2CH T2, T2CON SCU_PAGE  MODSUSP  PMCON2 MODPISEL1  IRCON4 IRCON3 XADDRH PORT_PAGE P3 OD SSC_BRH SSC_BRL SSC_TSL SSC_TONL SSC_PISEL  CCU6_PISEL0H CCU6_PISEL0H CCU6_PISEL0H CCU6_MCMOUTH CCU6_MCMOUTH CCU6_MCMOUTH CCU6_MCMOUTH CCU6_MCMOUTH CCU6_PISE	ENO EO CONO			T21 T2L T21 RC24 T21 RC24 T21 RC24 T21 RC24 T21 T2NOD T21 T2CON WOTH WOTH WOTH WOTH WOTH WOTH WOTH WOTH
C6 C6 C6 C5 C4 C3 C1 C2 C1 C2 C1 C0 BF BB	BCON NMISR NMICON EXICONI  EXICONO IRCON2 IRCON2 IRCON0 IRCON0 IRCON0 MODPISEL  P3_DIR P3_DATA  CCU6_CMPMODIFL CCU6_ISRH CCU6_ISRH CCU6_ISRH CCU6_ISRL  P2_DIR P2_DATA CCU6_MCMOUTSL CCU6_TCTA4H CCU6_CC63SRL  P5_DIR P5_DATA CCU6_CC63SRL	FEAH FEAL PASSWD CMCON  PLL CON OSC CON PMCON1 PMCON0 ID P3_PUDEN P3_PUDEN P3_PUDSEL  CCU6_TCTR0H CCU6_TT2DTCH CCU6_TT2DTCH CCU6_TT2PTH CCU6_TT3PRH CCU6_TT3PRH CCU6_TT3PRH CCU6_TCU6_TCU6_TCU6_TCU6_TCU6_TCU6_TCU6_	P3_ALTSEL0  CCU6_MCMCTR CCU6_PSLR CCU6_ISSL  P5_ALTSEL1 P5_ALTSEL1 P5_ALTSEL1 P5_ALTSEL1	T2, T2L T2, T2CH T2, T2CH T2, T2CH T2, T2CON SCU_PAGE  MODSUSP  PMCON2 MODPISEL1  IRCON4 IRCON3 XADDRH PORT_PAGE P3 OD SSC_BRH SSC_BRH SSC_BRH SSC_BRH SSC_TBL SSC_CONL SSC_PISEL  CCU6_PISEL2 CCU6_PISEL2 CCU6_PISEL0H CCU6_PISEL0H CCU6_PISEL0H CCU6_PISELOH CCU6_PISELOH CCU6_PISELOH CCU6_PISELOH CCU6_MCMOUTH CCU6_MCMOUTL SSC_SSC_SSC_SSC_SSC_SSC_SSC_SSC_SSC_SSC	ENO  EO  GCONO  H1  FH0  TL1			T21 T2L T21 RC24 T21 RC24 T21 RC24 T21 RC24 T21 T2NOD T21 T2CON WOTH WOTH WOTH WOTH WOTH WOTH WOTH WOTH
C6 C6 C6 C5 C4 C3 C2 C1 C2 C1 C0 BF BE BB BB BB BA BB BB BB BB BB BB BB BB BB	BCON NMISR NMICON EXICONI  EXICONO IRCON2 IRCON2 IRCON0 IRCON0 IRCON0 MODPISEL  P3_DIR P3_DATA  CCU6_CMPMODIFL CCU6_ISRH CCU6_ISRH CCU6_ISRH CCU6_ISRL  P2_DIR P2_DATA CCU6_MCMOUTSL CCU6_TCTA4H CCU6_CC63SRL  P5_DIR P5_DATA CCU6_CC63SRL	FEAH FEAL PASSWD CMCON  PLL CON OSC CON PMCON1 PMCON0 ID P3_PUDEN P3_PUDEN P3_PUDSEL  CCU6_TCTR0H CCU6_TT2DTCH CCU6_TT2DTCH CCU6_TT2PTH CCU6_TT3PRH CCU6_TT3PRH CCU6_TT3PRH CCU6_TCU6_TCU6_TCU6_TCU6_TCU6_TCU6_TCU6_	P3_ALTSEL0  CCU6_MCMCTR CCU6_PSLR CCU6_ISSL  P5_ALTSEL1 P5_ALTSEL1 P5_ALTSEL1 P5_ALTSEL1	T2. T2L T2. RC2H T2. RC2H T2. RC2H T2. RC2H T2. RC2H T2. RC2H T2. T2MOD T2. T2CON SOU_PAGE  MODSUSP  PMCON2 MODPISEL2  MODPISEL1  IRCON4 IRCON3 XADDRH PORT_PAGE P3 OD SSC_BRH SSC_BRH SSC_BRH SSC_FIBL SSC_CONL SSC_FIBL SSC_CONL SSC_SSC_SSC_SSC_SSC_SSC_SSC_SSC_SSC_SSC	ENO  EO  CONO  THI THO THO THO TO THO THO THO THO THO THO			T21 T2L T21 RC24 T21 RC24 T21 RC24 T21 RC24 T21 T2NOD T21 T2CON WOTH WOTH WOTH WOTH WOTH WOTH WOTH WOTH
C6 C6 C6 C5 C4 C3 C2 C1 C1 C0 BF BE BB	BCON NMISR NMICON EXICONI  EXICONO IRCON2 IRCON2 IRCON0 IRCON0 IRCON0 MODPISEL  P3_DIR P3_DATA  CCU6_CMPMODIFL CCU6_ISRH CCU6_ISRH CCU6_ISRH CCU6_ISRL  P2_DIR P2_DATA CCU6_MCMOUTSL CCU6_TCTA4H CCU6_CC63SRL  P5_DIR P5_DATA CCU6_CC63SRL	FEAH FEAL PASSWD CMCON  PLL CON OSC CON PMCON1 PMCON0 ID P3_PUDEN P3_PUDEN P3_PUDSEL  CCU6_TCTR0H CCU6_TT2DTCH CCU6_TT2DTCH CCU6_TT2PTH CCU6_TT3PRH CCU6_TT3PRH CCU6_TT3PRH CCU6_TCU6_TCU6_TCU6_TCU6_TCU6_TCU6_TCU6_	P3_ALTSEL0  CCU6_MCMCTR CCU6_PSLR CCU6_ISSL  P5_ALTSEL1 P5_ALTSEL1 P5_ALTSEL1 P5_ALTSEL1	T2. T2L T2. RC2H T2. RC2H T2. RC2H T2. RC2H T2. RC2H T2. RC2H T2. T2MOD T2. T2CON SOU_PAGE  MODSUSP  PMCON2 MODPISEL2  MODPISEL1  IRCON4 IRCON3 XADDRH PORT_PAGE P3 OD SSC_BRH SSC_BRH SSC_BRH SSC_FIBL SSC_CONL SSC_FIBL SSC_CONL SSC_SSC_SSC_SSC_SSC_SSC_SSC_SSC_SSC_SSC	ENO  EO  CONO  HI  FLI  LLO  MOD  MOD			T21 T2L T21 RC24 T21 RC24 T21 RC24 T21 RC24 T21 T2NOD T21 T2CON WOTH WOTH WOTH WOTH WOTH WOTH WOTH WOTH
C6 C6 C6 C5 C4 C3 C1 C2 C1 C2 C1 C0 BF BE BB	BCON NMISR NMICON EXICON1  EXICON0 IRCON2 IRCON0 IRCON1 IRCON0 MODPISEL  P3_DIR P3_DATA  CCU6_CMPMODIFH CCU6_ISRH CCU6_ISRH CCU6_ISRH CCU6_ISRH CCU6_ISRH CCU6_CGSSRH  CCU6_CCGSSRH CCU6_CCGSSRH CCU6_CCGSSRH CCU6_CCGSSRH P1_DIR P5_DATA P1_DIR P1_DATA	FEAH FEAL PASSWD CMCON  PLL CON OSC CON PMCON1 PMCON0 ID  P3 PUDEN P3 PUDEN P3 PUDSEL  CCU6 T12DTCL  P2 PUDSEL CCU6 T12DTCL  P2 PUDSEL CCU6 T12PTC CCU	P3_ALTSEL0  CCU6_MCMCTR CCU6_PSLR CCU6_PSLR CCU6_ISSL	T2. T2L T2. RC2H T2. RC2H T2. RC2H T2. RC2H T2. RC2H T2. RC2H T2. T2MOD T2. T2CON SOU_PAGE  MODSUSP  PMCON2 MODPISEL2  MODPISEL1  IRCON4 IRCON3 XADDRH PORT_PAGE P3 OD SSC_BRH SSC_BRH SSC_BRH SSC_FIBL SSC_CONL SSC_FIBL SSC_CONL SSC_SSC_SSC_SSC_SSC_SSC_SSC_SSC_SSC_SSC	ENO  EO  CONO  THI THO THO THO TO THO THO THO THO THO THO			T21 T2L T21 R024 T21 R024 T21 R024 T21 R024 T21 R024 T21 T2MOD T21 T2CON WDTH WDTL WDTWINB WDTREL WDTCON  MD5 MR5 MD4 MR4 MD3 MR3 MD2 MR2 MD1 MR1 MD0 MR0 MD0 MR0 MDUSTAT  CD CON CD STATC CD CORD2L CD CORD2H CD CD CORD2H CD C
C6 C6 C6 C6 C5 C4 C3 C2 C1 C1 C1 C2 C1 BF BE BB	BCON NMISR NMICON EXICON1  EXICON0 IRCON2 IRCON0 IRCON1 IRCON0 MODPISEL  P3_DIR P3_DATA  CCU6_CMPMODIFH CCU6_ISRH CCU6_ISRH CCU6_ISRH CCU6_ISRH CCU6_ISRH CCU6_CGSSRH  CCU6_CCGSSRH CCU6_CCGSSRH CCU6_CCGSSRH CCU6_CCGSSRH P1_DIR P5_DATA P1_DIR P1_DATA	FEAH FEAL PASSWD CMCON  PLL CON OSC CON PMCON1 PMCON0 ID  P3 PUDEN P3 PUDEN P3 PUDSEL  CCU6 T12DTCL  P2 PUDSEL CCU6 T12DTCL  P2 PUDSEL CCU6 T12PTC CCU	P3_ALTSEL0  CCU6_MCMCTR CCU6_PSLR CCU6_PSLR CCU6_ISSL	T2, T2L T2, T2MC2H T2, FRC2H T2, FRC2H T2, FRC2H T2, T2MC0D T2, T2CON SCU_PAGE  MODSUSP  PMCON2 MODPISEL2  IRCON4 IRCON3 XADDRH PORT_PAGE P3 OD SSC_BRH SSC_BRH SSC_BRH SSC_BRH SSC_FIBL SSC_CONL SSC_FIBL SSC_SONL SSC_FIBL SSC_CONL SSC_FIBL SSC_CONL SSC_FIBL SSC_CONL SSC_FIBL SSC_CONL SSC_FIBL SSC_CONL SSC_FIBL SSC_SONL SSC_FIBL SSC_FIBL SSC_CONL SSC_FIBL SSC_SONL SSC_FIBL SSC_SONL SSC_FIBL SSC_SONL SSC_FIBL SSC_SONL SSC_FIBL SSC_FIB	ENO  EO  CONO  THI THO THO THO TO THO THO THO THO THO THO			T21 T2L T21 RC2H T21 RC2H T21 RC2H T21 RC2CH T21 T2MOD T21 T2CON WDTH WDTL WDTWINB WDTREL WDTCON  MD5 MR5 MD4 MR4 MD3 MR3 MD2 MR2 MD1 MR1 MD0 MR0 MD0 MR0 MD0 MR0 CD CORD MDUSTAT  CD CORD CD STATC CD CORD CD C

		Interrupt Vector Addresses		
Interrupt Mode	Vector Address	Assignment for XC888	Enable Bit	SFR
NMI	0073h	Watchdog Timer NMI	NMIWDT	NMICON
		PLL NMI	NMIPLL	
		FLASH NMI	NMIFLASH	
		VDDC Prewarning NMI	NMIVDD	
		VDDP Prewarning NMI	NMIVDDP	
		FLASH ECC NMI	NMIECC	
XINTRO	0003h	External interrupt 0	EX0	IEN0
XINTR1	000Bh	Timer 0	ETO	
XINTR2	0013h	External interrupt 1	EX1	1
XINTR3	001Bh	Timer 1	ET1	1
XINTR4	0023h	UART	ES	1
XINTR5	002Bh	T2	ET2	7
		UART Fractional devider		
		(normal divider overflow)		
		MultiCAN Node 0		
		LIN		
XINTR6	0033h	MultiCAN NOdes 1 and 2	EADC	IEN1
		ADC[1:0]		
XINTR7	003Bh	SSC	ESSC	1
XINTR8	0043h	External Interrupt 2	EX2	1
		T21		
		CORDIC		
		UART 1		
		UART 1 Fractional Devider		
		(normal divider overflow)		
		MDU [1:0]		
XINTR9	004Bh	External Interrupt 3	EXM	1
		External Interrupt 4		
		External Interrupt 5		
		External Interrupt 6		
		MultiCAN Node 3		
XINTR10	0053h	CCU6 INPO	ECCIP0	1
		MultiCAN Node 4		
XINTR11	005Bh	CCU6 INP1	ECCIP1	1
		MultiCAN Node 5		
XINTR12	0063h	CCU6 INP2	ECCIP2	1
		MultiCAN Node 6		
XINTR13	006Bh	CCU6 INP3	ECCIP3	1
· ··· · · · · · · <del>· · · · · · · · · · </del>		MultiCAN Node 7	=======	



Note: The pins shaded in blue are not available in the PG-TQFP-48 package.

