

CDA 3201 Computer Logic Design Fall 2016

Homework 5

Points: 100

Questions 1 to 5: 17 points each Question 6: 15 points

1. A Mealy Finite State Machine (FSM) has two binary inputs X_1 and X_2 and one output. The machine outputs a 0 and resets to 00 state whenever it receives two consecutive input strings that are identical (for example 01 followed by 01). In all other cases it outputs a 1. Use the following convention to label each state:

Label the state as PQ if it is reached after receiving two input strings $X_1X_2=P$ and $X_1X_2=Q$ where P and Q are the decimal values of X_1X_2 . Note that P and Q range from 0 to 3; for example, if the previous two inputs to a state are 01 and 11 it is labeled as 13. For states which are children of 00 (reset) use $P=0$ irrespective of how the 00 state is reached.

Draw the FSM clearly labeling all inputs, outputs and state names, but, to decrease clutter, DO NOT draw any outgoing transitions for states 20, 21, 23, 30, 31, 32. Hint: the FSM has more than 10 states but its structure is simple and repetitive.

2. A sequential machine operates with an overlapping sliding window and has 1 input (X) and two outputs (Z1 and Z2) which have a default value of 1. An output $Z_1=0$ occurs every time the input sequence 100 is completed provided that the sequence 011 has never occurred. An output $Z_2=0$ occurs every time the input 011 has occurred. But once the sequence 011 has occurred, Z_1 is permanently reset to 1 and will not change even if a sequence of 100 occurs. Draw the Mealy state graph with no more than 8 states and the corresponding state table.

Example input : 100110011. Corresponding Z_1 output: 110111111; Z_2 output: 111101110.

3. A Moore machine has an input (X) and outputs (Y and Z). YZ represents a 2 bit binary number equal to the number of 1's that have been received as inputs. The circuit resets when the total number of 1's received is 3 or when the total number of 0's received is 3. Draw the state graph and state transition table for the machine.
4. A FSM receives one bit of data at each clock cycle and outputs a 1 when the sequence 11 or 1001 is received. It resets to start state after detecting either one of these two sequences.
 - (a) Draw the Mealy state diagram.
 - (b) Implement the FSM using D flip flop by deriving the minimized next state and output logic functions.
5. The decimal digits 0 through 9 are encoded as 4-bit binary numbers. They are transmitted in disjoint windows of length 4 with the least significant bit first and are input to a Mealy circuit. The circuit generates an output of 1(0) when the fourth bit is received if the 4 bits have been even (odd) parity; the circuit output is a Don't-Care for the first 3 bits. Construct an incompletely specified table for the circuit.
6. Design the state diagram for the control unit of a coin-operated Coke machine. Coke costs 125 cents and the machine accepts quarters and dollars. Change should be returned if more than 125

cents is deposited. Assume that the machine dispenses the product and change, if any, and resets once at least 125 cents are deposited.