NAME: __Solutions__ **UNumber:**_____ **Computer Logic Design**

Duration: 75 Minutes **CDA 3201** **November 5, 2015**

Closed Book, Notes, HW **Exam 2** **R. Kasturi**

One sheet of Letter size paper written on front and back is allowed.

SHOW ALL WORK TO GET PARTIAL CREDIT. MAKE REASONABLLE ASSUMPTIONS.

I (One point each) Answer True or False. Unless otherwise noted, all numbers are in decimal.

_F_ a. The number of states in a Finite State Machine is equal to the number of D flip flops used.

_F_ b. The number of arcs in a Mealy machine cannot exceed the number of states.

_F_ c. A 3-bit Johnson counter (3-bit shift register with its output connected back to the input through an inverter) and starts from 000 state will only sequence through 3 other states before repeating.

_F_ d. The output propagation delay of each flip flop in a FSM must be at least equal to or greater than the clock period for proper operation.

_F_ e. If a circuit has both Static 0 and Static 1 hazard then it is said to exhibit Dynamic hazard.

_T_ f. When an odd number of inverters are cascaded (i.e., output of the first inverter is connected to input of the second and so on and the output of the last inverter connected back to the input of the first one) we get an oscillating circuit (i.e., each flip flop changing between 0 and 1 states endlessly.

_T_ g. A 3 to 8 line decoder plus an 8 input OR gate are adequate to realize any function of 3 variables.

_T_ h. A ROM includes a built-in decoder that maps the address lines into word select lines of the memory array.

_T_ i. In a Programmable Array Logic (PAL), the AND array is programmable but the OR array is fixed.

_F_ j. If an edge triggered D flip flop is replaced with a T flip flop, it responds to input changes at both rising and falling edges.

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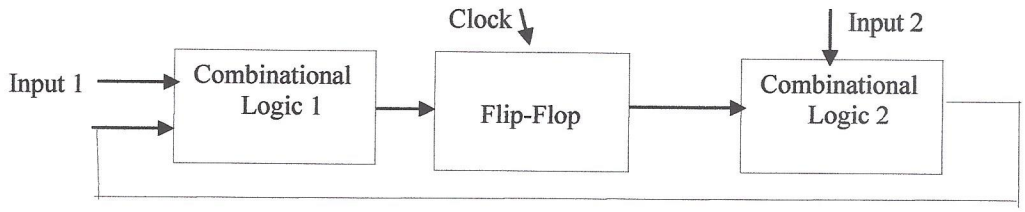
II (a) (5 points) Consider the following sequential logic circuit block diagram. Typical propagation delay through **each** combinational logic circuit is 0.1 ns but the worst case delay is 0.2 ns. Setup time for flip flop is 0.2 ns, hold time is 0.3 ns, and the propagation delay through flip flop is 0.4 ns. Calculate the highest possible clock frequency for proper operation.



Total Worst-case Delay $= T_{CL1}^{(MAX)} + T_{PD} + T_{SU} + T_{CL2}^{(MAX)}$

(Refer to Fig. 13.18 in the Book) $= 0.2 + 0.4 + 0.2 + 0.2$

$= 1\ nS. =$ clock Period 'T'

Highest Possible Clock Frequency for Proper Operation

$= \frac{1}{T} = \frac{1}{1 \cdot 10^{-9}}\ Hz = 1\ GHz.$

(b) (5 points) The R and S inputs to an RS Latch changes values after each second. The initial values are (R=1,S=0) and then changes in the following sequence: (R=0,S=0), (0,1), (1,1), (1,0), (1,1), (0,0), and then remains unchanged. Sketch the corresponding value of its Q output. Explain any anomalous behavior.

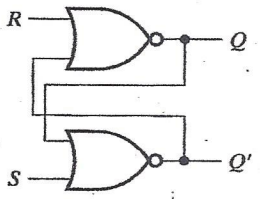
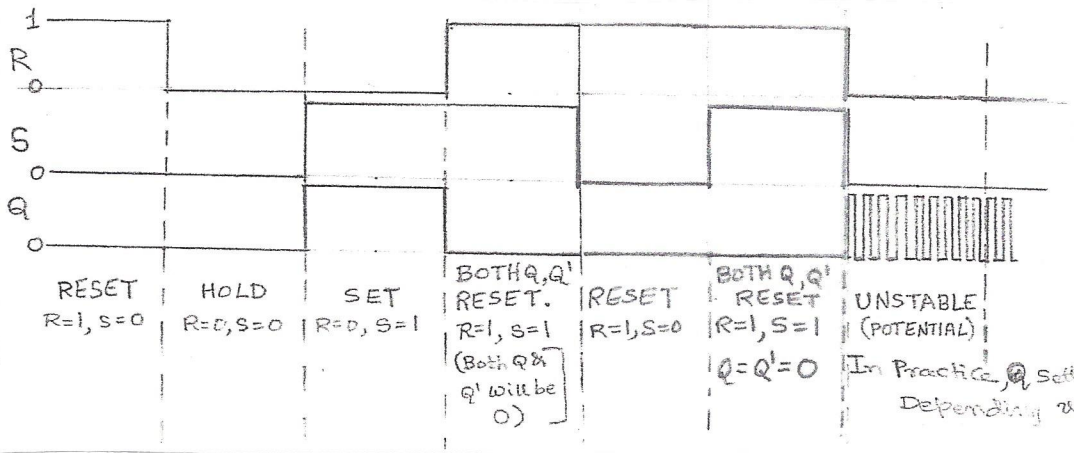


Figure 6.5 ***R-S* latches.**



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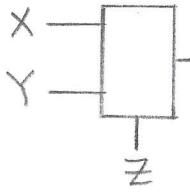
III (a) (5 points) A full adder takes A, B, C_I as inputs and outputs the sum S and carry-out C_O. Complete the truth table. Write expressions for S and C_O in sum of products form. Implement the full adder using only three 2:1 multiplexers and one inverter.

A	B	C_I	S	C_O
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

$$S = \bar{A}\bar{B}C_I + \bar{A}B\bar{C}_I + A\bar{B}\bar{C}_I + ABC_I$$

$$C_O = \bar{A}BC_I + A\bar{B}C_I + AB\bar{C}_I + ABC_I$$

The output of a 2:1 MUX has the form,



So we need to Rewrite S and C_O in this form.

$$S = (\bar{A}B + A\bar{B})\bar{C}_I + (\bar{A}\bar{B} + AB)C_I$$

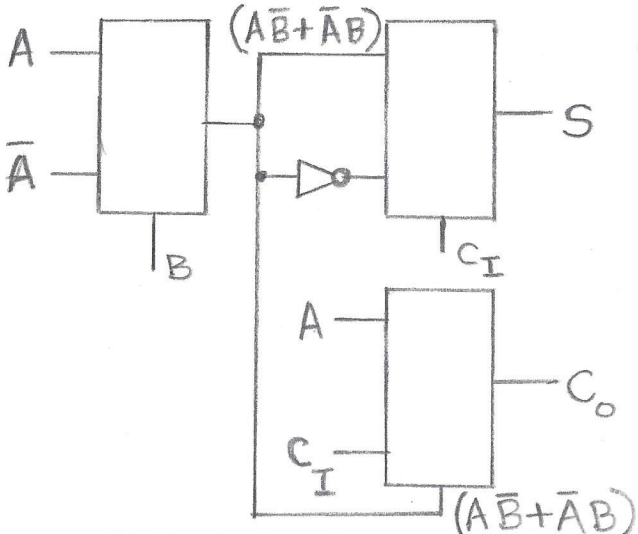
But $(\bar{A}\bar{B} + AB) = \overline{(\bar{A}B + A\bar{B})}$.

Thus $$S = (\bar{A}B + A\bar{B})\bar{C}_I + \overline{(\bar{A}B + A\bar{B})}C_I$$

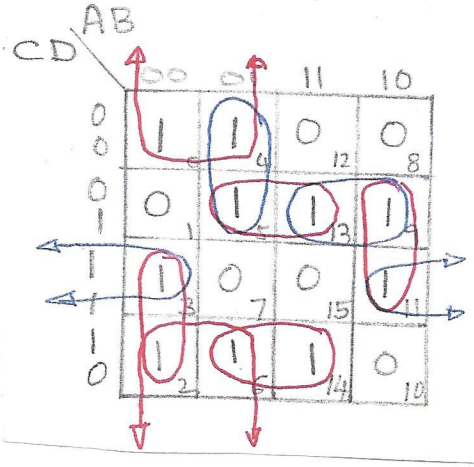
Similarly,

$$C_O = (A\bar{B} + \bar{A}B)C_I + AB$$
$$= (A\bar{B} + \bar{A}B)C_I + A(\bar{A}\bar{B} + AB)$$
$$= C_I(A\bar{B} + \bar{A}B) + A.\overline{(A\bar{B} + \bar{A}B)}$$

These lead to the Circuit on left.



(b) (5 points) Implement $F(A, B, C, D) = \sum m(0,2,3,4,5,6,9,11,13,14)$ as a hazard-free circuit and write the corresponding Boolean expression.



MINIMUM COVER (as Shown in RED)

$$= \bar{A}\bar{D} + B\bar{C}D + A\bar{B}D + \bar{A}\bar{B}C + BC\bar{D}$$

To make it HAZARD-FREE add terms (as shown in BLUE)

$$= \bar{A}B\bar{C} + A\bar{C}D + \bar{B}CD$$

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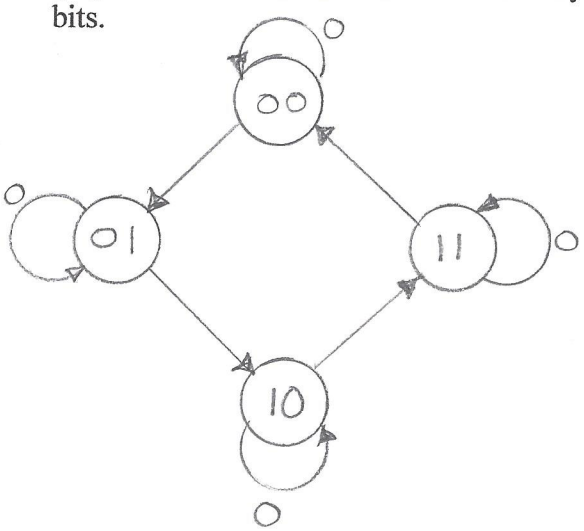
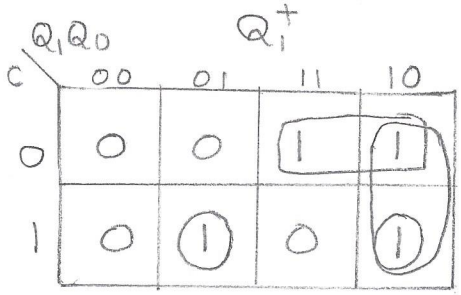
IV (a) (5 points) A two bit up counter has one input C and no additional outputs other than the two state bits, Q1 and Q0. When C=0 the counter holds its present value. When C = 1 it transitions from 00 to 01 to 10 to 11 and back to 00 after each clock. Draw the state transition graph and the state transition table clearly showing the input, present state bits, and next state bits.



INPUT	PRESENT $Q_1 Q_0$	NEXT $Q_1^+ Q_0^+$
0	00	00
1	00	01
0	01	01
1	01	10
0	10	10
1	10	11
0	11	11
1	11	00

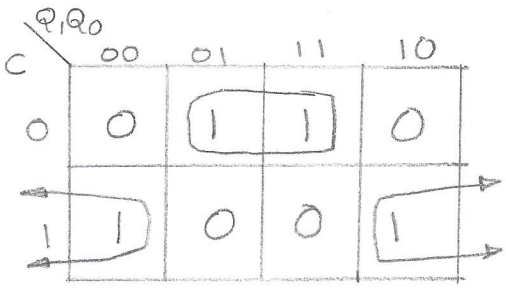
(b) (5 points) Design the counter using D flip-flops and additional logic as needed. i.e., derive the expressions for the D inputs in terms of C, Q1 and Q0 using K Maps. Assume that the flip flops have no other control inputs such as Set, Reset, or Load. Draw the logic circuit diagram.



$$D_1 = Q_1^+ = Q_1' Q_0 C + Q_1 C' + Q_1 Q_0'$$
$$= Q_1' Q_0 C + Q_1 Q_0' C + Q_1 C'$$

This helps to write as XOR

$$= C(Q_1 \oplus Q_0) + Q_1 C'$$



$$D_0 = Q_0^+ = Q_0 C' + Q_0' C$$
$$= Q_0 \oplus C$$