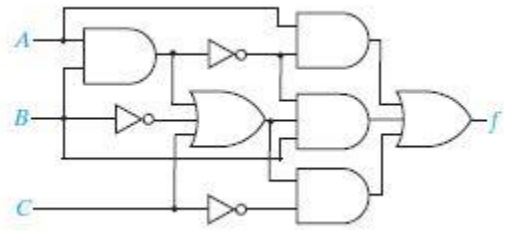
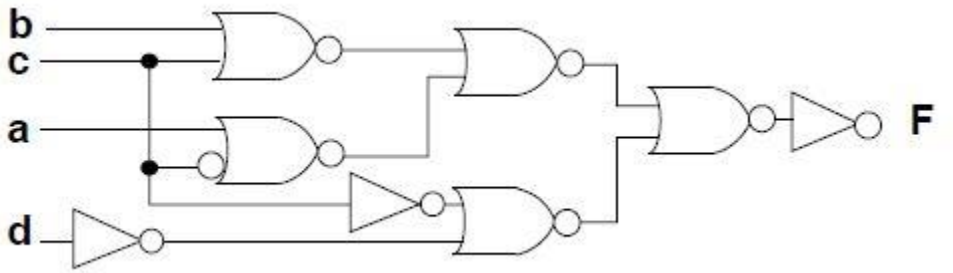
CDA Computer Logic Design
Homework 3

Points: 100

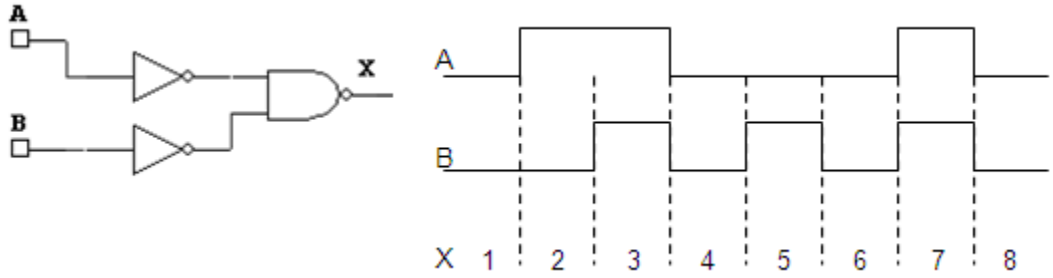
1) Implement the below logic circuit by using only NAND gates. (Do not simplify except to delete two inverters in series, if any) (15 points)



2) a) Find the hazards in the below circuit (5 points)
b) Modify the circuit so that it is hazard free (10 points)

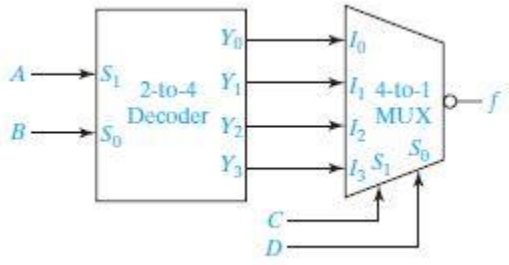


3) Complete the timing diagram for the given circuit. Assume that all gates have a propagation delay of 1 ns (10 points)



4) Implement a full adder
(a) using two 8-to-1 MUXes. Connect X,Y, and Cin to the control inputs of the MUXes and connect 1 or 0 to each data input. (5 points)
(b) using two 4-to-1 MUXes and one inverter. Connect X and Y to the control inputs of the MUXes, and connect 1's, 0's, Cin, or C'in to each data input. (5 points)
(c) again using two 4-to-1 MUXes, but this time connect Cin and Y to the control inputs of the MUXes, and connect 1's, 0's, X, or X' to each data input. Note that in this fashion, any N-variable logic function may be implemented using a 2(N−1)-to-1 MUX. (5 points)

5) The circuit below has a 2-to-4 decoder with active high outputs connected to a 4-to-1 MUX with an active low output. Derive a minimum SOP or a minimum POS expression for the output, f(A, B, C, D). (15 points)



6) Show how to make an 8-to-1 MUX using a PAL. Assume that PAL has 14 inputs and six outputs and assume that each output OR gate may have up to four AND terms as inputs, as in Figure 9-33. (Hint: Wire some outputs of the PAL around to the inputs, external to the PAL. Some PALs allow this inside the PAL to save inputs.) (15 points)

7) The following PLA will be used to implement the following equations:
X = AB'D + A'C' + BC + C'D'
Y = A'C' + AC + C'D'
Z = CD + A'C' + AB'D
(a) Indicate the connections that will be made to program the PLA to implement these equations. (7 points)
(b) Specify the truth table for a ROM which realizes these same equations. (8 points)