

HW 4 Solution

1. What are the main functions of the CPU?

Ans.

The CPU is responsible for fetching program instructions, decoding each instruction that is fetched and performing the indicated sequence of operations on the correct data.

2. How is the ALU related to the CPU? What are its main functions?

Ans.

The ALU is part of the CPU. It carries out arithmetic operations (typically only integer arithmetic) and can carry out logical operations such as AND, OR, and XOR, as well as shift operations.

3. How many bits are required to address a $4M \times 32$ main memory if

- i. Main memory is byte-addressable?
- ii. Main memory is word-addressable?

Ans.

- a. There are $4M \times 4$ bytes which equals $2^2 \times 2^{20} \times 2^2 = 2^{24}$ total bytes, so 24 bits are needed for an address
 - b. There are $4M$ words which equals $2^2 \times 2^{20} = 2^{22}$, so 22 bits are required for an address
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4. How many bits are required to address a $2M \times 8$ main memory if

- i. Main memory is byte-addressable?
- ii. Main memory is word-addressable?

Ans.

- a. There are $2M \times 1$ bytes, or 2×2^{20} total bytes, so 21 bits are needed for an address
 - b. There are $2M$ words, or 2×2^{20} total words, so 21 bits are required for an address
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5. Assume a 2^{21} byte memory:

- a. What are the lowest and highest addresses if memory is byte-addressable?
- b. What are the lowest and highest addresses if memory is word-addressable, assuming a 16-bit word?
- c. What are the lowest and highest addresses if memory is word-addressable, assuming a 32-bit word?

Ans.

- a. There are 2^{21} bytes, which can all be addressed using addresses 0 through $2^{21}-1$ with 21 bit addresses or 0000.....0000 to 111.....111 (21 **0 and 1**)
 - b. There are only 2^{20} words and addressing each requires using addresses 0 through $2^{20}-1$
 - c. There are only 2^{19} words and addressing each requires using addresses 0 through $2^{19}-1$
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- Problem 6

16. Explain the steps of the fetch-decode-execute cycle. Your explanation should include what is happening in the various registers.

Ans.

Fetch: Load the PC into the MAR; fetch the instruction and place it into the IR; increment PC by 1;

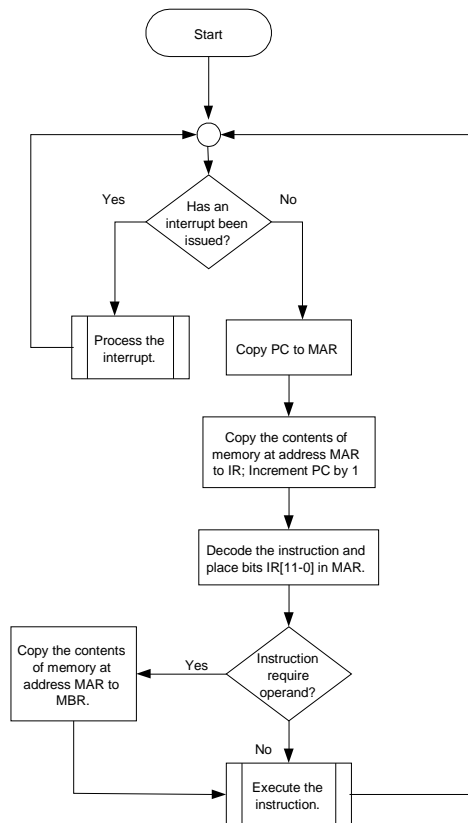
Decode: Decode the instruction using IR[15-12]; if necessary, place IR[11-0] into MAR and fetch operand, placing result into MBR;

Execute: Execute instruction

- Problem 7

Combine the flowcharts that appear in Figures 4.11 and 4.12 so that the interrupt checking appears at a suitable place.

Ans.



- Problem 8

Explain why, in MARIE, the MAR is only 12 bits wide while the AC is 16 bits wide.

Hint: Consider the difference between data and addresses

Ans.

MARIE can handle 16-bit data, so the AC must be 16 bits wide. However, MARIE's memory is limited to 4096 address locations, so the MAR only needs to be 12 bits wide to hold the largest address.

- Problem 9: Use a few sentences to answer each of the following questions. The answers can be found in section 4.1 to 4.7 in the textbook.

1. What purpose does the datapath in a CPU serve?

Datapath of a CPU is a network of registers and ALUs connected by buses. It provides temporary storage of data and functional units for transforming data.

2. What does the control unit in a CPU do?

The control unit of a CPU is in charge of sequencing operations performed by the datapath, and makes sure that correct data are where they need to be at the correct time.

3. Where are registers located and what are the different types?

Registers are located in the datapath of a CPU. There are special-purpose registers that holds some particular type of information all the time, and general-purpose registers that can hold various types of information. Special-purpose registers are solely controlled by the CPUs, and programers do not have accesses to them. General-purpose registers are exposed and manipulated by programers so that the programmers can use these registers in their programs. In addition, there are status registers which hold status of information as the results of operations performed by the CPU. These are also specialpurpose registers.

4. How does the ALU know which function to perform? the ALU knows which operation to perform as it is controlled by the signals coming from the control unit.

5. Explain the differences between data buses, address buses, and control buses.

a data bus is the collection of wires that specifically carries data, which is the actual information that needs to be moved from one location in a CPU to another. An address bus is a collection of wires that carries address information for accessing memory or register IDs for accessing specific registers. A control bus is the collection of wires carries the information specifying the particular operations that need to be performed by the ALU, or read/write operations that need to be performed by the memory, or IO requests for IO communications, etc.

6. Explain the relation between clock cycle time and clock frequency.

Clock cycle time means the amount time each clock cycle takes, while the clock frequency is the reciprocal of the cycle time. For example, an 1 GHz clock signal has a cycle time of 1 ns.

7. Explain the differences between memory-mapped I/O and instruction-based I/O. See page 203 for explanation.

8. Explain the differences between byte addressable and word addressable. See page 204 for explanation.

9. Explain what interrupts are, and list four reasons that trigger interrupts. See page 208 - 209 for explanation.