

## Lab Final

### State Diagram:

Two inputs:

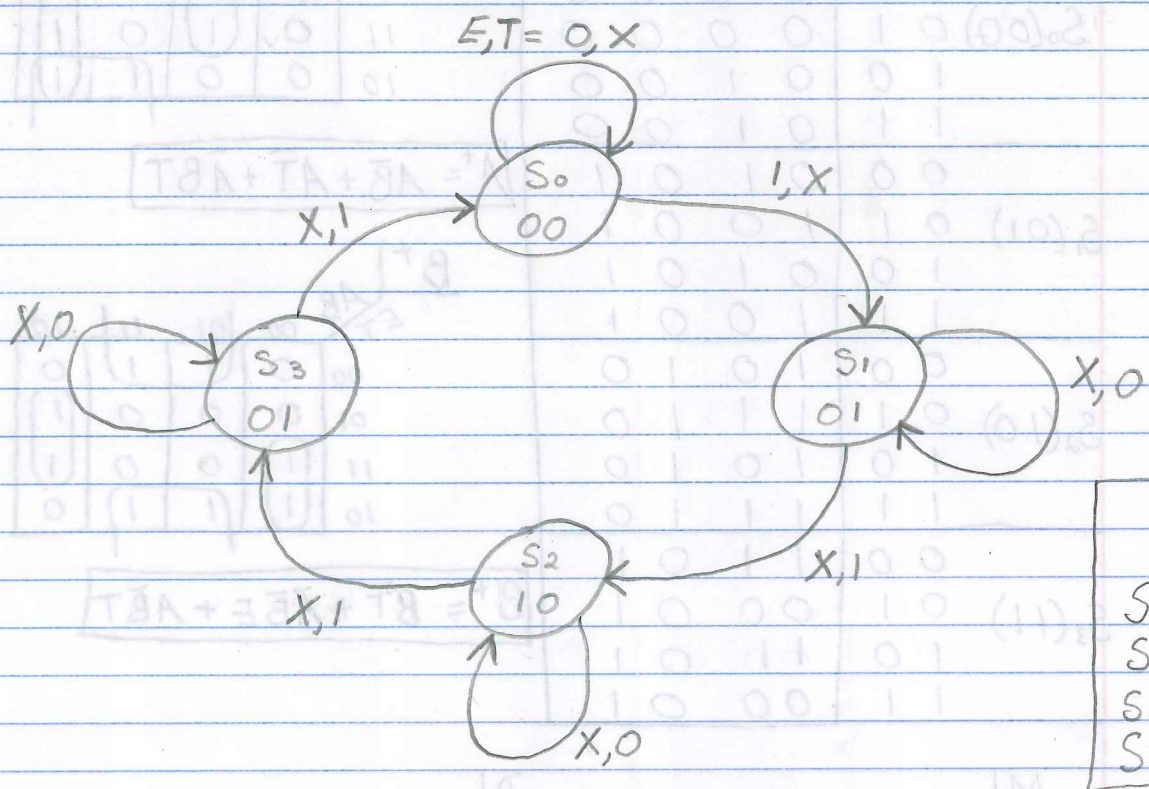
$E$  = enable bit

$T$  = Terminal Counter bit that comes from LS/63 chip. Chip outputs a 1 when 4s have passed

Two outputs:

$M$  = outputs 1 when moving & 0 when not (MSB)

$D$  = outputs 1 when door open & 0 when closed (LSB)



$S_0$ : Idle state, not moving & door closed

$S_1$ : Enable input received, door open for 4 seconds before moving

$S_2$ : Elevator moving for 4s, door closed

$S_3$ : Elevator stops moving & opens door for 4s then goes idle

\* Floor changes through a combinational circuit that receives the outputs for state  $S_2$  of  $M=1$  &  $D=0$  together with  $T=1$  input bit. Logic will output a 1 to a TFF on this condition



## State Table:

Present State	Next State				Output M, D
	E, T = 00	E, T = 01	E, T = 11	E, T = 10	
S <sub>0</sub>	S <sub>0</sub>	S <sub>0</sub>	S <sub>1</sub>	S <sub>1</sub>	0 0
S <sub>1</sub>	S <sub>1</sub>	S <sub>2</sub>	S <sub>2</sub>	S <sub>1</sub>	0 1
S <sub>2</sub>	S <sub>2</sub>	S <sub>3</sub>	S <sub>3</sub>	S <sub>2</sub>	1 0
S <sub>3</sub>	S <sub>3</sub>	S <sub>0</sub>	S <sub>0</sub>	S <sub>3</sub>	0 1

## Truth Table:

A	B	E	T	A <sup>+</sup>	B <sup>+</sup>	M	D
<b>S<sub>0</sub> (00)</b>							
0	0	0	0	0	0	0	0
0	1	0	1	0	0	0	0
1	0	0	1	0	1	0	0
1	1	0	1	0	1	0	0
<b>S<sub>1</sub> (01)</b>							
0	0	0	1	0	1	0	1
0	1	1	0	1	0	0	1
1	1	1	0	1	0	0	1
<b>S<sub>2</sub> (10)</b>							
0	0	1	0	1	0	1	0
0	1	1	1	1	1	1	0
1	0	1	1	1	0	1	0
1	1	1	1	1	1	1	0
<b>S<sub>3</sub> (11)</b>							
0	0	1	1	0	1	0	1
0	1	0	0	0	0	0	1
1	0	1	1	1	1	0	1
1	1	0	0	0	0	0	1

A <sup>+</sup>	AB			
ET	00	01	11	10
00	0	0	1	1
01	0	1	0	1
11	0	1	0	1
10	0	0	1	1

$$A^+ = A\bar{B} + A\bar{T} + \bar{A}BT$$

B <sup>+</sup>	AB			
ET	00	01	11	10
00	0	1	1	0
01	0	0	0	1
11	1	0	0	1
10	1	1	1	0

$$B^+ = B\bar{T} + \bar{A}\bar{B}E + A\bar{B}T$$

M	AB			
ET	00	01	11	10
00	0	0	0	1
01	0	0	0	1
11	0	0	0	1
10	0	0	0	1

$$M = A\bar{B}$$

D	AB			
ET	00	01	11	10
00	0	1	1	0
01	0	1	1	0
11	0	1	1	0
10	0	1	1	0

$$D = B$$