Homework #4 (Covers Unit-11, Unit-12 and Unit-13)
CDA Computer Logic Design
Total Points: 100

Notes:

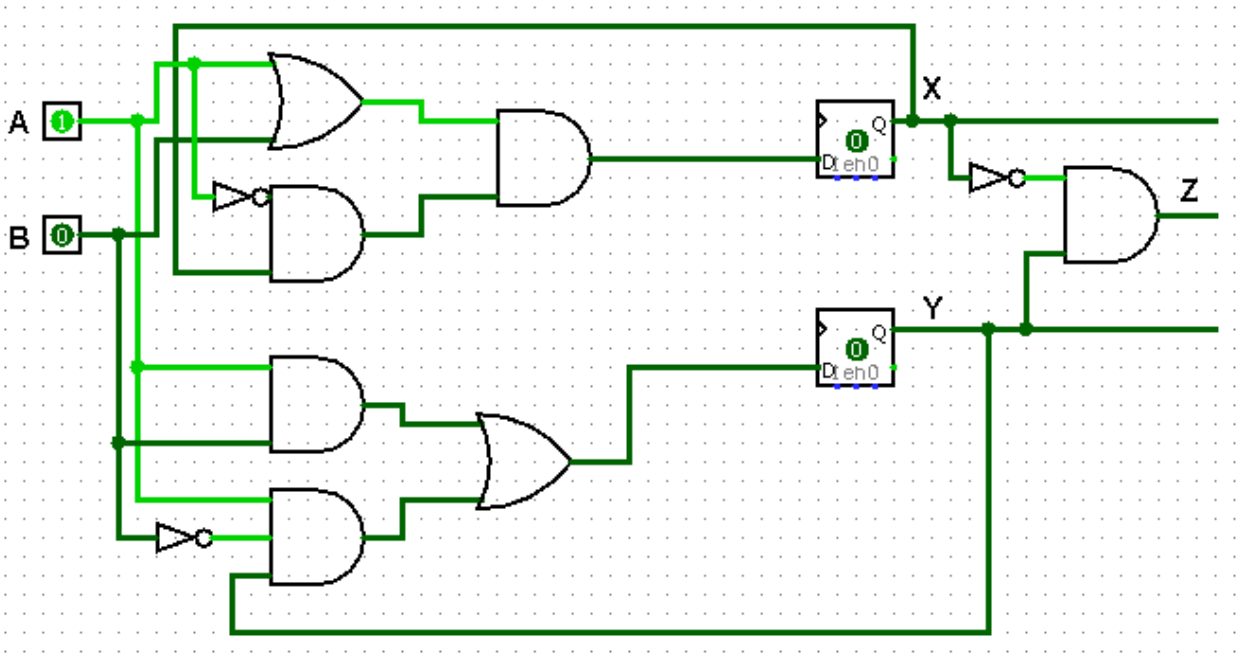
1. All homework should be done and submitted individually
2. Show all steps for each question to get full points (Use extra pages if required)
3. Submit electronically in canvas as a single pdf file
4. Follow instructions for each question
5. A' is the complement of A

Name: SOLUTIONS **UID:**

Q1. (3x5 points) A sequential circuit with two D flip-flops, X and Y; two inputs, A and B; and one output, Z, is specified by the following next-state and output equations:

$$X(t+1) = (A + B)(A'X)$$
$$Y(t+1) = AB + AB'Y$$
$$Z = X'Y$$

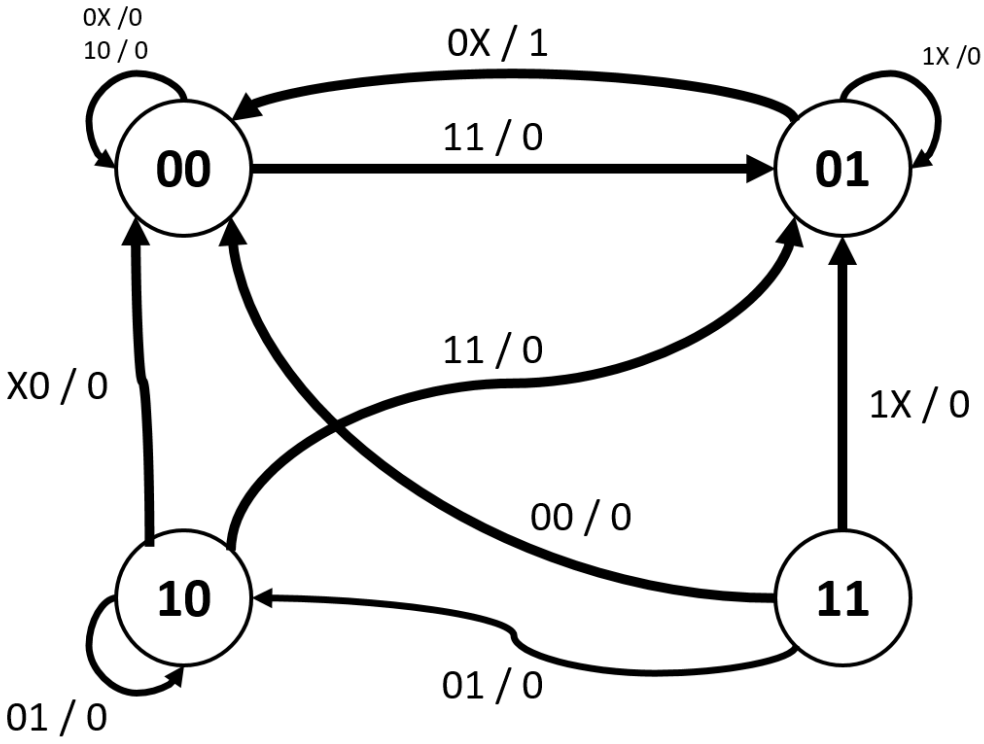
(a) Draw the logic diagram of the circuit



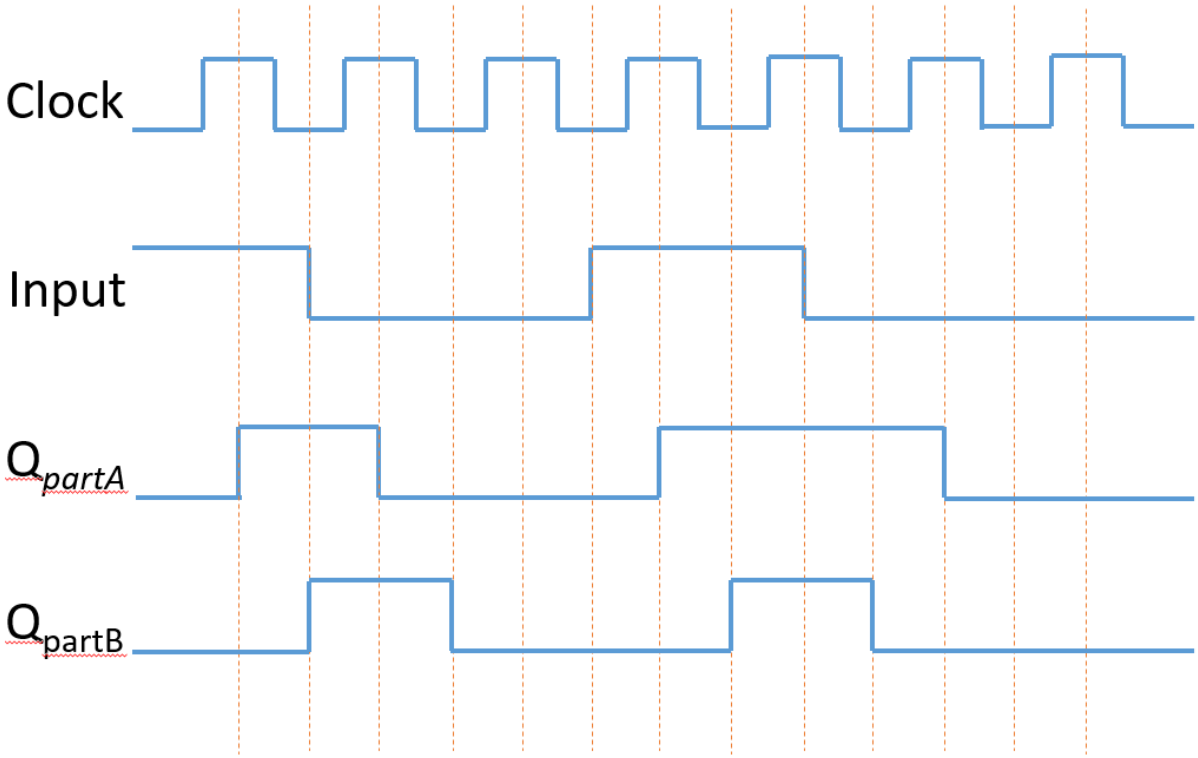
(b) Derive the state table

Present State		Inputs		Next State		Output
X	**Y**	**A**	**B**	**X**	**Y**	**Z**
0	0	0	0	0	0	0
0	0	0	1	0	0	0
0	0	1	0	0	0	0
0	0	1	1	0	1	0
0	1	0	0	0	0	1
0	1	0	1	0	0	1
0	1	1	0	0	1	1
0	1	1	1	0	1	1
1	0	0	0	0	0	0
1	0	0	1	1	0	0
1	0	1	0	0	0	0
1	0	1	1	0	1	0
1	1	0	0	0	0	0
1	1	0	1	1	0	0
1	1	1	0	0	1	0
1	1	1	1	0	1	0

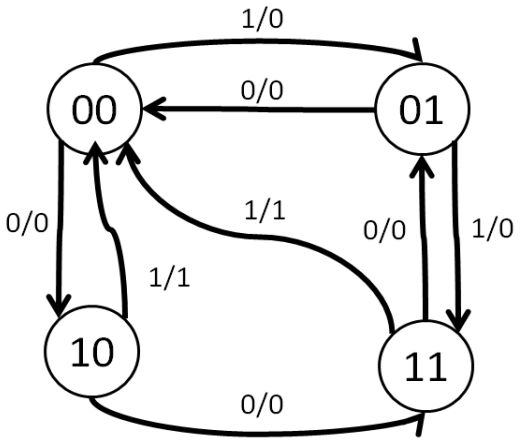
(c) Draw the corresponding state diagram



Q2. (2x5 points) Given the input and clock transitions, indicate the output of a D flip flop assuming:
(a) It is negative-edge triggered
(b) It is positive-edge triggered



Q3. (2x10 points) Given the state diagram below, (for reference: 0/0 → Input / Output)



(a) create the state table

Present State		Input	Next State D Inputs		Output
Q1	**Q2**	**I**	**D1**	**D2**	**O**
0	0	0	1	0	0
0	0	1	0	1	0
0	1	0	0	0	0
0	1	1	1	1	0
1	0	0	1	1	0
1	0	1	0	0	1
1	1	0	0	1	0
1	1	1	0	0	1

D1	Q1Q2			
Input I	00	01	11	10
0	1	0	0	1
1	0	1	0	0

D1 = Q2'I' + Q1'Q2I

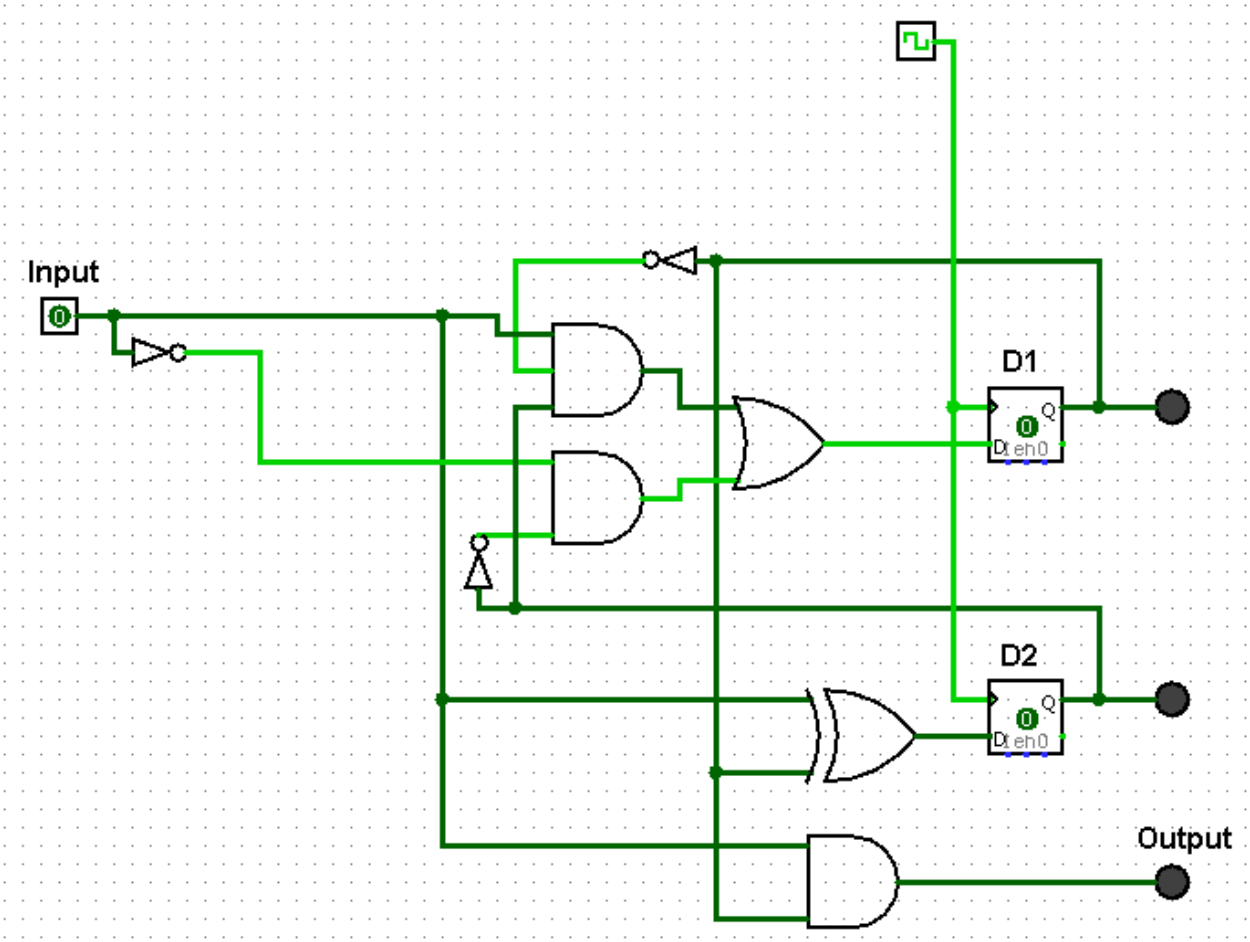
D2	Q1Q2			
Input I	00	01	11	10
0	0	0	1	1
1	1	1	0	0

D2 = Q1'I + Q1I' = I XOR Q1

Output	Q1Q2			
Input I	00	01	11	10
0	0	0	0	0
1	0	0	1	1

Output = Q1I

(b) create a sequential circuit design using only two D flip flops, and any additional simple logic gates (AND, OR, NOT, XOR, NAND, NOR)



Q4. (2x10 points) An A-B flip-flop behaves as follows:

If AB = 00, the flip-flop changes its current state,
If AB = 01, the flip-flop holds,
If AB = 10, the flip-flop is reset, i.e..Q=0
If AB = 11, the flip-flop changes its current state

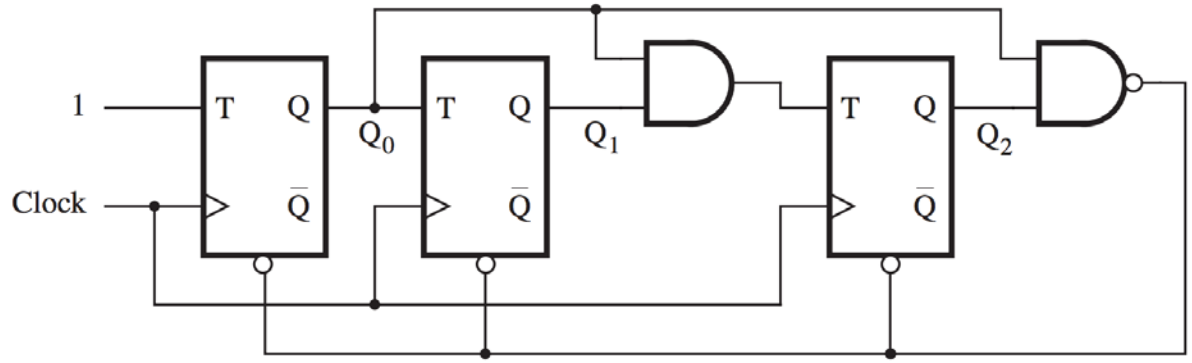
(a) Give the characteristic (next-state) equation for this flip-flop.

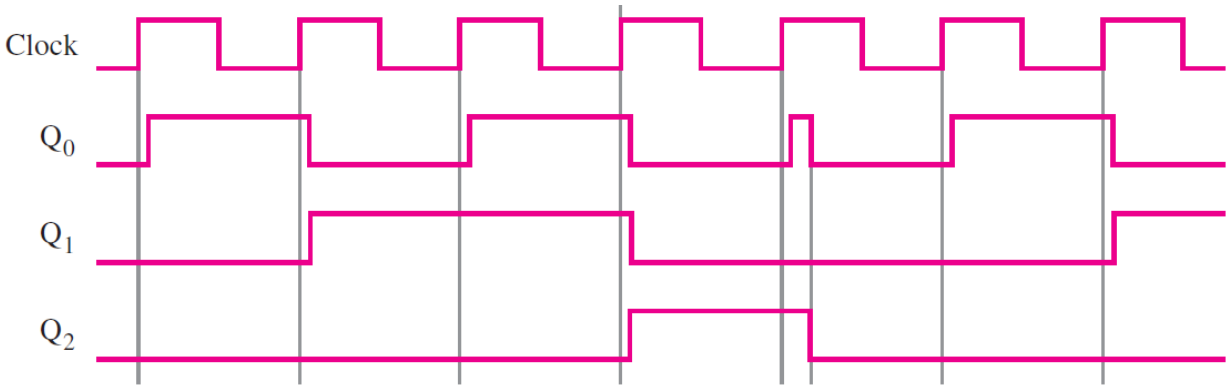
$Q^+ = A'B'Q' + A'BQ + ABQ'$

(b) Create the state table

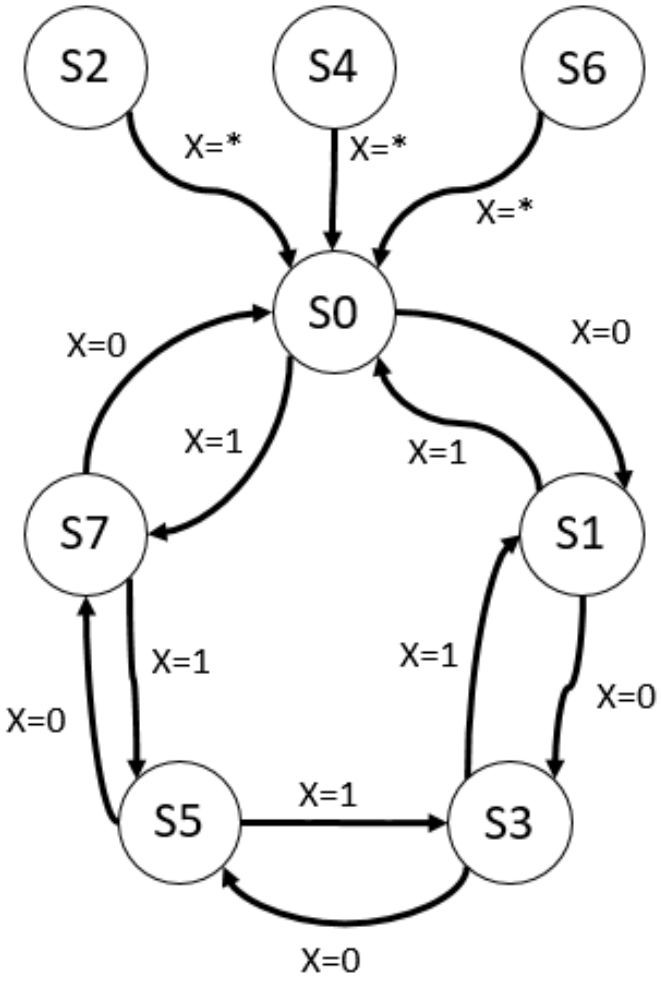
A	B	Present State	Next State
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0

Q5. (15 points) For the following circuit complete the timing diagram.





Q6. (2x10 points) Design a synchronous sequential circuit that will count through the sequence 0,1,3,5,7 when the control input, x=0; and through the sequence 7,5,3,1,0 when x=1. The circuit should return to state 0 if it falls into states 2, 4, or 6. Note: the sequence cycles – 0,1,3,5,7,0,1,3,…
(a) Draw a state diagram for the circuit



(b) Draw a state transition table for the circuit

X = 0							
Present State				Next State			
State	Flip-flop			State	Flip-flop		
	Q2	Q1	Q0		Q2	Q1	Q0
S0	0	0	0	S1	0	0	1
S1	0	0	1	S3	0	1	1
S2	0	1	0	S0	0	0	0
S3	0	1	1	S5	1	0	1
S4	1	0	0	S0	0	0	0
S5	1	0	1	S7	1	1	1
S6	1	1	0	S0	0	0	0
S7	1	1	1	S0	0	0	0

X = 1							
Present State				Next State			
State	Flip-flop			State	Flip-flop		
	Q2	Q1	Q0		Q2	Q1	Q0
S0	0	0	0	S7	1	1	1
S1	0	0	1	S0	0	0	0
S2	0	1	0	S0	0	0	0
S3	0	1	1	S1	0	0	1
S4	1	0	0	S0	0	0	0
S5	1	0	1	S3	0	1	1
S6	1	1	0	S0	0	0	0
S7	1	1	1	S5	1	0	1