CDA 3201L – Computer Logic Design Laboratory
Lab Exercise 1

Combinational Logic Circuits (I)

Part A: Simplify the following Boolean expression using the Laws of Boolean algebra, and implement the resulting circuit using inverters, 2-input AND gates, and 2-input OR gates.

$$Z = \overline{Y}\,(\overline{W}\,U + W\overline{U}) + \overline{U}\,Y$$

Part B: Verify that the NOR operation is functionally complete using Laws of Boolean algebra. (Hint: Implement the functions NOT, AND, and OR only using 2-input NOR gates).

IMPORTANT: Lab grade will depend on the working of the circuit and will be checked off by the lab instructor.

References:

"Fundamentals of Logic Design", 7th Edition, by Charles H. Roth Jr. and Larry L Kinney, 2014, ISBN-13: 978-1133628477 or ISBN-10: 1133628478, CENGAGE Learning, Stamford, CT, USA

Notes:

1. You can use http://en.wikipedia.org/wiki/List of 7400 series integrated circuits to find the TTL chip you need.
2. Datasheets of some commonly used TTL chips can be found at the following sites:
    - http://www.jameco.com
    - http://www.ti.com/sc/docs/psheets/databook.htm
    - http://www.datasheetcatalog.com/fairchildsemiconductor/1/