NAME: ___Solutions_____ UNumber:_____ Computer Logic Design
Duration: 75 Minutes CDA 3201 November 3, 2016
Closed Book, Notes, HW Exam 2 R. Kasturi
Scientific calculator and one sheet of Letter size paper written on front and back are allowed.
SHOW ALL WORK TO GET PARTIAL CREDIT. MAKE REASONABLLE ASSUMPTIONS.

I (One point each) Answer True or False.

_F_ a. Every state of a Moore Finite State Machine must have direct arcs to every other state.

_T_ b. The output from a Mealy circuit must be read just prior to active clock edge to avoid reading *false outputs*.

_F_ c. A Mealy machine cannot have self-arcs (transitions originating and terminating in the same state).

_T_ d. A Read Only Memory (ROM) with n address lines and m bits per word can be designed to implement m different functions of n variables.

_F_ f. In a Programmable Array Logic (PAL), product terms can be shared among multiple OR gates.

_T_ e. In a Mealy machine the output responds to changes in the input without waiting for the registers to change state at the next clock pulse.

_F_ g. When the inputs J and K of a JK flip-flop are both equal to 1, its Q output holds its previous value.

_T_ h. Implementation of the function Z = (AB+C)(D+E+FG)+H exactly as expressed results in a 4 level function.

_F_ i. For proper operation, the D input of the flip flop must be stable for at least T_h (Hold time) time units *before* the clock edge.

_T_ j. Any Boolean function can be implemented using **only** OR gates and Inverters

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II (a) (5 points) Implement the function $f(A,B,C,D) = \sum m(0,3,5,7,11,12,13,15)$ using a 4:1 multiplexer with C and D as control inputs and one XNOR gate to form one of the inputs to the multiplexer.

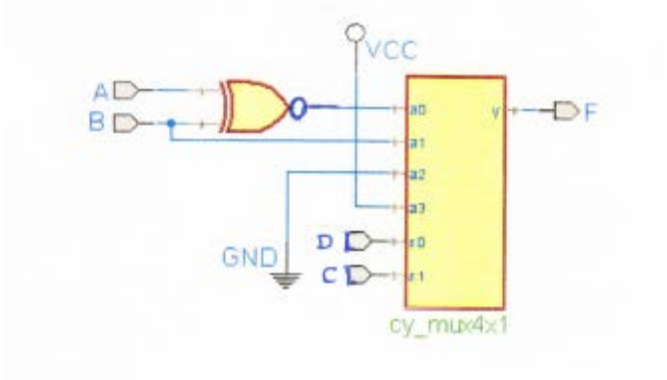
$$f(A,B,C,D) = \overline{A}\,\overline{B}\,\overline{C}\,\overline{D} + \overline{A}\,\overline{B}CD + \overline{A}B\overline{C}D + \overline{A}BCD + A\overline{B}CD + AB\overline{C}\,\overline{D} + AB\overline{C}D + ABCD$$

After simplification and rewriting to include all combinations of variables A,B, and C, we get

$$f(A,B,C,D) = \overline{A}\,\overline{B}\,\overline{C}\,\overline{D} + \overline{A}\,\overline{B}CD + \overline{A}B\overline{C}D + \overline{A}BCD + A\overline{B}\,\overline{C}\,.0 + A\overline{B}CD + AB\overline{C}\,.1 + ABCD$$

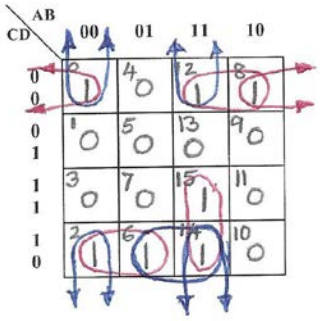
Now collect terms of variables C and D to get,

$$f(A,B,C,D) = \left(\overline{A}\,\overline{B} + AB\right).\overline{C}\,\overline{D} + (B).\overline{C}D + (0).C\overline{D} + 1.CD$$
$$= \overline{(A\,XOR\,B)}.\overline{C}\,\overline{D} + (B).\overline{C}D + (0).C\overline{D} + 1.CD$$



(b) (5 points) Find the **minimized sum of products form** of the function F (A, B, C, D) = $\prod M$ (1,3,4,5,7,9,10,11,13). Identify additional terms needed to make it a hazard free circuit.

CD \ AB	00	01	11	10
00	1	0	1	1
01	0	0	0	0
11	0	0	1	0
10	1	1	1	0



Original function groupings (shown in Red): B'C'D' + AC'D' + ABC + A'CD'
Additional terms added (shown in Blue): A'B'D' + BCD' +ABD'

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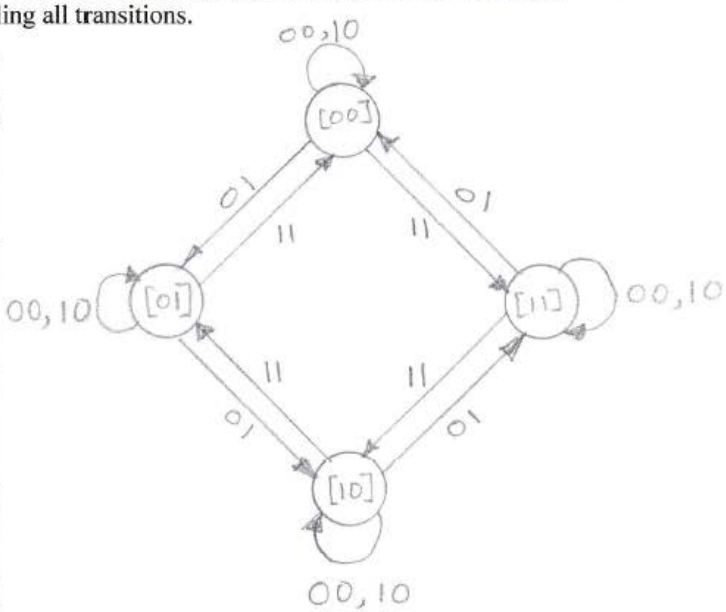
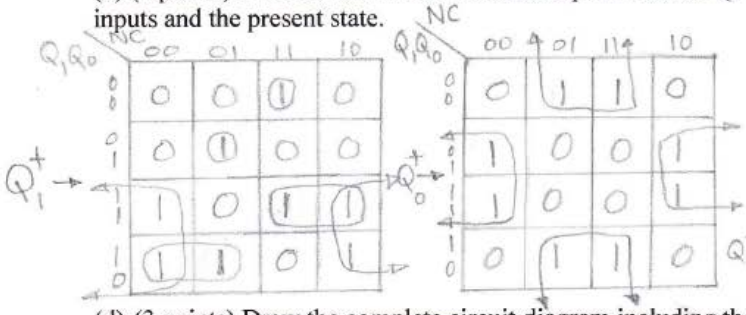
III (a) (3 points) A two-bit counter is controlled by two inputs, N and C. When C= 0, counting is disabled and the D flip-flops' state remain unchanged. When N= 0 and C = 1, the counter advances in the forward direction. When N=1 and C = 1, the counter advances in the reverse direction. The state transition table is shown below. Draw the Moore state diagram clearly labeling all transitions.

Inputs		Present		Next State	
N	C	Q1	Q0	Q1+	Q0+
0	0	0	0	0	0
		0	1	0	1
		1	0	1	0
		1	1	1	1
0	1	0	0	0	1
		0	1	1	0
		1	0	1	1
		1	1	0	0
1	0	0	0	0	0
		0	1	0	1
		1	0	1	0
		1	1	1	1
1	1	0	0	1	1
		0	1	0	0
		1	0	0	1
		1	1	1	0



(b) (4 points) Find the minimized Boolean expressions for Q1+ and Q0+ in terms of the inputs and the present state.



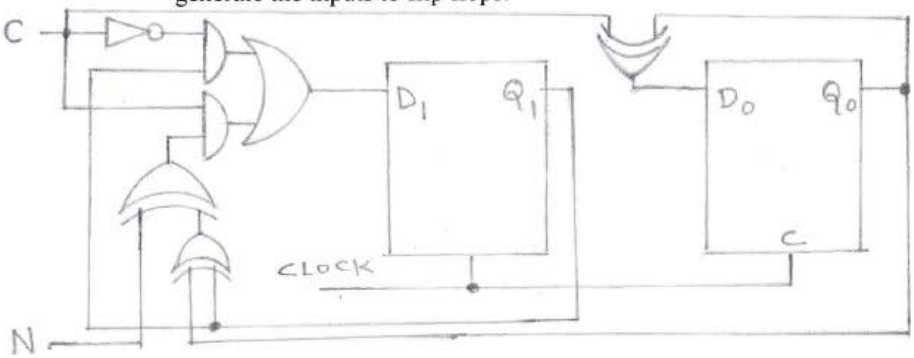
$Q_0^+ = C\bar{Q}_0 + \bar{C}Q_0 = C \oplus Q_0$

$Q_1^+ = \bar{C}Q_1 + NQ_1Q_0 + \bar{N}Q_1\bar{Q}_0 + NC\bar{Q}_1\bar{Q}_0 + \bar{N}C\bar{Q}_1Q_0$

This can also be written as

$Q_1^+ = \bar{C}Q_1 + C[Q_1 \oplus Q_0 \oplus N]$

(d) (3 points) Draw the complete circuit diagram including the combinational logic to generate the inputs to flip flops.



There are other Equivalent Comb logic diagrams

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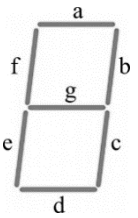
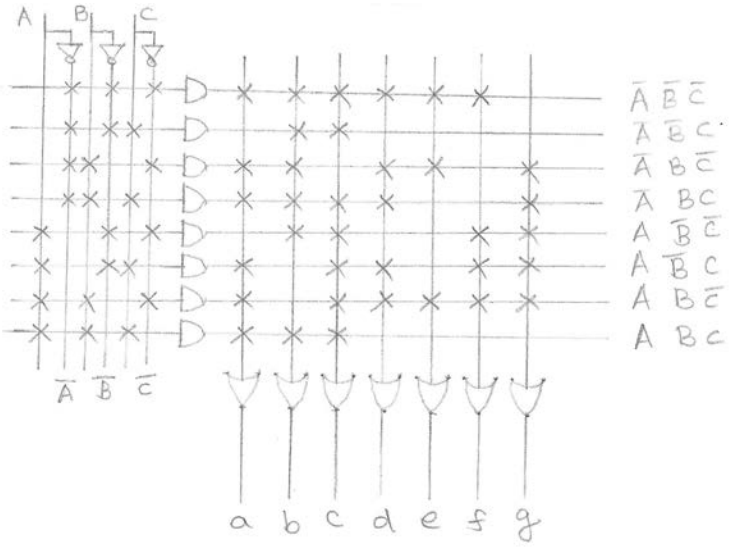
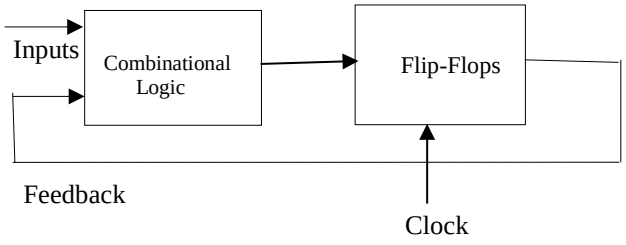
IV (a) (6 points) You have been chosen to lead the first group of settlers on a distant planet. You decide to seize this opportunity to discard the decimal system (with its many inefficiencies such as the BCD representation with unused bit combinations) and replace it with the more efficient octal system. Your first task is to design the logic circuit to display the 3 bit octal numbers from 0 to 7 on a seven segment display shown below (for number 1 use segments b and c; for 6 include segment a). Write the Truth Table with A, B, C representing the input bits (A is the MSB) and a,b,c,d,e,f and g representing the outputs to the seven segments. Implement the circuit using a Programmable Logic Array (use simplified notation to represent multiple inputs to AND and OR gates).

Number	A	B	C	a	b	c	d	e	f	g
0	0	0	0	1	1	1	1	1	1	0
1	0	0	1	0	1	1	0	0	0	0
2	0	1	0	1	1	0	1	1	0	1
3	0	1	1	1	1	1	1	0	0	1
4	1	0	0	0	1	1	0	0	1	1
5	1	0	1	1	0	1	1	0	1	1
6	1	1	0	1	0	1	1	1	1	1
7	1	1	1	1	1	1	0	0	0	0





(b) (4 points) Consider the following sequential logic circuit block diagram. Typical delay through the combinational logic circuit is 3 ns but the worst case delay is 5 ns. Setup times for flip flops is 2 ns, hold time is 1 ns, and the propagation delay through flip flops is 3 ns. Calculate the highest possible clock frequency for proper operation.



$T_{period} \geq Tcl - worst + Tpd + Tsu$
$\geq 5 + 3 + 2 = 10\ ns$
Frequency $= 1/Tperiod$ = 1/10x10^{-9}
= 100 MHz