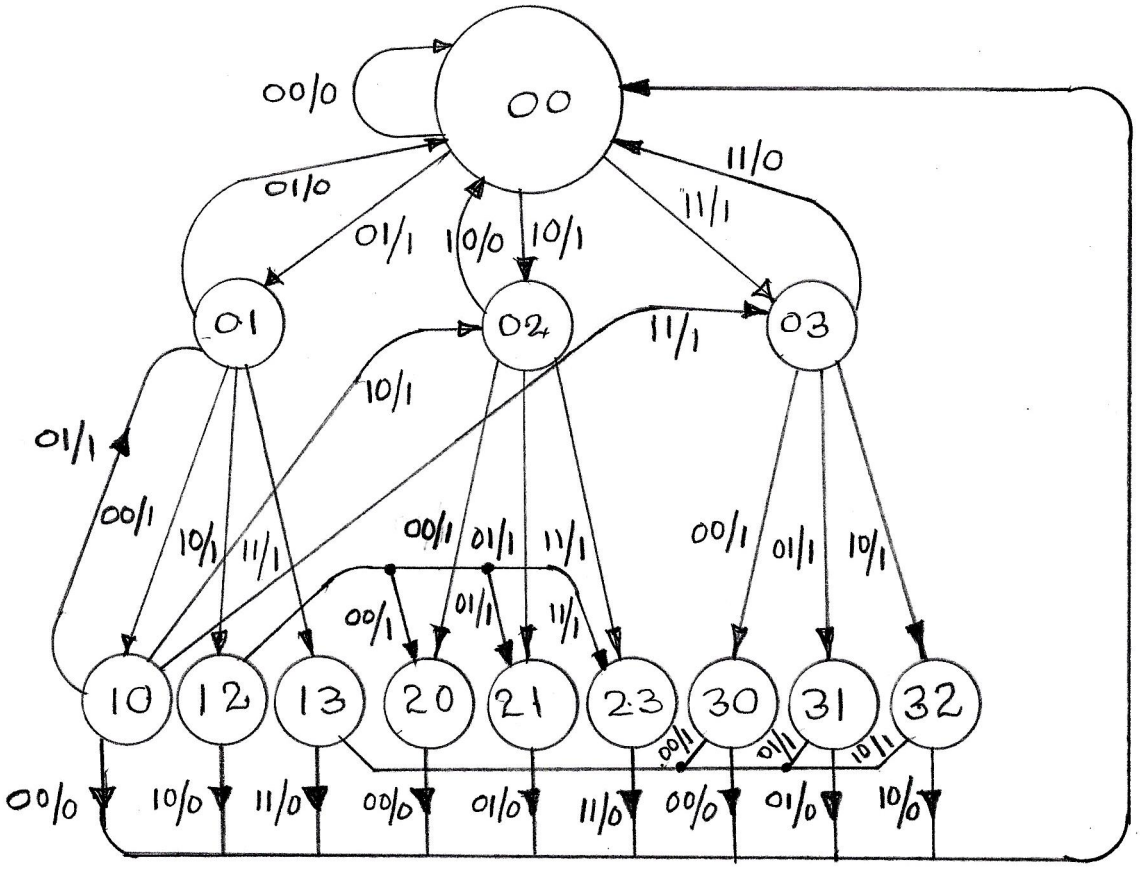
CDA 3201 Computer Logic Design Fall 2016
Solutions to Homework 5

Points: 100
Questions 1 to 5: 17 points each. Q6: 15 points

1. A Mealy Finite State Machine (FSM) has two binary inputs X1 and X2 and one output. The machine outputs a 0 and resets to 00 state whenever it receives two consecutive input strings that are identical (for example 01 followed by 01). In all other cases it outputs a 1. Use the following convention to label each state:

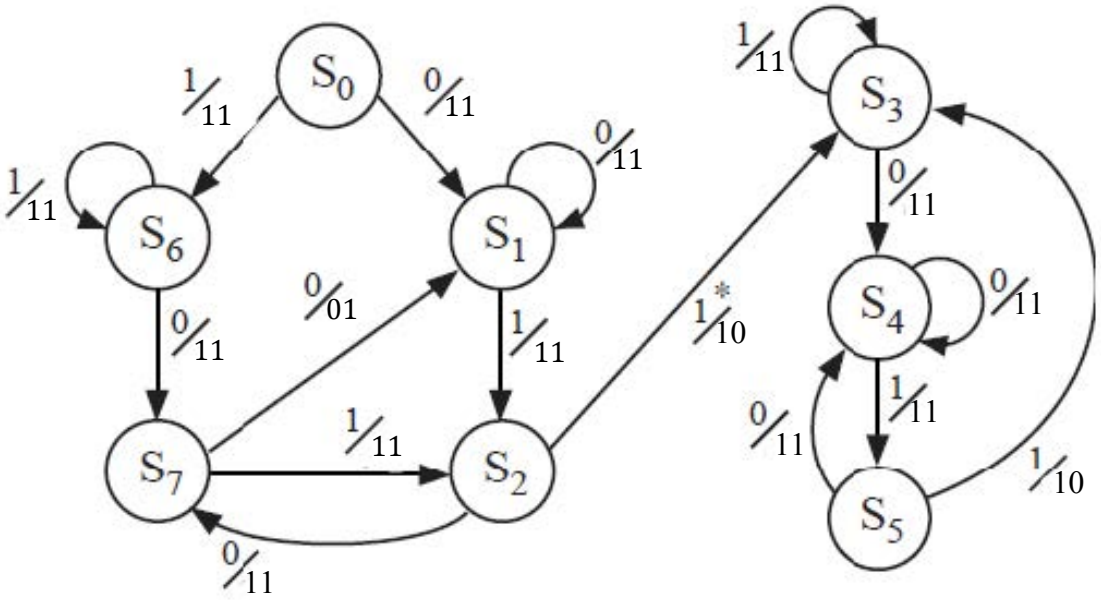
   Label the state as PQ if it is reached after receiving two input strings X1X2=P and X1X2=Q where P and Q are the decimal values of X1X2. Note that P and Q range from 0 to 3; for example, if the previous two inputs to a state are 01 and 11 it is labeled as 13. For states which are children of 00 (reset) use P=0 irrespective of how the 00 state is reached.

   Draw the FSM clearly labeling all inputs, outputs and state names but to decrease clutter **DO NOT draw any outgoing transitions from states 20,21,23,30,31,32**. Hint: the FSM has more than 10 states but its structure is simple and repetitive.



2. A sequential machine operates with an overlapping sliding window and has 1 input (X) and two outputs (Z1 and Z2) which have a default value of 1. An output Z1=0 occurs every time the input sequence 100 is completed provided that the sequence 011 has never occurred. An output Z2 = 0 occurs every time the input 011 has occurred. But once the sequence 011 has occurred, Z1 is permanently reset to 1 and will not change even if a sequence of 100 occurs. Draw the Mealy state graph with no more than 8 states and the corresponding state table.

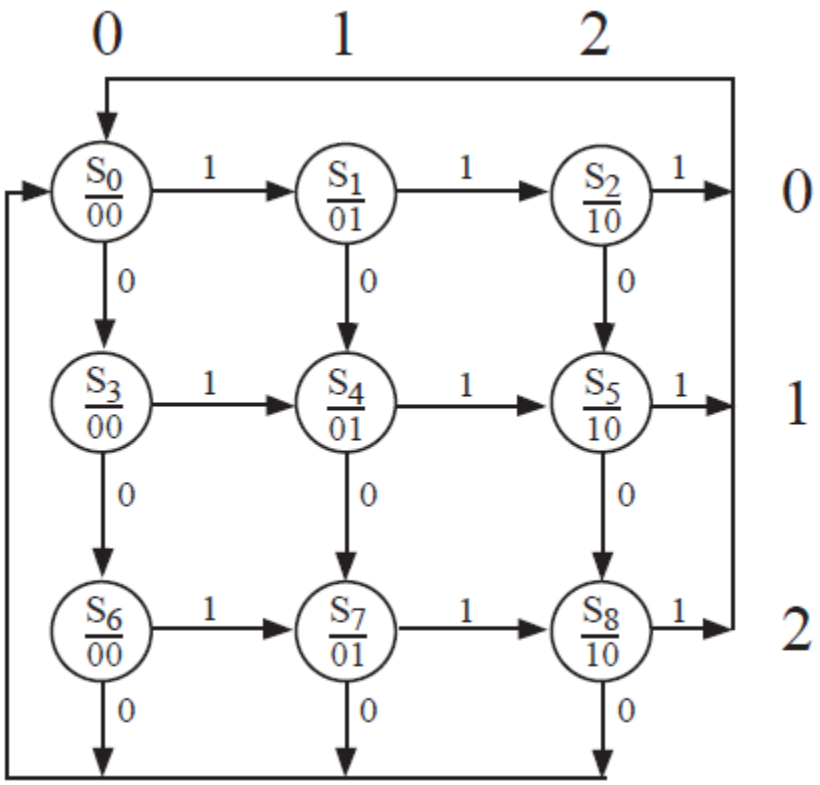
   Example input: 100110011. Corresponding Z1 output: 110111111; Z2 output: 111101110.



- When this point is reached in the graph, 011 has been received and we are only looking for 011 to occur again.

State	Meaning	Next State		Z_1Z_2	
		X=0	X=1	X=0	X=1
S0	Reset	S1	S6	11	11
S1	Prev input was 0/011 has not occurred	S1	S2	11	11
S2	Prev input was 01/011 has not occurred	S7	S3	11	10
S3	No sequence / 011 has occurred	S4	S3	11	11
S4	Prev input was 0/011 has occurred	S4	S5	11	11
S5	Prev input was 01/011 has occurred	S4	S3	11	10
S6	Prev input was 1/011 has not occurred	S7	S6	11	11
S7	Prev input was 10/011 has not occurred	S1	S2	01	11

3. A Moore machine has an input (X) and outputs (Y and Z). YZ represents a 2 bit binary number equal to the number of 1's that have been received as inputs. The circuit resets when the total number of 1's received is 3 or when the total number of 0's received is 3. Draw the state graph and state transition table for the machine.



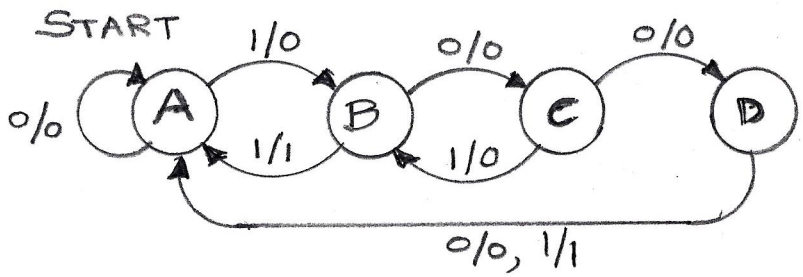
** Horizontally: Number of 1's modulo
3. ** Vertically: Number of 0's modulo 3.

State	Next State		YZ
	X=0	X=1	
S0	S3	S1	00
S1	S4	S2	01
S2	S5	S0	10
S3	S6	S4	00
S4	S7	S5	01
S5	S8	S0	10
S6	S0	S7	00
S7	S0	S8	01
S8	S0	S0	10

4. A FSM receives one bit of data at each clock cycle and outputs a 1 when the sequence 11 or 1001 is received. It resets to start state after detecting either one of these two sequences.

i) Draw the Mealy state diagram

ii) Implement the FSM using D flip flops by deriving the minimized next state and output logic functions.



Present State/D1D0	Next State/Output		D1+D0+	
	X=0	X=1	X=0	X=1
A/00	A/0	B/0	00	01
B /01	C/0	A/1	11	00
C/11	D/0	B/0	10	01
D/10	A/0	A/1	00	00

From the State Transition Table above, we can determine the logic functions for Next State, D1+ and D0+ shown below:

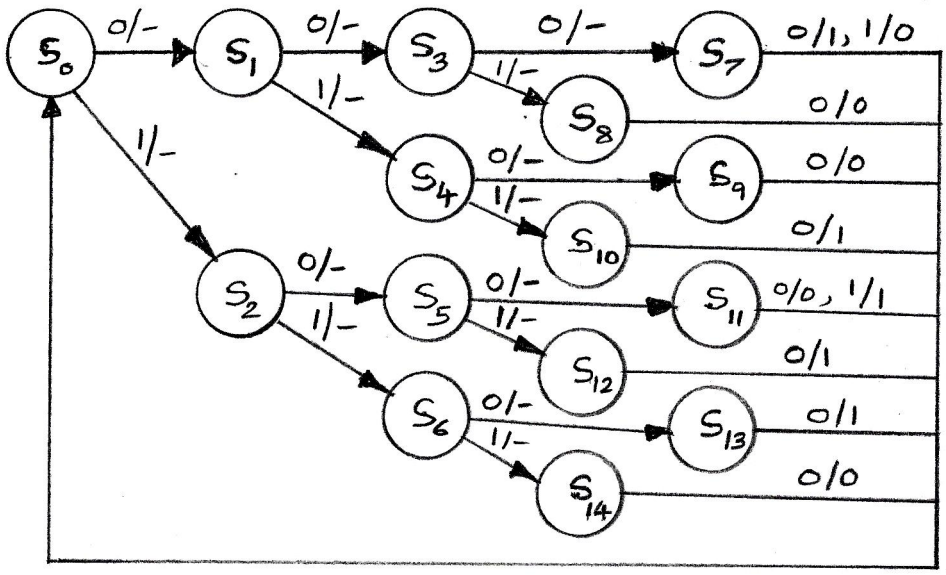
D1+ = D0 X'

D0+ = D1' D0' X + D1' D0 X' + D1 D0 X

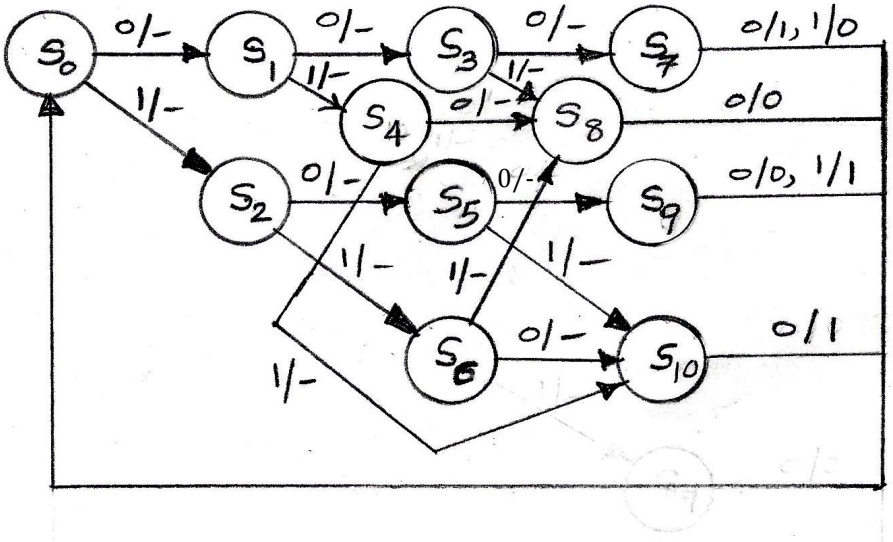
Z = D1' D0 X + D1 D0' X

5. The decimal digits 0 through 9 are encoded as 4-bit binary numbers. They are transmitted in disjoint windows of length 4 with the least significant bit first and are input to a Mealy circuit. The circuit generates an output of 1 (0) when the fourth bit is received if the 4 bits have been even (odd) parity; the circuit output is a Don't-Care for the first 3 bits. Construct an incompletely specified table for the circuit.

   A simpler implementation shown below requires branching to two separate states after each bit is received except for the last bit (MSB).



   This requires 15 states. However a more compact representation is possible by observing that we only need to keep track of the parity (except we must not include paths for bit strings which do not occur in a BCD string) as shown below.



6. Design the state diagram for the control unit of a coin-operated Coke machine. Coke costs 125 cents and the machine accepts quarters and dollars. Change should be returned if more than 125 cents is deposited. Assume that the machine dispenses the product and change, if any, and resets once at least 125 cents are deposited.