Excersises for Lecture 2

Exercise 1: Truth table and n,p-transistors

3.1

	N-type	P-type
Gate = 1	1	0
Gate = 0	0	1

3.2

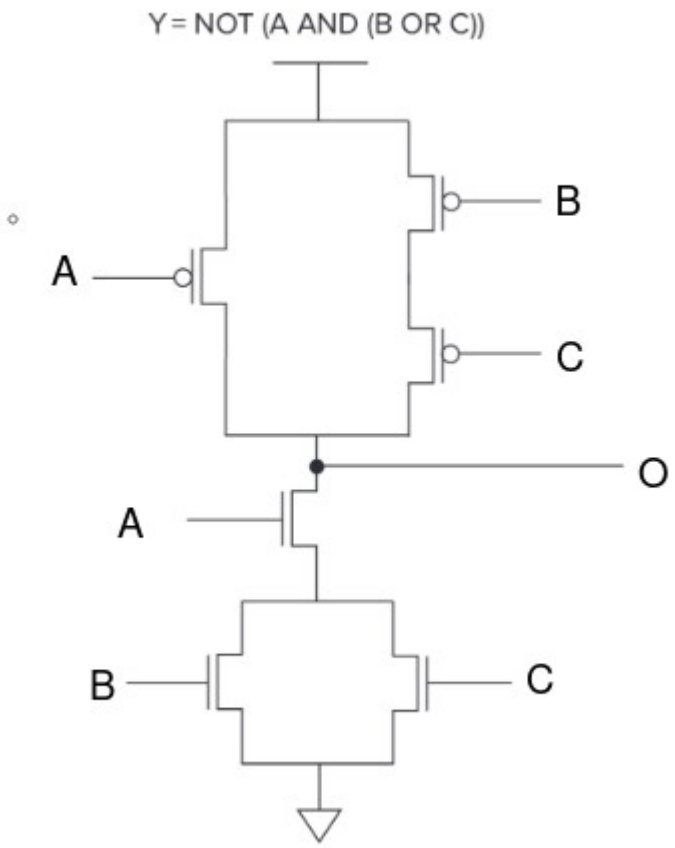
From top to bottom: P-type, N-type

3.5 (NOT(A) or NOT(B)) AND NOT(C)

A	B	C	Out
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

Exercise 2: Deeper understanding of transistors to gates

3.8 not A or not(B and C) = not A or (not B and not C)



3.10

Only when:

A = B = F = 0

C = D = E = 1

Exercise 3: Understanding of gates

3.13

The 4 left most bits is 0, and either (the bite 5ᵗʰth from right and N) or (6th and Z) or (7th and P) are 1.

so in more english = the 7 bite number is less than 8 (unsigned binary).

3.14

A	B	C	Out
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

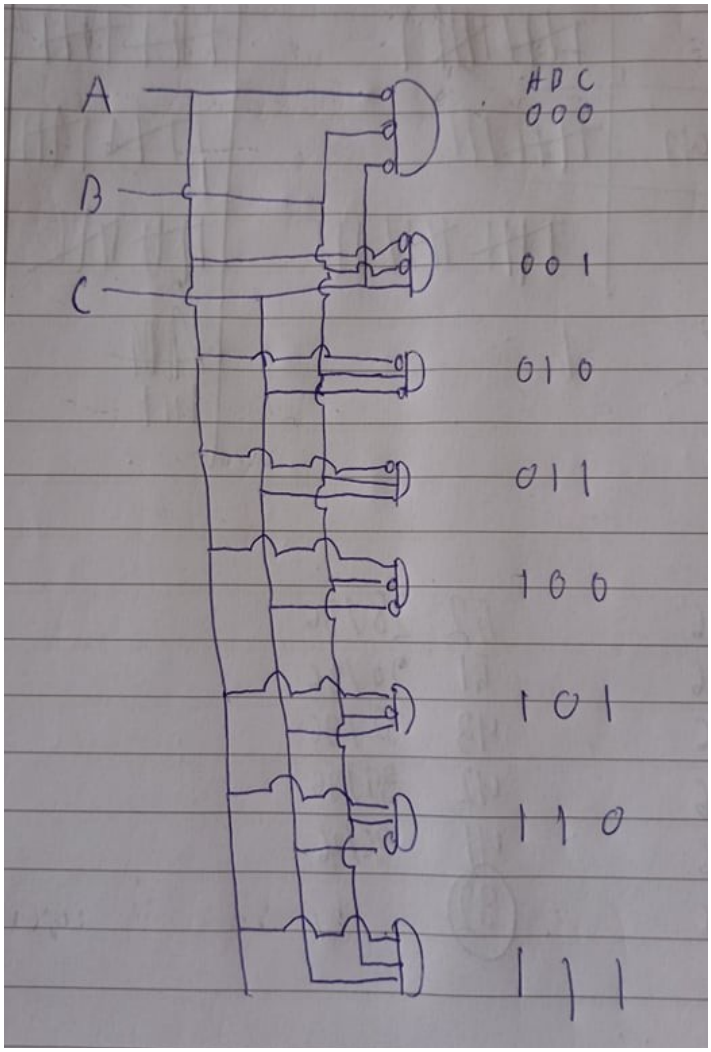
3.15

The AND gate

A	B	Out
0	0	0
0	1	0
1	0	0
1	1	1

Exercise 4: Complex gate systems

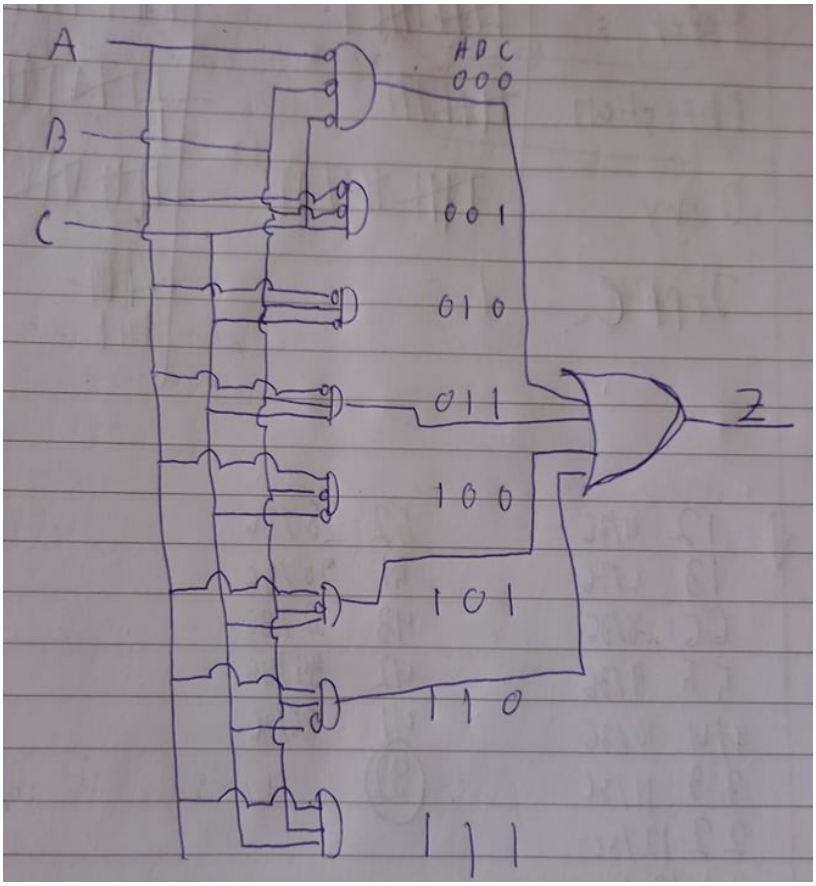
3.18



3.19

2^5 = 32

3.22



Exercise 5:

3.30.A

It selects which bitstring of B or C to use in the adder.

3.37

(2^3 – 1) * 64 bits = 384 bits = 48 bytes

3.38

addressability = number of bits of information stored in each location

memory address = the unique identifier for a memory location.