



PSoC® Creator™

Project Datasheet for userKitCtrlApp

Creation Time: 05/20/2019 10:17:44

User: DESKTOP-8VRB4J6\fresi

Project: userKitCtrlApp

Tool: PSoC Creator 4.2

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1 Overview

The Cypress PSoC 5 is a family of 32-bit devices with the following characteristics:

- High-performance 32-bit ARM Cortex-M3 core with a nested vectored interrupt controller (NVIC) and a high-performance DMA controller
- Digital system that includes configurable Universal Digital Blocks (UDBs) and specific function peripherals, such as USB, I2C and SPI
- Analog subsystem that includes 20-bit Delta Sigma converters (ADC), SAR ADCs, 8-bit DACs that can be configured for 12-bit operation, comparators, op amps and configurable switched capacitor (SC) and continuous time (CT) blocks to create PGAs, TIAs, mixers, and more
- Several types of memory elements, including SRAM, flash, and EEPROM
- Programming and debug system through JTAG, serial wire debug (SWD), and single wire viewer (SWV)
- Flexible routing to all pins

Figure 1 shows the major components of a typical [CY8C58LP](#) series member PSoC 5LP device. For details on all the systems listed above, please refer to the [PSoC 5LP Technical Reference Manual](#).

Figure 1. CY8C58LP Device Series Block Diagram



Table 1 lists the key characteristics of this device.

Table 1. Device Characteristics

| Name | Value |
|----------------------|----------------------------|
| Part Number | CY8C5888LTI-LP097 |
| Package Name | 68-QFN |
| Family | PSoC 5LP |
| Series | CY8C58LP |
| Max CPU speed (MHz) | 0 |
| Flash size (kB) | 256 |
| SRAM size (kB) | 64 |
| EEPROM size (bytes) | 2048 |
| Vdd range (V) | 1.71 to 5.5 |
| Automotive qualified | No (Industrial Grade Only) |
| Temp range (Celsius) | -40 to 85 |
| JTAG ID | 0x2E161069 |

NOTE: The CPU speed noted above is the maximum available speed. The CPU is clocked by Bus Clock, listed in the [System Clocks](#) section below.

Table 2 lists the device resources that this design uses:

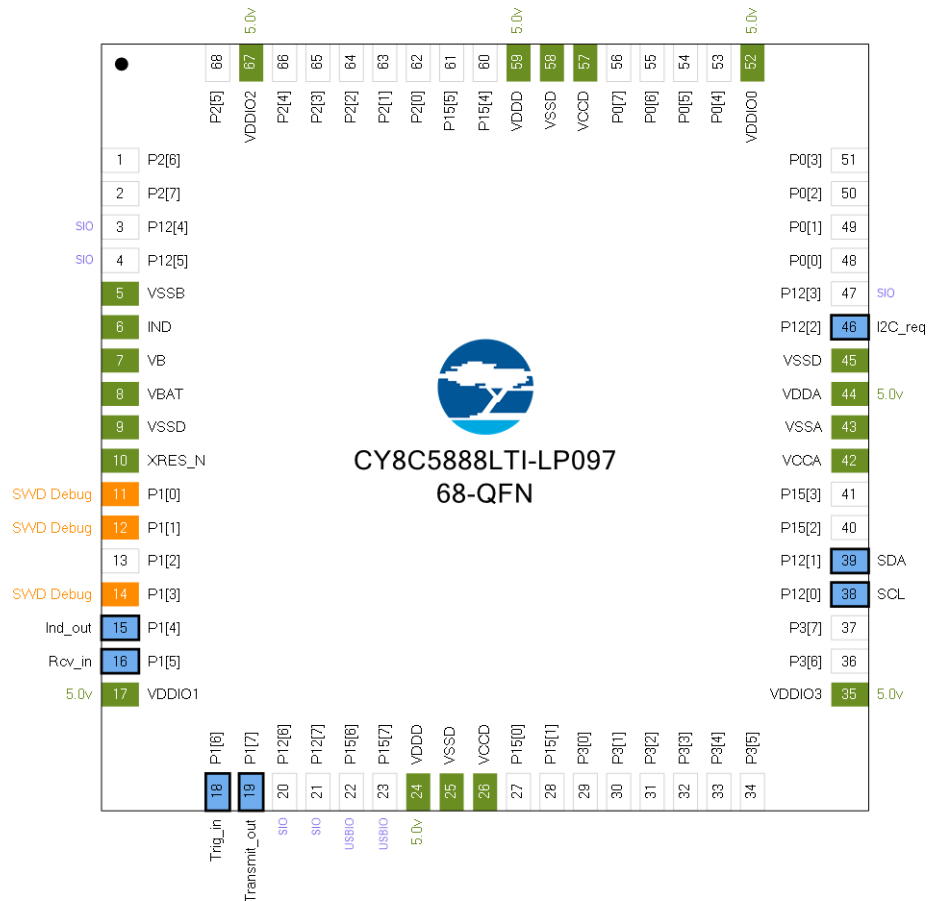
Table 2. Device Resources

| Resource Type | Used | Free | Max | % Used |
|-----------------------|------|------|-----|----------|
| Digital Clocks | 5 | 3 | 8 | 62.50 % |
| Analog Clocks | 2 | 2 | 4 | 50.00 % |
| CapSense Buffers | 0 | 2 | 2 | 0.00 % |
| Digital Filter Block | 1 | 0 | 1 | 100.00 % |
| Interrupts | 6 | 26 | 32 | 18.75 % |
| IO | 10 | 38 | 48 | 20.83 % |
| Segment LCD | 0 | 1 | 1 | 0.00 % |
| CAN 2.0b | 0 | 1 | 1 | 0.00 % |
| I2C | 1 | 0 | 1 | 100.00 % |
| USB | 0 | 1 | 1 | 0.00 % |
| DMA Channels | 2 | 22 | 24 | 8.33 % |
| Timer | 1 | 3 | 4 | 25.00 % |
| UDB | | | | |
| Macrocells | 3 | 189 | 192 | 1.56 % |
| Unique P-terms | 2 | 382 | 384 | 0.52 % |
| Total P-terms | 2 | | | |
| Datapath Cells | 1 | 23 | 24 | 4.17 % |
| Status Cells | 0 | 24 | 24 | 0.00 % |
| Control Cells | 1 | 23 | 24 | 4.17 % |
| Control Registers | 1 | | | |
| Opamp | 0 | 4 | 4 | 0.00 % |
| Comparator | 0 | 4 | 4 | 0.00 % |
| Delta-Sigma ADC | 1 | 0 | 1 | 100.00 % |
| LPF | 0 | 2 | 2 | 0.00 % |
| SAR ADC | 0 | 2 | 2 | 0.00 % |
| Analog (SC/CT) Blocks | 2 | 2 | 4 | 50.00 % |
| DAC | | | | |
| VIDAC | 0 | 4 | 4 | 0.00 % |

2 Pins

Figure 2 shows the pin layout of this device.

Figure 2. Device Pin Layout



2.1 Hardware Pins

Table 3 contains information about the pins on this device in device pin order. (No connection ["n/c"] pins have been omitted.)

Table 3. Device Pins

| Pin | Port | Name | Type | Drive Mode | Reset State |
|-----|--------|-----------------|-----------|---------------|----------------|
| 1 | P2[6] | GPIO [unused] | | | HiZ Analog Unb |
| 2 | P2[7] | GPIO [unused] | | | HiZ Analog Unb |
| 3 | P12[4] | SIO [unused] | | | HiZ Analog Unb |
| 4 | P12[5] | SIO [unused] | | | HiZ Analog Unb |
| 5 | VSSB | VSSB | Dedicated | | |
| 6 | IND | IND | Dedicated | | |
| 7 | VB | VB | Dedicated | | |
| 8 | VBAT | VBAT | Dedicated | | |
| 9 | VSSD | VSSD | Power | | |
| 10 | XRES_N | XRES_N | Dedicated | | |
| 11 | P1[0] | Debug:SWD_IO | Reserved | | |
| 12 | P1[1] | Debug:SWD_CK | Reserved | | |
| 13 | P1[2] | GPIO [unused] | | | HiZ Analog Unb |
| 14 | P1[3] | Debug:SWV | Reserved | | |
| 15 | P1[4] | Ind_out | Dgtl Out | Strong drive | HiZ Analog Unb |
| 16 | P1[5] | Rcv_in | Analog | HiZ analog | HiZ Analog Unb |
| 17 | VDDIO1 | VDDIO1 | Power | | |
| 18 | P1[6] | Trig_in | Dgtl In | Res pull down | HiZ Analog Unb |
| 19 | P1[7] | Transmit_out | Dgtl Out | Strong drive | HiZ Analog Unb |
| 20 | P12[6] | SIO [unused] | | | HiZ Analog Unb |
| 21 | P12[7] | SIO [unused] | | | HiZ Analog Unb |
| 22 | P15[6] | USB IO [unused] | | | HiZ Analog Unb |
| 23 | P15[7] | USB IO [unused] | | | HiZ Analog Unb |
| 24 | VDDD | VDDD | Power | | |
| 25 | VSSD | VSSD | Power | | |
| 26 | VCCD | VCCD | Power | | |
| 27 | P15[0] | GPIO [unused] | | | HiZ Analog Unb |
| 28 | P15[1] | GPIO [unused] | | | HiZ Analog Unb |
| 29 | P3[0] | GPIO [unused] | | | HiZ Analog Unb |
| 30 | P3[1] | GPIO [unused] | | | HiZ Analog Unb |
| 31 | P3[2] | GPIO [unused] | | | HiZ Analog Unb |
| 32 | P3[3] | GPIO [unused] | | | HiZ Analog Unb |
| 33 | P3[4] | GPIO [unused] | | | HiZ Analog Unb |
| 34 | P3[5] | GPIO [unused] | | | HiZ Analog Unb |
| 35 | VDDIO3 | VDDIO3 | Power | | |
| 36 | P3[6] | GPIO [unused] | | | HiZ Analog Unb |
| 37 | P3[7] | GPIO [unused] | | | HiZ Analog Unb |
| 38 | P12[0] | SCL | Dgtl I/O | OD, DL | HiZ Analog Unb |
| 39 | P12[1] | SDA | Dgtl I/O | OD, DL | HiZ Analog Unb |
| 40 | P15[2] | GPIO [unused] | | | HiZ Analog Unb |
| 41 | P15[3] | GPIO [unused] | | | HiZ Analog Unb |
| 42 | VCCA | VCCA | Power | | |
| 43 | VSSA | VSSA | Power | | |
| 44 | VDDA | VDDA | Power | | |
| 45 | VSSD | VSSD | Power | | |

| Pin | Port | Name | Type | Drive Mode | Reset State |
|-----|--------|---------------|-----------------|------------|----------------|
| 46 | P12[2] | I2C_req | Software In/Out | OD, DL | HiZ Analog Unb |
| 47 | P12[3] | SIO [unused] | | | HiZ Analog Unb |
| 48 | P0[0] | GPIO [unused] | | | HiZ Analog Unb |
| 49 | P0[1] | GPIO [unused] | | | HiZ Analog Unb |
| 50 | P0[2] | GPIO [unused] | | | HiZ Analog Unb |
| 51 | P0[3] | GPIO [unused] | | | HiZ Analog Unb |
| 52 | VDDIO0 | VDDIO0 | Power | | |
| 53 | P0[4] | GPIO [unused] | | | HiZ Analog Unb |
| 54 | P0[5] | GPIO [unused] | | | HiZ Analog Unb |
| 55 | P0[6] | GPIO [unused] | | | HiZ Analog Unb |
| 56 | P0[7] | GPIO [unused] | | | HiZ Analog Unb |
| 57 | VCCD | VCCD | Power | | |
| 58 | VSSD | VSSD | Power | | |
| 59 | VDDD | VDDD | Power | | |
| 60 | P15[4] | GPIO [unused] | | | HiZ Analog Unb |
| 61 | P15[5] | GPIO [unused] | | | HiZ Analog Unb |
| 62 | P2[0] | GPIO [unused] | | | HiZ Analog Unb |
| 63 | P2[1] | GPIO [unused] | | | HiZ Analog Unb |
| 64 | P2[2] | GPIO [unused] | | | HiZ Analog Unb |
| 65 | P2[3] | GPIO [unused] | | | HiZ Analog Unb |
| 66 | P2[4] | GPIO [unused] | | | HiZ Analog Unb |
| 67 | VDDIO2 | VDDIO2 | Power | | |
| 68 | P2[5] | GPIO [unused] | | | HiZ Analog Unb |

Abbreviations used in Table 3 have the following meanings:

- HiZ Analog Unb = Hi-Z Analog Unbuffered
- Dgtl Out = Digital Output
- HiZ analog = High impedance analog
- Dgtl In = Digital Input
- Res pull down = Resistive pull down
- Dgtl I/O = Digital In/Out
- OD, DL = Open drain, drives low

2.2 Hardware Ports

Table 4 contains information about the pins on this device in device port order. (No connection ["n/c"], power and dedicated pins have been omitted.)

Table 4. Device Ports

| Port | Pin | Name | Type | Drive Mode | Reset State |
|--------|-----|-----------------|-----------------|---------------|----------------|
| P0[0] | 48 | GPIO [unused] | | | HiZ Analog Unb |
| P0[1] | 49 | GPIO [unused] | | | HiZ Analog Unb |
| P0[2] | 50 | GPIO [unused] | | | HiZ Analog Unb |
| P0[3] | 51 | GPIO [unused] | | | HiZ Analog Unb |
| P0[4] | 53 | GPIO [unused] | | | HiZ Analog Unb |
| P0[5] | 54 | GPIO [unused] | | | HiZ Analog Unb |
| P0[6] | 55 | GPIO [unused] | | | HiZ Analog Unb |
| P0[7] | 56 | GPIO [unused] | | | HiZ Analog Unb |
| P1[0] | 11 | Debug:SWD_IO | Reserved | | |
| P1[1] | 12 | Debug:SWD_CK | Reserved | | |
| P1[2] | 13 | GPIO [unused] | | | HiZ Analog Unb |
| P1[3] | 14 | Debug:SWV | Reserved | | |
| P1[4] | 15 | Ind_out | Dgtl Out | Strong drive | HiZ Analog Unb |
| P1[5] | 16 | Rcv_in | Analog | HiZ analog | HiZ Analog Unb |
| P1[6] | 18 | Trig_in | Dgtl In | Res pull down | HiZ Analog Unb |
| P1[7] | 19 | Transmit_out | Dgtl Out | Strong drive | HiZ Analog Unb |
| P12[0] | 38 | SCL | Dgtl I/O | OD, DL | HiZ Analog Unb |
| P12[1] | 39 | SDA | Dgtl I/O | OD, DL | HiZ Analog Unb |
| P12[2] | 46 | I2C_req | Software In/Out | OD, DL | HiZ Analog Unb |
| P12[3] | 47 | SIO [unused] | | | HiZ Analog Unb |
| P12[4] | 3 | SIO [unused] | | | HiZ Analog Unb |
| P12[5] | 4 | SIO [unused] | | | HiZ Analog Unb |
| P12[6] | 20 | SIO [unused] | | | HiZ Analog Unb |
| P12[7] | 21 | SIO [unused] | | | HiZ Analog Unb |
| P15[0] | 27 | GPIO [unused] | | | HiZ Analog Unb |
| P15[1] | 28 | GPIO [unused] | | | HiZ Analog Unb |
| P15[2] | 40 | GPIO [unused] | | | HiZ Analog Unb |
| P15[3] | 41 | GPIO [unused] | | | HiZ Analog Unb |
| P15[4] | 60 | GPIO [unused] | | | HiZ Analog Unb |
| P15[5] | 61 | GPIO [unused] | | | HiZ Analog Unb |
| P15[6] | 22 | USB IO [unused] | | | HiZ Analog Unb |
| P15[7] | 23 | USB IO [unused] | | | HiZ Analog Unb |
| P2[0] | 62 | GPIO [unused] | | | HiZ Analog Unb |
| P2[1] | 63 | GPIO [unused] | | | HiZ Analog Unb |
| P2[2] | 64 | GPIO [unused] | | | HiZ Analog Unb |
| P2[3] | 65 | GPIO [unused] | | | HiZ Analog Unb |
| P2[4] | 66 | GPIO [unused] | | | HiZ Analog Unb |
| P2[5] | 68 | GPIO [unused] | | | HiZ Analog Unb |
| P2[6] | 1 | GPIO [unused] | | | HiZ Analog Unb |
| P2[7] | 2 | GPIO [unused] | | | HiZ Analog Unb |
| P3[0] | 29 | GPIO [unused] | | | HiZ Analog Unb |
| P3[1] | 30 | GPIO [unused] | | | HiZ Analog Unb |
| P3[2] | 31 | GPIO [unused] | | | HiZ Analog Unb |
| P3[3] | 32 | GPIO [unused] | | | HiZ Analog Unb |

| Port | Pin | Name | Type | Drive Mode | Reset State |
|-------|-----|---------------|------|------------|----------------|
| P3[4] | 33 | GPIO [unused] | | | HiZ Analog Unb |
| P3[5] | 34 | GPIO [unused] | | | HiZ Analog Unb |
| P3[6] | 36 | GPIO [unused] | | | HiZ Analog Unb |
| P3[7] | 37 | GPIO [unused] | | | HiZ Analog Unb |

Abbreviations used in Table 4 have the following meanings:

- HiZ Analog Unb = Hi-Z Analog Unbuffered
- Dgtl Out = Digital Output
- HiZ analog = High impedance analog
- Dgtl In = Digital Input
- Res pull down = Resistive pull down
- Dgtl I/O = Digital In/Out
- OD, DL = Open drain, drives low

2.3 Software Pins

Table 5 contains information about the software pins on this device in alphabetical order. (Only software-accessible pins are shown.)

Table 5. Software Pins

| Name | Port | Type | Reset State |
|---------------|--------|-----------------|----------------|
| Debug:SWD_CK | P1[1] | Reserved | |
| Debug:SWD_IO | P1[0] | Reserved | |
| Debug:SWV | P1[3] | Reserved | |
| GPIO [unused] | P0[2] | | HiZ Analog Unb |
| GPIO [unused] | P0[3] | | HiZ Analog Unb |
| GPIO [unused] | P0[1] | | HiZ Analog Unb |
| GPIO [unused] | P0[0] | | HiZ Analog Unb |
| GPIO [unused] | P15[3] | | HiZ Analog Unb |
| GPIO [unused] | P3[6] | | HiZ Analog Unb |
| GPIO [unused] | P3[5] | | HiZ Analog Unb |
| GPIO [unused] | P3[4] | | HiZ Analog Unb |
| GPIO [unused] | P15[2] | | HiZ Analog Unb |
| GPIO [unused] | P3[3] | | HiZ Analog Unb |
| GPIO [unused] | P3[7] | | HiZ Analog Unb |
| GPIO [unused] | P0[4] | | HiZ Analog Unb |
| GPIO [unused] | P2[2] | | HiZ Analog Unb |
| GPIO [unused] | P2[1] | | HiZ Analog Unb |
| GPIO [unused] | P2[3] | | HiZ Analog Unb |
| GPIO [unused] | P2[5] | | HiZ Analog Unb |
| GPIO [unused] | P2[4] | | HiZ Analog Unb |
| GPIO [unused] | P2[0] | | HiZ Analog Unb |
| GPIO [unused] | P0[6] | | HiZ Analog Unb |
| GPIO [unused] | P0[5] | | HiZ Analog Unb |
| GPIO [unused] | P0[7] | | HiZ Analog Unb |
| GPIO [unused] | P15[5] | | HiZ Analog Unb |
| GPIO [unused] | P15[4] | | HiZ Analog Unb |
| GPIO [unused] | P2[6] | | HiZ Analog Unb |
| GPIO [unused] | P15[0] | | HiZ Analog Unb |
| GPIO [unused] | P2[7] | | HiZ Analog Unb |
| GPIO [unused] | P1[2] | | HiZ Analog Unb |
| GPIO [unused] | P15[1] | | HiZ Analog Unb |
| GPIO [unused] | P3[1] | | HiZ Analog Unb |
| GPIO [unused] | P3[2] | | HiZ Analog Unb |
| GPIO [unused] | P3[0] | | HiZ Analog Unb |
| I2C_req | P12[2] | Software In/Out | HiZ Analog Unb |
| Ind_out | P1[4] | Dgtl Out | HiZ Analog Unb |
| Rcv_in | P1[5] | Analog | HiZ Analog Unb |
| SCL | P12[0] | Dgtl I/O | HiZ Analog Unb |
| SDA | P12[1] | Dgtl I/O | HiZ Analog Unb |
| SIO [unused] | P12[4] | | HiZ Analog Unb |
| SIO [unused] | P12[5] | | HiZ Analog Unb |
| SIO [unused] | P12[6] | | HiZ Analog Unb |
| SIO [unused] | P12[7] | | HiZ Analog Unb |
| SIO [unused] | P12[3] | | HiZ Analog Unb |
| Transmit_out | P1[7] | Dgtl Out | HiZ Analog Unb |

| Name | Port | Type | Reset State |
|-----------------|--------|---------|----------------|
| Trig_in | P1[6] | Dgtl In | HiZ Analog Unb |
| USB IO [unused] | P15[6] | | HiZ Analog Unb |
| USB IO [unused] | P15[7] | | HiZ Analog Unb |

Abbreviations used in Table 5 have the following meanings:

- HiZ Analog Unb = Hi-Z Analog Unbuffered
- Dgtl Out = Digital Output
- Dgtl I/O = Digital In/Out
- Dgtl In = Digital Input

For more information on reading, writing and configuring pins, please refer to:

- Pins chapter in the [System Reference Guide](#)
 - CyPins API routines
- Programming Application Interface section in the [cy_pins component datasheet](#)

3 System Settings

3.1 System Configuration

Table 6. System Configuration Settings

| Name | Value |
|---|----------------|
| Device Configuration Mode | Compressed |
| Enable Error Correcting Code (ECC) | False |
| Store Configuration Data in ECC Memory | True |
| Instruction Cache Enabled | True |
| Enable Fast IMO During Startup | True |
| Unused Bonded IO | Allow but warn |
| Heap Size (bytes) | 0x80 |
| Stack Size (bytes) | 0x0800 |
| Include CMSIS Core Peripheral Library Files | True |

3.2 System Debug Settings

Table 7. System Debug Settings

| Name | Value |
|--------------------------|--|
| Debug Select | SWD+SWV (serial wire debug and viewer) |
| Enable Device Protection | False |
| Embedded Trace (ETM) | False |
| Use Optional XRES | False |

3.3 System Operating Conditions

Table 8. System Operating Conditions

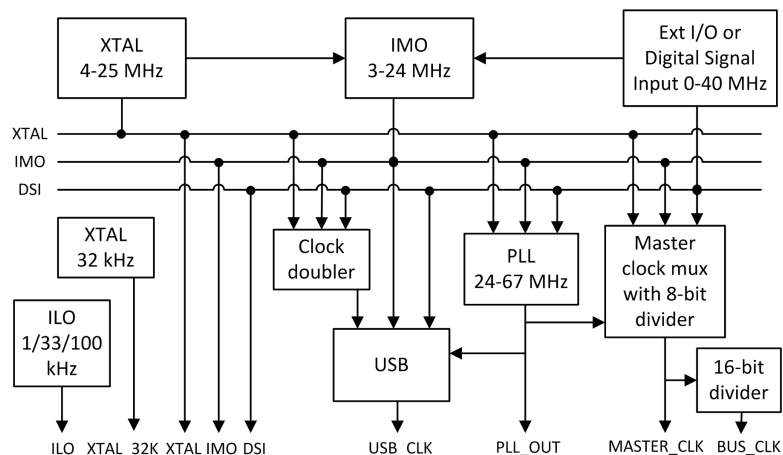
| Name | Value |
|-------------------|----------------|
| VDDA (V) | 5.0 |
| VDDD (V) | 5.0 |
| VDDIO0 (V) | 5.0 |
| VDDIO1 (V) | 5.0 |
| VDDIO2 (V) | 5.0 |
| VDDIO3 (V) | 5.0 |
| Variable VDDA | False |
| Temperature Range | -40C - 85/125C |

4 Clocks

The clock system includes these clock resources:

- Four internal clock sources increase system integration:
 - 3 to 74.7 MHz Internal Main Oscillator (IMO) $\pm 1\%$ at 3 MHz
 - 1 kHz, 33 kHz, and 100 kHz Internal Low Speed Oscillator (ILO) outputs
 - 12 to 80 MHz clock doubler output, sourced from IMO, MHz External Crystal Oscillator (MHzECO), and Digital System Interconnect (DSI)
 - 24 to 80 MHz fractional Phase-Locked Loop (PLL) sourced from IMO, MHzECO, and DSI
- Clock generated using a DSI signal from an external I/O pin or other logic
- Two external clock sources provide high precision clocks:
 - 4 to 25 MHz External Crystal Oscillator (MHzECO)
 - 32.768 kHz External Crystal Oscillator (kHzECO) for Real Time Clock (RTC)
- Dedicated 16-bit divider for bus clock
- Eight individually sourced 16-bit clock dividers for the digital system peripherals
- Four individually sourced 16-bit clock dividers with skew for the analog system peripherals
- IMO has a USB mode that synchronizes to USB host traffic, requiring no external crystal for USB. (USB equipped parts only)

Figure 3. System Clock Configuration



4.1 System Clocks

Table 9 lists the system clocks used in this design.

Table 9. System Clocks

| Name | Domain | Source | Desired Freq | Nominal Freq | Accuracy (%) | Start at Reset | Enabled |
|----------------|---------|------------|--------------|--------------|--------------|----------------|---------|
| BUS_CLK | DIGITAL | MASTER_CLK | ? MHz | 24 MHz | ±1 | True | True |
| PLL_OUT | DIGITAL | IMO | 24 MHz | 24 MHz | ±1 | True | True |
| MASTER_CLK | DIGITAL | PLL_OUT | ? MHz | 24 MHz | ±1 | True | True |
| IMO | DIGITAL | | 3 MHz | 3 MHz | ±1 | True | True |
| ILO | DIGITAL | | ? MHz | 1 kHz | -50,+100 | True | True |
| USB_CLK | DIGITAL | IMO | 48 MHz | ? MHz | ±0 | False | False |
| XTAL | DIGITAL | | 24 MHz | ? MHz | ±0 | False | False |
| XTAL 32kHz | DIGITAL | | 32.768 kHz | ? MHz | ±0 | False | False |
| Digital Signal | DIGITAL | | ? MHz | ? MHz | ±0 | False | False |

4.2 Local and Design Wide Clocks

Local clocks drive individual analog and digital blocks. Design wide clocks are a user-defined optimization, where two or more analog or digital blocks that share a common clock profile (frequency, etc) can be driven from the same clock divider output source.

Figure 4. Local and Design Wide Clock Configuration

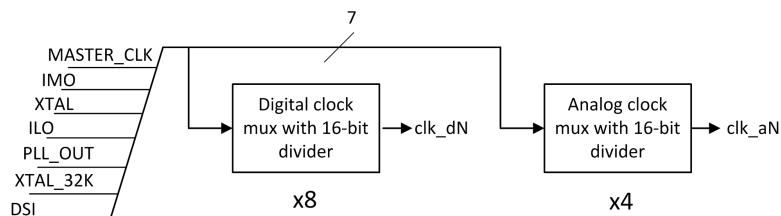


Table 10 lists the local clocks used in this design.

Table 10. Local Clocks

| Name | Domain | Source | Desired Freq | Nominal Freq | Accuracy (%) | Start at Reset | Enabled |
|-----------------------|---------|------------|--------------|--------------|--------------|----------------|---------|
| I2C_BusClock | DIGITAL | BUS_CLK | ? MHz | 24 MHz | ±1 | True | True |
| ADC_DeISig_Ext_CP_Clk | DIGITAL | MASTER_CLK | ? MHz | 24 MHz | ±1 | True | True |
| ADC_DeISig_theACLK | ANALOG | MASTER_CLK | 128 kHz | 127.66 kHz | ±1 | True | True |
| Clock_LO | ANALOG | MASTER_CLK | 20.2 kHz | 20.202 kHz | ±1 | True | True |
| transmit_clock | DIGITAL | MASTER_CLK | 20 kHz | 20 kHz | ±1 | False | True |
| timer_clock | DIGITAL | MASTER_CLK | 500 Hz | 500 Hz | ±1 | True | True |
| pwm_clock | DIGITAL | MASTER_CLK | 1 Hz | 366.211 Hz | ±1 | True | True |
| mixerFreq_clock | DIGITAL | IMO | 200 Hz | 200 Hz | ±1 | True | True |

- Clocking System chapter in the [PSoC 5LP Technical Reference Manual](#)
- Clocking chapter in the [System Reference Guide](#)
 - CyPLL API routines
 - CyIMO API routines
 - CyILO API routines
 - CyMaster API routines
 - CyXTAL API routines

5 Interrupts and DMAs

5.1 Interrupts

This design contains the following interrupt components: (0 is the highest priority)

Table 11. Interrupts

| Name | Intr Num | Vector | Priority |
|---------------------|----------|--------|----------|
| isr_filter | 0 | 0 | 7 |
| isr_mixerFreq | 1 | 1 | 7 |
| isr_trigger | 2 | 2 | 7 |
| isr_triggerBlocking | 3 | 3 | 7 |
| I2C_I2C_IRQ | 15 | 15 | 7 |
| ADC_DelSig_IRQ | 29 | 29 | 7 |

For more information on interrupts, please refer to:

- Interrupt Controller chapter in the [PSoC 5LP Technical Reference Manual](#)
- Interrupts chapter in the [System Reference Guide](#)
 - CyInt API routines and related registers
- Datasheet for [cy_isr component](#)

5.2 DMAs

This design contains the following DMA components: (0 is the highest priority)

Table 12. DMAs

| Name | Priority | Channel Number |
|------------|----------|----------------|
| DMA_DelSig | 2 | 10 |
| DMA_Filter | 2 | 8 |

For more information on DMAs, please refer to:

- PHUB and DMAC chapter in the [PSoC 5LP Technical Reference Manual](#)
- DMA chapter in the [System Reference Guide](#)
 - DMA API routines and related registers
- Datasheet for [cy_dma component](#)

6 Flash Memory

PSoC 5LP devices offer a host of Flash protection options and device security features that you can leverage to meet the security and protection requirements of an application. These requirements range from protecting configuration settings or Flash data to locking the entire device from external access.

Table 13 lists the Flash protection settings for your design.

Table 13. Flash Protection Settings

| Start Address | End Address | Protection Level |
|---------------|-------------|------------------|
| 0x0 | 0x3FFFF | U - Unprotected |

Flash memory is organized as rows with each row of flash having 256 bytes. Each flash row can be assigned one of four protection levels:

- U - Unprotected
- F - Factory Upgrade
- R - Field Upgrade
- W - Full Protection

For more information on Flash memory and protection, please refer to:

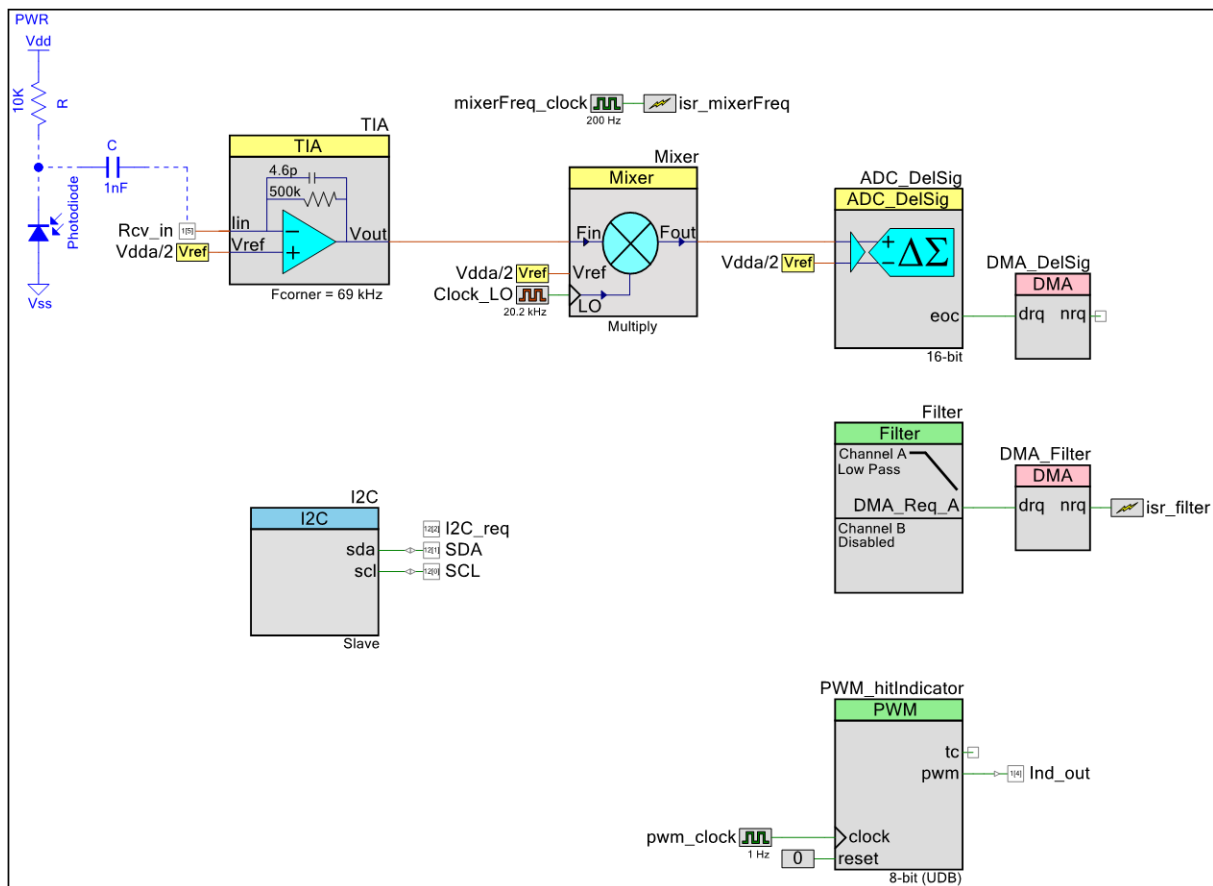
- Flash Protection chapter in the [PSoC 5LP Technical Reference Manual](#)
- Flash and EEPROM chapter in the [System Reference Guide](#)
 - CyWrite API routines
 - CyFlash API routines

7 Design Contents

This design's schematic content consists of the following 2 schematic sheets:

7.1 Schematic Sheet: Receiver

Figure 5. Schematic Sheet: Receiver

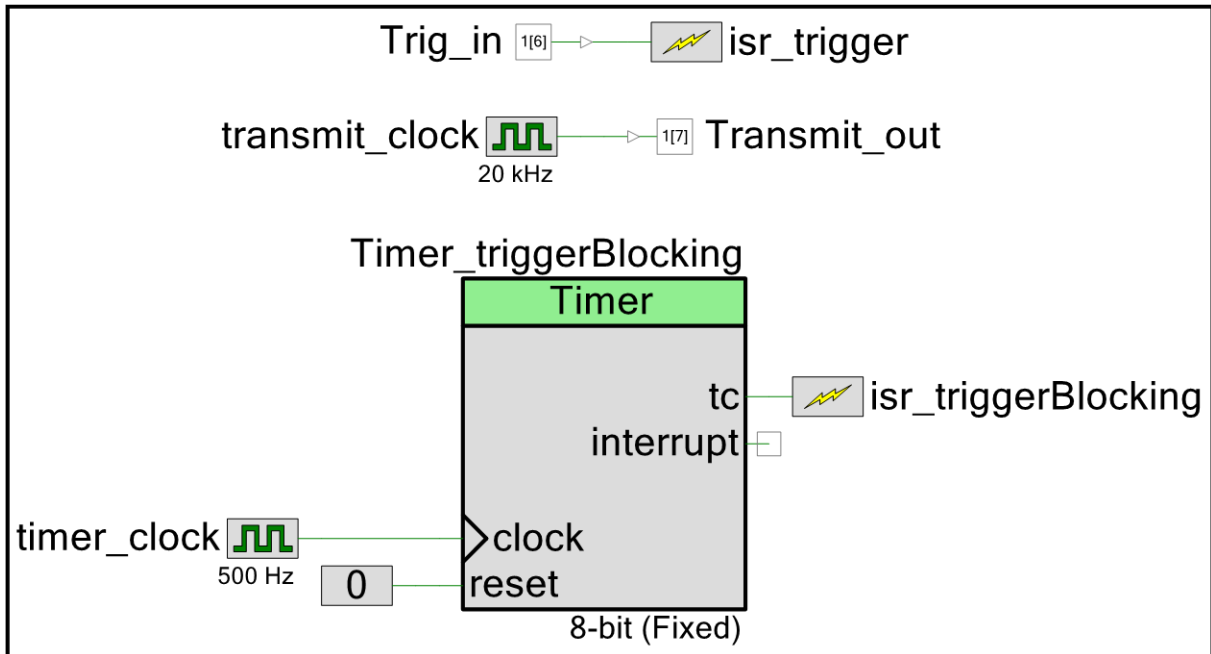


This schematic sheet contains the following component instances:

- Instance [ADC_DelSig](#) (type: ADC_DelSig_v3_30)
- Instance [Filter](#) (type: Filter_v2_30)
- Instance [I2C](#) (type: I2C_v3_50)
- Instance [Mixer](#) (type: Mixer_v2_0)
- Instance [PWM_hitIndicator](#) (type: PWM_v3_30)
- Instance [TIA](#) (type: TIA_v2_0)

7.2 Schematic Sheet: Transmitter

Figure 6. Schematic Sheet: Transmitter



This schematic sheet contains the following component instances:

- Instance [Timer_triggerBlocking](#) (type: Timer_v2_80)

8 Components

8.1 Component type: ADC_DelSig [v3.30]

8.1.1 Instance ADC_DelSig

Description: Delta-Sigma ADC

Instance type: ADC_DelSig [v3.30]

Datasheet: [online component datasheet for ADC_DelSig](#)

Table 14. Component Parameters for ADC_DelSig

| Parameter Name | Value | Description |
|-------------------------|----------------------|---|
| ADC_Alignment | Right | This parameter determines how the result is aligned in the 24 bit result word. |
| ADC_Alignment_Config2 | Right | This parameter determines how the result is aligned in the 24 bit result word. |
| ADC_Alignment_Config3 | Right | This parameter determines how the result is aligned in the 24 bit result word. |
| ADC_Alignment_Config4 | Right | This parameter determines how the result is aligned in the 24 bit result word. |
| ADC_Charge_Pump_Clock | true | Low power charge pump clock selection |
| ADC_Clock | Internal | Parameter for selecting the ADC clock type. |
| ADC_Input_Mode | Differential | Differential or Single ended input mode |
| ADC_Input_Range | -Input +/- 2*Vref | Choose input operating mode that best supports the range of the signals being measured. |
| ADC_Input_Range_Config2 | -Input +/- Vref | Choose input operating mode that best supports the range of the signals being measured. |
| ADC_Input_Range_Config3 | -Input +/- Vref | Choose input operating mode that best supports the range of the signals being measured. |
| ADC_Input_Range_Config4 | -Input +/- Vref | Choose input operating mode that best supports the range of the signals being measured. |
| ADC_Power | Medium Power | Sets power level of ADC. |
| ADC_Reference | Internal 1.024 Volts | Selects voltage reference source and configuration. |
| ADC_Reference_Config2 | Internal 1.024 Volts | Selects voltage reference source and configuration. |
| ADC_Reference_Config3 | Internal 1.024 Volts | Selects voltage reference source and configuration. |
| ADC_Reference_Config4 | Internal 1.024 Volts | Selects voltage reference source and configuration. |
| ADC_Resolution | 16 | ADC Resolution in bits |
| ADC_Resolution_Config2 | 16 | ADC Resolution in bits |
| ADC_Resolution_Config3 | 16 | ADC Resolution in bits |
| ADC_Resolution_Config4 | 16 | ADC Resolution in bits |

| Parameter Name | Value | Description |
|---------------------------|----------------|---|
| Clock_Frequency | 64000 | Determines the ADC clock frequency. |
| Comment_Config1 | Default Config | Parameter which holds the user comment for the config1. |
| Comment_Config2 | Second Config | Parameter which holds the user comment for the config2. |
| Comment_Config3 | Third Config | Parameter which holds the user comment for the config3. |
| Comment_Config4 | Fourth Config | Parameter which holds the user comment for the config4. |
| Config1_Name | CFG1 | This parameter is used to create constants in the header file for config 1. |
| Config2_Name | CFG2 | This parameter is used to create constants in the header file for config 2. |
| Config3_Name | CFG3 | This parameter is used to create constants in the header file for config 3. |
| Config4_Name | CFG4 | This parameter is used to create constants in the header file for config 4. |
| Configs | 1 | Number of active configurations |
| Conversion_Mode | 2 - Continuous | ADC conversion mode |
| Conversion_Mode_Config2 | 2 - Continuous | ADC conversion mode |
| Conversion_Mode_Config3 | 2 - Continuous | ADC conversion mode |
| Conversion_Mode_Config4 | 2 - Continuous | ADC conversion mode |
| Enable_Vref_Vss | false | Determines whether or not to connect ADC's reference Vssa to AGL[6]. |
| EnableModulatorInput | false | When this parameter is enabled, the modulator input terminal will be enabled on the symbol. |
| Input_Buffer_Gain | 1 | Gain of input amplifier |
| Input_Buffer_Gain_Config2 | 1 | Gain of input amplifier |
| Input_Buffer_Gain_Config3 | 1 | Gain of input amplifier |
| Input_Buffer_Gain_Config4 | 1 | Gain of input amplifier |
| Input_Buffer_Mode | Rail to Rail | Buffer Mode type selection |
| Input_Buffer_Mode_Config2 | Rail to Rail | Buffer Mode type selection |
| Input_Buffer_Mode_Config3 | Rail to Rail | Buffer Mode type selection |
| Input_Buffer_Mode_Config4 | Rail to Rail | Buffer Mode type selection |
| Ref_Voltage | 1.024 | Set reference voltage |
| Ref_Voltage_Config2 | 1.024 | Set reference voltage |
| Ref_Voltage_Config3 | 1.024 | Set reference voltage |
| Ref_Voltage_Config4 | 1.024 | Set reference voltage |
| rm_int | false | Removes internal interrupt (IRQ) |
| Sample_Rate | 2000 | Sample Rate in Hz |
| Sample_Rate_Config2 | 10000 | Sample Rate in Hz |
| Sample_Rate_Config3 | 10000 | Sample Rate in Hz |
| Sample_Rate_Config4 | 10000 | Sample Rate in Hz |
| Start_of_Conversion | Software | Continuous conversions or hardware controlled |
| User Comments | | Instance-specific comments. |

8.2 Component type: Filter [v2.30]

8.2.1 Instance Filter

Description: Filter consumes the entire DFB in one filter placement.

Instance type: Filter [v2.30]

Datasheet: [online component datasheet for Filter](#)

Table 15. Component Parameters for Filter

| Parameter Name | Value | Description |
|-------------------------|--------|---|
| ChannelEnableA | true | Channel Enable parameter for Channel A |
| ChannelEnableB | false | Channel Enable parameter for Channel B |
| ChannelTypeA | 1 | Parameter to hold filter type for Channel A |
| ChannelTypeB | 0 | Parameter to hold Filter type for Channel B |
| CoefficientEntryEnableA | false | CoefficientEntry enable parameter for channel A |
| CoefficientEntryEnableB | false | CoefficientEntry enable parameter for channel B |
| DisplaySettingsA | 50307 | Parameter to hold response display user settings for channel A |
| DisplaySettingsB | 50307 | Parameter to hold response display user settings for channel B |
| DmaEnableA | true | To Enable/Disable the DMA data ready signal for Channel A |
| DmaEnableB | false | To Enable/Disable the DMA data ready signal for Channel B |
| IrqEnableA | false | To Enable/Disable the interrupt data ready signal for channel A |
| IrqEnableB | false | To Enable/Disable the interrupt data ready signal for channel B |
| MinBusClockVal | 0.0181 | |
| User Comments | | Instance-specific comments. |

8.3 Component type: I2C [v3.50]

8.3.1 Instance I2C

Description: Standard I2C communication interface

Instance type: I2C [v3.50]

Datasheet: [online component datasheet for I2C](#)

Table 16. Component Parameters for I2C

| Parameter Name | Value | Description |
|----------------|----------|--|
| Address_Decode | Hardware | Determines either hardware or software address match logic. |
| BusSpeed_kHz | 100 | I2C Data Rate in kbps. Standard settings are 50, 100, 400 or 1000. The value must be between 1 and 1000. |

| Parameter Name | Value | Description |
|-----------------------------|---------------|--|
| EnableWakeup | false | Determines if I2C is selected as wakeup source. |
| ExternalBuffer | false | Exposes scl and sda in and out terminals outside the component. |
| Externi2cIntrHandler | false | Allows I2C interrupt handler to be set outside the I2C component. This feature intended only for PM/SM bus usage. |
| ExternTmoutIntrHandler | false | Allows I2C timeout interrupt handler to be set outside the I2C component. This feature intended only for PM/SM bus usage. |
| Hex | true | Indicates that address has been input in hexadecimal format. |
| I2C_Mode | Slave | Determines I2C mode (Slave/Master/Multi-Master/Multi-Master-Slave). |
| I2cBusPort | Any | Determines which I2C pins have been selected. Select I2C0/I2C1 and connect to corresponding pins to be able use I2C as wakeup source. |
| Implementation | FixedFunction | Determines either I2C implementation Fixed Function or UDB. |
| NotSlaveClockMinusTolerance | 25 | Internal component clock negative tolerance value in Master, Multi-Master or Multi-Master-Slave mode. |
| NotSlaveClockPlusTolerance | 5 | Internal component clock positive tolerance value in Master, Multi-Master or Multi-Master-Slave mode. |
| PrescalerEnabled | false | Enables prescaler (7-bit counter) to expand timeout timer range. |
| PrescalerPeriod | 3 | Prescaler period of timeout timer. |
| SclTimeoutEnabled | false | Enables low time monitoring of scl line. |
| SdaTimeoutEnabled | false | Enables low time monitoring of sda line. |
| Slave_Address | 8 | 7-bits I2C slave address. |
| SlaveClockMinusTolerance | 5 | Internal component clock negative tolerance value in Slave mode. |
| SlaveClockPlusTolerance | 50 | Internal component clock positive tolerance value in Slave mode. |
| TimeoutImplementation | UDB | Determines either timeout timer feature implementation as UDB or Fixed Function. The Fixed Function implementation only available for PSoC5LP. |

| Parameter Name | Value | Description |
|------------------------------|-------|--|
| TimeOutms | 25 | Determines maximum time allowed for scl or sda to be low state (in mS). The timeout timer generates interrupt after timeout expires. |
| TimeoutPeriodff | 39999 | Period of timeout timer (Fixed Function). |
| TimeoutPeriodUdb | 39999 | Period of timeout timer (UDB). |
| UdbInternalClock | false | Determines either internal or external clock source for I2C UDB. |
| UdbSlaveFixedPlacementEnable | false | Enables fixed placement for I2C UDB. Only available in slave mode. |
| User Comments | | Instance-specific comments. |

8.4 Component type: Mixer [v2.0]

8.4.1 Instance Mixer

Description: Signal Mixer

Instance type: Mixer [v2.0]

Datasheet: [online component datasheet for Mixer](#)

Table 17. Component Parameters for Mixer

| Parameter Name | Value | Description |
|------------------|---------------------|---|
| LO_clock_freq | 20.202 | Determines the LO clock frequency |
| LO_Source | External | Selects the LO Source: External or Internal |
| Mixer_Type | Multiply (Up) Mixer | Select Mixer type: Multiply (up mixing) or Sampling (down mixing) |
| Power | High | Selects the power level |
| Signal_Frequency | 11 | Input Signal Frequency. |
| User Comments | | Instance-specific comments. |

8.5 Component type: PWM [v3.30]

8.5.1 Instance PWM_hitIndicator

Description: 8 or 16-bit Pulse Width Modulator

Instance type: PWM [v3.30]

Datasheet: [online component datasheet for PWM](#)

Table 18. Component Parameters for PWM_hitIndicator

| Parameter Name | Value | Description |
|------------------------|-------|--|
| CaptureMode | None | Defines the functionality of the capture Input. The parameter determines which signal on the capture input is required to capture the current count value to the FIFO. |
| CompareStatusEdgeSense | true | Enables edge sense detection on compare outputs for use in edge sensitive interrupts |

| Parameter Name | Value | Description |
|-----------------|---------------|--|
| CompareType1 | Less | Sets the compare value comparison type setting for the compare 1 output |
| CompareType2 | Less | Sets the compare value comparison type setting for the compare 2 output |
| CompareValue1 | 102 | Compares Output 1 to value |
| CompareValue2 | 63 | Compares Output 2 to value |
| DeadBand | Disabled | Defines whether dead band outputs are desired or not. |
| DeadTime | 1 | Defines the number of required dead band clock cycles |
| DitherOffset | 0.00 | Allows the user to implement dither to get more bits out of a 8 or 16 bit PWM. |
| EnableMode | Software Only | Specifies the method of enabling the PWM. This can be either hardware or software. |
| FixedFunction | false | Determines whether the fixed function counter timer is used or the UDB implementation is used. |
| InterruptOnCMP1 | false | Enables the interrupt on compare1 true event |
| InterruptOnCMP2 | false | Enables the interrupt on compare2 true event |
| InterruptOnKill | false | Enables the interrupt on a kill event |
| InterruptOnTC | false | Enables the interrupt on terminal count event |
| KillMode | Disabled | Parameter to select the kill mode for build time. |
| MinimumKillTime | 1 | Sets the minimum number of clock cycles that a kill must be active on the outputs when KillMode is set to Minimum Kill Time mode |
| Period | 146 | Defines the PWM period value |
| PWMMode | One Output | Defines the overall mode of the PWM |
| Resolution | 8 | Defines the bit width of the PWM (8 or 16 bits) |
| RunMode | Continuous | Defines the run mode options to be either continuous or one shot |
| TriggerMode | None | Determines the mode of starting the PWM, i.e. triggering the PWM counter to start |
| UseInterrupt | false | Enables the placement and usage of the status register |
| User Comments | | Instance-specific comments. |

8.6 Component type: TIA [v2.0]

8.6.1 Instance TIA

Description: Trans-Impedance Amplifier

Instance type: TIA [v2.0]

userKitCtrlApp Datasheet

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Datasheet: [online component datasheet for TIA](#)

Table 19. Component Parameters for TIA

| Parameter Name | Value | Description |
|---------------------|------------|--|
| Capacitive_Feedback | 4.6 pF | Capacitive feedback for the TIA |
| Fcorner | 69 kHz | Calculated -3dB frequency for the given feedback settings. |
| Power | High Power | Power setting for TIA |
| Resistive_Feedback | 500k ohms | Nominal resistive feedback for the TIA |
| User Comments | | Instance-specific comments. |

8.7 Component type: Timer [v2.80]

8.7.1 Instance Timer_triggerBlocking

Description: 8, 16, 24 or 32-bit Timer

Instance type: Timer [v2.80]

Datasheet: [online component datasheet for Timer](#)

Table 20. Component Parameters for Timer_triggerBlocking

| Parameter Name | Value | Description |
|------------------------|---------------|--|
| CaptureAlternatingFall | false | Enables data capture on either edge but not until a valid falling edge is detected first. |
| CaptureAlternatingRise | false | Enables data capture on either edge but not until a valid rising edge is detected first. |
| CaptureCount | 2 | The CaptureCount parameter works as a divider on the hardware input "capture". A CaptureCount value of 2 would result in an actual capture taking place every other time the input "capture" is changed. |
| CaptureCounterEnabled | false | Enables the capture counter to count capture events (up to 127) before a capture is triggered. |
| CaptureMode | None | This parameter defines the capture input signal requirements to trigger a valid capture event |
| EnableMode | Software Only | This parameter specifies the methods in enabling the component. Hardware mode makes the enable input pin visible. Software mode may reduce the resource usage if not enabled. |
| FixedFunction | true | Configures the component to use fixed function HW block instead of the UDB implementation. |
| InterruptOnCapture | false | Parameter to check whether interrupt on a capture event is enabled or disabled. |

| Parameter Name | Value | Description |
|---------------------|------------|---|
| InterruptOnFIFOFull | false | Parameter to check whether interrupt on a FIFO Full event is enabled disabled. |
| InterruptOnTC | false | Parameter to check whether interrupt on a TC is enabled or disabled. |
| NumberOfCaptures | 1 | Number of captures allowed until the counter is cleared or disabled. |
| Period | 49 | Defines the timer period (This is also the reload value when terminal count is reached) |
| Resolution | 8 | Defines the resolution of the hardware. This parameter affects how many bits are used in the Period counter and defines the maximum resolution of the internal component signals. |
| RunMode | Continuous | Defines the hardware to run continuously, run until a terminal count is reached or run until an interrupt event is triggered. |
| TriggerMode | None | Defines the required trigger input signal to cause a valid trigger enable of the timer |
| User Comments | | Instance-specific comments. |

9 Other Resources

The following documents contain important information on Cypress software APIs that might be relevant to this design:

- Standard Types and Defines chapter in the [System Reference Guide](#)
 - Software base types
 - Hardware register types
 - Compiler defines
 - Cypress API return codes
 - Interrupt types and macros
- Registers
 - The full PSoC 5LP register map is covered in the [PSoC 5LP Registers Technical Reference Manual](#)
 - Register Access chapter in the [System Reference Guide](#)
 - § CY_GET API routines
 - § CY_SET API routines
- System Functions chapter in the [System Reference Guide](#)
 - General API routines
 - CyDelay API routines
 - CyVd Voltage Detect API routines
- Power Management
 - Power Supply and Monitoring chapter in the [PSoC 5LP Technical Reference Manual](#)
 - Low Power Modes chapter in the [PSoC 5LP Technical Reference Manual](#)
 - Power Management chapter in the [System Reference Guide](#)
 - § CyPm API routines
- Watchdog Timer chapter in the [System Reference Guide](#)
 - CyWdt API routines
- Cache Management
 - Cache Controller chapter in the [PSoC 5LP Technical Reference Manual](#)
 - Cache chapter in the [System Reference Guide](#)
 - § CyFlushCache() API routine