

# Performing dynamic partial reconfiguration on IntelFPGA technology using Quartus II

DR. ALEXANDER E. BEASLEY

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WIP

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# Chapter 1

## Introduction

This guide is intended for use with IntelFPGA's (formally Altera) Quartus II design software.

This guide will cover starting a new project, creating and instantiating a dynamic partial reconfiguration controller, creating reconfigurable design revisions and generating output files.

Device families supported:

- Cyclone V
- Arria 10
- Stratix V

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## Chapter 2

# Creating a new project

This chapter covers creating a new project using the Quartus II new project wizard. A dynamically reconfigurable project can be started in just the same way as a static logic design.

Opening Quartus II will give the splash screen seen in Figure 2.1.

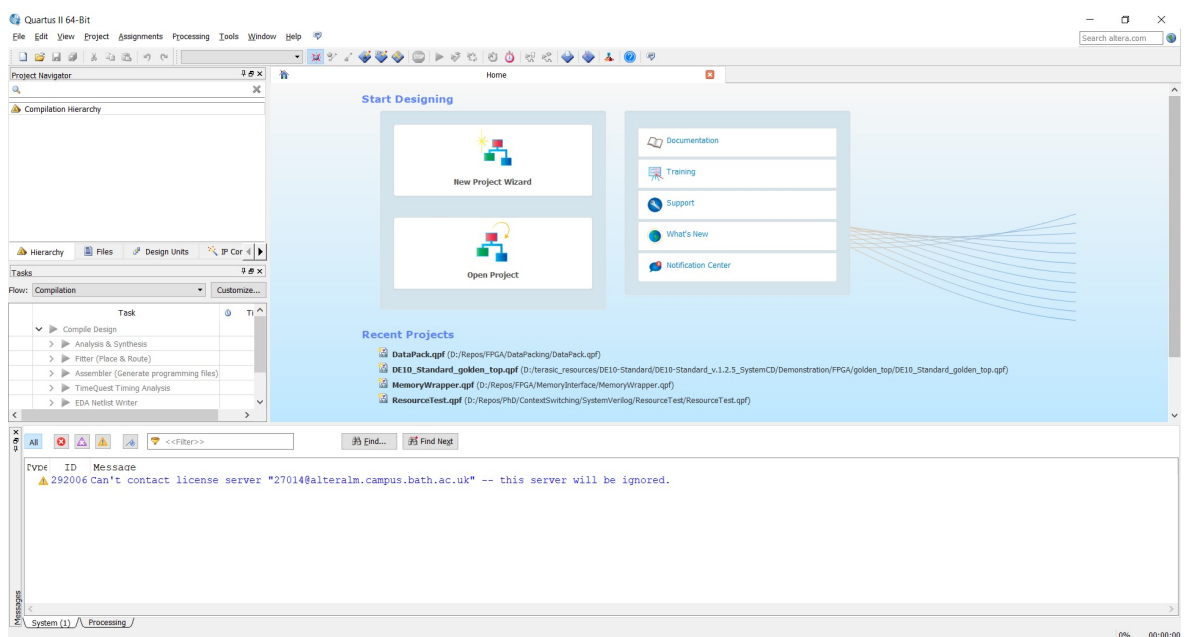


Figure 2.1: Quartus II start screen

Start the new project wizard using the ‘new project wizard’ button or ‘File >new...’. The new project dialogue as seen in Figure 2.2 will open. From this, select ‘New Quartus II Project’.

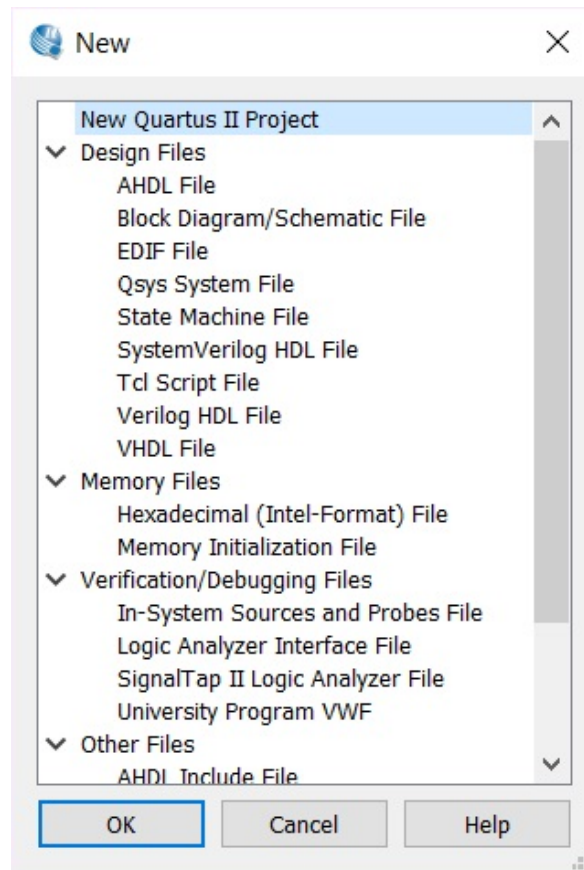


Figure 2.2: Quartus II new project dialogue

Figure 2.3 shows the introduction page for a new project. The page summarises each step of the new project wizard. Select 'Next'.

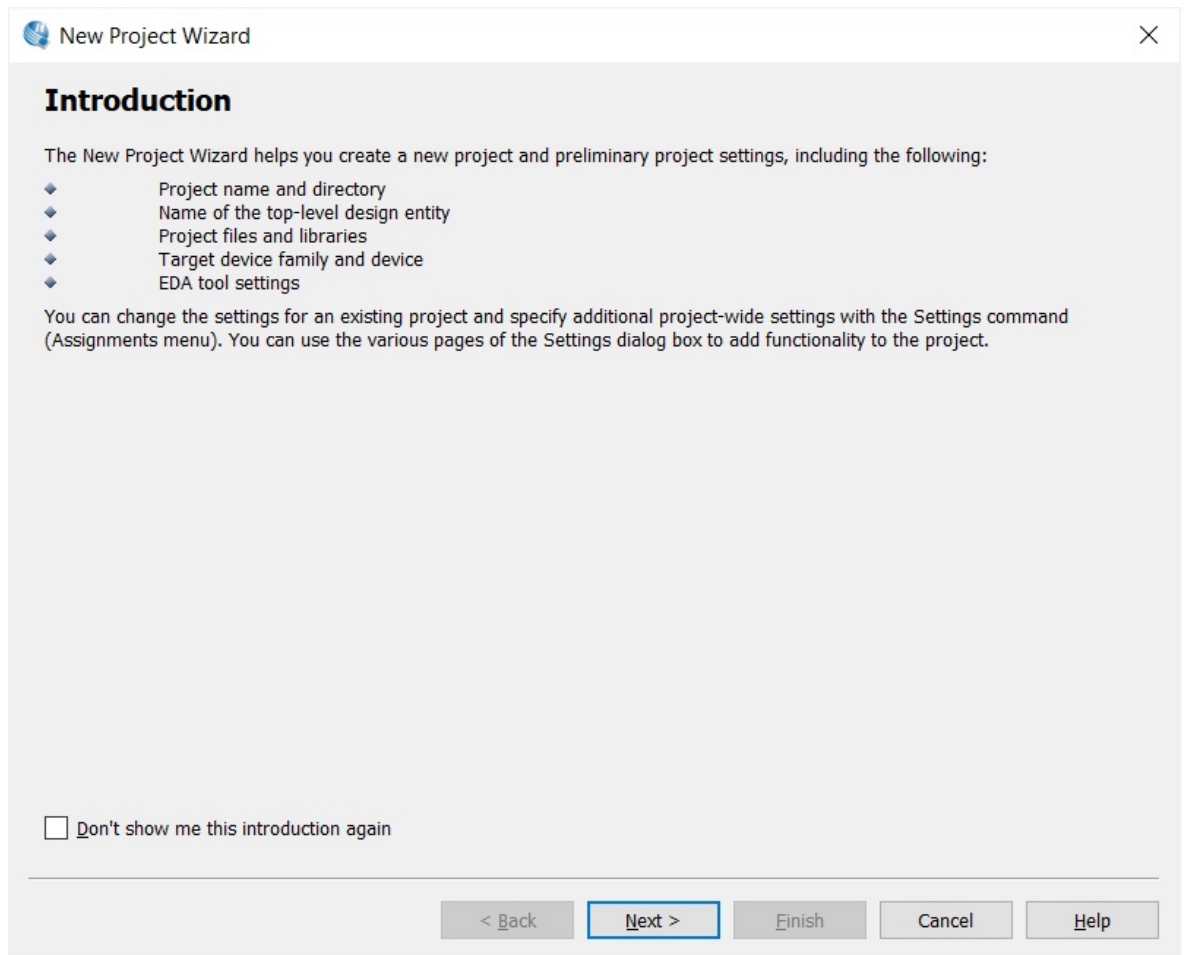


Figure 2.3: Quartus II new project introduction

The next page will ask for some basic file path information for the project (Figure@2.4). Fill the top box in with the directory in which the project will be stored. Enter the name of the top level module in the second and third boxes. Typically these will be the same, as prompted by the form auto filling the third box with the contents of the second box.



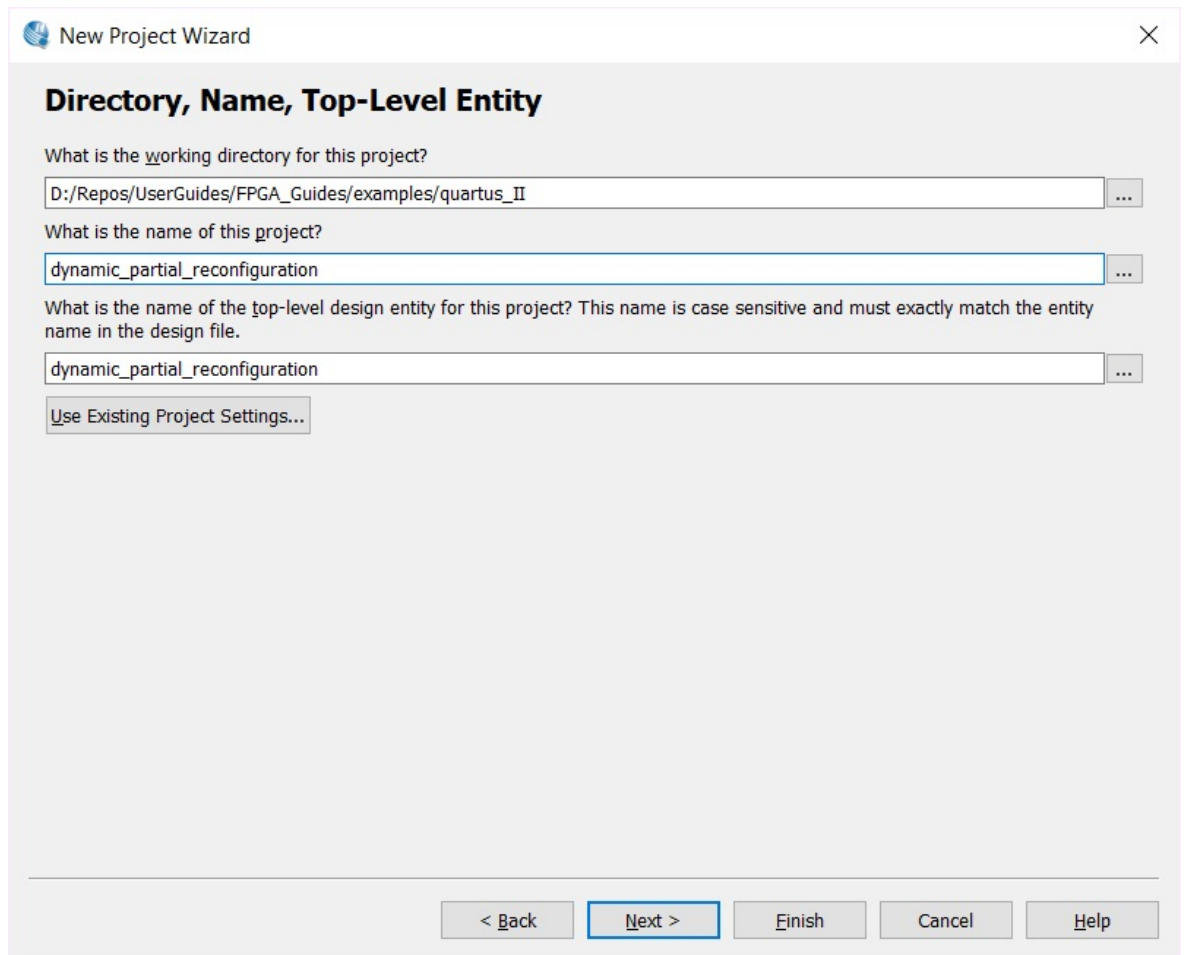


Figure 2.4: Quartus II new project location

From the project type window (Figure 2.5) select 'Empty project'.

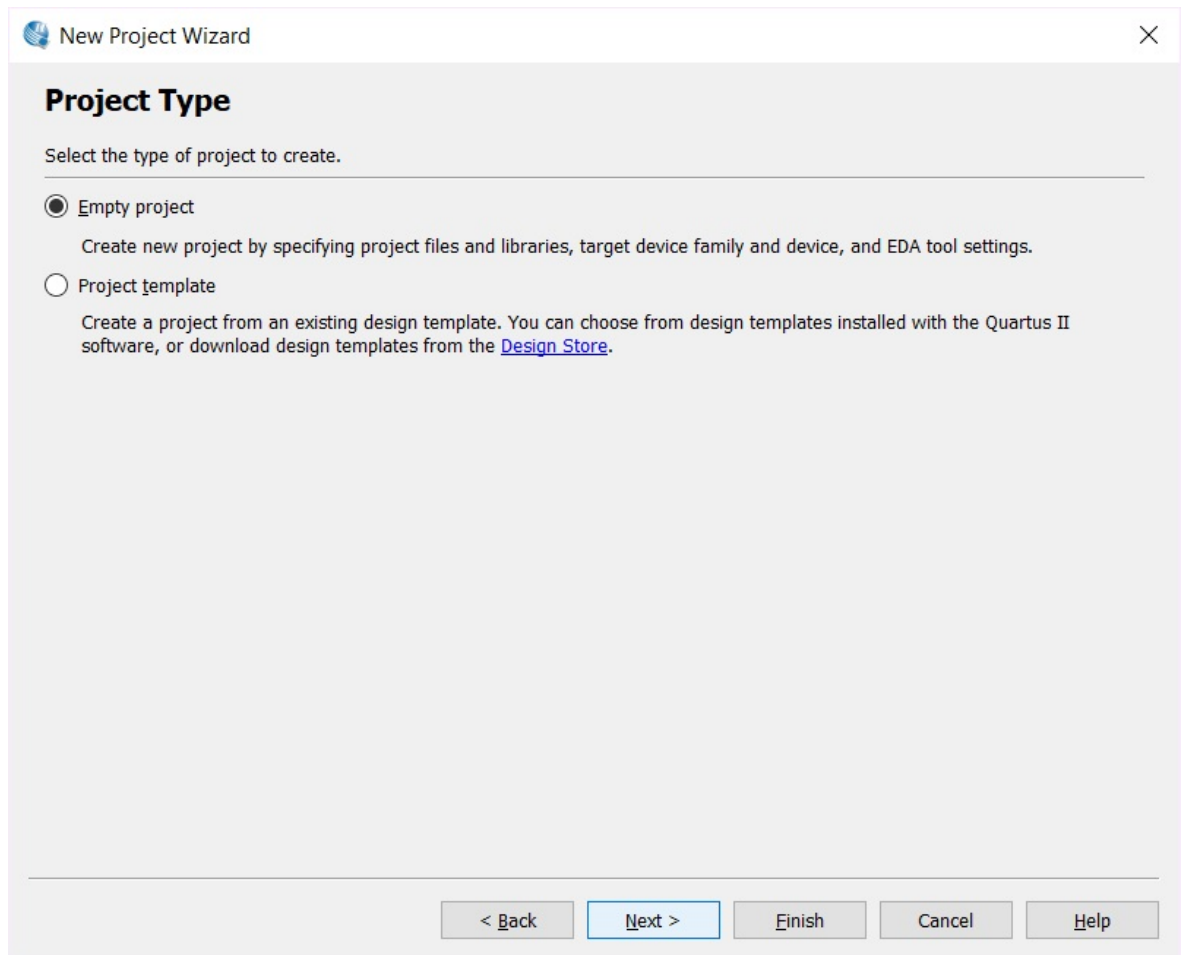


Figure 2.5: Quartus II new project type

In the Add Files window (Figure 2.6) click on the ‘...’ button to navigate to any existing design files you wish to add to the project. Once finished, or if you have no files, select ‘Next’.

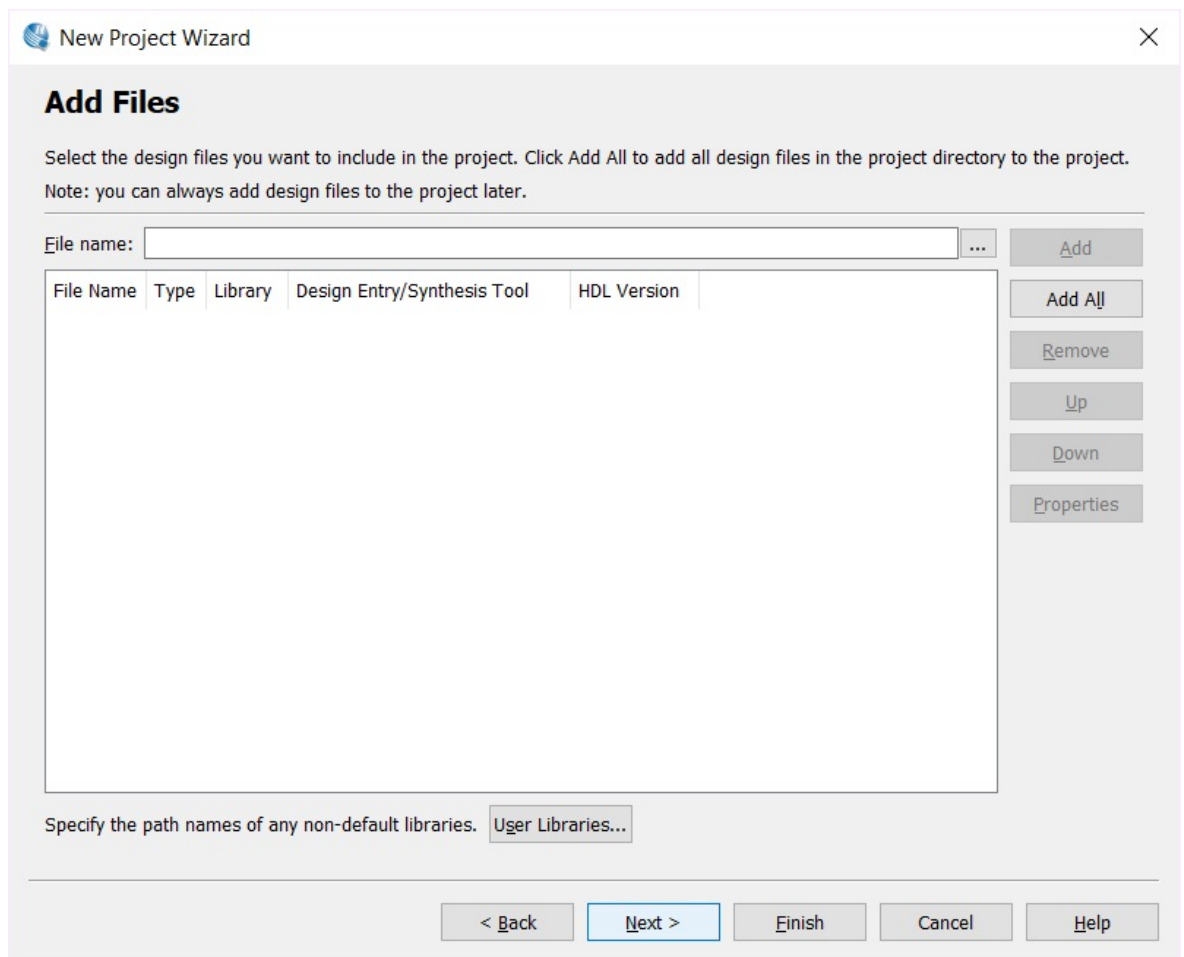


Figure 2.6: Quartus II add existing files to new project

In the Family & Device Settings window (Figure 2.7) choose the device you will be implementing your design on. You will need the device family support pack installed for the family of devices you are using. These can be found on the downloads page of the IntelFPGA along with the Quartus II software.

**New Project Wizard**

### Family & Device Settings

Select the family and device you want to target for compilation.  
You can install additional device support with the Install Devices command on the Tools menu.

To determine the version of the Quartus II software in which your target device is supported, refer to the [Device Support List](#) webpage.

Device family

Family: Cyclone V (E/GX/GT/SX/SE/ST)

Devices: All

Target device

☐ Auto device selected by the Fitter

☒ Specific device selected in 'Available devices' list

☐ Other: n/a

Show in 'Available devices' list

Package: Any

Pin count: Any

Core Speed grade: Any

Name filter: 5CSXFC6D6F31C6

☒ Show advanced devices

Available devices:

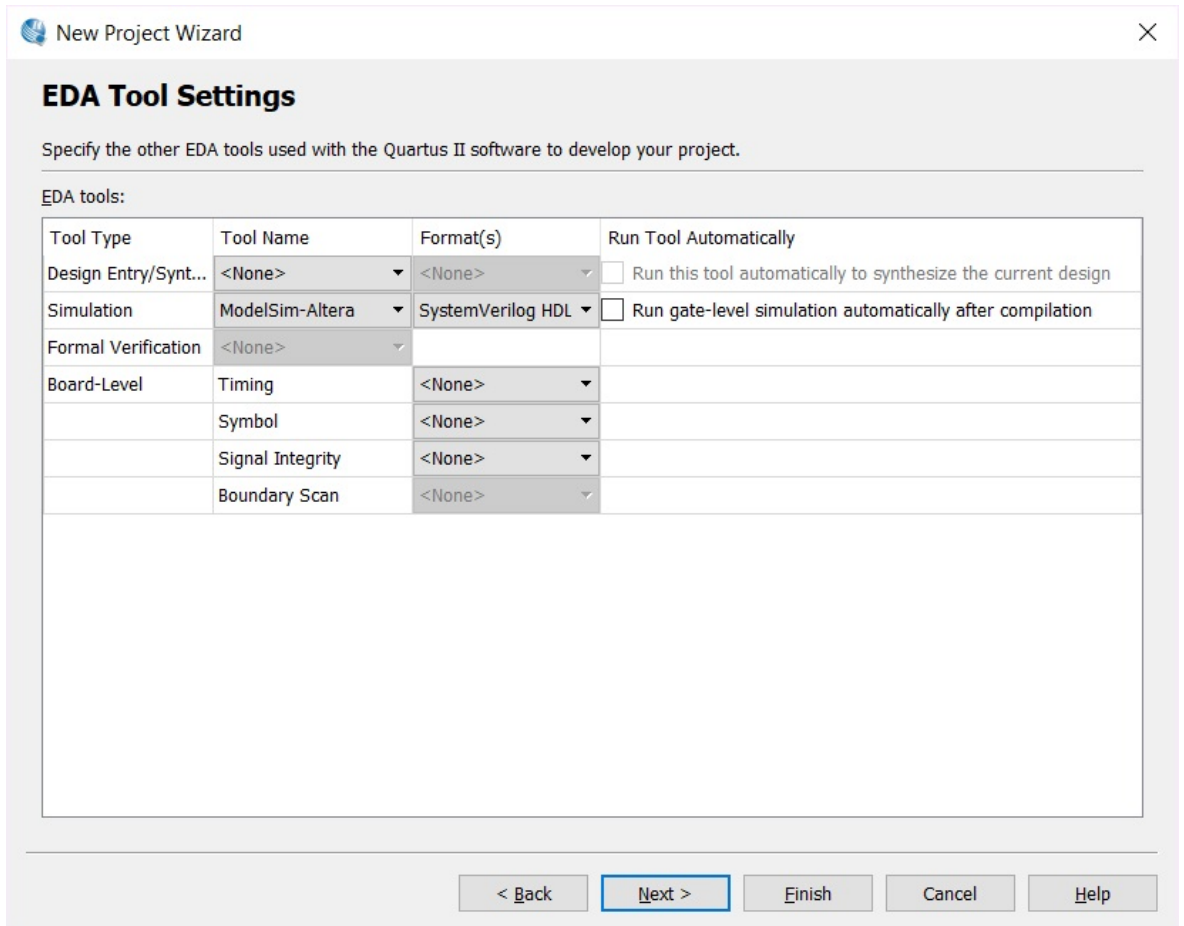
Name	Core Voltage	ALMs	Total I/Os	GPIOs	GXB Channel PMA	GXB Channel PC
5CSXFC6D6F31C6	1.1V	41910	499	457	9	9

< Back   **Next >**   Finish   Cancel   Help

Figure 2.7: Quartus II select device

The EDA Tool Settings page (Figure 2.8) allows you to specify any additional tools you wish to use during implementing and verification. The defaults for these fields are <None>. If you do not have any other verification software, leave the fields as their default setting. These options can be changed later in the settings dialogue.

*N.B. when you download the Quartus II software, you have the option to download ModelSim-Altera. This is a licence free version of Mentor's ModelSim software that can be used to perform logic simulation.*



**EDA Tool Settings**

Specify the other EDA tools used with the Quartus II software to develop your project.

EDA tools:

Tool Type	Tool Name	Format(s)	Run Tool Automatically
Design Entry/Synt...	<None>	<None>	<input type="checkbox"/> Run this tool automatically to synthesize the current design
Simulation	ModelSim-Altera	SystemVerilog HDL	<input type="checkbox"/> Run gate-level simulation automatically after compilation
Formal Verification	<None>		
Board-Level	Timing	<None>	
	Symbol	<None>	
	Signal Integrity	<None>	
	Boundary Scan	<None>	

< Back   Next >   Finish   Cancel   Help

Figure 2.8: Quartus II set EDA tool settings

Once you have worked your way through the ‘new project wizard’ a summary of your settings will be shown (Figure 2.9). Click Finish’ to start designing using Quartus II.

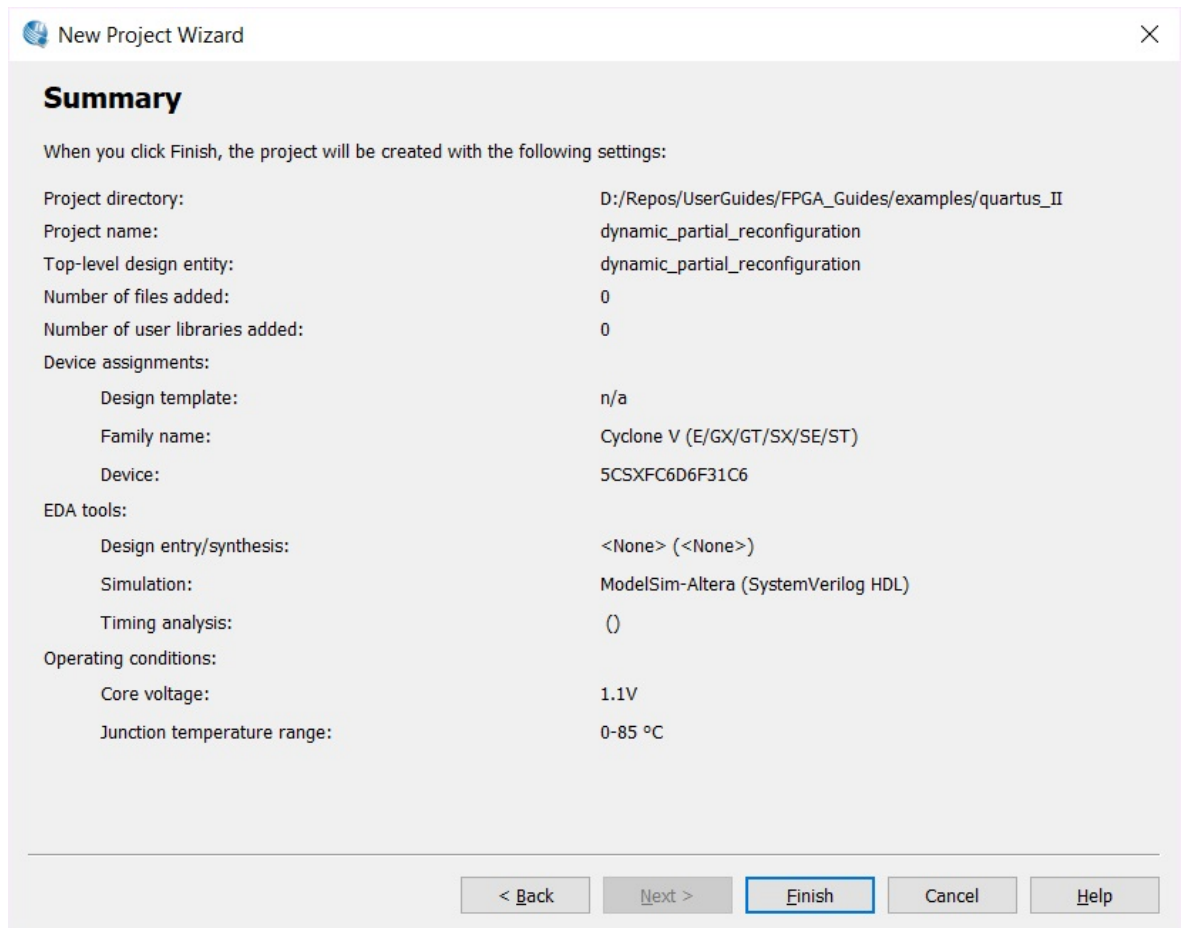


Figure 2.9: Quartus II new project summary

To open a blank design file choose ‘File >New ...’ or use the blank page symbol in the top left (under File) to open the ‘New ...’ dialogue. From this select the type of design file you require, for example ‘SystemVerilog File’. This will open up a blank text file and automatically include it in the source files list for the project. When you save the file, the file extension will default to the correct extension for the Hardware Descriptive Language (HDL) you have chosen.