
**SiPEED**

Sheet: /PWR\_TREE/  
File: PWR\_TREE.kicad\_sch

Title: Tang\_Mega\_138K\_Dock

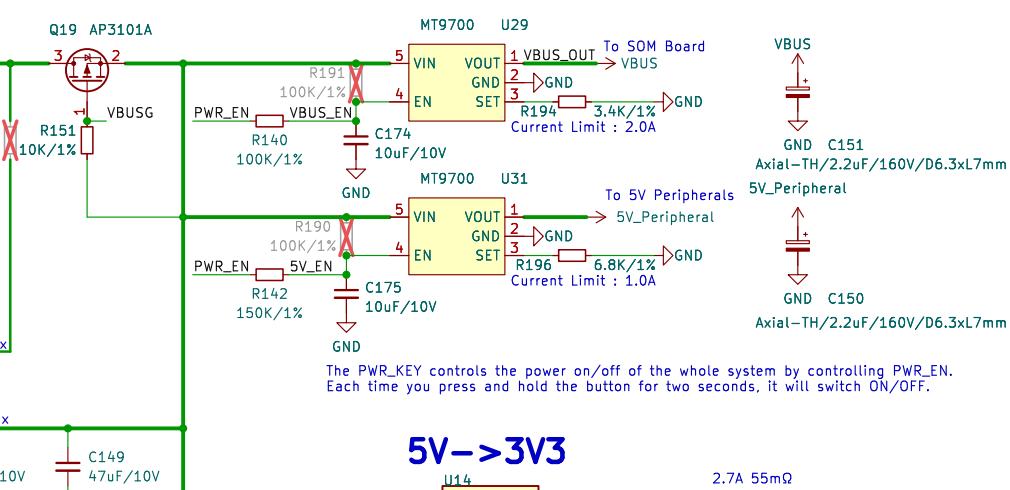
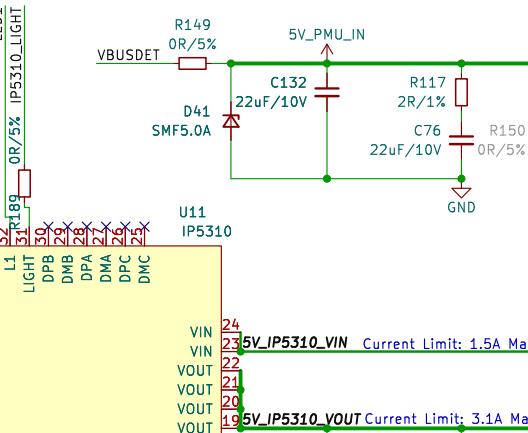
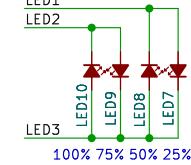
Size: A4 Date: 2024-08-28

KiCad E.D.A. 8.0.6

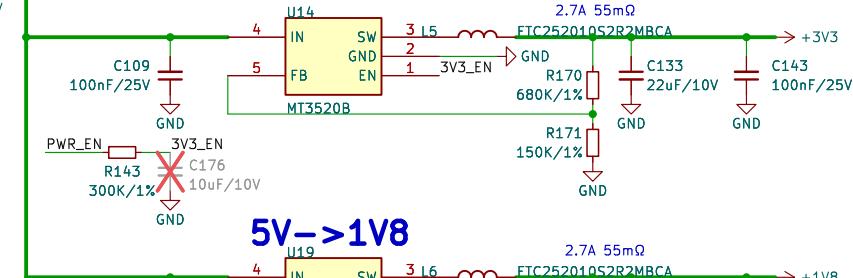
Rev: 1.2

Id: 2/21

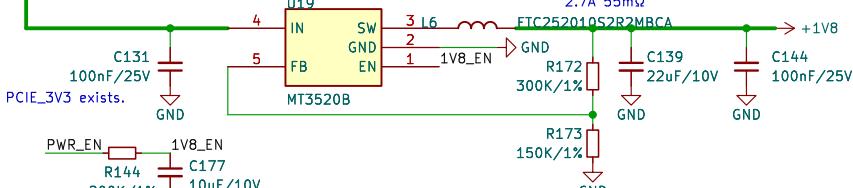
# PMIC



**5V->3V3**



**5V->1V8**



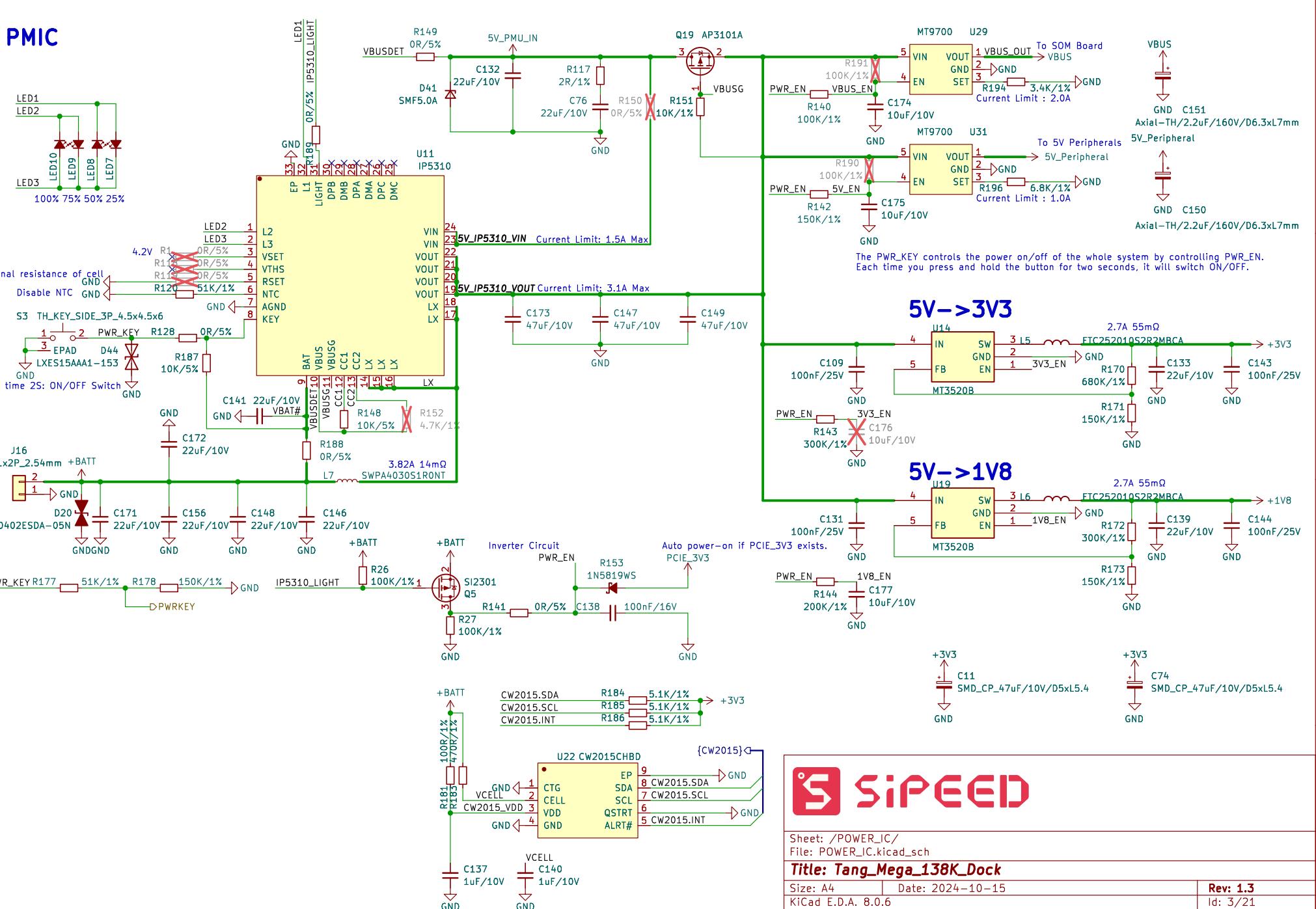
**SiPEED**

Sheet: /POWER\_IC/  
File: POWER\_IC.kicad\_sch

Title: Tang\_Mega\_138K\_Dock

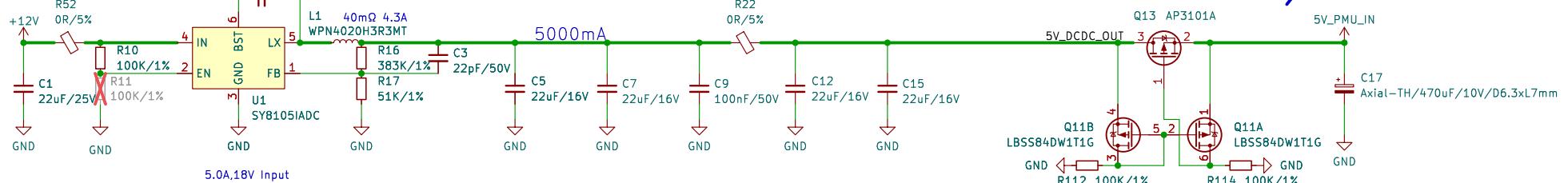
Size: A4 Date: 2024-10-15  
KiCad E.D.A. 8.0.6

Rev: 1.3  
Id: 3/21

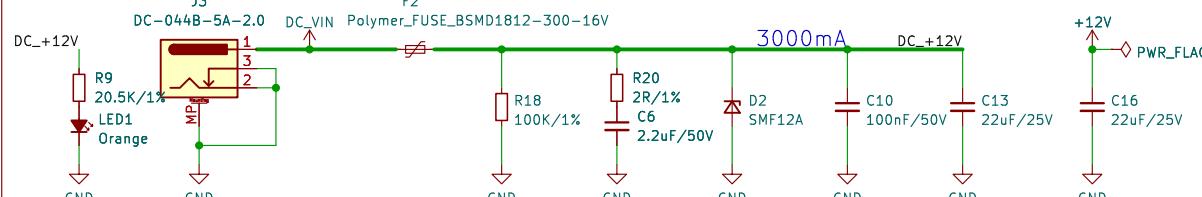


## 5V0 DC-DC

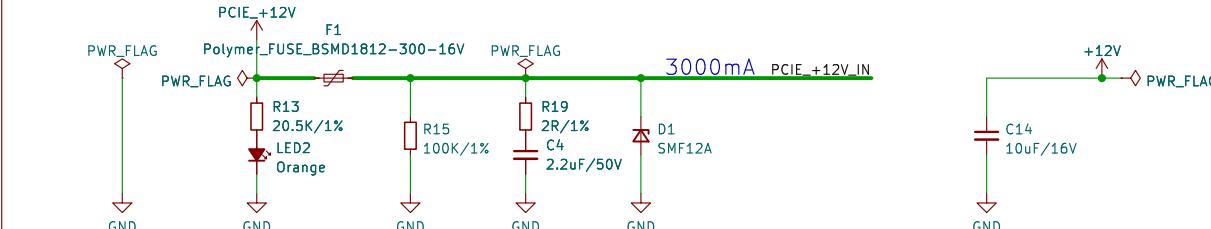
$$V_{out} = 0.6 * (1 + 383K / 51K) \approx 5.10V$$



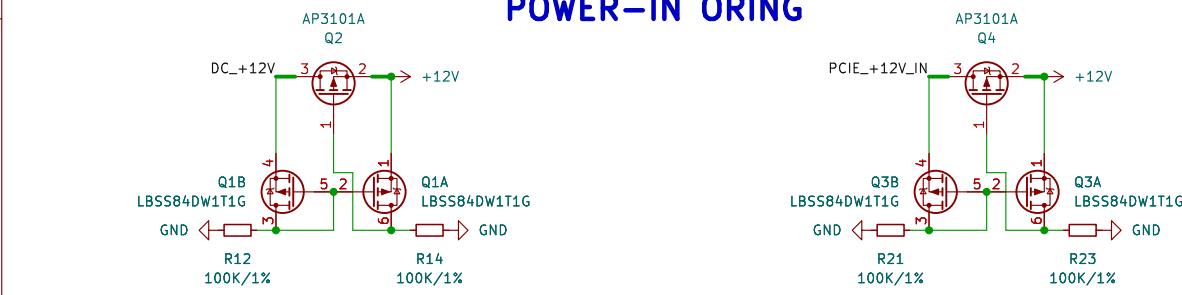
## 12V DC-IN



## 12V PCIE-IN



## POWER-IN ORING



SiPEED

Sheet: /POWER/  
File: SYS\_POWER.kicad\_sch

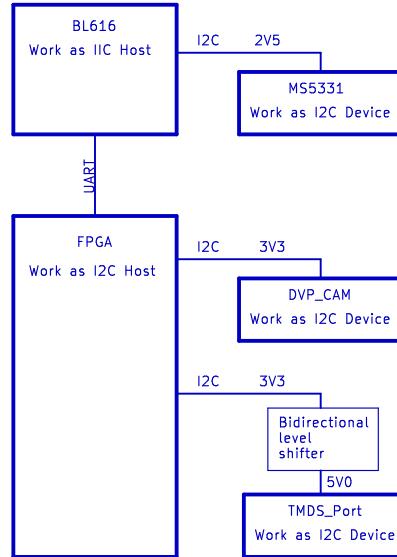
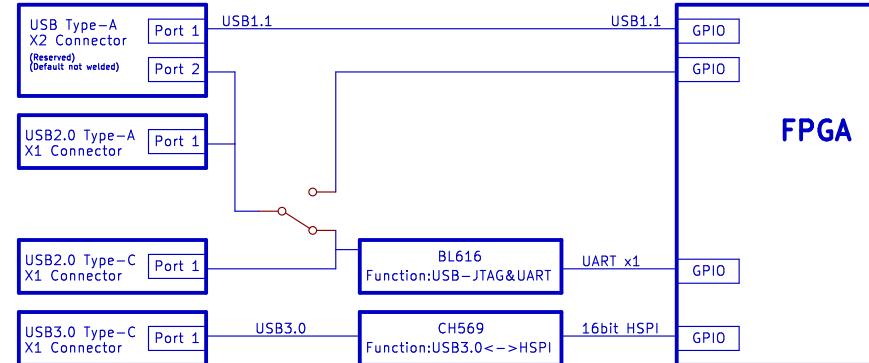
Title: Tang\_Mega\_138K\_Dock

Size: A4 Date: 2024-10-15  
KiCad E.D.A. 8.0.6

Rev: 1.3  
Id: 4/21

A

A

**IIC connection****USB connection**

B

B

C

C

D

D



Sheet: /Block\_Diagram/  
File: Block\_Diagram.kicad\_sch

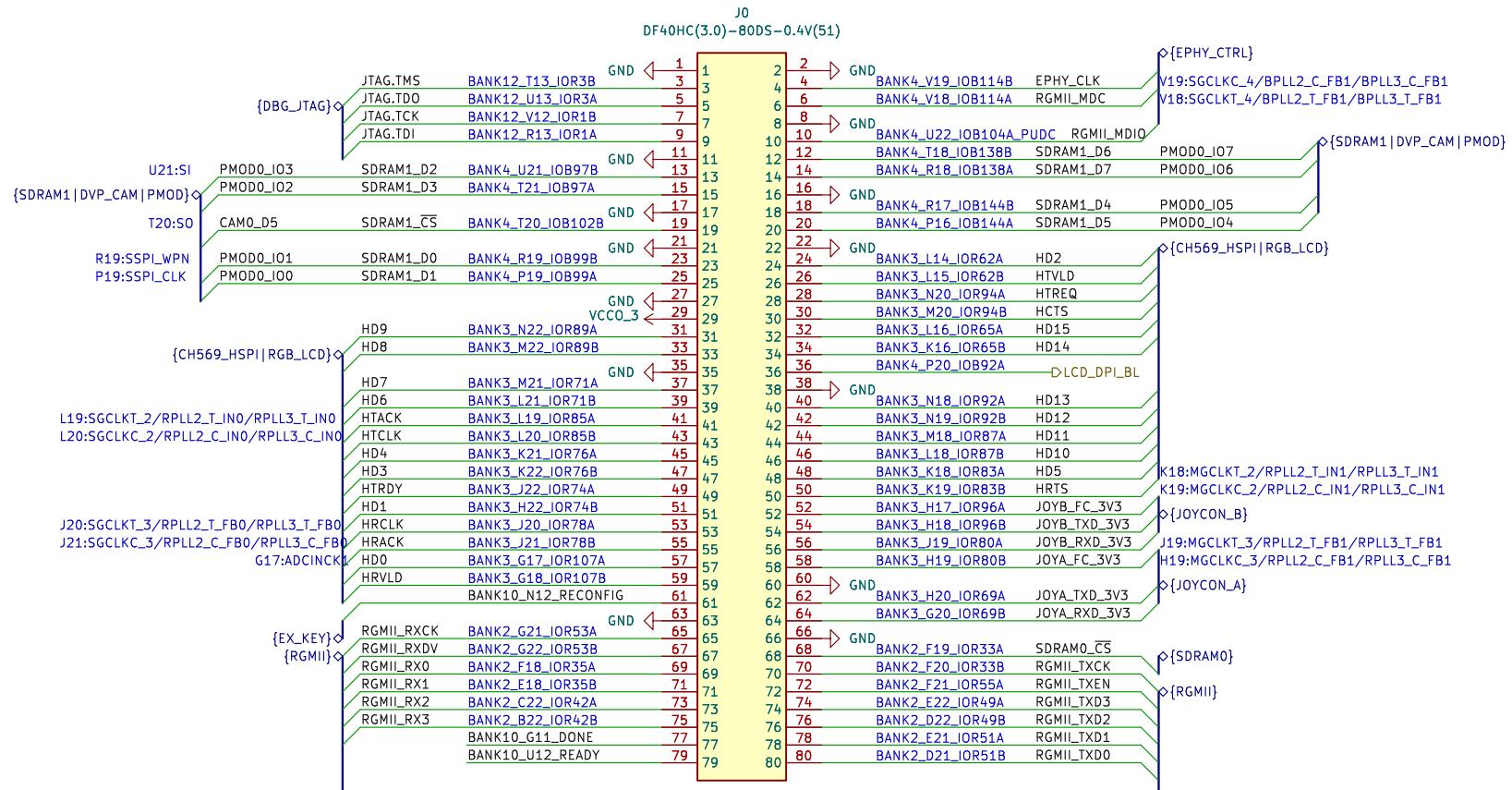
**Title: Tang\_Mega\_138K\_Dock**

Size: A4 Date: 2024-10-15

KiCad E.D.A. 8.0.6

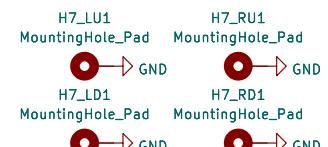
**Rev: 1.3**

Id: 5/21



H5  
MH\_HEATSINK

H6  
MH\_HEATSINK



 SiPEED

Sheet: /SOM\_BTB0/  
File: SOM\_BTB0.kicad\_sch

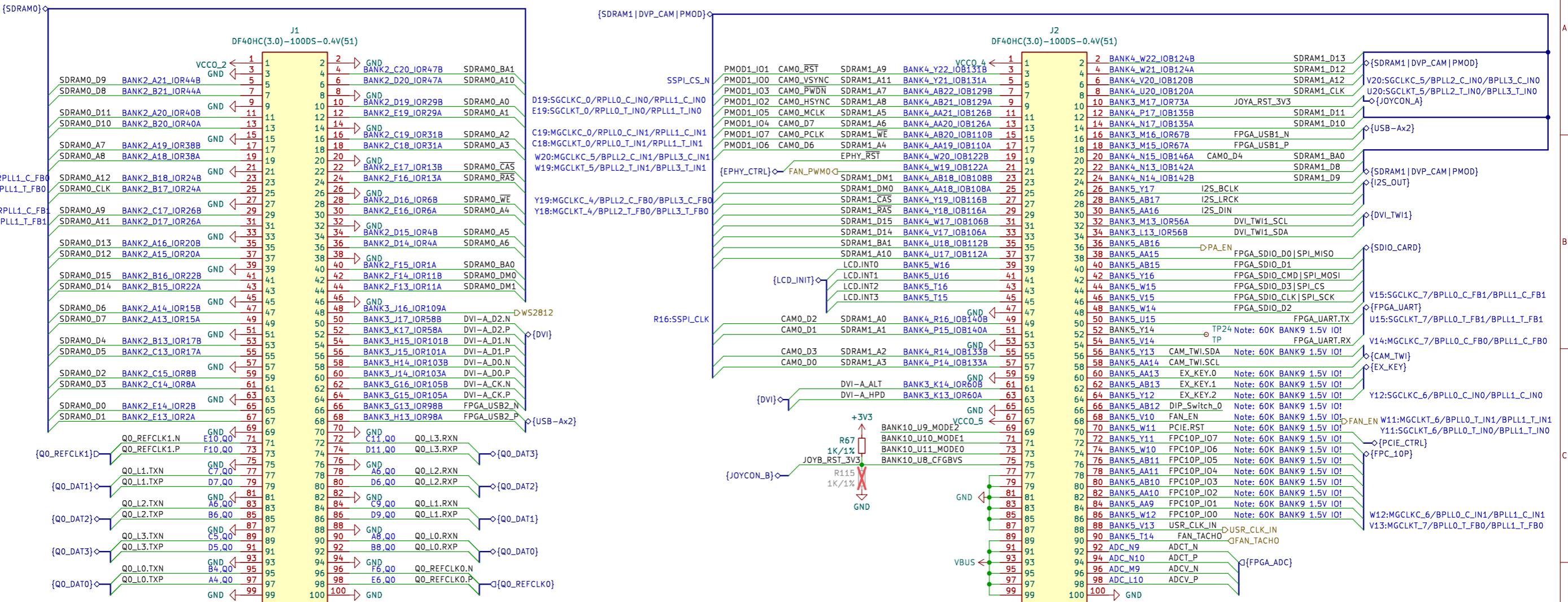
Title: Tang\_Mega\_138K\_Dock

Size: A4 Date: 2024-10-15

KiCad E.D.A. 8.0.6

Rev: 1.3

Id: 6/21

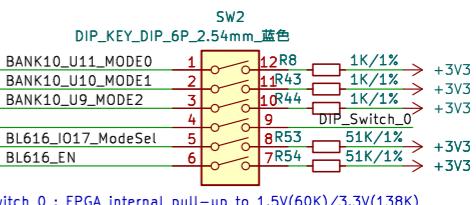


VCC0\_2 TP

VCC0\_3 TP

VCC0\_4 TP

VCC0\_5 TP

**Switch****SiPEED**Sheet: /SOM\_BT1&2/  
File: SOM\_BT1-2.kicad\_sch**Title: Tang\_Mega\_138K\_Dock**

Size: A3 Date: 2024-10-15

KiCad E.D.A. 8.0.6

Rev: 1.3

Id: 7/21

表 4-2 GW5AT-138/GW5AST-138 配置模式选择

配置模式	MODE[2:0] <sup>[1]</sup>	Bus Width	相关说明
JTAG	XXX/101 <sup>[3]</sup>	-	外部 Host 通过 JTAG 接口对 GW5AT & GW5AST 系列 FPGA 产品进行配置
MSPI <sup>[2]</sup>	001	x1,x2,x4	FPGA 作为 Master，通过 SPI 接口从外部 Flash（或其他器件）读取配置数据进行配置
SSPI <sup>[2]</sup>	010	x1,x4	外部 Host 通过 SPI 接口对 GW5AT & GW5AST 系列 FPGA 产品进行配置
Master SERIAL	000	x1	FPGA 作为 Slave 以前，通过 DIN 接口从外部读取配置数据进行配置
Slave SERIAL	111	x1	外部 Host 通过 DIN 接口对 GW5AT & GW5AST 系列 FPGA 产品进行配置
Master CPU	100	x8,x16,x32	FPGA 作为 Slave 以前，通过 DBUS 接口从外部读取配置数据进行配置
Slave CPU	110	x8,x16,x32	外部 Host 通过 DBUS 接口对 GW5AT & GW5AST 系列 FPGA 产品进行配置

Table 4-2 GW5AT-138/GW5AST-138 Configuration Modes

Configuration Mode	MODE[2:0] <sup>[1]</sup>	Bus Width	Description
JTAG	XXX/101 <sup>[3]</sup>	-	GW5AT & GW5AST series of FPGA products are configured by external Host via JTAG interface
MSPI <sup>[2]</sup>	001	x1, x2, x4	As a Master, FPGA reads data from external Flash (or other devices) via the SPI interface for configuration
SSPI <sup>[2]</sup>	010	x1, x4	GW5AT & GW5AST series of FPGA products are configured by external Host via SPI interface
Master SERIAL	000	x1	Before FPGA used as a Slave, FPGA reads data from external devices via the DIN interface for configuration
Slave SERIAL	111	x1	GW5AT & GW5AST series of FPGA products are configured by external Host via DIN interface
Master CPU	100	x8, x16, x32	Before FPGA used as a Slave, FPGA reads data from external devices via the DBUS interface for configuration
Slave CPU	110	x8, x16, x32	GW5AT & GW5AST series of FPGA products are configured by external Host via DBUS interface

BL616 SEL[0..1] SWITCH

NO.	CONFIG	SEL0(EN)	SEL1(MODE)
0	Disable BL616 Use other debugger	0	X
1	JTAG mode	1	1
2	Game mode	1	0

GND R2 150K/1% BL616\_EN  
GND R3 150K/1% BL616\_ModeSel

{DBG\_MODE}

GND R4 1.5K/5% BANK10\_U11\_MODE0  
GND R5 1.5K/5% BANK10\_U10\_MODE1  
GND R6 1.5K/5% BANK10\_U9\_MODE2  
GND R7 1.5K/5% BANK10\_U8\_CFGBVSBL616\_I017\_ModeSel 1 1K/1% +3V3  
BL616\_I017\_ModeSel 2 1K/1% +3V3  
BL616\_I017\_ModeSel 3 1K/1% +3V3  
BL616\_I017\_ModeSel 4 1K/1% +3V3  
BL616\_I017\_ModeSel 5 51K/1% +3V3  
BL616\_I017\_ModeSel 6 51K/1% +3V3BL616\_EN 7 51K/1% +3V3  
BL616\_EN 8 51K/1% +3V3

DIP\_Switch\_0 : FPGA internal pull-up to 1.5V(60K)/3.3V(138K)

TP20  
TP21  
TP22  
TP23GND R1 1.5K/5% BANK10\_U10\_MODE1  
GND R2 1.5K/5% BANK10\_U9\_MODE2  
GND R3 1.5K/5% BANK10\_U8\_CFGBVSBL616\_I017\_ModeSel 1 1K/1% +3V3  
BL616\_I017\_ModeSel 2 1K/1% +3V3  
BL616\_I017\_ModeSel 3 1K/1% +3V3  
BL616\_I017\_ModeSel 4 1K/1% +3V3  
BL616\_I017\_ModeSel 5 51K/1% +3V3  
BL616\_I017\_ModeSel 6 51K/1% +3V3

DIP\_Switch\_0 : FPGA internal pull-up to 1.5V(60K)/3.3V(138K)

GND R1 1.5K/5% BANK10\_U10\_MODE1  
GND R2 1.5K/5% BANK10\_U9\_MODE2  
GND R3 1.5K/5% BANK10\_U8\_CFGBVSBL616\_I017\_ModeSel 1 1K/1% +3V3  
BL616\_I017\_ModeSel 2 1K/1% +3V3  
BL616\_I017\_ModeSel 3 1K/1% +3V3  
BL616\_I017\_ModeSel 4 1K/1% +3V3  
BL616\_I017\_ModeSel 5 51K/1% +3V3  
BL616\_I017\_ModeSel 6 51K/1% +3V3

DIP\_Switch\_0 : FPGA internal pull-up to 1.5V(60K)/3.3V(138K)

GND R1 1.5K/5% BANK10\_U10\_MODE1  
GND R2 1.5K/5% BANK10\_U9\_MODE2  
GND R3 1.5K/5% BANK10\_U8\_CFGBVSBL616\_I017\_ModeSel 1 1K/1% +3V3  
BL616\_I017\_ModeSel 2 1K/1% +3V3  
BL616\_I017\_ModeSel 3 1K/1% +3V3  
BL616\_I017\_ModeSel 4 1K/1% +3V3  
BL616\_I017\_ModeSel 5 51K/1% +3V3  
BL616\_I017\_ModeSel 6 51K/1% +3V3

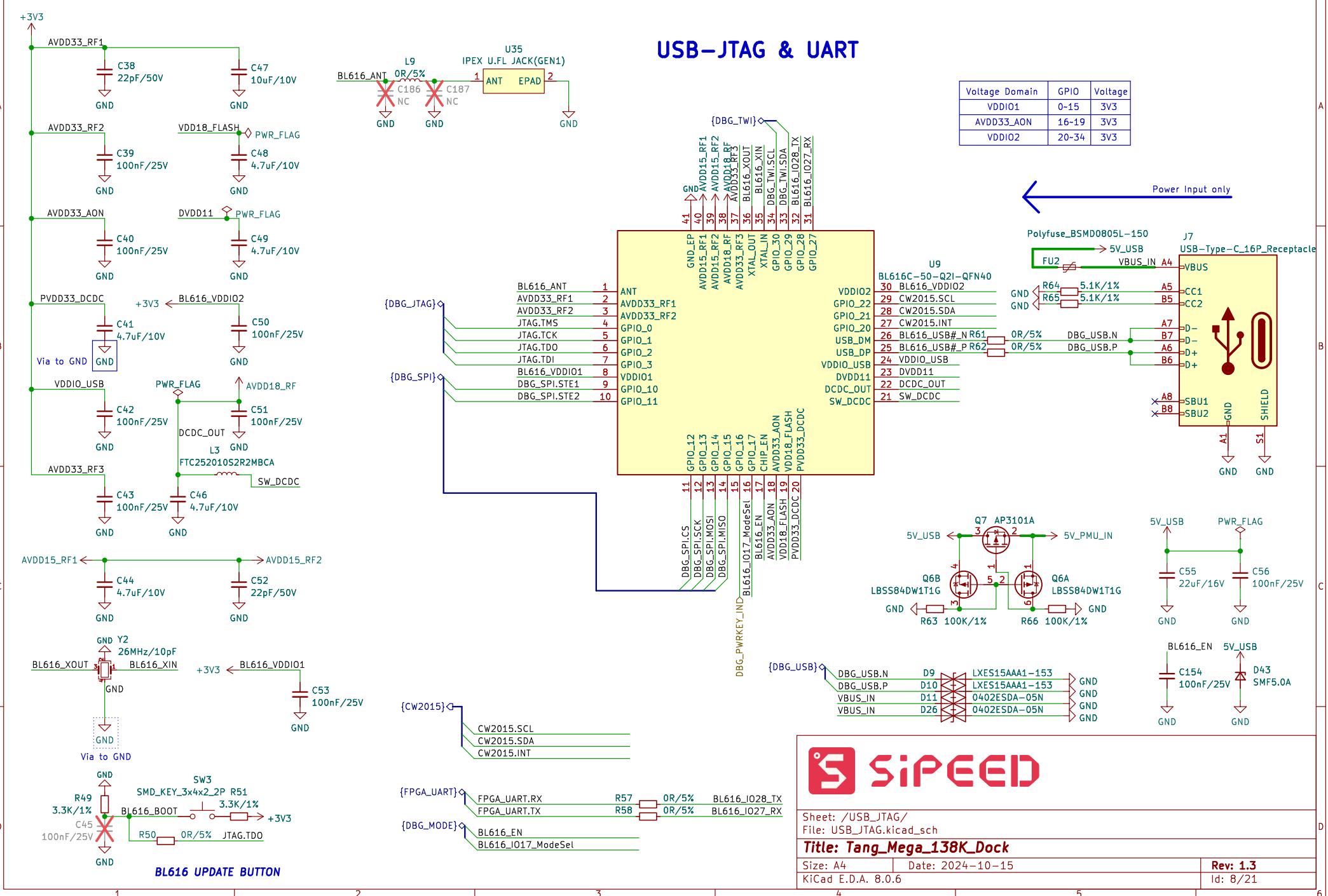
DIP\_Switch\_0 : FPGA internal pull-up to 1.5V(60K)/3.3V(138K)

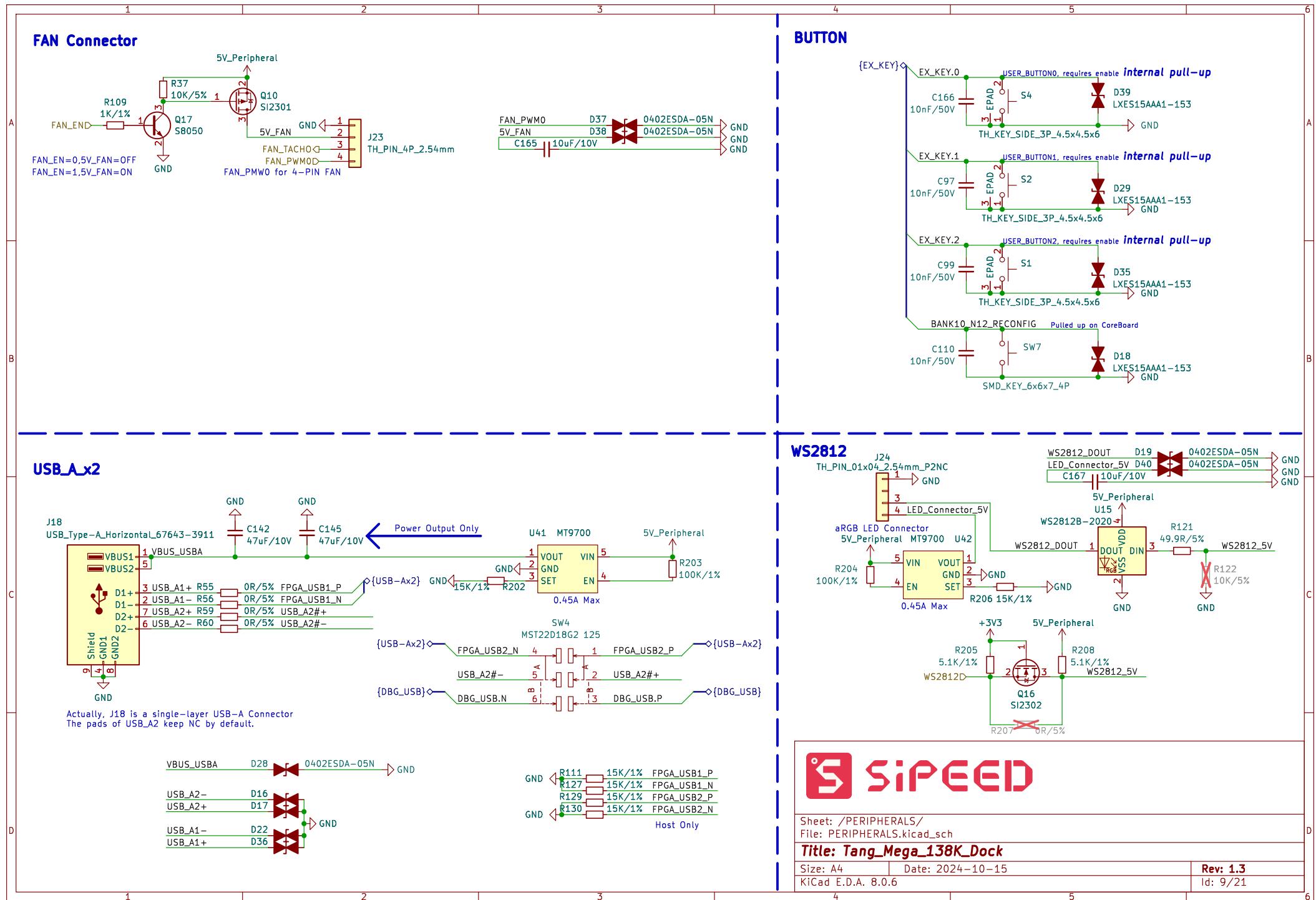
GND R1 1.5K/5% BANK10\_U10\_MODE1  
GND R2 1.5K/5% BANK10\_U9\_MODE2  
GND R3 1.5K/5% BANK10\_U8\_CFGBVSBL616\_I017\_ModeSel 1 1K/1% +3V3  
BL616\_I017\_ModeSel 2 1K/1% +3V3  
BL616\_I017\_ModeSel 3 1K/1% +3V3  
BL616\_I017\_ModeSel 4 1K/1% +3V3  
BL616\_I017\_ModeSel 5 51K/1% +3V3  
BL616\_I017\_ModeSel 6 51K/1% +3V3

DIP\_Switch\_0 : FPGA internal pull-up to 1.5V(60K)/3.3V(138K)

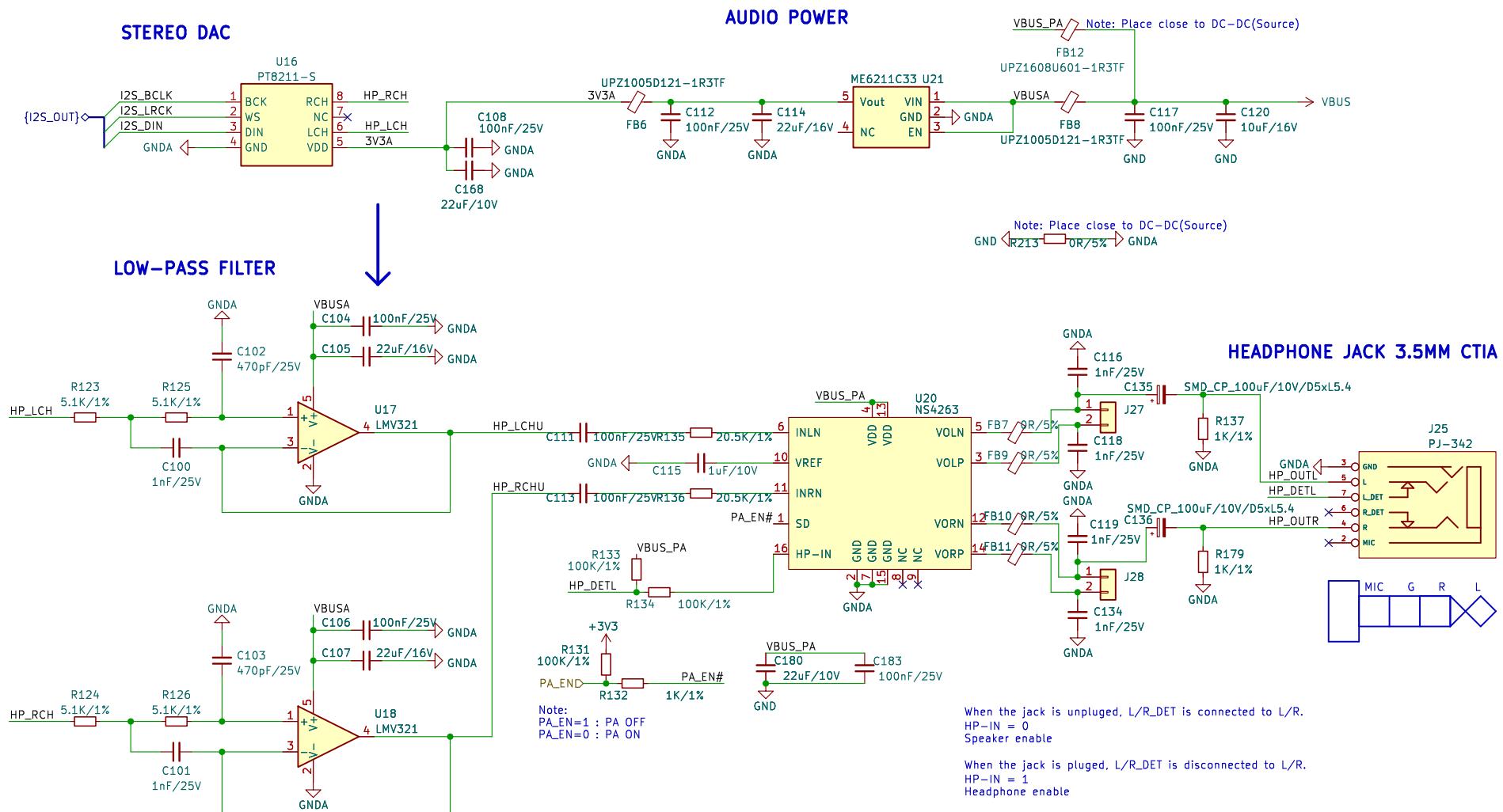
GND R1 1.5K/5% BANK10\_U10\_MODE1  
GND R2 1.5K/5% BANK10\_U9\_MODE2  
GND R3 1.5K/5% BANK10\_U8\_CFGBVSBL616\_I017\_ModeSel 1 1K/1% +3V3  
BL616\_I017\_ModeSel 2 1K/1% +3V3  
BL616\_I017\_ModeSel 3 1K/1% +3V3  
BL616\_I017\_ModeSel 4 1K/1% +3V

## USB-JTAG & UART





FPGA-Audio



Sheet: /FPGA\_AUDIO/  
File: DAC+PA.kicad\_sch

Sheet: /FPGA\_AUDIO/  
File: DAC+PA.kicad\_sch

Title: Tang Mega 138K Dock

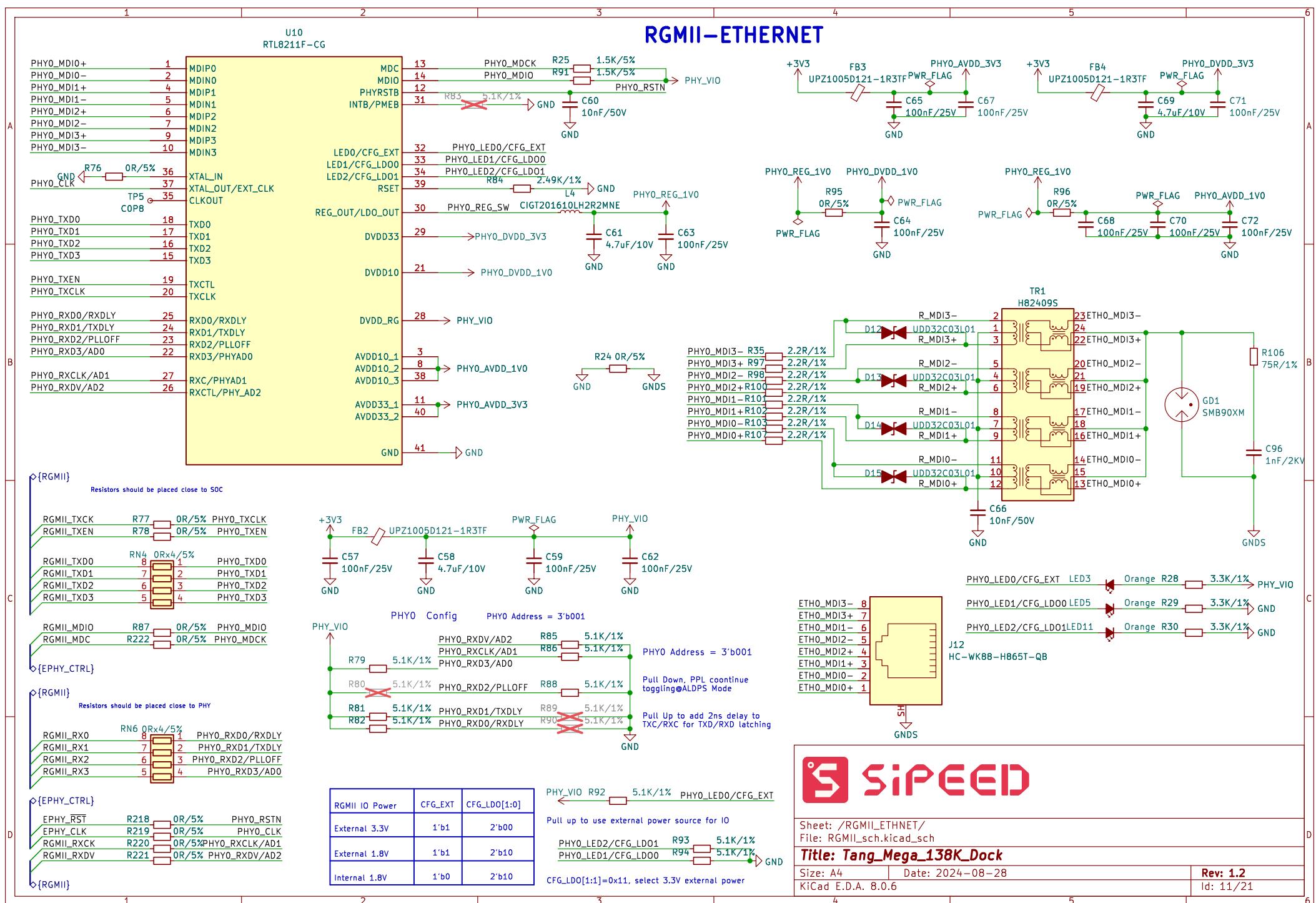
Size: A4 Date: 2024-10-15

KiCad E.D.A. 8.0.6

Rev: 1.3

Id: 10/21

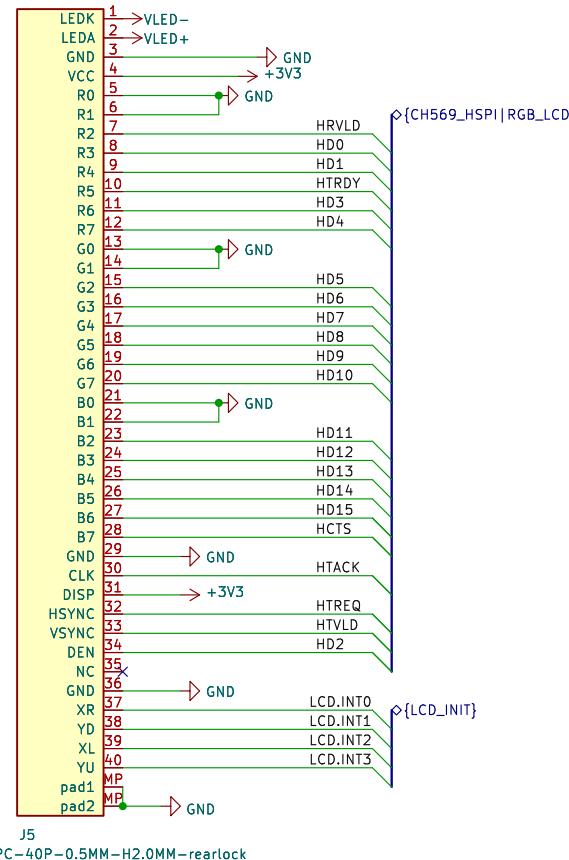
# RGMII-ETHERNET



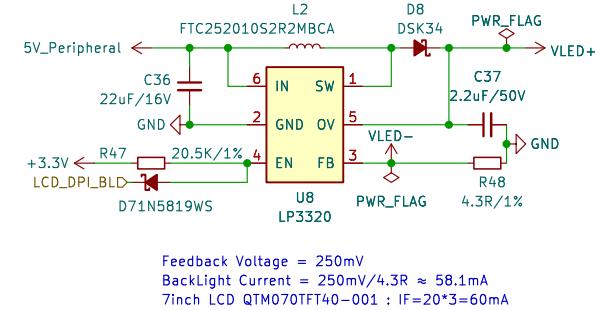
# RGB LCD Display

A

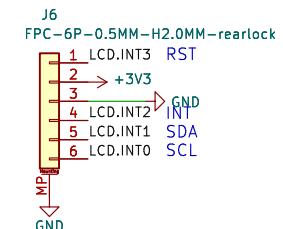
## RGB LCD Display Connector



## BACKLIGHT Driver



## Capacitive Touch Connector



LCD.INT1 R192 5.1K/1% → +3V3  
LCD.INT0 R193 5.1K/1% → +3V3



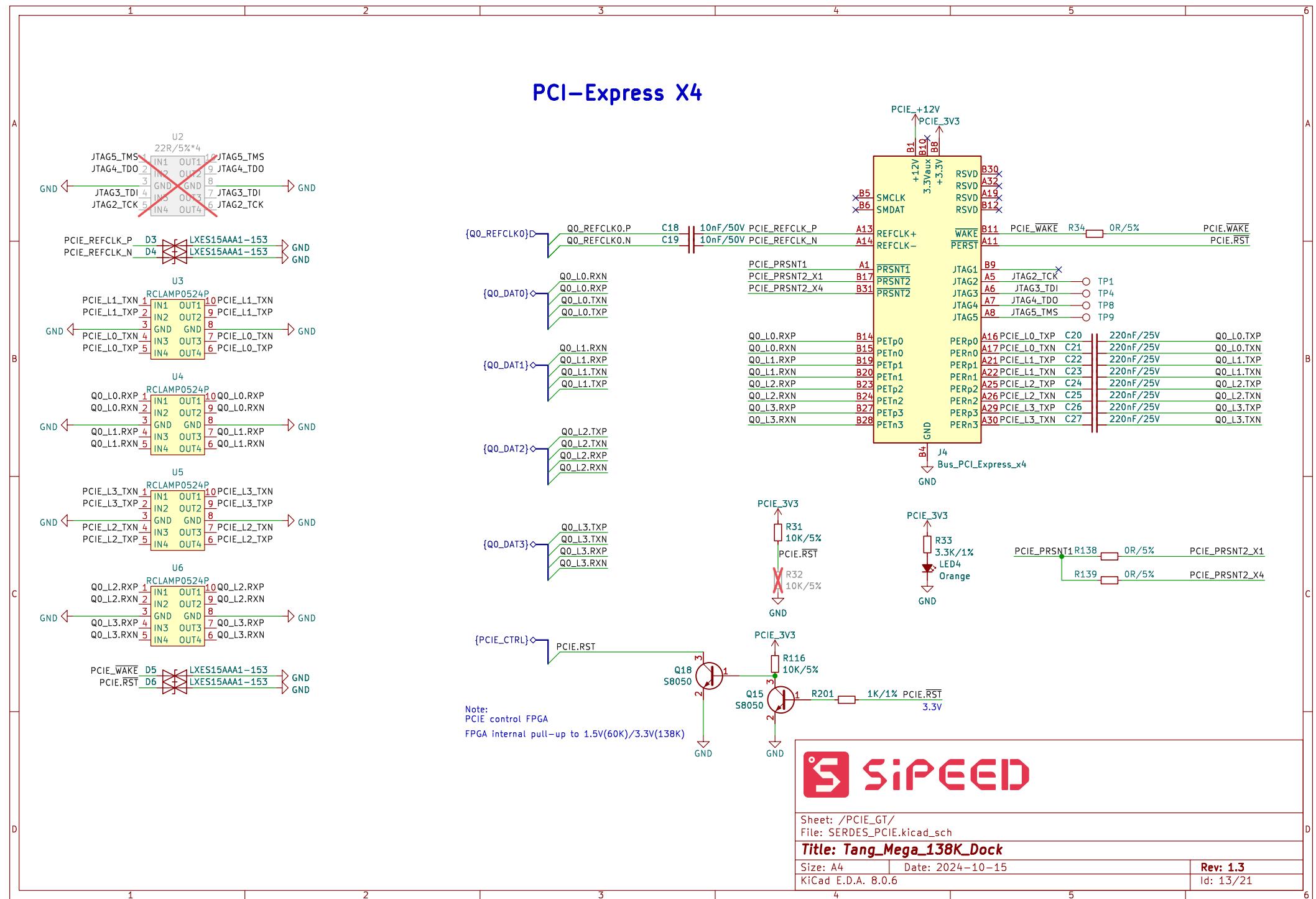
Sheet: /SYS\_DPI/  
File: LCD\_DPI.kicad\_sch

Title: Tang\_Mega\_138K\_Dock

Size: A4 Date: 2024-08-28  
KiCad E.D.A. 8.0.6

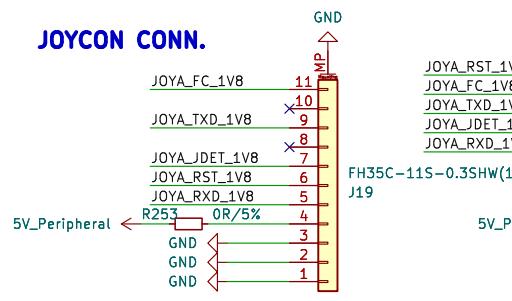
Rev: 1.2  
Id: 12/21

# PCI-Express X4



1 2 3 4 5 6

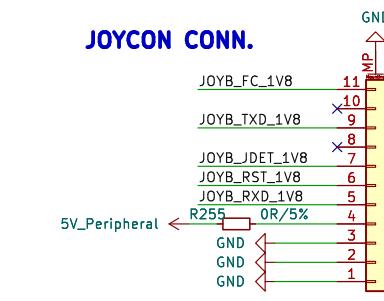
### JOYCON Conn.



JOYA\_RST\_1V8  
JOYA\_FC\_1V8  
JOYA\_TXD\_1V8  
JOYA\_JDET\_1V8  
JOYA\_RXD\_1V8  
TP3  
TP10  
TP11  
TP12  
TP13

5V\_Peripheral  
C200  
22uF/16V  
GND  
GND  
GND

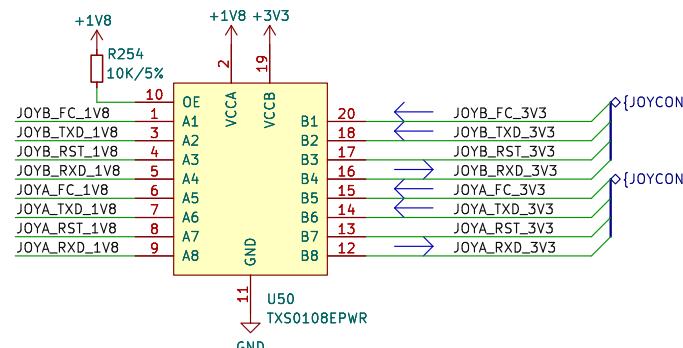
### JOYCON Conn.



JOYB\_RST\_1V8  
JOYB\_FC\_1V8  
JOYB\_TXD\_1V8  
JOYB\_JDET\_1V8  
JOYB\_RXD\_1V8  
TP2  
TP14  
TP15  
TP16  
TP17

5V\_Peripheral  
C202  
22uF/16V  
GND  
GND  
GND

### Bi-directional Voltage Translator



+1V8  
C54  
100nF/25V  
GND  
+3V3  
C92  
100nF/25V  
GND

Note:  
RST=0: Enable JOYCON  
RST=1: Disable JOYCON

JDET=1:  
HIGH when connected to console via Bluetooth.  
Joy-Con will not send serial data post-handshake unless pin is pulled LOW by console.



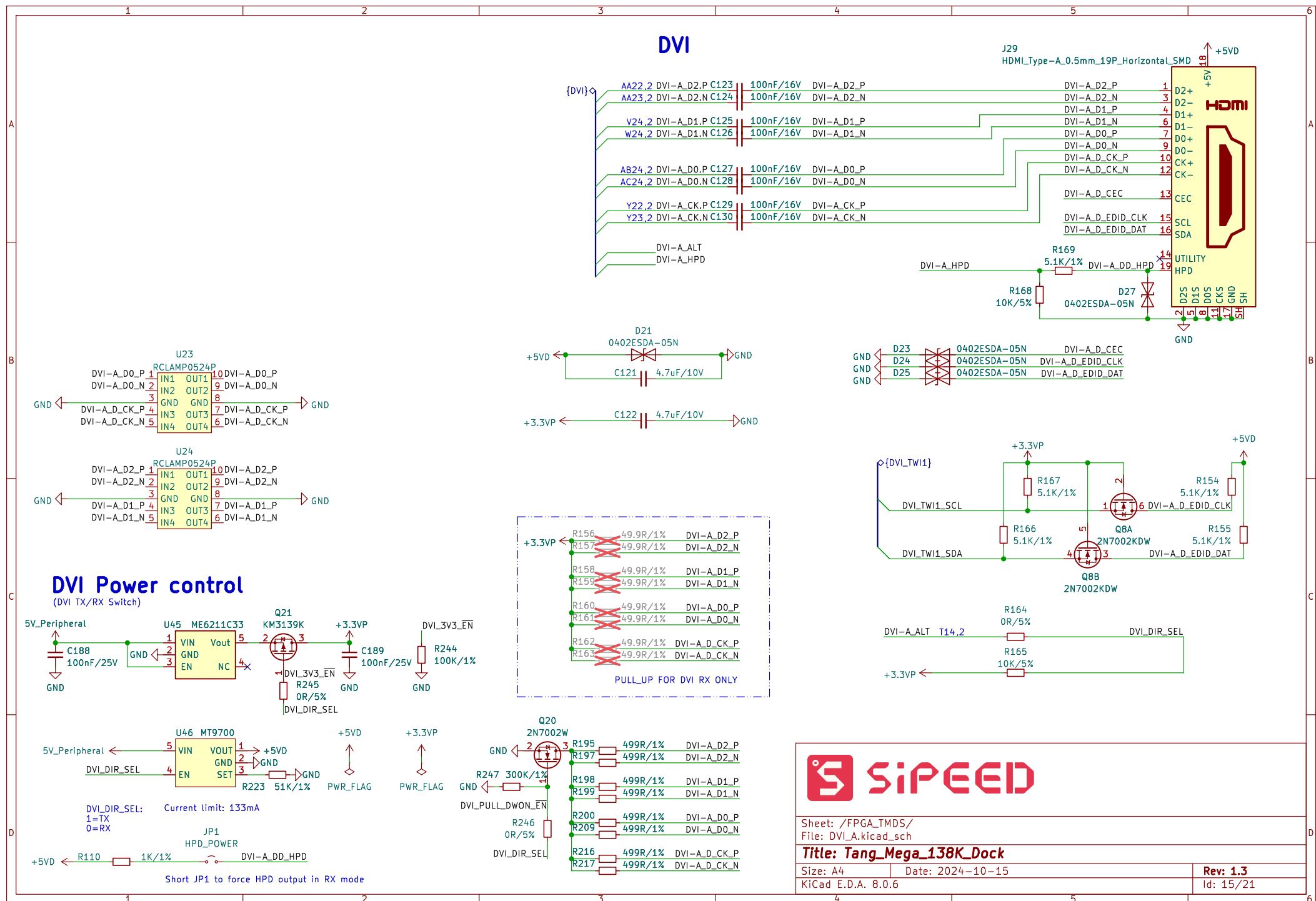
Sheet: /JOYCON/  
File: JOYCON.kicad\_sch

Title: Tang\_Mega\_138K\_Dock

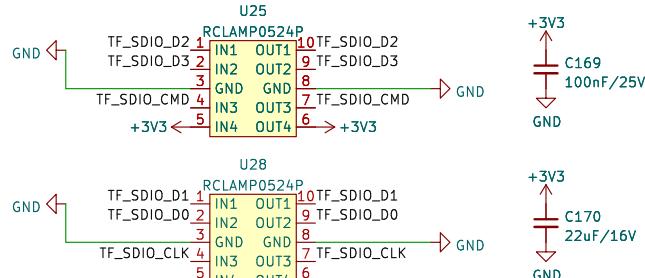
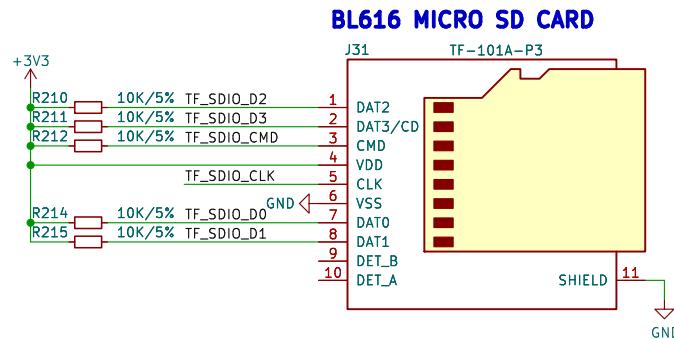
Size: A4 Date: 2024-10-15  
KiCad E.D.A. 8.0.6

Rev: 1.3  
Id: 14/21

1 2 3 4 5 6



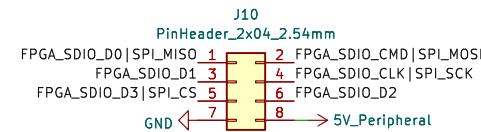
# STORAGE



EVB mode : BL616\_SPI high-Z , FPGA can work in SPI mode or SDIO mode

Game mode : BL616\_SPI Master , FPGA\_SPI Slave , FPGA\_SPI\_CS disable , FPGA\_SDIO\_D1/D2 work as SPI\_CS(input) or other function

Q1 : How to switch between EVB mode and Game mode?  
A1: Switch DBG\_ModeSel through SW2(GP Switch DIP)



Sheet: /SYS\_STORAGE/

File: SDIO&M.2.kicad\_sch

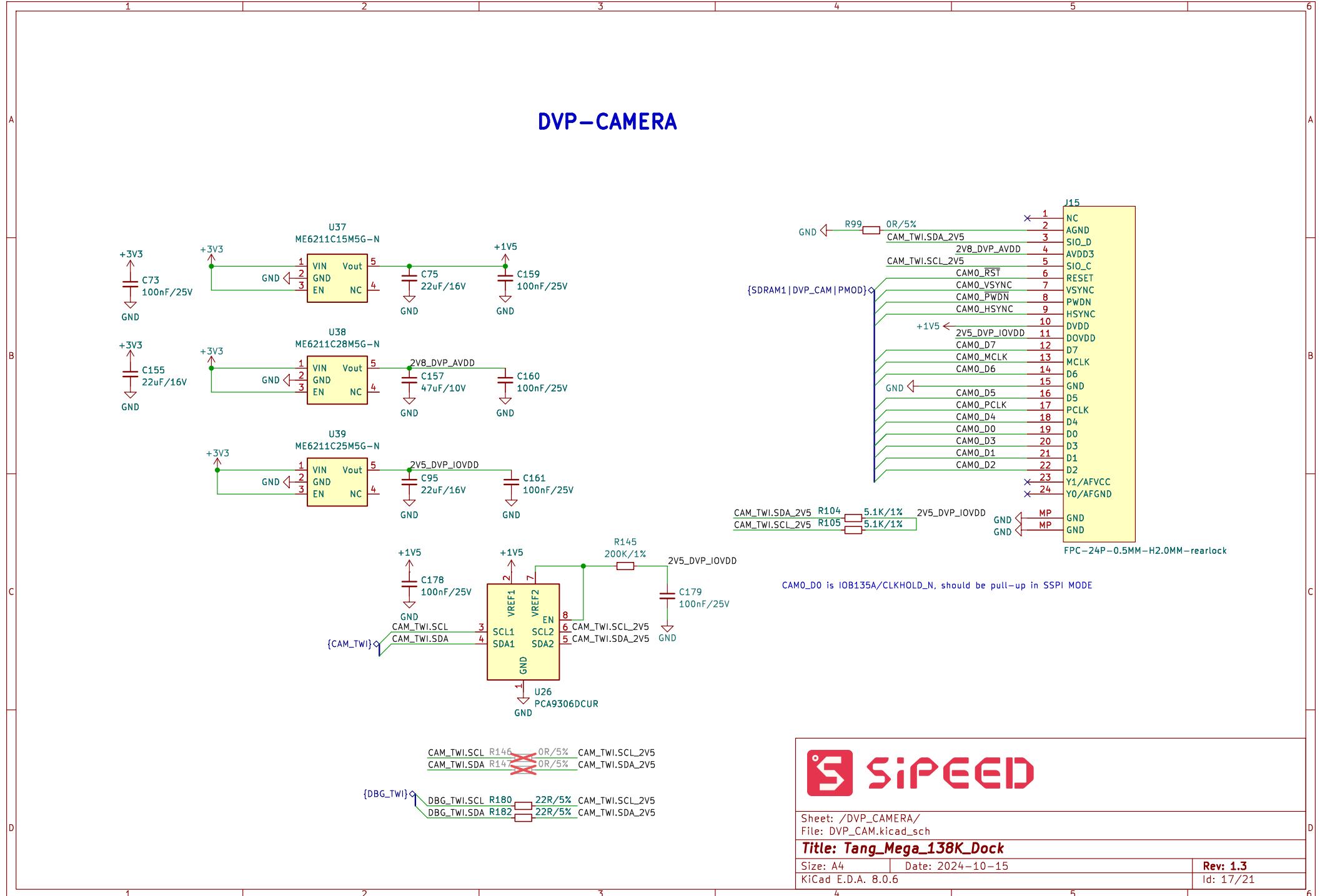
**Title: Tang\_Mega\_138K\_Dock**

Size: A4 Date: 2024-08-28

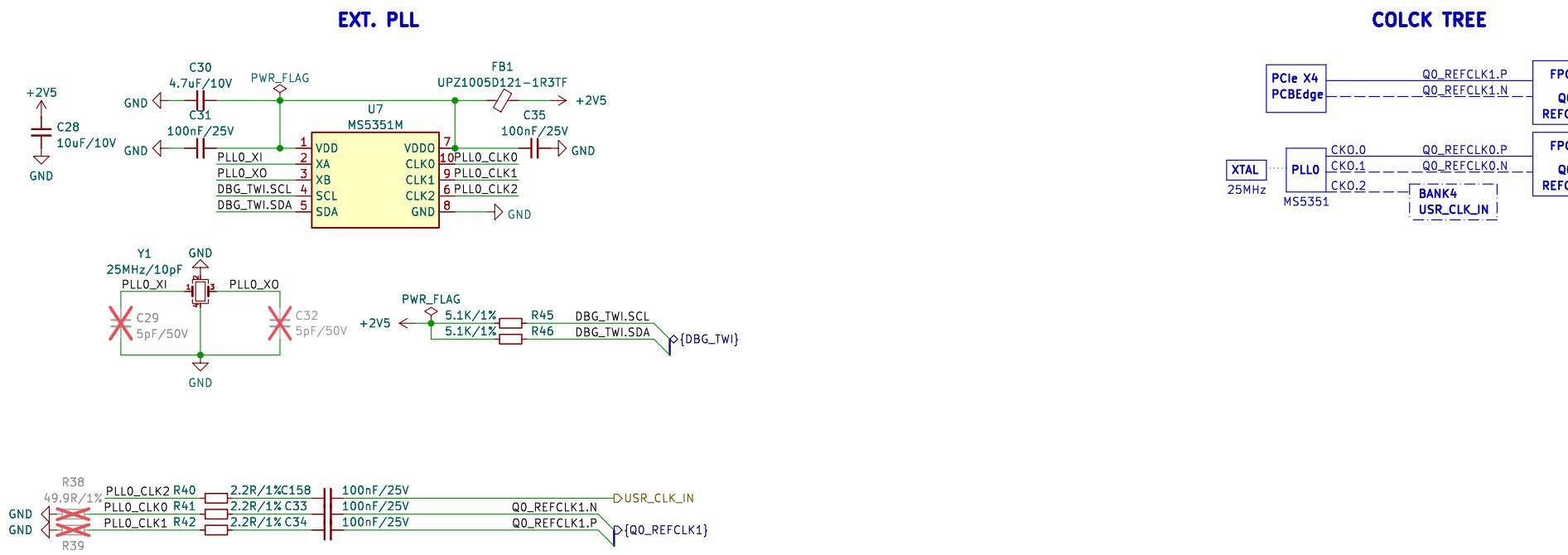
KiCad E.D.A. 8.0.6

Rev: 1.2

Id: 16/21



# CLOCK



Sheet: /SYS\_CLOCK/  
File: CLOCK.kicad\_sch

Title: Tang\_Mega\_138K\_Dock

Size: A4 Date: 2024-10-15

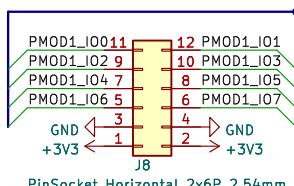
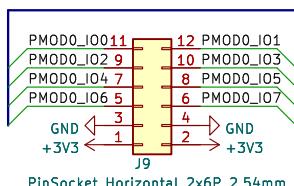
KiCad E.D.A. 8.0.6

Rev: 1.3

Id: 18/21

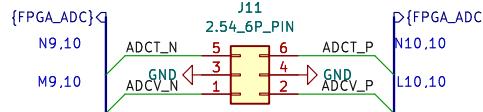
# EX CONN.

## PMOD

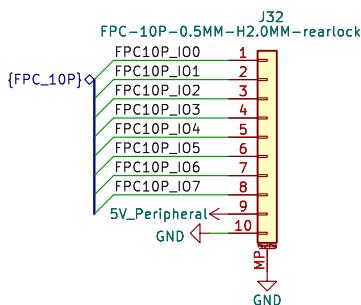


{SDRAM1 | DVP\_CAM | PMOD}

## ADC Conn.

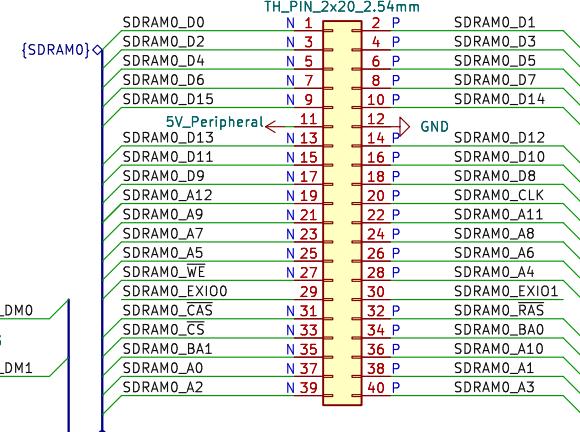


## FPC10P Conn.



# EX CONN.

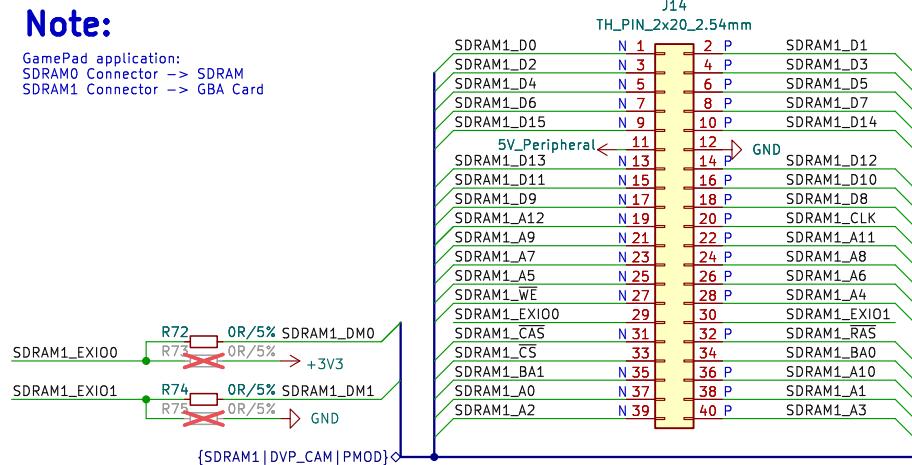
## SDRAM0 Conn. Close to PCIE connector



## Note:

GamePad application:  
SDRAM0 Connector → SDRAM  
SDRAM1 Connector → GBA Card

## SDRAM1 Conn. Close to PMOD connector



Sheet: /FPGA\_EXT\_CONN./  
File: EX\_CONN..kicad\_sch

Title: Tang\_Mega\_138K\_Dock

Size: A4 Date: 2024-10-15

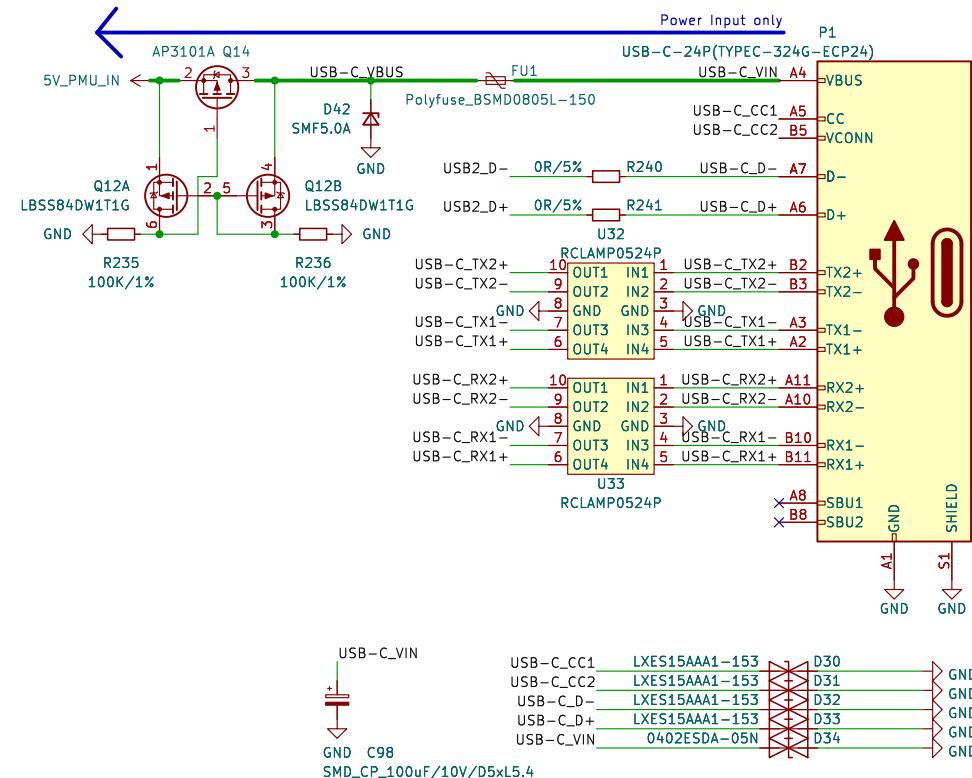
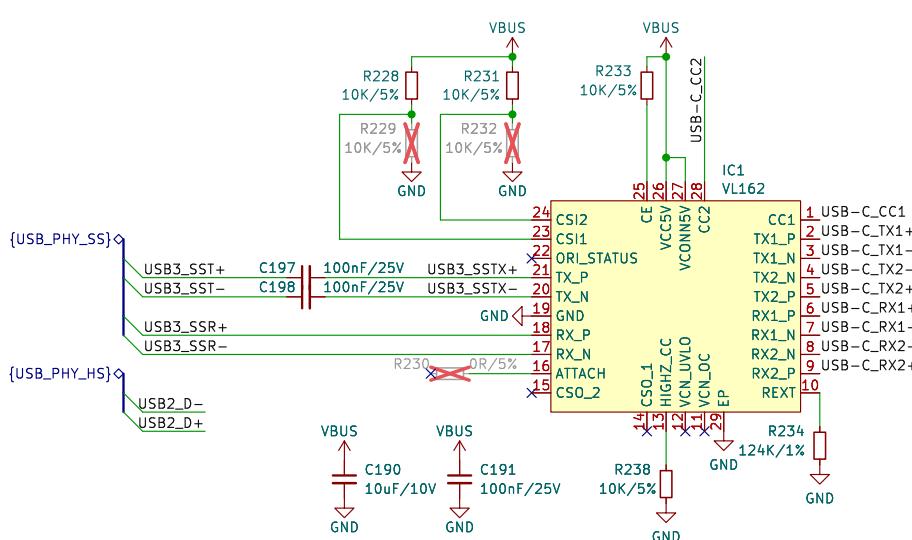
KiCad E.D.A. 8.0.6

Rev: 1.3

Id: 19/21

1 2 3 4 5 6

CH569  $\longleftrightarrow$  USB 2:1 Data Switch  $\longleftrightarrow$  CH569 USB-C Connector



Sheet: /SYS\_USB-C\_UFP/  
File: USBC\_UFP.kicad\_sch

Title: Tang\_Mega\_138K\_Dock

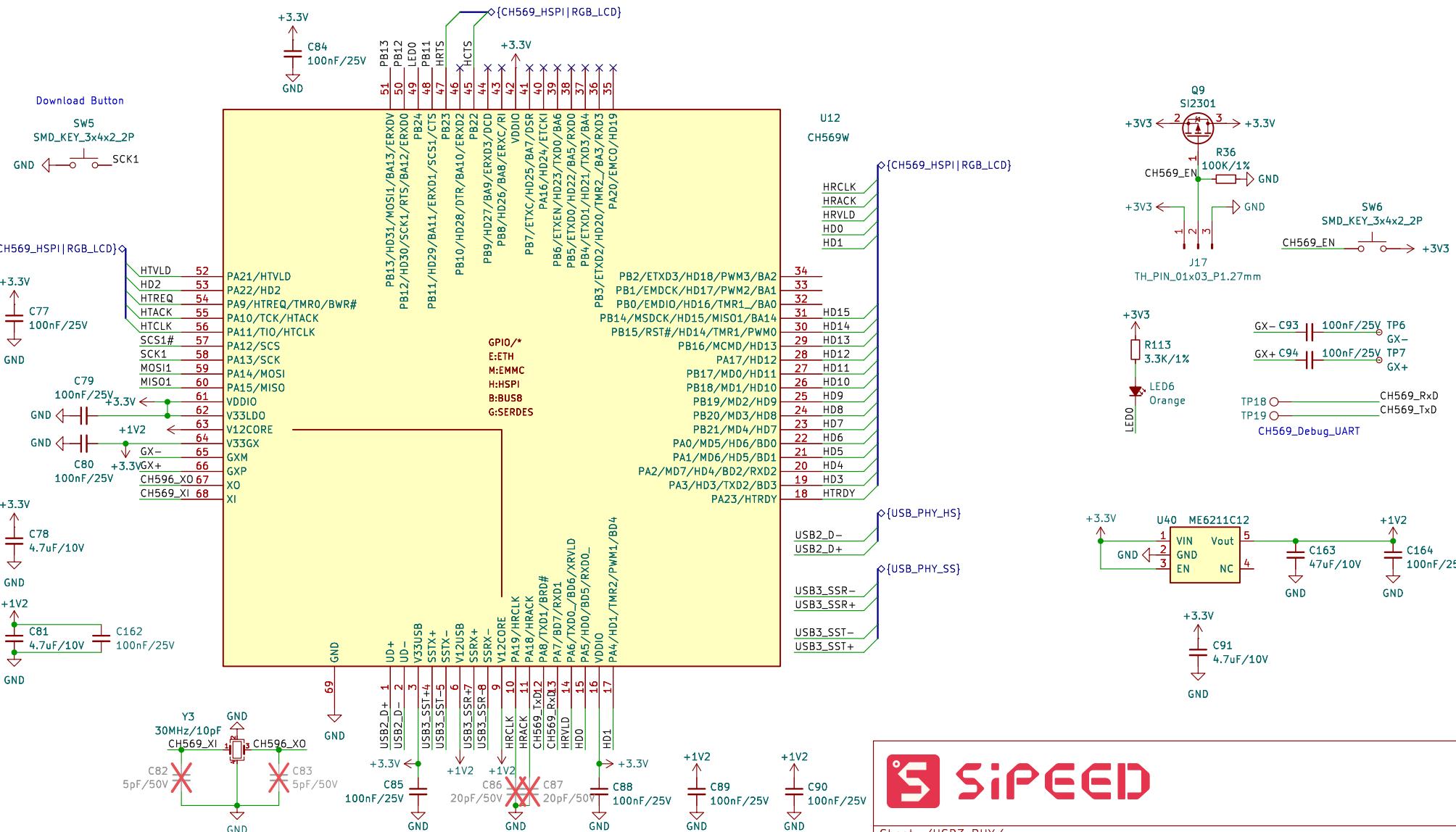
Size: A4 Date: 2024-08-28

KiCad E.D.A. 8.0.6

Rev: 1.2  
Id: 20/21

1 2 3 4 5 6

# USB3-PHY



 **SiPEED**

Sheet: /USB3\_PHY/  
File: USB3\_PHY.kicad\_sch  
**Title: Tang\_Mega\_138K\_Dock**  
Size: A4 Date: 2024-08-28  
KiCad E.D.A. 8.0.6 Rev: 1.2  
Id: 21/21