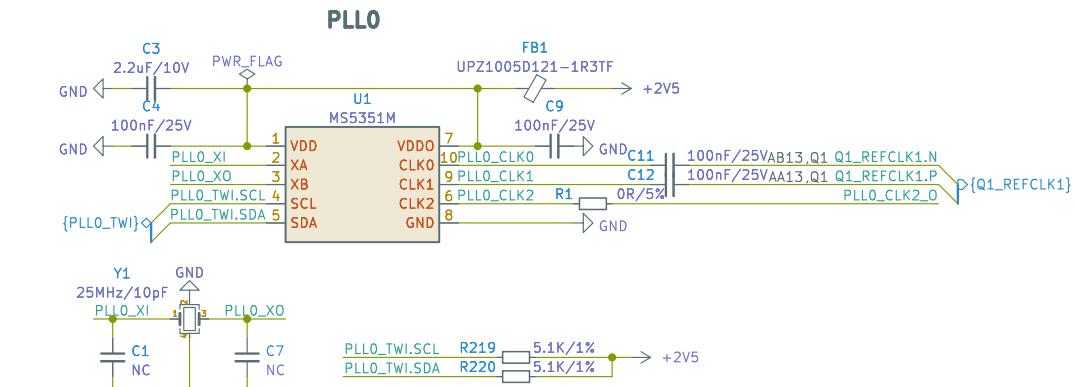


# CLOCK

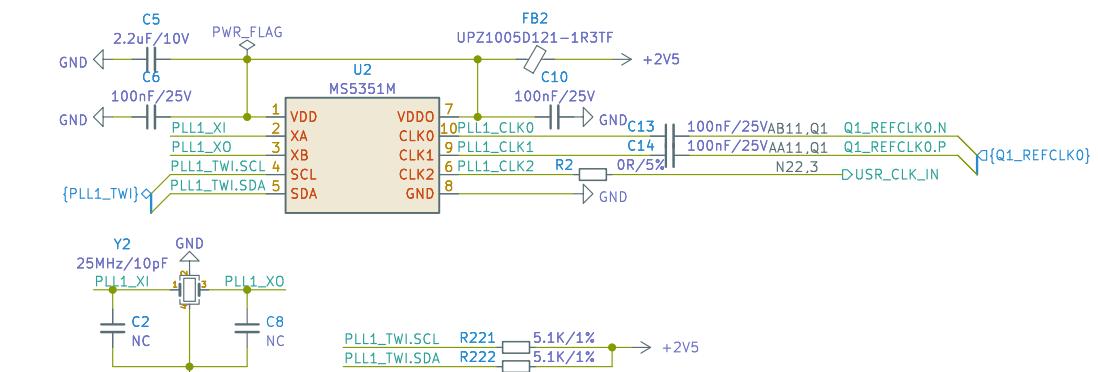
## EXT. PLL



TWI\_MUX\_CFG: SEL[0..2]=0,1,1

{N19,3}: SEL0=0  
{P19,3}: SEL1=1  
{P26,3}: SEL2=1

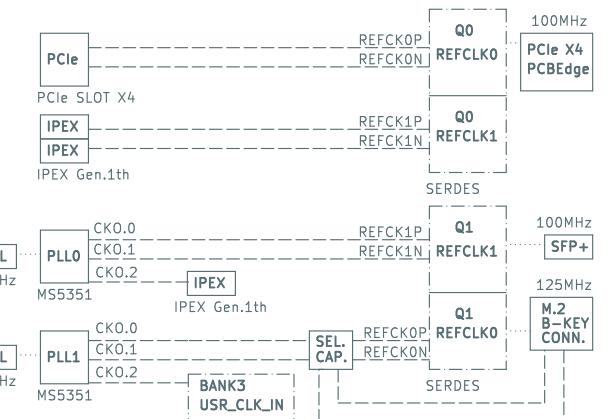
## PLL1



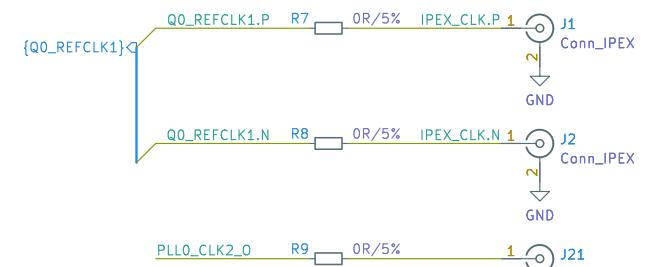
TWI\_MUX\_CFG: SEL[0..2]=1,0,0

{N19,3}: SEL0=1  
{P19,3}: SEL1=0  
{P26,3}: SEL2=0

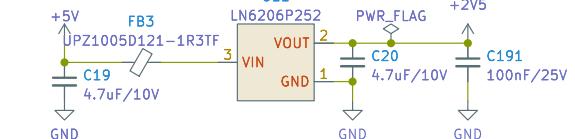
## CLOCK TREE



## IPEX RF CONN.



## EXT. PLL POWER



Update notes: Fixed the issues of clock tree.

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Sheet: /FPGA\_CLOCK/  
File: CLOCK.kicad\_sch

Title: TANG\_MEGA-138K-Pro\_Dock-4071f\_Schematics

Size: A4 Date: 2024-10-10  
KiCad E.D.A. 8.0.5

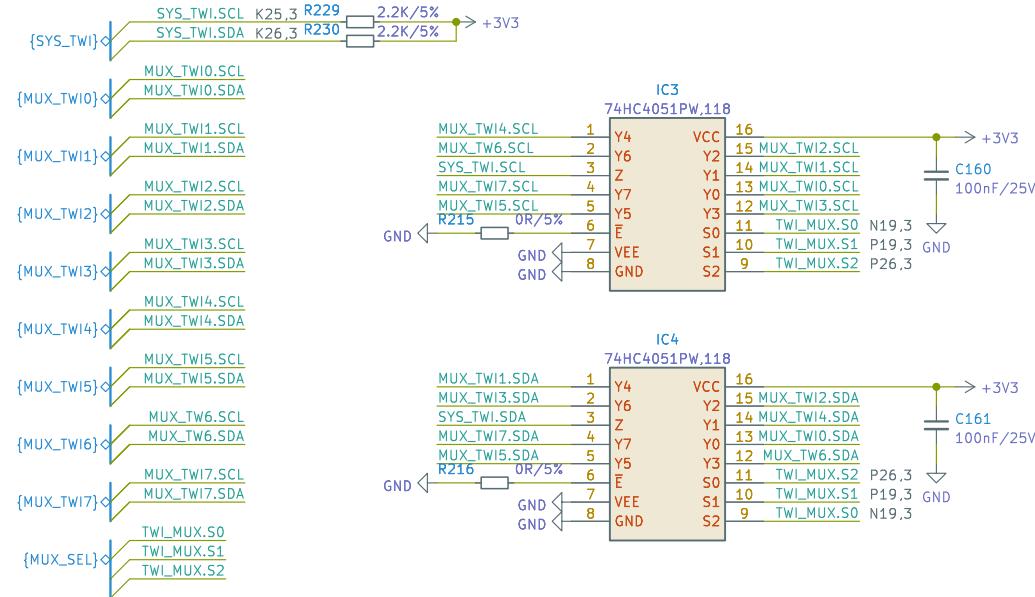
Rev: 1.2  
Id: 3/19

1 2 3 4 5 6

A

A

## 8-WAY TWI MUX



NO.	CONFIG	SEL0	SEL1	SEL2
0	SFPO	0	0	0
1	SFP1	0	0	1
2	EEPROM	0	1	0
3	DVI_A_DDC MS5331-0	0	1	1
4	DVI_B_DDC MS5331-1	1	0	0
5	DVP_CAM	1	0	1
6	MIPI_RX0	1	1	0
7	MIPI_RX1	1	1	1



Update notes: Rename the DVI\_TX\_DDC to DVI\_A\_DDC, DVI\_RX\_DDC to DVI\_B\_DDC.  
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Sheet: /TWI\_MUX/  
File: TWI\_MUX.kicad\_sch

**Title: TANG\_MEGA-138K-Pro\_Dock-4071f\_Schematics**

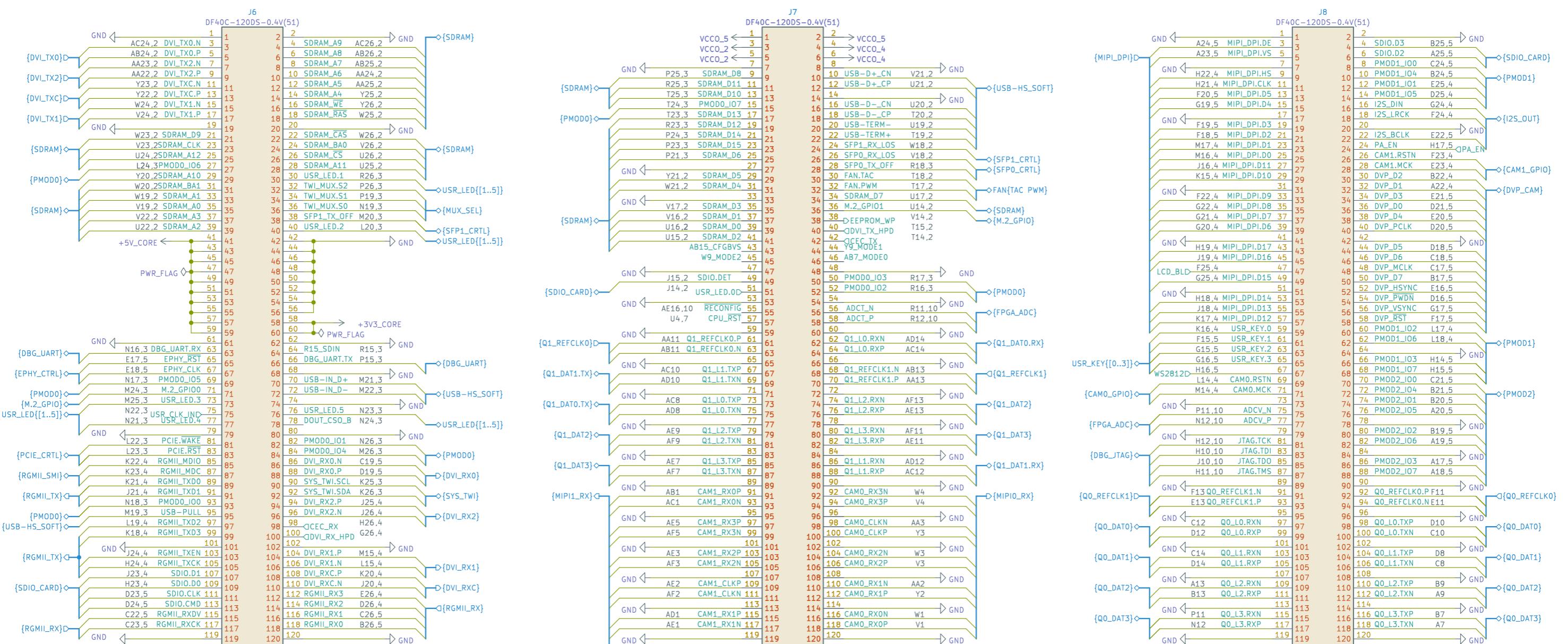
Size: A4 Date: 2024-10-10  
KiCad E.D.A. 8.0.5

Rev: 1.2  
Id: 4/19

1 2 3 4 5 6

# FPGA CORE MODULE

Note: that the pinout (numbers) of these conn. here is mirrored compared to the SOM.



## TEST POINT

TP24 R15\_SDIN  
R15\_SDIN

TP25 DOUT\_CSO\_B  
DOUT\_CSO\_B

TP12  $\Rightarrow$  +3V3\_CORE  
DOUT\_CSO\_B

+5V\_CORE  
C136  
220uF/25V

## MODE SET



NOTE: MODE[0..2] is set to 001 by default on CM Board  
Set CFGBVS to 1 to enable maximum driving of the pin during FPGA configuration

CONFIG	MODE0	MODE1	MODE2
JTAG	X	X	X
MSPI	0	0	1
SSPI	0	1	0
MSERIAL	0	0	0
S SERIAL	1	1	1
MCPU	1	0	0
SCPU	1	1	0



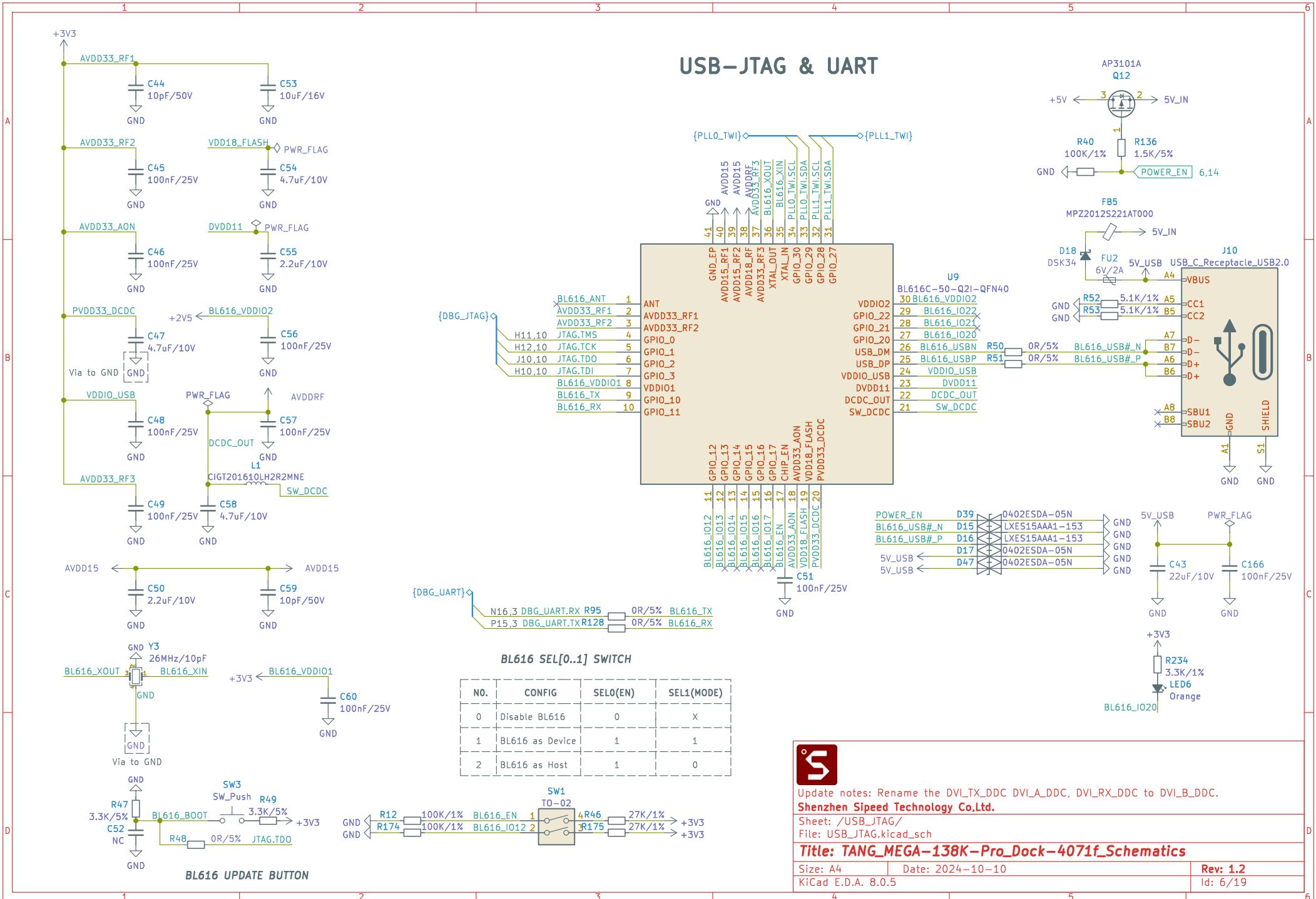
Update notes: Rename the DVI\_TX\_DDC DVI\_A\_DDC, DVI\_RX\_DDC to DVI\_B\_DDC.  
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Sheet: /FPGA\_BTB/  
File: CONN\_BTB.kicad\_sch

Title: TANG\_MEGA-138K-Pro\_Dock-4071f\_Schematics

Size: A3 Date: 2024-10-10  
KiCad E.D.A. 8.0.5

Rev: 1.2  
Id: 5/19



# PCI-Express X4

A

B

C

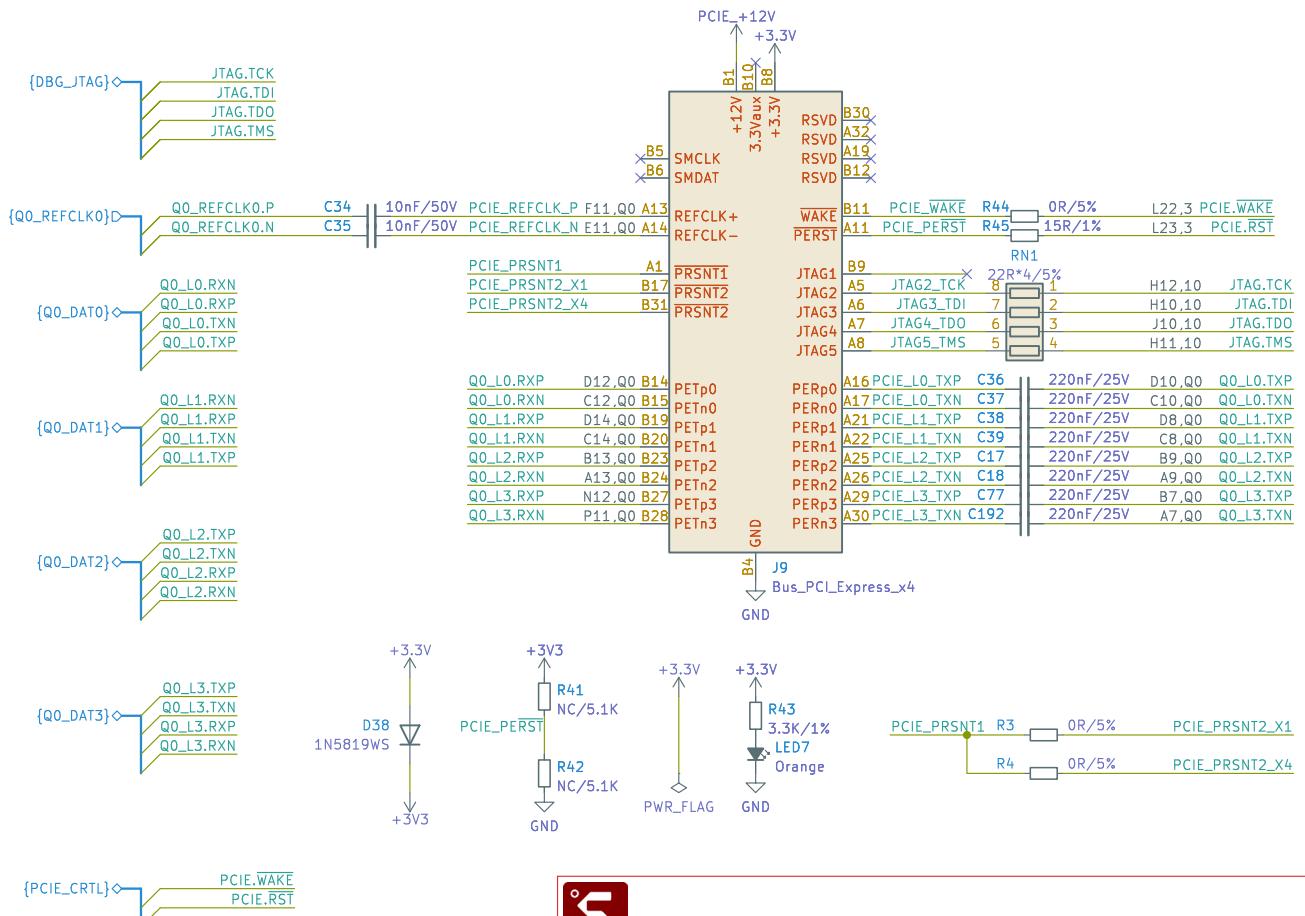
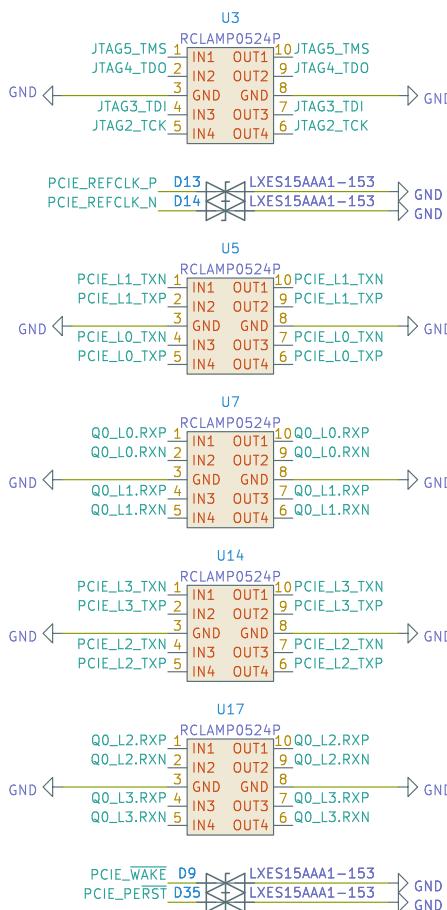
D

A

B

C

D



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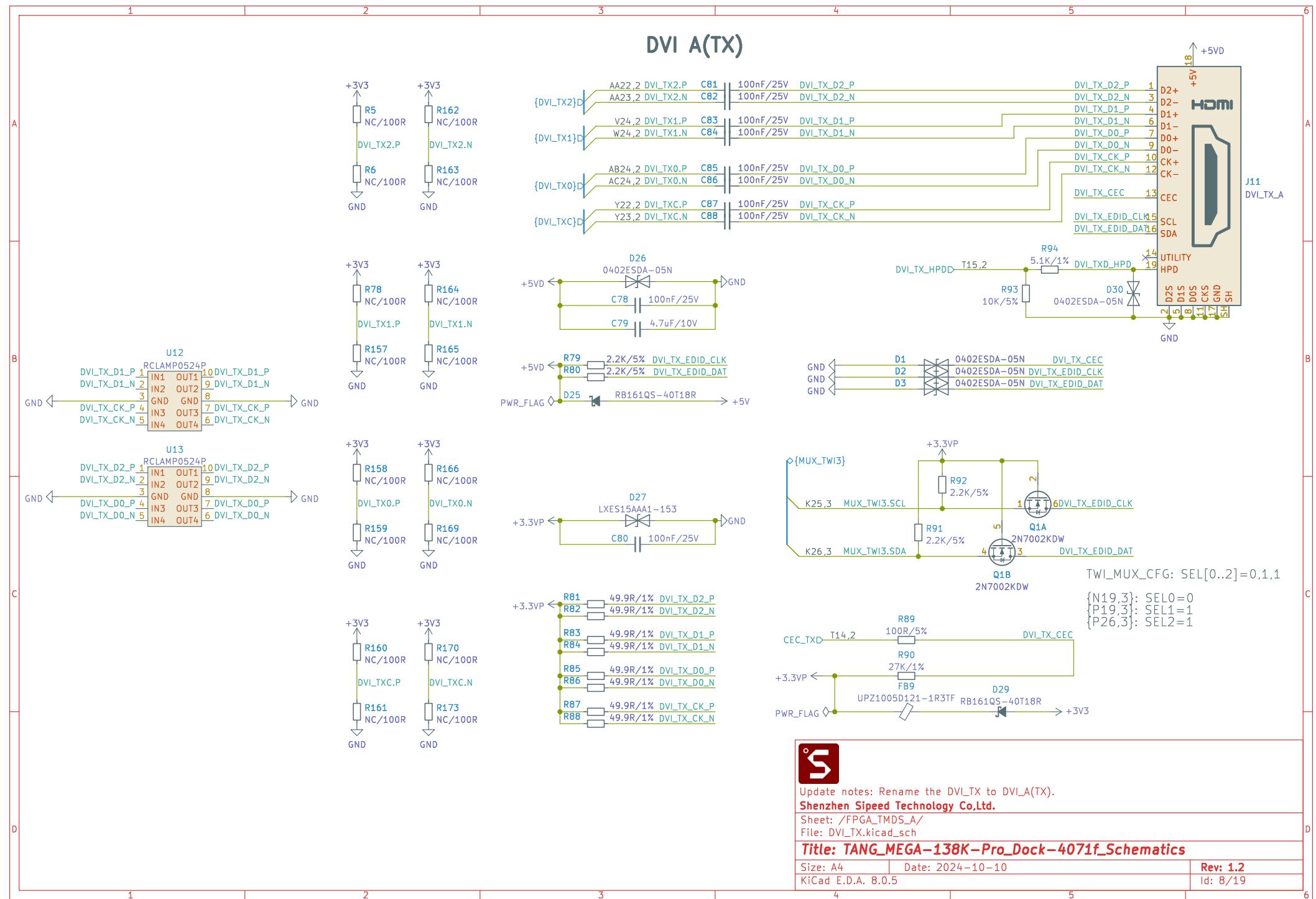
Sheet: /FPGA\_PCIE/  
File: PCIe\_sch.kicad\_sch

**Title: TANG\_MEGA-138K-Pro\_Dock-4071f\_Schematics**

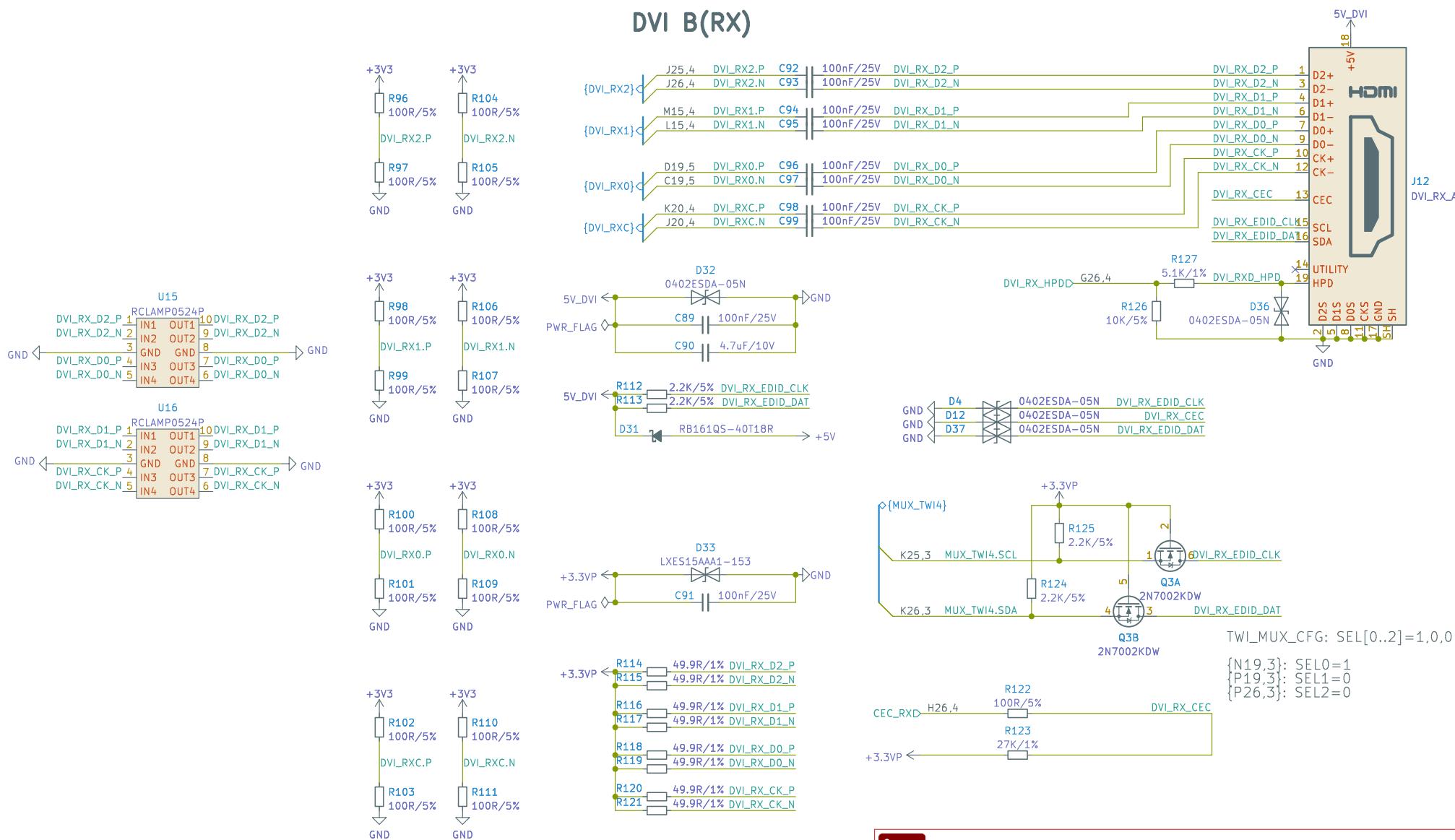
Size: A4 Date: 2024-10-10  
KiCad E.D.A. 8.0.5

Rev: 1.2  
Id: 7/19

# DVI A(TX)



# DVI B(RX)



Update notes: Rename the DVI\_RX to DVI\_B(RX)  
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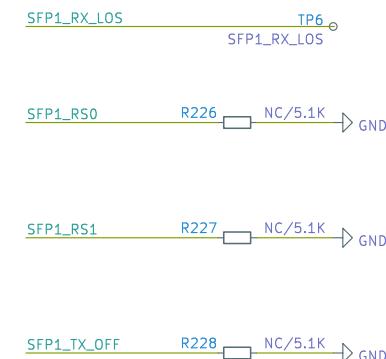
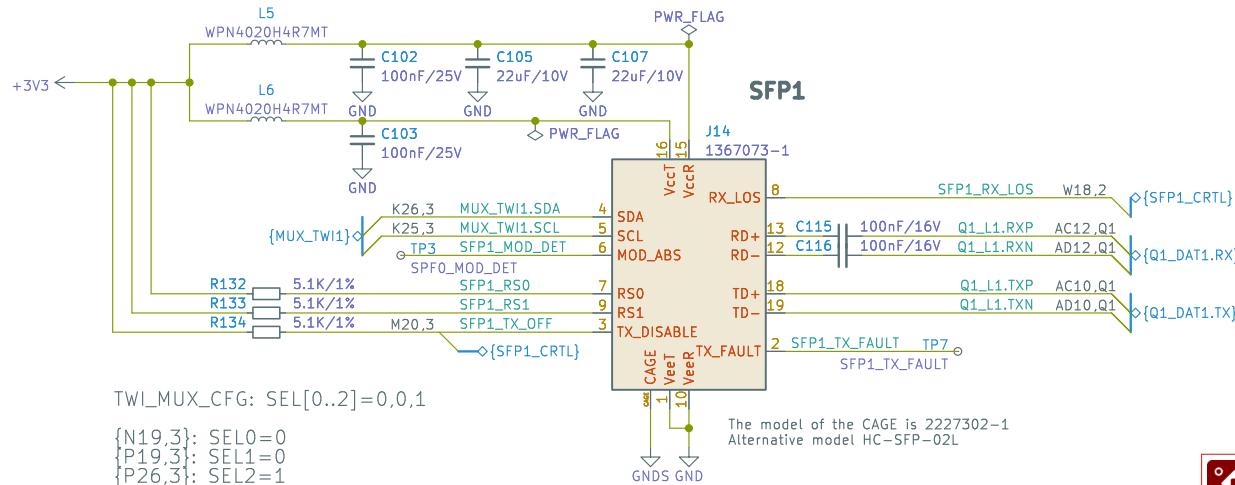
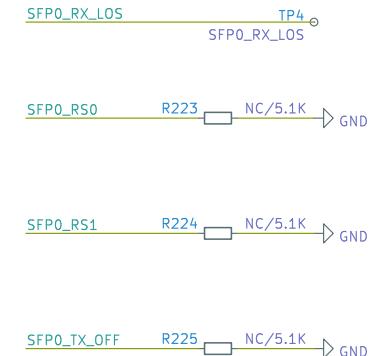
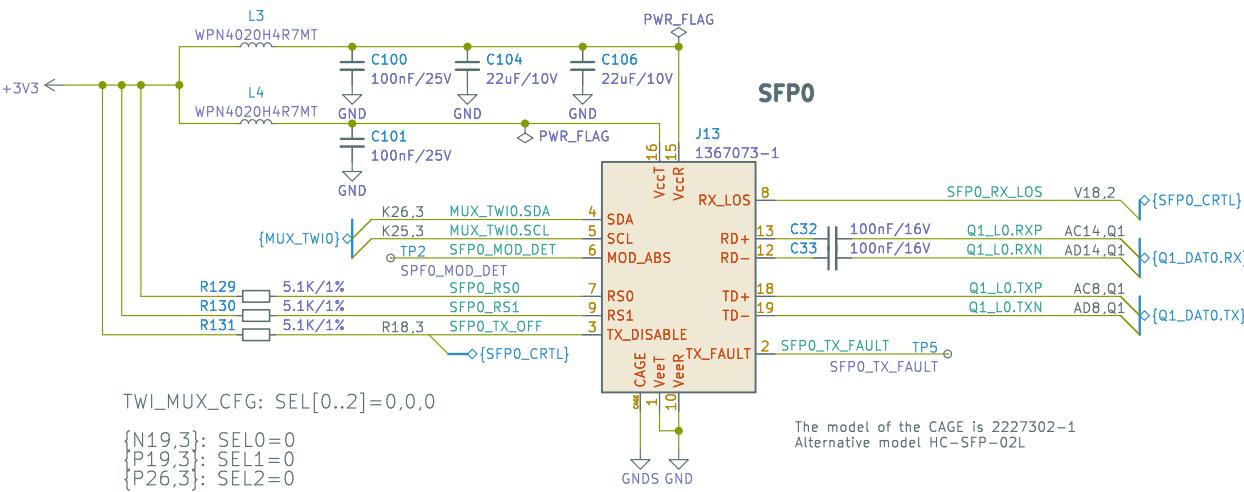
Sheet: /FPGA\_TMDs\_B/  
File: DVI\_RX.kicad\_sch

Title: TANG\_MEGA-138K-Pro\_Dock-4071f\_Schematics

Size: A4 Date: 2024-10-10  
KiCad E.D.A. 8.0.5

Rev: 1.2  
Id: 9/19

# SFP+



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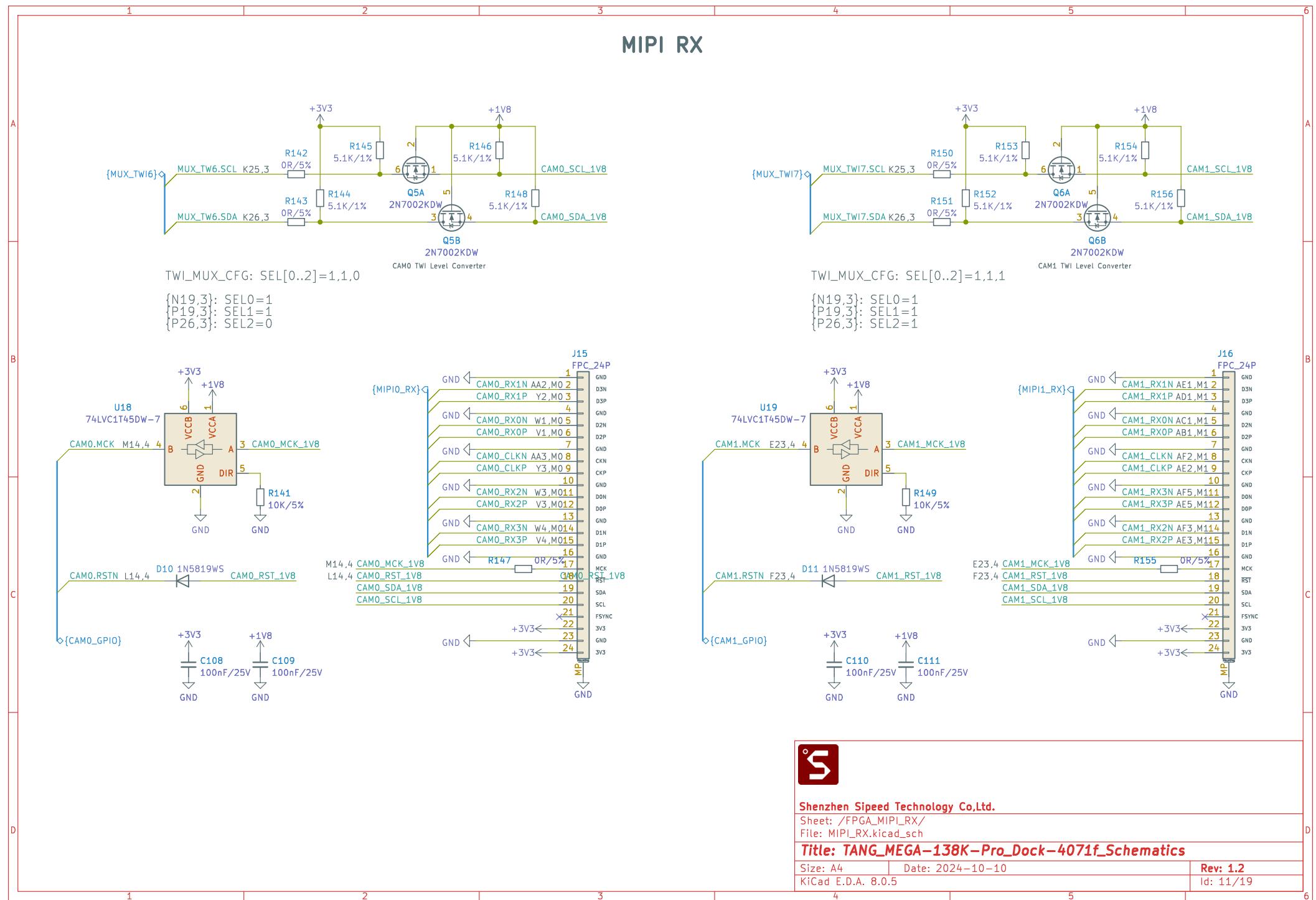
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File: SFP-PLUS.kicad\_sch

Title: TANG\_MEGA-138K-Pro\_Dock-4071f\_Schematics

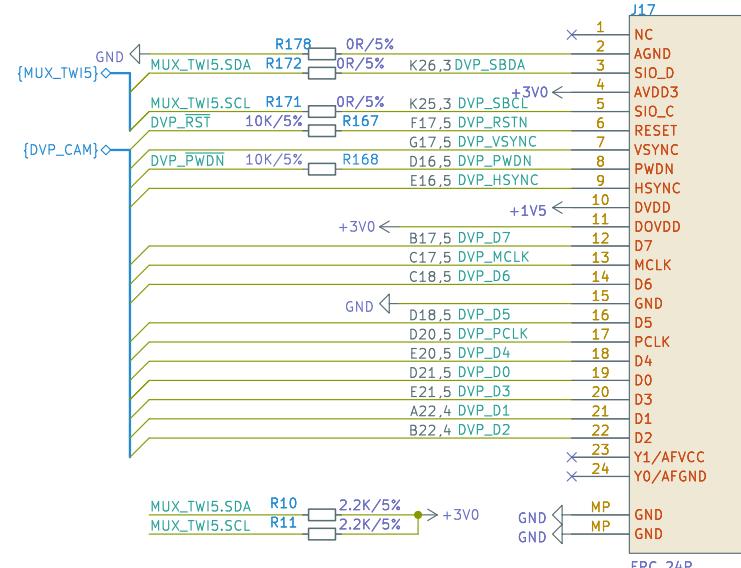
Size: A4 Date: 2024-10-10  
KiCad E.D.A. 8.0.5

Rev: 1.2  
Id: 10/19

# MIPI RX

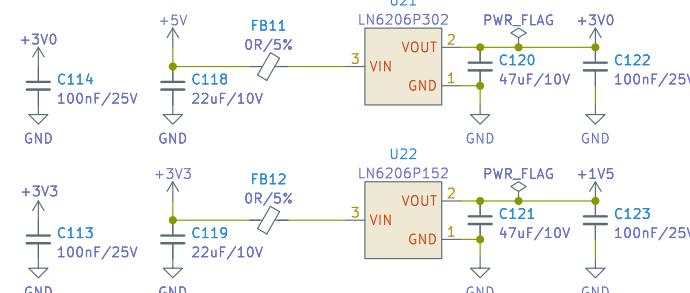


## DVP-CAMERA



TWI\_MUX\_CFG: SEL[0..2]=1,0,1

{N19,3}: SEL0=1  
{P19,3}: SEL1=0  
{P26,3}: SEL2=1



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Sheet: /DVP\_CAMERA/

File: DVP.kicad\_sch

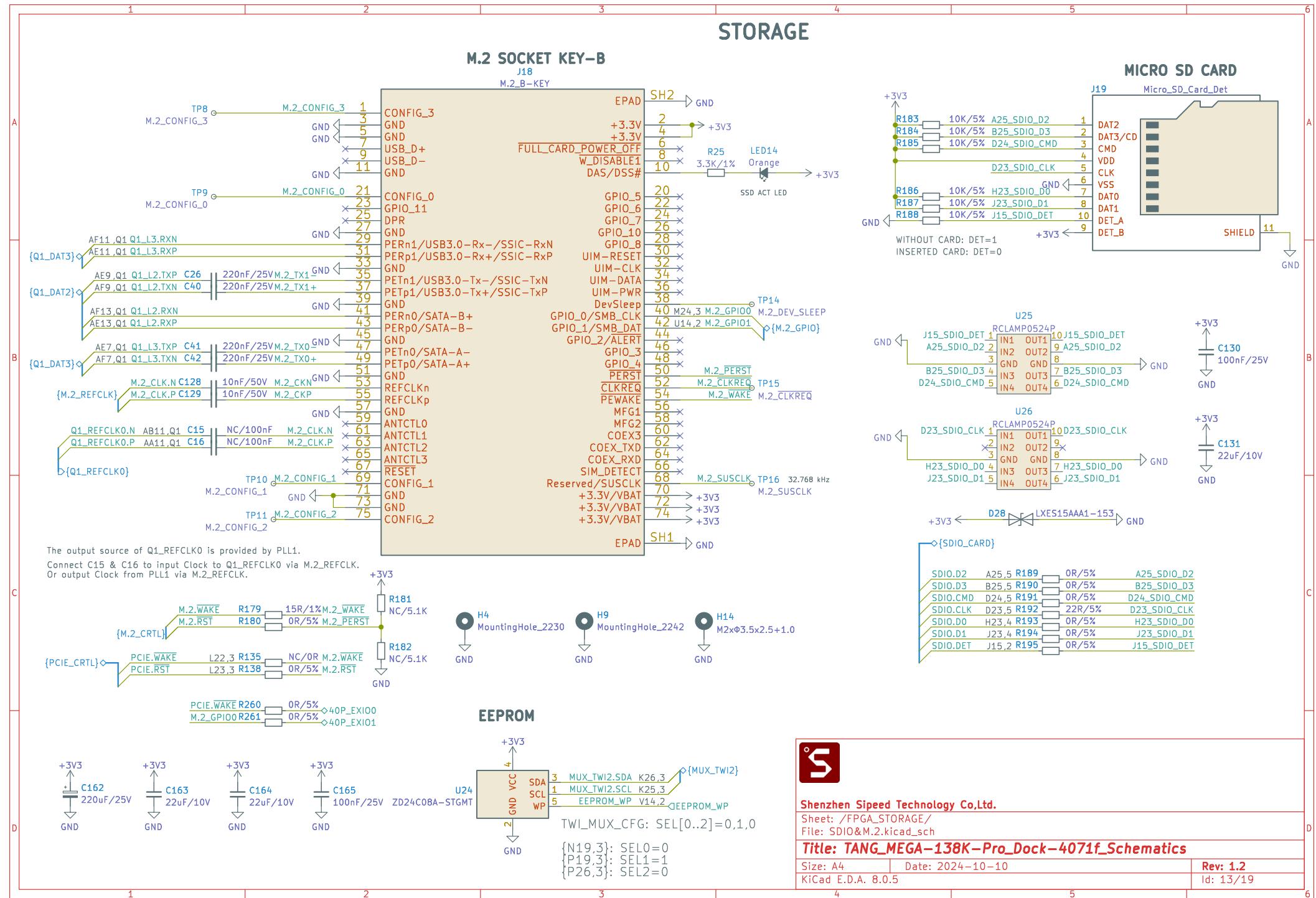
**Title: TANG\_MEGA-138K-Pro\_Dock-4071f\_Schematics**

Size: A4 Date: 2024-10-10

KiCad E.D.A. 8.0.5

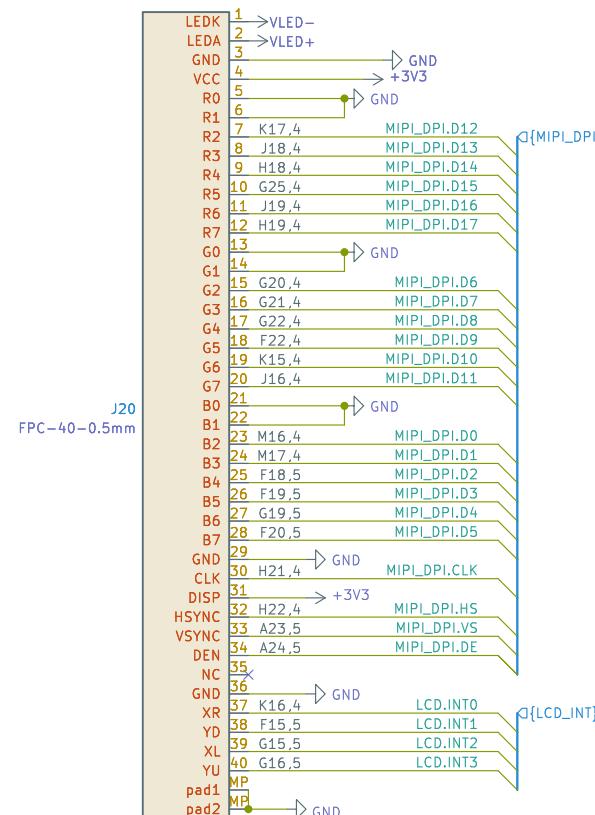
Rev: 1.2

Id: 12/19

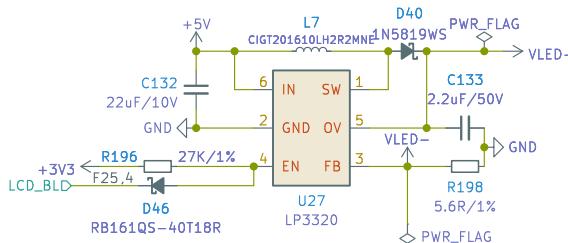


# FPGA-LCD

## MIPI DPI CONN.



## LCD BACKLIGHT



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Sheet: /FPGA\_LCD/  
File: LCD\_DPI.kicad\_sch

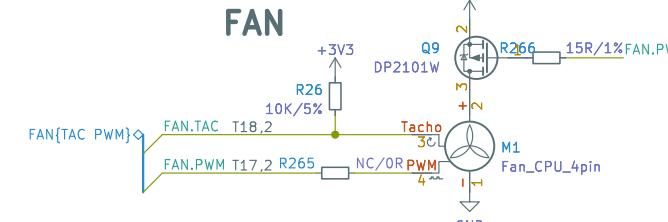
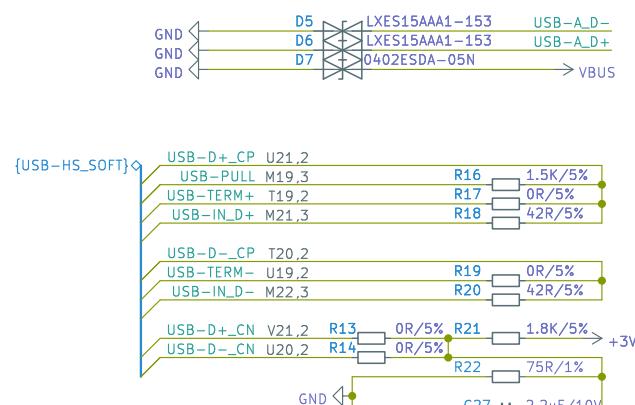
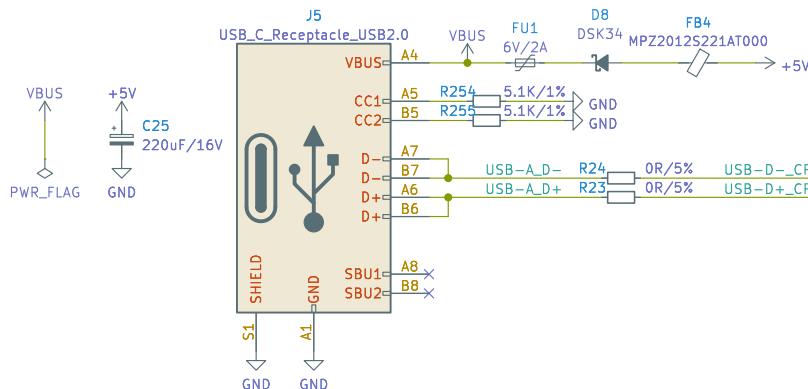
Title: TANG\_MEGA-138K-Pro\_Dock-4071f\_Schematics

Size: A4 Date: 2024-10-10  
KiCad E.D.A. 8.0.5

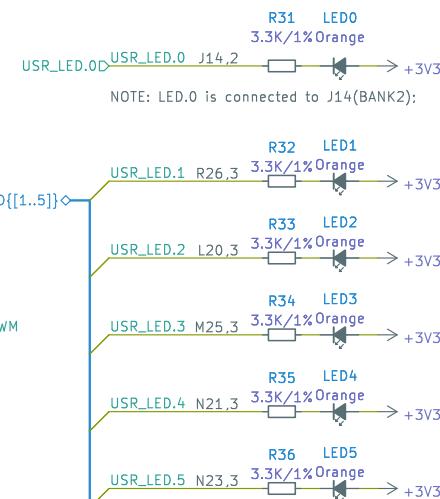
Rev: 1.2  
Id: 14/19

## PERIPHERALS

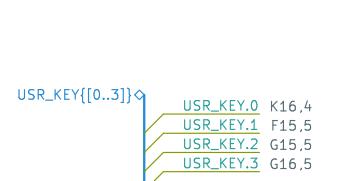
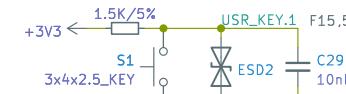
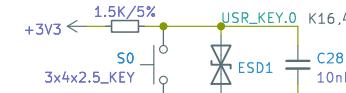
USB2.0-DEV.



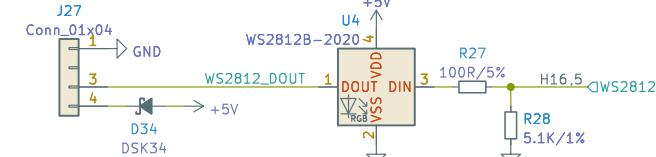
LED



## **BUTTON**



WS2812



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Sheet: /PERIPHERALS/  
File: PERIPHERALS.kicad\_sch

Title: TANG\_MEGA-138K-Pro\_Dock-4071f\_Schematics

Size: A4 Date: 2024-10-10

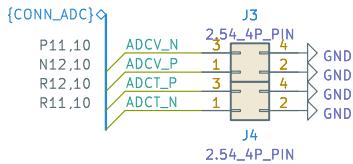
KiCad E.D.A. 8.0

Rev: 1.2

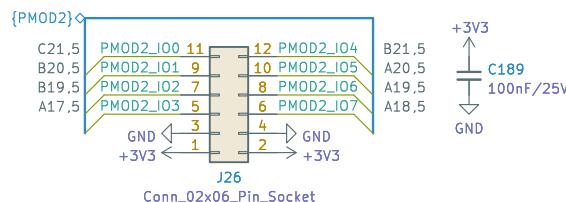
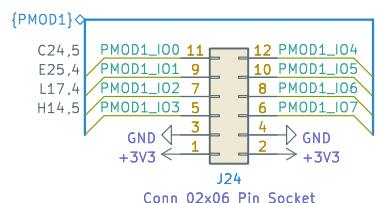
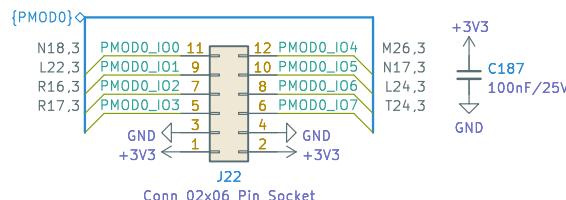
Id: 15/19

# EX CONN.

## ADC CONN.



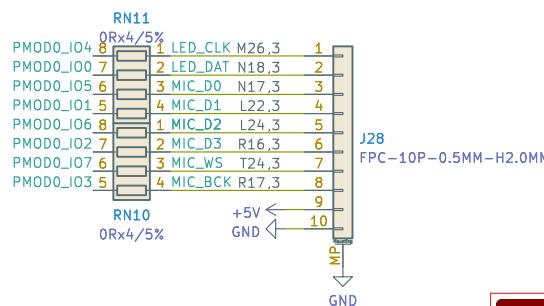
## PMOD



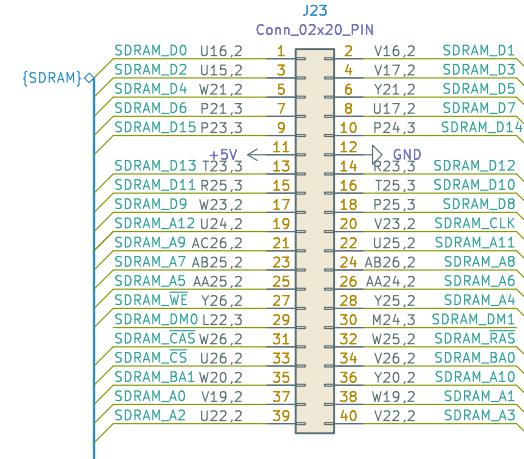
## SSPI

PIN	FUCTION	PMODO
N18	SSPI_SO	I00
R16	SSPI_CLK	I02
R17	SSPI_WP	I03
N17	SSPI_SI	I05
L24	SSPI_CS	I06
T24	SSPI_HOLD	I07

## MIC-ARRAY CONN.



## SDRAM CONN.



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Sheet: /FPGA\_EXT\_CONN./

File: EX\_CONN\_.kicad\_sch

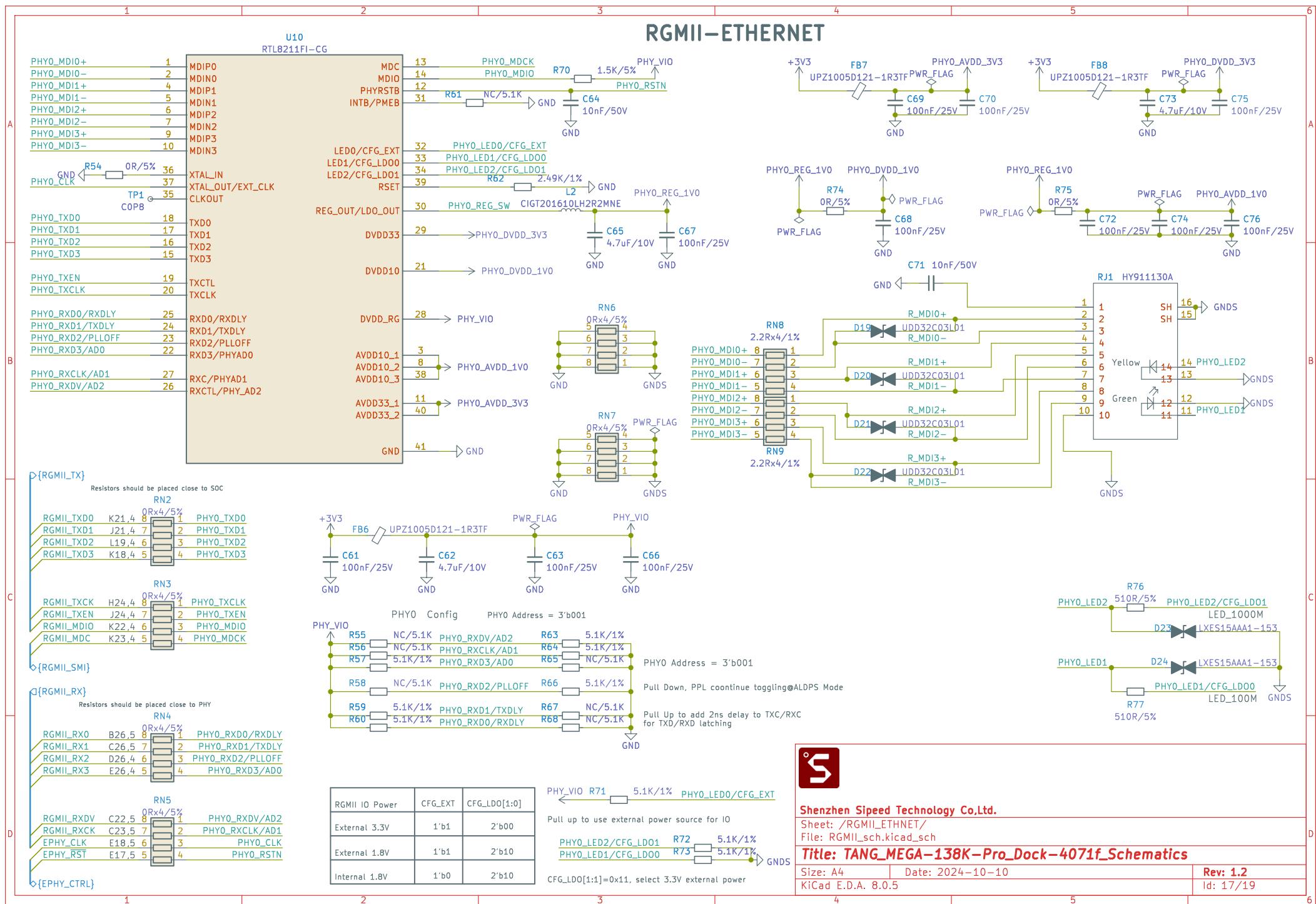
Title: TANG\_MEGA-138K-Pro\_Dock-4071f\_Schematics

Size: A4 Date: 2024-10-10

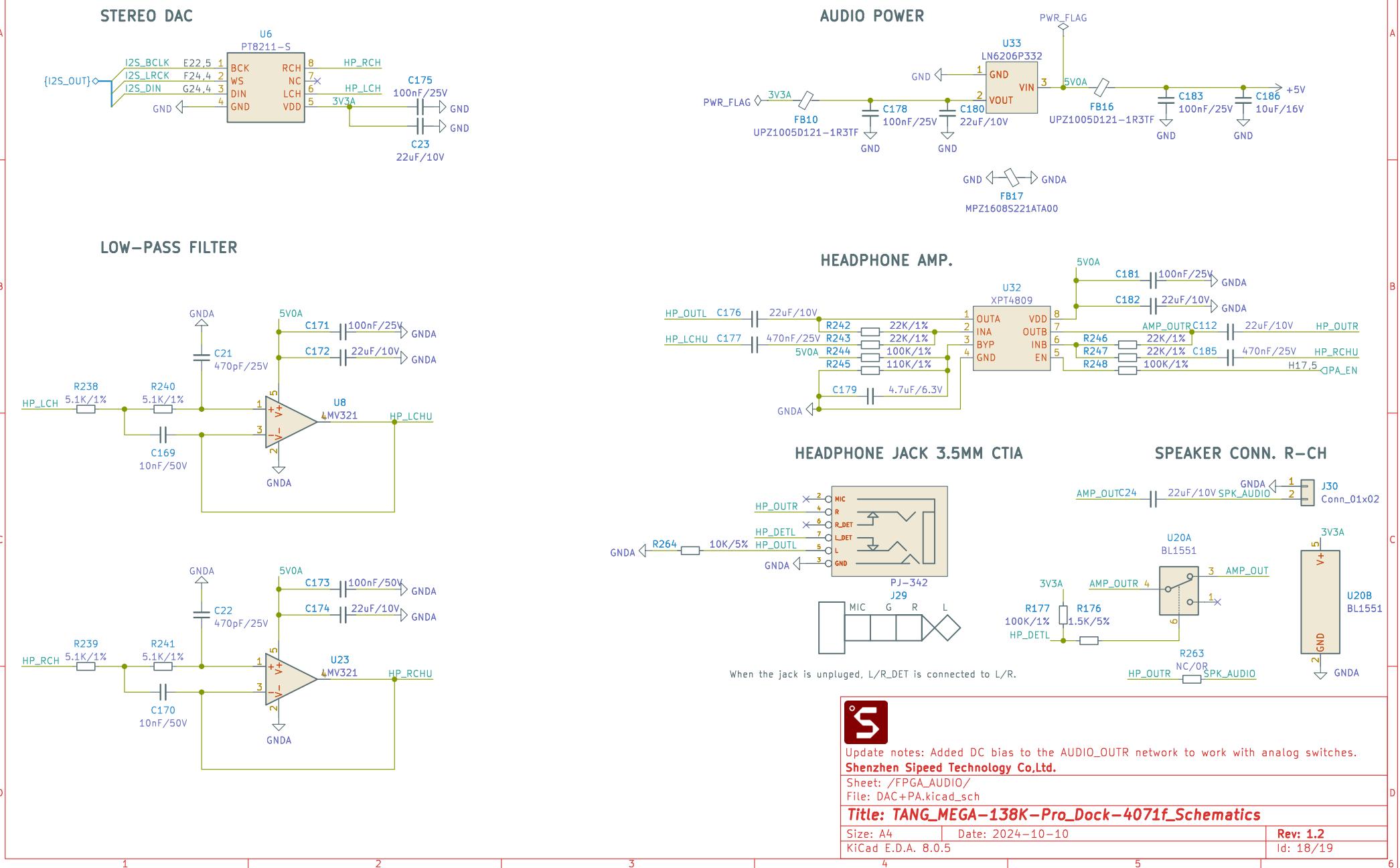
KiCad E.D.A. 8.0.5

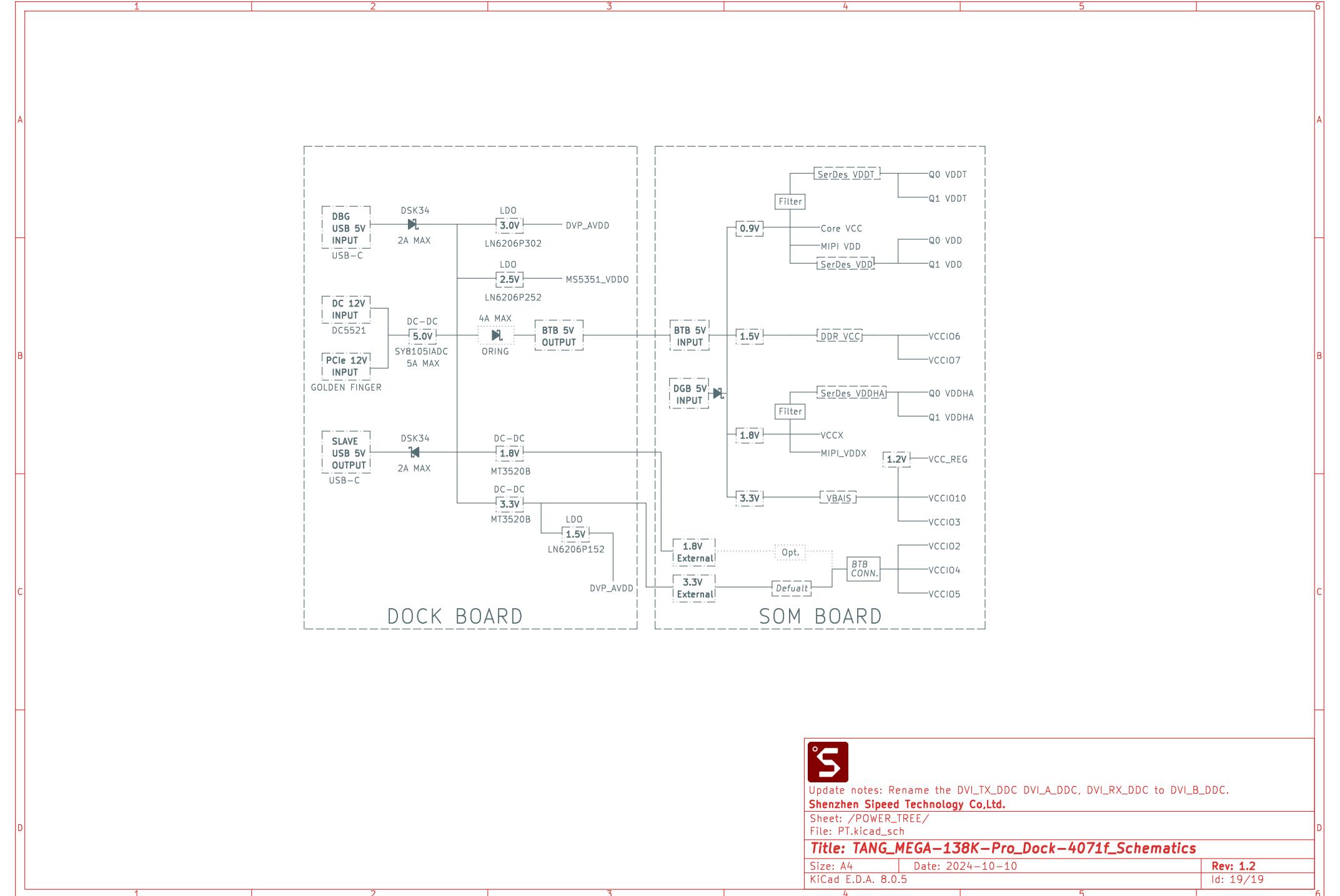
Rev: 1.2

Id: 16/19



# FPGA-Audio





Update notes: Rename the DVI\_TX\_DDC DVI\_A\_DDC, DVI\_RX\_DDC to DVI\_B\_DDC.  
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Sheet: /POWER\_TREE/  
File: PT.kicad\_sch

**Title: TANG\_MEGA-138K-Pro\_Dock-4071f\_Schematics**

Size: A4 Date: 2024-10-10  
KiCad E.D.A. 8.0.5

Rev: 1.2  
Id: 19/19