ECSE 548 (VLSI) Project Proposal - Direct-Mapped Cache

Group 2

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Proposed Design

- 128-bit Direct-Mapped Cache
- Cache Controller

Deisgn Plan / Main Components

- **Memory:** Main component of the cache which stores all the cache memory data. Memory cells are implemented using flip-flops/srams with read and write enable signals. Each memory line consists of 8 bits of data, a 6-bit tag* and a 4-bit set. This means the Cache stores data in 16 8-bit caches sets, capable of storing 4 machine instructions for a CPU in total.
- **Muxes/Demuxes:** Muxes and demuxes are used for memory decoding and encoding.
- **Comparator:** Deisnged from a full adder, used to compare the tags of data from the memory.

**We are assuming that the CPU we are deisgning a Cache for is using a memory of 1024 bytes (1KB) in size*

Evaluation Approach

- Time performance and power consumption evaluation using *SPICE*
- Area estimation (From layout in Electric)
- SystemVerilog testbenches to prove correctness
- ***Potential*** Integration with MIPS (time permitting)
- ***Potential*** performance comparison with a *N-way Set-Associative Cache* (time permitting)

Deliverables for Mid-Project Status Report

- Microarchitecture
- Schematics of Cache and Cache Controller
- Standard library cells
- SystemVerilog testbenches
- ***Potential*** SPICE simulation results