ECSE 548 (VLSI) Project Proposal - Direct-Mapped Cache

Group 2

Progress on Achieving Goals indicated in Proposal

- Microarchitecture : **Done**

- Schematics of Cache (whole circuit and each component) : **Done**

- System Verilog Testbenches : **Partially Done** - Every component (**Mux, Demux, Comparator, SRAM Array**) except *srams* were tested because *srams* are analog and need to be tested using analog simulation software (SPICE in our case). SPICE simulations are in progress.

- Schematics of Cache Controller : **Not Done**
1. Not enough time (midterms and paper submissions);
2. We encountered design issues with Cache Controller (please refer to next section for more details)

Problems Encountered So Far

1. Wrong assumption on the memory size of MIPS. - This was resolved after the clarifications from the Professor Meyer and the corresponding changes in design are represented in next section.

2. We discussed about two write policies: *write-through* and *write-back*. Due to controller complexity of write-back, we prefer to go for *write-through*.

3. After read/write-miss, we have some issues for the ouput at this particular time: usually simple processors are supposed to wait. We need to discuss this with Professor.

Modifications in Design

1. We corrected assumptions on memory size of MIPS to 256 Bytes. The sizes of Tag and Set signals were re-adjusted to 4-bit and 4-bit respectively according to the corrected assumption.

2. For the performance evaluation, SPICE simulation is a must instead of a potential option.

3. Integration to MIPS becomes a must instead of a potential option.