EECS 318 – VLSI CAD

Instructor	Office	Office Hours	Telephone	e-mail
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With Very Large Scale Integration (VLSI) technology there is an increased need for Computer-Aided Design (CAD) techniques and tools to help in the design of large digital systems that deliver both performance and functionality. Such high performance tools are of great importance in the VLSI design process, both to perform functional, logical and behavioral modeling and verification to aid the testing process. This course discusses the fundamentals in behavioral languages, both Verilog and VHDL, with Hands-on experience with state-of-the-art computer-aided design tools.

- **TA:** ??
- **Classes:** T R 10:00-11:15AM
- **Recommended Textbooks:**
  1. The Verilog Hardware Description Language, by Philip R. Moorby, Donald E. Thomas, (Kluwer Academic Publishers,) http://www.wkap.nl/
  2. The Student's Guide to VHDL, by Peter J. Ashenden, Morgan Kaufman.
- **Prerequisites:** EECS281, EECS315
- **Topics:**
  1. Structure design concept
  2. Design tools
  3. Basic Feature of Verilog
  4. Basic Verilog Modeling Techniques
  5. Basic Feature of VHDL
  6. Basic VHDL Modeling Techniques
  7. Algorithmic Level Design
  8. Register Level Design Models
  9. Detailed level Models
  10. Multi-level Models
  11. Logic Level Simulation algorithms
- **Labs:** Labs will be due at the beginning of class on the date specified, almost always on Thursday. Late assignment earns 5% penalty per day up to 25%.
- **Grades:** Are based on 5 laboratory projects each earning 20%.