```
module busdriver (busin, bushigh, buslow, enh, enl);
input [15:0] busin;
output [7:0] bushigh, buslow;
input enh, enl;
        driver  busar3(busin[15:12], bushigh[7:4], enh);
        driver  busar2 (busin[11:8], bushigh[3:0], enh);
        driver  busar1(busin[7:4], buslow[7:4], enl);
        driver  busar0(busin[3:0], buslow[3:0], enl);
endmodule

module busdriver_equiv (busin, bushigh, buslow, enh, enl);
input [15:0] busin;
output [7:0] bushigh, buslow;
input enh, enl;
   driver busar[3:0] (.out({bushigh, buslow}), .in(busin),.en({enh, enh,enl,enl}));
endmodule
```

```
module driver (in, out, en);
input [3:0] in;
output [3:0] out;
input en;
        bufif0 ar[3:0] (out, in, en); // array of three-state buffers
endmodule


module driver_equiv (in, out, en);
input [3:0] in;
output [3:0] out;
input en;
        bufif0 ar3 (out[3], in[3], en); // each buffer declared separately
        bufif0 ar2 (out[2], in[2], en);
        bufif0 ar1 (out[1], in[1], en);
        bufif0 ar0 (out[0], in[0], en);
endmodule
```

and	0	1	x	z
0	0	0	0	0
1	0	1	x	x
x	0	x	x	x
z	0	x	x	x

or	0	1	x	z
0	0	1	x	x
1	1	1	1	1
x	x	1	x	x
z	x	1	x	x

xor	0	1	x	z
0	0	1	x	x
1	1	0	x	x
x	x	x	x	x
z	x	x	x	x

nand	0	1	x	z
0	1	1	1	1
1	1	0	x	x
x	1	x	x	x
z	1	x	x	x

nor	0	1	x	z
0	1	0	x	x
1	0	0	0	0
x	x	0	x	x
z	x	0	x	x

xnor	0	1	x	z
0	1	0	x	x
1	0	1	x	x
x	x	x	x	x
z	x	x	x	x

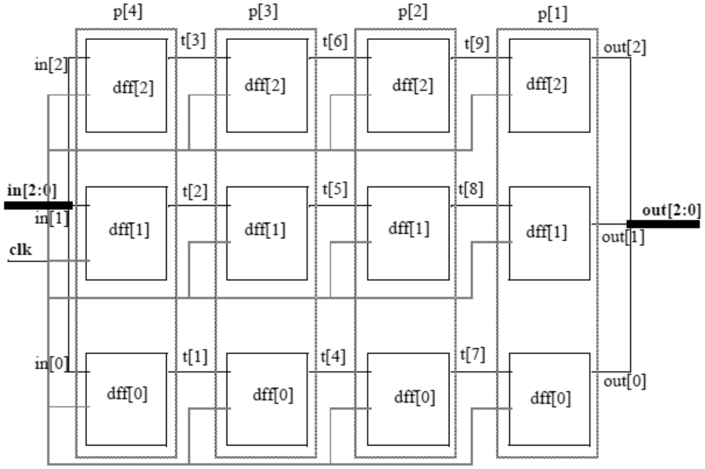
```
and X1 (out, a,b);
```

buf	
input	output
0	0
1	1
x	x
z	x

not	
input	output
0	1
1	0
x	x
z	x

```
buf b1 X1(z,i);
```

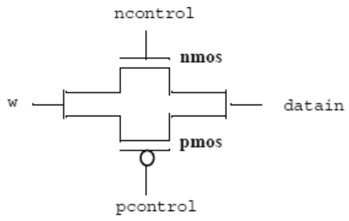
```
module dffn (q, d, clk);
parameter bits = 1;
input [bits-1:0] d;
output [bits-1:0] q;
input clk ;
        DFF dff[bits-1:0] (q, d, clk); // create a row of D flip-flops
endmodule
module MxN_pipeline (in, out, clk);
parameter M = 3, N = 4;                     // M=width,N=depth
input [M-1:0] in;
output [M-1:0] out;
input clk;
wire [M*(N-1):1] t;
        // #(M) redefines the bits parameter for dffn
        // create p[1:N] columns of dffn rows (pipeline)
        dffn #(M) p[1:N] ({out, t}, {t, in}, clk);
endmodule
```



Bidirectional pass switches: tran, tranif0, tranif1, rtran, rtranif0, rtranif1;

tranif1 t1 (inout1,inout2,control);

cmos and rcmos



cmos (w, datain, ncontrol, pcontrol);

nmos (w, datain, ncontrol);
pmos (w, datain, pcontrol);

pullup, pulldown;

pullup (strong1) p1 (neta), p2 (netb);

bufif0		CONTROL			
		0	1	x	z
D	0	0	z	L	L
A	1	1	z	H	H
T	x	x	z	x	x
A	z	x	z	x	x

bufif1		CONTROL			
		0	1	x	z
D	0	z	0	L	L
A	1	z	1	H	H
T	x	z	x	x	x
A	z	z	x	x	x

notif0		CONTROL			
		0	1	x	z
D	0	1	z	H	H
A	1	0	z	L	L
T	x	x	z	x	x
A	z	x	z	x	x

notif1		CONTROL			
		0	1	x	z
D	0	z	1	H	H
A	1	z	0	L	L
T	x	z	x	x	x
A	z	z	x	x	x

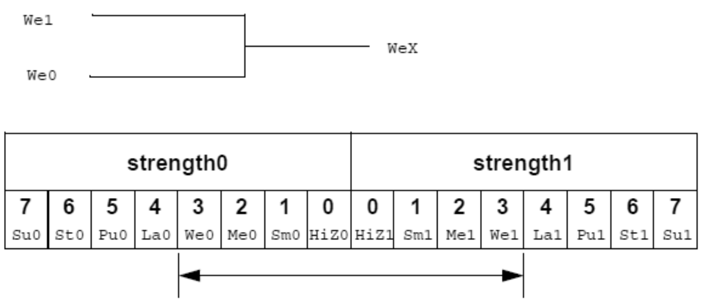
bufif1 X1 (outw, inw, control);

pmos rpmos		CONTROL			
		0	1	x	z
D	0	0	z	L	L
A	1	1	z	H	H
T	x	x	z	x	x
A	z	z	z	z	z

nmos rnmos		CONTROL			
		0	1	x	z
D	0	z	0	L	L
A	1	z	1	H	H
T	x	z	x	x	x
A	z	z	z	z	z

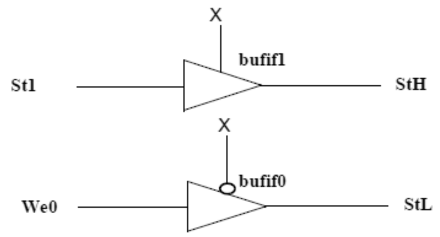
pmos p1 (out, data, control);

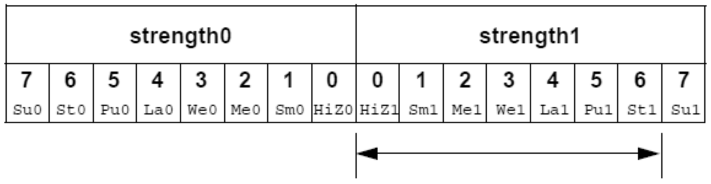
unidirectional: cmos, nmos, pmos, rcmos, rpmos



strength0								strength1							
7	6	5	4	3	2	1	0	0	1	2	3	4	5	6	7
Su0	St0	Pu0	La0	We0	Me0	Sm0	HiZ0	HiZ1	Sm1	Me1	We1	La1	Pu1	St1	Su1

Figure 7-5—Weak x signal strength





strength0								strength1							
7	6	5	4	3	2	1	0	0	1	2	3	4	5	6	7
Su0	St0	Pu0	La0	We0	Me0	Sm0	HiZ0	HiZ1	Sm1	Me1	We1	La1	Pu1	St1	Su1

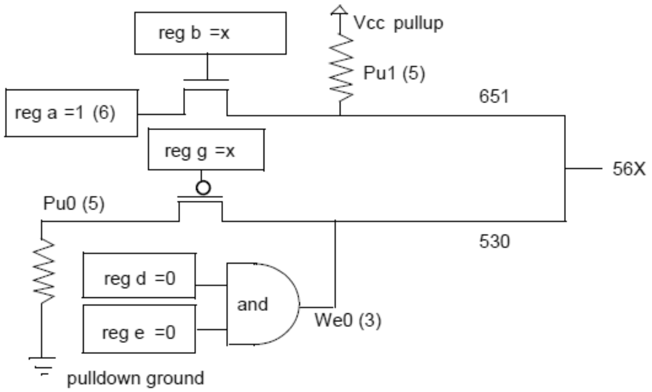
H range

–Strength levels for scalar net signal values

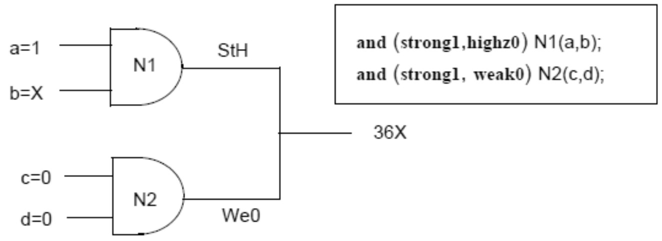
Strength name	Strength level
supply0	7
strong0	6
pull0	5
large0	4
weak0	3
medium0	2
small0	1
highz0	0
highz1	0
small1	1
medium1	2
weak1	3
large1	4
pull1	5
strong1	6
supply1	7

strength0								strength1							
7	6	5	4	3	2	1	0	0	1	2	3	4	5	6	7
Su0	St0	Pu0	La0	We0	Me0	Sm0	HiZ0	HiZ1	Sm1	Me1	We1	La1	Pu1	St1	Su1

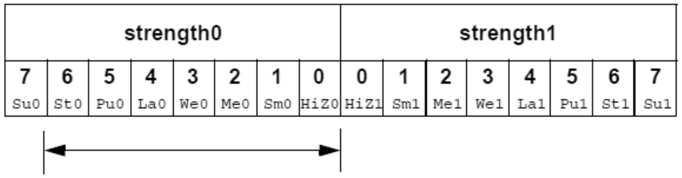
Scale Strength



Ambiguous strengths from switch networks

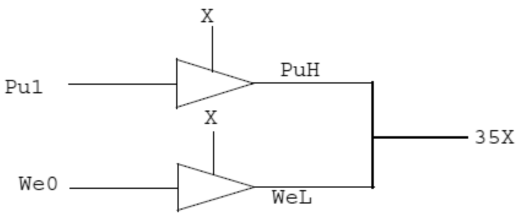


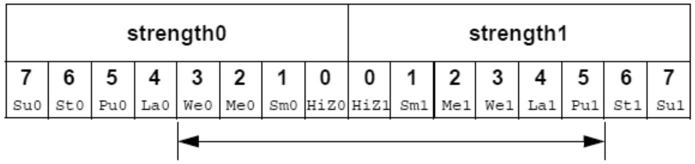
```
and (strong1,highz0) N1(a,b);
and (strong1, weak0) N2(c,d);
```



strength0								strength1							
7	6	5	4	3	2	1	0	0	1	2	3	4	5	6	7
Su0	St0	Pu0	La0	We0	Me0	Sm0	HiZ0	HiZ1	Sm1	Me1	We1	La1	Pu1	St1	Su1

L range

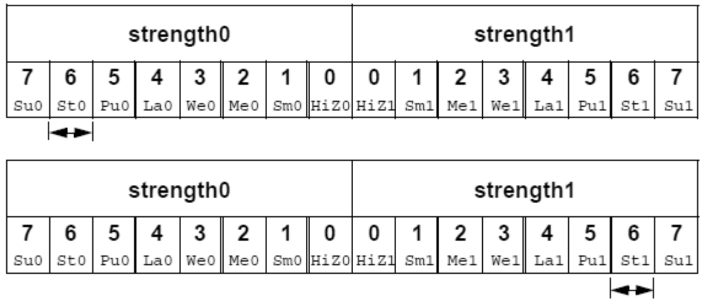




strength0								strength1							
7	6	5	4	3	2	1	0	0	1	2	3	4	5	6	7
Su0	St0	Pu0	La0	We0	Me0	Sm0	HiZ0	HiZ1	Sm1	Me1	We1	La1	Pu1	St1	Su1

Unknown signal range

Wired logic: trand, wand, trior, wor



strength0								strength1							
7	6	5	4	3	2	1	0	0	1	2	3	4	5	6	7
Su0	St0	Pu0	La0	We0	Me0	Sm0	HiZ0	HiZ1	Sm1	Me1	We1	La1	Pu1	St1	Su1

strength0								strength1							
7	6	5	4	3	2	1	0	0	1	2	3	4	5	6	7
Su0	St0	Pu0	La0	We0	Me0	Sm0	HiZ0	HiZ1	Sm1	Me1	We1	La1	Pu1	St1	Su1

```
wired AND logic value result:    0
wired OR  logic value result:    1
```

Input strength	Reduced strength
Supply drive	Pull drive
Strong drive	Pull drive
Pull drive	Weak drive
Large capacitor	Medium capacitor
Weak drive	Medium capacitor
Medium capacitor	Small capacitor
Small capacitor	Small capacitor
High impedance	High impedance

Strength redunction rules