tsmc *Taiwan Semiconductor Manufacturing Co., LTD*

SECURITY **B**
TSMC-RESTRICTED

Ver	Eff_Date	ECN No.	Author	Change Description
2.6	05-17-06	E070200616013	R. G. Wu	1.Add NP.R.3 and PP.R.3 2.Refine RPO.C.4, RPO.C.5, OD.W.3 and NT_N.I.3 3.Remove Old Doc. No. "TA-10A5-4001"

Revisor : R. G. Wu (PDS)

Revising Line Manager : Y. C. Harn

Approvals:

Please refer EDW workflow to see detail approval records

Title

TSMC 0.18UM LOGIC 1P6M SALICIDE 1.8V/3.3V DESIGN RULE

Document No. : T-018-LO-DR-001

Contents	: 91	Review
Attach.	: 0	(Date & Sig.) :
Total	: 91	
File Format	: W	

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Ver	Eff_Date	ECN No.	Author	Change Description
2.2	05-30-01	E011615	S. C. Kuo	1.Add redundancy guideline for embedded SRAM and modify user guide 2.Add description of planar capacitor Emb-SRAM in user guide 3.Delete metal fuse rule and alignment mark rule for there's a separate document 4.Modify NP.E.6/PP.E.6 5.Modify Seal-ring rule 6.Modify figure of NP/PP 7.Add layout grid 0.005um at 1X
2.3	11-02-01	F012402	S. J. Peng	1.Add planar capacitor Emb-SRAM rules 2.Delete DSER guide Pait I item 17 (P.5), Planar capacitor Emb-SRAM guidelines
2.4	07-04-03	70325001	Alex Fanh	1. Revise NW resistor rule NWR.O.1. NW resistor under STI add "NP to OD extension" rule. 2. Merge section of "Redundancy Guideline for Embedded SRAM" and "Dummy Layout for Embedded SRAM" to "SRAM Guideline". 3. Keep no Polyimide(PM) over seal ring and assembly isolation . Seal ring rule add some wordings. 4. Add the section of "Guidelines for NC (No-Connect) pin during ESD testing"
2.5	04-23-04	E070200416009	T. M. Fu	1. Revise wide metal and metal slot rules. 2. Revise NTN.W.1. 3. Move NTN section to the front. 4. Refine ESD guidelines and wording.

Title

TSMC 0.18UM LOGIC 1P6M SALICIDE 1.8V/3.3V DESIGN RULE

Document No. : T-018-LO-DR-001

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Ver	Eff_Date	ECN No.	Author	Change Description
0.1	05-13-98	T981419	C. C. Tsai	Original
0.2	09-15-98	F983509	C. C. Tsai	Increase manufacturability and make design rule description more clear
1.0	10-09-98	F983951	C. C. Tsai	Make design rule more compatible with Si data
1.1	11-05-98	F984419	C. C. Tsai	Modify P5 to make process margin safer
1.2	03-23-99	F991129	C. C. Tsai	1.Make rule more clear and safer (change items refer to P.5) 2.Change Document Number from "TA-10A5-4001" to "T-018-LO-DR-001"
2.0	05-18-00	F001803	J. H. Hsu	1.Guideline for migration to CL018LV and poly resistor, P3V, RPO.C.6, antenna ratio for top metal, native device rule, metal fuse rule 2.Recommendation of NW resitor under STI, N2V/N3V/NP/PP.C.4, NP/PP.S.2, passivatioin rules 3.Ph layer, OD.W.3, CO.S.2, CO.C.2, A.R.3, A.R.6, ESD guideline
2.1	09-29-00	F003714	C. P. Yeh	1.Use guide update 2.Delete N2V/N3V/P2V/P3V 3.Merge via rule/metal rule 4.ESD guideline update

Title

TSMC 0.18UM LOGIC 1P6M SALICIDE 1.8V/3.3V DESIGN RULE

Document No. : T-018-LO-DR-001

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* * * TSMC * * *

TSMC 0.18UM LOGIC 1P6M SALICIDE 1.8V/3.3V DESIGN RULE

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Contents

Page :

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0. USER GUIDE

This section includes four parts:
Part I, Recommendations for users to design better circuits.
Part II, Non-shrinkable rules for the shrink in the future generation
Part III, List the changes different from last version

Part IV, Migration guide from CL018G to CL018LV

PART I

The design rule layout grid is 0.005um at 1X.
This section lists the recommendations for users to design with high yield and better reliability.

1. To obtain more accurate resistance as in SPICE model, it is strongly recommended that the NW resistor width ≥ 2.1 μm and the resistor square number $N_{sq} \geq 5$.

2. For stacked structure (CO/VIA1, VIA1/VIA2, VIA2/VIA3, VIA3/VIA4, VIA4/VIA5, CO/VIA1/VIA2, VIA1/VIA2/VIA3, VIA2/VIA3/VIA4, CO/VIA1/VIA2/VIA3, VIA1/VIA2/VIA3/VIA4, VIA2/VIA3/VIA4/VIA5, CO/VIA1/VIA2/VIA3/VIA4/VIA5 stacks), it is suggested to keep M1/2/3/4/5 as 0.45x0.45 μm^2 square shape, M6 as 0.9x0.9 μm^2 square, and contact/via at the center of metal island as much as possible.

3. Follow antenna rules to ensure gate oxide reliability.

4. Add dummy pads at chip corners for better CMP planarization.

5. The chip corner power line layout is suggested for more resistance to thermal stress induced metal delamination and oxide crack. The structure must be M6/VIA5/M5/VIA4/M4/VIA3/M3/VIA2/M2/VIA1/M1/STI. For detail layout, please contact TSMC.

6. Use bigger metal end-of-line extension whenever possible.

7. Use redundant contacts and vias whenever possible. For redundant via insertion, it is recommended to use TSMC's insertion utility. (Document number: T-018-LO-DR-001-C4)

8. Use anchor at end of isolated long metal lines whenever possible. (The suggested anchor-shape is as the shaded region in Fig. R1)

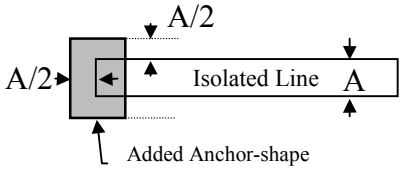

Fig. R1

9. Add dummy OD and poly patterns at edge of memory cell array to improve cell uniformity.

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10. Increase PP.E.3/NP.E.3 up to 0.18 μm if OD width ≤ 0.42 μm. It's also recommended that the length of such narrow pickup OD be less than 50 μm.

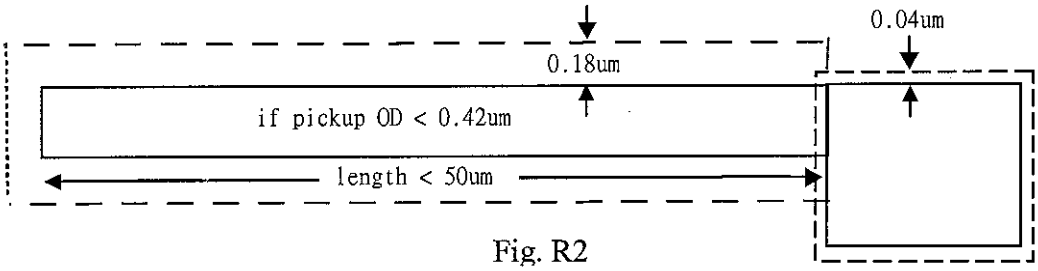
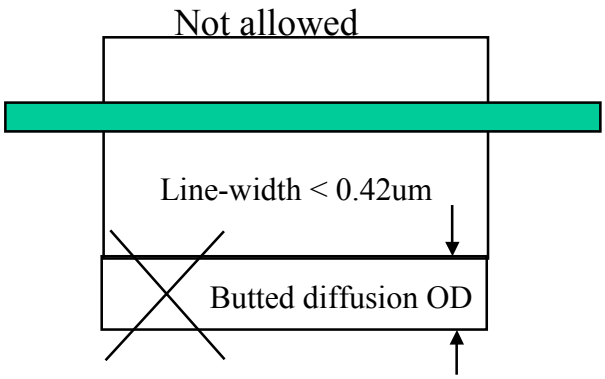


Fig. R2

11. To prevent insufficient butted diffusion area from implant misalignment, it's recommended to make the width of butted diffusion larger than 0.42 μm. Please also refer to OD.W.3.



12. To minimize risk of current leakage resulting from LDD shadowing effect, keep 45° bent poly on OD as short as possible and 90° bent poly layout shown below should be avoided.

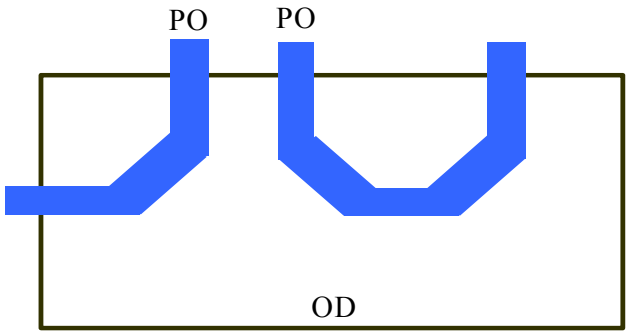


Fig. R3 L and U are not recommended due to electrical degradation

13. For *5V High Voltage Tolerant I/O designed by 3.3V NMOS (up to 5V at I/O pad)*, ESD implant is required unless special design by customer. TSMC will use ESD Dummy layer (ESD3DMY, see Rule no. 23) to generate ESD mask (no. 111) by logic operation.

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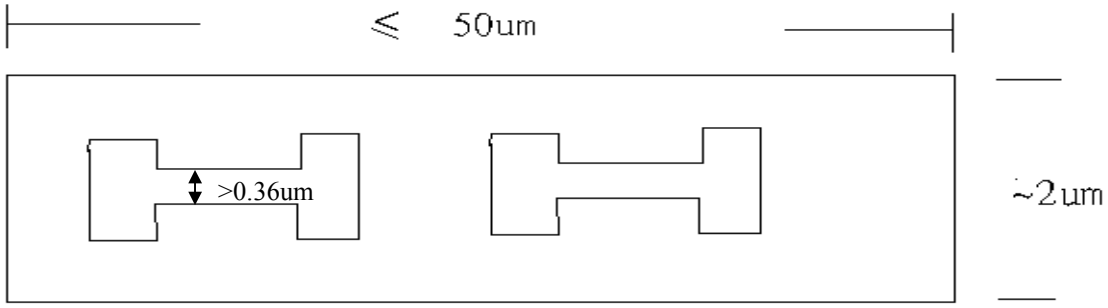
14. Avoid long narrow strip type of OD(L > 50um & W < 2um) which enclose STI sharp polygon inside . Minimum STI width inside is 0.36um.



15. Apply/calculate current density rules after metal slots are added.

16. For accumulated SRAM density larger than 1.5M, redundancy is needed. Please refer to the most-updated version of "TSMC 0.15um/0.18um/0.25um SRAM engineer report of SRAM redundancy for C025/C018/C015" (document no. T-018-SM-RP-001) as embedded SRAM redundancy guideline.

17. If your products will be used in high reliability requirement applications, such as automotives, please contact TSMC account manager for the associated document.

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PART II

Due to the limitation of process technology, some rules are expected to be non-shrinkable in the next generation technology. To dumb-shrink to the next generation, it's suggested to pre-relax these rules in 0.18 µm generation. Their rule numbers and page numbers are listed in the following table. Besides, those rules listed in USER GUIDE, PART IV CL018LV MIGRATION GUIDELINE also need be followed.

Non-shrinkable Rules	
Page No	**Rule No.**
18	NW.S.2
21	OD.C.1, OD.C.5, OD.C.6
24	OD2.S.1
26	PO.W.1, PO.W.2, PO.S.1, PO.S.2 for 3.3V
39	NP.C.4, NP.C.5, NP.E.1, NP.E.3, NP.E.6, NP.A.1
42	PP.C.4, PP.C.5, PP.E.1, PP.E.3, PP.E.6, PP.A.1
45	RPO.C.1, RPO.C.2, RPO.C.4, RPO.C.5, RPO.C.6, RPO.E.1
49	M1.E.1, M1.S.2
51	VIA1.E.1
53	M2.E.1, M2.S.2
55	VIA2.E.1
57	M3.E.1, M3.S.2
59	VIA3.E.1
61	M4.E.1, M4.S.2
63	VIA4.E.1
65	M5.E.1, M5.S.2
67	VIA5.W.1, VIA5.S.1, VIA5.E.1
69	M6.W.1, M6.S.1, M6.S.2, M6.E.1

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PART III

CHANGES BETWEEN VERSION 2.4 AND VERSION 2.5

1. Refine wide-metal & slotting rules:
    a. Clearly define wide-metal as being >35x35um (both width and length).
    b. Add the slot density "AMS.DN.Mx " to replace all slotting rules.
    c. Slotting dimension rules became guidelines.
2. Refine ESD rule/guidance wording:
    a. Add descriptions for SDI-dummy for DRC purpose.
    b. Add descriptions for some process-control-related items for DRC, including ESD.5x, 6 and 11.
3. Move NTN rule to the front & relax NTN.W.1 from 0.86 to 0.74um.

CHANGES BETWEEN VERSION 2.1 AND VERSION 2.2

0. Add redundancy guideline for embedded SRAM and modify user guide.
1. Add description of planar capacitor Emb-SRAM in user guide.
2. Delete metal fuse rule and alignment mark rule for there's a separate document.
3. Modify NP.E.6/PP.E.6
4. Modify Seal-ring rule
5. Modify figure of NP/PP
6. Add layout grid 0.005um at 1X

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CHANGES BETWEEN VERSION 2.0 AND VERSION 2.1

Item.	V2.0	V2.1	Remark
User guide part I	None	13. ESD implant	TSMC should use ESD Dummy layer to generate additional ESD mask by logic operation.
	None	14. OD layout guide line	Avoid long strip OD with narrow STI polygon inside
	None	15. Current density rule related	Apply/calculate current density after metal slots are added
User guide part IV	Rule 4, NW space 0.86um	Deleted	Allow NW space 0.6 (NW.S.2)
NW resistor in OD rule.	None	Add descriptions	Transfer Fig 1(a) to 7 rule items.
NWR.C.2	0.3	0.22	Minimum clearance from RPO to related OD
OD.W.3	> 0.42	≥ 0.42	Make DRC consistent with rule
PO.R.2	Maximum length of poly between two contacts	Maximum length of salicide poly on STI between two contacts or between one contact and poly line end when poly width ≤ 0.24um	Description modification
N2V/N3V/P2V/P3V	Existed	Deleted	N2V/N3V/P2V/P3V masks are generated by logical operations as default to simplify the tape out process.
Via rule	Via 1~4, 4 sets of rule with the same dimensions	Via x (x=1,2,3,4), 1 set of rule	Merge Via 1~4 rule
Metal rule	Metal 2~5, 4 sets of rule with the same dimensions	Metal x (x=2,3,4,5), 1 set of rule	Merge Metal 2~5 rule
Current density specification	None	It's nominal AlCu thickness ...	Description modification
Metal fuse rule Item M.	20	10	In consistence with CL025
Latch-up prevention Fig1	A > 20	A > 15	Correct typing error
Dummy layouts for embedded SRAM	None	Add dummy layouts rule for embedded SRAM	Prevent proximity and loading effect. Detail guidelines and their GDS-II examples are provided in SRAM cell layout documents
AM.S.3	None	35um	Maximum slots space
ESD guide line: (on 5V High Voltage Tolerant I/O)	None	ESD3DMY (CAD layer 234) is required.	TSMC should use ESD3DMY layer to generate additional ESD mask by logic operation.
ESD poly spacing	None	Poly spacing between inactive poly and active poly is 0.25um~0.45um	Better ESD performance once spacing 0.25um~0.45um.
ESD Rule 9	None	The minimum Lg in I/O buffer for ESD implant is 0.4um ESD performance is not guaranteed once Lg > 0.5 um.	No approved data in tsmc for Lg > 0.5um.
ESD implantation rule	Existed (ESD(110))	Deleted	Use ESD3DMY (CAD layer, 234) to generate additional ESD layer.

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PART IV

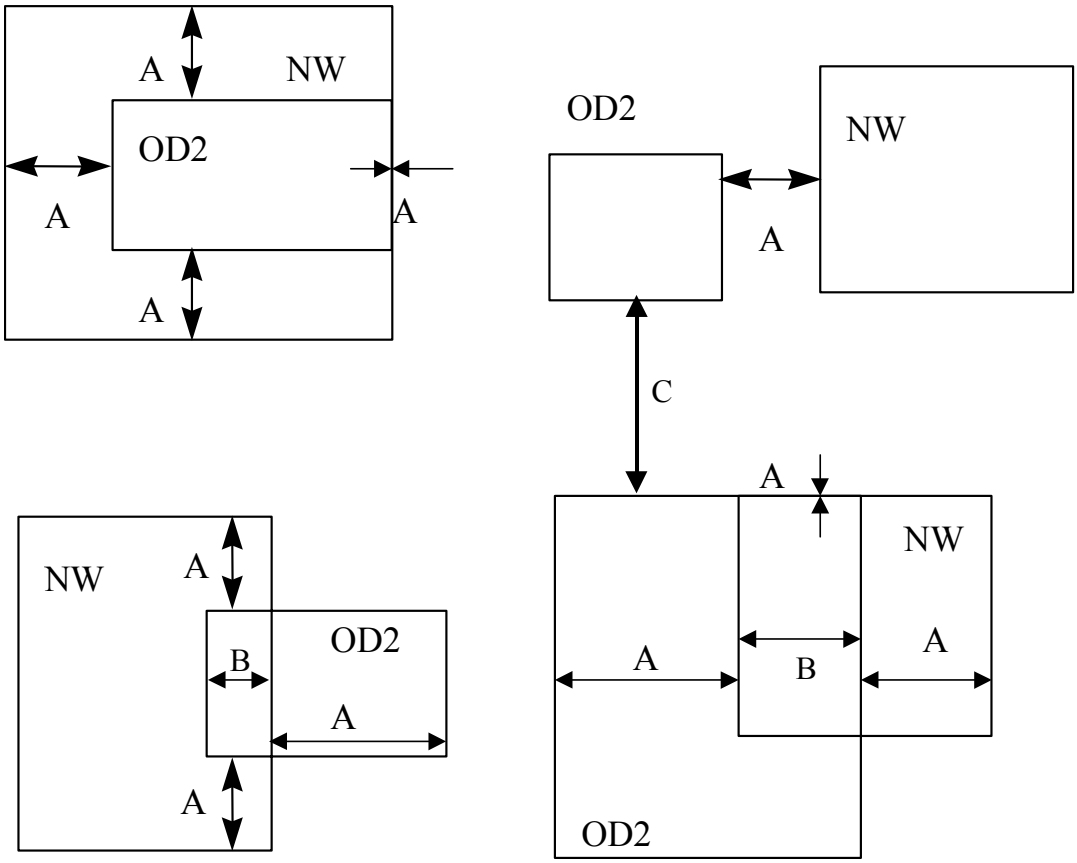
CL018LV MIGRATION GUIDELINE

Database conversion from CL018G to CL018 LV process

To facilitate customers converting CL018G database to CL018LV database, following guidelines are provided:

Modify OD2 and NW layout and make them meet following rules in addition to the original design rules.

Rule 1. Minimum clearance/extension between OD2 and NW Align if space less than 0.860 um	A	0.86 µm
Rule 2. Minimum overlap between OD2 and NW	B	0.86 µm
Rule 3. Minimum spacing between two OD2 regions	C	0.86 µm



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1. INTRODUCTION

The physical design rule of 0.18μm salicide process included in this manual is used as a basic layout guide for those who want to design and layout a circuit based on TSMC 0.18μm LOGIC, 1.8V/3.3V process. This includes 1P3M to 1P6M process.

Among them, salicide, 1.8V/3.3V 1P6M process is treated as a generic process. For other process, please refer to following table for its usage of this design rule.

Process	Optional Rule Set
1P5M	Skip Metal5 and Via4 layers Treat Metal6 as top metal and Via5 as top Via
1P4M	Skip Metal5, Metal4, Via4 and Via3 layers Treat Metal6 as top metal and Via5 as top Via. (Seal ring, bond pad and metal stress relief are excluded from this application, please refer to these layers for further detail.)
1P3M	Skip Metal5, Metal4, Metal3, Via4, Via3 and Via2 layers Treat Metal 6 as top metal and Via5 as top Via. (Seal ring, bond pad and metal stress relief are excluded from this application, please refer to these layers for further detail.)

This design rule (or layout rule) has been defined as the dimension on wafer. The difference of a feature size between mask pattern and wafer pattern should be adjusted by CAD (Computer-Aided Design) bias. For CAD bias, please refer to document TA-10A5-6101 “TSMC 0.18μm LOGIC 1P6M Salicide 1.8V/3.3V Masking Layers and Bias”.

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1.1 RESERVED MASK NAMES

The following names are reserved for standard mask steps, which should not be used for other purpose without further instructions.

OD --- Definition of thin oxide for device, and interconnection.

ODR --- Definition of reverse thin oxide.

PW --- Definition of P-Well.

NW --- Definition of N-Well.

OD2 --- Definition of thick oxide for device.

PO --- Definition of Poly-Si.

N2V --- Definition of 1.8V-NLDD implantation.

P2V --- Definition of 1.8V-PLDD implantation.

P3V --- Definition of 3.3V-PLDD implantation.

N3V --- Definition of 3.3V-NLDD implantation.

NP --- Definition of N+ implantation.

PP --- Definition of P+ implantation.

ESD --- Definition of ESD implantation.

RPO --- Definition of salicide protection.

CO --- Definition of contact window from M1 to OD or PO.

M1 --- Definition of 1st metal for interconnection.

VIA1 -- Definition of via1 hole between M2 and M1.

M2 --- Definition of 2nd metal for interconnection.

VIA2 -- Definition of via2 hole between M3 and M2.

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M3 --- Definition of 3rd metal for interconnection.

VIA3 -- Definition of via3 hole between M4 and M3.

M4 --- Definition of 4th metal for interconnection.

VIA4 -- Definition of via4 hole between M5 and M4.

M5 --- Definition of 5th metal for interconnection.

VIA5 -- Definition of via5 hole between M6 and M5.

M6 --- Definition of 6th metal for interconnection.

CB --- Definition of passivation opening window at bonding pad.

PM --- Definition of polyimide opening window.

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1.2 TERMINOLOGY

The following definitions are used in the physical design rules :

N+ OD	:	OD covered with NP.
P+ OD	:	OD covered with PP.
Cold N-Well	:	N-Well connected to the most positive voltage (Vdd).
Hot N-Well	:	N-Well not connected to the most positive voltage
Hot N+ diffusion	:	all N+ diffusion regions outside the N-Well which have a potential not equal to the substrate voltage.
Hot P+ diffusion	:	all P+ diffusion regions inside the N-Well which have a potential not equal to the N-Well potential.
Cold diffusions	:	
Outside N-Well	:	a diffusion which has the potential the same as the substrate.
Inside N-Well	:	a diffusion which has the potential the same as the N-Well.

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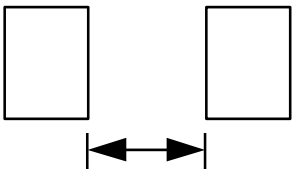
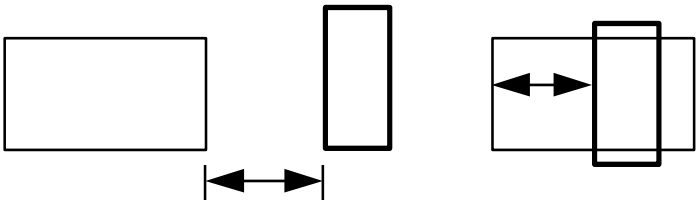
1.3 DEFINITION OF THE LAYOUT LAYERS

WIDTH :

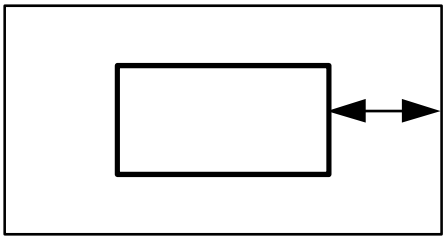
SPACE :



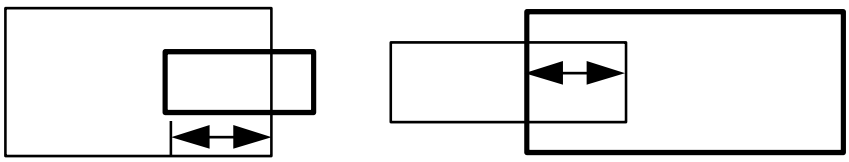
CLEARANCE :



EXTENSION :



OVERLAP :



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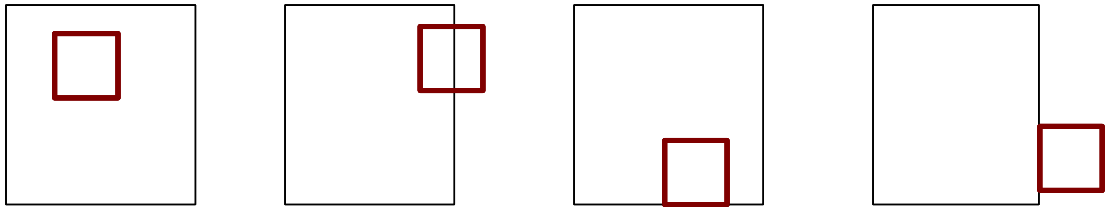
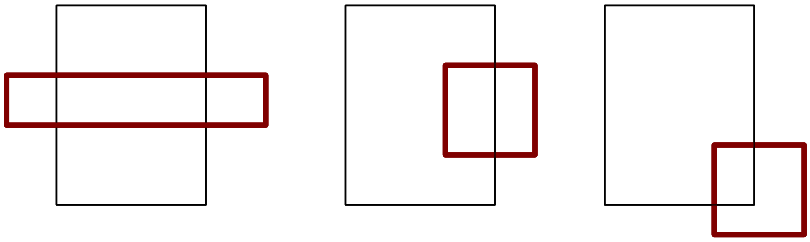
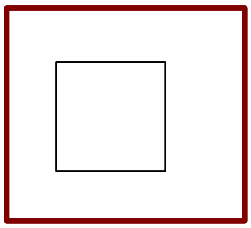
Interact



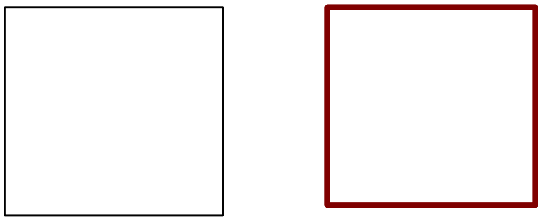
Cut



Inside



Outside



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1.4 PITCHES

OD transistor pitch	0.500 um
OD interconnect pitch	0.500 um
PO transistor pitch	0.43/0.555 um
PO interconnect pitch	0.430 um
M1 pitch	0.460 um
M2 pitch	0.560 um
M3 pitch	0.560 um
M4 pitch	0.560 um
M5 Pitch	0.560 um
M6 Pitch	0.900 um
Min. length of a transistor	0.180 um
Min. width of a transistor	0.220 um
PO interconnect width	0.180 um
OD interconnect width	0.220 um
CO width	0.220 um
VIA1 width	0.260 um
VIA2 width	0.260 um
VIA3 width	0.260 um
VIA4 width	0.260 um
VIA5 width	0.360 um
N+/P+ spacing	0.860 um

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2. KEY PROCESS SEQUENCE

Masking Sequence	Digitized Pattern	Digitized Area (Dark/Clear)
1. Thin Oxide (OD)	Thin Oxide	D
2. Trench (ODR)	Thin Oxide	C
3. P-Well (PW)	N-Well	D
4. N-Well (NW)	N-Well	C
5. Thick Oxide (OD2)	Thick Oxide	D
6. Poly (PO)	Poly	D
7. NLDD Implant (N2V)	1.8V-NLDD Implant	C
8. PLDD Implant (P2V)	1.8V-PLDD Implant	C
9. PLDD Implant (P3V)	3.3V-PLDD Implant	C
10. NLDD Implant (N3V)	3.3V-NLDD Implant	C
11. N+ S/D Implant (NP)	N+ S/D Implant	C
12. P+ S/D Implant (PP)	P+ S/D Implant	C
* ESD (ESD)	ESD Implant	C
13. RPO (RPO)	Resist Protection Oxide	D
14. Contact (CO)	Contact	C
15. Metal-1 (M1)	Metal-1	D
16. Via1 Hole	Via1	C
17. Metal-2 (M2)	Metal-2	D
18. Via2 Hole	Via2	C
19. Metal-3 (M3)	Metal-3	D
20. Via3 Hole	Via3	C
21. Metal-4 (M4)	Metal-4	D
22. Via4 Hole	Via4	C
23. Metal-5 (M5)	Metal-5	D
24. Via5 Hole	Via5	C
25. Metal-6 (M6)	Metal-6	D
26. Pads (CB)	Bonding Pads	C
* Polyimide (PM)	Polyimide Window	D

1. Total 26 masks with 26 masking steps (excluding optional masks for ESD and Polyimide).
2. Trench mask is a reverse tone of Thin Oxide mask with bias.
3. PW mask is a reverse tone of N-Well mask without bias

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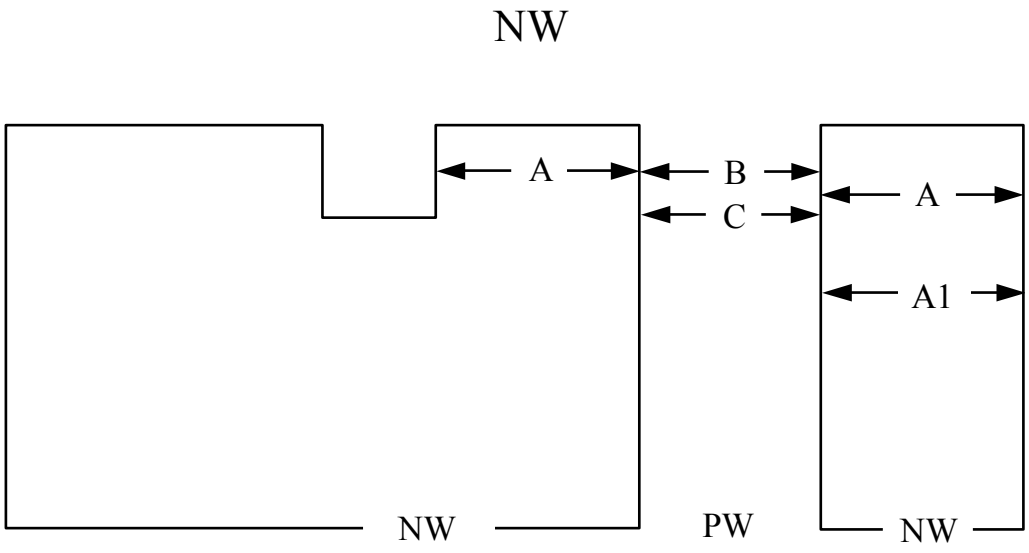
3. LAYOUT RULE DESCRIPTION

◘ N-Well Rule (192)

Rule No.	Description	Label		Layout Rule
Layer :	NW --- N-Well			
NW.W.1	Minimum dimension of a NW region	A	≧	0.86 um
NW.W.2	Minimum dimension of a hot NW region	A1	≧	2.10 um
	Please refer to NW resistor layout rule in the next page for detail layout rule			
NW.S.1	Minimum space between two NW regions with different potential	B	≧	1.40 um
NW.S.2	Minimum space between two NW regions with the same potential Merge if space is less than 0.6 um	C	≧	0.6um
	(Below item is referred from the ESD Section)			
ESD.11	Butting or inserted Substrate/Well pick-up's in the ESD N/PMOS are strictly prohibited.			



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❑ NW resistor layout rule

For the SPICE simulation accuracy concern, it is strongly recommended that the NW resistor width ≥ 2.1 μm and the resistor square number N_{sq} ≥ 5. Please use 1.4 μm as the minimum NW space to prevent from the resistance decrease of NW resistor due to mergence of different regions.

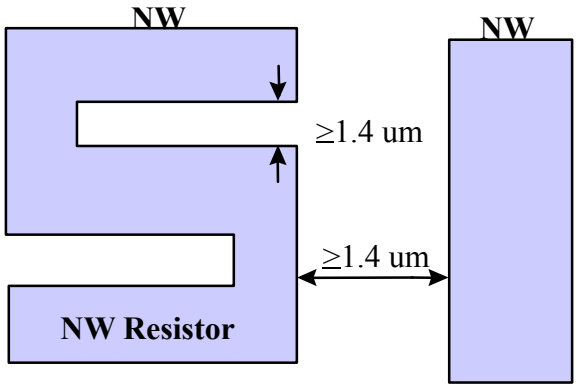

Fig 1(a) NW resistor within OD
- Add RPO to prevent NW resistance region from forming salicide.
- Dummy layer (RWDMY) is needed for DRC, to avoid LDD and N+/P+ implanting into NW resistance region.

Rule No.	Description	Label		Layout Rule
NWR.E.1	Minimum extension of OD to NW	A	≧	1.0 um
NWR.E.2	Minimum extension of salicide NW to CO	B	≧	0.3 um
NWR.C.1	Minimum clearance from RPO to related NW	C	≧	0.3 um
NWR.C.2	Minimum clearance from RPO to related OD	D	≧	0.22 um
NWR.C.3	Minimum clearance from RPO to CO in RPO hole	E	≧	0.3 um
NWR.O.1	Minimum overlap of RPO to NP	F	≧	0.4 um
NWR.R.1	P+/N+ implant inside NW resistance region is not allowed			

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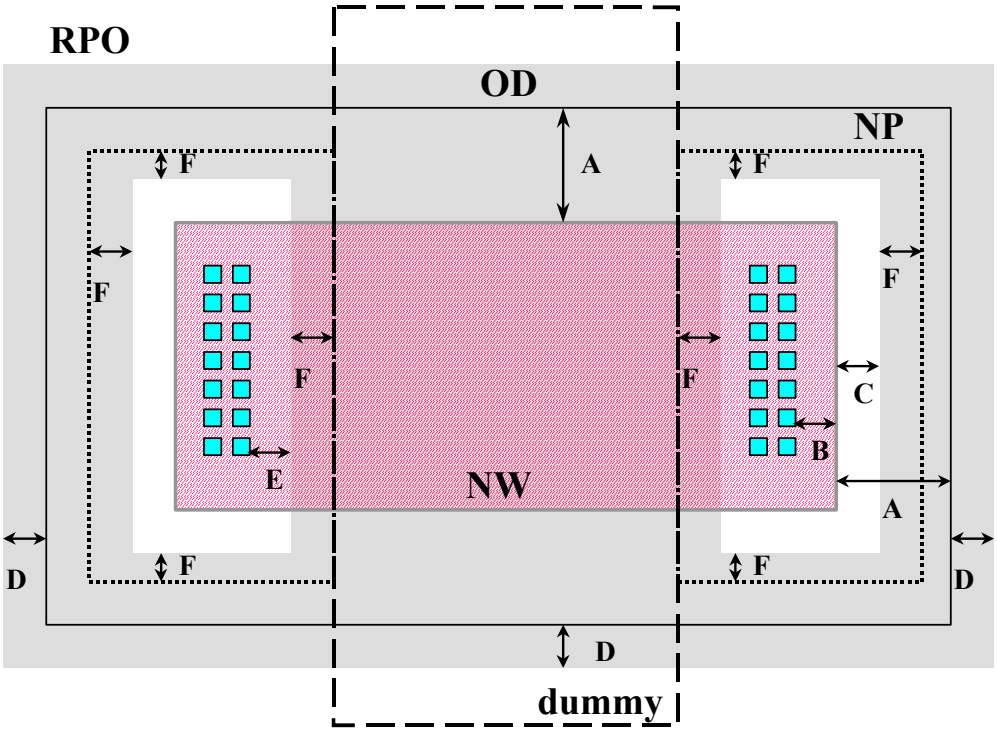

Fig 1(a)

Fig. 1(b) NW resistor under STI

Rule No.	Description	Label		Layout Rule
NWR.E.3	Minimum extension of a NP region beyond a OD region	G	≧	0.18 um

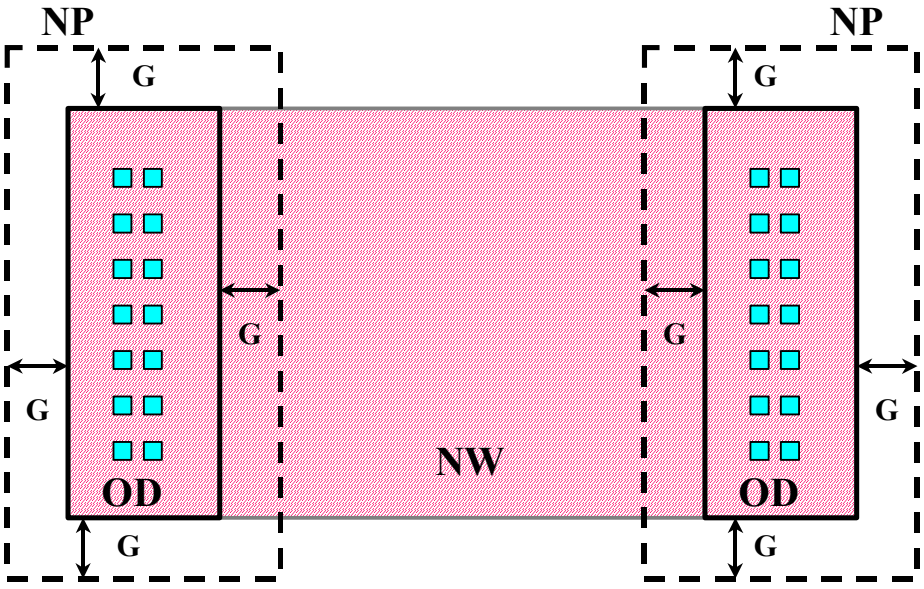

Fig 1(b)

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◘ NT_N (Native Device Blocked Implant Definition) Rule

This layer is not a masking layer but used to merge with NW to generate PW mask

Rule No.	Description	Label		Layout rule (um)
Layer :	NT_N -- NT_N implant Definition to Block PW, Channel_N and VT_N Implantation for NMOS Native Device)			
NT_N.I.2	Only one OD region allowed to be put in an NT_N region			
NT_N.I.3	A P+ Poly gate is not allowed to be put in an NT_N region			
NT_N.I.4	A bent Poly region is not allowed to be put in an NT_N region			
NT_N.W.1	Minimum dimension of a NT_N region.	A	≧	0.74
NT_N.W.2	Minimum Po1y gate dimension of a 1.8V blocked NT_N device.	B	≧	0.50
	Minimum Po1y gate dimension of a 3.3V blocked NT_N device		≧	1.20
NT_N.S.1	Minimum space between two NT_N regions..	C	≧	0.86
NT_N.E.1	Maximum and Minimum extension from a NT_N region beyond an NP OD region.	D	=	0.26
NT_N.C.1	Minimum clearance from a NT_N region to nominal OD region.	E	≧	0.52
NT_N.C.2	Minimum clearance from a NT_N region to an N-well edge.	F	≧	1.66
NT_N.PO.1	Minimum overlap of a PO region extended into field oxide (endcap)	G	≧	0.35

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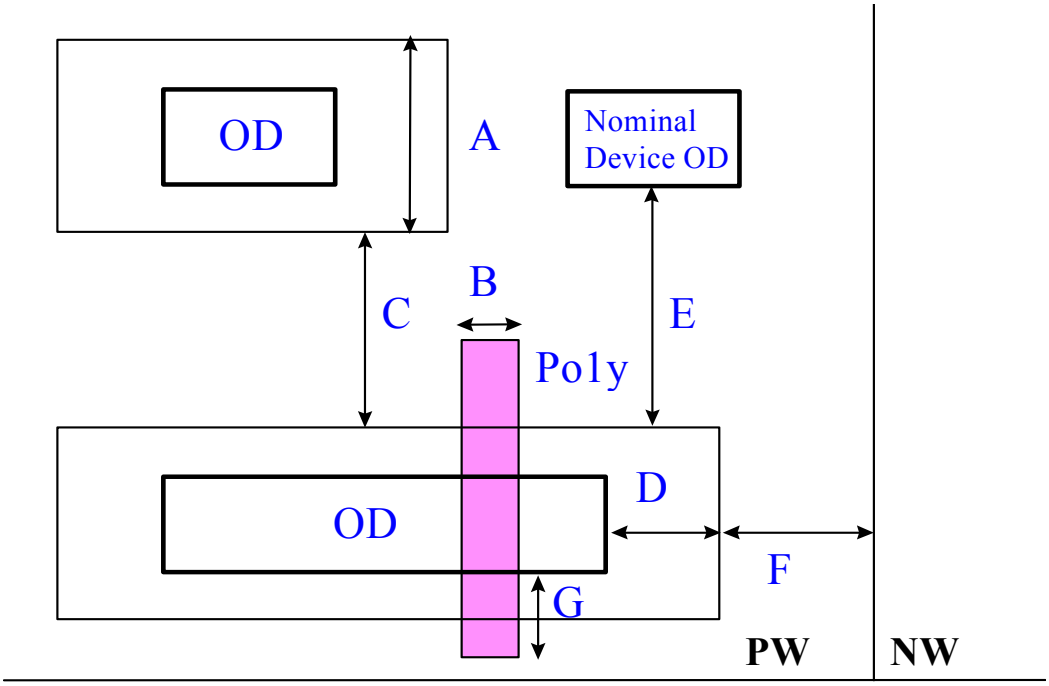

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❑ Thin Oxide Rule (120)

Rule No.	Description	Label		Layout Rule
Layer :	OD --- Thin Oxide Definition			
OD.W.1	Minimum width of an OD region to define the width of NMOS/PMOS	A	≧	0.220 um
OD.W.2	Minimum width of an OD region for interconnect (N+/or P+)	B	≧	0.220 um
OD.S.1	Minimum space between two OD regions (both regions are either inside or outside a N-well) which can be either N+ to N+, P+ to P+ or N+ to P+	C	≧	0.280 um
OD.C.1	Minimum clearance from NW edge to a N+OD region which is inside the NW	D	≧	0.120 um
OD.C.2	Minimum clearance from NW edge to a N+OD region which is outside a cold NW	E	≧	0.430 um
OD.C.3	Minimum clearance from NW edge to a N+OD region which is outside a hot NW	E’	≧	0.430 um
OD.C.4	Minimum clearance from NW edge to a P+OD region which is inside a NW	F	≧	0.430 um
OD.C.5	Minimum clearance from NW edge to a P+OD region (for PW pick up) which is outside a NW	G	≧	0.120 um
OD.C.6	Minimum clearance from poly edge to the edge of butted diffusion OD region	H	≧	0.320 um
OD.S.2	Minimum space of N+ OD to P+ OD for butted diffusion.	I	≧	0.000 um
OD.W.3	a) Width (J) of at lease one segment of the consecutive N+/P+ butted diffusion OD ≥ 0.42um. b) When J < 0.42um, length (T) of OD (source) interact with N+/P+ butted diffusion OD ≤ 0.8um.	J,T		
OD.A.1	Minimum area of a stand-along OD region		≧	0.202 um^2

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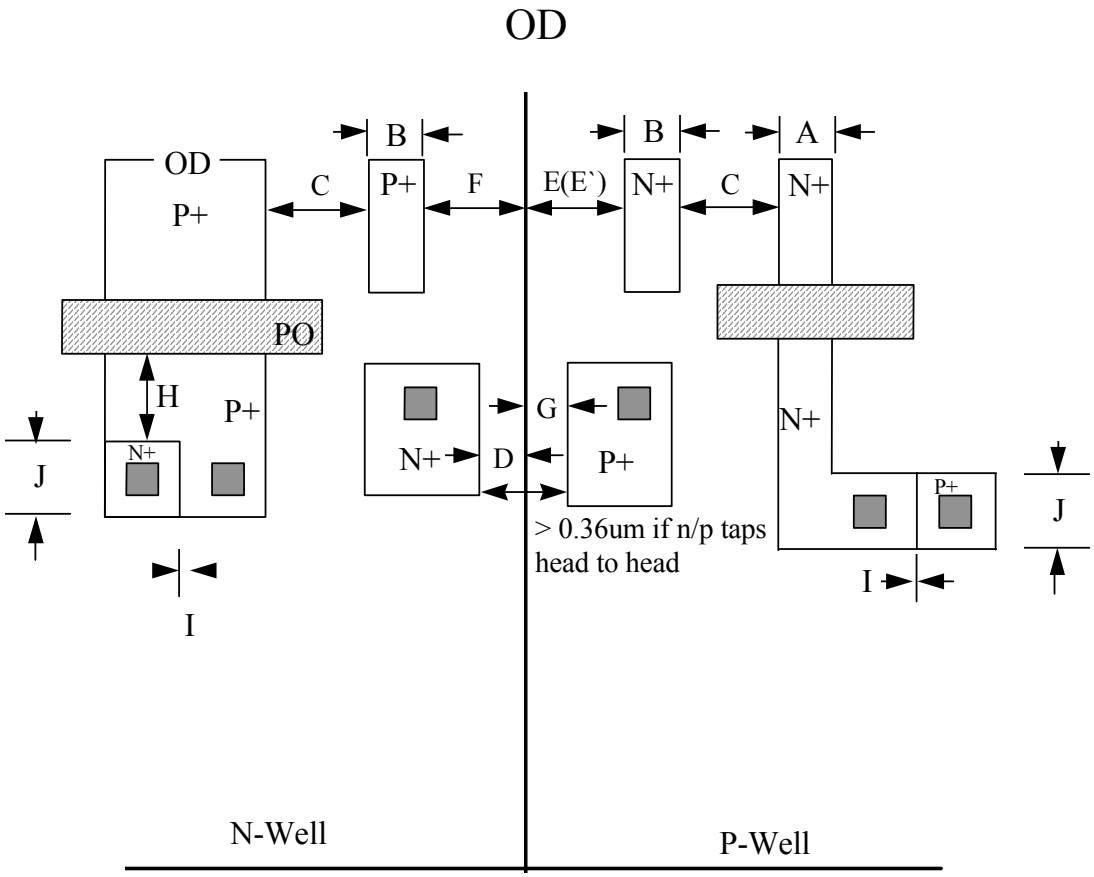
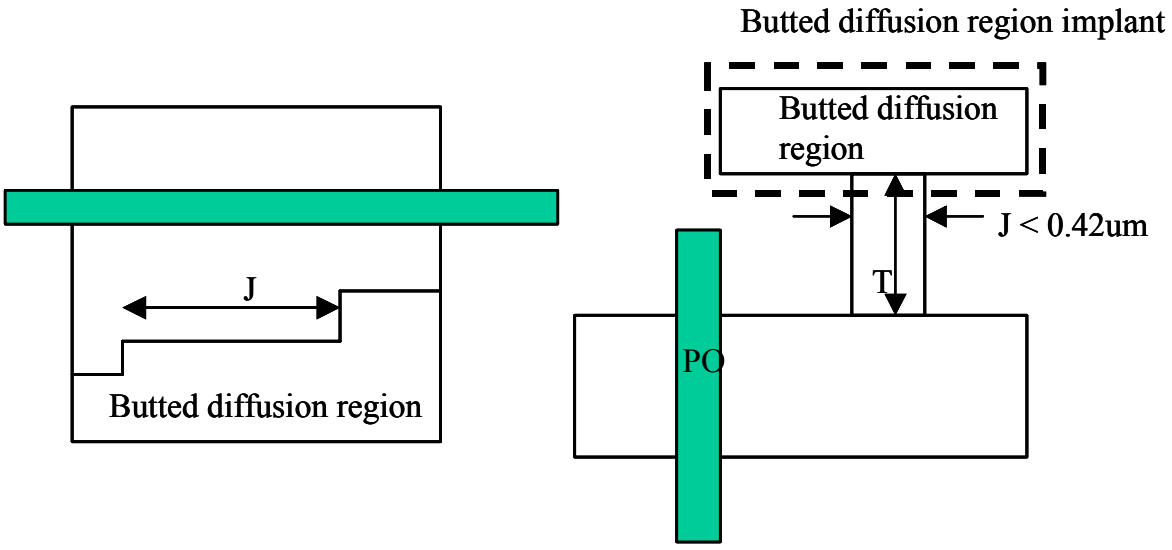
Note: If N-well and P-well pick-ups are put head-to-head each other across well boundary, spacing between N-pickup OD and P-pickup OD will be 0.36 µm to meet implant layout rules (please refer to correct and incorrect layouts in next page)





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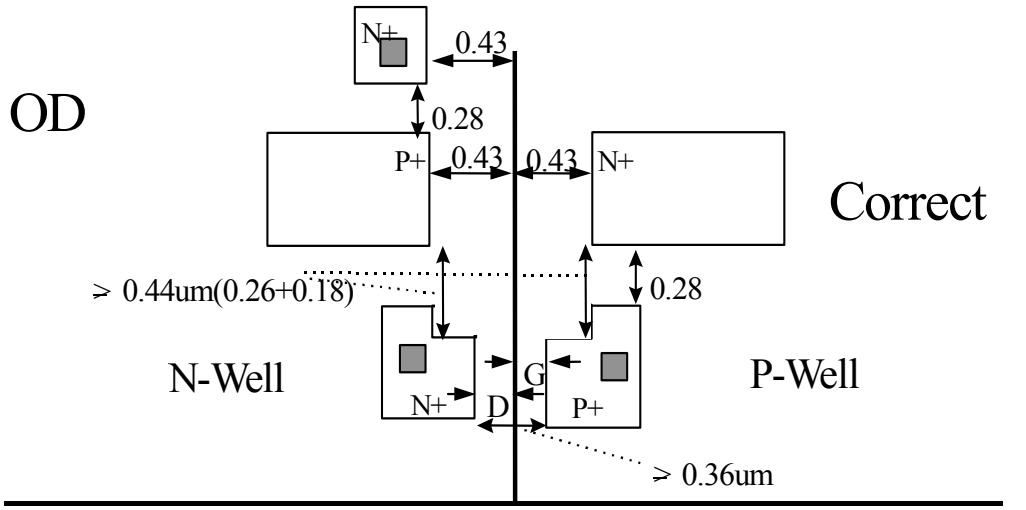

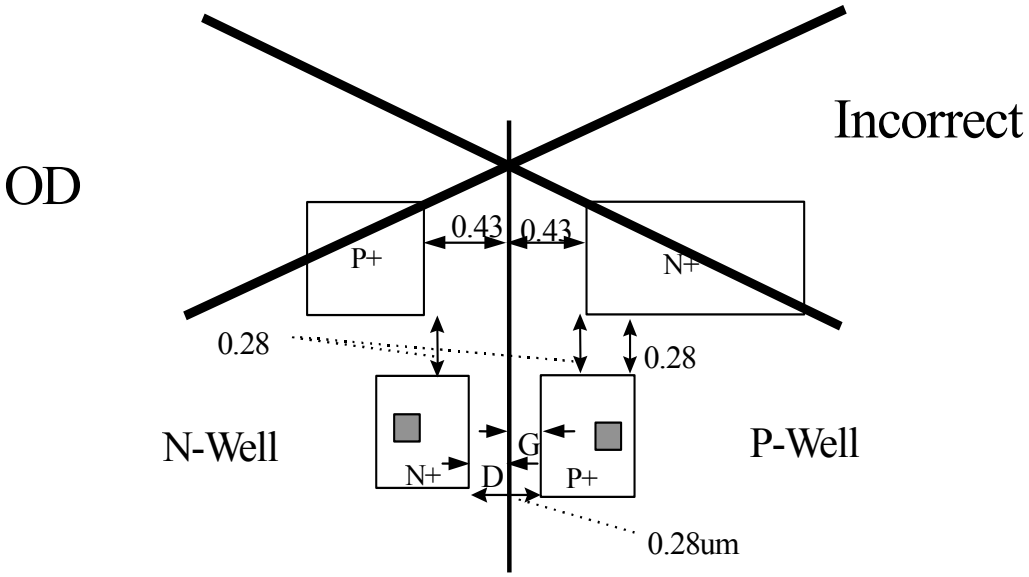

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Thick Oxide Rule (132)

Rule No.	Description	Label		Layout Rule
Layer :	OD2 --- Thick Oxide Definition This layer is used to define 3.3V transistor (NMOS and PMOS)			
OD2.E.1	Minimum extension of an OD2 region beyond an active OD region	A	≧	0.320 um
OD2.S.1	Minimum space between two OD2 regions. Merge if the space is less than 0.450 um.	B	≧	0.450 um
OD2.C.1	Minimum clearance between active OD region and OD2 region	C	≧	0.320 um
OD2.C.2	Minimum clearance between OD2 region and 1.8V transistor gate poly.	D	≧	0.400 um
OD2.E.2	Minimum extension of OD2 region beyond 3.3 V transistor gate poly. (OD2 cut poly GATE is not allowed. Please refer to the attached figure in this section.)	E	≧	0.400 um

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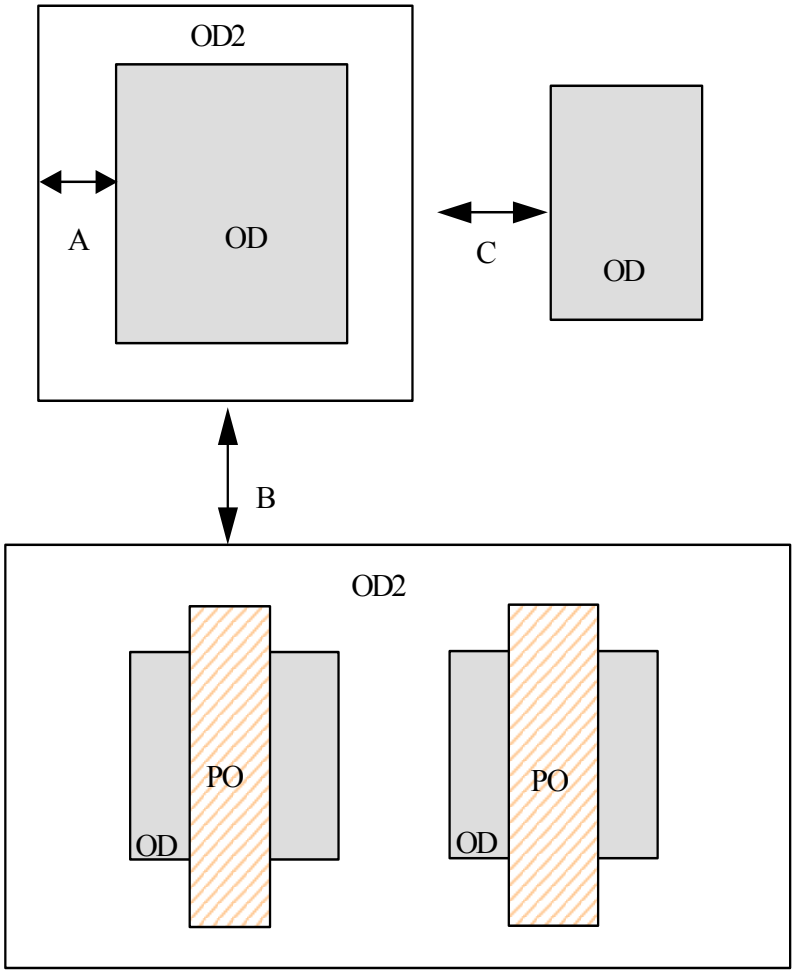
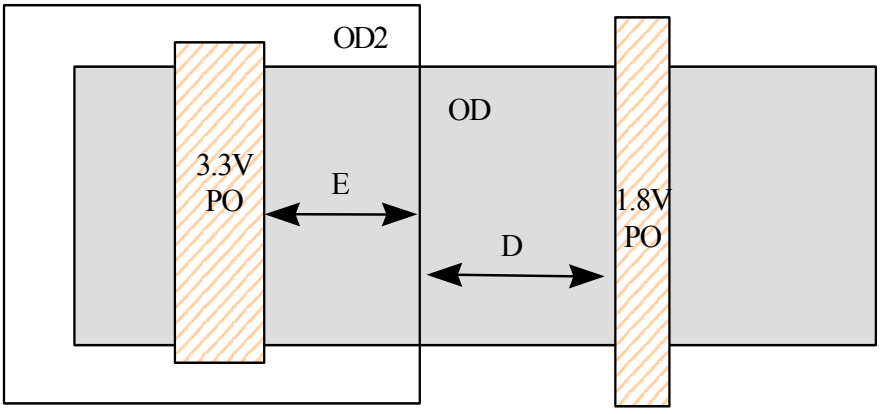
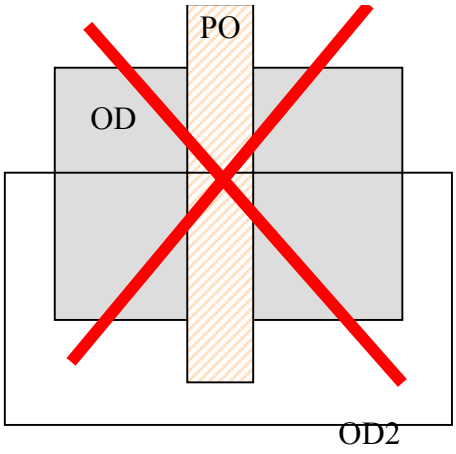
OD2



OD2 cut gate is NOT allowed.





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Poly Rule (130)

All the un-doped poly region will be converted into P+ or N+ doped poly by logic operation at TSMC (please refer to TA-10A5-6101.) If un-doped poly is to be reserved intentionally in your circuit design, please use a dummy layer to define this region and contact our product engineer.

Rule No.	Description	Label		Layout Rule
Layer :	PO --- Poly Si			
PO.W.1	Minimum width of a PO region for the channel length of 1.8V PMOS	A	≧	0.180 um
	Minimum width of a PO region for the channel length of 3.3V PMOS	A1	≧	0.300 um
PO.W.2	Minimum width of a PO region for the channel length of 1.8V NMOS	B	≧	0.180 um
	Minimum width of a PO region for the channel length of 3.3V NMOS	B1	≧	0.350 um
PO.W.3	Minimum width of a PO region for interconnect.	C	≧	0.180 um
PO.S.1	Minimum space between two PO regions on OD area with contacts (including butting contact) in the spacing.	D	≧	0.375 um
PO.S.2	Minimum space between two PO regions on OD area without contacts (including butting contact) in the spacing.	D1	≧	0.250 um
PO.S.3	Minimum space between two PO regions on field oxide area.	D2	≧	0.250 um
PO.C.1	Minimum clearance from an OD region to an PO on field oxide.	E	≧	0.100 um
PO.C.2	Minimum clearance from an OD region to a related PO inside OD	F	≧	0.320 um
PO.O.1	Minimum overlap of a PO region extended into field oxide (endcap)	G	≧	0.220 um

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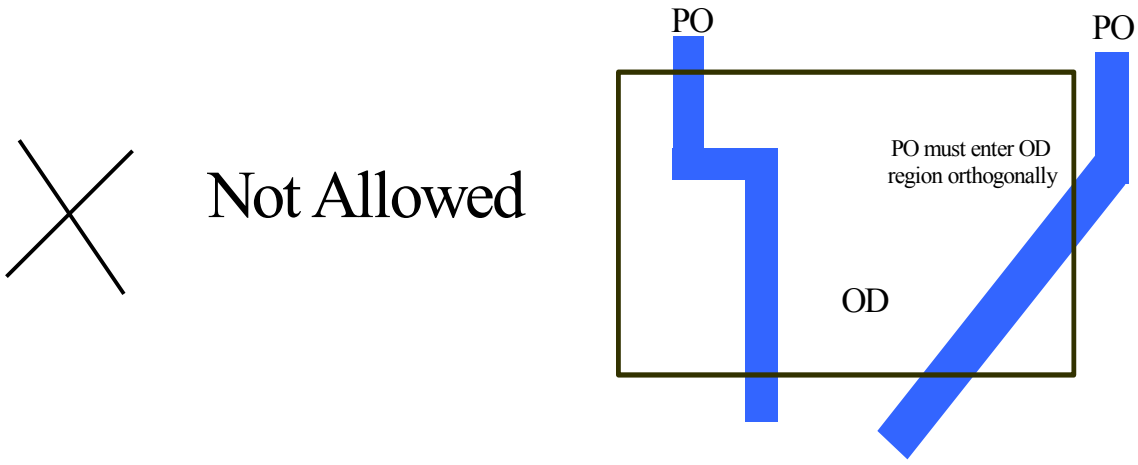
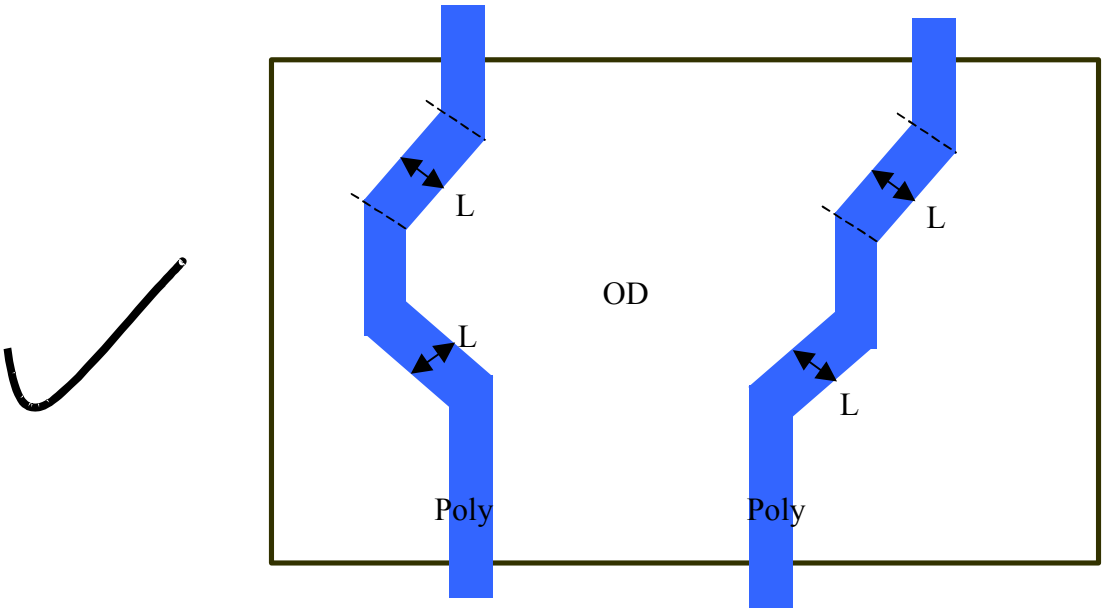
PO.R.1 A) Below poly bent layouts are not allowed



(B) Minimum channel length of 1.8V NMOS and
PMOS 45° poly bent layout
L ≥ 0.21 um.



PO.R.2 Maximum length of salicide poly on STI between two contacts or between one contact and poly line end when poly width ≤ 0.24um H ≦ 50 um

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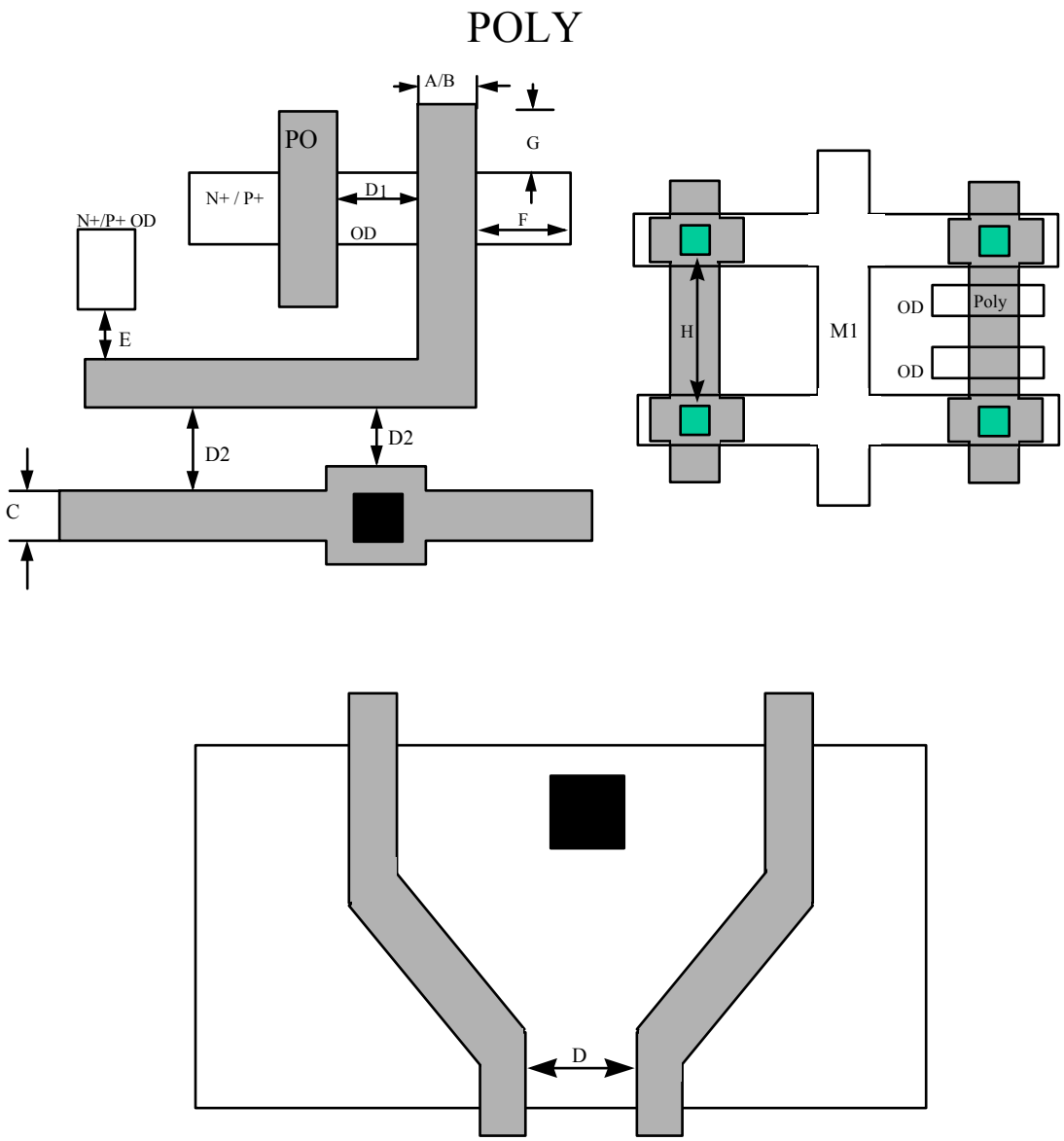
PO.R.3 Minimum poly density across full chip. ≧ 14%

1. It is recommended to use TSMC's auto-fill utilities (Document No.: T-018-LO-DR-001-C2) to add dummy PO if poly density is less than 14%.

2. Please be aware of the coupling capacitor effect while dummy PO are added.



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❑ Poly Resistor and OD Resistor Guideline

1. The total resistance of the resistor is calculated based on the equation and data listed in SPICE model document (T-018-LO-SP-001).

2. For poly resistor, it is strongly recommended that the resistor width ≥ 1.0 μm and the resistor square number N_{sq} ≥ 5. For OD resistor, it is strongly recommended that the resistor width ≥ 2.0 μm and the resistor square number N_{sq} ≥ 5.

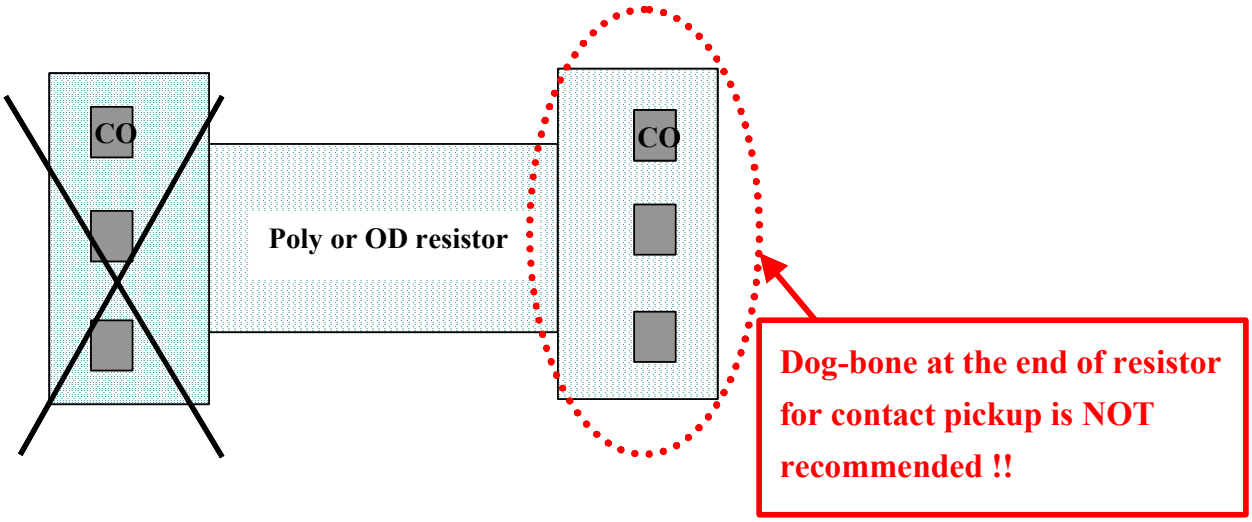
3. The sheet resistance in SPICE model of non-salicided N+/P+ PO/OD resistors is resulted from N2V/NP and P2V/PP combinations, respectively. To obtain precise resistance, dummy layers (DMN2V & DMP2V) are required. If N2V/P2V/N3V/P3V are derived from logical operation, please ensure correct implants in case the resistor traverses NW/PW or 1.8V/3.3V. The dummy layers should follow the implant design rules related to poly resistor shown below.

4. It is strongly recommended that the clearance from an RPO to a contact on the PO or OD resistor must be equal to 0.22μm.

5. It is strongly recommended that the minimum clearance of the resistor to un-related implant regions be 0.26μm.

6. It is strongly recommended that contact pickup of the resistor should be in a single column.

7. It is strongly recommended not to use dog-bone at the end of the poly or OD resistor for contact pickup.



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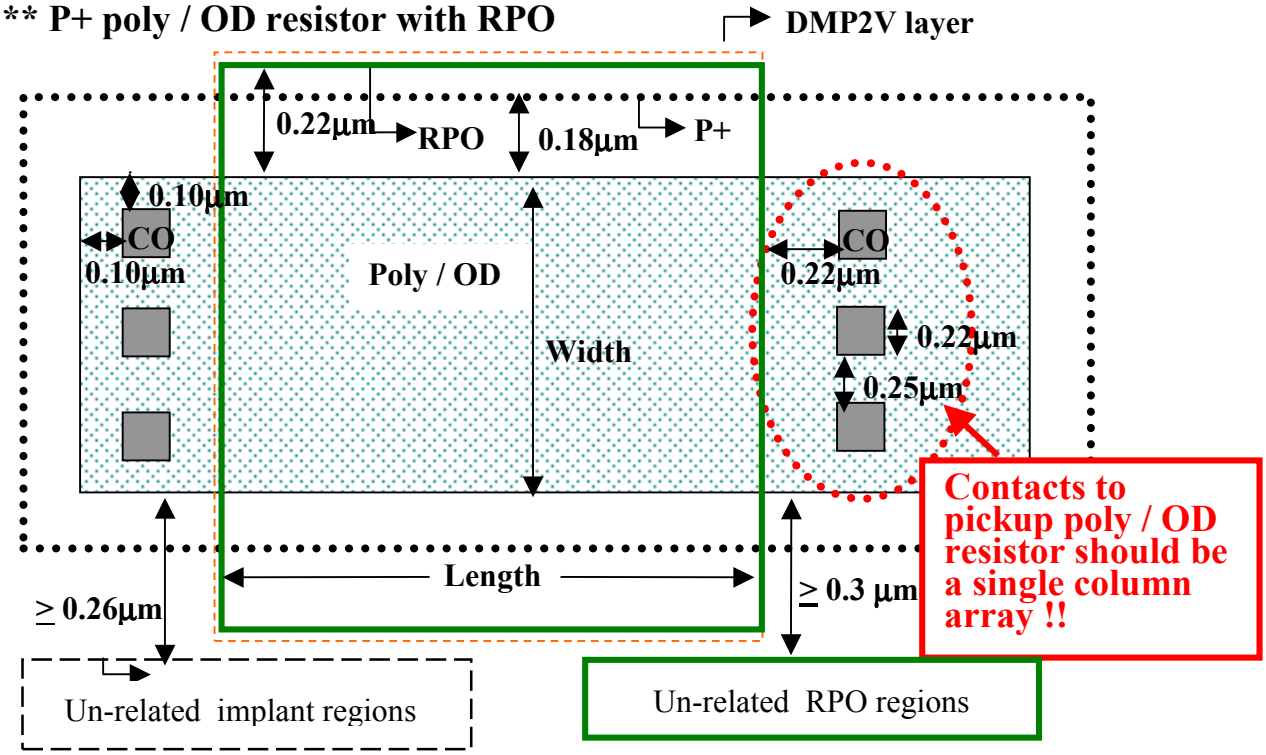
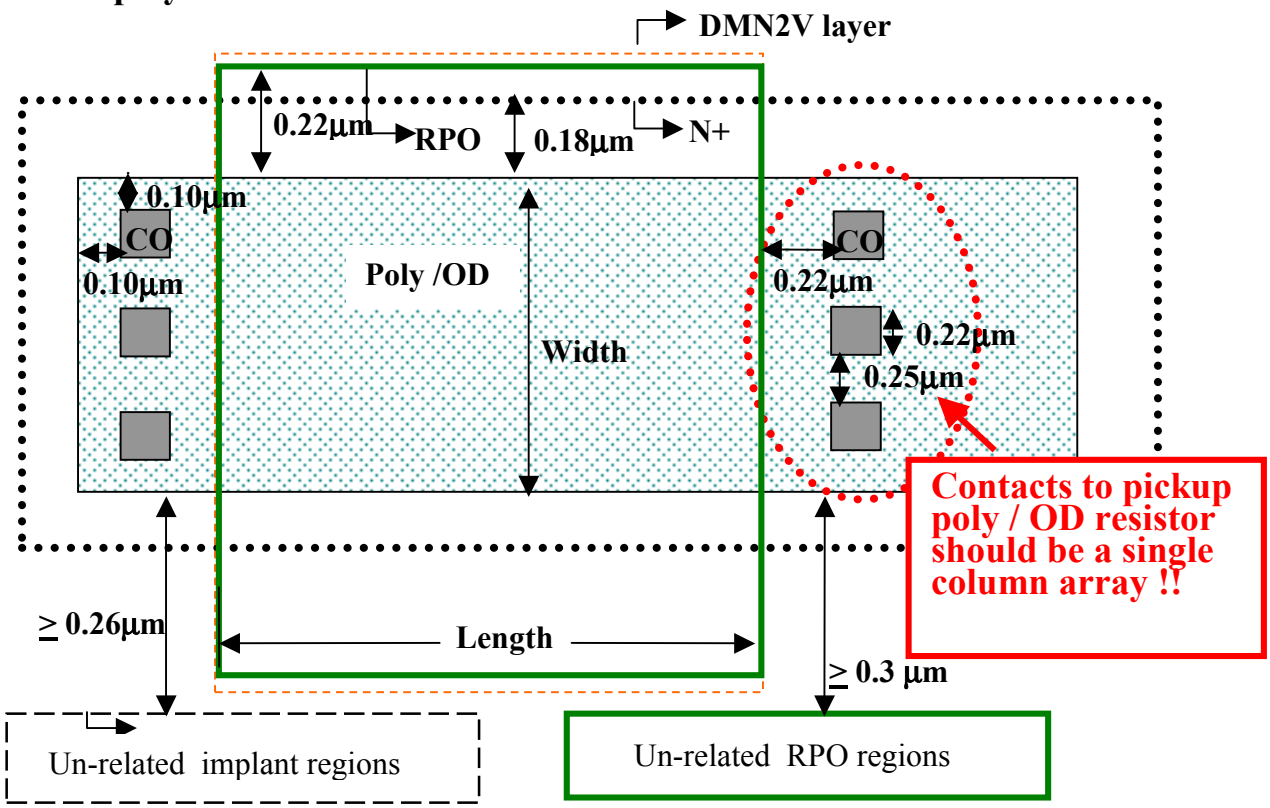
** P+ poly / OD resistor with RPO



** N+ poly / OD resistor with RPO



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N+ S/D Rule (198)

Rule No.	Description	Label		Layout Rule
Layer :	NP --- N+ S/D Implantation			
NP.W.1	Minimum width of a NP region	A	≧	0.440 um
NP.S.1	Minimum space between two NP regions. Merge if the space is less than 0.440 um	B	≧	0.440 um
NP.C.1	Minimum clearance from a NP region to a P+ active OD region (inside N-well)	C	≧	0.260 um
NP.C.2	Minimum clearance from a NP region to a non-butted edge of P-well pick-up P+OD region if the distance between P+OD and N-well ≥ 0.43um.	C1	≧	0.100 um
NP.C.3	Minimum clearance from a NP region to a non-butted edge of P-well pick-up P+OD region if the distance between P+OD and N-well < 0.43um.	C2	≧	0.180 um
NP.C.4	Minimum clearance from a NP edge to a P-Channel PO gate. This rule must extend out of gate in the direction of PO by 0.35um. The equivalent P-Channel area must not be covered with NP: ((((PO AND OD) SIZING 0.03) AND PO) SIZING 0.32)	D	≧	0.320 um
NP.C.5	Minimum clearance from a NP edge to a N-Channel PO gate. This rule must extend out of gate in the direction of PO by 0.35um. The equivalent N-Channel area must be covered with NP: ((((PO AND OD) SIZING 0.03) AND PO) SIZING 0.32)	E	≧	0.320 um
NP.O.1	Minimum overlap from a NP edge to an OD region	F	≧	0.230 um
NP.E.1	Minimum extension of a NP region beyond a N+ active OD region	G	≧	0.180 um
NP.E.3	Minimum extension of a NP region beyond a N-well pick-up N+OD region if the distance between N+OD and P-well ≥ 0.43um.	H	≧	0.020 um

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NP.E.4	Minimum extension of a NP region beyond a N-well pick-up N+OD region if the distance between N+OD and P-well < 0.43 um. To follow this rule and NP.C.1 simultaneously, N+ tap OD to P+ active OD minimum spacing must increase up to 0.44um. To follow this rule and NP.C.3 simultaneously, N+ tap OD to P+ tap OD minimum spacing must increase up to 0.36 um.	H1	≧	0.180 um
NP.C.6	Clearance from a NP region to the butted edge of a butted diffusion P+ OD (inside P-well)	I	=	0.000 um
NP.E.5	Minimum extension of a NP region along the edge of a butted diffusion N+OD/P+OD	H2	≧	0.000 um
NP.A.1	Minimum area of NP region		≧	0.3844 um^2
NP.E.6	Minimum extension of NP region beyond a PO as a resistor. PRO PO without NP or PP implant is not allowed.	L	≧	0.18 um
NP.R.1	NP overlapped with PP is not allowed			
NP.R.2	It is prohibited that NP is generated by reverse tone of PP, since this operation might violate NP.C.1 and NP.C.2			
NP.R.3	OD must be fully covered by {NP OR PP} except: a) OD without interacting {CO OR PO} b) NW resistor			

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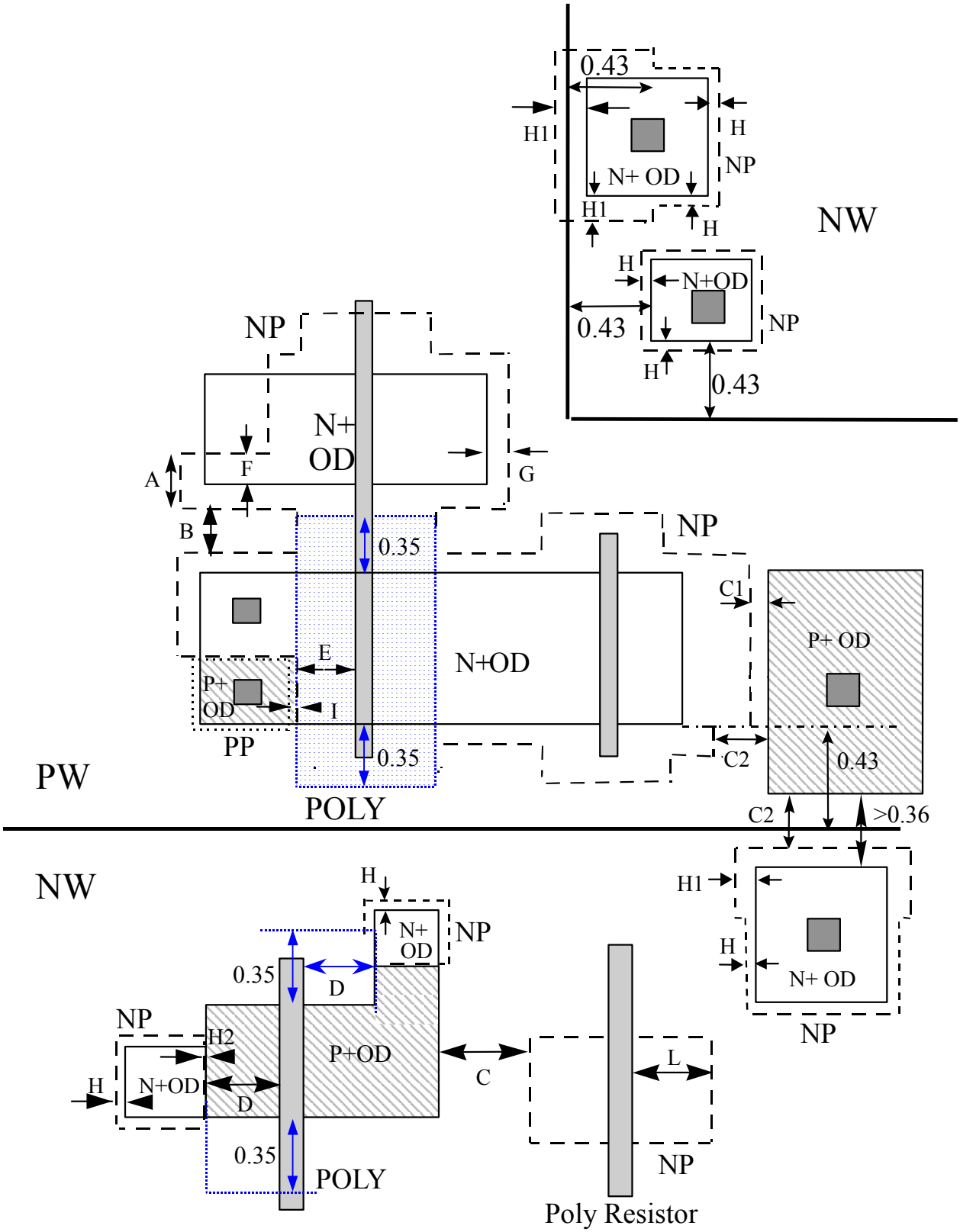

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P+ S/D Rule (197)

Rule No.	Description	Label		Layout Rule
Layer :	PP --- P+ S/D Implantation			
PP.W.1	Minimum width of a PP region	A	≧	0.440 um
PP.S.1	Minimum space between two PP regions. Merge if the space is less than 0.440 um	B	≧	0.440 um
PP.C.1	Minimum clearance from a PP region to a N+ active OD region (inside P-well)	C	≧	0.260 um
PP.C.2	Minimum clearance from a PP region to a non-butted edge of N-well pick-up N+OD region if the distance between N+OD and P-well ≥ 0.43um.	C1	≧	0.100 um
PP.C.3	Minimum clearance from a PP region to a non-butted edge of N-well pick-up N+OD region if the distance between N+OD and P-well < 0.43um.	C2	≧	0.180 um
PP.C.4	Minimum clearance from a PP edge to a N-Channel PO gate. This rule must extend out of gate in the direction of PO by 0.35um. The equivalent N-Channel area must not be covered with PP: ((((PO AND OD) SIZING 0.03) AND PO) SIZING 0.32)	D	≧	0.320 um
PP.C.5	Minimum clearance from a PP edge to a P-Channel PO gate. This rule must extend out of gate in the direction of PO by 0.35um. The equivalent P-Channel area must be covered with PP: ((((PO AND OD) SIZING 0.03) AND PO) SIZING 0.32)	E	≧	0.320 um
PP.O.1	Minimum overlap from a PP edge to an OD region	F	≧	0.230 um
PP.E.1	Minimum extension of a PP region beyond a P+ active OD region	G	≧	0.180 um
PP.E.3	Minimum extension of a PP region beyond a P-well pick-up P+OD region if the distance between P+OD and N-well ≥ 0.43um.	H	≧	0.020 um

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PP.E.4	Minimum extension of a PP region beyond a P-well pick-up P+OD region if the distance between P+OD and N-well < 0.43 um. To follow this rule and PP.C.1 simultaneously, P+ tap OD to N+ active OD minimum spacing must increase up to 0.44um. To follow this rule and PP.C.3 simultaneously, P+ tap OD to N+ tap OD minimum spacing must increase up to 0.36 um.	H1	≧	0.180 um
PP.C.6	Clearance from a PP region to the butted edge of a butted diffusion N+ OD (inside N-well)	I	=	0.000 um
PP.E.5	Minimum extension of a PP region along the edge of a butted diffusion P+OD/N+OD	H2	≧	0.000 um
PP.A.1	Minimum area of PP region		≧	0.3844 um^2
PP.E.6	Minimum extension of PP region beyond a PO as a resistor. RPO PO without NP or PP implant is not allowed.	L	≧	0.18 um
PP.R.1	PP overlapped with NP is not allowed			
PP.R.2	It is prohibited that PP is generated by reverse tone of NP, since this operation might violate PP.C.1, and PP.C.2			
PP.R.3	OD must be fully covered by {NP OR PP} except a) OD without interacting {CO OR PO} b) NW resistor			

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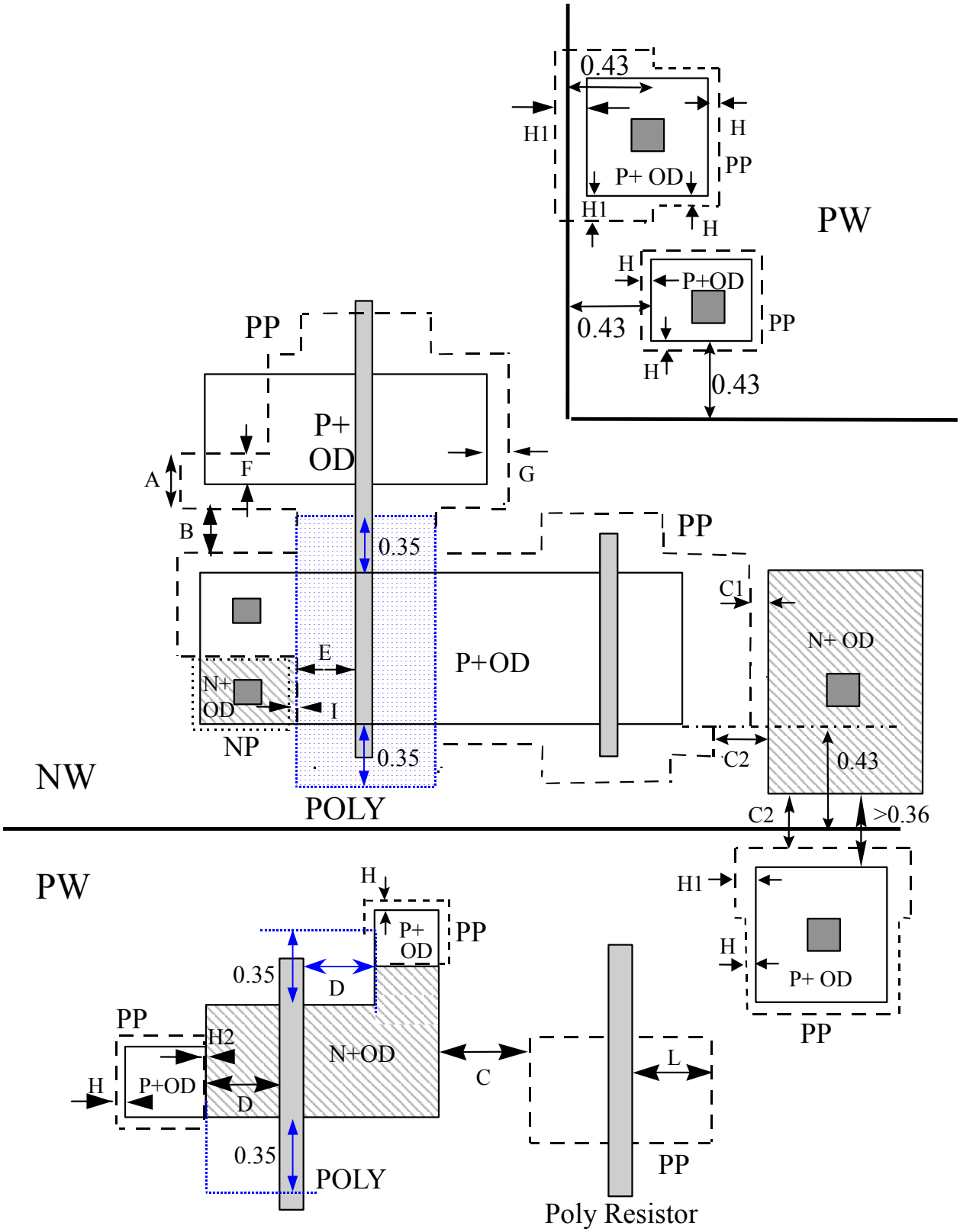

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Resist Protection Oxide Rule (155)

Rule No.	Description	Label		Layout Rule
Layer :	RPO --- Non-Salicide Area Definition			
RPO.W.1	Minimum RPO width	A	≧	0.430 um
RPO.S.1	Minimum RPO spacing	B	≧	0.430 um
RPO.C.1	Minimum clearance from RPO to unrelated OD	C	≧	0.220 um
RPO.C.2	Minimum clearance from RPO to CO	D	≧	0.220 um
RPO.C.3	Minimum clearance from RPO to Poly on OD	E	≧	0.450 um
RPO.C.4	Minimum clearance from RPO to related OD (RPO fully inside OD is not allowed)	F	≧	0.220 um
RPO.E.1	Minimum extension of OD to RPO	G	≧	0.220 um
RPO.C.5	Minimum extension of RPO to Poly resistor on field oxide (RPO fully inside PO is not allowed)	H	≧	0.220 um
RPO.C.6	Minimum clearance of RPO to unrelated Poly on field oxide	I	≧	0.300 um
RPO.A.1	Minimum area of RPO		≧	2 um^2
	(Below items are referred from the ESD Section)			
ESD.5x	NMOS and PMOS of I/O buffer should have a non-salicide area on drain side, that is RPO mask should block drain side of device (except contact region should keep salicided).			
ESD.5A	For high voltage tolerant I/O designed by 3.3V NMOS: RPO should cover all inactive poly gate and extend to active region (*Poly spacing ≥ 0.25um*). RPO also needs to overlap the active poly gate by 0.05um.			0.05
ESD.5B	For high voltage tolerant I/O designed by 1.8V NMOS: RPO should cover inactive poly gate completely, and the clearance between RPO and active poly gate is 0.45um.			0.25

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ESD.5C	For regular 3.3V I/O in NMOS region: RPO on the drain side needs to overlap poly gate by 0.05um.	0.05
ESD.5E	For all PMOS and regular 1.8V I/O in NMOS region: RPO to poly spacing is 0.45um.	0.45
ESD.5D	For the grounded gate ESD protection device between Vcc/Vss: It is suggested that RPO fully covers the non-contacted poly gate, source/drain. Except the Vcc/Vss protection, the RPO on the source side should be removed, or if used, must follow design rules related to RPO (width, spacing, etc).	
ESD.5F	The minimum width of RPO on drain side (X) and RPO edge to OD edge (Y) for 3.3V NMOS without ESD implant; and 1.8V NMOS High Voltage tolerant (up to 3.3V)..	Y≥X≥ 1.95 um
ESD.5G	The minimum width of RPO on drain side (X) and RPO edge to OD edge (Y) for 1.8V NMOS without ESD implant and 3.3V PMOS and 1.8V PMOS.	Y≥X≥ 1.5 um

*** Please keep contacts be salicided in RPO block area.**
**** If poly resistor is used, please follow poly resistor guideline.**
***** If RPO is used in ESD circuit, please follow ESD guideline.**
****** Except ESD design application, RPO partially intersect OD (or PO) is NOT recommended. It is recommended the RPO must intersect the related OD (or PO) and divide it into two or more regions. (Please see the Fig.1 in this section). If such layouts were still used, please make sure the function of circuit is correct.**

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RPO

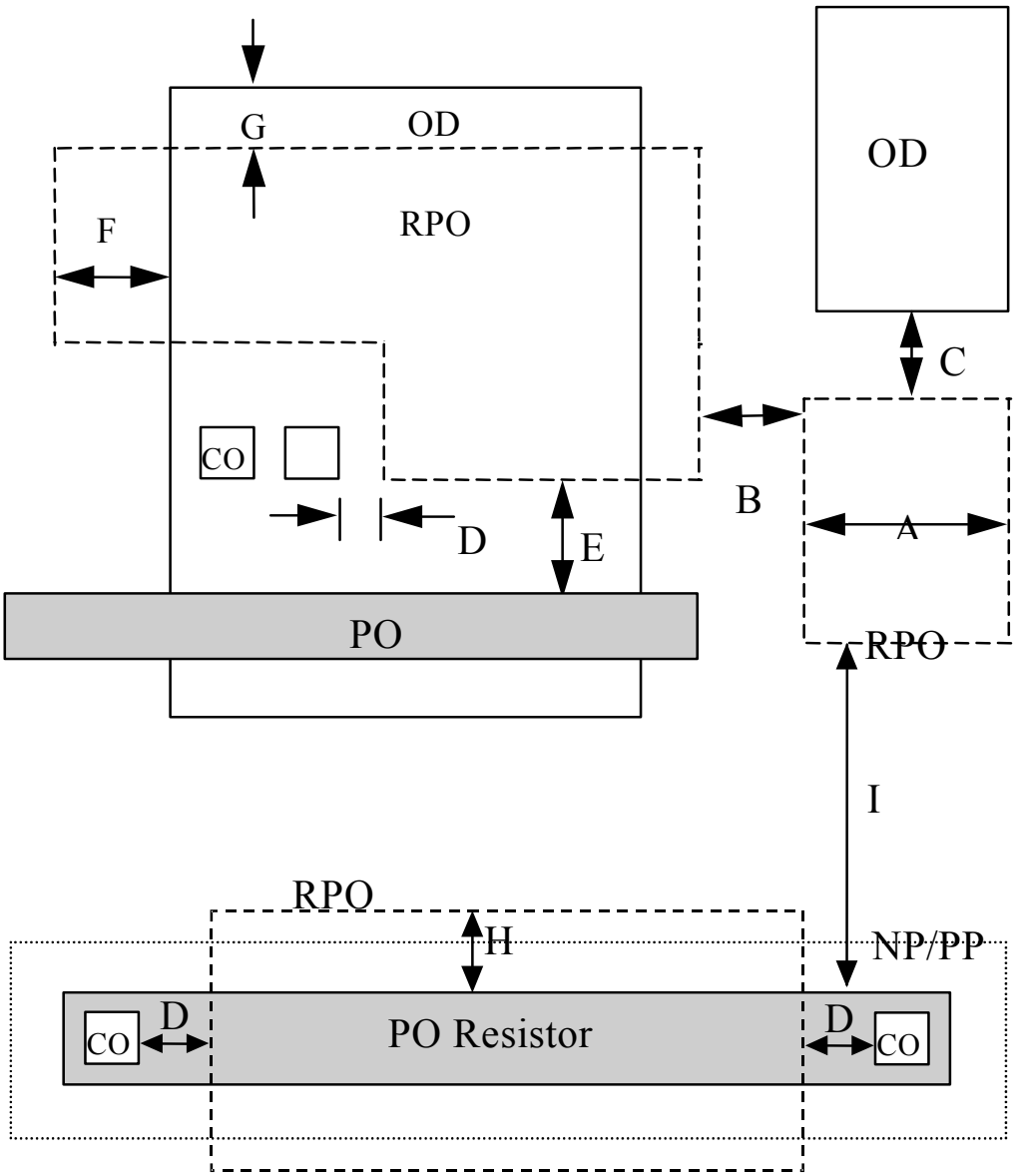
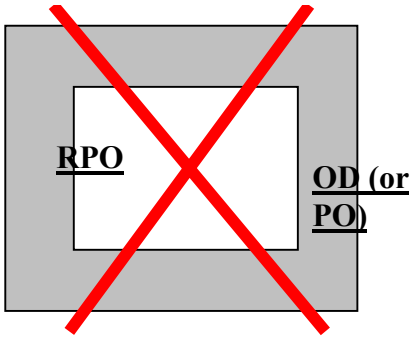
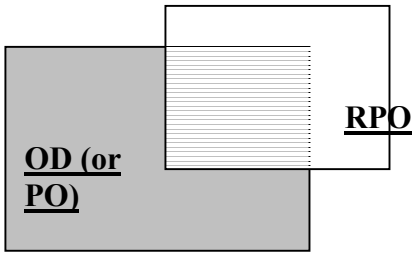
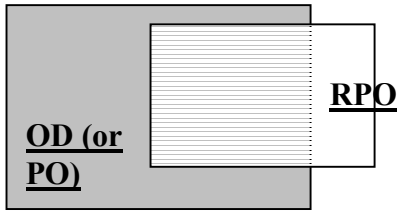


Fig.1 RPO partially intersect OD (or PO) is NOT recommended.

RPO.C.4 & RPO.C.5:
RPO fully inside OD (or PO) is NOT allowed.







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Contact Rule (156)

Rule No.	Description	Label		Layout Rule
Layer :	CO --- Contact Window			
CO.W.1	Minimum and maximum width of a CO region	A	=	0.220 um
CO.S.1	Minimum space between two CO regions	B	≧	0.250 um
CO.S.2	Minimum space between two CO regions in a contact array with both row and column numbers equal to or larger than 4. As shown in shaded area, two contact regions within 0.3 um distance is considered to be in the same array. (ex. 2×8, 3×3, 3×8 use B, and 4×4, 4×5, 4×8 use B1)	B1	≧	0.280 um
CO.C.1	Minimum clearance from a CO on OD region to a PO gate	C	≧	0.160 um
CO.C.2	Minimum clearance from a CO on PO region to an OD region	D	≧	0.200 um
CO.E.1	Minimum extension of an OD region beyond a OD CO region.	E	≧	0.100 um
CO.E.2	Minimum extension of a PO region beyond a Poly CO region.	F	≧	0.100 um
CO.E.3	Minimum extension of a PP region beyond a OD CO region.	G	≧	0.120 um
CO.E.4	Minimum extension of a NP region beyond a OD CO region.	H	≧	0.120 um
CO.R.1	CO on gate region is forbidden			
CO.R.2	OD Contact sitting on NP/PP boundary is not allowed.			
CO.R.3	Non-salicided contacts are not allowed			
	(Below item is referred from the ESD Section)			
ESD.6	The minimum clearance of poly edge to CO edge on source side for NMOS and PMOS	Z	≧	0.75 um

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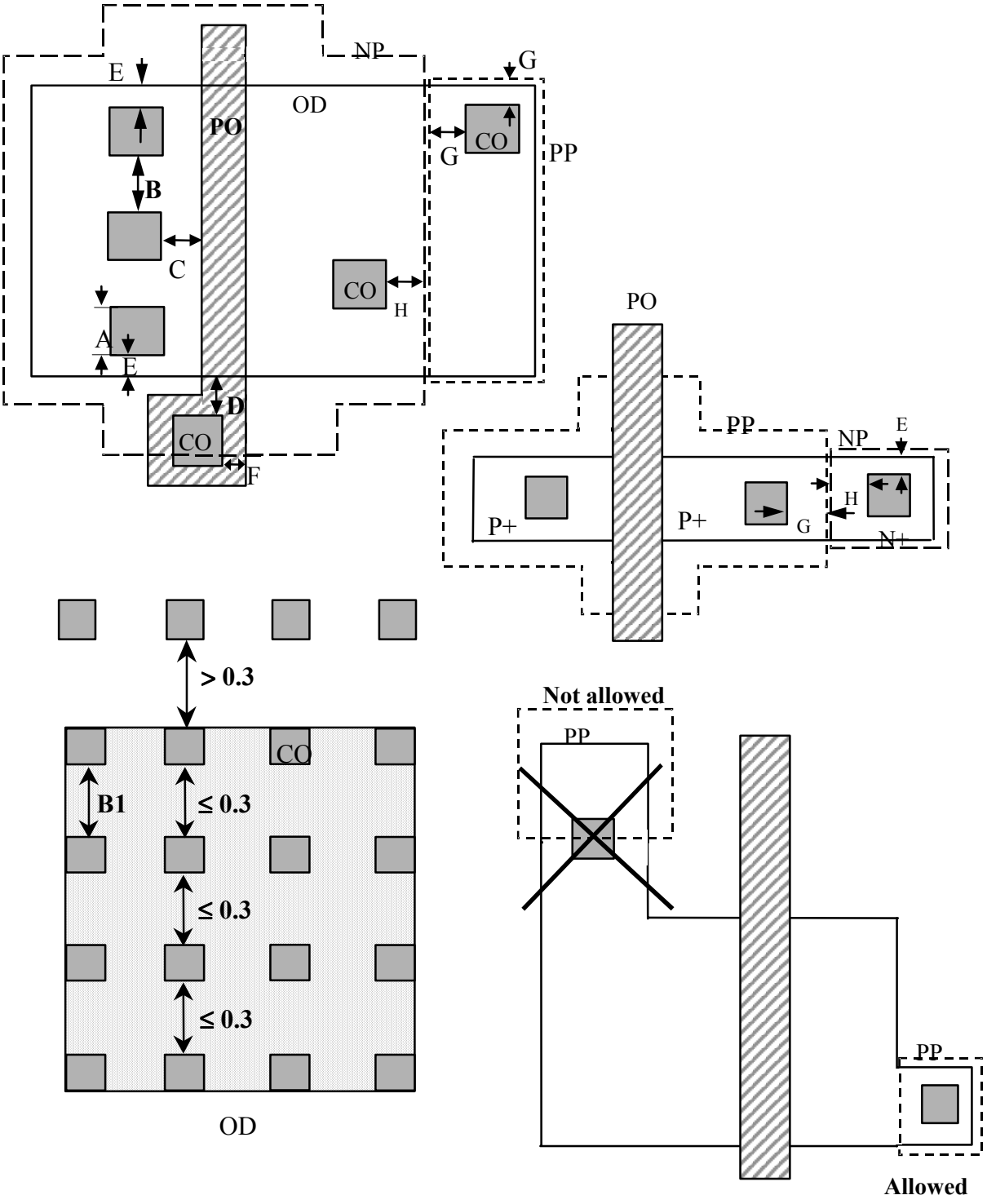
CO



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Metal 1 Rule (160)

Rule No.	Description	Label		Layout Rule
Layer :	M1 --- Metal 1			
M1.W.1	Minimum width of M1 region	A	≧	0.230 um
M1.S.1	Minimum space between two M1 regions	B	≧	0.230 um
M1.E.1	Minimum extension of M1 region beyond CO region	C	≧	0.005 um
M1.E.2.	Minimum extension of M1 end-of-line region beyond CO region. For CO located at the 90 degree corner, at least one side of metal extension must be treated as end-of-line and another side can follow M1.E.1 (see next page)	C1	≧	0.060 um
M1.S.2	Minimum space between metal lines with one or both metal line width and length are greater than 10um; the minimum space must be maintained between a metal line and a small piece of metal (<10um) that is connected to the wide metal within 1.0 um range from the wide metal.	D	≧	0.600 um
M1.A.1	Minimum area of M1 region	E	≧	0.202 um^2
M1.R.1	Minimum density of M1 across full chip. Density is calculated as Total metal layout area/chip area. It is recommended to use TSMC's auto-fill utilities (Document No.: T-018-LO-DR-001-C3) to add dummy metal if M1 density is less than 30%.		≧	30 %

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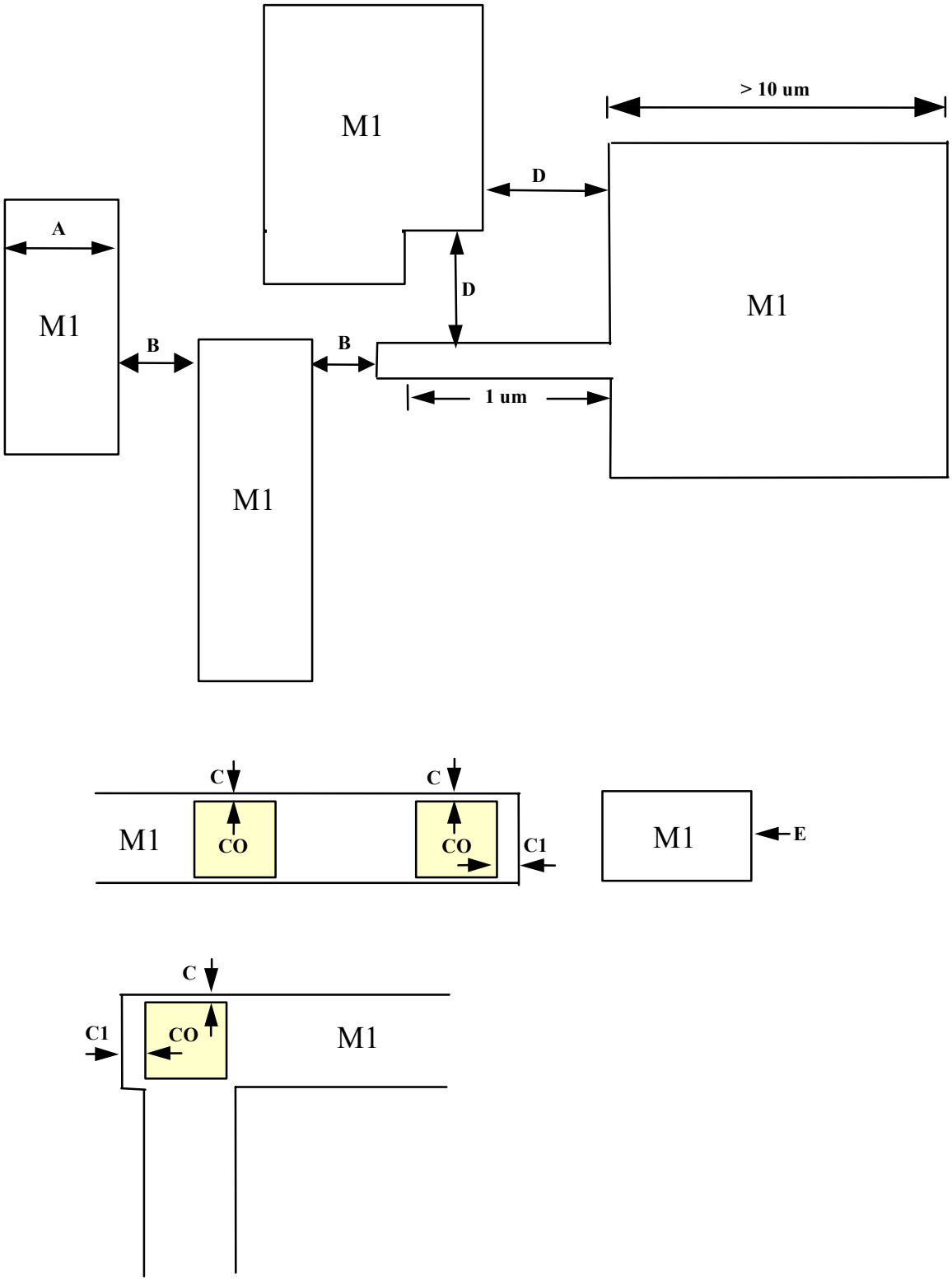

METAL 1

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❑ Via x (x=1,2,3,4) Rule (178,179,173,174)

Rule No.	Description	Label		Layout Rule
Layer :	VIAx --- Via x Hole			
VIAx.0	VIAx can be located at any region			
VIAx.W.1	Minimum and maximum width of VIAx region	A	=	0.260 um
VIAx.S.1	Minimum space between two VIAx regions	B	≧	0.260 um
VIAx.E.1	Minimum extension of Mx region beyond VIAx region.	C	≧	0.010 um
VIAx.E.2	Minimum extension of Mx end-of-line region beyond VIAx region. For VIAx located at the 90 degree corner, at least one side of metal extension must be treated as end-of-line and another side can follow VIAx.E.1 (see next page)	C1	≧	0.060 um
VIAx.C.1	VIAx can be fully or partially stacked on any combination of stacked structure such as stacked VIAx-1../CO.			

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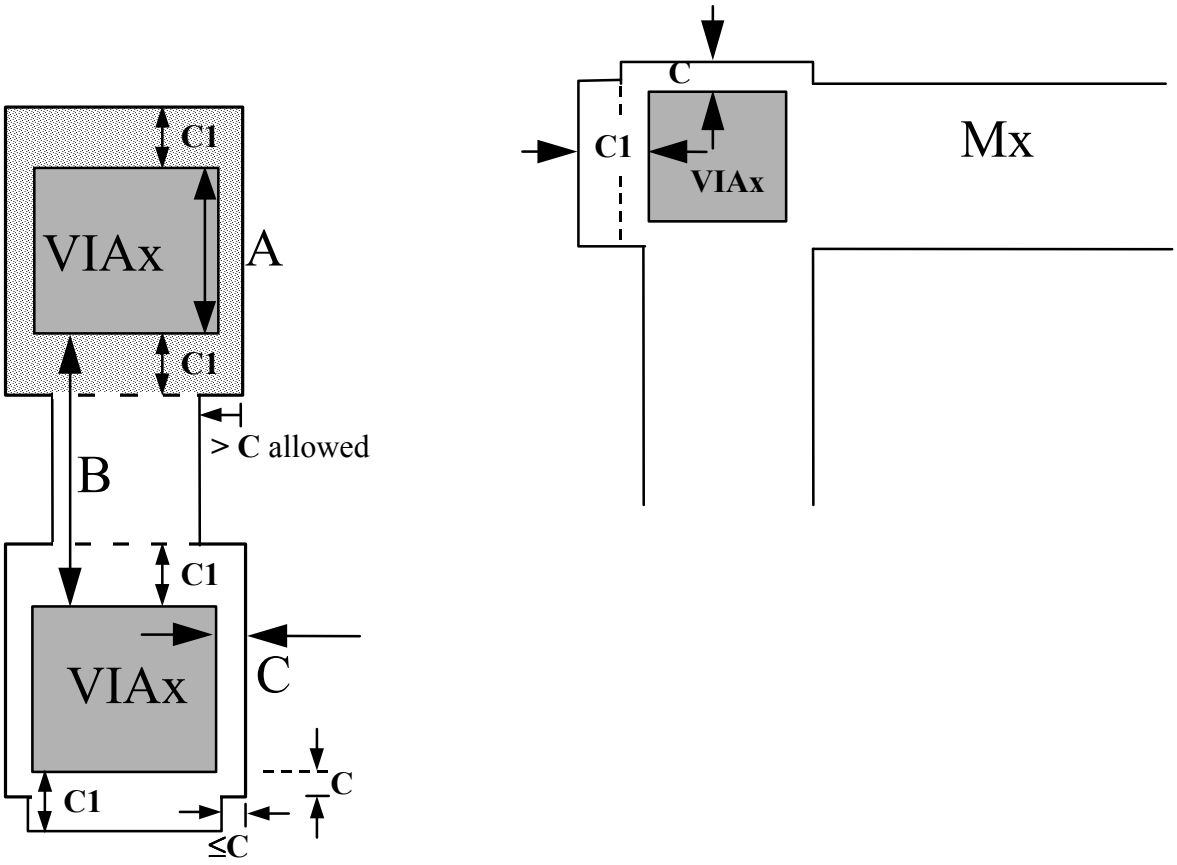
Via x (x=1,2,3,4)



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❑ Metal x (x=2,3,4,5) Rule (180, 181, 184, 185)

Rule No.	Description	Label		Layout Rule
Layer :	Mx --- Metal x			
Mx.W.1	Minimum width of Mx region	A	≧	0.280 um
Mx.S.1	Minimum space between two Mx regions	B	≧	0.280 um
Mx.E.1	Minimum extension of Mx region beyond VIAx-1 region	C	≧	0.010 um
Mx.E.2.	Minimum extension of Mx end-of-line region beyond VIAx-1 region. For VIAx-1 located at the 90 degree corner, at least one side of metal extension must be treated as end-of-line and another side can follow Mx.E.1 (see next page)	C1	≧	0.060 um
Mx.S.2	Minimum space between metal lines with one or both metal line width and length are > 10um; the minimum space must be maintained between a metal line and a small piece of metal (<10um) that is connected to the wide metal within 1.0 um range from the wide metal	D	≧	0.60 um
Mx.A.1	Minimum area of Mx region	E	≧	0.202 um^2
Mx.R.1	Minimum density of Mx across full chip Density is calculated as Total metal layout area/chip area. It is recommended to use TSMC's auto-fill utilities (Document No.: T-018-LO-DR-001-C3) to add dummy metal if Mx density is less than 30%.)		≧	30 %

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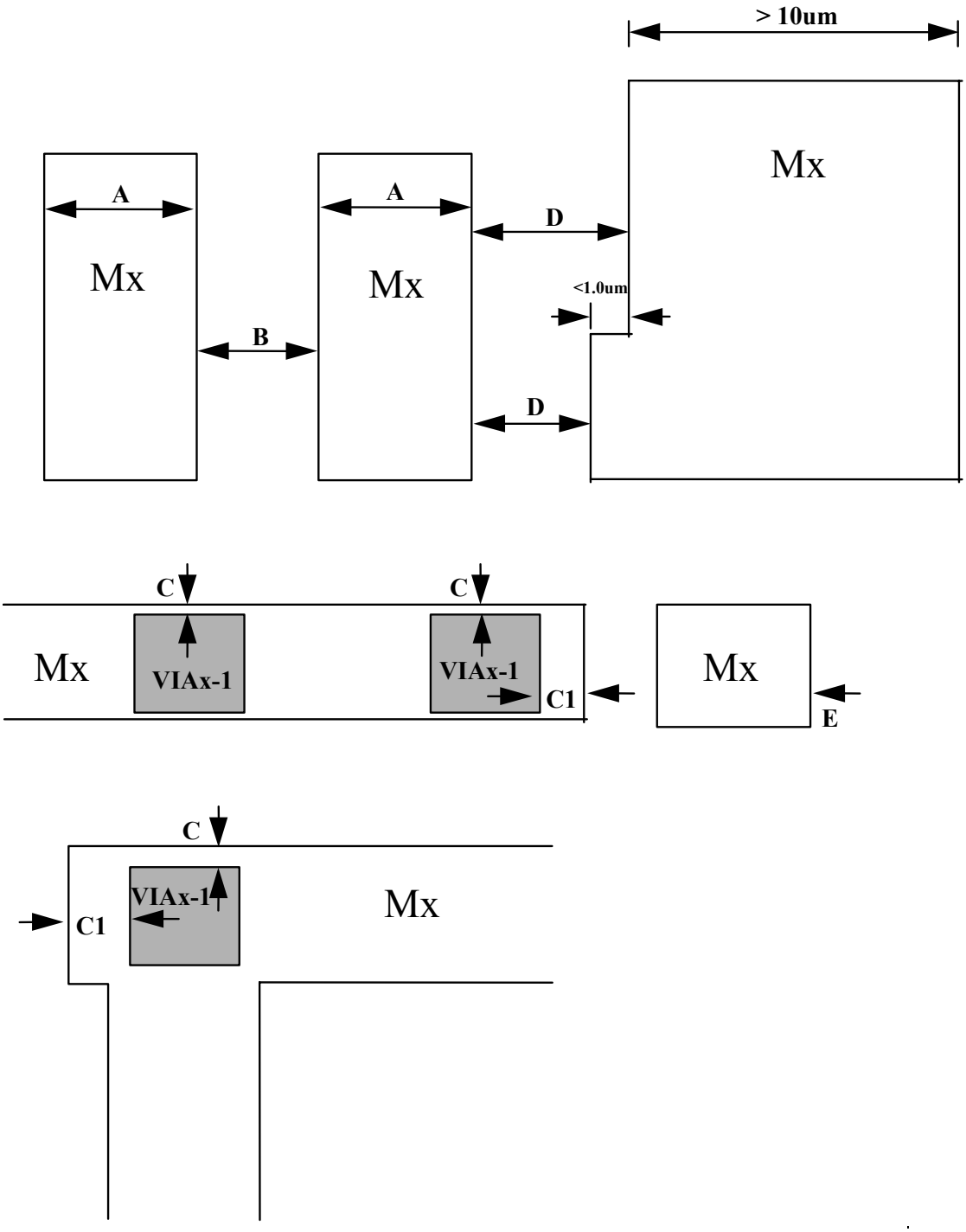

Metal x (x=2,3,4,5)

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Via 5 Rule (175)

Rule No.	Description	Label		Layout Rule
Layer :	VIA5 --- Via 5 Hole			
VIA5.W.1	Minimum and maximum width of VIA5 region	A	=	0.360 um
VIA5.S.1	Minimum space between two VIA5 regions	B	≧	0.350 um
VIA5.E.1	Minimum extension of M5 region beyond a VIA5 region	C	≧	0.010 um
VIA5.E.2	Minimum extension of M5 line-end region beyond VIA5 region For VIA5 located at the 90 degree corner, at least one side of metal extension must be treated as end-of-line and another side can follow VIA5.E.1 (see next page for examples of correct and incorrect layouts, rectangular instance shown in shaded area is recommended)	C1	≧	0.060 um
VIA5.C.1	VIA5 can be fully or partially stacked on Via4, Via3, Via2, Via1, any combination of stacked structure such as stacked Via5/Via4/Via3/Via2/Via1/CO.			

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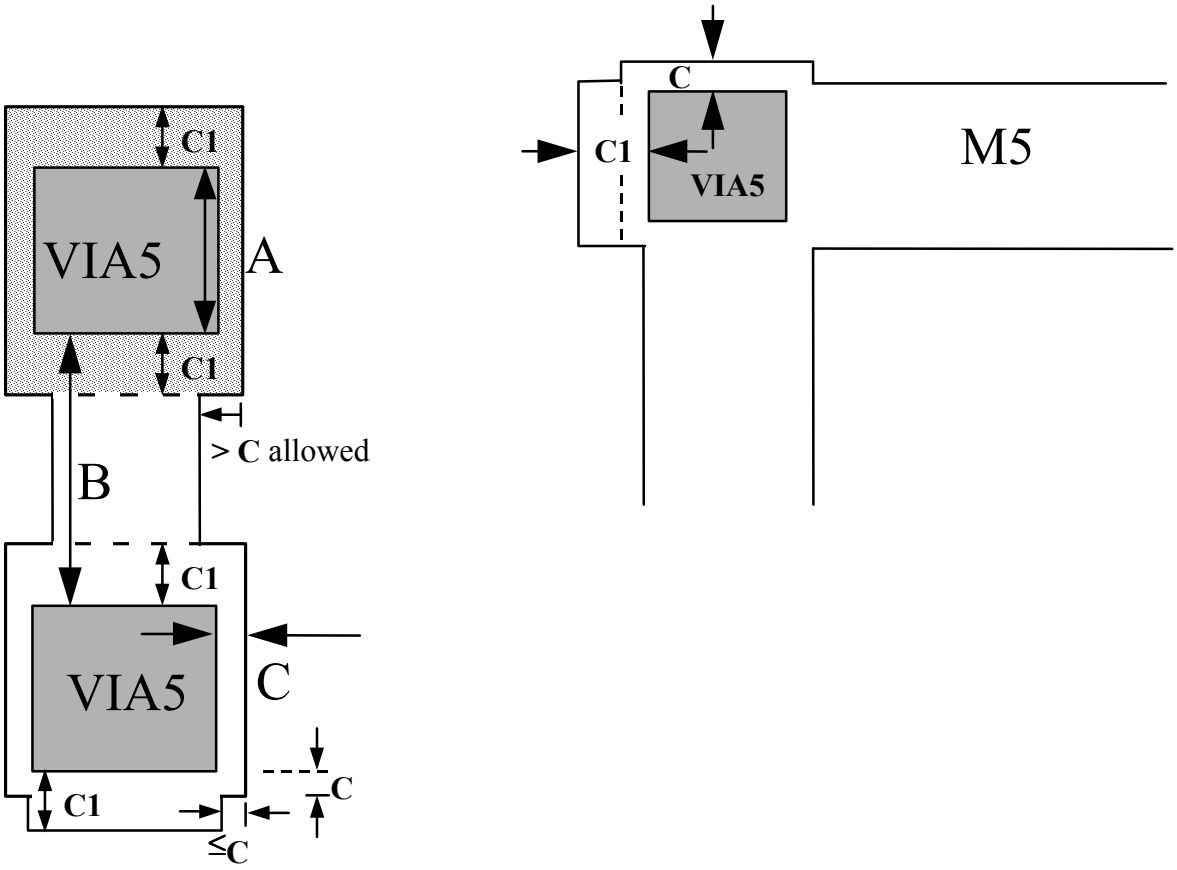
Via5



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❑ Metal 6 Rule (Top Metal Layer) (186)

Rule No.	Description	Label		Layout Rule
Layer :	M6 --- Metal 6			
M6.W.1	Minimum width of M6 region	A	≧	0.440 um
M6.S.1	Minimum space between two M6 regions	B	≧	0.460 um
M6.E.1	Minimum extension of M6 region beyond a VIA5 region	C	≧	0.090 um
M6.S.2	Minimum space between metal lines with one or both metal line width and length are greater than 10um; the minimum space must be maintained between a metal line and a small piece of metal (<10um) that is connected to the wide metal within 1.0 um range from the wide metal.	D	≧	0.600 um
M6.A.1	Minimum area of M6 region	E	≧	0.562um^2
M6.R.1	Minimum density of M6 across full chip Density is calculated as Total metal layout area/chip area. It is recommended to use TSMC's auto-fill utilities (Document No.: T-018-LO-DR-001-C3) to add dummy metal if M6 density is less than 30%.)		≧	30 %

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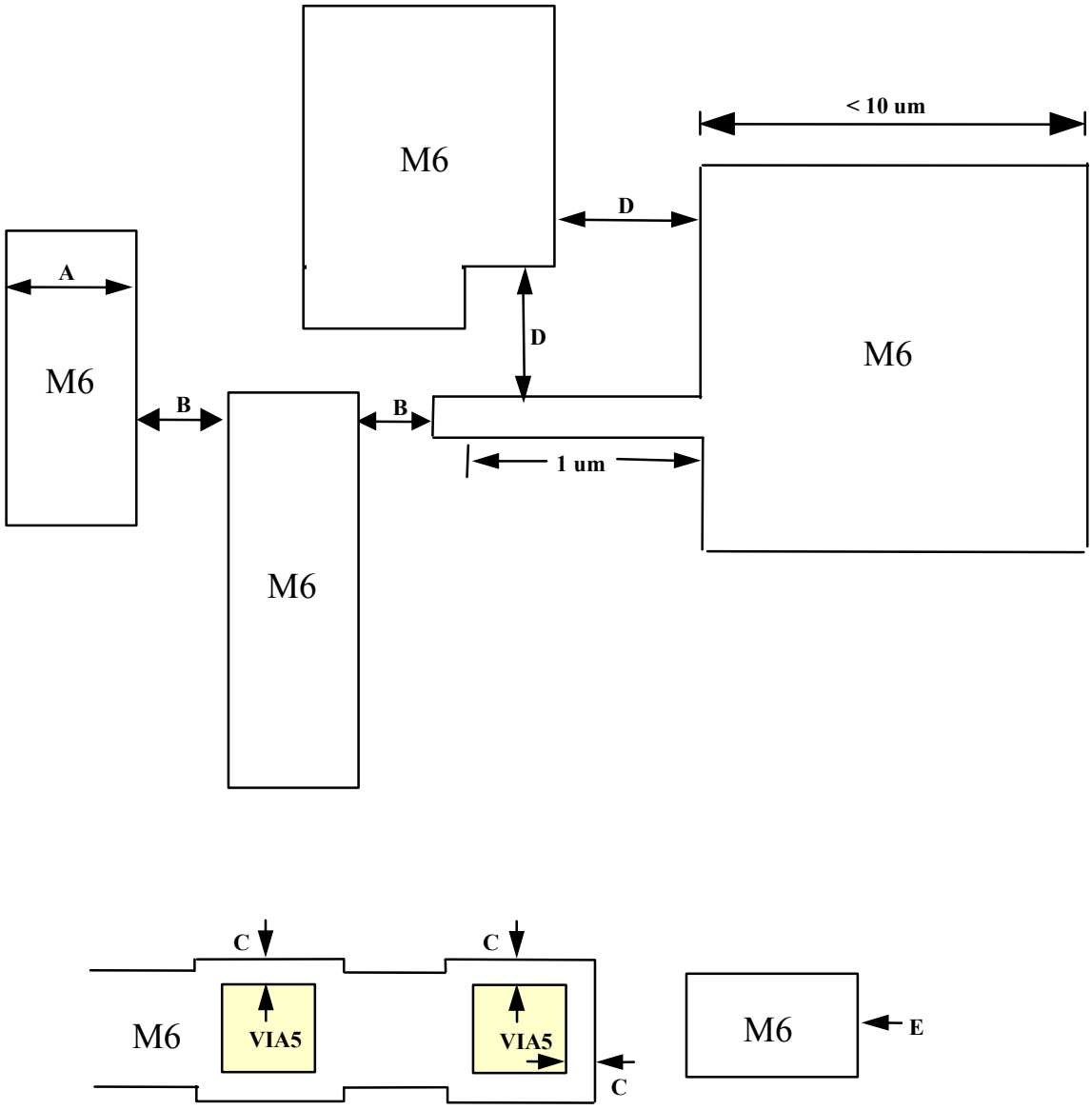

METAL 6

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Passivation & Polyimide Rule (107 & 009)

Please refer to "TSMC WIRE BOND, FLIP CHIP AND INTERCONNECTION DESIGN RULE" (Doc. No.T-000-CL-DR-002) for details.

Metal Fuse Rule

Please refer to "TSMC Al Metal Fuse Design Rule" (Doc. No. T-000-LO-DR-003) for details.

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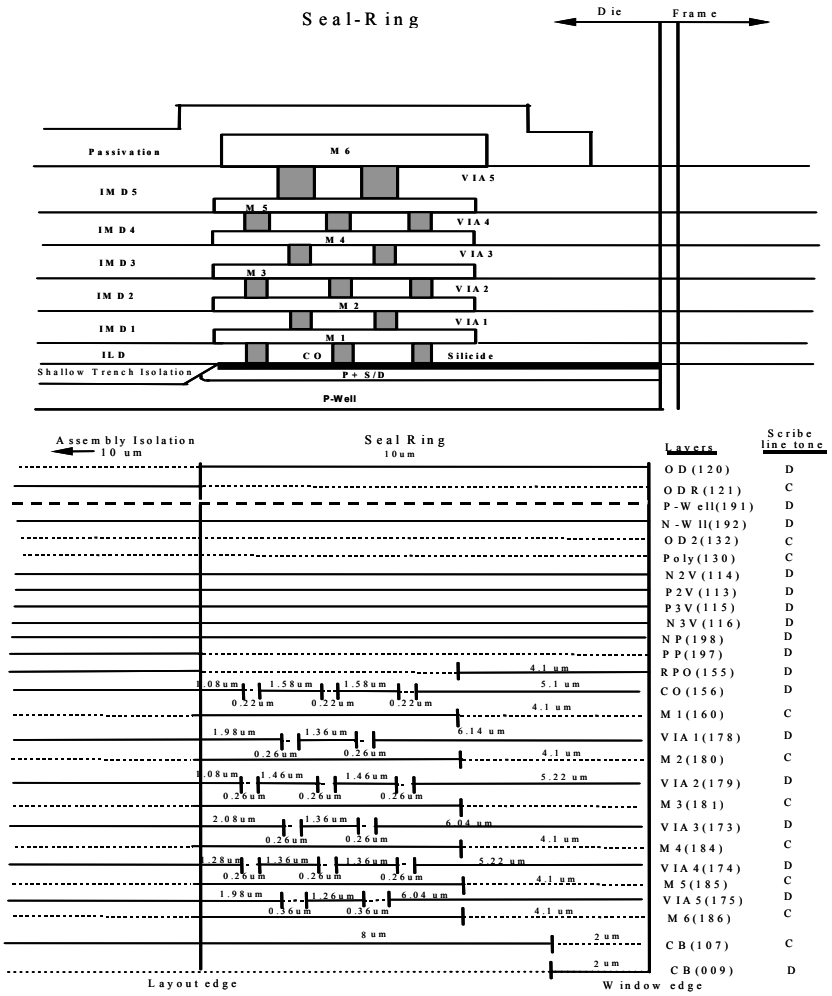
❑ Seal-Ring Rule

If seal ring is added by TSMC, TSMC will add assembly isolation and seal-ring structure at the same time.

SR.S.1	Minimum assembly isolation. It also depends on the capability of assembly house to require layer distance.	5.0 um
SR.E.1	Minimum extension of metal to CO/VIA in guard ring. Propose to exactly follow the dimensions in the figure below.	0.6 um

TSMC recommend scribe line seal and scribe guard ring rules as follows.



…… Digitized area are clear on mask.

* For SPPM process, please skip metal5 and via4 layers.
* For SPQM process, please skip metal5, metal4, via4 and via3 layers
* For SPTM process, please skip metal5, metal4, metal3 via4, via3, and via2 layers.

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❑ Antenna Effect Prevention Design Rules

Rule No.	Description	Layout Rule
Layer :	Poly, Metal 1, 2, 3, 4, 5 or 6	
A.R.1	Maximum drawn ratio of field poly perimeter area to the active poly gate area connected directly to it	200
A.R.2	When the protection diode is not used, the maximum ratio of single-layer metal perimeter area to the active poly gate area. (for M1 to M6)	400
A.R.3	When a protection diode with area larger than 0.203 um^2 is used, the maximum ratio of single-layer metal perimeter area to the active Poly gate area can be calculated by the following equation: Ratio = diode area * 400 + 2200 for M1, 2, 3, 4, and 5 single layer. Ratio = diode area * 8000 + 30000 for M6 single layer.	
A.R.4	Maximum drawn ratio of CO area to the active Poly gate area connected directly to it.	10
A.R.5	When the protection diode is not used, the maximum single layer drawn ratio of Via area to the active Poly gate area connected directly to it.	20
A.R.6	When a protection diode with area larger than 0.203 um^2 is used, the maximum drawn ratio of Via area to the active Poly gate area can be calculated by the following equation: Ratio = diode area * 83.33 + 75 for single layer	

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The definition of Poly, M1-M6 antenna ratio for each layer is

ratio = 2 [(L +W1)x t] / W2 x l

- L : floating metal length connected to gate
- W1 : floating metal width connected to gate
- t : metal thickness
- W2 : connected transistor channel width
- l : connected transistor channel length

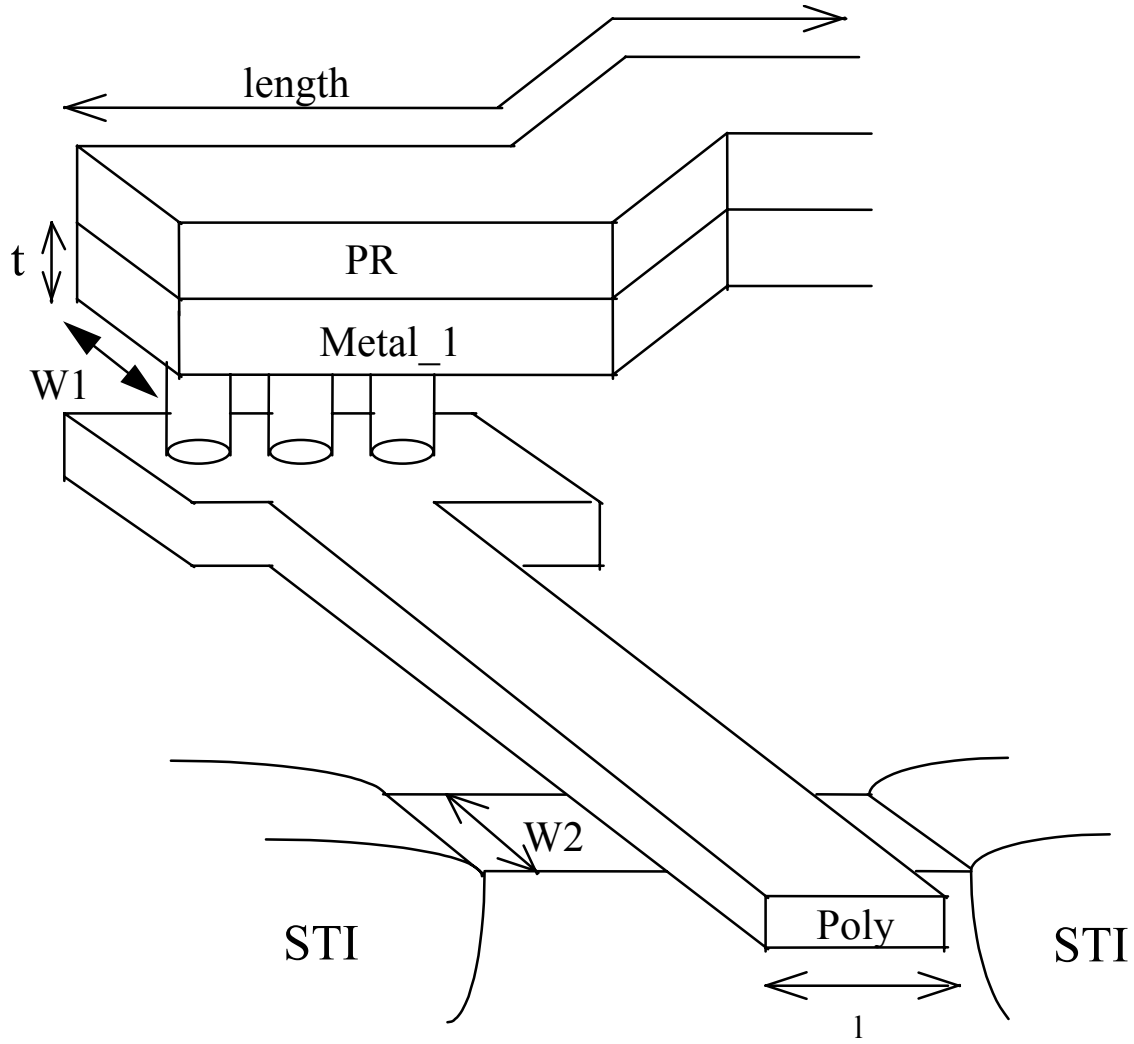
The definition of CO, Via1-Via5 antenna ratio is

ratio = {total contact (via) area}/ W2 x l

The thickness of poly is 2000A

The thickness of M1-M5 is 5300A.

The thickness of M6 is 9900A.



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❑ I/O ESD Protection Circuit Design and Layout Guideline:

This guideline is targeted to meet HBM >2KV and MM >200V ESD spec.
The ESD performance also depends on layout-style, which can not be completely described in this guideline.
❑ **For *5V High Voltage Tolerant I/O designed by 3.3V NMOS (up to 5V at I/O pad)* (abbreviated to *5VT NMOS* below), ESD implant is required unless special design by customer. TSMC will use ESD Dummy layer (ESD3DMY, see Rule no. 23) to generate ESD mask (no. 111) by logic operation.**

- **ESD Implantation Rule (mask no. 110) is obsoleted in 2.1 revision.**
- **For customers who use tsmc-style ESD design structure, additional ESD implant (mask no. 111) is required to improve ESD performance.**
- **For customers who use their own ESD design structure, or do not use *5VT NMOS*, it depends on customer's option to implement ESD implant.**
- **Dummy layer in Rule no. 234 is required to guarantee ESD performance.**

I/O design style	CAD layer 234	ESD mask (no.111)
tsmc-style I/O w/i *5VT NMOS*	Drawn Require	Generated by tsmc Logic operation
tsmc-style I/O w/o *5VT NMOS*	No	No
Non tsmc-style ESD	Depend	Depend

❑Guidelines for NC (No-Connect) pin during ESD testing
A NC pin on an IC package is defined as an isolated pin that is not connected to any bond pad on a die. NC pin might be zapped during ESD testing. For a certain combination of packages and ESD testers, zapping NC pin could potentially generate damage to other connected pins [Ref. 1 & 2]. To avoid damage during NC pin ESD testing, the suggestions are:

(1) Do not zap NC pin, or
(2) Insert a delay time between each zapping. The longer delay time is better. This delay time is dependent on package and tester; or
(3) After zapping a NC pin, briefly short it to ground before zapping next pin.

Ref. 1 – A. Amerasekera, C. Duvvury, "ESD in Silicon Integrated Circuits", 2nd edition, John Wiley & Sons Ltd., p.23
Ref. 2 – M. Matsumoto, M. Ura, K. Miyamoto, "New Failure Mechanism due to Non-Wired Pin ESD Stressing", EOS/ESD

❑ I/O ESD Protection Circuit Design and Layout Guideline:

This guideline is targeted to meet HBM >2KV and MM >200V ESD spec.
The ESD performance also depends on layout-style, which can not be completely described in this guideline.

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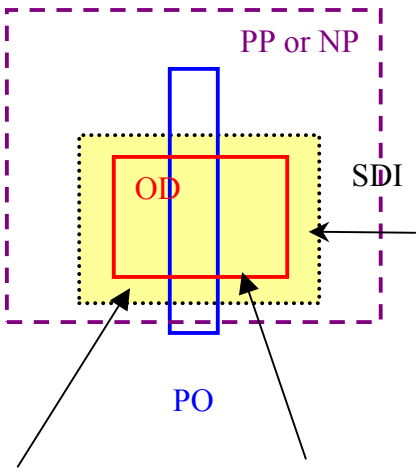
SDI Dummy Layer Description:

SDI (CAD layer:58) is a required DRC dummy layer that directs the DRC checking of I/O ESD and latch-up guidelines. Draw the SDI layer on all the ESD MOS OD regions that are connected to pads. The SDI should cover the ESD MOS OD region, including the source, gate, and drain regions; but not necessarily include the field PO and well strap OD regions.



Source Drain

The SDI Dummy Layer Layout

Note: The items remarked by Ⓖ are the ESD guidelines which DRC might not check. The others are some process-control-related items, which might degrade ESD performance. They should be checked by DRC.

Rule No.	Description		Layout Rule
ESD.1 Ⓖ	NMOS and PMOS for ESD protection follow finger type structure with unique finger dimension and layout style.		
ESD.2 Ⓖ	Minimum NMOS total finger width for I/O buffer.		360 um
ESD.3 Ⓖ	Minimum PMOS total finger width for I/O buffer.		360 um
ESD.4 Ⓖ	Unit finger width of NMOS and PMOS for I/O buffer (Fig.2)	G	20 ~ 60 um
ESD.5x	NMOS and PMOS of I/O buffer should have a non-salicide area on drain side, that is RPO mask should block drain side of device (except contact region should keep salicided). TSMC will do a logic operation to align I/O ESD design (see Table-1: No. 1 & 3)		

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ESD.5A	For high voltage tolerant I/O designed by 3.3V NMOS (see N1 and N2 in Fig.1a): RPO should cover all inactive poly gate and extend to active region (*Poly spacing ≥ 0.25um*). RPO also needs to overlap the active poly gate by 0.05um. (see Fig.1b).	0.05
ESD.5B	For high voltage tolerant I/O designed by 1.8V NMOS (see N1 and N2 in Fig.1a): RPO should cover inactive poly gate completely, and the clearance between RPO and active poly gate is 0.25um (see Fig.1c).	0.25
ESD.5C	For regular 3.3V I/O in NMOS region (see N3 in Fig.1d): RPO on the drain side needs to overlap poly gate by 0.05um. (see Fig. 1e)	0.05
ESD.5E	For all PMOS (see P1 in Fig.1a and P3 in Fig.1d) and regular 1.8V I/O in NMOS region (see N3 in Fig.1d): RPO to poly spacing is 0.45um. (see Fig.1f)	0.45
ESD.5D	For the grounded gate ESD protection device between Vcc/Vss (see Ncs in Fig.1a and Fig.1d): It is suggested that RPO fully covers the non-contacted poly gate, source/drain.(see Fig.1g) Except the Vcc/Vss protection (see Ncs in Fig.1a and Fig.1d), the RPO on the source side should be removed, or if used, must follow design rules related to RPO (width, spacing, etc).	
ESD.5F	The minimum width of RPO on drain side (X) and RPO edge to OD edge (Y) for 3.3V NMOS without ESD implant; and 1.8V NMOS High Voltage tolerant (up to 3.3V).	Y≥X≥ 1.95 um
ESD.5G	The minimum width of RPO on drain side (X) and RPO edge to OD edge (Y) for 1.8V NMOS without ESD implant and 3.3V PMOS and 1.8V PMOS.	Y≥X≥ 1.5 um
ESD.6	The minimum clearance of poly edge to CO edge on source side for Z NMOS and PMOS	0.75 um
ESD.7 Ⓖ	Minimum resistance of I/O as R in Fig.4.	200 Ω
ESD.8 Ⓖ	For I/O buffers, if more than half of total fingers are used (NMOS and PMOS be considered separately), the poly gates of dummy fingers should be connected through 1KΩ resistors to VDD/VSS of buffers. And if less than half of total fingers are used, the poly gates of dummy fingers should be connected through a soft-pull device to VDD/VSS as illustrated in Fig.4. The equivalent resistance of the soft pull device should be larger than 5 KΩ *under ESD zap condition*. If MOS's are used as the soft-pull devices, their gates should be connected through 1KΩ resistors (R1 in Fig.4) to VDD/VSS of internal circuits. (For more details, please see "Tips for Soft Pull".)	

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ESD.9 Ⓖ	Minimum gate length for I/O buffer.	Lg	Table 2
ESD.10 Ⓖ	ESD protection device should be surrounded by the appropriate base guard-ring. All other devices should be placed outside this guard-ring. It is illustrated in Fig. 2.		
ESD.11	Butting or inserted Substrate/Well pick-up's in the ESD N/PMOS are strictly prohibited. (see Fig.3)		
ESD.12 Ⓖ	Contacts and vias should be used as many as possible, and at least capable of bearing 100mA DC current (please calculate it from EM data).		
ESD.13 Ⓖ	Minimum total width of metal lines connecting bond pad and ESD protecting devices.	I	20 um
ESD.14 Ⓖ	Minimum Vss and Vdd power ring metal width.		50 um
ESD.15 Ⓖ	Corners of conducting layers in ESD discharge paths should be tapered with 45 degree layout.		
ESD.16 Ⓖ	Minimum metal width on drain side of ESD devices.	H	4.5 um
ESD.17 Ⓖ	At least the NMOS4 in Fig.4 should be added after resistor R as the secondary ESD protection. For better ESD immunity, both PMOS to VDD and NMOS to VSS should be used there if no conflict with circuit operation. *ESD implant can not be used in the secondary protecting devices*. The suggested device sizes for secondary protection are: for 3.3V I/O :NMOS is 20/0.35 and PMOS is 20/0.30 for 1.8V I/O :NMOS is 20/0.20 and PMOS is 20/0.20 If the performance of CDM is concerned, the secondary protection should be put close to the device gate being protected.		 (use 3.3V devices) (use 1.8V devices)
ESD.18 Ⓖ	Bypass discharge cells should be inserted between separated VDD's and VSS's to ensure no ESD damage to internal circuits. It is of special importance to the isolated powers used only by a small circuit (<5K gates) The connections are illustrated in Fig.5. (For more details, please see "Tips for Power Bus".)		
ESD.19 Ⓖ	All nodes directly connecting to ESD discharge path should follow ESD dimension rules.		
ESD.20 Ⓖ	OD area of edge side of ESD devices or I/O buffers should be Source or Bulk rather than Drain (see Fig.2), to avoid the unwanted parasitic bipolar effect or abnormal discharge path in ESD zapping.		

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ESD.21 Ⓖ Space between any two OD areas of the same type (N to N, or P to P) with one of the following connections should be larger than 2.4um, or a base guard ring (pickup ring) should be inserted in between them:
One connects to a pad, and the other connects to another pad.
One connects to a pad, and the other connects to VDD or VSS.
One connects to VDD, and the other connects to VSS or another separated VDD.

ESD.22 Ⓖ For RPO DRC purpose, we need two dummy layers in ESD protection device. The layers should cover all ESD protection devices.

ESD1DMY (CAD#136) is for the cascade NMOS in high voltage tolerant I/O designed by 1.8V NMOS (see Fig.1c) and Vcc/Vss protection (see Fig.1g).

ESD2DMY (CAD #137) is for the cascade NMOS in high voltage tolerant I/O designed by 3.3V NMOS (see Fig.1b) and 3.3V NMOS (see Fig.1e).

ESD.23 Ⓖ ESD implant is required for *5V High Voltage Tolerant I/O designed by 3.3V NMOS (up to 5V at I/O pad)*. It needs ESD3DMY layer to generate ESD mask (No. 111) by logical operation.

ESD3DMY (CAD#234) is for the cascade NMOS in high voltage tolerant I/O designed by 3.3V NMOS (see Fig.1b).

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Table 1. RPO layout vs. ESD protection devices

No.		1	2	3	4	5	6	7
I/O Device		**3.3V NMOS High Voltage tolerant (up to 5V)**	**1.8V NMOS High Voltage tolerant (up to 3.3V)**	**3.3V NMOS Regular I/O**	**1.8V NMOS Regular I/O**	**3.3V NMOS Vdd/Vss protection**	**1.8V NMOS Vdd/Vss protection**	**3.3/1.8V PMOS**
I/O & ESD protection Structure	**High Voltage tolerant I/O**	**v**	**v**					**v**
	Regular 3.3V I/O			**v**				**v**
	Regular 1.8V I/O				**v**			**v**
	Vdd/Vss ESD protection					**v**	**v**	
RPO width on drain side (min.)		≥ 1.95	≥ 1.95	≥ 1.95	≥ 1.5	≥ 1.95	≥ 1.95	≥ 1.5
RPO to 1st-poly space		RPO to completely cover poly	RPO to completely cover poly	RPO to overlap 1st-poly by ≥ 0.05	≥ 0.45	RPO to completely cover poly andSource	RPO to completely cover poly and cover Source	≥ 0.45
1st poly to 2nd-poly spacing		≥ 0.25	≥ 0.25					
RPO to 2nd-poly space		RPO overlap to 2nd-poly by ≥ 0.05	≥ 0.25					
ESD implant (mask 111) Required dummy layer (see ESD rule 23)		Y ESD3DMY	N	N	N	N	N	N
Dummy layer for DRC (see ESD rule 22)		ESD2DMY	ESD1DMY	ESD2DMY		ESD1DMY	ESD1DMY	
Illustration		**Fig.1b**	**Fig.1c**	**Fig.1e**	**Fig.1f**	**Fig.1g**	**Fig.1g**	**Fig.1f**

Table 2. Lg for I/O buffer

	NMOS	PMOS	ESD IMP *
1.8V Device	0.25 um	0.25 um	
3.3V Device	0.4 um	0.3 um	0.4um

- **ESD performance is not guaranteed once Lg > 0.5um.**

ESD IMP* : ESD mask (no. 111) can be generated by tsmc internal logic operation, using CAD layer 234, see ESD rule 23).

❑ Analogy and High Speed Input

For analogy and High-Speed input ESD designs, please refer to document: *T-018-MM-RP-016*. Customers need to contact their account mangers and sign NDA's before acquiring this document.

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❑ Tips for Soft Pull

The major point of using soft pull scheme is to balance the breakdown voltage and speed of the used and unused (dummy) I/O fingers under ESD zapping. Since the breakdown voltage of MOS devices is dependent on gate voltage, the different gate potential between the used and unused fingers may cause a non-uniform ESD discharge path, and local damage may happen.

The gates of used fingers is initially floated since power is off. The ESD voltage impulse is easy to couple into the floated gates, and make the breakdown voltage lower than those with grounded gates. The soft pull scheme can make the gate conditions more similar between used and unused fingers, but still hard to make them exactly the same.

Another approach is using the major population to bear ESD energy:

If used fingers is more than the dummy, the gate of dummy fingers be grounded through 1KΩ to Vss to make the breakdown voltage higher than the used fingers, and force the used fingers to breakdown earlier (see soft-pull in Fig.4).

If used fingers is less than the dummy, strong voltage coupling to the gate of dummy fingers is desired. Efficient gate-coupling circuitry (see Dynamic RC coupling circuit in Fig.4) can be applied to the dummy fingers. (the detail information please refer IEEE Trans. Elec. Dev., p. 2076, 1998, or USA patent 6034552)

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❑ Tips for Power Bus

The ESD Protection design is not only for the input, output, or power pins; but also for the whole chip to avoid ESD damage to internal circuits. Especially in the mixed-mode IC, separated digital and analog powers are used, the interface devices between the digital and analog circuits are sensitive to ESD damage.

To prevent the problem, inter-power ESD protection circuits should be added according to the following suggestions to have better ESD immunity:

1. Using ESD clamping circuits to provide discharge paths between VDD and VSS under ESD stress.
2. Use low voltage transistor in ESD clamp for low voltage circuit protection. High voltage transistor for high voltage circuit protection.
3. Using ESD conduction circuits connecting separated power lines, as illustrated in Fig.5.

For applications of ESD conduction circuits, two approaches are recommended.

Approach 1:

The example in Fig.5a shows a multiple power ESD protection design which have three separate powers . The ESD conduction circuit is open in normal operation. In ESD stress the two power lines will be connected when the potential difference induced from ESD pulse sufficient to turn on it. The most well known structure for this ESD conduction circuit is series connected diodes (Two paths of series connected diodes in parallel but with opposite direction to each other). The diode number in series depends on the level difference and noise margin between the connected power lines. These two powers interact only when the level difference or noise is larger than the turn on voltage of the cascade diodes.

Approach 2:

If there are too many power pairs, structure in Fig.5b is recommended. All power lines are connected through ESD conduction circuits to a Common VDD and VSS.

For VDD to VSS ESD clamping circuit, NMOS with gate soft-pulled to VSS is recommended.

The recommended application guidelines for ESD conduction circuit and ESD clamping circuit are:

1. At least 1 Clamping and/or Conduction cell inserted every 1000um of power line.

2. All the layout guidelines are the same as those for IO buffers. An additional guideline is the source side should be treated the same as drain side since ESD pulse can comes from either side.

3. The suggested width for the ESD clamping NMOS is 480um, length is the same as in Table 1.

4. The suggested layout for ESD conduction diodes is finger type with total area larger than 2500um^2, and periphery larger than 1100um. OD's and Contacts for both ends of the diode should be inter-digital layout to keep low series resistance and uniform current flow.

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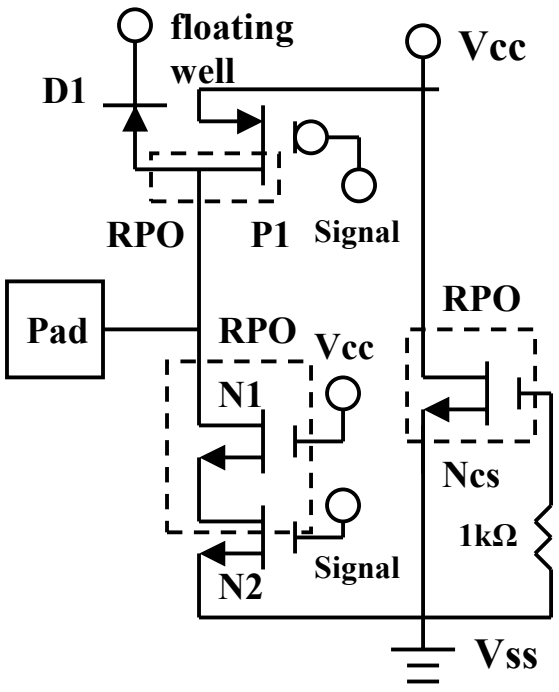
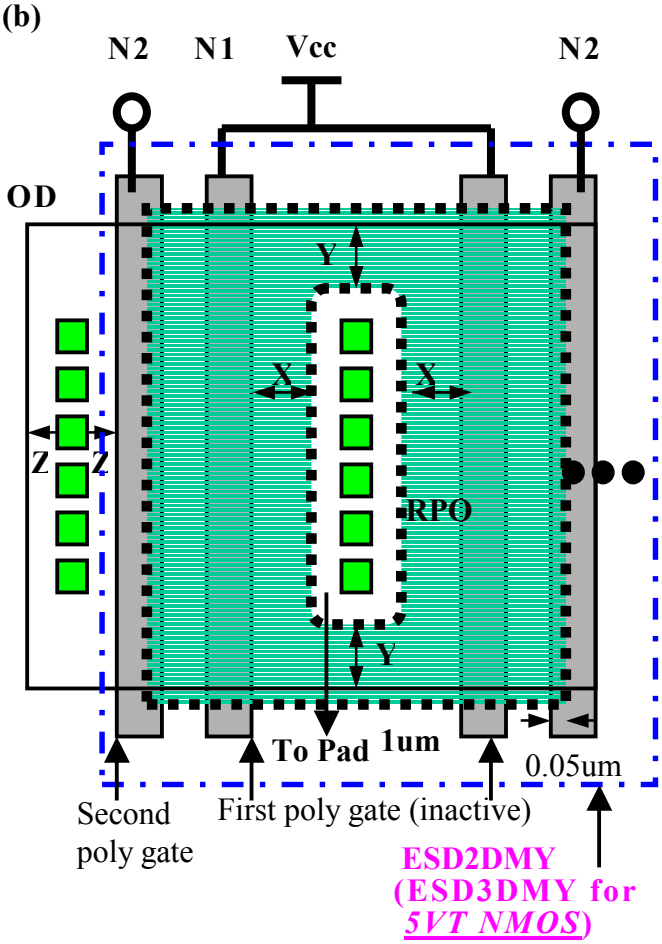
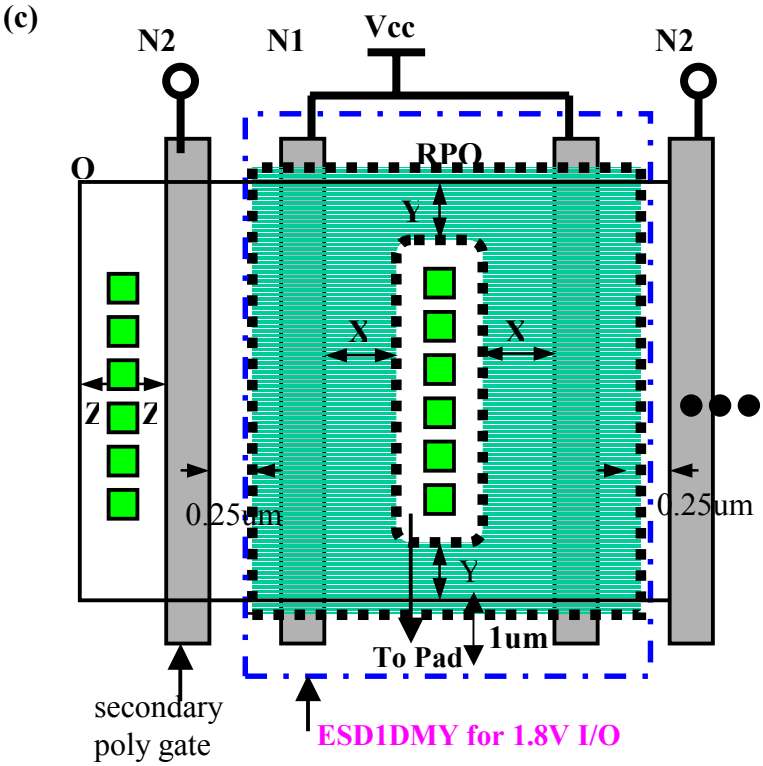
(a)



(b)



(c)



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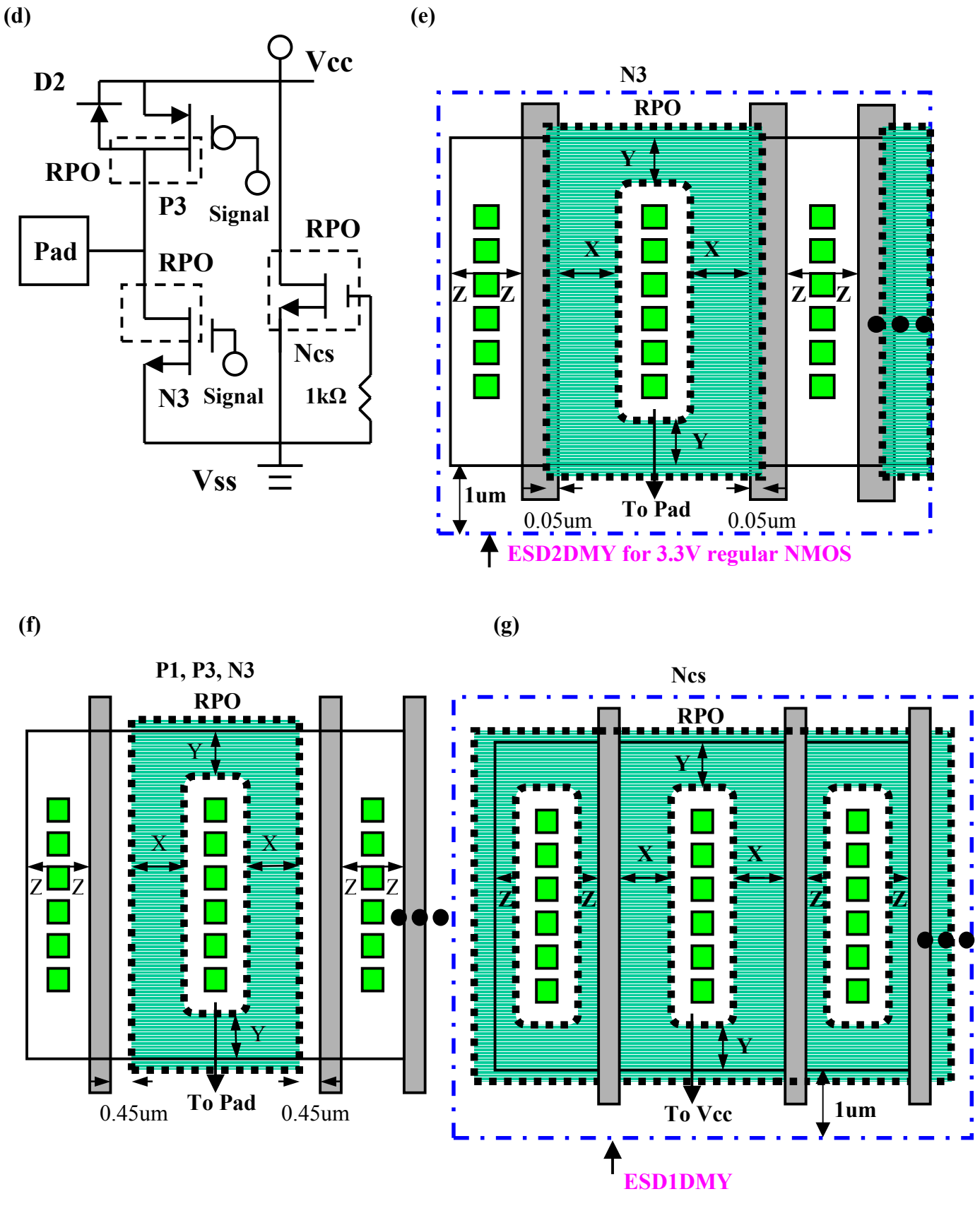

Fig 1. Schematic and the dimensions of ESD device

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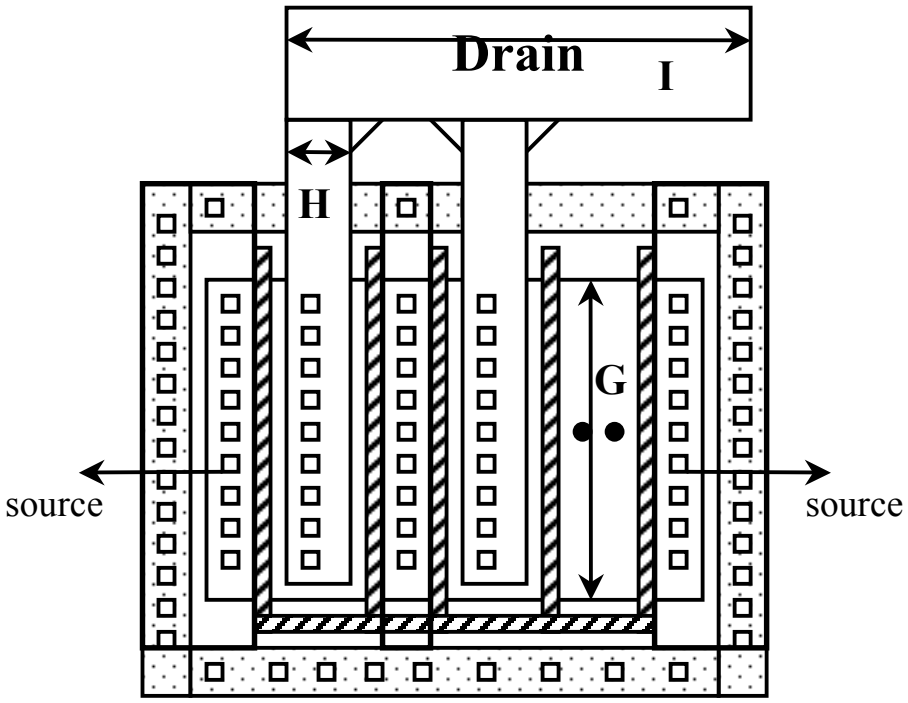

Fig 2. ESD cell layout

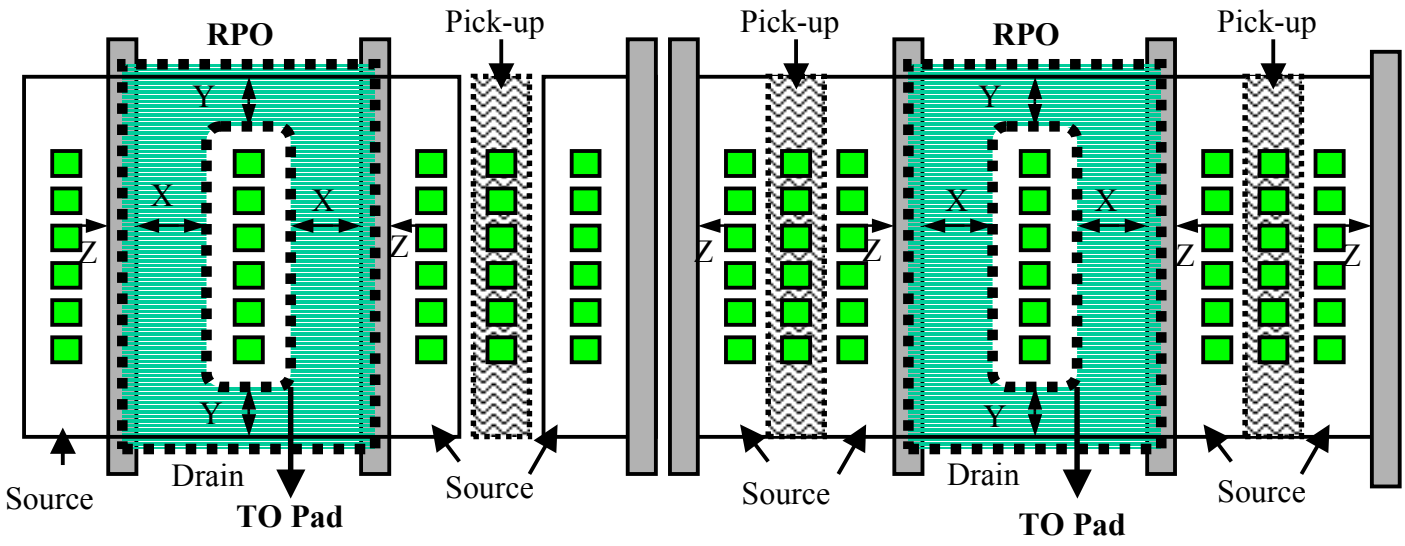

Fig 3. Butting or inserted pickup between source diffusion of ESD devices are prohibited.

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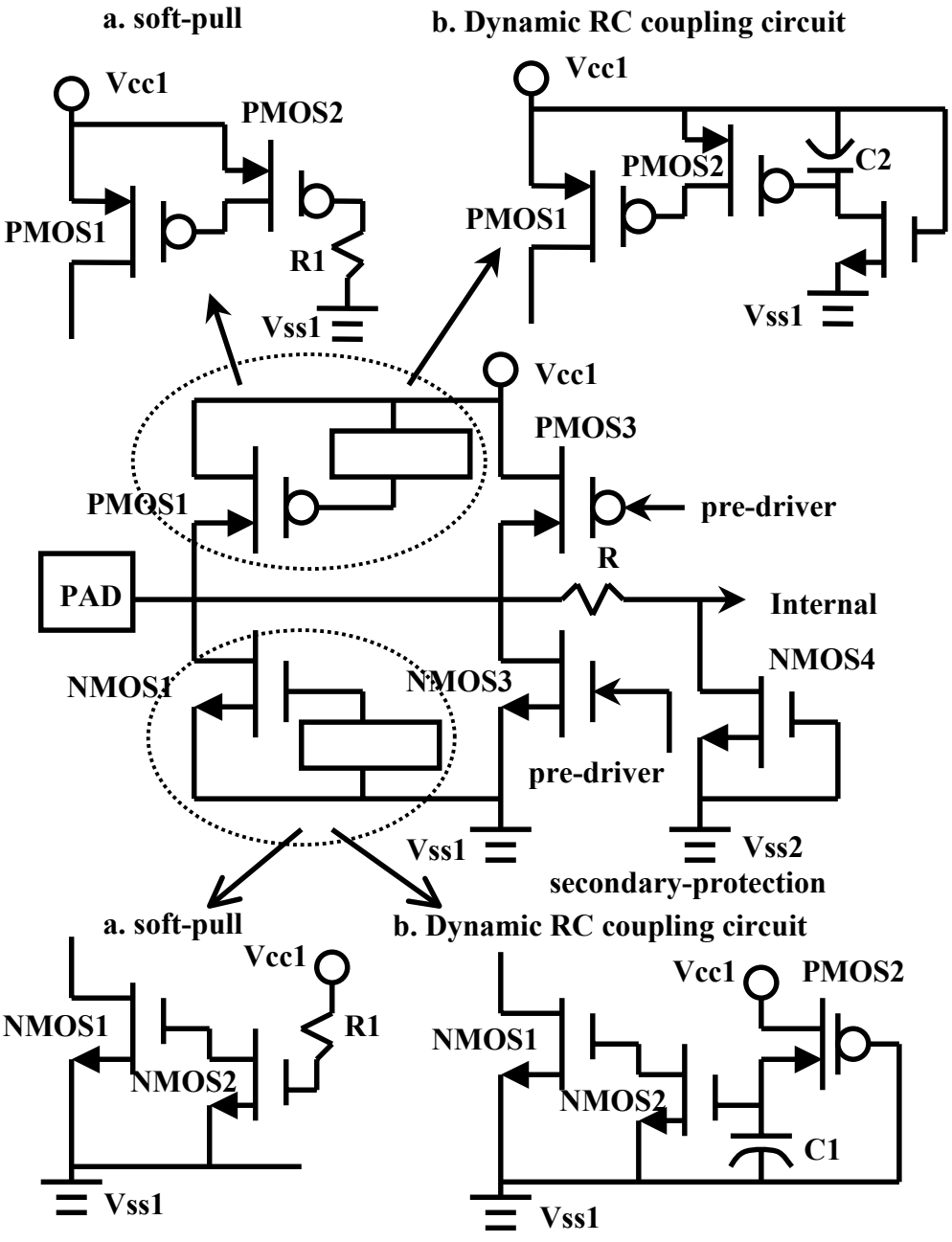

Fig 4. ESD protection circuit and soft pull device

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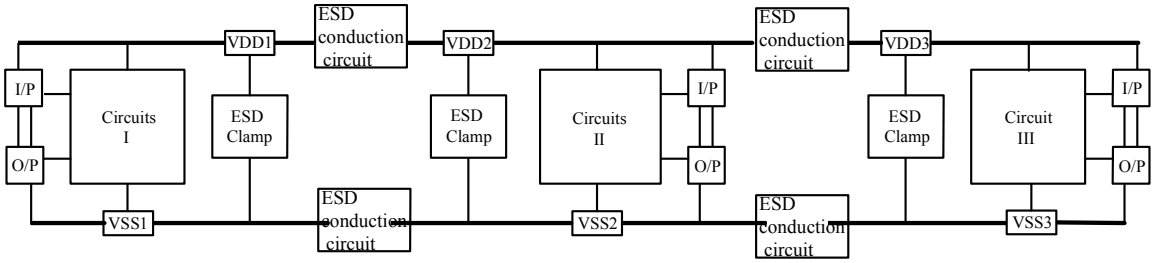
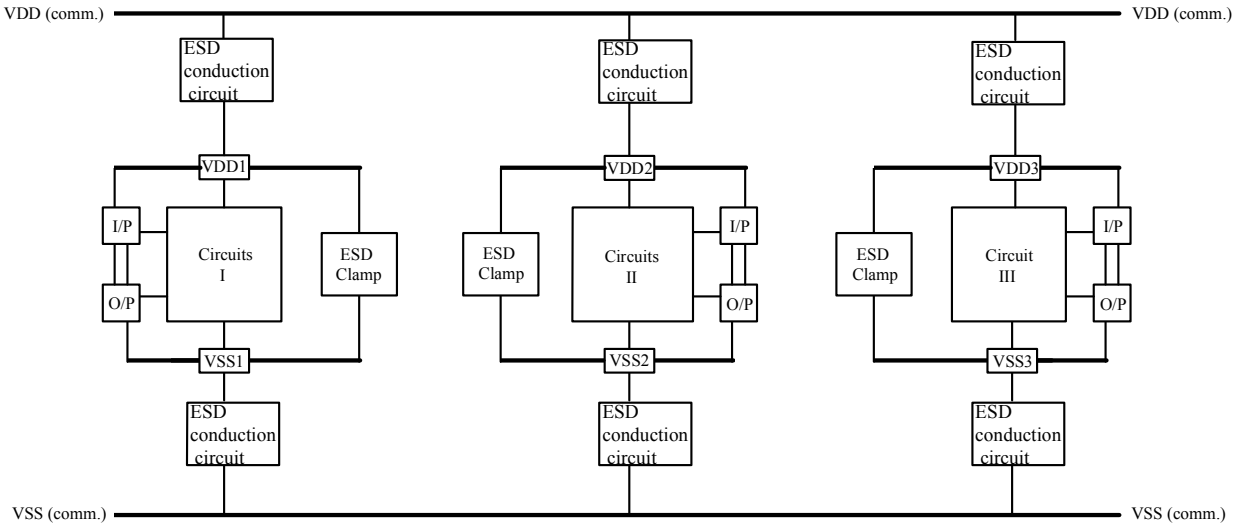


(a)



(b)

Fig 5 Schematic of multiple power ESD protection design

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Layout Guideline for Latch-Up Prevention

Rule No.	Description	Layout Rule
1.	For I/O buffers and ESD devices, a double guard ring structure should be inserted in between NMOS's and PMOS's, as illustrated in Fig.1.	
2.	For I/O buffers and ESD devices, the minimum spacing between NMOS and PMOS.	A 15um
3.	For I/O and internal circuits, the maximum distance from any point inside Source/Drain OD area to the nearest pickup OD in the same NW or PW.	B 30um
4.	A guard ring structure with *NW psudo-collector and P+pickup* should be inserted in between I/O buffer and internal circuit area.(refer to Fig.2)	
5.	The minimum spacing between I/O buffer and internal circuit area.	C 50um
6.	Any hot OD area connecting to I/O pads should be surrounded by double guard ring.	
7.	Any ***NW without direct connection to VDD*** and with hot OD inside it should be surrounded by double guard ring.	
8.	For special devices such as Bipolar transistor, diode, resistor, or special circuits such as charge pump, power regulator, high noise or high power circuitry, double guard ring should be inserted surrounding and between them.	
9.	All the guard rings and pickups should be connected to VDD/VSS with very low series resistance. That is, ***NW should be tied together with N+OD, and OD should be tied together with contacts and metals of VDD/VSS. Contacts and via's should be used as many as possible.***	

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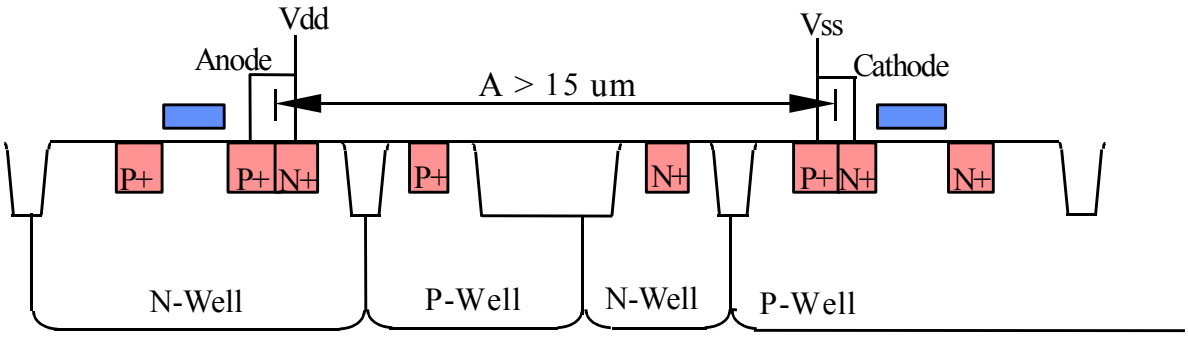
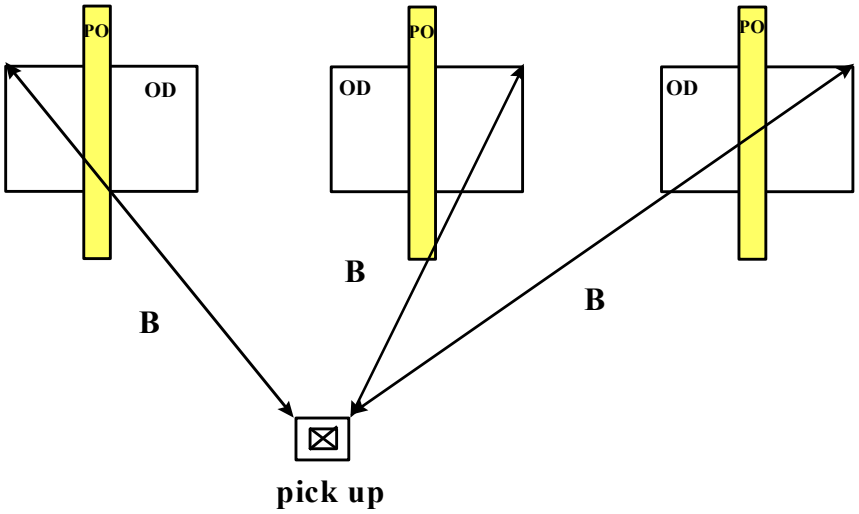


Fig.1



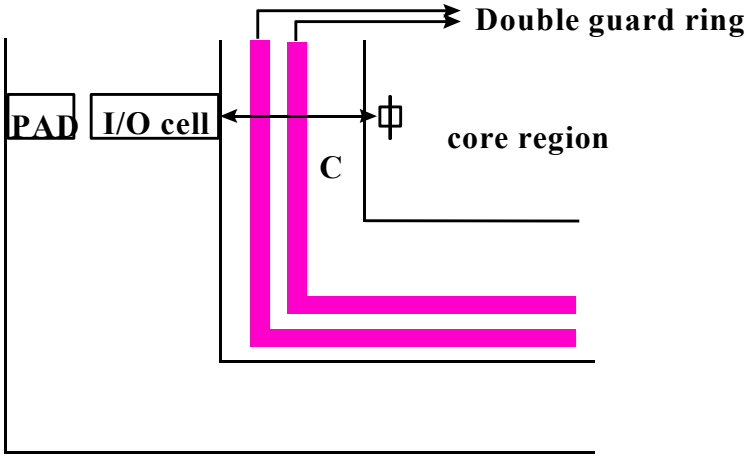


Fig.2

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Current Density Specification

(1) Metal Line

Jmax of M1=1.0 mA/um (at 110°C)
Jmax of M2=1.0 mA/um (at 110°C)
Jmax of M3=1.0 mA/um (at 110°C)
Jmax of M4=1.0 mA/um (at 110°C)
Jmax of M5=1.0 mA/um (at 110°C)
Jmax of M6=1.6 mA/um (at 110°C)

(2) Contact and Vias

Jmax per Contact =0.53 mA/ct (at 110°C)
Jmax per Via1=0.28 mA/Via (at 110°C)
Jmax per Via2=0.28 mA/Via (at 110°C)
Jmax per Via3=0.28 mA/Via (at 110°C))
Jmax per Via4=0.28 mA/Via (at 110°C)
Jmax per Via5=0.706 mA/Via (at 110°C)

(3) Stack Contact/Via

Jmax per CV1=0.28 mA/Via (at 110°C)
Jmax per CV12=0.28 mA/Via (at 110°C)
Jmax per CV123=0.28 mA/Via (at 110°C))
Jmax per CV1234=0.28 mA/Via (at 110°C)
Jmax per CV12345=0.28 mA/Via (at 110°C)
Jmax per V12=0.28 mA/Via (at 110°C)
Jmax per V23=0.28 mA/Via (at 110°C)
Jmax per V123=0.28 mA/Via (at 110°C))
Jmax per V34=0.28 mA/Via (at 110°C)
Jmax per V234=0.28 mA/Via (at 110°C)
Jmax per V1234=0.28 mA/Via (at 110°C)
Jmax per V45=0.28 mA/Via (at 110°C)
Jmax per V345=0.28 mA/Via (at 110°C))
Jmax per V2345=0.28 mA/Via (at 110°C)
Jmax per V12345=0.28 mA/Via (at 110°C)

Jmax is maximum DC current allowed per um of metal line width or per via or per contact. The number is based on 0.1% point of measurement data at 20% resistance increase after 10 year continuous operation. Use the following table to convert Jmax from one temperature to another.

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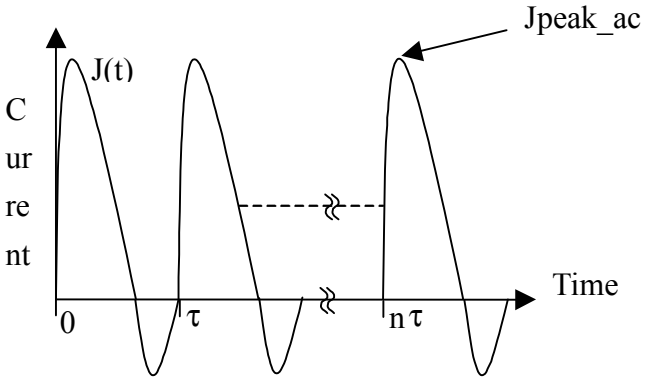
Rating Fator of Jmax vs Temperature

Temp.	70°C	85°C	100°C	110°C	125°C	150°C	175°C
rating factor of Jmax	1	0.609	0.386	0.290	0.195	0.107	0.062
	1.64	1	0.634	0.477	0.320	0.175	0.102
	2.59	1.58	1	0.753	0.505	0.276	0.162
	3.44	2.10	1.33	1	0.671	0.367	0.215
	5.13	3.13	1.98	1.49	1	0.547	0.320
	9.38	5.71	3.62	2.73	1.83	1	0.585
	16.0	9.76	6.19	4.66	3.12	1.71	1

Example : Jmax at 125°C = 0.671 * Jmax at 110°C = 0.671 * 1mA/μm = 0.671mA/μm for M1 to M5.

AC operation guideline (this guideline is not applicable to flip chip package)



$J_{rms} = \{ (\int_{0 \text{ to } \tau} J^2(t)dt)/\tau \}^{1/2}$,
$J_{av} = \{ (\int_{0 \text{ to } \tau} J(t)dt)/\tau \}$,
where J(t) is the current density flowing through a metal line.

J_{av} is AVERAGE current density through a metal line. The numbers given below are for 10% resistance increase after 10 year continuous operation at 110°C.

$J_{av} \leq$ 1mA/um (= 2.5 x 10^5 A/cm^2) for M1 to M5 (4 KÅ thickness),
$J_{av} \leq$ 1.6mA/um (= 2.0 x 10^5 A/cm^2) for M6 (8 KÅ thickness)
It's nominal AlCu thickness instead of genuine total thickness.

J_{rms} is root-mean-square current density through a metal line. The numbers given below are for <10 °C Joule heating.

$J_{rms} \leq$ 8mA/um (= 2 x10^6 A/cm^2) for M1
$J_{rms} \leq$ 4mA/um (= 1 x10^6 A/cm^2) for M2 to M5,
$J_{rms} \leq$ 8mA/um (= 1 x10^6 A/cm^2) for M6

J_{peak_ac} is the current density at which metal line will start MELTING due to excessive Joule heating. Design should stay away from J_{peak_ac} as far as possible. J_{peak_ac} can be calculated as follows:

J_{peak_ac} = 5 x10^6 /sqrt(Duty cycle), in A/cm^2 for M1 to M6

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Duty cycle is the ratio of pulse width of J_{peak_ac} to period. For convenience, one could measure the pulse width of J_{peak_ac} at half of the peak.

Example :
If pulse width is 1ns and period is 10ns, duty cycle is 0.1 or 10%. Square root of 0.1 is 0.31.
$J_{peak\_ac} = 5 \times 10^6 / 0.31 = 1.5 \times 10^7$ A/cm^2 ,

No J_{rms} and J_{peak} are given for contact and via because Joule heating mainly comes from metal line, and metal line starts melting earlier than via in this technology.

Note : If space permits, it is preferable to have more contacts or vias than required by EM rules. This will reduce interconnect resistance and also improve reliability. Avoid using only one contact or via in one metal line unless it is absolutely necessary and allowed by rules.

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Stress Release Rule

0 DESCRIPTION :

1. Power line around the chip corner and dummy pads should be set to prevent the thermal stress induced problem. Please refer to the rule in “Chip Corner Power Line and Dummy Pad ”.

2. Users must add open slot in the wide metal line where the metal is greater than 35.0um. Please refer to the rule in “ Metal Stress Relief -- metal slot ”.

3. Large chip need to follow the “Polyimide“ requirement rule.

4. Keep top metal space less than 10.0um. User should place dummy patterns on top metal layer for the space greater than 10.0um. Please refer to the “Assembly Stress Protection – dummy metal ” .

1 TERMINOLOGY

Corners : four triangular regions in the corner whose sides are along the edge of the chip inside the seal-ring.

MT: top metal layer for all processes. For example, M2 layer for 2LM process, M3 layer for 3LM process, M4 layer for 4LM process, M5 layer for 5LM, or M6 layer for 6LM

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2.LAYOUT DEFINITION

I. Chip Corner Power Line and Dummy Pad

These rules can reduce the impact of damage induced by thermal stress during packaging and field application. Figure 1 is the general layout. Dummy pad must be constructed by STI/M1/VIA1/M2/VIA2/…./MT. Detailed layouts and cross section are depicted in Figure 2,3,4. Figure 5 is chip size-dependent power line layout. Figure 6 is the case of power line outside bond pads.

Rule No.	Description	Label		Layout Rule (um)
Rule				
ADP.1	User must add dummy pads in the chip corners. The dummy pads should fill every chip corners as many as possible. The layout is described as following spec. (from A to H; associated schematic diagram is in Figure 2).			
ADP.S.1	Minimum space between two Vias at the same level	D	≧	0.58
ADP.C.1	Minimum clearance between two Vias at different levels	E	≧	0.23
ADP.C.2	Minimum clearance between two VIA4 or VIA5 at different levels	E1	≧	0.16
ADP.E.1	Minimum extension of Metal over VIA	F	≧	3.0
ADP.W.1	Minimum and maximum width of a VIA1 to 4 region	G	=	0.26
ADP.W.2	Minimum and maximum width of VIA5 region	G1	=	0.36
Guideline				
ADP.S.2	Minimum space between two dummy pads	A	≧	2.0
ADP.S.3	Minimum space between seal ring and outer dummy pads edge	B	≧	25.0
ADP.W3	Maximum width of a dummy pad	C	≦	80.0
ADP.W.4	Minimum width of a dummy pad	C1	≧	40.0

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Rule

ADP.2	Power line must have “anchor” design, that should be constructed by the following rule (I, J, and K ; associated schematic diagram is in Figure 3). If Vdd and Vss are stacked in this region. User can by-pass this rule.			
ADP.S.4	Minimum space between two Vias at the same level	I	≧	0.58
ADP.C.2	Minimum clearance between two Vias at different levels	J	≧	0.23
ADP.E.2	Minimum extension of Metal over VIA	K	≧	0.2
ADP.R.1	No active circuit is allowed inside the square region between the first two pads counted from the edge as shown in Figure 1.			
ADP.R.2	No active circuit is allowed inside the square area fully covered the corners.			

Rule

ADP.3	There must be power line or wide metal line around the corner in top metal layer(Figure 5).			
ADP.R.3	For large die, whose size is greater than 100mm^2, power line or wide metal should be placed around every corners. The metal line should turn 45 degree from 350um(L) of the chip corner and turn 45 degree again from 350um of adjacent edge. The metal also need to extend at least 700um(N) from the starting point of turnaround (L, N in Figure 5).	L N		350 700
ADP.R.4	For small die, whose size is less than 100mm^2, power line or wide metal should be placed around every corner. The metal line should turn 45 degree from 125um(L1) of the chip corners and turn 45 degree again from 125um of adjacent edge. The metal also need to extend at least 400um(N1) from the starting point of turnaround (L1, N1 in Figure 5).	L1 N1		125 400
ADP.R.5	For power line outside bond pads, dummy pattern (with the same structure as dummy pad) should be put in the region as shown in Fig 6.			

Guideline

ADP.R.6	For any kind of chip size, the length of inside edge of power line corner should be larger than 15um(P in Figure 5).	P	≧	15

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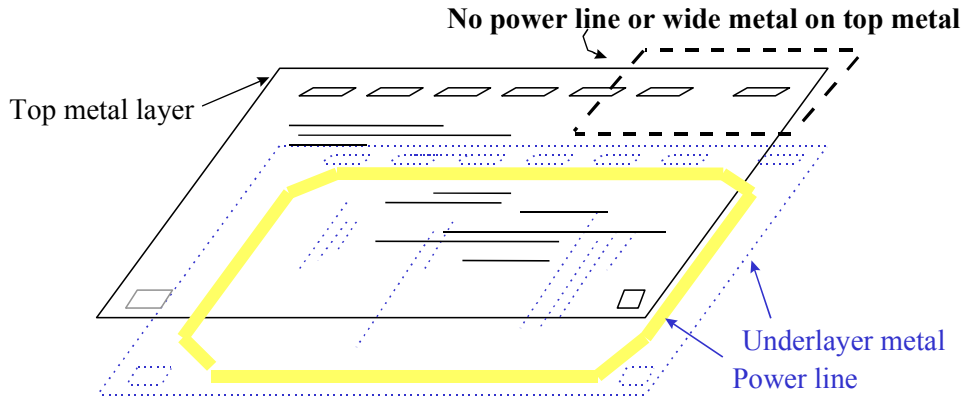
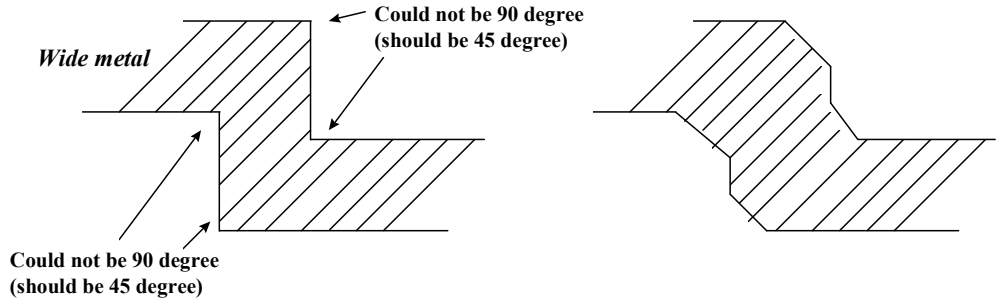
Not allowed layout (1) - without power line or wide metal on top metal around corner



Not allowed layout (2) - wide metal turn 90 degree



Not allowed

Allowed

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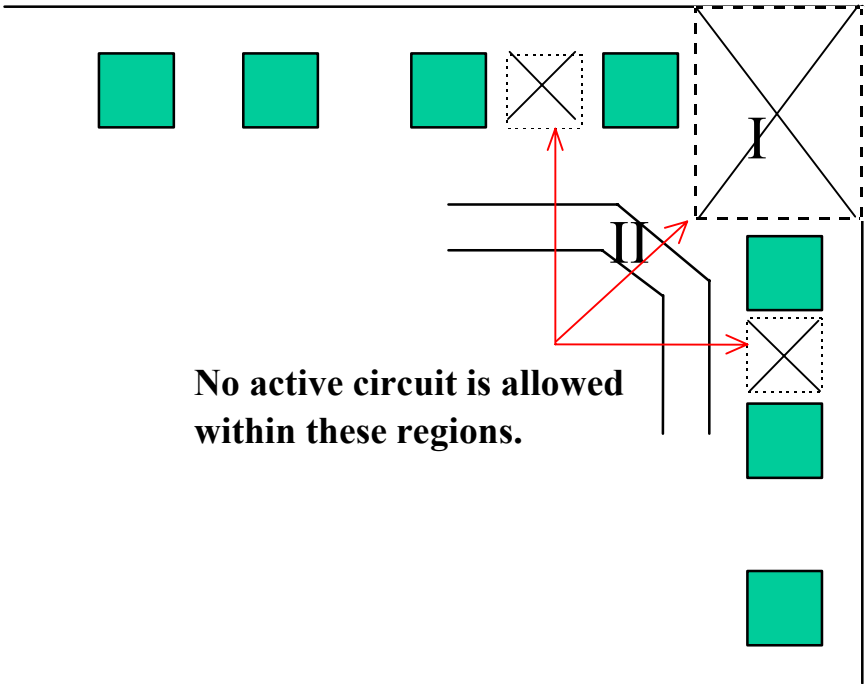

Figure 1 Chip Corner (I) and Power Line (II) Layout

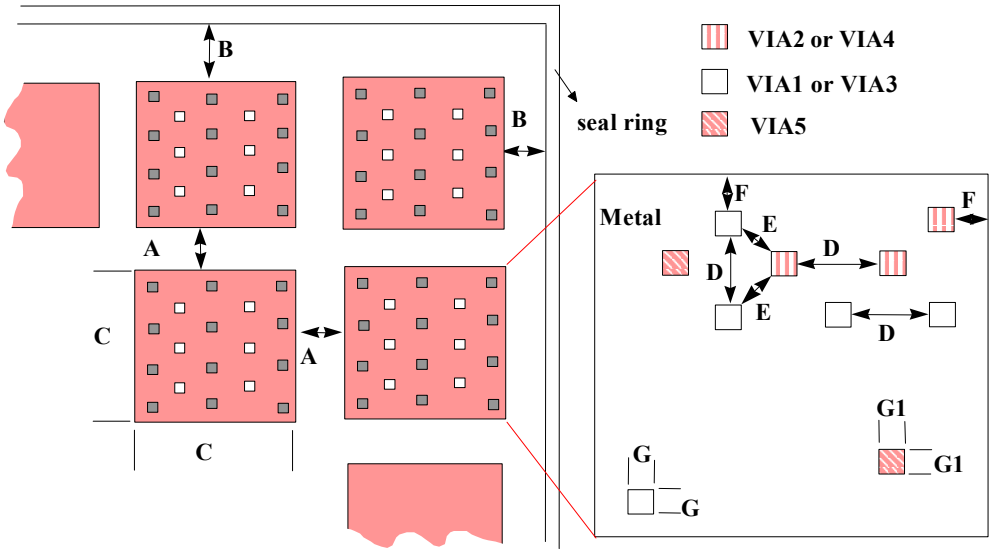

Figure 2 Chip corner dummy pad layout, region I in Figure 1

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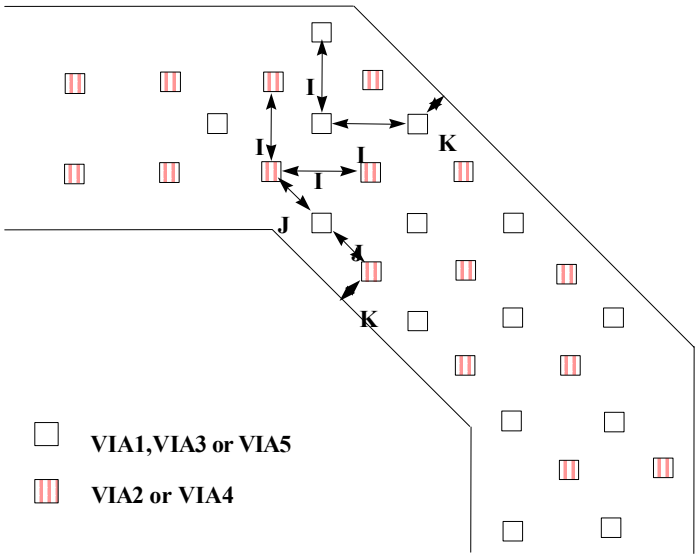

Figure 3 Chip corner power line layout, region II in Figure 1

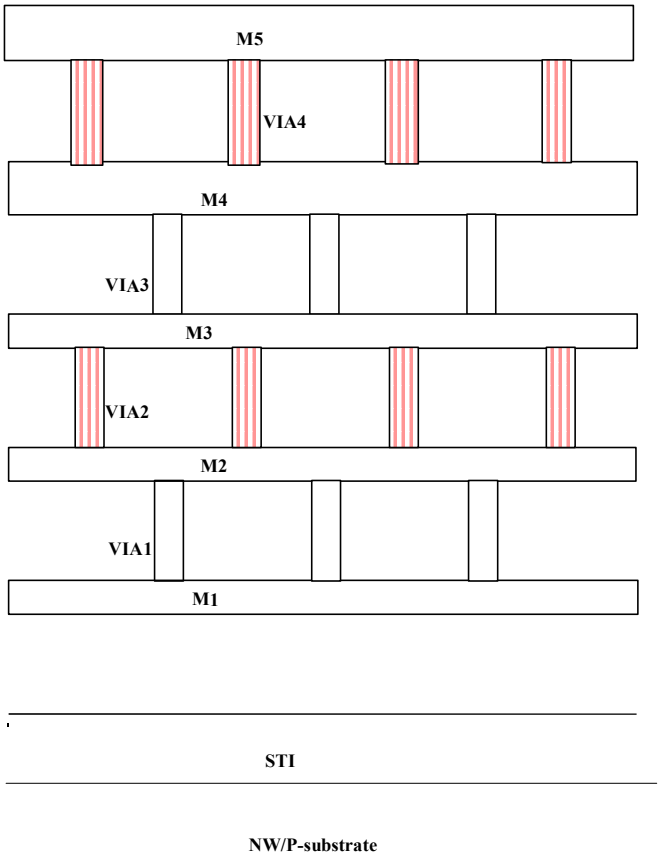

Figure 4 Cross section of power line and dummy pad

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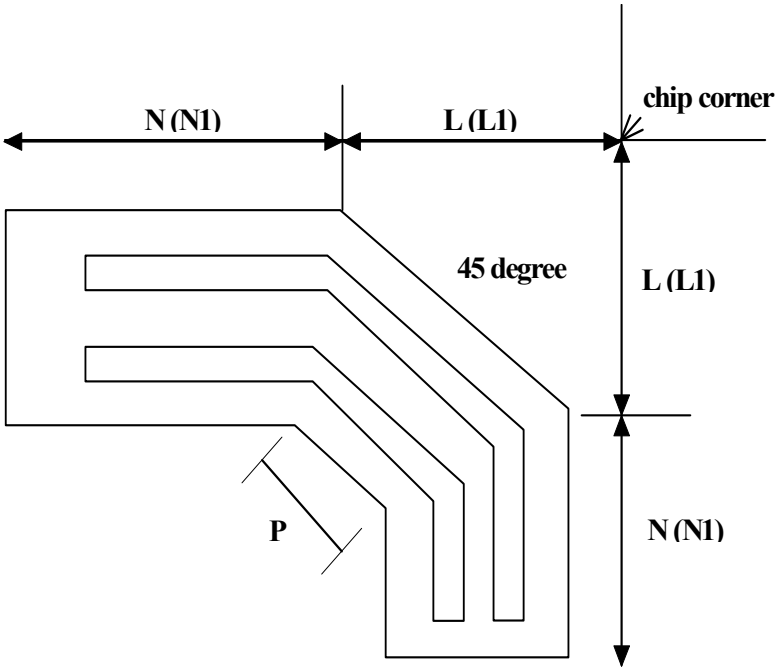

Figure 5 Chip corner power line layout
for chip size > 100mm^2(L, N) and ≤100mm^2(L1, N1)

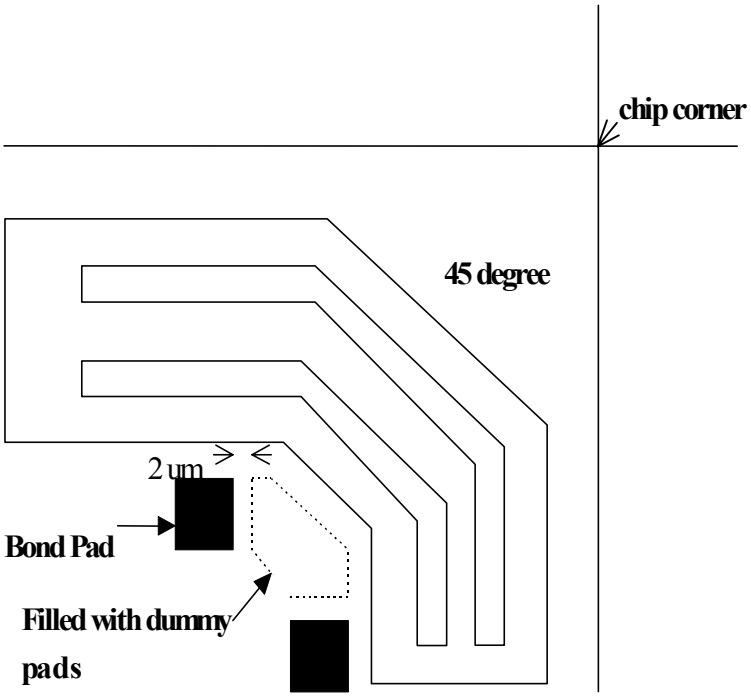

Figure 6 Chip corner dummy pads in case of power line outside bond pads

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II. Metal Stress Relief -- metal slot

Rule No.	Description		Layout Rule (um)
Rule	**All metal layers must follow this rule**		
AMS.1	The metal "slot" must be placed for releasing stress of wide metal line. The wide metal is defined as being > 35um*35um (both width and length). Only bonding pads area are excluded.		35.0
AMS.DN.Mx	Minimum slot density for the wide metal. (Slot density is defined as the slot area dividing by the wide metal area.) Open holes (>10um*10um) area is NOT included in the calculation of slot density.		≥1.5%
AM.W.1	Minimum width of at least one metal branch, which is connected to the wide metal line. No slot is allowed to be placed opposite to the metal branch. (Please make sure that the current density of the metal follows EM rule)	G	10.0
Guideline			
Slotting	Slot dimension could be > 1um (or >4um) in width and ≥ 10um in length. **[NOTE]**: Mx.S.2 require >1um space for normal metal; M6T.S.2 require >4um space for extra thick metal. Slot-to-slot spacing could be ≥ 10um. Slot-to-metal edge spacing could be ≥ 10um.	A,B C,D E,F	
AM.R.1	To avoid EM problems resulting from current funneling due to slot, the length of the slot should be parallel to current flow direction.		
AM.R.2	The starting position of the parallel slots should be staggered.		

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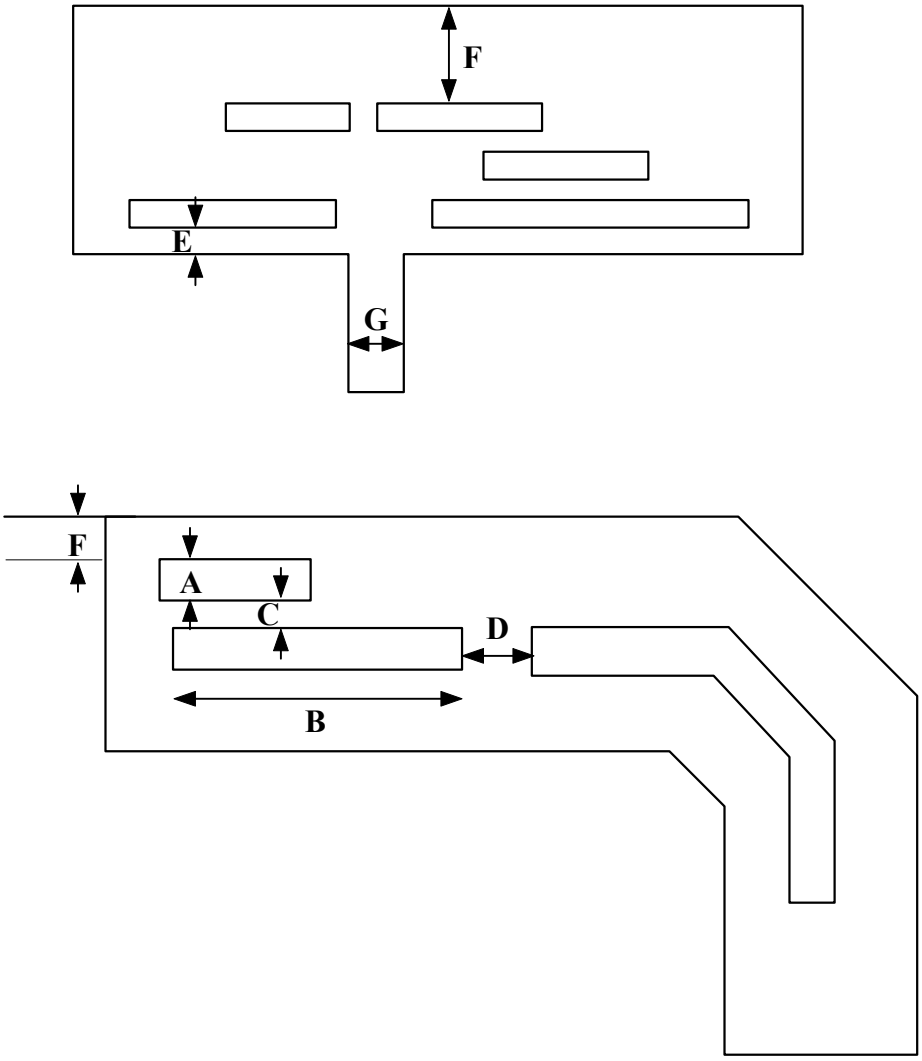
Slot definitions



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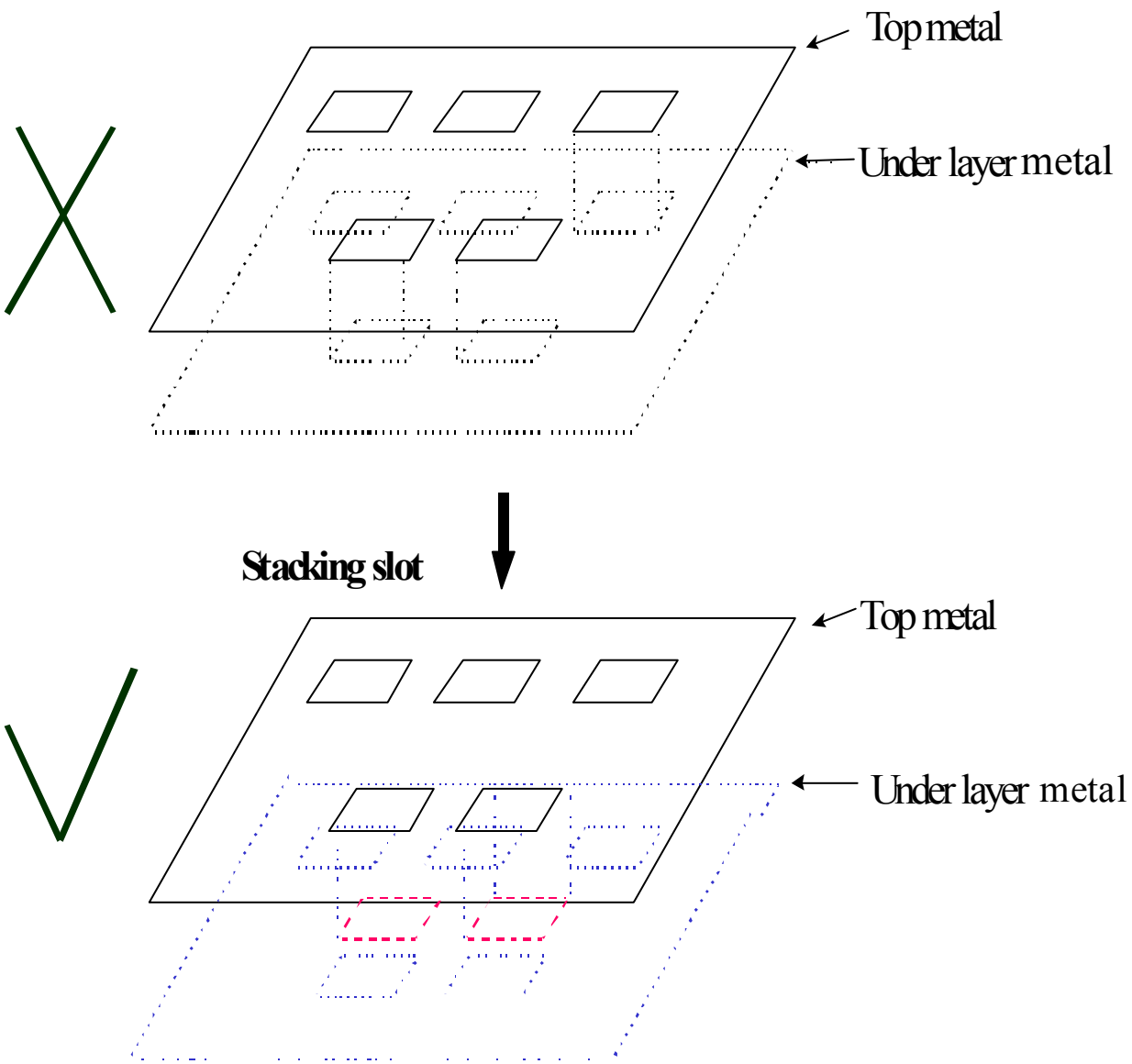
Not recommended slot Layout(1) – stacking slot



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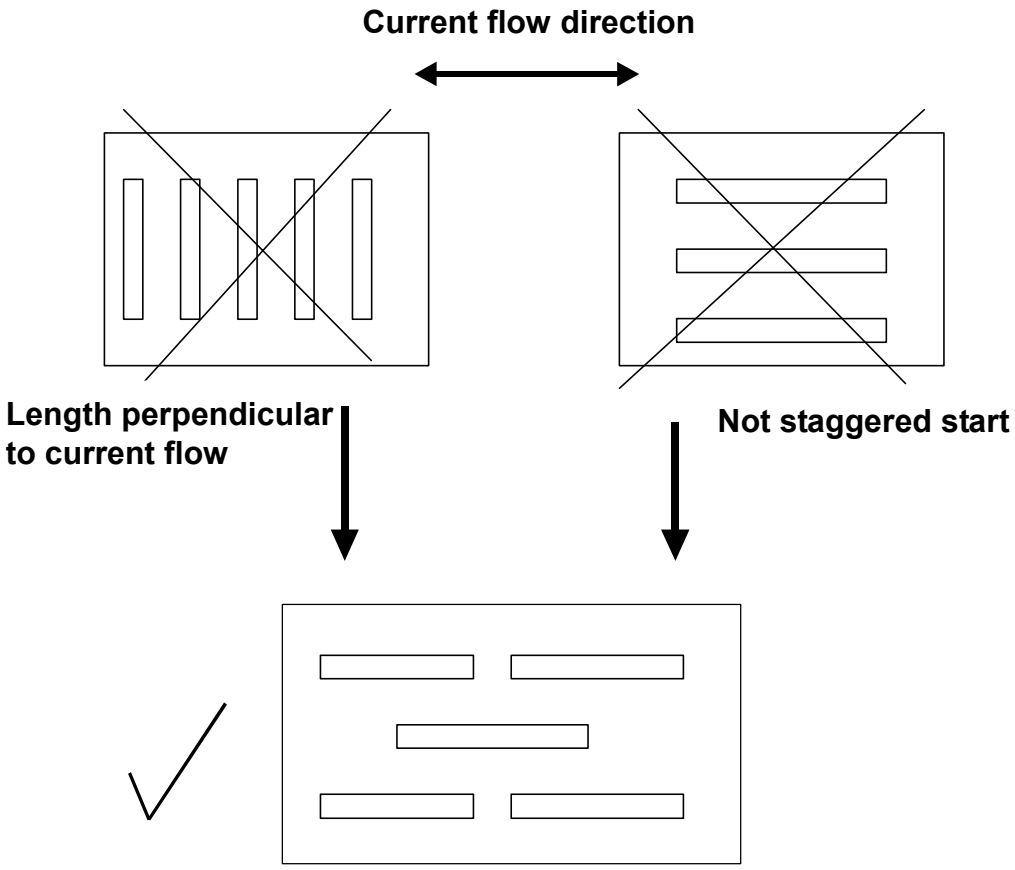
Not recommended slot Layout(2) – vertical & side by side slot



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V. Assembly Stress Protection -- dummy metal

Rule No.	Description	Label		Layout rule (um)
Guideline				
AMT.S.1	Maximum space between two MT features when the width of either MT feature is less than 10um. User should add dummy metal to meet the requirement	A	≦	10.0
AMT.W.1	Minimum width of a dummy MT block	B	≧	2.0
AMT.W.1	Maximum width of a dummy MT block	B1	≦	4.0
AMT.L.1	Minimum length of a dummy MT block	C	≧	2.0
AMT.L.1	Maximum length of a dummy MT block	C1	≦	10.0
AMT.S.2	Minimum space between a MT feature and a dummy MT block	D	≧	2.0
AMT.S.3	Maximum space between a MT feature and a dummy MT block	D1	≦	10.0
AMT.S.4	Minimum and maximum space between two neighbor dummy MT blocks	E	=	2.0
AMT.R.1	Minimum number of dummy MT blocks to be put in a large open area beside a MT feature.	F	≧	3.0

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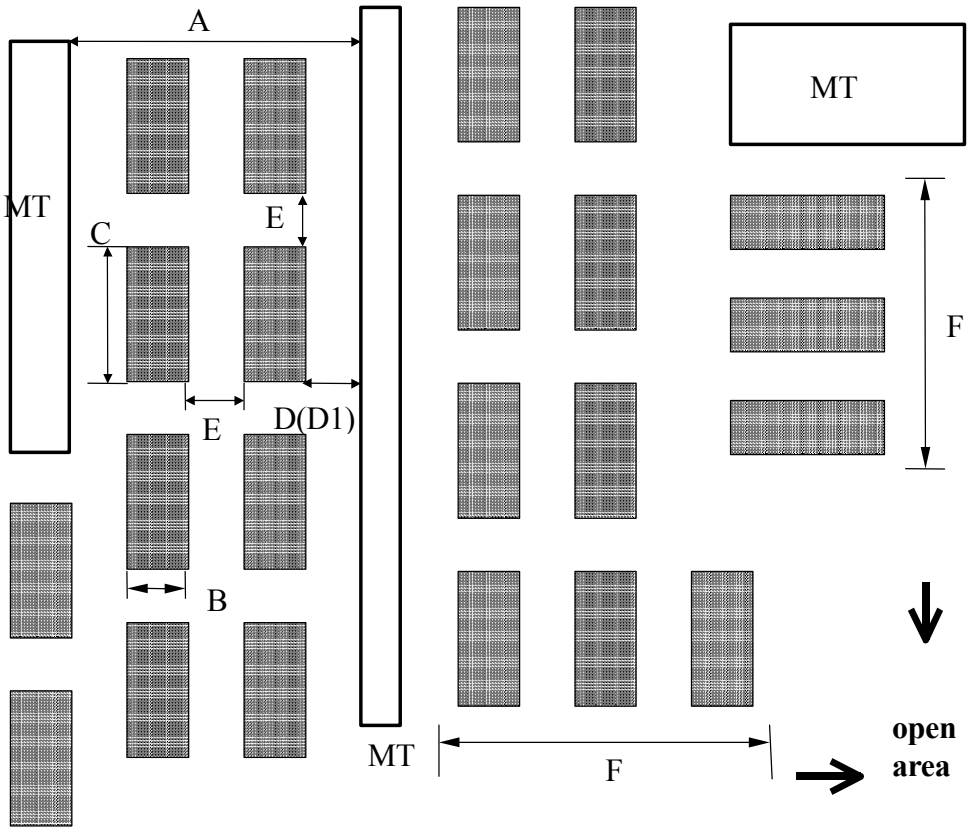
Dummy MT(Top Metal)



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Note for High Reliability Applications

If your products will be used in high reliability requirement applications, such as automotives, please contact TSMC account manager for the associated document.

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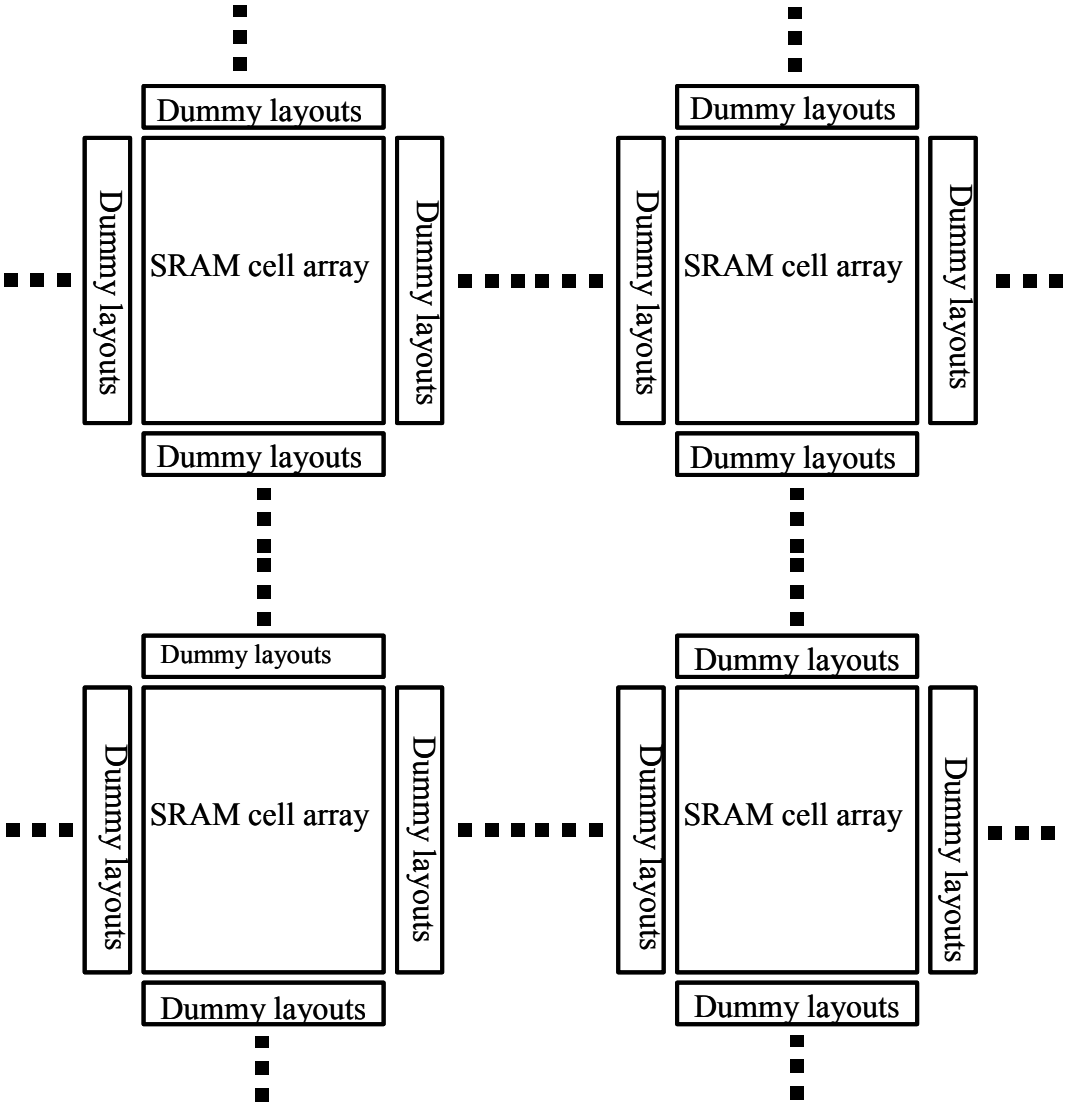
SRAM Guideline

1. Customer-designed SRAM bit-cell must be approved by tsmc's R&D and PE in order to guarantee SRAM cell electrical performance
2. Please don't use logic SPICE model to design SRAM unless it strictly follows logic design rule to design SRAM and approved by tsmc's R&D and PE.
3. For accumulated SRAM density >1.5M bits, redundancy is needed. Please refer to the most updated version of "TSMC 0.15um/0.18um/0.25um SRAM engineer report of SRAM redundancy for C025/C018/C015 " (document no.:T-018-SM-RP-001) as embedded SRAM redundancy guideline.
4. Dummy Layouts for Embedded SRAM
   - If SRAM cell arrays are used, dummy layouts must be added to provide similar surrounding for every cell so as to evade proximity and loading effect.
   - Please refer to these guidelines and their GDS-II examples in TSMC SRAM cell layout documents to add dummy layouts, in both column and row, at array edge and at connection/tap in-between arrays as follows.



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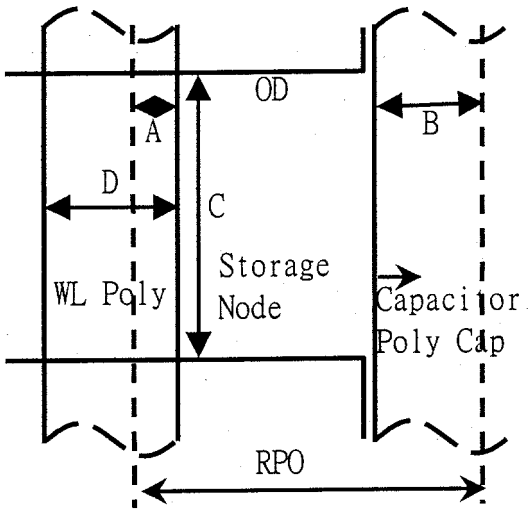
❑ Planar capacitor Emb-SRAM Rule

Please Use RPO blocking on storage node to avoid salicide formation. It is “must” for RPO on storage node.

Rule No.	Description	Layout rule (um)
T1.O.1	RPO overlay with WL Poly	A = 0.03
T1.O.2	Minimum RPO overlay with capacitor Poly Cap	B ≧ 0.05
T1.R.1	Borderless CO is forbidden. I(Please follow CO.E.1)	
T1.R.2	Use of minimum OD with(C) & poly width (D) for pass gate is forbidden (exceed at least 0.01um) to avoid short channel & narrow width effects.	

* Please follow RPO pitch rules RPO.W.1, RPO.S.1



* Above rules are not supported by DRC commend file

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