Assignment 5

Reference Unit: Unit 7 Memories

Background: Spice, Circuit level CMOS Design, Transistor Dimensioning

Objectives:

1) Design and Verify a 6T SRAM Cell

Support: Refer to Unit 7 Lecture Slide Set.

Tasks:

Write down a single .cir file in spice that is self –contained (You can use as many sub-circuit as you want, but you should copy/paste them all in a single .cir file). Use the pt/nt macros as basic MOS elements.

a) Design a 6T SRAM cell, using the following template:

```
.subckt T6_MemCell bitline bitlinen wordline  vdd vdds gnd gnds
[ ….. ]
.ends
```

b) Build a circuit composed by two different instances of the subcircuit above, sharing the same bitlines but with independent wordlines

c) Write down Stimuli in order to verify the cell behavior, in the following manner: Write a 1 on cell 0, a zero on cell 1, then read cell 0 and then read cell one. You are free to use PWL sources or additional CMOS component to generate your stimuli in order to guarantee the behavior described above.

d) Propose a dimensioning of the 6T cell transistors in order to obtain the smallest possible area while preserving the correct functioning. Define area supposing each unity of Wm# used as 1 μm^2 similarly to what already done in Assignment 4.

e) Add now 6 more cells (with independent wordlines) connected to the same bitlines. Repeat the same write/read cycle on the first two cells. Does the transistor dimensioning still hold?

Deliverables:

a) Self-contained cir file containing all material described above, with only the final dimensioning of 6T cell transistors. Only pt_ and nt_ macros can be used as libraries
b) 6-slide report based on the template available on Canvas. The report should contain, among any other info you believe significant:
   - Screen capture of one write and one read cycle with detailed description of the cell functioning
   - Final area value
   - Description of criteria used for transistor balancing