ENSC 450: Register File

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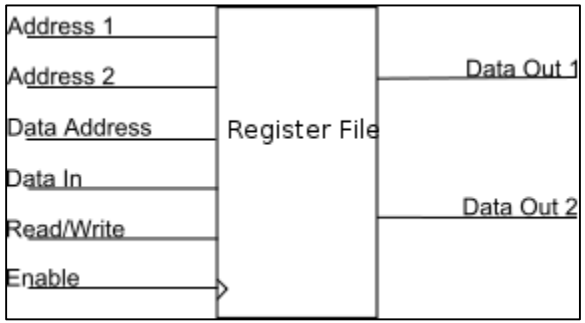
Outline

- Scope of Presentation:
  - Designed Register File in VHDL
  - Performed automated layout implementation of Register File
  - Record timing anaylsis and understand design trade-offs
- Description of Register File
- Methodology: Front End & Back End Design
- Results
- Conclusion

Register File

- Contains 32 16-bit registers
- Block Diagram:



Single Register:

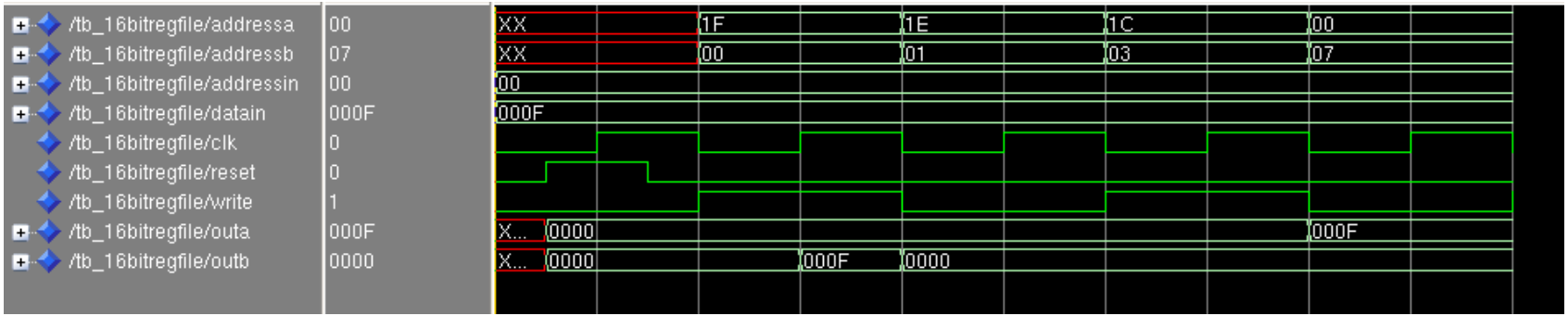
```
SingleReg: process(clk,reset,write)
    begin
    if reset = '1' then
        Reg <= X"0000";
    elsif (clk'event and clk = '1' and write = '1') then
        Reg <= data;
    end if;
end process SingleReg;

dataOut <= Reg;
```

- Functions:
  - Writes data to specified Data Address location when Write is enabled
  - Outputs data from specified Address1 and Address2 registers
- VHDL was written by ourselves, with Fabio's assistance

Register File (2)

- Application:
  - Used as temporary storage inside CPU to store values, such as computational, counters, pointers, etc.
- Testbench Inputs:
  - AddressA, AddressB, AddressIn, DataIn, Clk, Reset, and Write signals as shown below



Methodology – Front End Design

- Using ModelSim, simulate testbench for expected behaviour
- Using Synopsys Design Complier, perform logic synthesis
    - To evaluate the best possible achievable performance and area/power penality, synthesis design unconstrained (at a high period) and constrained (at the faster possible period)
    - Evaluate timing, area, and power results
- Optimize Design by selecting reasonable period
- Using ModelSim, verify expected behaviour of synthesized netlist

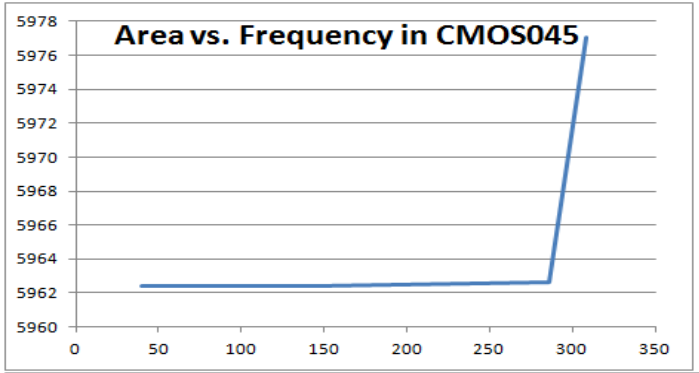
Synthesis Results

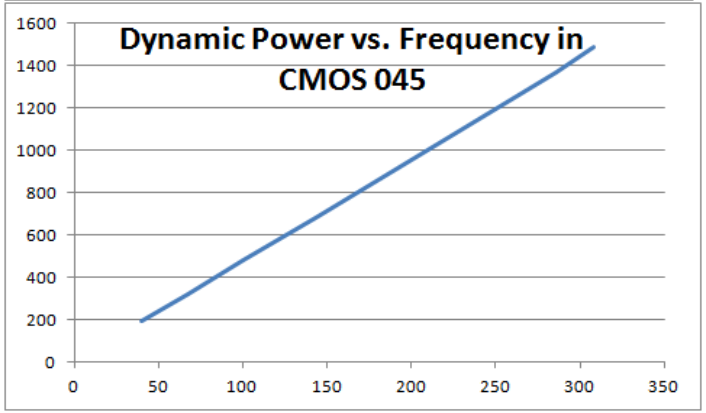
Period (ns)	Frequency(MHz)	Area (um^2)	Data Arrival Time (ns)	MET/VIO	Total Dynamic Power (uW)
3.25	308	5977.020115	2.44	MET	1487.3
3.5	286	5962.656114	2.6	MET	1367.8
7	143	5962.390114	2.6	MET	683.8518
10	100	5962.390114	2.6	MET	478.6962
15	67	5962.390114	2.6	MET	319.1308
25	40	5962.390114	2.6	MET	191.4785

- Critical Path: from addressA[1] to outA[0]
  - Longest delay is input external delay = 0.80ns
  - Input external delay is due to input and output wires parasitic from the clock to the register
  - Total data arrival time = 2.60ns

Optimization

- Plotting the results:
  - The highest frequency we can run our circuit at without compromising area is at 286MHz
  - Additionally, 40Mhz is the lowest frequency we can run our circuit at without violating setup times
- Thus, we will perform Back End Design at 286MHz (period = 3.5ns) and 40Mhz (period = 25ns)





Methodology – Back End Design

- Using Encounter and scripts provided, perform:
  - Import Design & Floor Planning
  - Placing & Optimization
  - Clock Tree Synthesis & Optimization
  - Routing & Finishing
- Checked session logs for errors and major warnings. Also, checked reports for design violations
- Analyzed timing reports and summaries

Constraints

- Using TT transistor characteristics with 045nm technology at 25^{o}C, constrained design with a 3.5ns and 25ns clock period.
- Fitted design into a chip with an area of ~8000um^{2}.

Period	Max Clock Skew	Max Latency
20ns	0.625ns	3.29ns
3.5ns	0.686ns	3.28ns

- Floor plan density = 90%

Back End Design Results

- Period 3.5ns:

Stage	Number of Cells	Cell Area µm2	Density	Data Arrival Time
Post-Synthesis	3647			2.3439
Placing	3518	5807.844	87.66%	2.65340
Post-Place OPT	3567	5852.798	88.34%	2.61520
CTS	3682	5872.748	88.64%	2.61780
Post-CTS OPT	3582	5874.344	88.66%	2.57260
Routing/Signoff	3582	5874.344	88.66%	2.55380
Finishing	4667	5874.344	99.90%	2.55380

- Period 25ns:

Stage	Number of Cells	Cell Area µm2	Density	Data Arrival Time
Post-Synthesis	3647			2.34391
Placing	3518	5807.578	87.66%	2.67560
Postplace OPT	3527	5801.194	87.56%	2.68840
CTS	3542	5821.144	87.87%	2.67830
Post CTS OPT	3542	5826.996	87.95%	2.6266
Routing/Signoff	3542	5826.996	87.95%	2.68661
Finishing	4880	5826.996	99.90%	2.68661

- Since our circuit is a Register File, speed is important. Hence, it would be best to run at 3.5ns for faster arrival time, despite small increase in area and density

Back End Design Results (2)

- After performing Place & Route, we were happy with our results because we didn’t have any unresolved violations in our circuit.
    - Thus, no changes to Floor Plan or constraints were applied.
- During optimization steps, trial routing was performed to estimate wire loads and delays
    - Buffers were inserted to decrease timing delays

Conclusion

- Chose to conclude with a Register File made with 45nm technology and 3.5ns clock period
    - Compared to the 25ns clock period, area is basically the same
    - Can run 5% faster than 25ns clock period
- At Period=3.5ns, the performance of our device is:
    - Area of Standard Cells: 5874.344 μm^2
    - Cell Utilization: 88.755%
    - Core Density (without filler cells): 88.66%
    - Unresolved violations and problems: None
    - Data Arrival Time: 2.55380 ns