# ENSC 450: Assignment 3


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# Outline

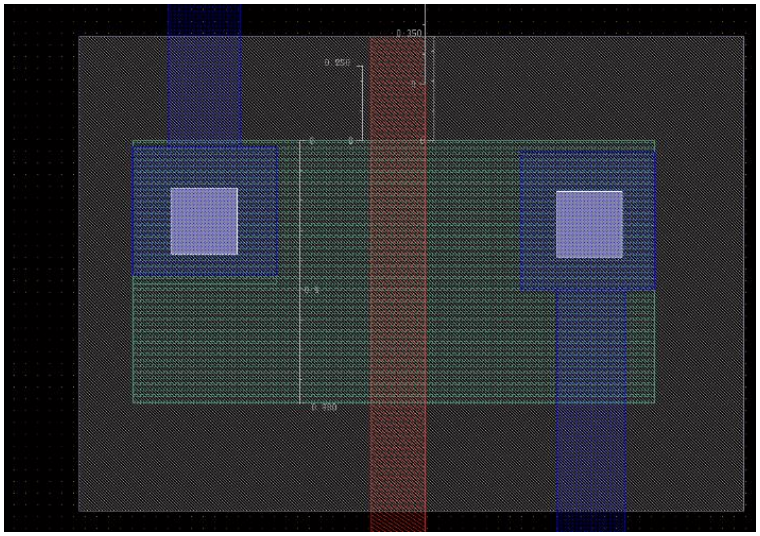
- Scope of Presentation:
  - Designed schematics and layouts of an Inverter cell
  - DRC/LVS Checks operated over layout design
  - Simulated extracted schematic from layout design
  - Modified schematic and layout design to have equal rise and fall output transition times
- Methodology Used
- Results
- Conclusion

# Methodology

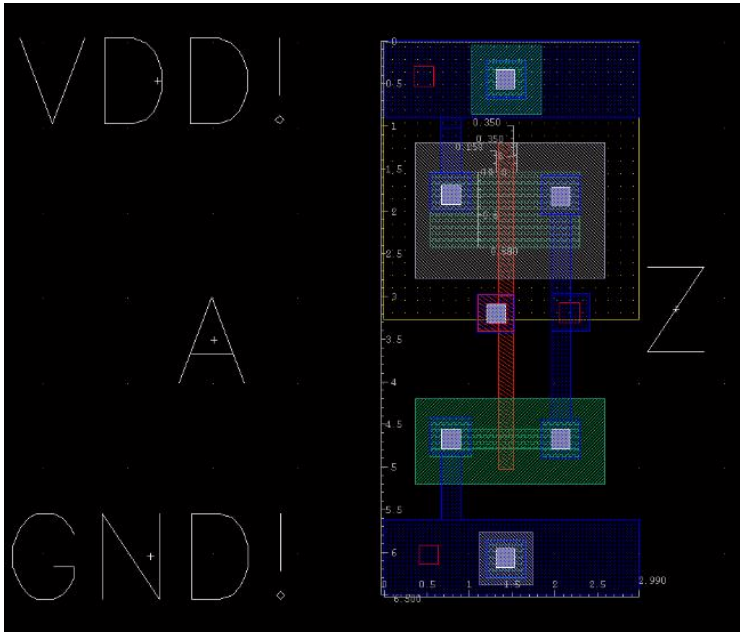
- By following the provided Layout Tutorial:
  - Designed and simulated schematic of Inverter cell with Width(PMOS) = Width(NMOS)
  - Designed and simulated a DRC-&-LVS-free layout of Inverter cell with Width(PMOS) = Width(NMOS)
  - Simulated net-lists of schematic and extracted circuits by HSPICE
- Since schematic and extract circuits match, modify the PMOS width of one net-list such that rise and fall output transition times are equal
  - Implemented corresponding changes to schematic and DRC-&-LVS-free layout designs
  - Simulated new designs

# Results

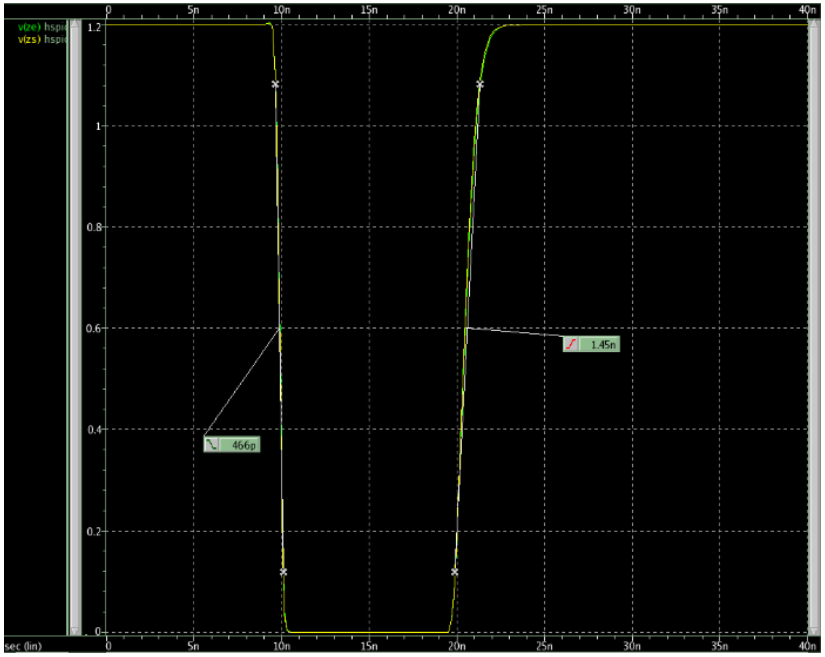
Final layout showing modifications made



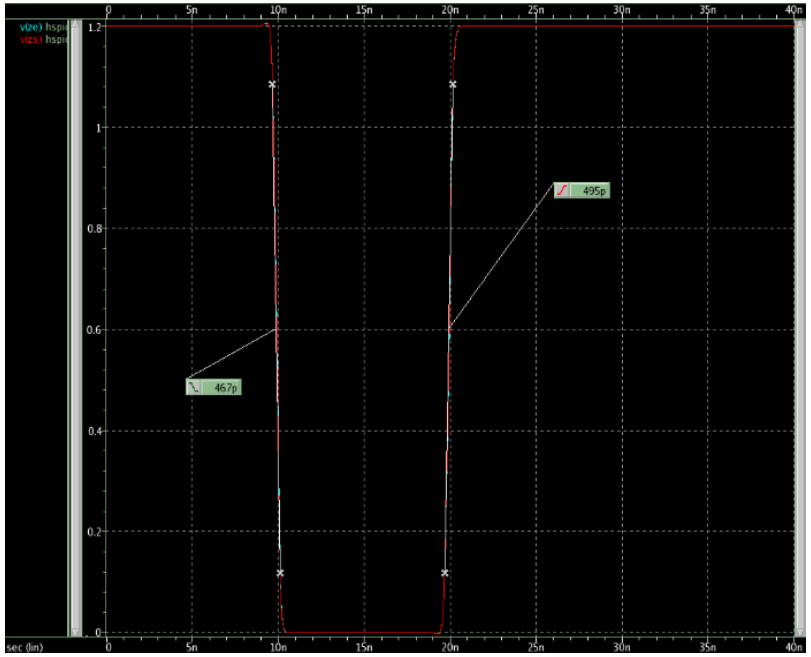
Screen capture of final layout




Spice Simulations Waveform (post layout) Task 1




Spice Simulations Waveform (post layout) Task 2



# Results (2)

| | Task 1 | | Task 2 | |
|---|---|---|---|---|
| | **Simulated** | **Extracted** | **Simulated** | **Extracted** |
| Area | 9.0087um | | 11.8854um | |
| Propagation Delay of Rise Time | 0.97091ns | 0.99032ns | 0.43791ns | 0.4212ns |
| Propagation Delay of Fall Time | 0.40215ns | 0.40826ns | 0.41639ns | 0.42190ns |
| Total Rise Time | 1.3936ns | 1.4404ns | 0.48308ns | 0.48919ns |
| Total Fall Time | 0.45432ns | 0.46275ns | 0.45759ns | 0.46181ns |

# Conclusion

- Modified the PMOS width to 880nm, from task(1) design of 220nm
  - On schematic, adjusted PMOS properties to W=880nm
  - On layout, stretched active layer of PMOS to W=880nm
  - To not violate any design rules, stretch Pplus layer such that Pplus-Extension-Over-Channel W≥ 350ns
- Since PMOS is used as a Pull-Up network, it determines the rise transition time of our inverter.
  - We increased the width of the PMOS in order to decrease it's rise transition time because PMOS transistors rely on hole mobility which is slower than electron mobility.
  - Thus PMOS must be wider in order to provide the same current. With a width of 4 times the width of the NMOS, the difference between our fall and rise transition times from both the extracted and simulated netlists is ~6%.