Assignment 3

Reference Unit: Unit 3 Layout and Cell Area Estimation

Background: CMOS Schematics and Layout, Design Rules, DRC/LVS Checks

Objectives:

1) Use the Cadence Virtuoso Suite to design schematics and layouts of basic StdCells
2) Modify the schematic and layout design to meet timing constraints
3) Extract and simulate a schematic from a layout description
4) Perform LVS/DRC Checks over a stdCell layout

Support: Refer to LAYOUT tutorial on /ensc/fac1/fcampi/Tutorials/Layout. The layout tutorial document is not available on Canvas due to the need to restrict circulation of design rules…

Tasks:

1) Design Schematic and Layout of an Inverter cell with Wp =Wn based on the tutorial available on /ensc/fac1/fcampi/Tutorials/Layout . Perform DRC and LVS cell until both yield positive results. Simulate both the schematic and the extracted circuits and measure Propagation delay and output transition time in the two cases
2) Modify your design in order to obtain symmetrical behavior between raise and fall output transition times. Perform DRC and LVS until both yield positive results. Simulate schematic and extracted circuit and measure raise and fall Propagation delay and raise and fall output transition time in the two cases

Deliverables:

1) Provide a zip file containing, for the circuits and layouts specified at task (1) and (2):
    a. a .cir spice decks similar to /ensc/fac1/fcampi/Tutorials/Layout/hspice/inv_layout.cir containing schematic and extracted layout netlist
    b. Screen captures of LVS and DRC results in pdf or jpg format
    c. Screen captures of schematic and layout GUI in pdf or jpg format

2) Provide a 6-slide report based on the template available on Canvas. The report should contain, among any other info you believe significant:
    a. Description of the modifications you performed on the layout resulting from Task (1) to meet Task(2) requirements and (brief) theoretical explanation for such modifications
    b. Screen capture of the final layout picture (Clearly showing the modifications described above)
    c. Spice simulation waveforms (post layout) of the two circuits of task(1) and task (2) (Possibly showing the two V(z) on the same panel)
    d. One table showing differences between the two circuits of task (1) and (2) in terms of Area, Propagation Delay and Output transition time for both Raise and Falling edge (You are welcome to use /ensc/fac1/fcampi/Tutorials/Layout/hspice/inv_layout.cir as reference for defining measurement statements)

In case for some reason your design is not DRC or LVS free, state it clearly in the report!