

# ENSC 450: Assignment 5

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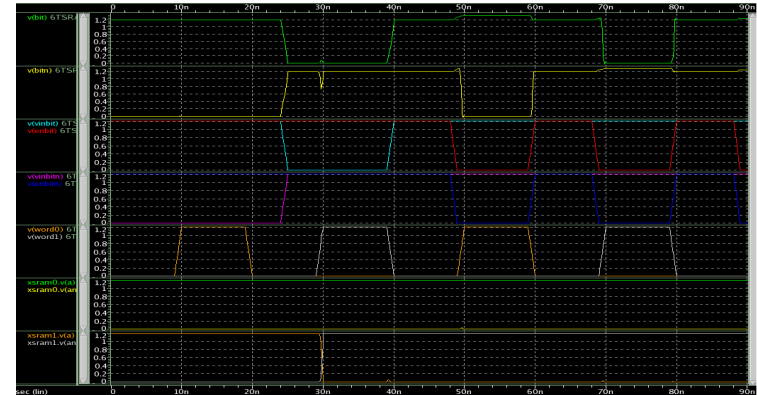
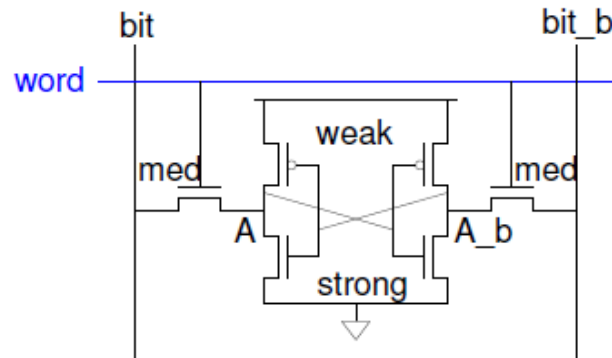
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# Outline

- Scope of Presentation:
  - Built 6TSRAM subcircuit
  - Instantiate 2 cells: cell 0 and cell 1
  - Want to write one into cell 0, zero into cell 1, read from cell 0, and read from cell 1
  - Optimization of criteria for transistor balancing
- Methodology
- Results
- Conclusion

# Methodology

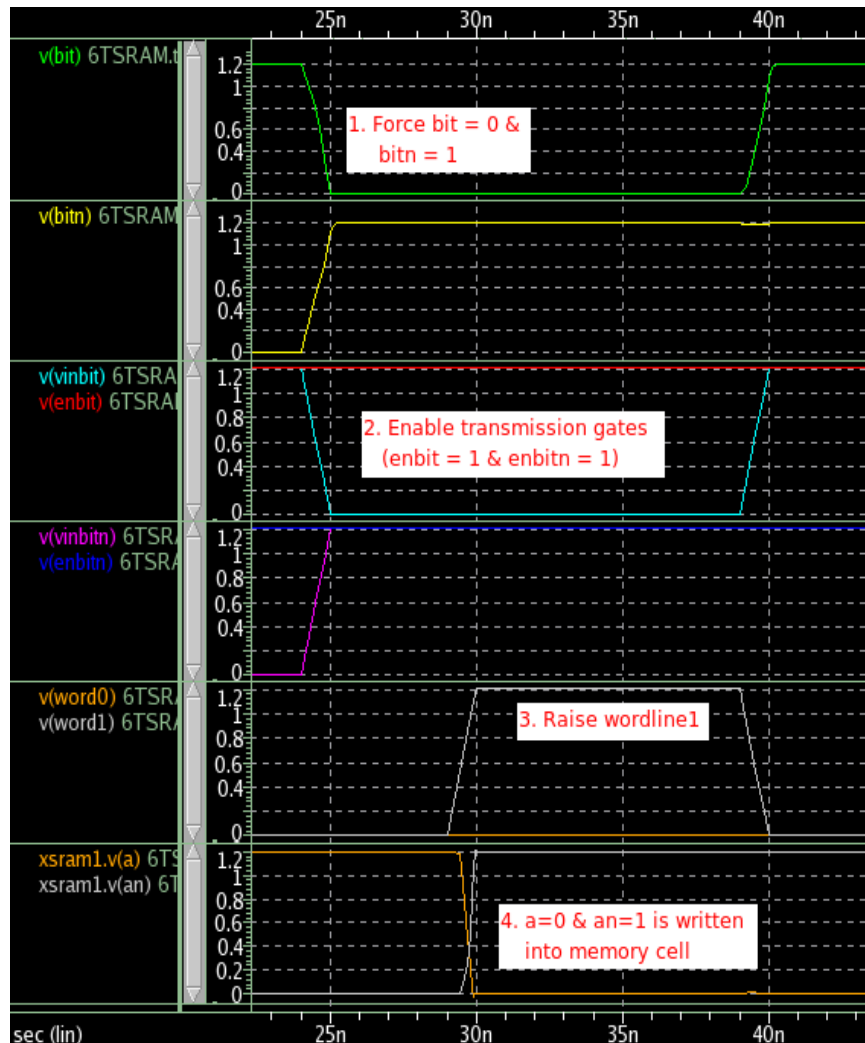
- Built SRAM using 6 transistors with PMOS having width  $2 \cdot W_m$  and NMOS having width  $W_m$



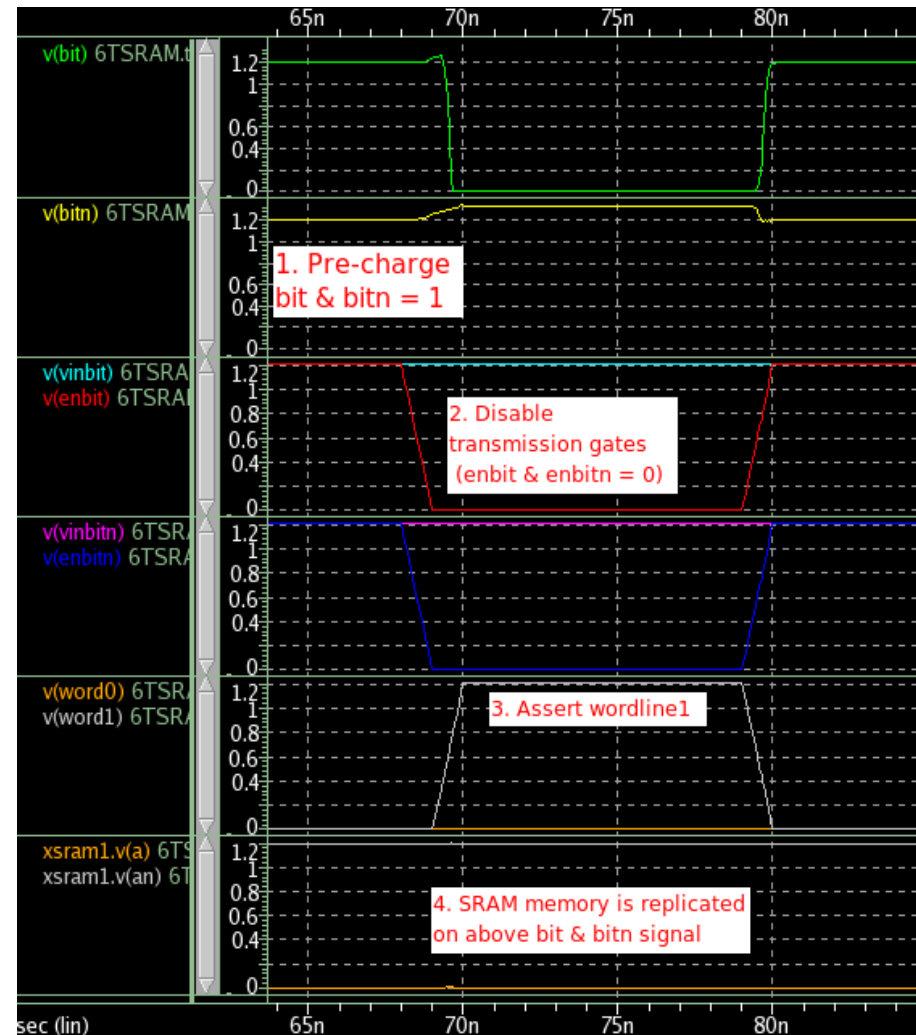
- Instantiated 2 SRAM subcircuit: cell 0 and cell 1
- Want to write one into cell 0, zero into cell 1, read from cell 0, and read from cell 1
- Added transmission gates for bitlines in order to control when bitline is an input and when it's an output
- Write:
  1. Force desired value onto bitline by enabling transmission gate
  2. Raise wordline
- Read:
  1. Pre-charge bitline and bit\_b to 1
  2. Disable transmission gates
  3. Raise wordline
- Once the SRAM was able to be correctly written into and read out from (above waveform diagram) we determined the minimal widths of the transistors.
- After the minimal width was determined we moved on to building an extra 6 SRAM cells

# Results

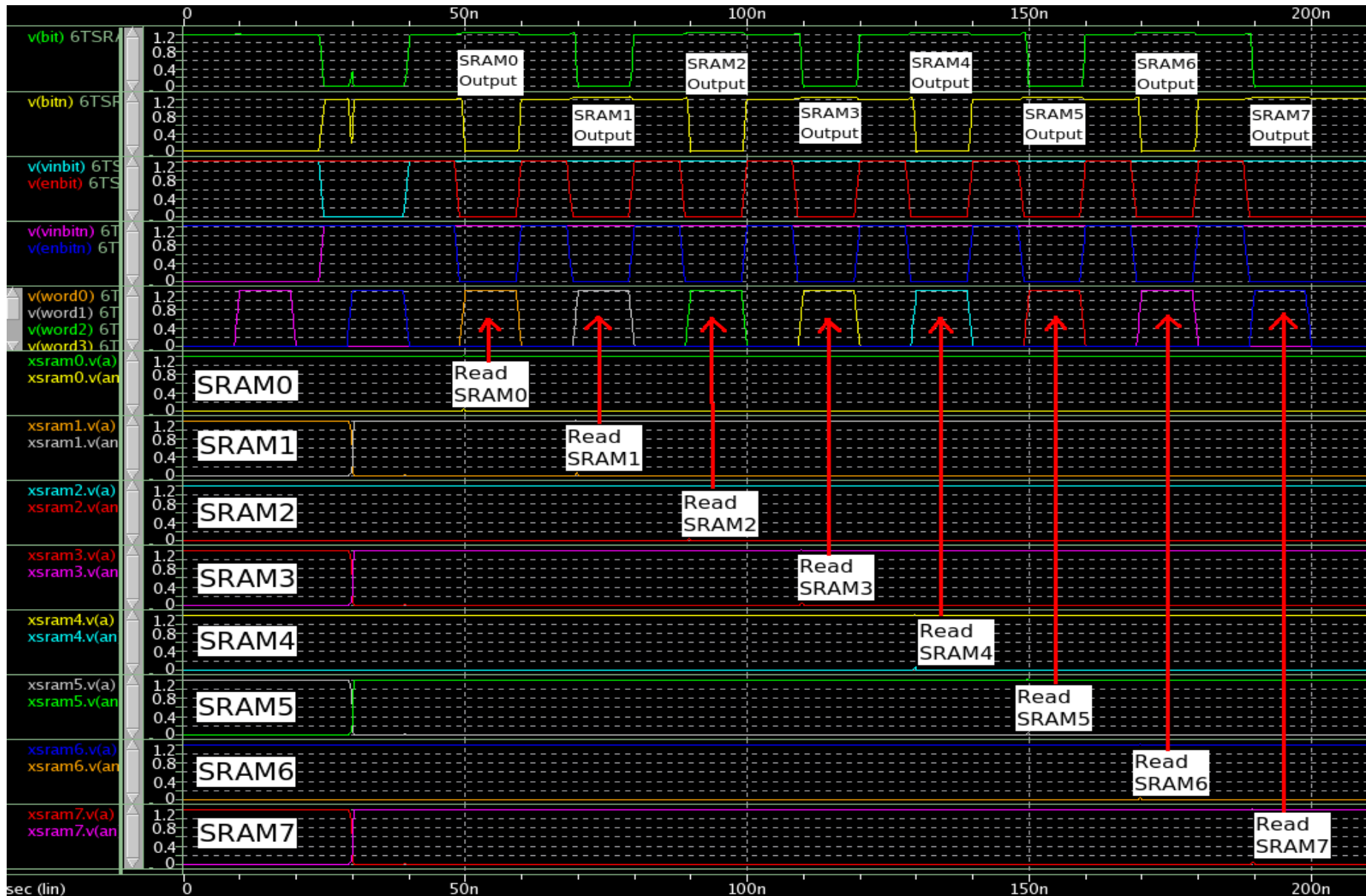
- Write 0 into cell 1



- Read 0 from cell 1



# Results (2)



# Conclusion

- Final area of 8 SRAM cells is  $6*8*1 = 48\mu\text{m}^2$
- We decided leave all PMOS and NMOS transistor widths to just  $W_m$ 
  - From the diagram below it is evident that this balancing works
  - With such small areas we can have higher density and lower power consumption in a cell