ENSC 450: Assignment 2

Barry Yim byim@sfu.ca

Cheng Jie (Jadan) Ou jou@sfu.ca

Bonnie Ha bha20@sfu.ca

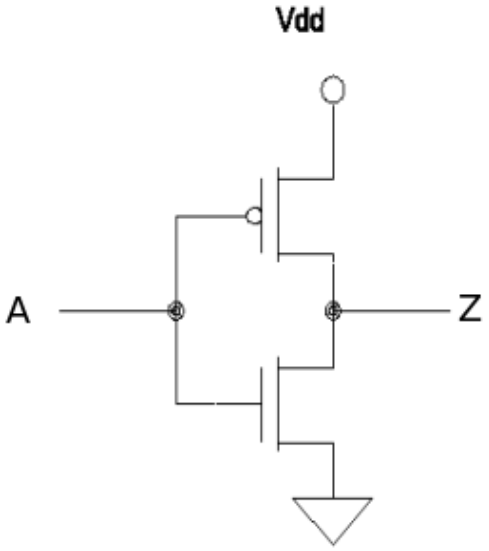
Outline

- Scope of Presentation:
  - Perform CMOS logic cell analysis, using HSPICE circuit simulator
  - Determine the size of internal transistors to yield raise/fall Output Transition Time <100ps
  - Evaluate the setup and hold time of the Flip-Flop designed considering clock transition time of 100ps.
- Methodology Used
- Results
- Conclusion

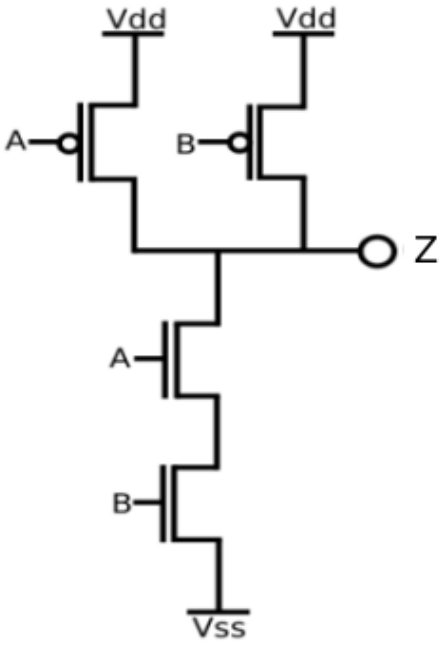
Methodology (1)

- Designed simple logic gates using HSPICE

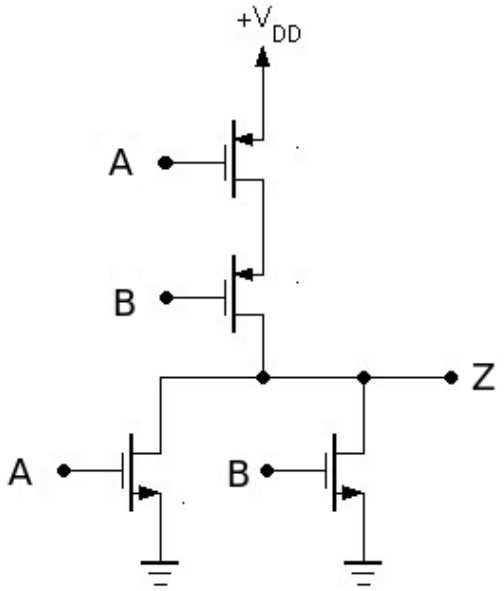
INVERTER



NAND



NOR



Logic of AND gate

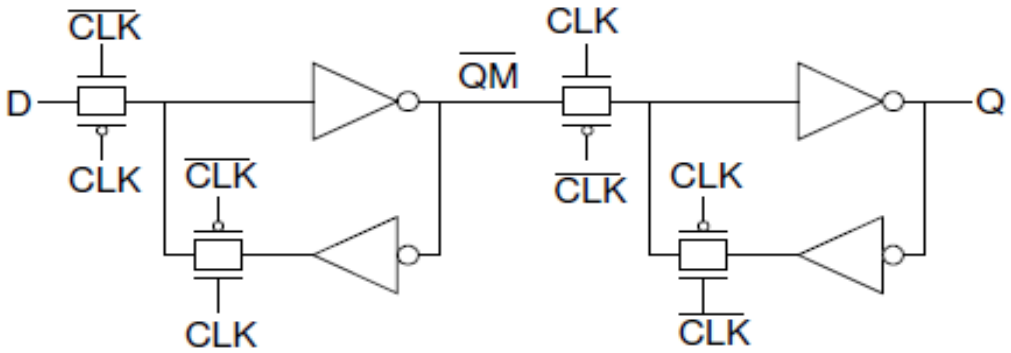
```
Xnand a b d vdd gnd vdds gnds NAND Wn=Wm#
Xinv d z vdd gnd vdds gnds INV Wn=Wm#
```

Logic of OR gate

```
Xnor a b d vdd gnd vdds gnds NOR Wn=Wm#
Xinv d z vdd gnd vdds gnds INV Wn=Wm#
```

Methodology (2)

- Designed a Flip-Flop using logic gates from Methodology 1
- Varied size ratio between PMOS and NMOS transistors in order to decrease rise and fall times to below 100ps
- Determined the setup time of FF by continuously decreasing the time frame between input transition (D) and clock transition until output (Q) becomes distorted
- Pin pointed the hold time of FF by changing the input (D) soon after clock begins to rise, and viewing output to see if desired waveform is produced
- Reduced setup time until greater rise/fall transition times were observed

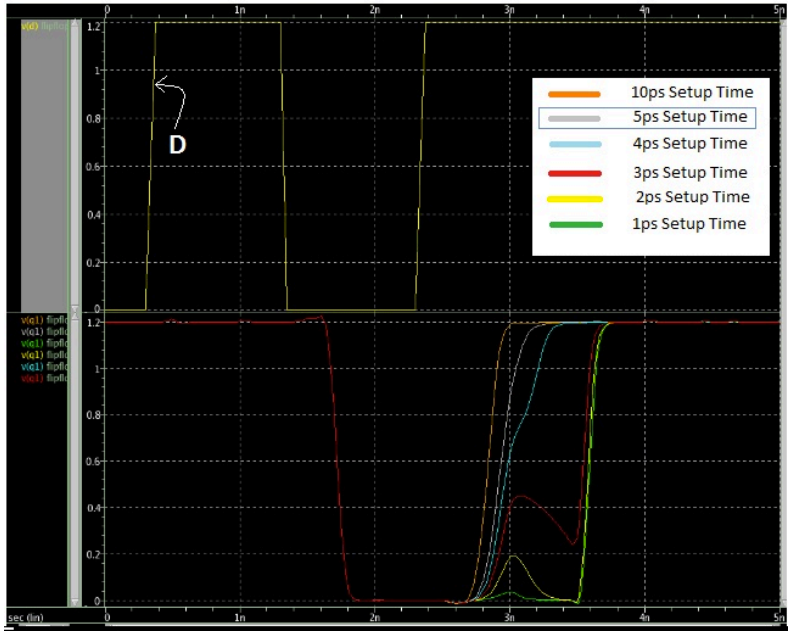


Flip Flop

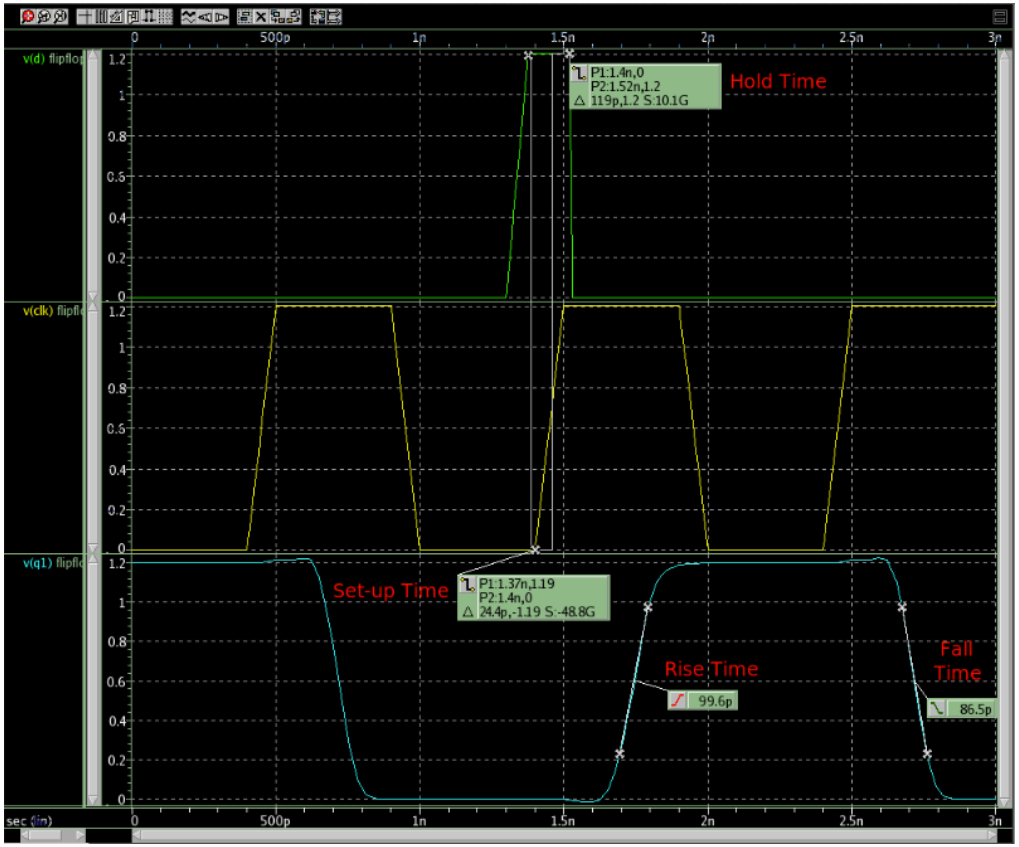
Results

Logic Operation	Number of Transistors
AND	6
NAND	4
NOR	4
OR	6
INVERTER	2

Setup Time Waveforms with Greater Rise Times

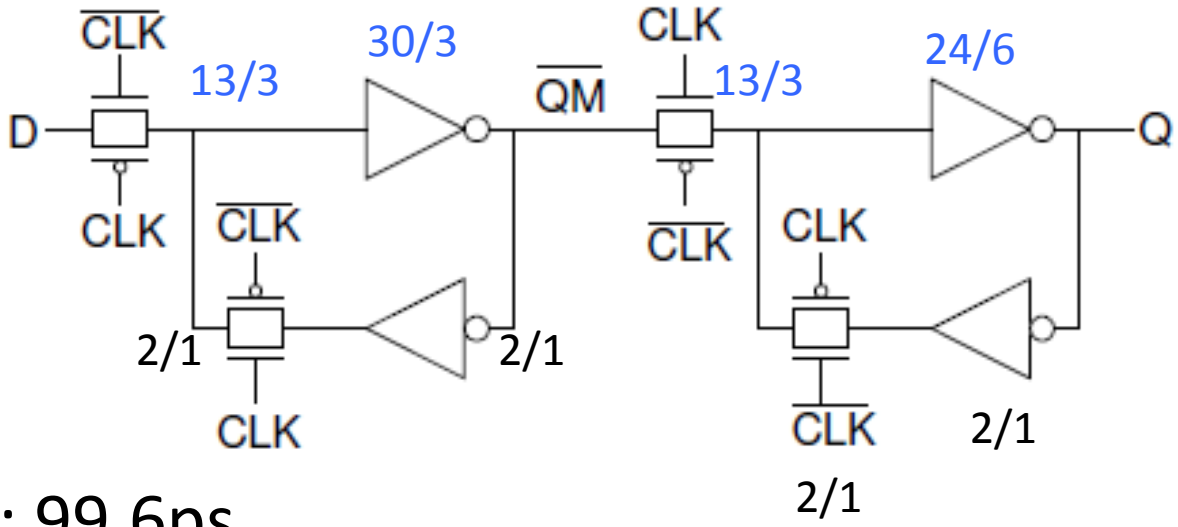


Final Results:



Conclusion

- Width Ratios of PMOS/NMOS:



- Rise Time: 99.6ps
- Fall Time: 86.5ps
- Set-up Time: 25ps
  - If <25ps, then rise time would increase >100ps
- Hold Time: 120ps
  - If <120ps, then output is distorted