Final Project

Reference Units: Unit 1, 5, 6

Background: VLSI Design Flow from HDL coding to layout

Objectives:

1) Explore all steps and design tradeoffs in the Automated layout implementation of a given HDL core

2) Utilize the Cadence Encounter Design implementation suite

Support: Refer to Tutorial rgb2gray [/ensc/fac1/fcampi/Tutorials/rgb2gray, https://canvas.sfu.ca/courses/13105/files/809693/download?wrap=1] for details

Tasks:

1) Identify a VHDL suite (One or more files) that performs a significant task. Example of such suite can be

i) A simple processor/DSP core (There are few examples available at http://opencores.org/ or I can provide some examples)
ii) A mathematical core: a good example could be a complex multiplier, a programmable shifter, ...
iii) A signal processing core such as a FIR filter, an FFT core, or something along those lines
iv) An image processing core such as a binarization engine, the rgb2gray of the Tutorial, ...
v) An on-chip communication/storage primitive: a DMA, a FIFO device, a Network-on-chip component (A switch/repeater), a Register File
vi) Cores coming from a project you developed, maybe on FPGA, in previous courses (If the upgrade of the HDL is not too complex)

If you can't propose anything suitable, please ask the instructor.

2) Set up a HDL test-bench for the proposed core simulation, and set tentative area, power, timing constraints for your device depending on its nature and its application field (Those can be refined further along the project) . Perform logic synthesis and estimate power, timing and area of the resulting netlist

3) Perform Post-Synthesis Verilog simulation on your post-synthesis netlist to verify the correctness of the synthesis

4) Following the rgb2grayscale tutorial, provide a layout implementation of the core using Cadence Encounter. Perform post-layout simulation on the netlist to verify the correctness of the process.

5) Depending on the implementation results, discuss eventual optimization with the instructor

Suggested Timeline for the project:

November 9: Selection of HDL, completion of Testbench, Logic Synthesis, post-synthesis simulation. Deliver 1 or 2 powerpoint slides describing the chosen code and its utilization

November 16: First round of P&R, post-layout simulation. Deliver 1 or 2 powerpoint slides describing P&R results compared to FE results and eventual issues encountered during P&R. Discuss optimization options with instructor.

November 16-29: Fixing eventual problems/bugs/Issue, implementing implementations, and eventual further required analyses

December 2-8: Project final discussion

Deliverable 1: Deliver (Via Canvas, no email due to file size) a tgz package containing

a) ***All related hdl files***
b) ***Synthesis script***
c) ***Complete set of final P&R scripts (including .conf and .cts)***
d) ***Post-synthesis and post-layout Verilog***
e) ***Final Post-layout DEF***

Deliverable 2: Deliver via email and/or on Canvas a 10 to 15 slides ***PDF*** file based on the assignment report template. Please use PDF format! The file should clearly report, in form of powerpoint presentation:

a) Application field of the HDL core, source, explanation of its functioning and of the inputs utilized in the test-bench
b) Final version of the constraints (Including BE constraints such as Floorplan, clock Skew and latency)
c) Synthesis Results (Timing, Area, Power). In particular, carefully describe the critical path!
d) Description of issues/challenges met during the Place&Route process
e) Description of chosen optimizations / analyses (try to be quantitative, show temporary results and explain how you planned to enhance them).
f) Final results (Floorplan, area, cell utilization, density, eventual unresolved violations and problems), Power analysis, Timing analysis

Project Presentation: The PDF file should be handed contextually to a presentation in the instructor's office, STRICTLY before the final exam date. A set of available time slot for the presentation will be published shortly and filled on a first-come first-served basis. ***Projects won't be graded if not presented before the exam date.***

<u>Projects will be graded with the very same criteria of Assignments. Refer to the following table for details:</u>

40 %	All designs and analyses ***<u>explicitly required by the assignment text</u>*** were fully completed and reported
20 %	All designs and analyses ***<u>NECESSARY</u>*** to a consistent reporting, even if not explicitly required in the text, were fully completed and reported
20 %	All design and analyses ***<u>information</u>*** NECESSARY to a consistent reporting were provided explicitly and in an understandable format in the report
20 %	The report conclusions demonstrate clear understanding of the performed work
10 %	The report format is clear and consistent with the specifications provided on the course website and during lectures