Assignment 4

Reference Unit: Unit 5 Delay, Power and Wires

Background: Design and Characterize Std Cell libraries at Spice level, definition of a liberty file, HDL synthesis on a custom made Standard Cell library

Objectives:

1) Use HSPICE to characterize a simple combinational std cells library
2) Manually describe and compile a liberty file
3) Understand the utilization of *liberty* (.lib) files in logic Synthesis
4) Optimize a HDL design by adapting the underlying StdCells library

Support: Use as reference all information available in /ensc/fac1/fcampi/Tutorials/liberty. In particular copy/paste to your folder the file Liberty/SpiceLib180_TT_1.2_25C.lib . *Remember to change its name and content appropriately.*

You will have to modify this file in the course of the assignment.

Tasks:

1) Using TSMC 180nm, describe a spice cir file that represents a minimal standard cell library for logic synthesis [A minimal StdCell library must be composed of at least a NOT_X1, a NOR_X1, and a NAND_X1]. With the experience gained during layout, use a Wp/Wn ratio that makes in/out transition symmetrical (range of 5/10%). Determine manually the width of each MOS in terms of Wm# (220nm) in order to preserve the unity inverter behavior also for the NAND and NOR.

2) Calculate manually the area of your cells supposing each unity of Wm# used as 1 μm^2; Calculate manually the Input capacitance of each node of each cell supposing the unity C (MOS with W=Wm#)=1pF. Fill the values you calculated in the .lib file

3) Choose Worst case reference conditions for your simulation: 1.05V, ss Transistors, 125C. Run HSPICE on the cells you have designed in order to fill the template liberty file timing tables for propagation time and output transition time. As you can see from the keyword lu_table_template you will need to repeat the measurements for

    - Cload = 1pF, 5fF Transition Time = 0.05, 0.10 ns

4) Compile the liberty file obtained with the following command (this is a synopsys tool, you'll need to source setup/FE_setup.csh):

    lc_shell-xg-t -x "read_lib <file.lib>; write_lib <Library name> -format db -output <file.db>; exit"

    Note, the library name is specified in the .lib file (you should customize it). Synthesize the design Assignment0.vhd of your previous assignment using the compiled library as target library. Determine the max speed allowed by your library, and the relative area cost.

5) Add new cells (one or more) in your liberty file in order to gain *at least* a 40% speedup in synthesis. Evaluate the cost in area of the new solution.

Deliverables:

a) .lib file of the final library (Including new cells). The .lib file MUST compile correctly into a .db file
b) .rpt files of the two synthesis
c) Vhd file of your Assignment0
d) Provide a 6-slide report based on the template available on Canvas. The report should contain, among any other info you believe significant:
    - Description of the spice simulations used to fill the liberty file
    - Description of all cells in your lib, with driving strength, area and input cap, specifying which cell(s) were added in a second time
    - PVT conditions used in simulations and synthesis
    - Description of critical path before AND after speedup INCLUDING transitions and Caps

Suggestion: Try to maintain, in all reports as well as in all Spice simulations, a consistent value of PVT. PVT impacts heavily the silicon performance, so having inconsistent PVT between cells is the worst error you can introduce in this type of assignment. Also, pay attention to units for any physical measurement (Time/Voltage/Capacitance/Temperature).