Lab 2: 1-digit BCD Counter

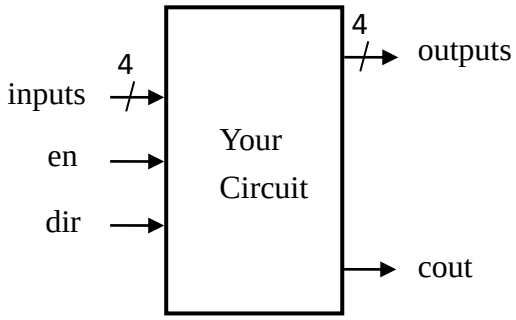
Due: 18:30, October 4, 2016

Objective

- Be familiar with Verilog and BCD counter

Action Items

1. Design a circuit that converts a 4-bit BCD number to its next or previous BCD number. The block diagram of the circuit is shown below.



- If en is 0, outputs = inputs and cout = 0.
- If en is 1 and dir is 1, the outputs and cout are as follows.

inputs[3]	inputs[2]	inputs[1]	inputs[0]	outputs[3]	outputs[2]	outputs[1]	outputs[0]	cout
0	0	0	0	0	0	0	1	0
0	0	0	1	0	0	1	0	0
0	0	1	0	0	0	1	1	0
0	0	1	1	0	1	0	0	0
0	1	0	0	0	1	0	1	0
0	1	0	1	0	1	1	0	0
0	1	1	0	0	1	1	1	0
0	1	1	1	1	0	0	0	0
1	0	0	0	1	0	0	1	0
1	0	0	1	0	0	0	0	1
1	0	1	0					
		⋮		0	0	0	0	0
1	1	1	1					

- If en is 1 and dir is 0, the outputs and cout are as follows.

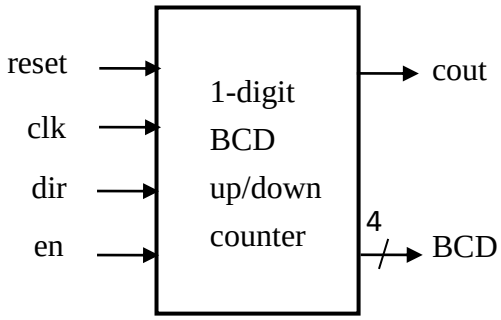
inputs[3]	inputs[2]	inputs[1]	inputs[0]	outputs[3]	outputs[2]	outputs[1]	outputs[0]	cout
0	0	0	0	1	0	0	1	1
0	0	0	1	0	0	0	0	0
0	0	1	0	0	0	0	1	0
0	0	1	1	0	0	1	0	0
0	1	0	0	0	0	1	1	0
0	1	0	1	0	1	0	0	0
0	1	1	0	0	1	0	1	0
0	1	1	1	0	1	1	0	0
1	0	0	0	0	1	1	1	0
1	0	0	1	1	0	0	0	0
1	0	1	0					
	⋮			0	0	0	0	0
1	1	1	1					

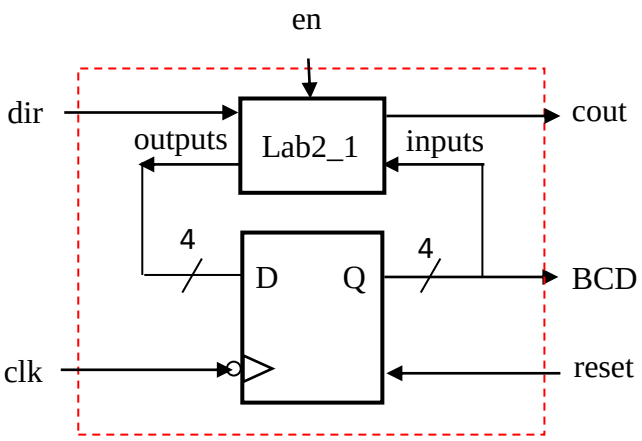
You have to use the following template for your design.

```
module lab2_1(inputs, en, dir, outputs, cout);
input [3:0] inputs;
input en, dir;
output [3:0] outputs;
output cout;
   // add your design here
endmodule
```

2. You have to create a testbench,which named Lab2_1_t.v by yourself to verify your design. In your testbench, you should try all the possible input combinations, and check if your design is correct or not. During demo, TA will ask you some questions about how you build your testbench.

3. Design a negative-edge triggered 1-digit BCD up/down counter whose block diagrams are shown below and test your module using the testbench file Lab2_2_t.v.





The clk is the clock signal. The reset is an asynchronous control signal which sets the counter to 0 (i.e., BCD=4'b0000) when it is 1. If en is 0, the counter remains unchanged; otherwise (i.e., en=1), the counter is incremented or decremented by 1 according to the value of dir. If the dir is 1, the counter is incremented; otherwise (i.e., dir=0), the counter is decremented. You must reuse your design of Lab2_1 to create the 1-digit BCD counter.

You have to use the following template for your design.

```
module lab2_2(clk, reset, en, dir, BCD, cout);
input clk, reset, en, dir;
output [3:0] BCD;
output cout;
   // add your design here
endmodule
```