	Result	Size	Time	Cycles	GPU	SM Frequency	Process	Attributes
Current	570 - init_cos_sin_table_kernel	(1, 1, 1)x(256, 1, 1)	2.69 us	3,839	0 - NVIDIA GeForce GTX 1660 Ti	1.42 Ghz	[41582] image	

Summary | Details | Source | Context | Comments | Raw | Session

Compare | Tools | View | Export

This table shows all results in the report. Use the column headers to sort the results in this report. Double-click a result to see detailed metrics. Double-click on demangled names to rename it.

ID	Estimated Speedup [%]	Function Name	Demangled Name	Duration [us] (2262.05 us)	Runtime Improvement [us] (1479.99 us)	Compute Throughput [%]	Memory Throughput [%]	# Registers [regi
0	95.83	init_cos_sin_table_...	init_cos_sin_table_...	2.69	2.58	0.17	1.51	
1	86.25	image_RGB2BW_ke...	image_RGB2BW_ke...	238.72	205.89	87.90	12.50	
2	62.46	noiseReduction_ker...	noiseReduction_ker...	225.92	141.12	46.61	48.68	

The following performance optimization opportunities were discovered for this result. Follow the rule links to see more context on the Details page.
Note: *Speedup estimates provide upper bounds for the optimization potential of a kernel assuming its overall algorithmic structure is kept unchanged.*

Small Grid
Est. Speedup: 95.83%

The grid for this launch is configured to execute only 1 block, which is less than the GPU's 24 multiprocessors. This can underutilize some multiprocessors. If you do not intend to execute this kernel concurrently with other workloads, consider reducing the block size to have at least one block per multiprocessor or increase the size of the grid to fully utilize the available hardware resources. See the Hardware Model description for more details on launch configurations.

Achieved Occupancy
Est. Speedup: 78.18%

The difference between calculated theoretical (100.0%) and measured achieved occupancy (21.8%) can be the result of warp scheduling overheads or workload imbalances during the kernel execution. Load imbalances can occur between warps within a block as well as across blocks of the same kernel. See the CUDA Best Practices Guide for more details on optimizing occupancy.

Imc Miss Stalls
Est. Speedup: 54.09%

On average, each warp of this workload spends 10.6 cycles being stalled waiting for an immediate constant cache (IMC) miss. A read from constant memory costs one memory read from device memory only on a cache miss; otherwise, it just costs one read from the constant cache. Immediate constants are encoded into the SASS instruction as 'c[bank][offset]'. Accesses to different addresses by threads within a warp are serialized, thus the cost scales linearly with the number of unique addresses read by all threads within a warp. As such, the constant cache is best when threads in the same warp access only a few distinct locations. If all threads of a warp access the same location, then constant memory can be as fast as a register access. This stall type represents about 54.1% of the total average of 19.6 cycles between issuing two instructions.