	Result	Size	Time	Cycles	GPU	SM Frequency	Process	Attributes
Current	586 - thresholding_kernel	(120, 68, 1)x(16, 16, 1)	143.74 us	205,883	0 - NVIDIA GeForce GTX 1660 Ti	1.43 Ghz	[87329] image	

Summary | Details | Source | Context | Comments | Raw | Session

Compare | Tools | View | Export

This table shows all results in the report. Use the column headers to sort the results in this report. Double-click a result to see detailed metrics. Double-click on demangled names to rename it.

ID	Estimated Speedup [%]	Function Name	Demangled Name	Duration [us] (2110.50 us)	Runtime Improvement [us] (1288.39 us)	Compute Throughput [%]	Memory Throughput [%]	# Reg
5	46.51	thresholding_kernel	thresholding_kernel..	143.74	66.85	67.72	67.72	
6	63.67	hough_kernel	hough_kernel..char..	880	560.33	82.54	18.18	

The following performance optimization opportunities were discovered for this result. Follow the rule links to see more context on the Details page.
Note: *Speedup estimates provide upper bounds for the optimization potential of a kernel assuming its overall algorithmic structure is kept unchanged.*

L1TEX Global Store Access Pattern
Est. Speedup: 46.51%
The memory access pattern for global stores to L1TEX might not be optimal. On average, only 15.9 of the 32 bytes transmitted per sector are utilized by each thread. This could possibly be caused by a stride between threads. Check the Source Counters section for uncoalesced global stores.

L1TEX Global Load Access Pattern
Est. Speedup: 36.76%
The memory access pattern for global loads from L1TEX might not be optimal. On average, only 19.3 of the 32 bytes transmitted per sector are utilized by each thread. This could possibly be caused by a stride between threads. Check the Source Counters section for uncoalesced global loads.

Uncoalesced Global Accesses
Est. Speedup: 35.07%
This kernel has uncoalesced global accesses resulting in a total of 386160 excessive sectors (36% of the total 1080000 sectors). Check the L2 Theoretical Sectors Global Excessive table for the primary source locations. The CUDA Programming Guide has additional information on reducing uncoalesced device memory accesses.