Si4032/4432 PA MATCHING

1. Introduction

This application note provides a description of the matching of the Power Amplifier (PA) on the Si4032/4432 RFIC. Specifically, this document does *not* address the matching procedure for the PA on the Si4031/4431 RFIC. Since the output power level on the Si4031/4431 RFIC is considerably lower than the Si4032/4432 RFIC, the matching procedure is somewhat different.

We wish to simultaneously achieve several goals with the matching network:

- Maximize RF output power
- Minimize current consumption (i.e., maximize efficiency)
- Constrain the peak voltage at the drain of the output devices
- Comply with ETSI and FCC specifications for spurious emissions

The matching procedure outlined in this document will allow for achieving the above-listed goals and is applicable for two different types of board configurations: one with separate antennas for the TX and RX paths and the other with a single antenna and an RF switch to select between the TX and RX paths. The differences in matching procedure required for the two board configurations are discussed in detail.

Table 1 and Table 2 are provided for users more interested in quickly obtaining matching component values than in the methodology used to develop the matching network.

1.1. Brief Overview of Matching Procedure

This application note discusses the matching philosophy and procedure for the Si4032/4432 RFIC in great detail. However, some users may be interested in quickly gaining a high-level overview of the procedure before getting into the fine details. For those readers, the main points of the matching procedure are summarized below:

- Choose LCHOKE (pull-up inductor) for high impedance at Fo
- Choose C0 (series capacitor) for low impedance at Fo
- Design a Chebyshev LPF (for attenuation of harmonics)
- Design LHARM-CHARM network (to provide good termination at harmonic frequencies)

1.2. Summary of Matching Network Component Values

Some users are not greatly interested in the theoretical development of the matching network; rather, they are concerned with quickly obtaining a set of component values for a given desired frequency of operation. For those users, the resulting component values for the PA matching network for multiple frequencies across the operating range of the Si4032/4432 RFIC are summarized. Table 1 provides the component values required for the Split TX/RX board configuration of Figure 1, while Table 2 provides the component values required for the Single Antenna with RF Switch board configuration of Figure 2.

Table 1. PA Match Network Component Values vs. Frequency (Split TX/RX Board)

Freq Band	L_{choke}	C0	L_{HARM}	C_{HARM}	R_{HARM}	L0	CM	LM	CM2	LM2
245 MHz	390 nH	220 pF	20 nH	22.0 pF	50 Ω	39 nH	15.0 pF	68 nH	15.0 pF	43 nH
315 MHz	390 nH	150 pF	18 nH	15.0 pF	50 Ω	33 nH	11.0 pF	56 nH	12.0 pF	33 nH
390 MHz	330 nH	120 pF	11 nH	15.0 pF	50 Ω	24 nH	10.0 pF	43 nH	10.0 pF	27 nH
433 MHz	270 nH	120 pF	11 nH	12.0 pF	50 Ω	24 nH	8.2 pF	39 nH	9.1 pF	24 nH
470 MHz	270 nH	100 pF	10 nH	11.0 pF	50 Ω	24 nH	6.8 pF	36 nH	8.2 pF	22 nH
868 MHz	120 nH	33 pF	5.6 nH	6.0 pF	50 Ω	10.0 nH	4.0 pF	18 nH	4.3 pF	12.0 nH
915 MHz	120 nH	33 pF	5.6 nH	5.6 pF	50 Ω	10.0 nH	3.9 pF	18 nH	3.9 pF	12.0 nH
950 MHz	100 nH	27 pF	5.1 nH	5.6 pF	50 Ω	8.2 nH	3.6 pF	15 nH	3.6 pF	11.0 nH

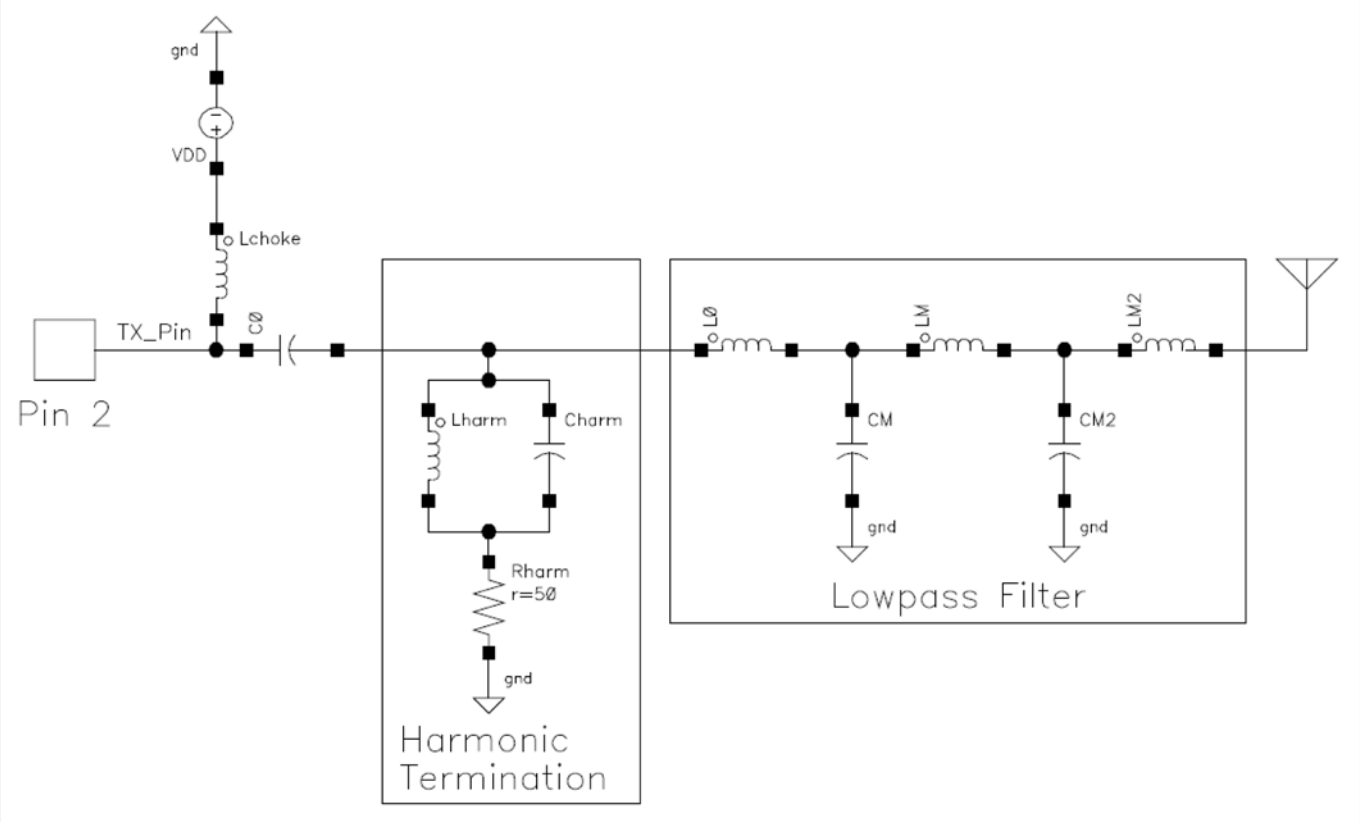

Figure 1. Matching Topology for Split TX/RX Board Configuration

Table 2. PA Match Network Component Values vs. Frequency (RF Switch Board)

Freq Band	L_{choke}	C0	L_{HARM}	C_{HARM}	R_{HARM}	L0	CM	LM	CM2	LM2	CM3
245 MHz	390 nH	220 pF	20 nH	22.0 pF	50 Ω	47 nH	12.0 pF	47 nH	18.0 pF	30 nH	18.0 pF
315 MHz	390 nH	150 pF	18 nH	15.0 pF	50 Ω	33 nH	10.0 pF	33 nH	15.0 pF	24 nH	15.0 pF
390 MHz	330 nH	120 pF	11 nH	15.0 pF	50 Ω	27 nH	8.2 pF	27 nH	9.1 pF	20 nH	9.1 pF
433 MHz	270 nH	120 pF	11 nH	12.0 pF	50 Ω	24 nH	6.8 pF	24 nH	8.2 pF	18 nH	8.2 pF
470 MHz	270 nH	100 pF	10 nH	11.0 pF	50 Ω	22 nH	5.6 pF	22 nH	9.1 pF	15 nH	9.1 pF
868 MHz	120 nH	33 pF	5.6 nH	6.0 pF	50 Ω	15.0 nH	3.3 pF	15 nH	4.7 pF	9.1 nH	4.7 pF
915 MHz	120 nH	33 pF	5.6 nH	5.6 pF	50 Ω	12.0 nH	3.0 pF	12 nH	4.3 pF	8.2 nH	4.3 pF
950 MHz	100 nH	27 pF	5.1 nH	5.6 pF	50 Ω	11.0 nH	3.0 pF	11 nH	4.0 pF	8.2 nH	4.0 pF

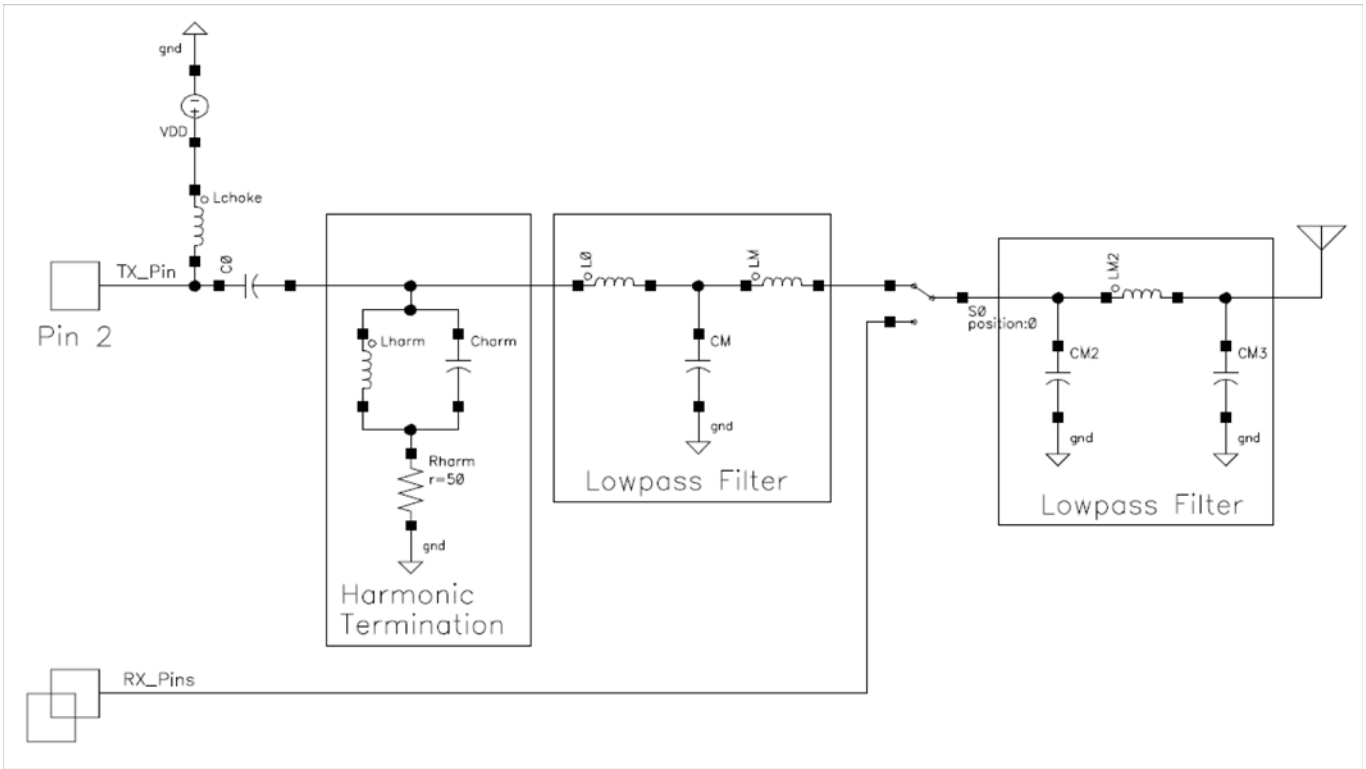

Figure 2. Matching Topology for Single Antenna with RF Switch Board Configuration

We recognize the fact that surface-mount 0603-size or 0402-size components themselves contain parasitic elements that modify their effective values at the frequency of interest. Furthermore, it is convenient to use the nearest-available 5% or 10% component values rather than the exact component values predicted by Filter Design CAD software or filter prototype tables. Additionally, any printed circuit board layout has parasitics, such as trace inductance, component pad capacitance, etc.

This means that it will almost certainly be necessary to "tweak" the final matching values for the reader's specific application and board layout. The above component values should be used as starting points and the values modified slightly to zero-in on the best filter response and impedance match to 50 Ω.

2. Power Amplifier Circuit Description

RF design engineers are familiar with matching conventional (Class A/B/C) power amplifiers. In such cases, the matching procedure is relatively simple: provide a load impedance that is the complex conjugate of the output impedance of the PA. The reader may also employ Load Pull techniques in which a match is found that optimizes the output power but differs from the complex conjugate of the PA output impedance. In these conventional classes of power amplifiers, the output waveform ranges from a full 360 degree copy or reproduction of the driving waveform (e.g., Class A) to a partial (less than 360 degrees) reproduction of the driving waveform (e.g., Class B or Class C).

However, the PA circuitry in the Si4032/4432 RFIC differs considerably from such a conventional power amplifier. Specifically, the PA circuitry in the Si4032/4432 is of a type known as a "switching power amplifier" or "switching power converter". The matching procedure for such a class of PA is entirely different and may not be immediately intuitive.

2.1. Basic Switching PA Circuit Topology

At the very heart of a switching PA is just that – a switch. In the Si4032/4432, the switch is provided by an NMOS transistor in an open-drain configuration, sized to handle the current required for the specified output power.

Figure 3 shows the typical matching circuit necessary to extract RF power from a switching amplifier. In very general terms, the value of the pull-up inductor “LCHOKE” is chosen to be a very large impedance at the frequency of operation (and its nearest harmonics), while the series-resonant output tank (L0-C0) is chosen to resonate at the frequency of operation. The shunt capacitance “CSHUNT” is required to store energy during the switching cycle. This shunt capacitance, along with the extra series inductance “LX”, also works to tailor the time-domain shape of the output waveform. It is important to understand that in order to optimize the efficiency of a switching-type amplifier, it is necessary to control the time-domain shape of the output waveform.

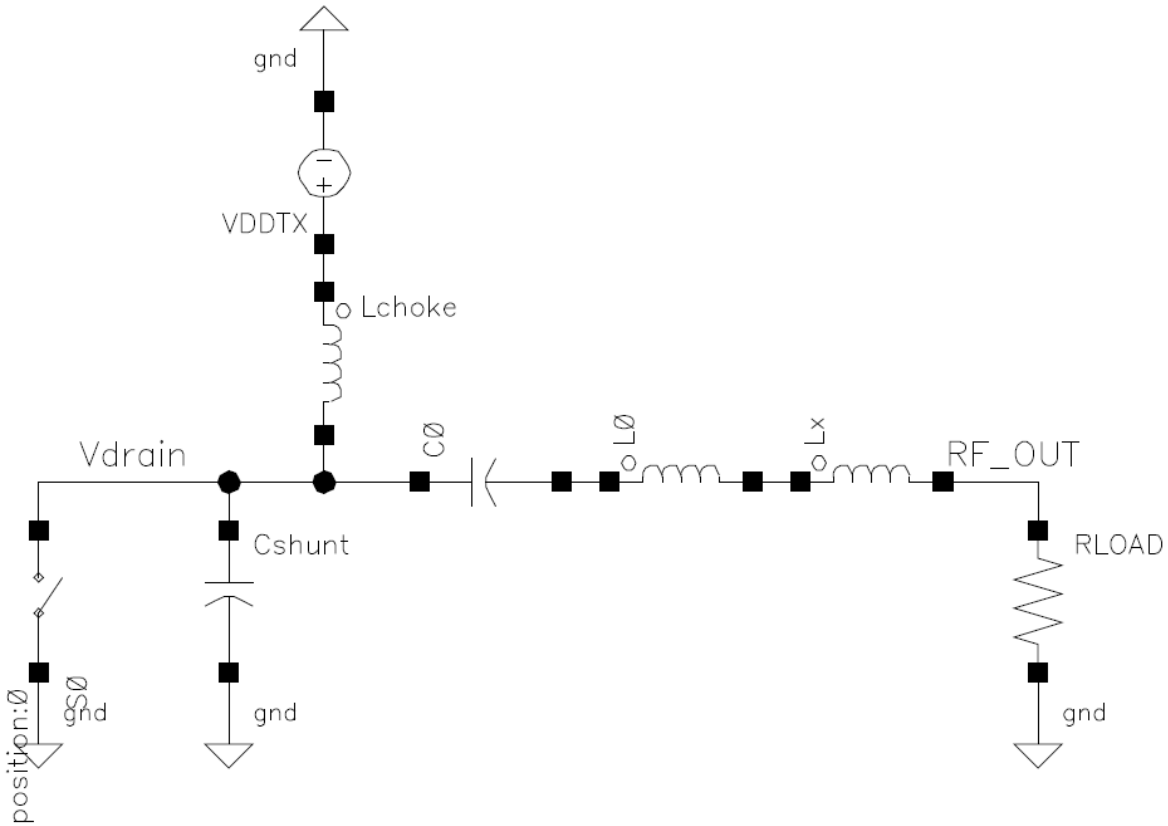

Figure 3. Basic Switching PA Circuit Topology

2.2. Theory of Operation of an Ideal Switching PA

So, exactly how does a switch "amplify" an RF signal?" The simple answer is that it does not. After all, as long as the input control signal to the switch is sufficient to toggle the switch between its ON and OFF states, the output waveform will remain the same. Thus, the amount of output power delivered to the load resistance is independent of the amplitude of the input control signal (i.e., amplitude of the RF signal at the gate of the output MOS device). In such a case, defining the "gain" or amplification factor of the PA no longer has much meaning. Technically speaking, it is more correct to refer to this circuit as a "power converter" rather than a "power amplifier".

So, if the circuit doesn't amplify the internal RF input signal, then what determines the level of the output power?

In an ideal switching PA, the level of output power is dependent primarily upon two parameters: 1) the dc supply voltage and 2) the load resistance. This statement is actually quite interesting because, theoretically, there is no limit to the amount of power we can extract from a switching PA. Higher levels of output power can be obtained by either increasing the supply voltage or by decreasing the load impedance presented to the switching output device.

Furthermore, in an ideal switching PA, it is theoretically possible to achieve 100% efficiency. This is a significant difference from conventional PAs. It is easily shown that the theoretical maximum efficiency of a Class-A PA is 50%; 78.5% for Class-B, and so on. However, in a switching PA, it is possible to tailor the output waveform such that the voltage across the switch is always zero during any period of time that the switch is conducting current, and the current conducted by the switch is always zero during any period of time that the voltage across the switch is non-zero. Thus, the power dissipated by the switching device itself is zero, and, in the absence of any other losses in the circuit, the efficiency approaches 100%.

For those readers that may have an interest in learning more about the theoretical operation of switching amplifiers (especially Class-E amplifiers), the following papers are recommended:

- *Class E - A New Class of High-Efficiency Tuned Single-Ended Switching Power Amplifiers*, N. Sokal and A. Sokal, IEEE Journal of Solid State Circuits, Vol. SC-10, No. 3, June 1975.
- *Idealized Operation of the Class-E Tuned Power Amplifier*, F. Raab, IEEE Transactions on Circuits and Systems, Vol. CAS-24, No. 12, December 1977.

2.3. Limitations of a Practical MOS Switching PA

In practice, of course, we must live with several factors that prevent us from ever achieving "ideal" operation of the switching PA. These factors include the maximum operating voltage of the switch (i.e., MOS output device), the maximum current (limited by the size of the MOS output device), ON and OFF state resistances of the MOS output device, non-zero switching times of the MOS output device, and losses in the output matching components due to finite Qs. All of these factors combine to limit the achievable output power and efficiency.

The limitation on the maximum drain voltage of the MOS output device turns out to be a considerable constraint. RF design engineers may be quite familiar with the waveforms obtained with inductively-loaded conventional PAs where the peak output voltage reaches a value equal to twice the dc supply voltage. However, the peak of the output voltage waveform in a switching PA may far exceed this "$2xV_{DD}$" rule-of-thumb. As is shown in the papers listed above, the peak drain voltage for a Class-E switching amplifier can reach 3.56 x V_{DD}.

The operational range of supply voltage for the Si4032/4432 RFIC is specified as V_{DD} = 1.8 to 3.6 V. It is apparent that if the switching PA circuit was matched for Class-E operation at V_{DD} = 3.6 V, the resulting peak drain voltage would reach 12.8 V peak. This exceeds the maximum voltage at which the MOS device can operate without damage. As a result, Class-E matching and operation is not recommended for the Si4032/4432 RFIC, except in those applications where the supply voltage is limited to the lower end of the specified range. The matching procedure discussed in this application note is thus primarily concerned with constraining the peak drain voltage to a specified maximum value.

The size of the MOS output device has the effect of limiting the amount of output power that can be extracted from a practical switching PA. In an ideal switching PA, we can increase the output power by either increasing the supply voltage or by decreasing the load resistance presented to the PA. We have just mentioned that the supply voltage cannot be increased indefinitely because the peak drain voltage may exceed the maximum voltage rating of the semiconductor process. Therefore, the only remaining option to increase output power is to decrease the load resistance.

This has the effect of requiring greater current handling capability in the switching device. While an ideal switch may carry an infinite amount of current, a practical MOS switch cannot. The size of the MOS output device in the Si4032/4432 is carefully designed to carry sufficient current to achieve its maximum specified output power; however, this level of current-handling capability is only available when the RFIC is commanded to its maximum TX output power mode (by the txpow[2:0] field in SPI Register 6Dh). The Si4032/4432 RFIC achieves a reduction in output power by reducing the number of active fingers (i.e., size) of the MOS output device; this effectively limits the current-handling ability of the output device to less than that desired by the combination of supply voltage and load impedance. That is to say, at the maximum setting(s) of the txpow[2:0] field, the PA output devices behave much like a switch, but at the lower settings of the txpow[2:0] field, the output devices behave more like a switch in series with a non-negligible resistance.

3. Matching Procedure for the Si4032/4432

As discussed above, published matching procedures for well-defined classes of operation of switching amplifiers (such as Class-D or Class-E) may lead to operating conditions that exceed the maximum ratings (voltage or current) for the semiconductor process. As a result, we turn to a "customized" matching methodology that satisfies our desire for output power and efficiency while maintaining operation below the maximum voltage and current ratings for the RFIC. Note that this matching methodology may not correspond to any predefined "classes" of amplifier operation.

3.1. Goals for the Matching Procedure

The matching methodology for the Si4032/4432 RFIC is aimed at achieving the following simultaneous goals:

- Obtain a minimum of +20 dBm of conducted RF output power
- Constrain the peak drain voltage to not exceed +6.5 V
- Achieve better than 40% efficiency on the PA output stage
- Comply with ETSI and FCC specifications for spurious emissions

These goals will be met under the following conditions:

- Operation at any frequency in the 240–960 MHz range
- Antenna load impedance = 50 Ω
- The chip is commanded to maximum output power mode (txpow[2:0] field)
- Output power is measured at the TX output pin of the chip, prior to any low-pass filter
- Limitation on peak drain voltage is met for any V_{DD} = 1.8 to 3.6 V
- Minimum of +20 dBm output power is met for V_{DD} = 3.3 V (minimum)

3.1.1. Comments on Peak Drain Voltage Limit

It should be noted that the +6.5 V peak drain voltage limit referred to above is not the same as the absolute maximum voltage rating at which the device may experience permanent damage. This absolute maximum voltage rating is shown in the Si4032/4432 Datasheet as +8.0 V on the TX output pin.

Instead, this peak drain voltage limit of +6.5 V has been calculated as a limit, which, if not exceeded for continuous periods of time, should allow for multiple years of operation without noticeable degradation in output power. That is to say, if the peak drain voltage were to momentarily slightly exceed +6.5 V, the device would likely not be instantaneously damaged but might suffer a small decrease in long-term reliability.

It should also be noted that the Si4032/4432 RFIC contains internal diode voltage clamps on the drain node of the MOS output device. The purpose of these diode clamps is to limit brief excursions of the peak drain voltage that may occur in excess of +6.5 V. Such variations in peak drain voltage may occur if the antenna load impedance varies considerably from 50 Ω (e.g., turning on the TX output without an antenna connected, etc.).

In all cases, the voltage limit specified by the absolute maximum voltage rating should not intentionally be exceeded (however briefly) because instantaneous damage may occur.

3.1.2. Comments on Achieving +20 dBm Output Power

This application note is largely targeted at applications that require +20 dBm output power. While this level of output power is certainly achievable, meeting the other design constraints requires careful attention to matching component selection and good board layout techniques. That is to say, it is possible to fail through poor design and board layout practices.

Conversely, it is a relatively simple matter to achieve slightly reduced levels of output power, such as +17 to +18 dBm. For example, the constraint on peak drain voltage becomes much easier to meet as the supply voltage is reduced; however, there will, naturally, be some corresponding reduction in output power as the V_{DD} supply voltage is lowered.

In short, obtaining +20 dBm output power is not difficult in itself, and constraining the peak drain voltage to less than +6.5 V is also not difficult; it is the *simultaneous* achievement of both these design goals that is challenging.

3.2. Overview of the Matching Procedure

3.2.1. Split TX/RX Board Configuration

The following steps provide a broad overview of the matching methodology for the Split TX/RX board configuration. Further details of each step will be provided later.

1. First, design a simple two-element LC matching network at the TX output pin to provide the desired output power into a purely resistive broadband load.
   a. The value of load resistance is chosen to obtain the desired output power, given the specified value of supply voltage (V_{DD} = 3.6 V in this scenario).
   b. The LC element values are chosen to provide as close to a (nearly) perfect square wave at the TX output pin as possible.
2. Next, design a low-pass filter to provide sufficient harmonic attenuation.
   a. The unfiltered square waveform at the TX output pin will naturally contain high levels of harmonics.
   b. Depending upon the output power level and desired level of harmonic attenuation, a 5th order low-pass filter will likely be required.
3. Finally, design an additional "harmonic termination" circuit to be connected in parallel with the input to the low-pass filter.
   a. The purpose of the additional circuit is to provide a good termination at the harmonic frequencies above the passband of the low-pass filter.
   b. This is necessary to maintain the square waveform at the TX pin.

3.2.2. Single Antenna with RF Switch Board Configuration

The following steps provide a broad overview of the matching methodology for the Single Antenna with RF Switch board configuration. Further details of each step will be provided later.

1. First, design a simple two-element LC matching network at the TX output pin in the same fashion as for the Split TX/RX board configuration.
2. Next, design two low-order low-pass filter sections to provide sufficient harmonic attenuation.
   a. The RF switch will itself generate some harmonic energy as the desired signal frequency passes through it. It is recommended to place some of the low-pass filter circuitry after the RF switch to attenuate these additional harmonic components.
   b. Thus the matching topology for the Single Antenna with RF Switch board configuration is comprised of two small low-pass filter sections with the RF switch embedded between them.
3. Finally, design the harmonic termination circuit in the same fashion as for the Split TX/RX board configuration.

3.3. Detailed Matching Procedure

In this section, we provide further details about each step of the matching procedures outlined above. We assume a supply voltage of V_{DD} = 3.6 V. While the Si4032/4432 RFIC is specified to deliver +20 dBm for V_{DD} = 3.3 V, we deliberately set the supply voltage to its maximum value (3.6 V) in order to design for the worst-case peak drain voltage. We expect to obtain slightly greater than +20 dBm for this maximum value of supply voltage.

3.3.1. Step #1: Design an L-C Match into Broadband Resistive Load

In Step #1, we first design a simple two-element L-C match network into a broadband resistive load.

3.3.1.1. TX Output Power and Efficiency

The value of load resistance presented to the PA output is chosen to obtain the desired output power, given the specified value of supply voltage (V_{DD} = 3.6 V in this scenario). The required value of load resistance may be determined by simulation or from the design equations for switching-type power amplifiers (given in the papers referenced previously). As it turns out, the optimum load impedance for a +20 dBm switching amplifier operating at V_{DD} = 3.6 V is reasonably close to 50 Ω. This is convenient, as it simplifies the later construction of the low-pass filter and matching network. However, it should be understood that this is merely a fortunate coincidence; if a lower

output level (e.g., +17 dBm) had been targeted, the required value of load resistance would have been higher than 50 Ω.

It should be clearly understood that the optimal value of load resistance (RLOAD) discussed above and the antenna impedance (RANT) are not the same parameter, nor do they necessarily have the same ohmic value. Given the arbitrary impedance of the antenna, it will later be our task to construct a matching network that transforms RANT into RLOAD, as seen at the TX output pin of the RFIC. If both impedances are the same value (e.g,. 50 Ω), the task of constructing the low-pass filter and matching network is greatly simplified, but it is not impossible to work with other values of RANT or RLOAD.

In this step of the design process, however, we ignore the actual antenna impedance and concentrate on matching to the desired load resistance (RLOAD = 50 Ω). We use the simplified matching architecture of Figure 4 and choose the L-C element value to provide as perfect a square wave at the TX output pin as is possible.

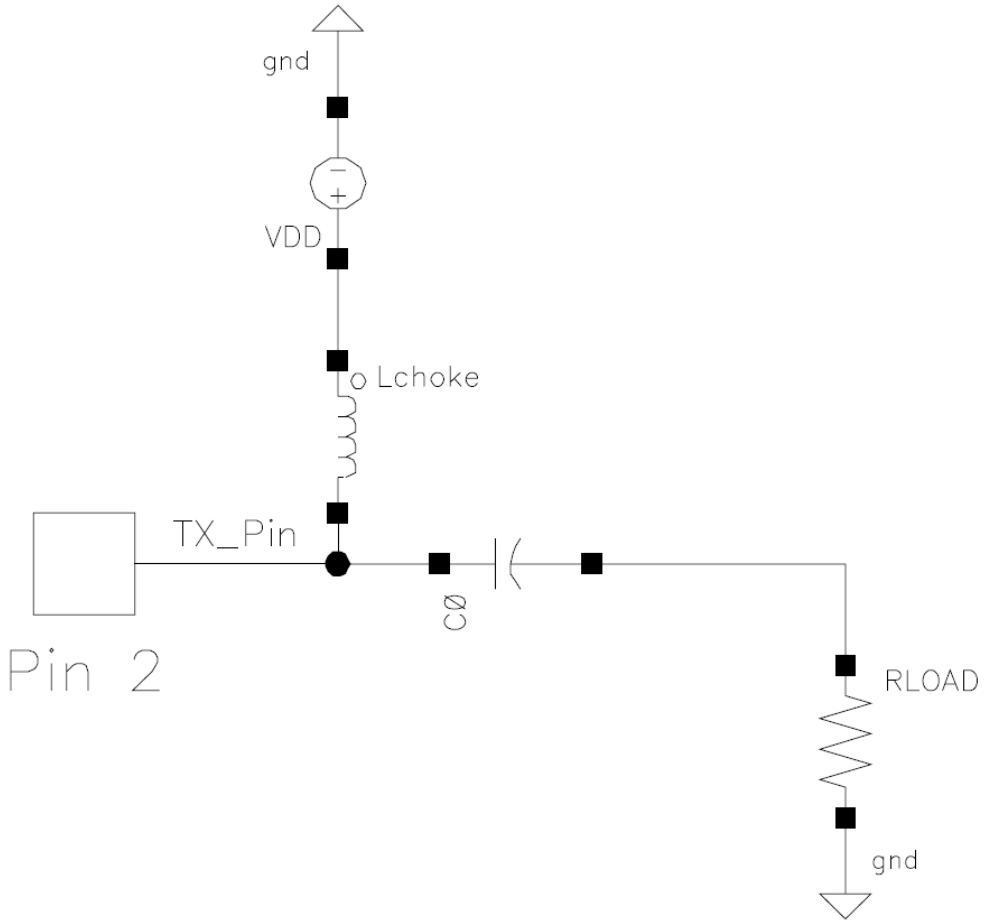

Figure 4. Simplified L-C Match into Broadband Load

A square waveform at the TX output pin is desirable for the following reasons:

- We wish to constrain the peak drain voltage so that it does not exceed +6.5 V.
- A square waveform provides maximum output power while satisfying the peak drain voltage requirement.

Clearly, some amount of current efficiency must be sacrificed in order to meet these two goals. That is to say, it is theoretically possible to obtain the desired output power level (+20 dBm) with lower current consumption (i.e., better efficiency) by operation in a traditional switching amplifier class (e.g., Class-E). However, the resulting peak drain voltage for such a matching network will be much higher and may approach voltage levels potentially

damaging to the RFIC. The loss in amplifier efficiency that results from constraining the drain voltage to lower peak values is not great and is an acceptable trade-off.

It can be shown in simulation that the L-C values that result in a good square wave at the TX output pin are a large value of inductance for the pull-up inductor, LCHOKE, and a large value of capacitance for the series capacitor, C0. The value of LCHOKE should be chosen such that it provides a high impedance at not only the fundamental operating frequency but also at the first few harmonic frequencies as well. Thus, a high-inductance value should be chosen, but not one so large as to already be at (or past) parallel self-resonance at the desired operating frequency. The exact inductance value is not critical; however, Silicon Labs recommends the following range of inductance values (assuming 0402-size or 0603-size inductors) as a function of the desired operating frequency:

- 315 MHz: approximately 390 nH
- 470 MHz: approximately 270 nH
- 915 MHz: approximately 120 nH

The value of series capacitor C0 should be chosen to provide a very low impedance at the desired operating frequency. This capacitor may be chosen to be approximately at series self-resonance. Silicon Labs recommends the following range of capacitance values (assuming 0402-size or 0603-size capacitors) as a function of the desired operating frequency:

- 315 MHz: approximately 150 pF
- 470 MHz: approximately 100 pF
- 915 MHz: approximately 33 pF

Since the load resistance, RLOAD, that we desire to present to the PA is equal to 50 Ω, it is quite simple to provide this load impedance with standard lab test equipment, such as a power meter or spectrum analyzer. (If our desired value for RLOAD had not been equal to 50 Ω, it would have been necessary to add a resistor either in series or shunt with our test equipment and to calculate an appropriate power correction factor.)

In Table 3, we show the typical output power and current consumption as a function of frequency for this simple L-C match. These typical results were obtained at V_{DD} = 3.3 V in maximum output power mode.

Table 3. Output Power vs. Frequency (Simple L-C Match)

Freq	L_{CHOKE}	C_0	V_{DD}	P_{OUT}	$I_{DD-TOTAL}$	$I_{DD-PAOUT}$	Efficiency
240 MHz	390 nH	150 pF	3.30 VDC	21.45 dBm	80.15 mA	58.65 mA	72.1%
315 MHz	390 nH	150 pF	3.30 VDC	20.88 dBm	79.34 mA	57.84 mA	64.2%
433 MHz	270 nH	100 pF	3.30 VDC	20.41 dBm	73.02 mA	51.52 mA	64.6%
470 MHz	220 nH	82 pF	3.30 VDC	20.74 dBm	77.10 mA	55.60 mA	64.6%
650 MHz	200 nH	68 pF	3.30 VDC	20.31 dBm	92.85 mA	71.35 mA	45.6%
868 MHz	120 nH	33 pF	3.30 VDC	20.20 dBm	94.91 mA	73.41 mA	43.2%
915 MHz	120 nH	33 pF	3.30 VDC	20.20 dBm	97.34 mA	75.84 mA	41.8%

3.3.1.2. Voltage Waveforms at TX Output Pin

It is not difficult to verify the resulting voltage waveform at the TX output pin (at least for the lower frequency bands of operation). A high-speed oscilloscope with an input bandwidth of at least 4 GHz (preferably higher) is required. A low-capacitance, high-bandwidth scope probe is also required, or, alternatively, the "resistive-sniffing" network of Figure 5 may be used.

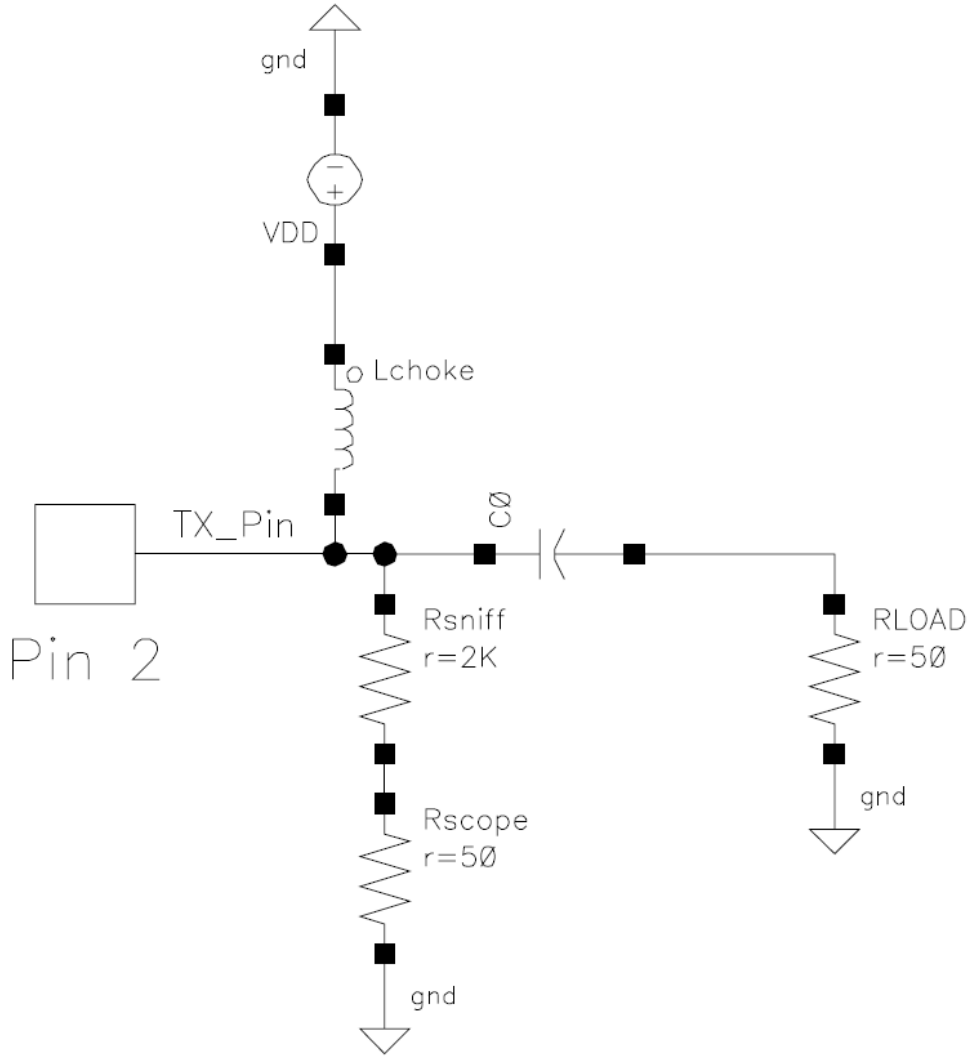

Figure 5. Resistive Sniffing Network

Using the "resistor sniffing" technique of Figure 5, the drain voltage waveforms of Figure 6 were observed for an operating frequency of 315 MHz. In the example shown here, component values of LCHOKE = 390 nH and C0 = 150 pF were used. A very nice square waveform was obtained, with a maximum drain voltage of 6.27 V (i.e. less than 6.5 V).

It should be noted that, as the operating frequency increases, it becomes more difficult not only to maintain a square waveform at the output but also to observe the square waveform. The input bandwidth of the oscilloscope used to display the waveform must increase in accordance with the operating frequency. Additionally, parasitic capacitances in the PCB layout, as well as in the output device(s) of the RFIC, tend to limit the high-frequency response of the amplifier.

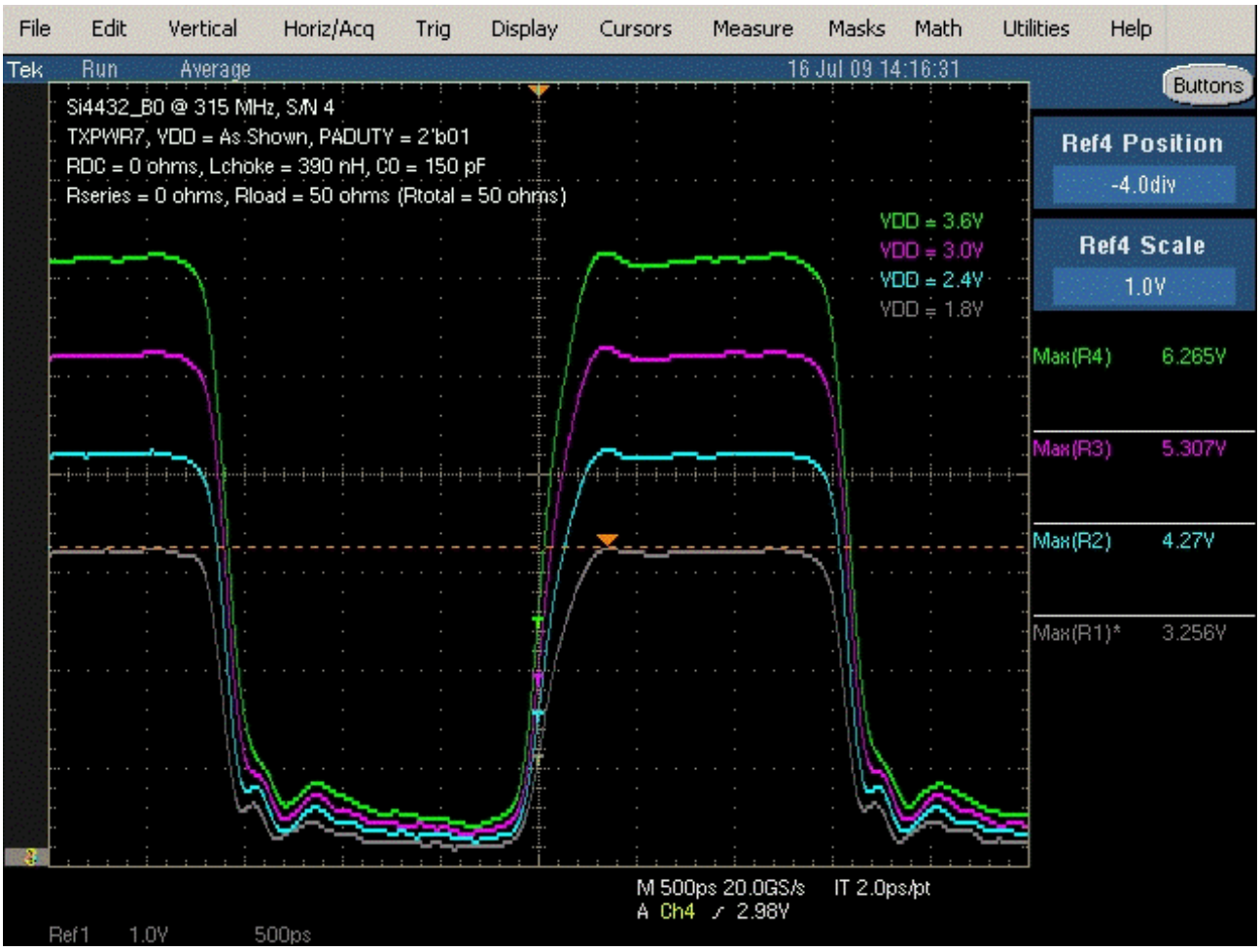

Figure 6. Drain Voltage Waveforms vs. V_{DD} (315 MHz)

3.3.2. Step #2: Design a Low-Pass Filter (for Split TX/RX Board Configuration)

In this step, we will design a low-pass filter network to attenuate the harmonics below the level required to meet applicable regulatory specs (e.g., FCC or ETSI). A Split TX/RX board configuration (i.e., a board configuration that does not contain an RF switch) is assumed in this example; the low-pass filter design process for a circuit with an RF switch will be discussed later.

3.3.2.1. Unfiltered Harmonic Spectrum

It should be understood that the square waveform at the TX output pin will naturally contain relatively high levels of harmonics. This is normal for such a switching-amplifier and matching topology. By way of example, the harmonic spectrum at the TX output pin for a simple L-C match at 315 MHz (LCHOKE = 390 nH, C0 = 150 pF, RLOAD = 50 Ω) is shown in Figure 7.

It is evident that, due to the approximate square waveform at the TX output pin, the odd-order harmonics are somewhat stronger than the even-order harmonics. As a result, the most problematic harmonic to attenuate may actually be the third harmonic rather than the second harmonic, which is closer in frequency.

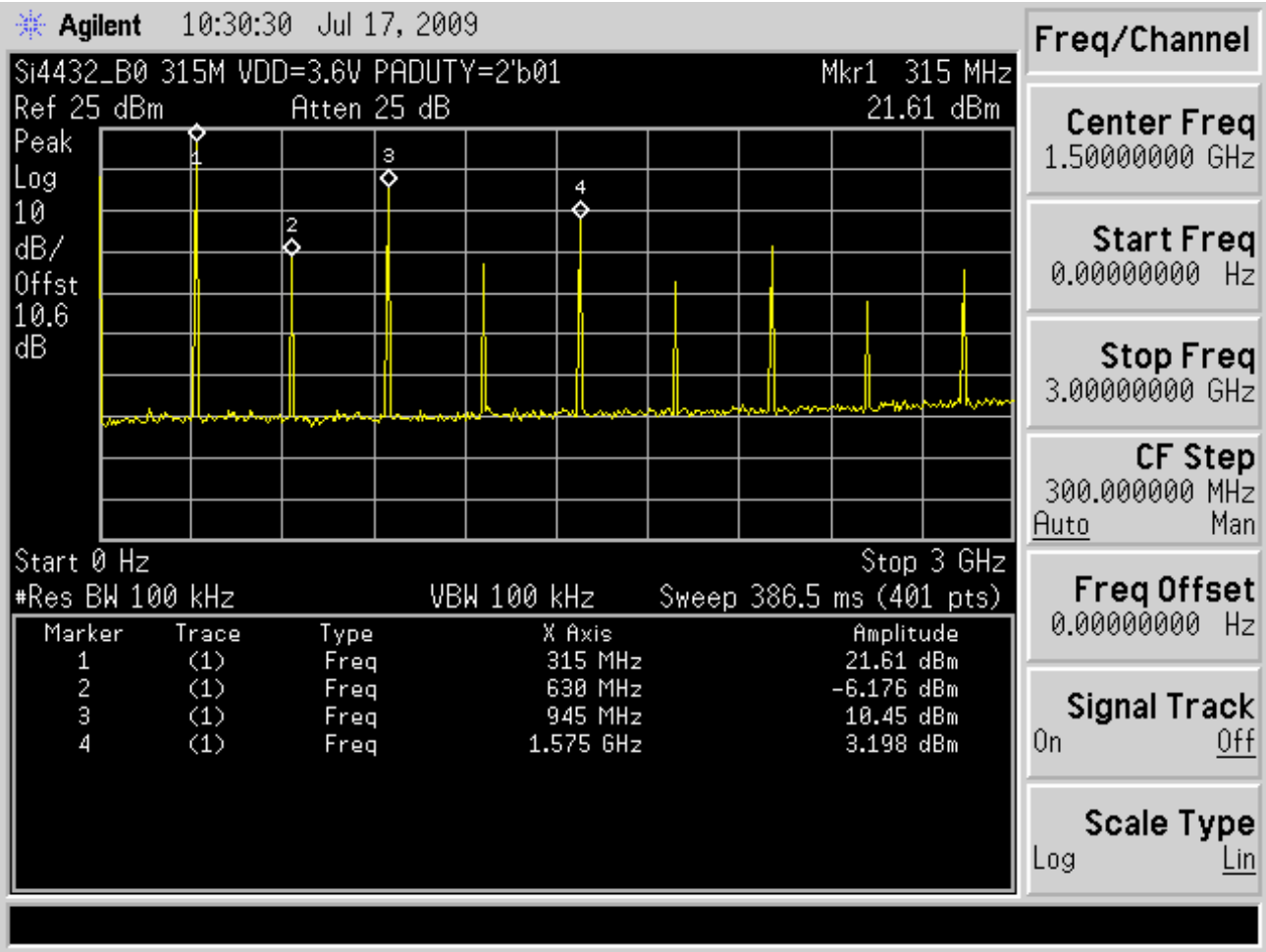

Figure 7. Unfiltered Harmonic Spectrum at TX Pin (at 315 MHz)

Note that the third harmonic is only about –11 dBc at an absolute level of approximately +10 dBm. In the event that the third harmonic falls in a "restricted band" as defined in FCC Part 15.205 and Part 15.209, this unwanted signal must be attenuated to less than –41 dBm (500 µV/meter at a distance of 3 meters). Accordingly, our LPF network must provide a minimum of 51 dB attenuation at the third harmonic frequency. It is likely that a fifth order (or higher) LPF network will be required to obtain this level of attenuation. Additionally, the user must pay careful attention to the layout of the printed circuit board. Unfortunately, it is relatively common to observe less-than-expected attenuation performance from a filter network due to poor PCB layout techniques.

3.3.2.2. Selecting a LPF Type

Our initial design goals for the low-pass filter are as follows:

- Minimal insertion loss at the desired operating frequency
- Minimum of 51 dB attenuation at the third harmonic
- Lowest filter order possible to still achieve this required harmonic attenuation
- 1:1 impedance transformation (i.e., 50 Ω input and 50 Ω output impedance)

Note that the amplitude characteristics in the lower portion of the passband of the LPF are relatively unimportant. Because the output signal contains no frequency components below the fundamental frequency, the frequency response of the filter below the desired operating frequency is also of little consequence. We are free to choose the filter type (e.g., Butterworth, Chebyshev, Elliptic) based primarily upon the filter's attenuation characteristics rather than its passband response.

A Butterworth filter design is unsuitable because it provides relatively poor high-frequency attenuation characteristics; there is no need to sacrifice high-frequency attenuation in order to obtain a maximally-flat in-band frequency response.

Similarly, an Elliptic filter design (Cauer-Chebyshev) provides insufficient attenuation at higher-order harmonic frequencies. While it may be possible (and advantageous) to tune a transmission zero in the stopband to the frequency of a problematic harmonic (e.g., N = 3), we pay for it with a decrease in attenuation at higher harmonic frequencies. As the unfiltered harmonic spectrum of Figure 7 clearly shows, there remain several higher-order harmonics with significant energy that cannot be ignored and must be attenuated.

As a result, we settle on a Chebyshev low-pass filter design as an acceptable filter response.

With a Chebyshev filter, it is possible to obtain a greater rate of attenuation roll-off in the stopband by accepting a larger amount of amplitude ripple in the passband. The next issue to be addressed is the amount of passband ripple to be targeted in the filter design.

Greater attenuation at high frequencies can be obtained by employing a filter designed for a relatively large amount of passband ripple, but this trade-off should not be pushed too far. While a reasonable amount of passband ripple is perfectly acceptable, there is a limit to what can be considered reasonable.

Figure 8 shows the passband frequency response of an ideal (lossless) Chebyshev filter with 0.25 dB of amplitude ripple in the passband. It is quickly apparent that in order to minimize the insertion loss of the filter at the desired operating frequency, it is necessary to design the cutoff frequency of the filter such that the desired operating frequency falls at one of the passband amplitude ripple peaks (Cursor “A” in the plot). If the filter cutoff frequency varies due to component tolerances, the filter response may vary such that the desired operating frequency falls on a minimum of the amplitude ripple response rather than on a maximum. In such a scenario, the filter insertion loss will increase, and the TX output power will decrease.

By designing for a limited amount of passband amplitude ripple, an upper limit is placed on the filter insertion loss due to mistuning of the component values. It is the opinion of Silicon Labs that a Chebyshev passband amplitude ripple of 0.25 to 0.5 dB represents a reasonable design tradeoff between high-frequency stopband attenuation and potential passband filter insertion loss due to component tolerance.

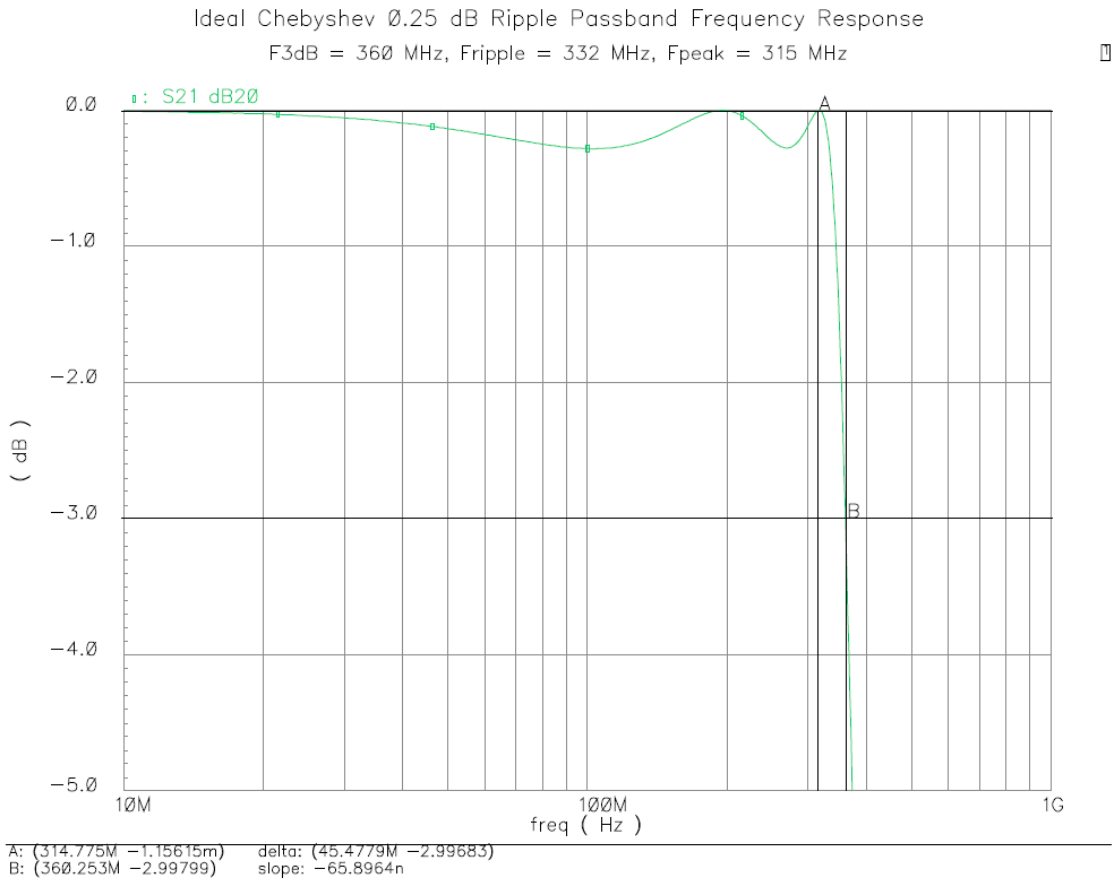

Figure 8. Ideal 0.25 dB Chebyshev Filter Response at 315 MHz

3.3.2.3. Calculation/Design of Component Values

Actual filter component values may be obtained by the usual design methods, such as Filter Design CAD software or tables of normalized filter values scaled to the desired frequency of operation. Note that Silicon Labs recommends designing the filter such that the desired operating frequency falls at a peak of the amplitude ripple response rather than at the 3 dB cutoff frequency or the equal amplitude ripple cutoff frequency. In this manner, the insertion loss of the filter will be minimized, and the TX output power will be maximized. For a fifth-order 0.25 dB Chebyshev filter, the ratio of F3dB:FPEAK is approximately 1.143:1. That is, if the desired operating frequency is 315 MHz, the filter must be designed for a 3 dB cutoff frequency of 315 x 1.143 = 360 MHz. For a fifth-order 0.5 dB Chebyshev filter, the ratio of F3dB:FPEAK is approximately 1.111:1.

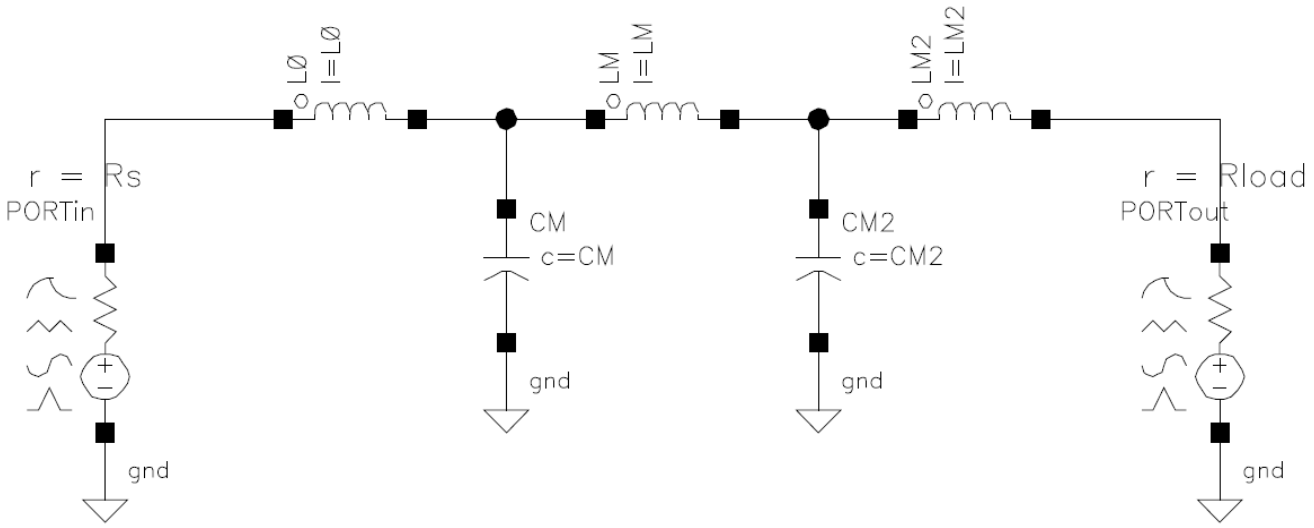

Figure 9. Low-Pass Filter Architecture

Figure 9 shows the general architecture of a fifth-order low-pass filter using the TEE-topology. After design of a 0.25 dB ripple Chebyshev filter with a peak frequency of 315 MHz (F3dB = 360 MHz), the following component values are obtained:

- L0 = 34.9 nH
- CM = 12.5 pF
- LM = 54.7 nH
- CM2 = 12.5 pF
- LM2 = 34.9 nH

It is generally sufficient to use the nearest available standard 5% component tolerance values. Making these substitutions results in the following set of component values:

- L0 = 33 nH
- CM = 12 pF
- LM = 56 nH
- CM2 = 12 pF
- LM2 = 33 nH

3.3.2.4. Simulation of Filter Frequency Response

Figure 10 shows the simulated frequency response of this ideal (lossless) filter network. Note that the filter attenuation at the third harmonic frequency (945 MHz) is 54 dB, validating the choice of filter type, order, and passband amplitude ripple.

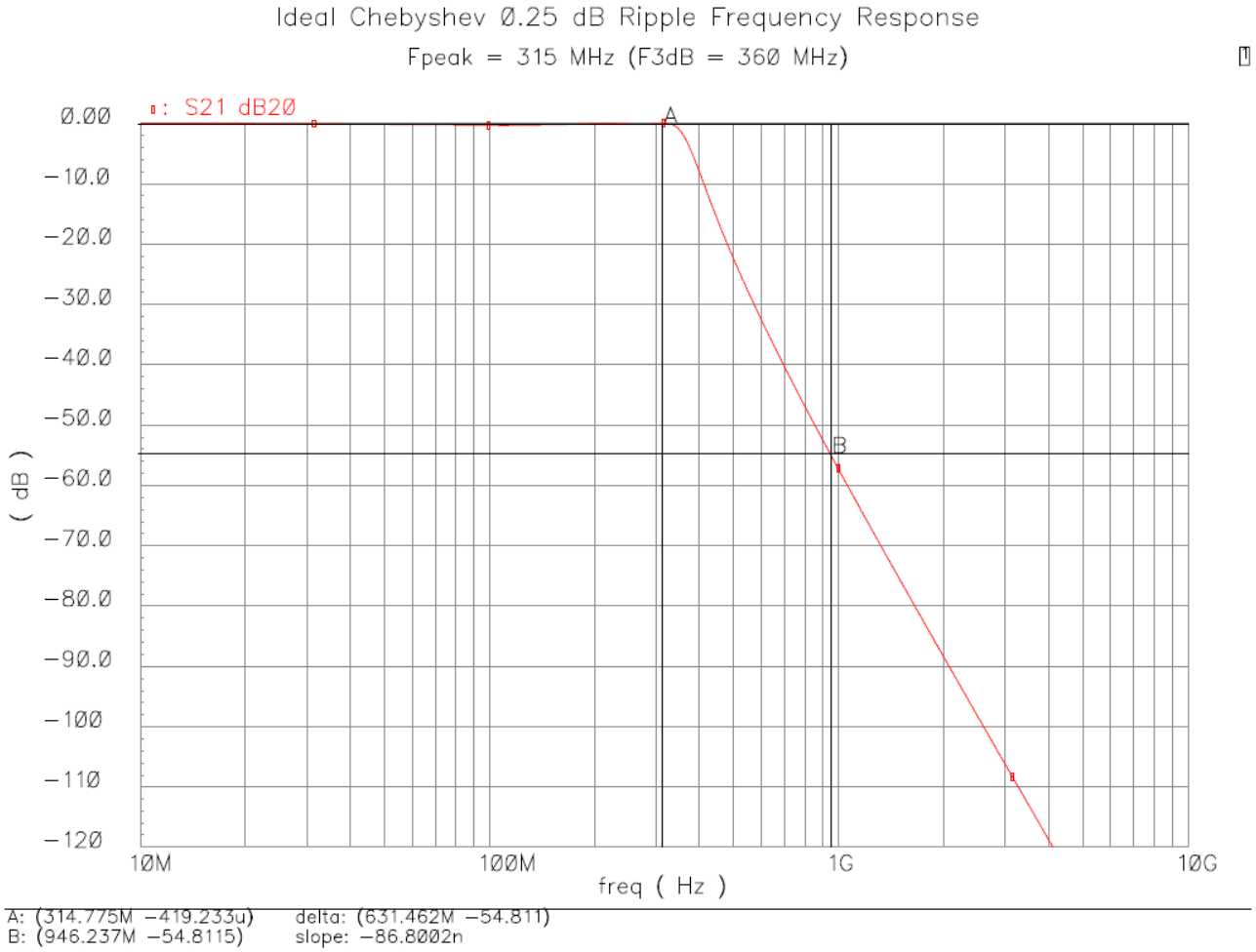

Figure 10. Ideal Simulated Freq Response of 0.25 dB Chebyshev Filter (315 MHz)

Such an ideal frequency response is not possible in practice because it is necessary to use inductors and capacitors with not only finite Qs, but also with internal self-resonances due to parasitic elements. These factors, as well as parasitic effects due to board layout, may cause the actual frequency response to be degraded relative to the ideal response shown in Figure 10.

The effects of using non-ideal components can be predicted by simulation with SPICE models obtained from the manufacturers of discrete components (e.g., Murata, CoilCraft, etc.) These simulation results are shown in Figure 11.

SPICE model simulations of non-ideal discrete components predict an in-band insertion loss of approximately 1.2 dB at the desired operating frequency (315 MHz, in this example). While not desirable, this value of filter insertion loss is fairly realistic, given the typical Qs of discrete components in 0402-size or 0603-size surface-mount packages. Discrete components of higher quality (e.g., wire-wound inductors) may be chosen in an effort to reduce insertion loss, but such parts are admittedly more expensive. It should be noted that the data sheet for the Si4032/4432 RFIC specifies the output power as measured at the TX output pin (i.e. measured in a test configuration similar to Figure 4 on page 9) prior to the insertion loss of any low-pass filter.

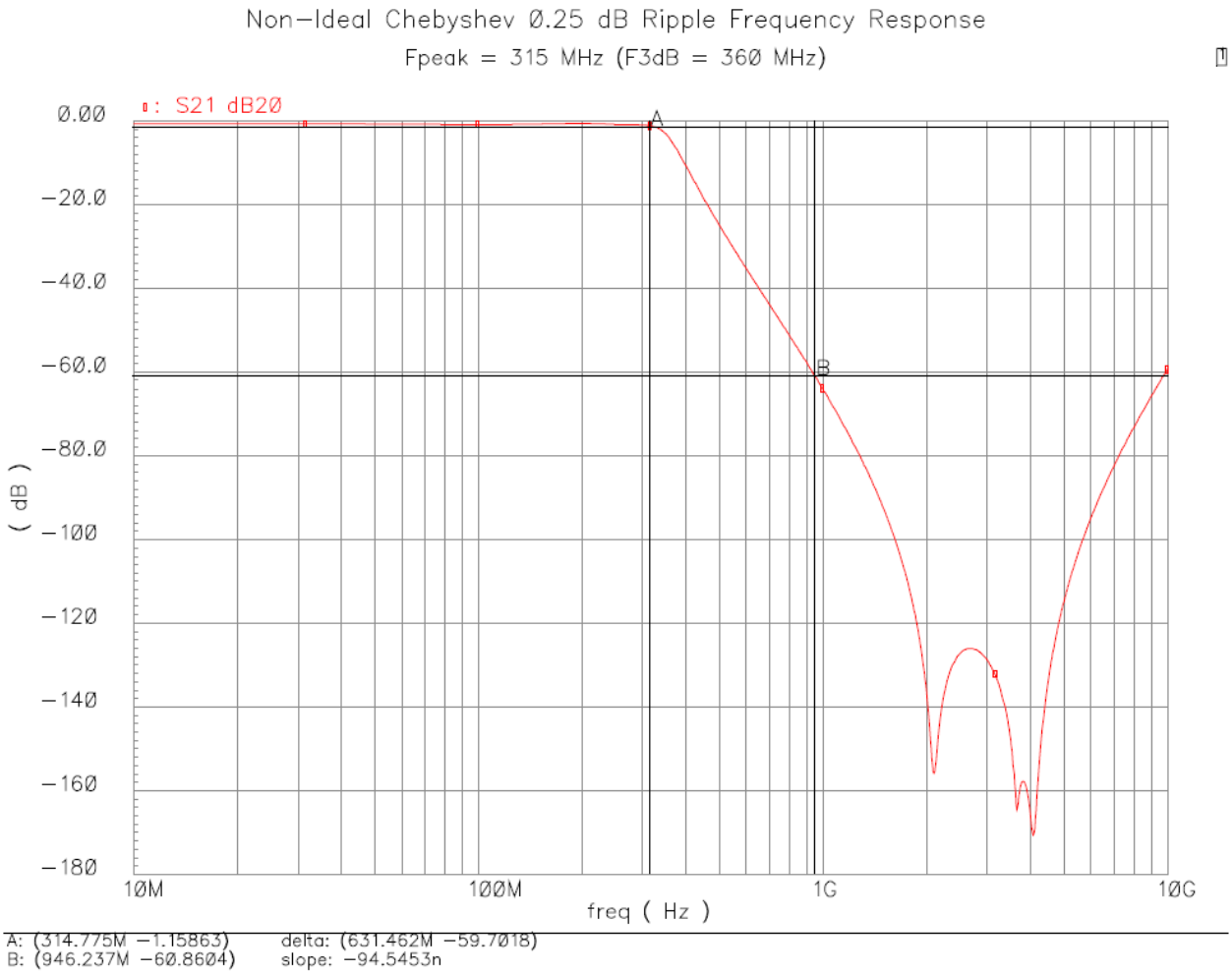

Figure 11. Non-Ideal Sim Freq Response of 0.25 dB Chebyshev Filter (315 MHz)

It can be seen that the simulated out-of-band attenuation at the third harmonic frequency (945 MHz) actually improves somewhat to 61 dB. It is apparent that there are now transmission zeroes in the simulated frequency response. These transmission zeroes (e.g., near 2.1 GHz and 4 GHz in Figure 11) are due to self-resonances in the discrete components. The shunt capacitors in the filter network (i.e. CM and CM2) exhibit a series self-resonance at some frequency, while the series inductors (i.e., L0, LM, and LM2) exhibit a parallel self-resonance at some frequency. The presence of such transmission zeroes may help to "bend down" the attenuation curve more quickly, resulting in improved attenuation at lower harmonic frequencies, but at the cost of degraded attenuation at higher harmonic frequencies. It is not advisable to rely too heavily upon "tuning" of these transmission zeroes to aid in meeting harmonic performance.

3.3.2.5. Measurement of Filter Frequency Response

This filter response can be obtained by building only the low-pass filter on a demonstration board. The resulting frequency response is shown in Figure 12.

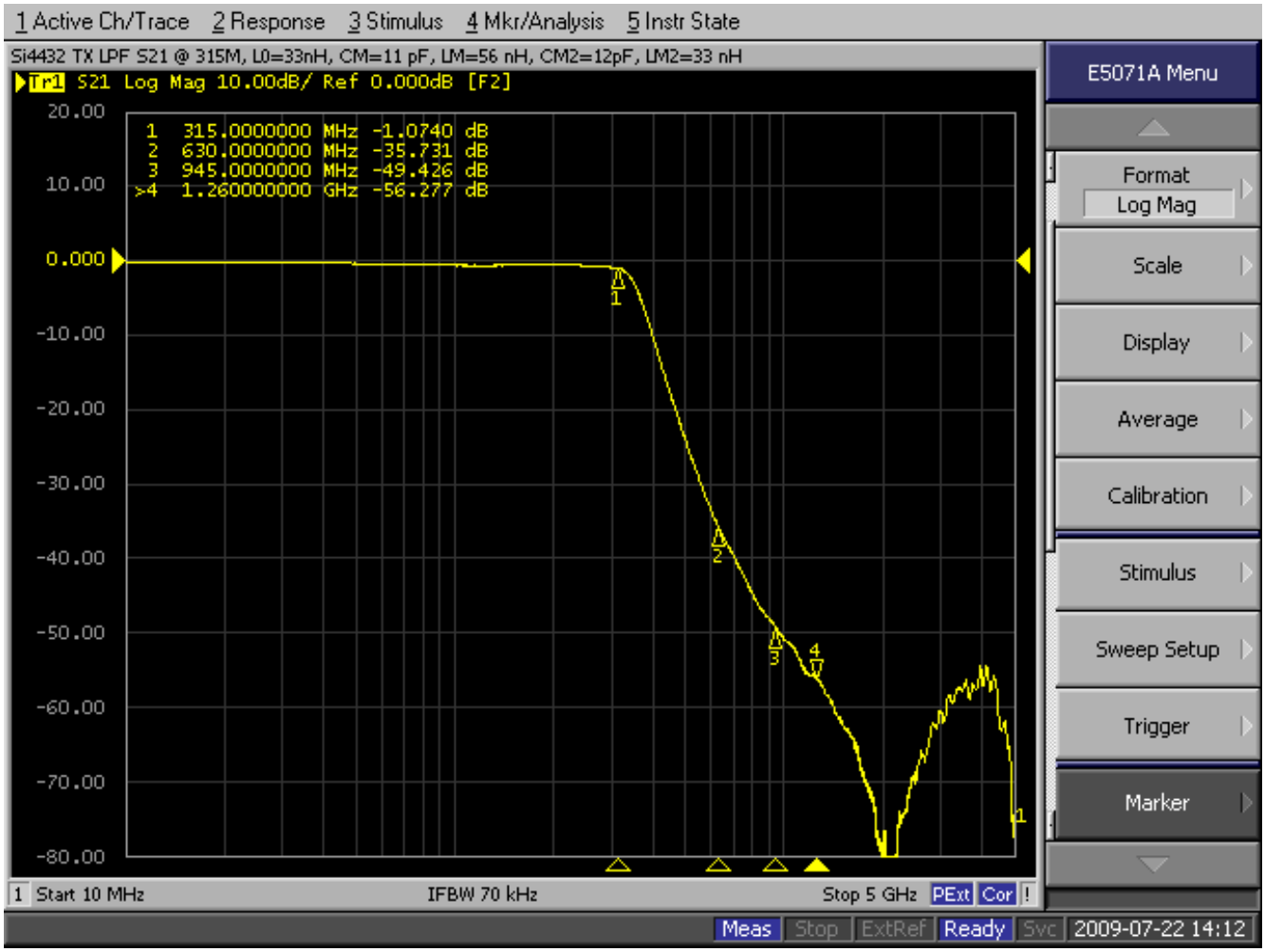

Figure 12. Actual Freq Response of 0.25 dB Chebyshev Filter (315 MHz)

It can be seen that the actual measured frequency response is quite similar to that predicted by simulation with SPICE models, with an in-band insertion loss of 1.07 dB at 315 MHz. However, the attenuation at the third harmonic frequency of 945 MHz is slightly less than predicted, at only 49.4 dB. As was discussed previously, it is possible to obtain slightly greater attenuation roll-off at the expense of greater in-band amplitude ripple (and thus potentially slightly higher insertion loss).

3.3.2.6. Impedance Considerations

Up to this point, we have only been concerned with simulation and measurement of the amplitude response over frequency. We have not yet paid attention to the impedance characteristics of the filter.

As discussed earlier, the power extracted from a switching-type amplifier is inversely proportional to the load resistance (RLOAD) presented to the output of the amplifier. It was stated (without proof) that the value of RLOAD appropriate for obtaining +20 dBm output power was approximately 50 Ω. It was for this reason that a filter response type providing a 1:1 impedance transformation was selected, since it is assumed that the antenna impedance (RANT) is also 50 Ω.

If the impedance (RLOAD) presented to the TX output of the RFIC differs from the target value of 50 Ω, the Si4032/4432 RFIC will continue to function well; however, certain parameters, such as TX output power or efficiency, may suffer somewhat as a result. For example, if the RLOAD impedance presented to the output of the PA is too high (e.g., as a result of accidental mistuning of the LPF network), it may not be possible to obtain the desired output power (+20 dBm). Conversely, if the RLOAD impedance is too low, the desired output power may easily be obtained (or exceeded), but at the expense of significantly increased current consumption.

For this reason, it is advisable to verify (by measurement) the impedance seen looking into the input of the low-pass filter network as built upon the RF Application Module. That is to say, it is recommended to verify the filter design when populated onto the actual module in which it is intended for use. In this fashion, the effects of board trace parasitics and ground via inductances may be included in the measurement. This measurement may be easily performed with a network analyzer. The value of RLOAD does not need to be exactly 50 Ω; a value anywhere in the range of RLOAD = (40 to 55) + j (–10 to +10) Ω should be sufficiently close.

3.3.3. Step #3: Design a Harmonic Termination Network

In Step 3, we finally design a network to provide a good impedance termination at all frequencies other than the fundamental operating frequency.

3.3.3.1. Reason for Proper Termination of Harmonic Signal Components

It should be noted that the nice square waveforms observed at the TX output pin in Step 1 (Figure 6 on page 12) were obtained with a broadband resistive RLOAD = 50 Ω. Although construction of a low-pass filter to attenuate the harmonics has been completed, the input impedance seen looking into this low-pass filter is not 50 Ω at all frequencies. With the TEE-filter topology that was chosen, the first component seen at the input of the filter is a series inductor; as a result, the input impedance becomes very high at frequencies above the passband. Because of this difference in characteristic impedance vs. frequency, it is not possible to simply "bolt on" the low-pass filter to the output of the PA and expect the same performance as with operation into a broadband resistive load.

It does make a significant difference. If the harmonic signal components are not terminated in (nearly) the same impedance as the fundamental, they can add constructively or destructively, resulting in a significantly distorted waveform at the TX output pin (i.e., no longer a square wave). The peak voltage of this waveform can reach a large value, potentially exceeding the absolute maximum voltage ratings of the RFIC.

As a result, it is desirable to design a sort of diplexer network. The fundamental signal component passes through (and is properly terminated by) a low-pass filter network while all other signal components are terminated in a separate network. Our goal is to obtain a network that provides a good impedance termination at all frequencies. The resulting voltage waveform at the TX output pin should, therefore, be indistinguishable from operation into a broadband resistive load.

3.3.3.2. Harmonic Termination Network Architecture

The harmonic termination network recommended by Silicon Labs is shown in Figure 13. It is essentially a parallel L-C tank with 50 Ω termination resistor added to the input of the low-pass filter. The idea is to choose the values of LHARM-CHARM such that the tank achieves parallel resonance at the desired fundamental operating frequency. At the fundamental frequency, this resonant tank exhibits (nearly) infinite impedance and essentially disconnects the 50 Ω harmonic termination resistor from the input of the low-pass filter. However, at all other frequencies, the LHARM-CHARM tank is far from parallel resonance and exhibits a low impedance, essentially connecting the 50 Ω RHARM termination resistor in parallel with the input of the low-pass filter. At these high harmonic frequencies, the input impedance seen looking into only the low-pass filter is very high; thus, the PA output is essentially terminated by only the RHARM resistor.

It should be noted that at all frequencies below the fundamental operating frequency, the PA output is terminated simultaneously by both paths and is essentially mismatched by seeing an effective 50 Ω // 50 Ω = 25 Ω load. However, this is of no consequence; there are no output signal components at any frequency below the fundamental that can be affected by such mis-termination.

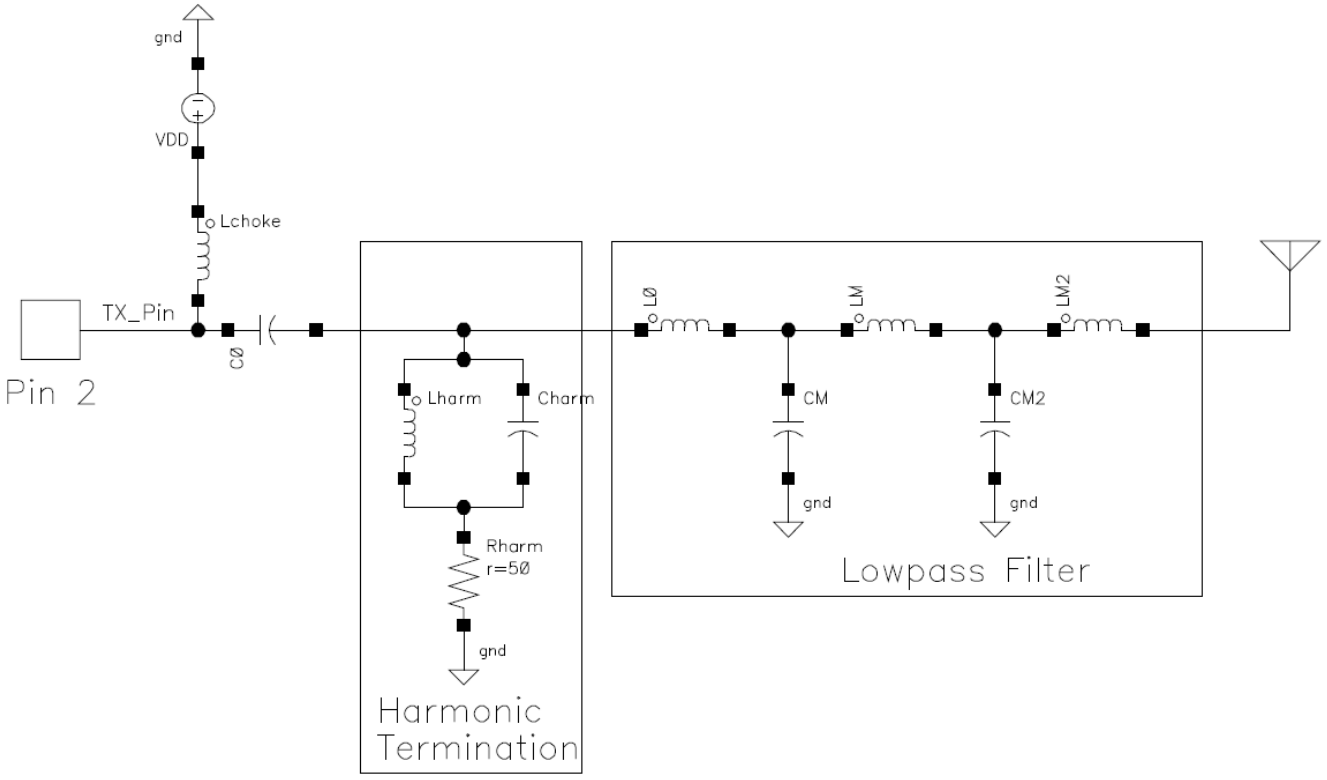

Figure 13. Lowpass Filter with Harmonic Termination Network

3.3.3.3. Selection of L_{HARM}-C_{HARM} Ratio

The need for choosing L_{HARM}-C_{HARM} to achieve parallel resonance at the desired operating frequency has been covered. However, there is obviously an infinite number of combinations of L_{HARM}-C_{HARM} values that can achieve parallel resonance at any given frequency.

There is an optimum L_{HARM}-C_{HARM} ratio. The simple explanation is that the L-C ratio determines how rapidly the tank impedance reduces from its maximum value of (near) infinity at its parallel resonant frequency to much lower values at frequencies far from resonance. This effectively determines how much the low-pass filter and the harmonic termination network "interact" with each other. It is preferable that these two networks not interact at all. The fundamental frequency is terminated by the low-pass filter; all harmonics are terminated by the harmonic termination network, and the processes are independent.

From a practical standpoint, however, the two networks are not so independent from each other. The impedance of the harmonic termination tank does not fall off so rapidly with increasing frequency that its effect upon the low-pass filter network can be ignored. In a similar fashion, the input impedance of the low-pass filter does not increase so rapidly with frequency that its effect upon the L_{HARM}-C_{HARM} network can be ignored.

In the time domain, a non-optimal L-C ratio can manifest itself as a voltage waveform at the TX pin that is not as flat as it could be (i.e., higher peak voltage than necessary). This is shown in Figure 14, which simulates with the optimum L-C ratio (red curve) as well as two non-optimum values of L-C ratio (blue and green curves).

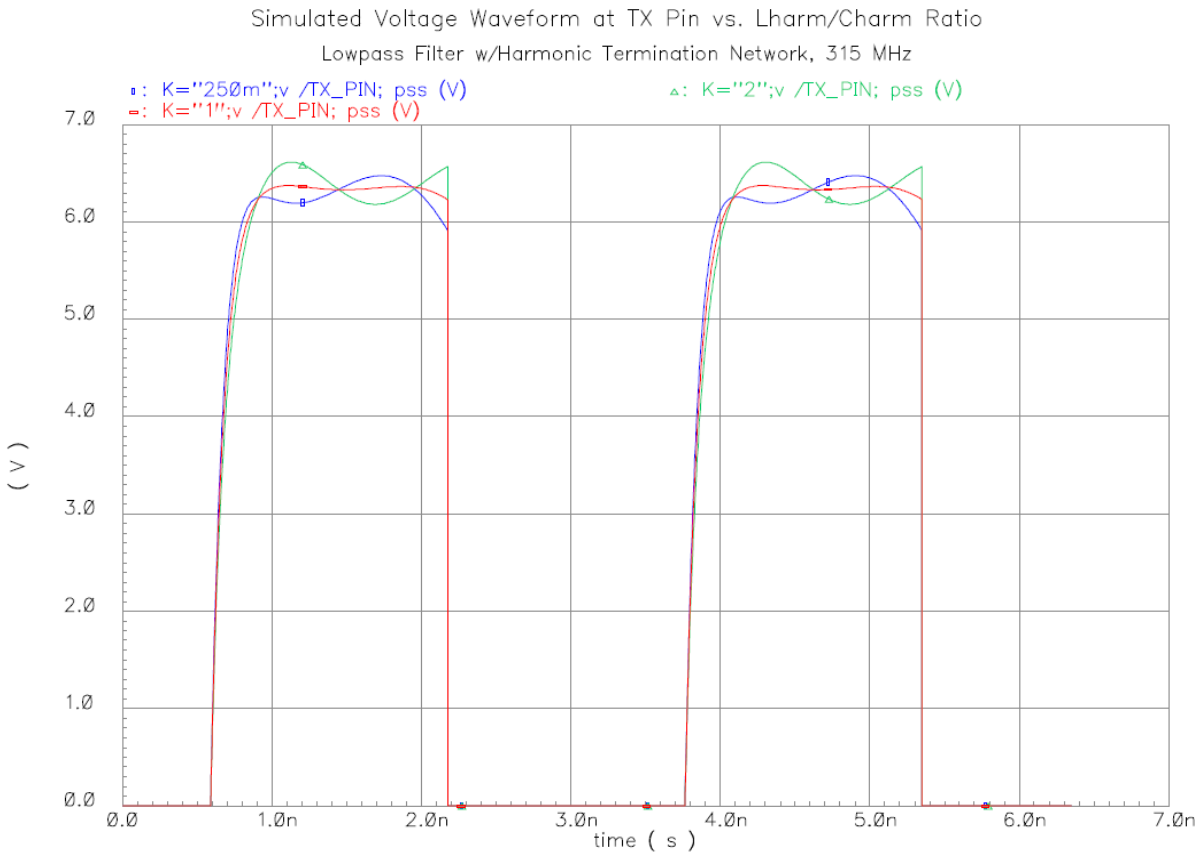

Figure 14. TX Voltage Waveforms vs. L_{HARM}-C_{HARM} Ration

The optimum L-C ratio has been determined by simulation, and has been found to be approximately equal to the following:

- L (in nH) / C (in pF) = 0.9

In practice, an L-C ratio anywhere between 0.8 and 1.0 will work reasonably well. It is suggested that the LHARM CHARM component values are chosen as the nearest 5% standard values that simultaneously:

- Provide parallel resonance at the desired operating frequency
- Provide an L-C ratio between 0.8 and 1.0

3.3.4. Low-Pass Filter Design Methodology for Board Configuration with RF Switch

In "3.3.2. Step #2: Design a Low-Pass Filter (for Split TX/RX Board Configuration)" on page 12 a low-pass filter was designed for a board configuration that did not contain an RF switch to select between the TX and RX paths, but instead provided a separate antenna for each path. The low-pass filter topology required for a board configuration containing an RF switch is somewhat different and is discussed in this section.

It would seem obvious to simply the place the RF switch immediately prior to the antenna. In such a topology, the common port of the switch would be connected to the antenna, one switched port would be connected to the RX path and LNA input match, and the other switched port would be connected to a TX path containing the exact same low-pass filter network developed for the Split TX/RX board configuration.

However, the RF switch itself is not a perfectly ideal component; it will re-generate some amount of harmonic energy, regardless of the cleanliness of the input signal from the TX low-pass filter. Thus it is necessary to place some amount of low-pass filtering after the RF switch and prior to the antenna. It is not required to increase the total order of low-pass filtering (i.e., number of filter poles); instead, it is generally sufficient to split the normal amount of low-pass filtering into two half-filter sections of approximately equal cutoff frequency. The RF switch is placed between these two half-filter sections. In this fashion, the final half-filter section cleans up any harmonic energy re-generated by the RF switch. This matching topology is shown in Figure 2 on page 3.

The design methodology for the two filter sections is quite simple: design one 3rd-order low-pass filter using a TEE-architecture, and another 3rd-order low-pass filter using a PI-architecture. (The use of the PI-architecture for one filter section is desirable as its shunt capacitive elements help to absorb any stray parasitic capacitance associated with the RF switch or the PCB traces.) A Chebyshev filter response is again recommended, with an in-band amplitude ripple of approximately 0.5 dB. The cutoff frequency of each section is chosen slightly higher than the desired operating frequency, such that the desired signal falls at the peak of the passband amplitude ripple.

3.3.5. Summary of Match

This completes the steps of the match design process. This match design process may be used to obtain matching component values at any desired operating frequency. Summary tables of these matching component values are shown in Table 1 on page 2 and Table 2 on page 3.

NOTES:

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