Wen-Chieh (Laurent) Lo

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Education

National Taiwan University Sept. 2020 – June 2024

Bachelor of Science in Electrical Engineering

- GPA: 3.99/4.3
- Relevant Coursework: , Computer Architecture(A), Digital Circuit Design Lab(A), Computer-aided VLSI System Design(A), Integrated Circuit Design(A), Algorithm, Data Structure, Linear Algebra, Discrete Math, Operating System,Computer Vision

Work Experience

Digital IC Design Intern, Mediatek July. 2023 – August 2023

- Designing NoC IP low-power clock control flow using clock management IP
  - Designed an automatic power-saving SPEC for the clock tree in NoC System Modules
  - Utilizing **Verdi** for module behavior tracing.
- Performance, Power, and Area analysis of Configuration BUS in interconnect
  - Utilizing **Perl**, and **Shell Script** for Synthesis flow design.

Lab Intern in Prof. Ryan Kastner's Lab,UC San Diego July. 2022 – August 2022

- Implemented an accumulator bitwidth optimization feature for the HLS4ML real-time Machine Learning Model Inference toolkit, reducing the user's time spent on finetuning.

Project Experience

Memory-Efficient Hardware Accelerator for Spliced Genome Alignment Prof. Yi-Chang Lu's Lab

- Developed an end-to-end spliced genome alignment in ASIC.
  - Developed a pipeline syncmer-minimizer extraction in the seeding stage.
  - Performing bitwidth reduction for alignment traceback that reduces over **98%** of memory usage.
  - Achieved **over 10x** speedup compared to minimap2 under TSMC 28nm process.

Automated Audio Beat Detection On FPGA Digital Circuit Lab

- Developed and implemented FPGA-based hardware for real-time music recording and automatic beat detection, utilizing an onset detection algorithm.
  - Analyzed Onset Strength in the frequency domain to detect potential beat formation.
  - Utilized a mere **25%** of the Altera DE2-115 FPGA's total logic, ensuring a lightweight implementation.
  - Achieved **70% accuracy** compared to fine-tuned Python onset detection tool Librosa.
  - Received the **2nd highest score** among all the teams

QR Decomposition of MIMO Demodulation Computer-Aided VLSI System Design

- Designed modified Gram-Schmidt Algorithm demodulation hardware for QR Decomposition in MIMO Receiver
  - Ranked **3rd** among Undergraduate Students in Final Performance.
  - Utilized **Verilog**, **Design Vision**, **Innovus**, and **PrimeTime** for ASIC RTL to APR design flow.

Automated Bitwidth Optimization for HLS4ML Prof. Ryan Kastner's Lab

- Developed an automatic accumulator bitwidth selection feature for a machine learning model deployment tool on FPGA.
  - Allowed users to automatically set up optimal accumulator bitwidth for different layers to achieve the most effective resource usage.
  - Established bitwidths for each layer using mathematical bounds to guarantee overflow prevention.

Technical Skills

- Language: Verilog, System Verilog, C ++, Python, Perl, Matlab
- Tools: Verdi, Design Vision, Innovus, PrimeTime, Quartus FPGA