Wen Chieh Lo

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Education

National Taiwan University, BS in Electrical Engineering — Sept 2020 – June 2024

- GPA: 3.99/4.30 (3.83/4.00)
- **Coursework:** Computer Architecture(A), Digital Circuit Design Lab(A), Computer-aided VLSI System Design(A), Integrated Circuit Design(A) Operating System(A), Algorithm, Data Structure, Linear Algebra, Discrete Math

Experience

Undergraduate Researcher, Prof. Yi-Chang Lu's Lab @ National Taiwan University — Feb. 2023 – Now

- Designed **the first memory-efficient syncmer based end-to-end hardware accelerated genome sequence aligner**, achieving **over 10x speedup** compared to minimap2 under TSMC 28nm process.
- Proposed the **first-ever hardware-friendly syncmer extraction hardware**, utilizing FIFO and a 2-stage buffer to enable pipelined dual-parameter offset syncmer extraction.
- Performed bitwidth reduction for alignment traceback, optimizing spliced alignment by storing traceback information with only 5 bits and using a heuristic to omit intermediate storage for long introns, reducing over **98% of memory usage**.

Digital IC Design Intern, SoC Integration Team @ MediaTek — Jul. 2023 – Aug. 2023

- Designed a **dynamic clock control flow for Network-on-Chip (NoC)** nodes with dynamic clock management IP, optimizing power efficiency and preventing packet transmission conflicts by ensuring no other packets are being transmitted during clock transitions.
- Developed a signaling mechanism to prevent data loss during clock restart, while supporting reliable transmission across different clock domains within the NoC system.
- Maintained the synthesis environment and for performance, power, and area analysis of Configuration BUS.

Undergraduate Researcher, Prof. Ryan Kastner's Lab @ UC San Diego — Jul. 2022 – Aug. 2022

- Developed an a**utomatic accumulator bitwidth optimization feature** for the HLS4ML real-time Machine Learning Model Inference toolkit, for both Fully Connected and Convolutional layers, leveraging the **wrap-around property** to ensure efficient resource utilization and overflow prevention.
- Established precision bounds (Pessimistic, Conservative, and Optimistic) based on weight data, input data, and kernel specifications, using a custom method to enable flexible bitwidth configurations for diverse neural network architectures.

Projects

QR Decomposition of MIMO Demodulation — Nov. 2023 – Dec. 2023

- Designed hardware for QR Decomposition in a MIMO receiver using the Modified Gram-Schmidt Algorithm.
- Implemented fine-grain pipelining to enhance throughput and optimized hardware re-utilization to improve resource efficiency.
- Ranked **3rd in final performance** among undergraduate teams in post-layout power-performance-area performance evaluation.

FPGA-Accelerated Audio Beat Detection Using Spectral Flux Analysis — April. 2023 – June. 2023

- Developed a music recording and automatic beat detection system on FPGA. Utilized 8-point pipelined FFT and spectral flux analysis in the frequency domain to analyze onset strength and identify potential beats.
- Utilized a mere **25% of the Altera DE2-115 FPGA's total logic**, ensuring a lightweight implementation.

Award

2021 Xilinx PYNQ AI/IoT Hackathon 2nd Place

Skills

Languages: Verilog, System Verilog, C ++, Python, Perl, Matlab

Technologies: Verdi, Design Vision, Innovus, PrimeTime, Quartus FPGA