MADVLSI: MP1 Report

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In Mini Project 1, I made a schematic diagram of an AND gate in xschem, a transistor layout design of the AND gate in Magic, and used Netgen to compare the differences between the two designs.

1 Schematic Capture and Simulation

Figure 1 shows the highest level of schematic diagram of the AND gate in xschem. It consists of two subcircuits, which are the NAND gate shown in Figure 2 and the inverter shown in Figure 3.

Figure 4 shows the schematic diagram of the AND gate that contains transient simulation configurations. The results of the simulation is shown in Figure 5.

2 Layout Design

The layout of the AND gate in Magic is shown in Figure 6.

3 Layout Versus Schematic

The layout versus schematic (LVS) output showed that the two circuits made in xschem and Magic matched up. The file can be accessed here.

4 Design files

All the design files of MP1 can be accessed here.

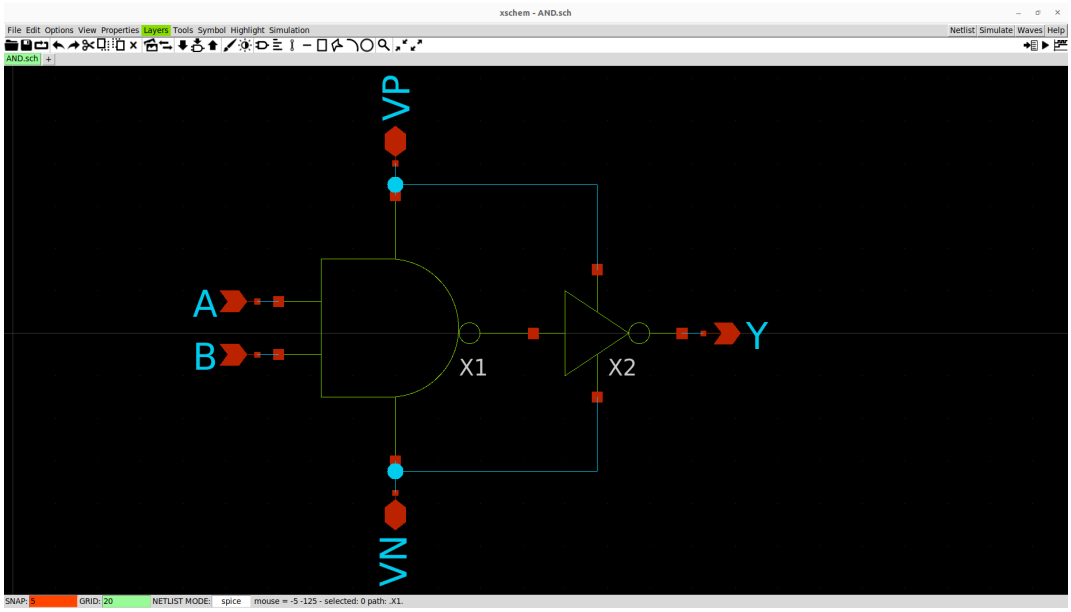

Figure 1: AND gate high level schematic diagram.

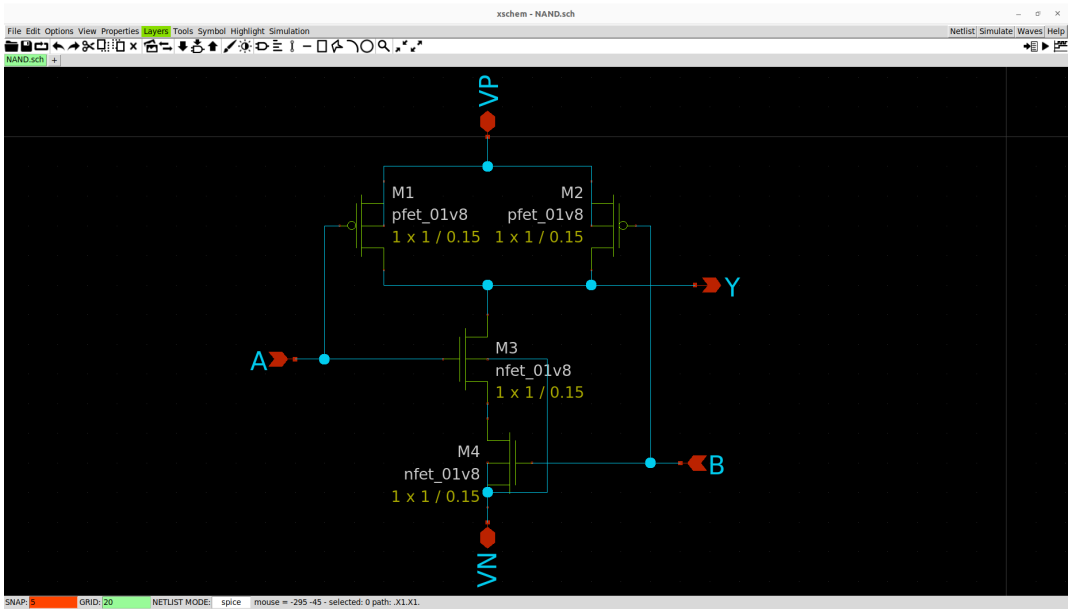

Figure 2: NAND gate schematic diagram.

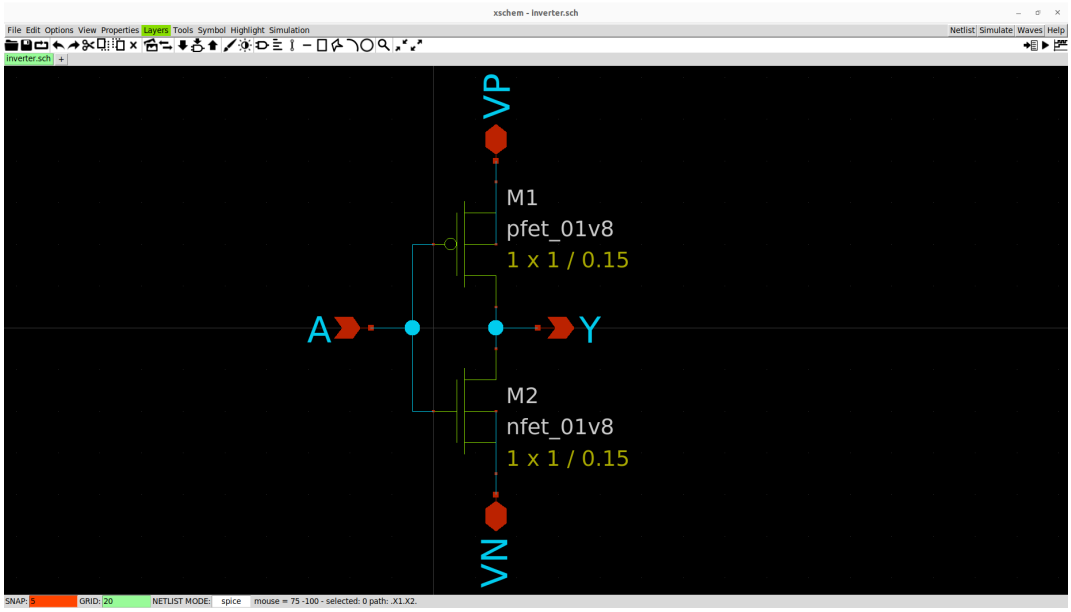

Figure 3: Inverter schematic diagram.

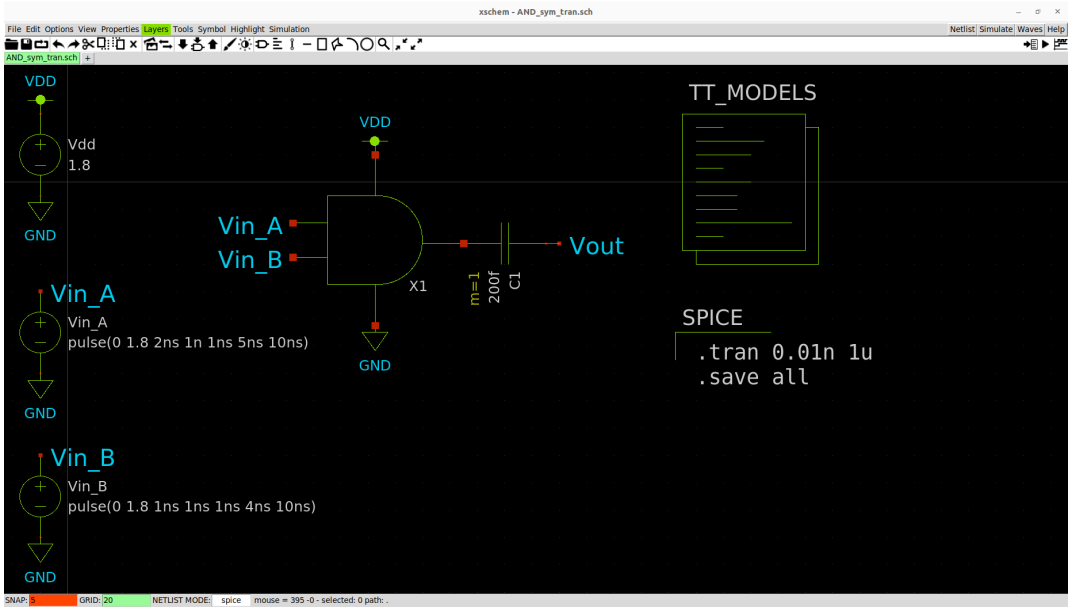

Figure 4: Simulation schematic diagram of the AND gate.

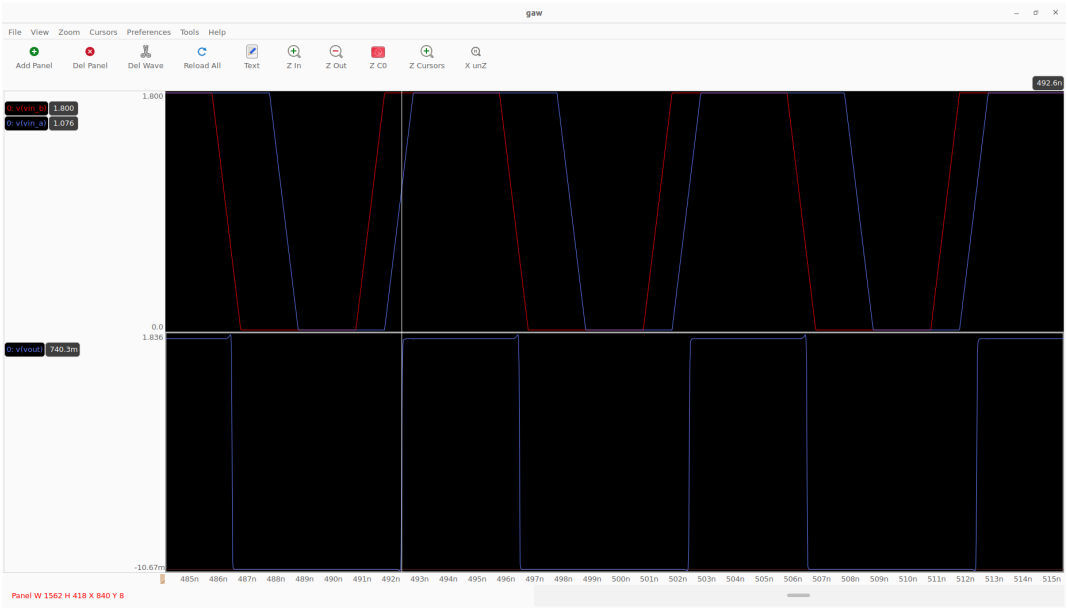

Figure 5: Transient simulation results.

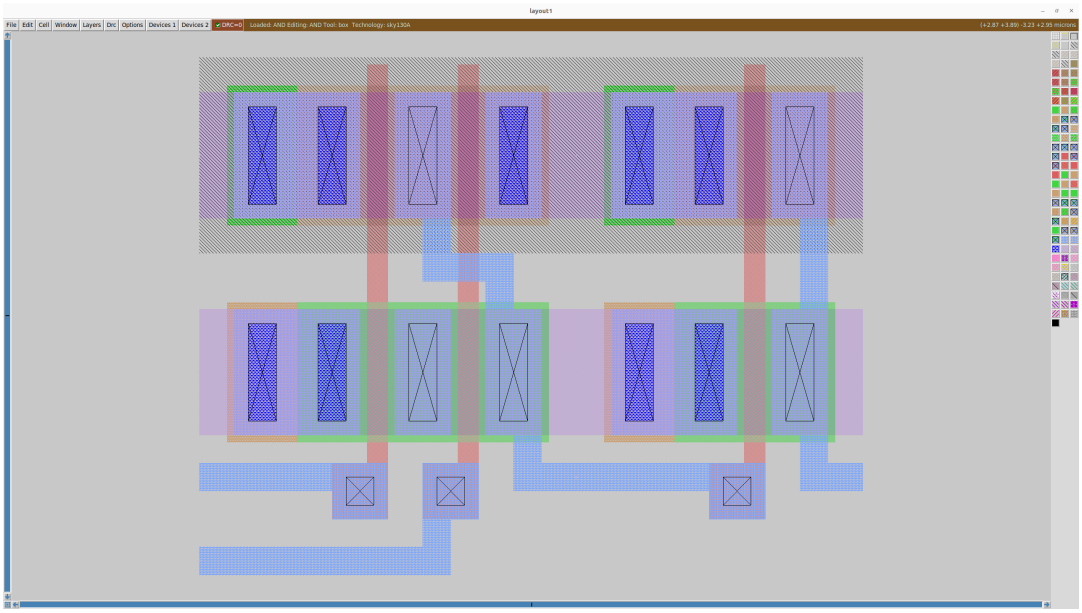

Figure 6: Layout of AND gate in Magic.