MADVLSI: MP3 Report

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1 Grok the Circuit

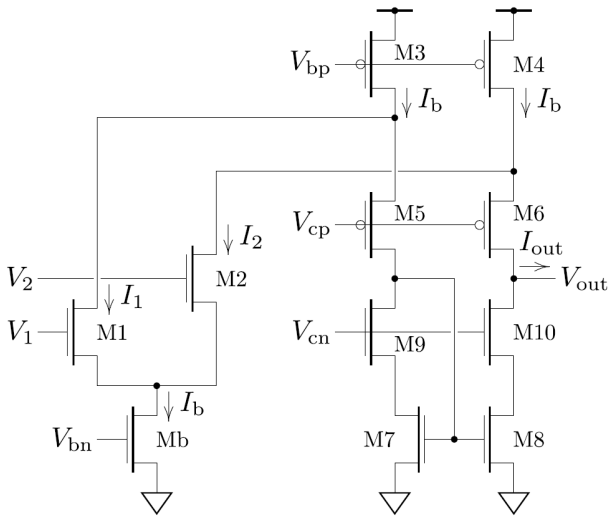

Figure 1: Schematic of a folded-cascode differential amplifier.

(a) Consider the differential amplifier circuit shown in the attached schematic comprising an nMOS differential pair, four pMOS transistors, and a nMOS low-voltage cascode current mirror. Such a circuit is called a folded-cascode differential amplifier. Transistors M5 and M6 act as cascode transistors, pinning the drains of the diff-pair transistors, M1 and M2. Transistors M3 and M4 act as current sources, providing pivot points for folding over the differential-pair output currents. Which input voltage is the noninverting input? Which is the inverting input? Explain your reasoning briefly.

When we slightly increase V_1, we can assume that the current through $M1$ would be $(I_1 + \delta I)$ and that through $M2$ would be $(I_2 - \delta I)$. Therefore, according to KCL, the current before the drain of $M5$ would be $(I_b - (I_1 + \delta I)) = (I_b - I_1 - \delta I)$, and that of $M6$ would be $(I_b - (I_2 - \delta I)) = (I_b - I_2 + \delta I)$. When both $M5$ and $M6$ are on and saturated, I_{out} should be equivalent to the current through $M6$, which experienced a small increase $+\delta I$. Therefore, V_1 is the noninverting input, and V_2 is the inverting input of the circuit.

(b) What is the allowable common-mode input voltage range of this circuit? Explain your reasoning.

Because we want Mb to be always saturated for proper operation of the circuit, we want to make sure that the drain voltage of Mb is always equal or greater than V_{DSsat}. Because we know that in a

typical source follower circuit, $V_{out} = \kappa(V_{in} - V_b)$ where V_{in} is the gate voltage of the source follower, we should at least make sure that the common-mode voltage satisfies this rule. Therefore, we have $\kappa(V_{cn} - V_b) \geq V_{DSsat}$, and we can further organize it to derive that $V_{cm} \geq V_b + \frac{V_{DSsat}}{\kappa}$.

(c) If the output voltage were fixed by a voltage source somewhere in the middle of the rails, what would be the output current in terms of I_1 and I_2 if the Early effect were negligible?

Because the current in $M7$, $M8$, $M9$ and $M10$ mirrors one another, the current through $M10$ should be $(I_b = I_1)$. Since we know that the current through $M6$ is $(I_b - I_2)$, we have $I_{out} = I_{M6} - I_{M10} = I_b - I_2 - I_b + I_1 = I_1 - I_2$.

(d) Do we need to make the bias current sourced by M3 and M4 equal to the diff-pair bias current, I_b? If so, explain why. If not, what constraints exist on this current level with respect to I_b?

We do not have to make the bias current coming from the current sources $M3$ and $M4$ equivalent to I_b, because it does not necessarily affect the magnitude of I_{out}, which equals the difference between I_1 and I_2. With that being said, we should still make sure that the bias current through $M3$ or $M4$ at least equals or is greater than both I_1 and I_2 (denoted by $max(I_1, I_2)$ so that the current could flow in the directions as we expected for proper operation of the circuit.

(e) Using the basic low-voltage cascode bias circuit that we discussed in class as a starting point, design a bias circuit for the folded-cascode amplifier that receives input from a single current source, I_b, and generates cascode bias voltages, V_{cn} and V_{cp}, optimally for a given bias current Ib so as to maximize the output voltage swing of the amplifier. Your circuit must also generate the other bias voltages, V_{bn} and V_{bp}, so that $I_3 = I_4 = I_b$.

The design of the voltage generator circuit is shown in Figure 2. Note that the transistors are unit-sized at this stage, and the sized layout-driven-schematics can be found in the design files package at the end of this document.

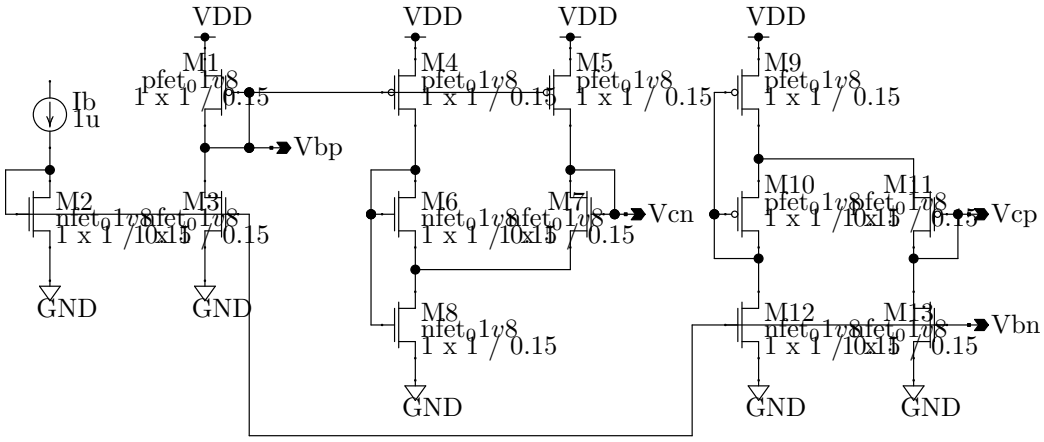

Figure 2: Design of the bias voltage generator and the cascode voltage generator circuits.

2 Schematic Capture and Simulation

(a) Voltage Transfer Characteristics. Perform a simulation to obtain VTCs as you sweep the noninverting input for at least five different values of the inverting input voltage that are spread evenly throughout the allowable common-mode input-voltage range. Turn in a plot showing these VTCs. What is the DC gain of this circuit from the slope of the VTCs?

The plot of VTC is shown in Figure 3. The DC gain of the circuit computed from the slope of the VTCs is approximately 510 ($\pm 5\%$).

(b) Voltage-to-Current Transfer Characteristics. Fix the output voltage of the amplifier somewhere in the middle of the rails so that all of the transistors in the output branch will operate in saturation. For a single value of the inverting input voltage (choose one of those for which you measured a VTC), measure the ouput current as you sweep the noninverting input around the inverting input voltage. Turn in a plot showing the amplifier's voltage-to-current characteristics. What is the incremental transconductance gain of the circuit? What are the limiting values of the output current?

The incremental transconductance gain of the circuit computed from the slope of voltage-to-current transfer characteristics curve is approximately $1.2 \times 10^{-5} \frac{1}{\Omega}$. The current input of the bias generator circuit is $I_b = 1\mu A$, and we can tell from the graph that I_out generally lies within the range from $-I_b$ to $+Ib$.

(c) Loopgain. Connect a 2-pF capacitor between the output of your amplifier and ground. Attach a DC source to the noninverting input and adjust its value to match the voltage that you used for the simulation of the circuit's voltage-to-current transfer characteristics. Simulate the loopgain of your circuit by attaching an AC voltage source in the feedback loop, as discussed in the tutorial video. You can use a 1-V AC magnitude and a phase of zero degrees for convenience. Perform an AC analysis on the circuit, measuring the loopgain of the circuit from 1 Hz to 1 GHz. Turn in a plot showing the magnitude (in dB) and phase (in degrees) of the amplifier's loopgain. How does the low-frequency gain compare with the one you obtained from the VTC? What is the unity-gain crossover frequency? How does this value compare with the one you would expect from the circuit's load capacitance and

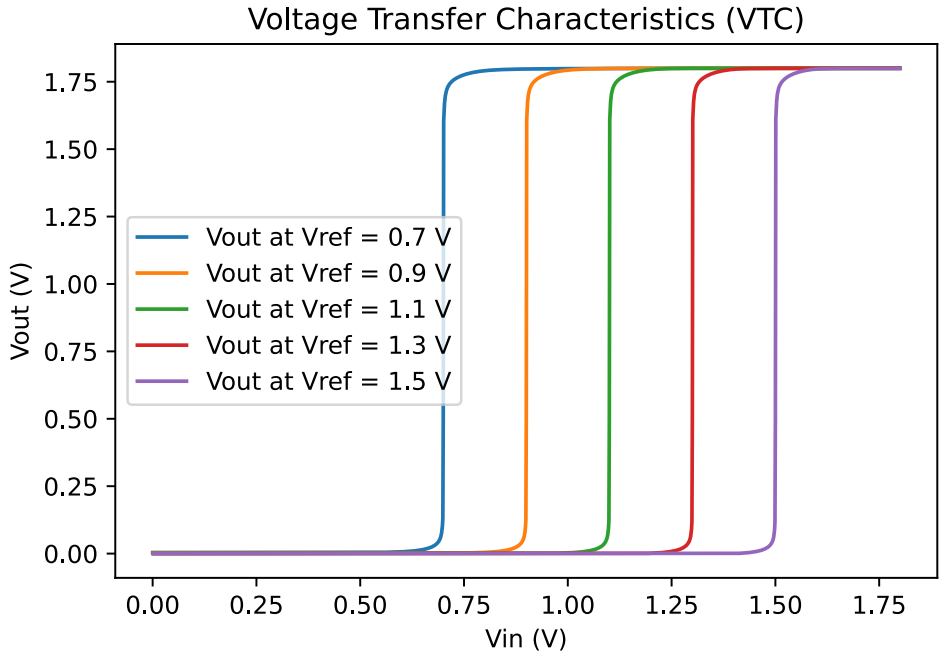

Figure 3: Plot of the Voltage Transfer Characteristics (VTC) of the circuit.

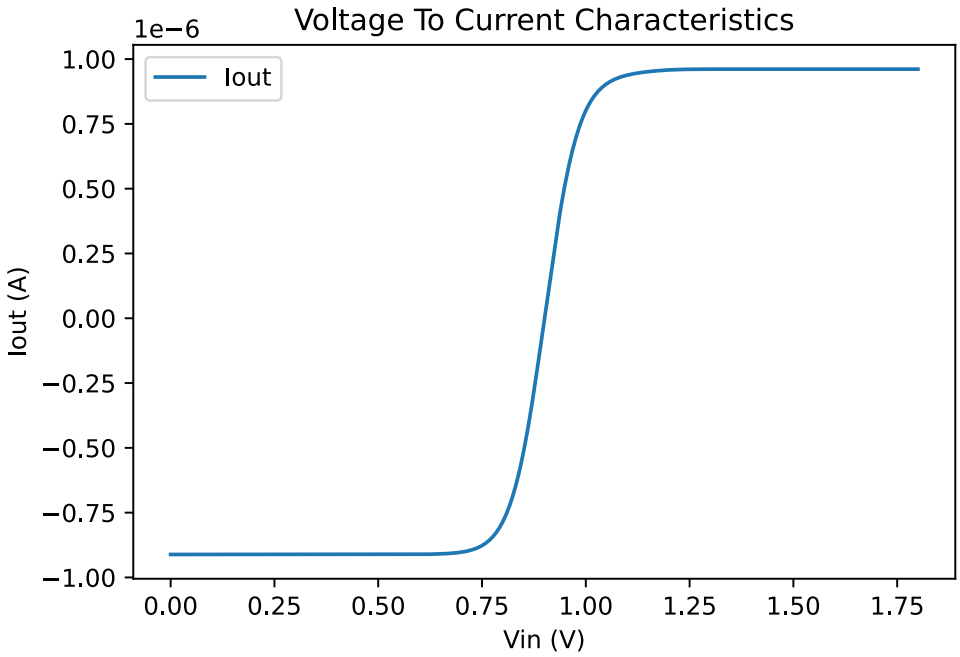

Figure 4: Plot of the voltage-to-current characterstics of the circuit.

its incremental transconductance gain?

The low-frequency gain extracted from the graph is 67.7 dB, which is equivalent to a linear atten-

uation of 2427. This is approximately five times compared to the result derived from the VTC. An estimation of the unity-gain crossover frequency can be drrived from the equation

$$f = \frac{Gm}{C} \times \frac{1}{2\pi} = \frac{1.12 \times 10^{-5}}{2 \times 10^{-12} \times 2\pi} \approx 0.891 \times 10^{6} Hz.$$

The unity-gain crossover frequency extracted from the data is approximately 0.925 MHz, which is quite close to the estimated value.

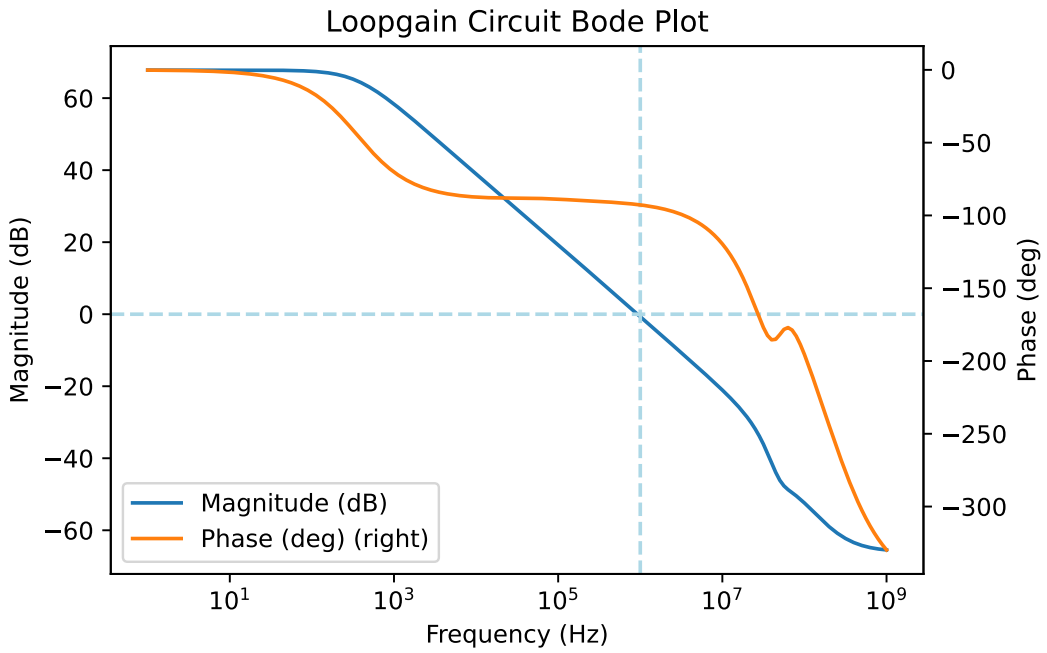

Figure 5: Bode plot of the circuit in its loopgain configuration.

(d) Unity-Gain Follower Frequency Response. With the 2-pF load capacitor in place, connect your amplifier as a unity-gain follower. Using the same DC offset as you have been using, perform an AC analysis of your circuit over the same range of frequencies that you just used for the open-loop response. Turn in a plot showing the magnitude and phase response of the circuits transfer function. How does the corner frequency in the circuit's response compare to the unity-gain crossover frequency in the loopgain?

The corner frequency of the circuit is approximately 0.55 MHz, which is about 0.35 MHz lower than the unity-gain crossover frequency in the loopgain.

3 Layout Design

The layout design of the top level circuit is shown in Figure 7.

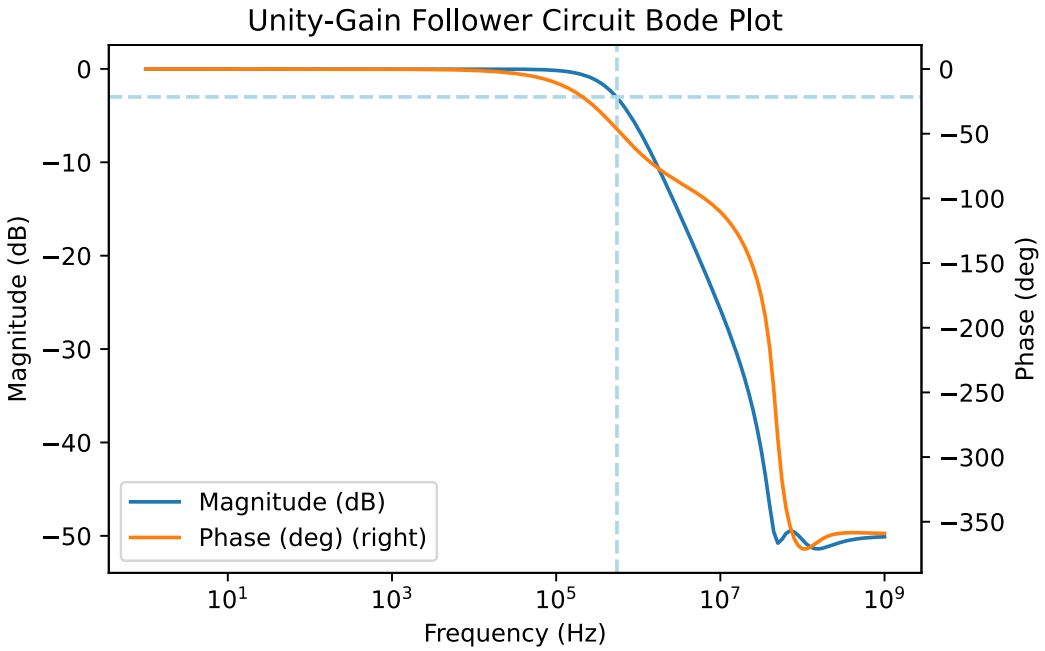

Figure 6: Bode plot of the circuit in its unity-gain follower configuration.

4 Layout Versus Schematic

The layout versus schematic (LVS) output can be accessed here. The results showed that the netlists matched uniquely.

5 Design files

All the design files of MP3 can be accessed here.

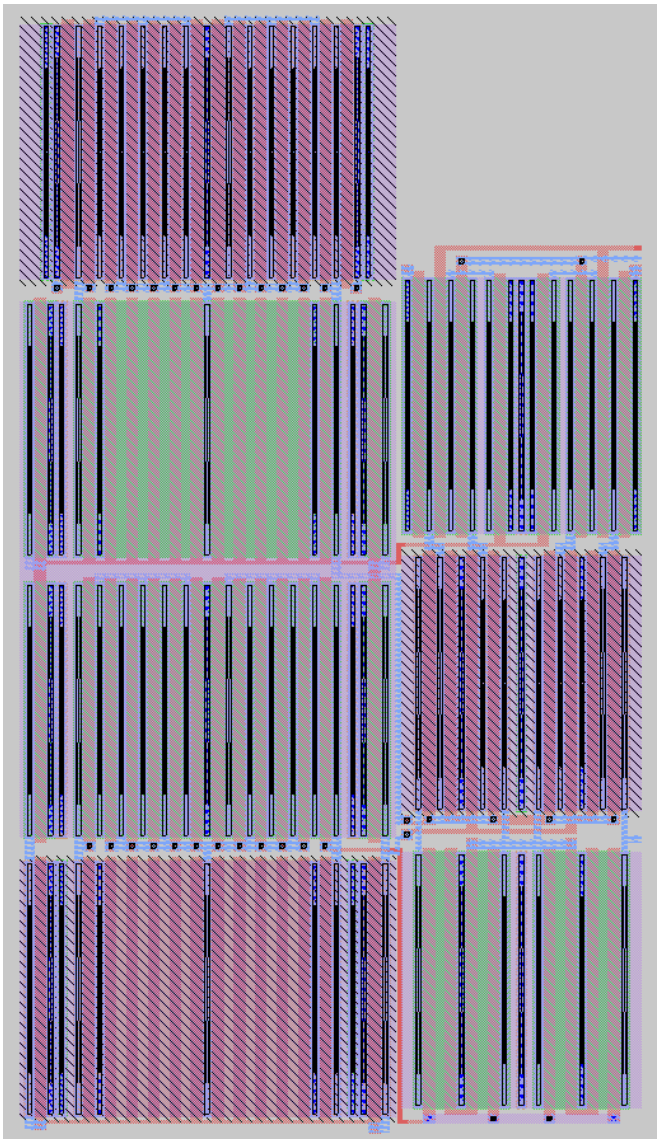

Figure 7: Layout of the cascode voltage generator circuit, the bias voltage generator circuit, and the folded-cascode differential amplifier.