MADVLSI: MP2 Report

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In Mini Project 2, we made a complementary set-reset logic (CSRL) D flip-flop unit, and connected four copies of it in series to make a 4-bit shift register. This report includes four main sections: schematic capture and simulation that shows the schematic diagram in xschem and transient simulation results, layout design in Skywater technology, a layout versus schematic (LVS) that compared the schematic and layout designs, and a link to the design files in the end.

1 Schematic Capture and Simulation

Figure 1 shows the transistor level schematic of the CSRL D flip-flop unit. The high level schematic of four of these D flip-flop units connected in series is shown in Figure 2.

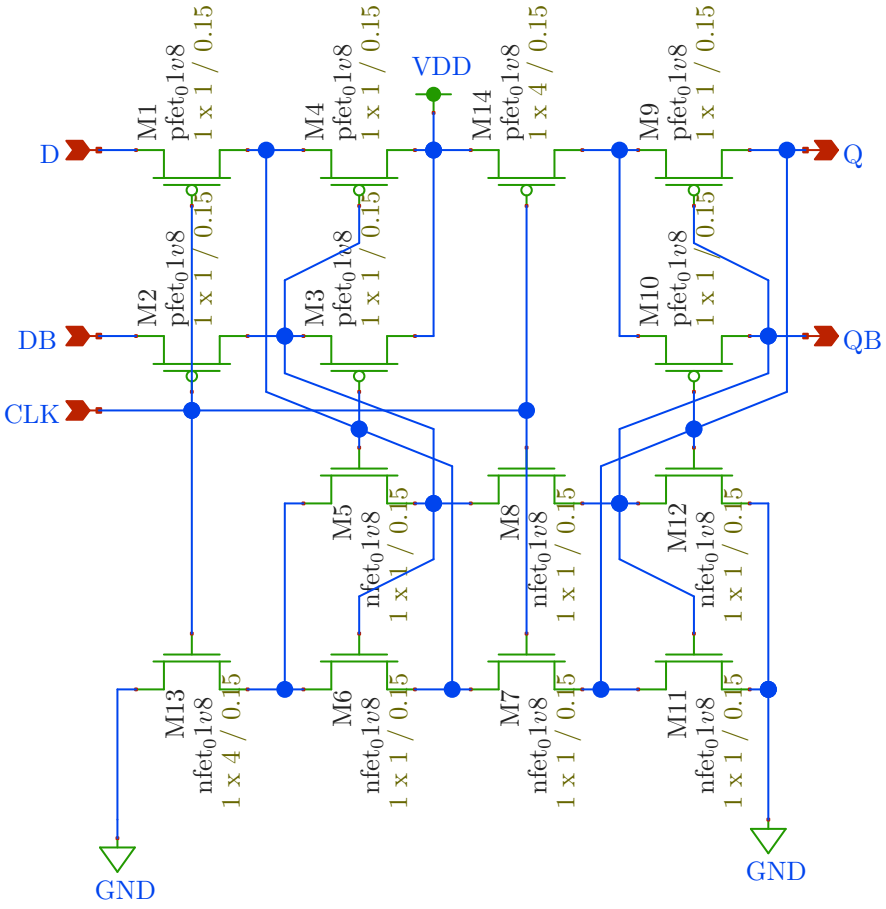

Figure 1: A transistor level layout-driven schematic of a CSRL D flip-flop unit created in xschem. (note: DB and QB in the schematic diagram stand for $\bar{D}$ and $\bar{Q}$ respectively.)

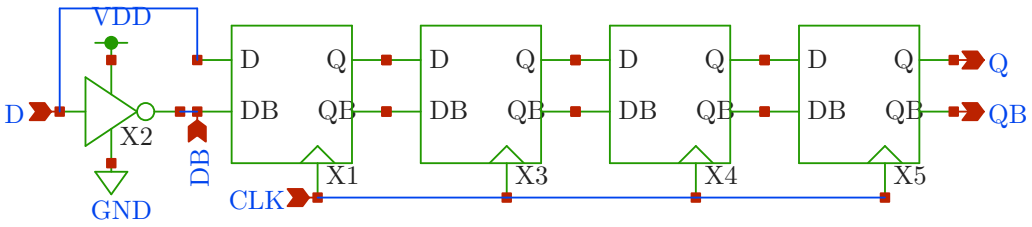

Figure 2: High level schematic of a four-bit register made from four CSRL D flip-flop units and an inverter that generates signals for the port of the first D flip-flop.

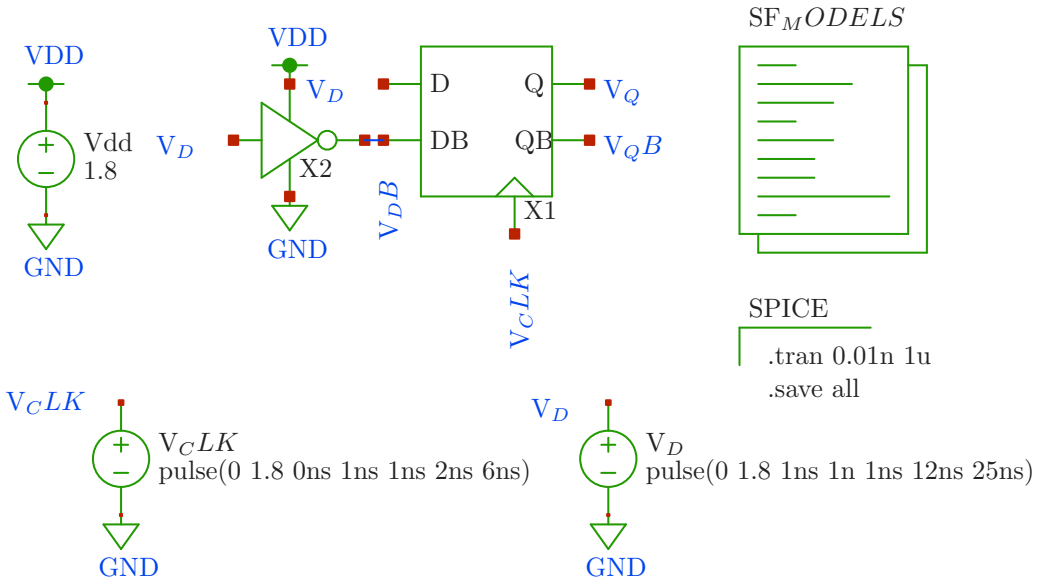

Figure 3: Simulation schematic diagram of the CSRL D flip-flop unit.

Figure 3 shows the schematic diagram of the single CSRL D flip-flop unit that contains the transient simulation configurations. The results of the simulation is shown in Figure 4.

Figure 5 shows the schematic diagram of the 4-bit shift register with transient simulation configurations. The results of the simulation is shown in Figure 6.

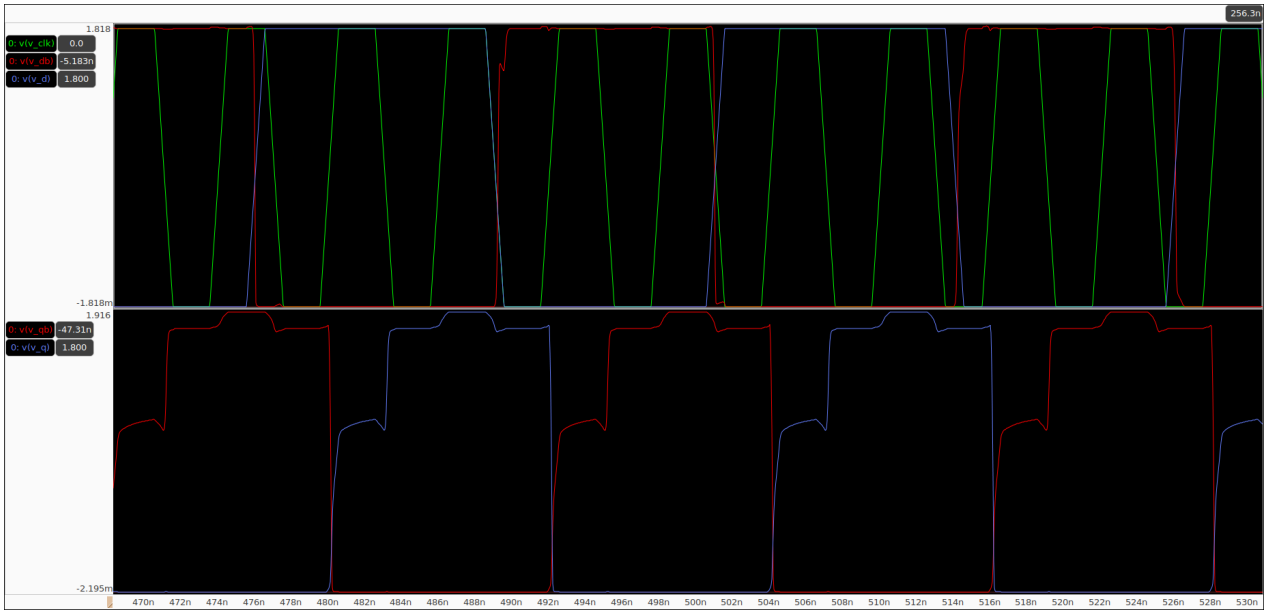

Figure 4: Simulation results of a CSRL D flip-flop in Ngspice.

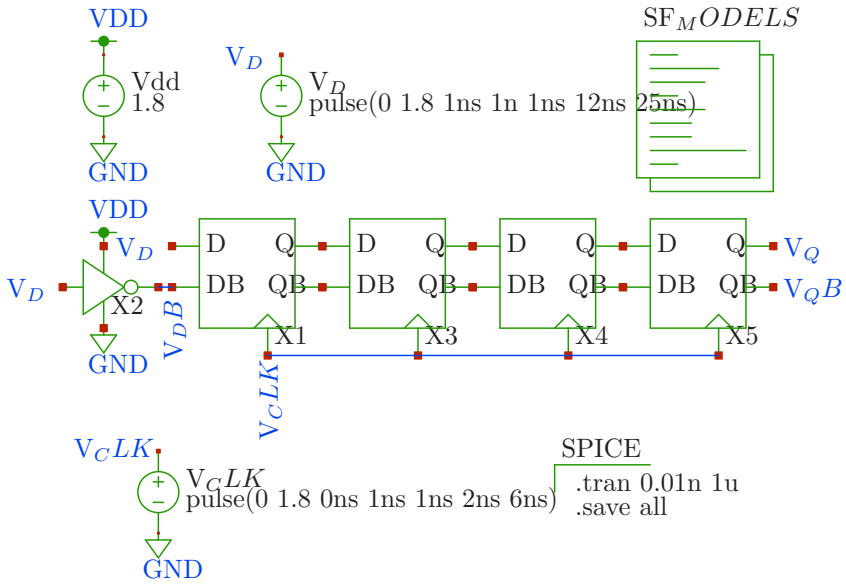

Figure 5: Transient simulation schematic of the four-bit shift register.

2 Layout Design

The layout of the single CSRL D flip-flop unit in Magic is shown in Figure 7. The dimension of a single D flip-flop is $3.400\mu m \times 10.700\mu m$ (width $\times$ height). The layout of the four-bit shift register, including the inverter that generates $\bar{D}$ signals for the first CSRL D flip-flop, is shown in Figure 8. The overall dimension of the four-bit shift register is $15.150\mu m \times 10.700\mu m$ (width $\times$ height).

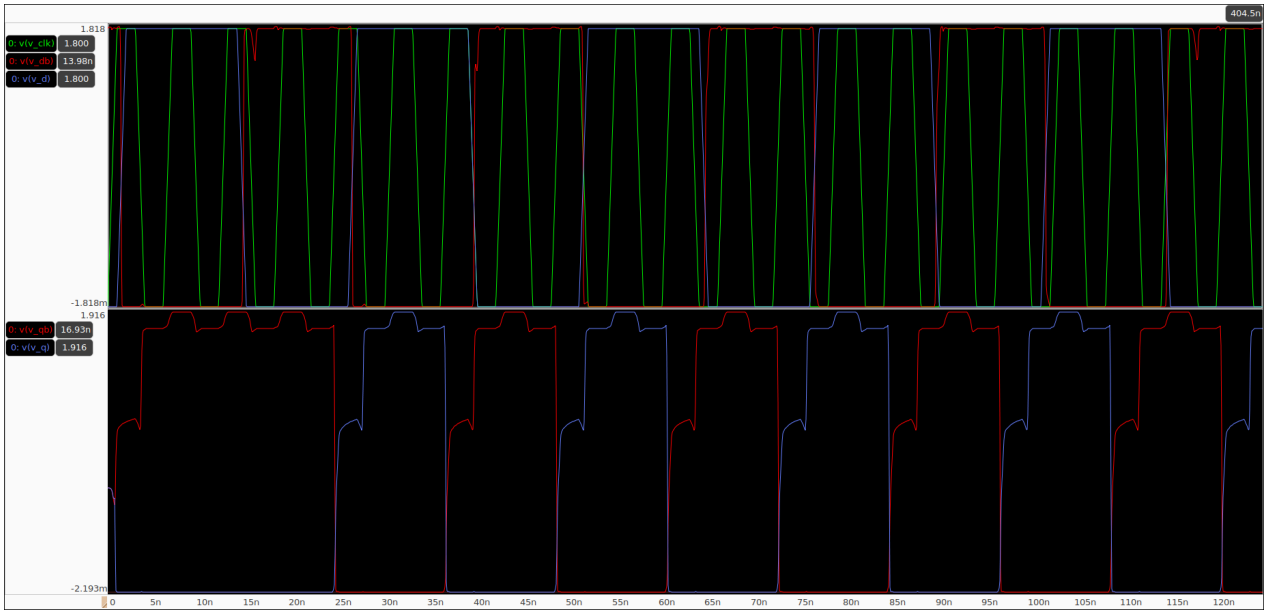

Figure 6: Simulation results of the four-bit shift register in Ngspice.

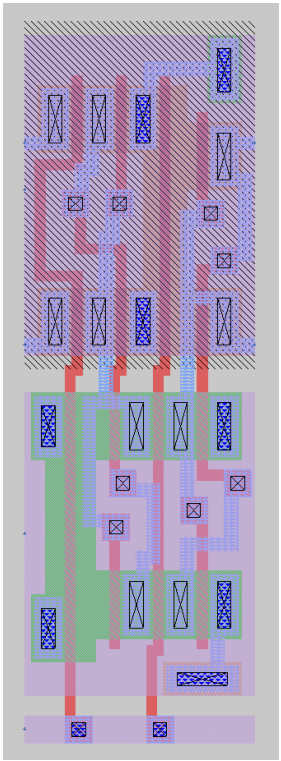

Figure 7: Layout of a CSRL D-flip-flop in Magic.

3 Layout Versus Schematic

The layout versus schematic (LVS) output can be accessed here. The results showed that the netlists matched uniquely.

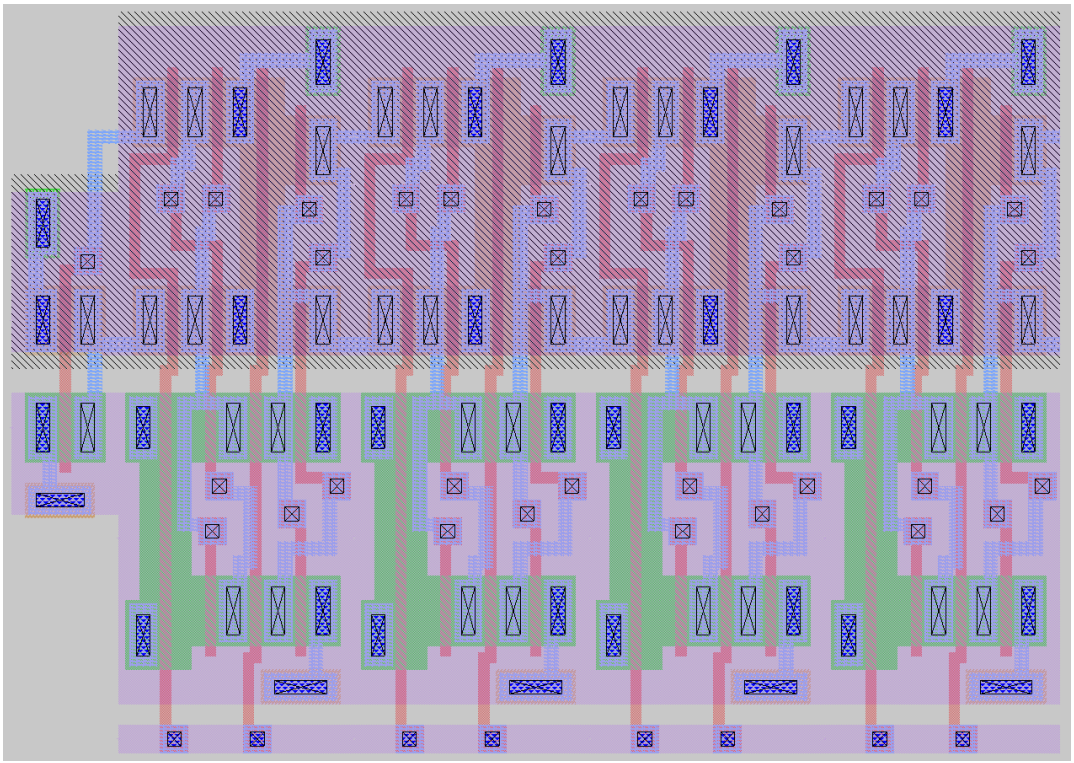

Figure 8: Layout of the four-bit shift register in Magic.

4 Design files

All the design files of MP2 can be accessed here.