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VIA University College

Mandatory Assignment
Table of content

1   1-bit register triggering.

Figure 1, Figure 2, Figure 3 and Figure 4 shows, 1-bit registers. Fill out the table below:

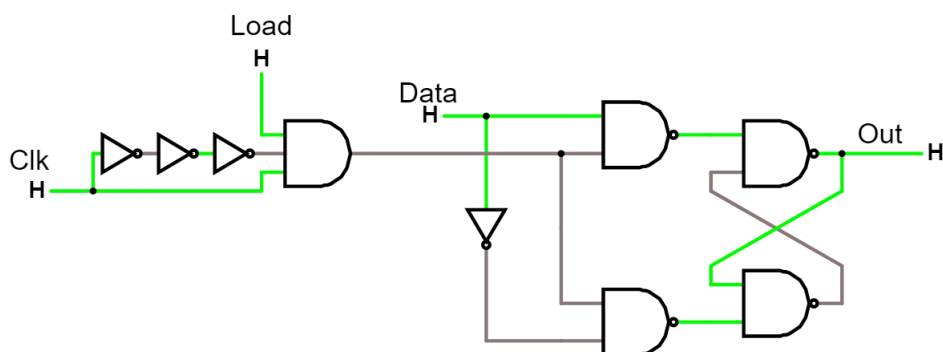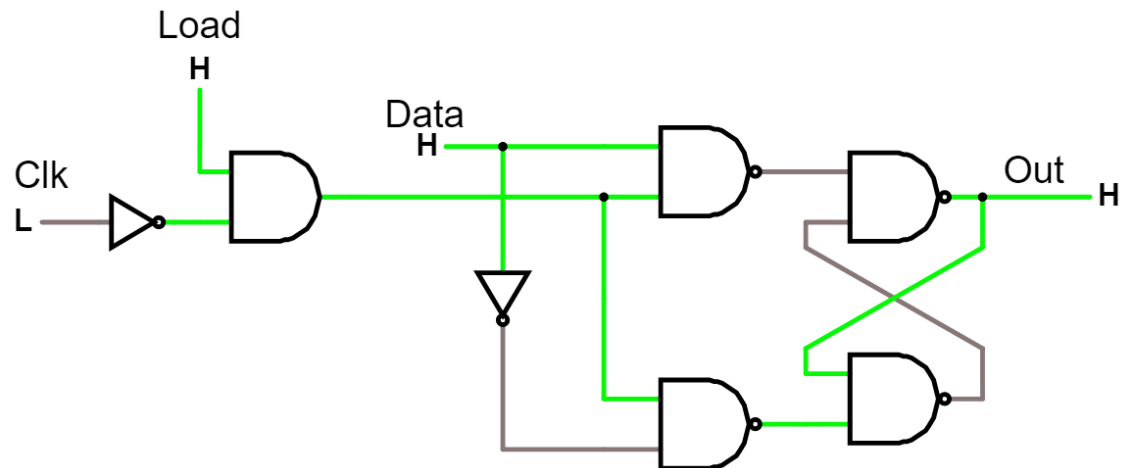| Trigger	
High level	Figure XX
Low level	Figure XX
Rising edge	Figure XX
Falling edge	Figure XX

Figure 1: 1-bit register. *Simulation*
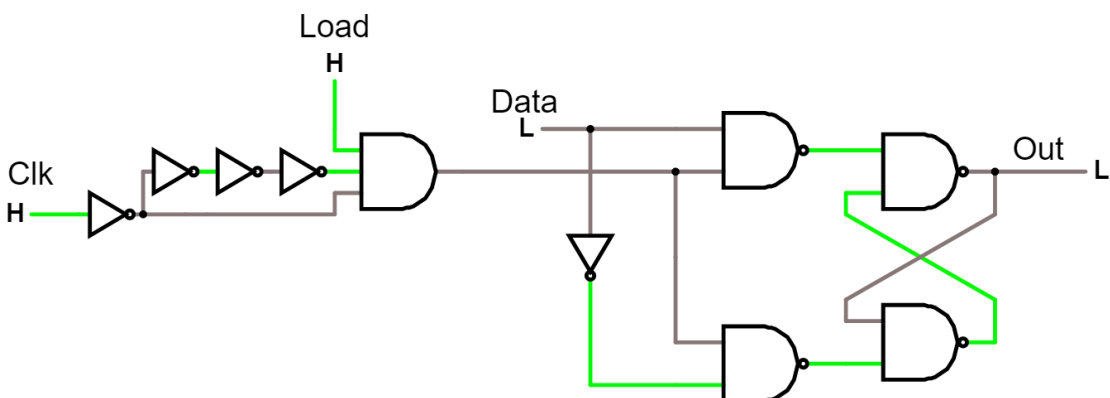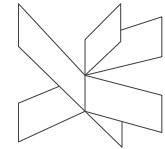

Figure 2: 1-bit register. *Simulation*

Load
H

Clk
L

Data
H

Out
H

Figure 3: 1-bit register. Simulation

Load
H

Clk
L

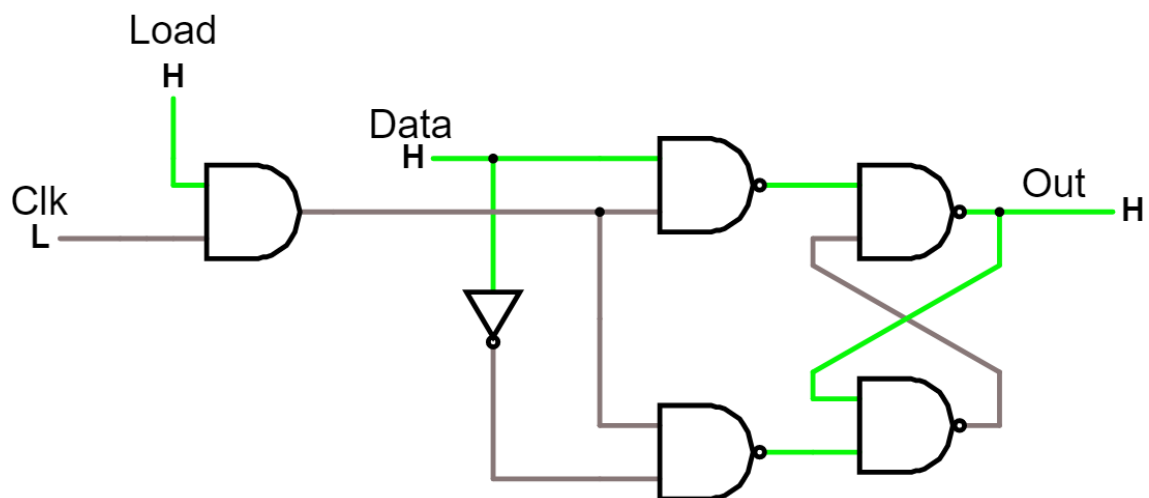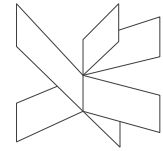Data
H

Out
H

Figure 4: 1-bit register. Simulation

2 Latches

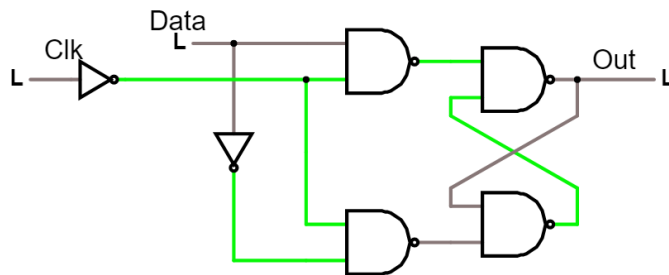## 2.1 How are the latch on Figure 9 triggered?

Figure 5 Simulation
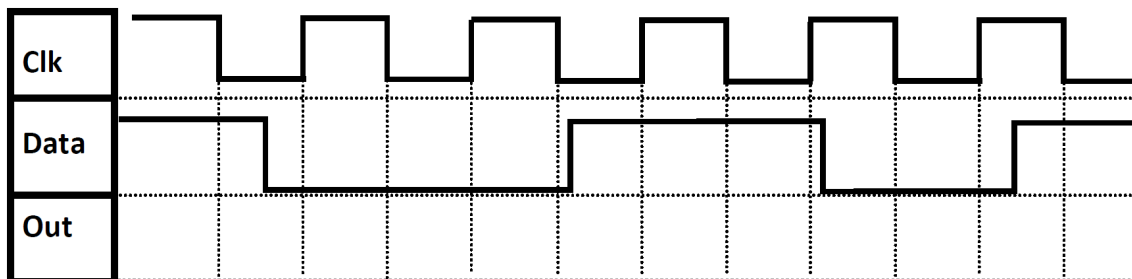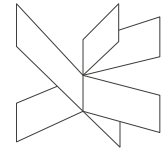
2.1.1 Draw 'Out' on Figure 6

Figure 6

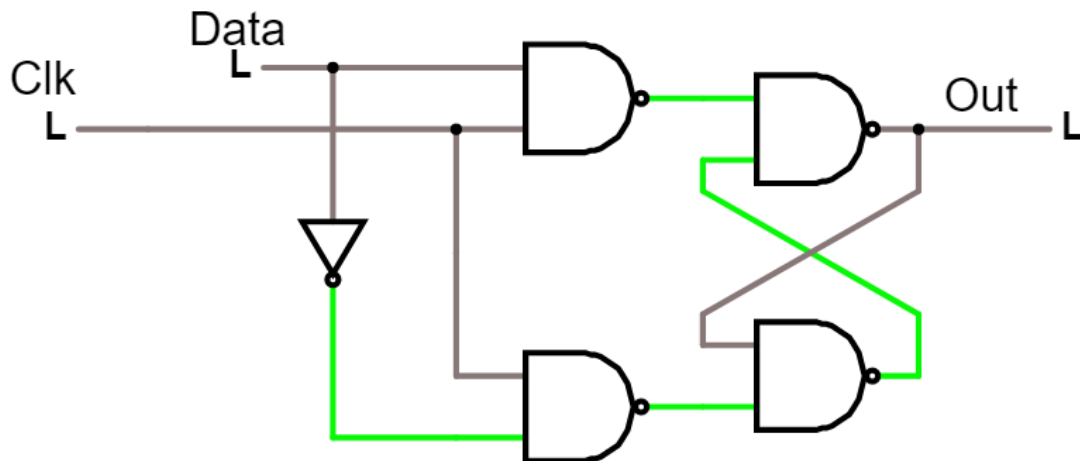## 2.2 How are the latch on Figure 7 triggered?

Figure 7. Simulation

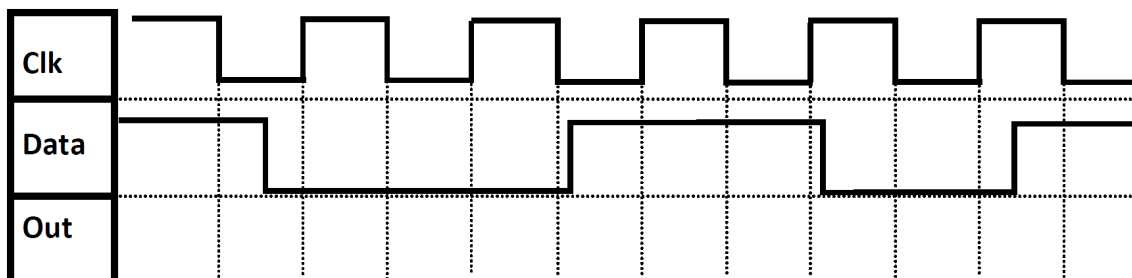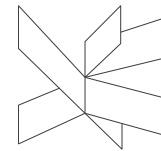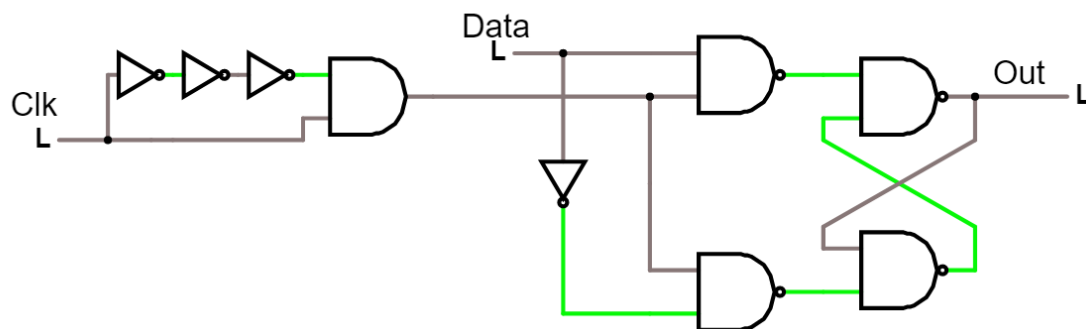### 2.2.1 Draw 'Out' on Figure 8

Figure 8

2.3 How are the latch on Figure 9 triggered?

Figure 9: Simulation

2.3.1 Draw 'Out' on Figure 10,

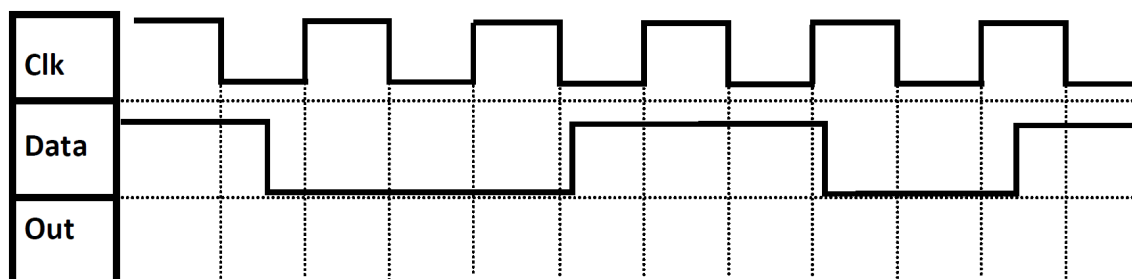| Clk	
Data	
Out	

Figure 10

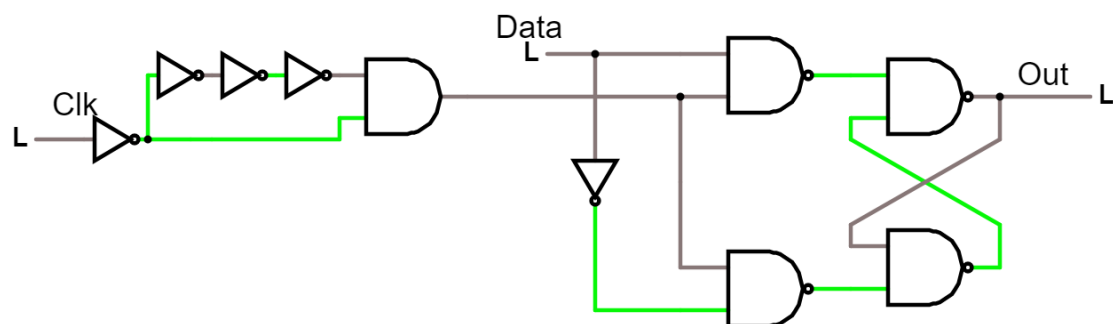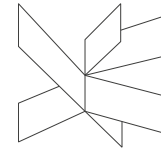## 2.4 How are the latch on Figure 11 triggered?

Figure 11: Simulation
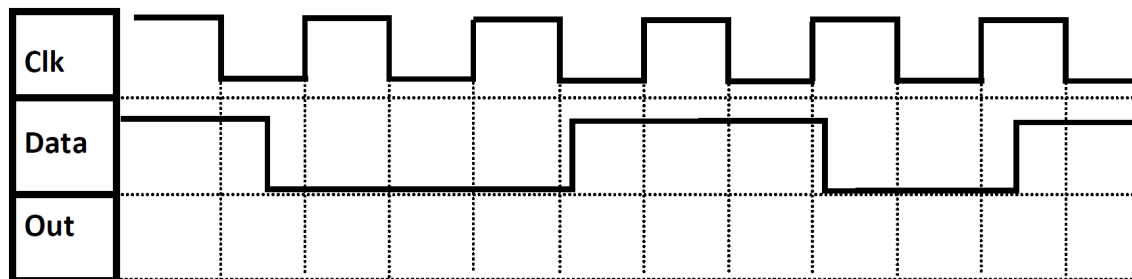
2.4.1 Draw 'Out' on Figure 12.

Figure 12

3 1-bit register

3.1 1-bit register High level triggered

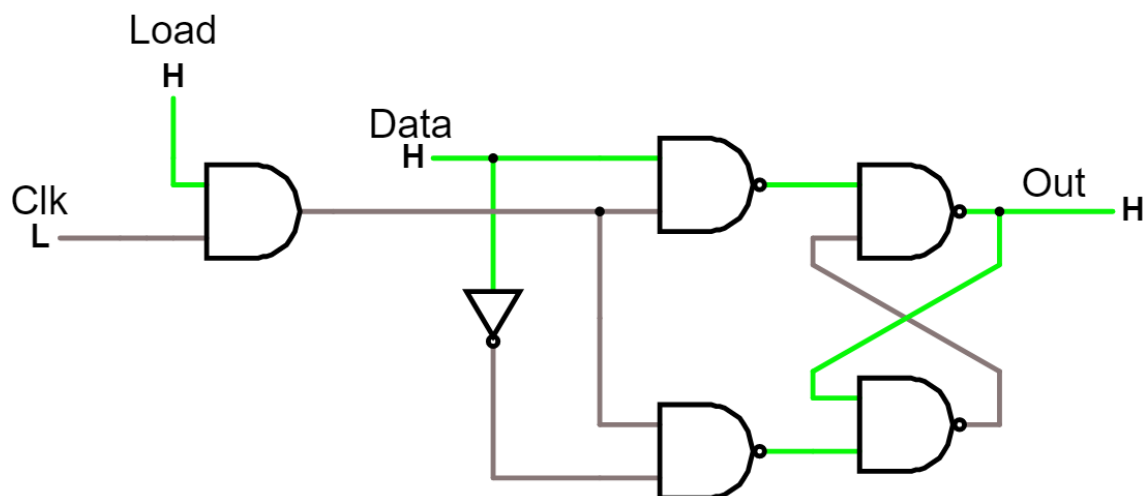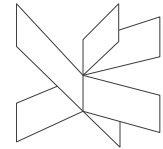A 1-bit register which is High-level triggered can be seen on Figure 13

Figure 13: 1-bit register. Simulation

Computer Architecture and Organization

TASK: Draw 'Out' on Figure 14

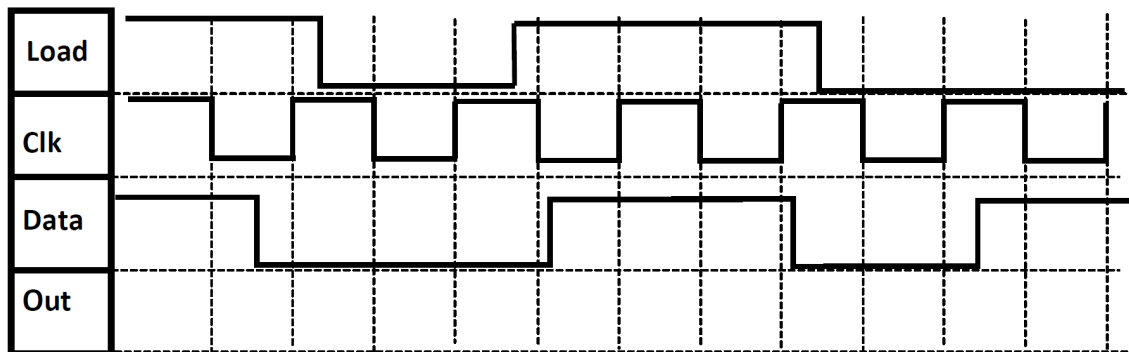*Figure 14*

3.2   1-bit register Low level triggered

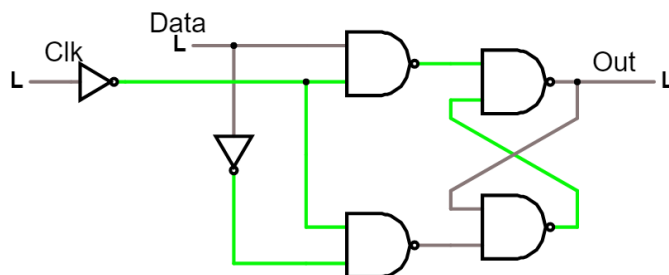A 1-bit register which is low-level triggered can be seen on Figure 15

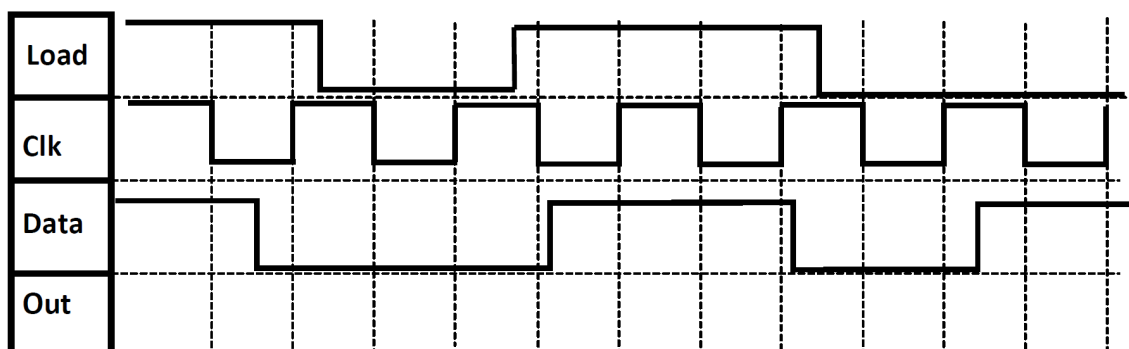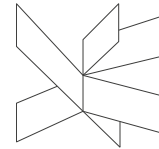*Figure 15 Simulation*

TASK: Draw 'Out' on Figure 16

Figure 16

3.3 1-bit register rising edge triggered

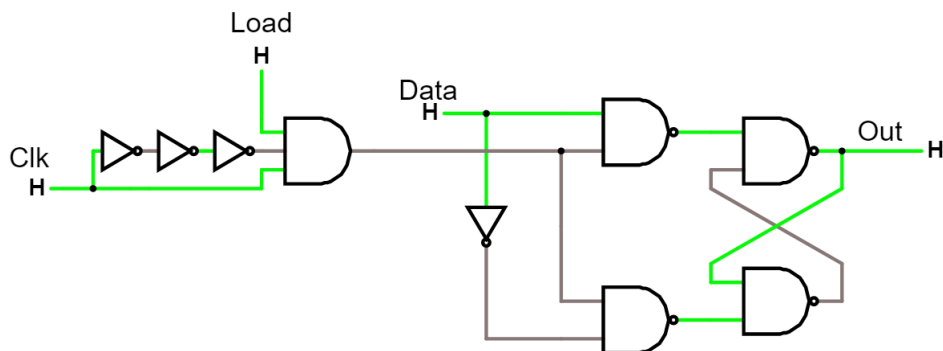A 1-bit register which is rising edge triggered can be seen on Figure 17
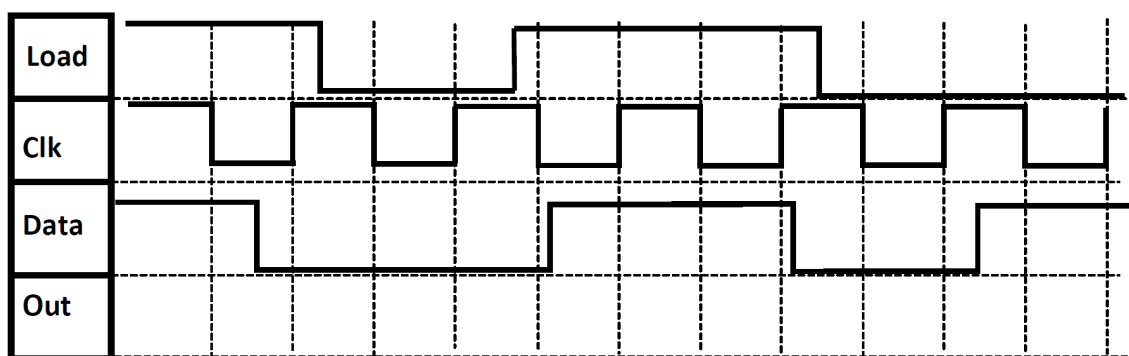

Figure 17: Simulation

TASK: Draw 'Out' on Figure 18

Figure 18

3.4 1-bit register falling edge triggered

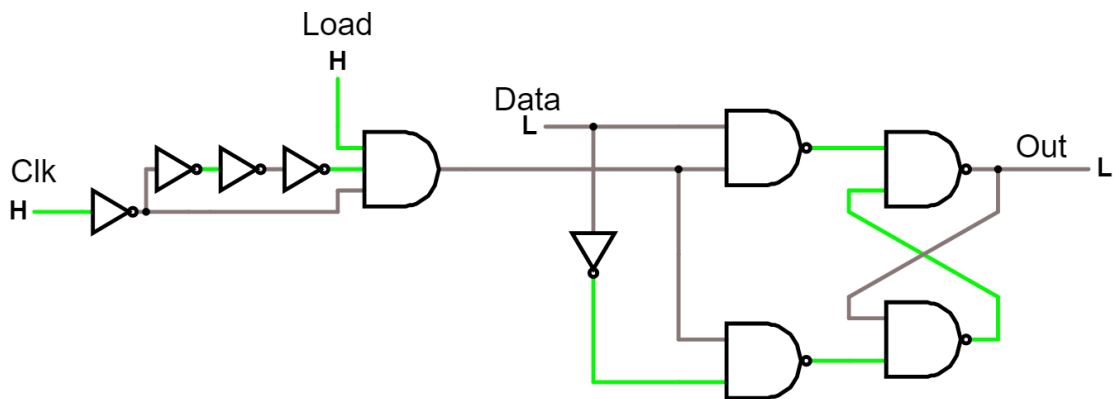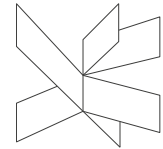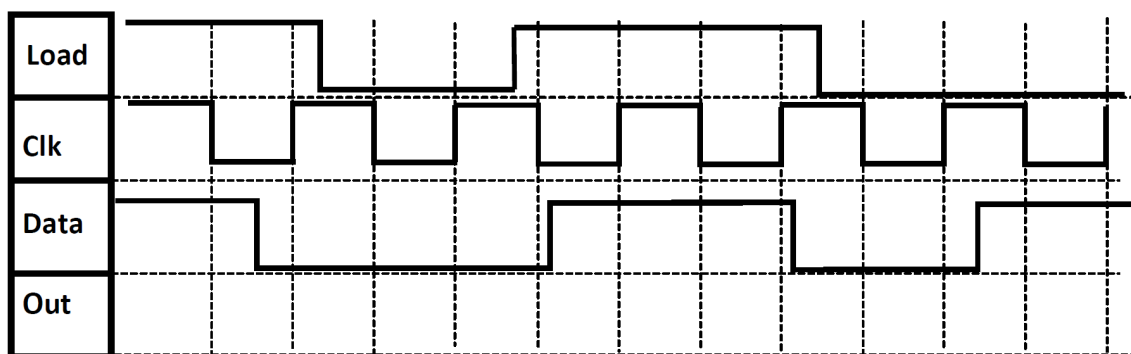A 1-bit register which is falling edge triggered can be seen on Figure 19.

Load
H

Data
L

Clk
H

Out
L

Figure 19: 1-bit register. Simulation

TASK: Draw 'Out' on Figure 20

Load	
Clk	
Data	
Out	

Figure 20