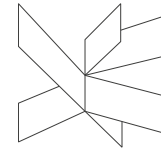


Mandatory Assignment

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1 1-bit register triggering.

Figure 1, Figure 2, Figure 3 and Figure 4 shows, 1-bit registers. Fill out the table below:

Trigger	
High level	Figure XX
Low level	Figure XX
Rising edge	Figure XX
Falling edge	Figure XX

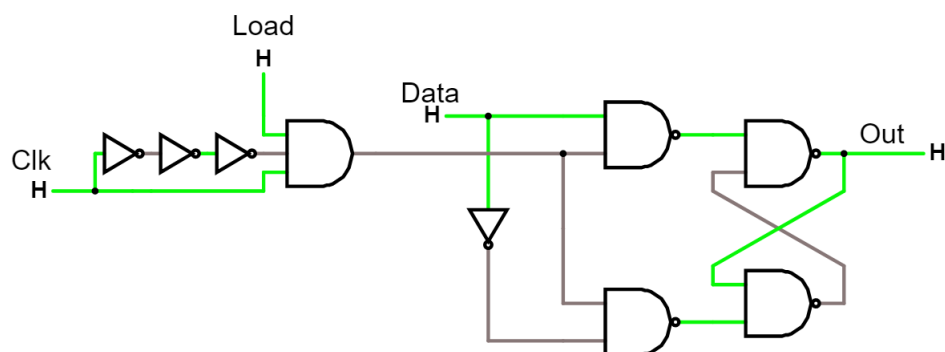


Figure 1: 1-bit register. [Simulation](#)

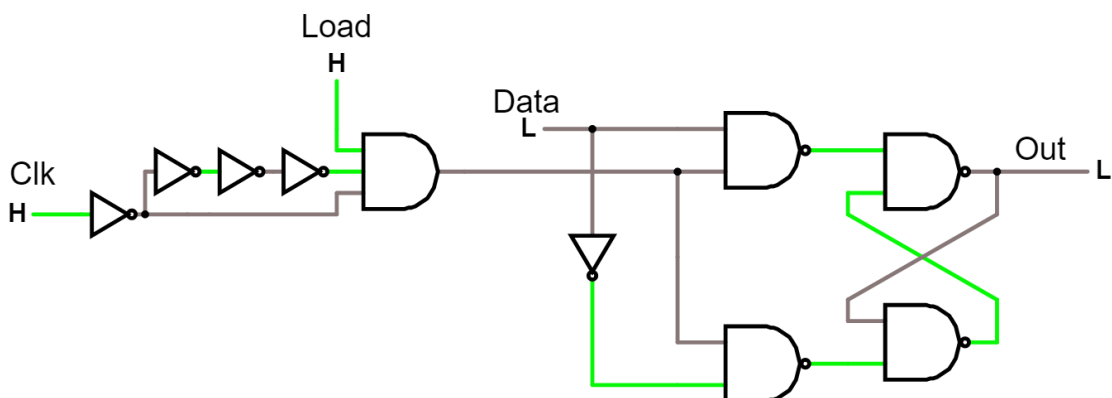


Figure 2: 1-bit register. [Simulation](#)

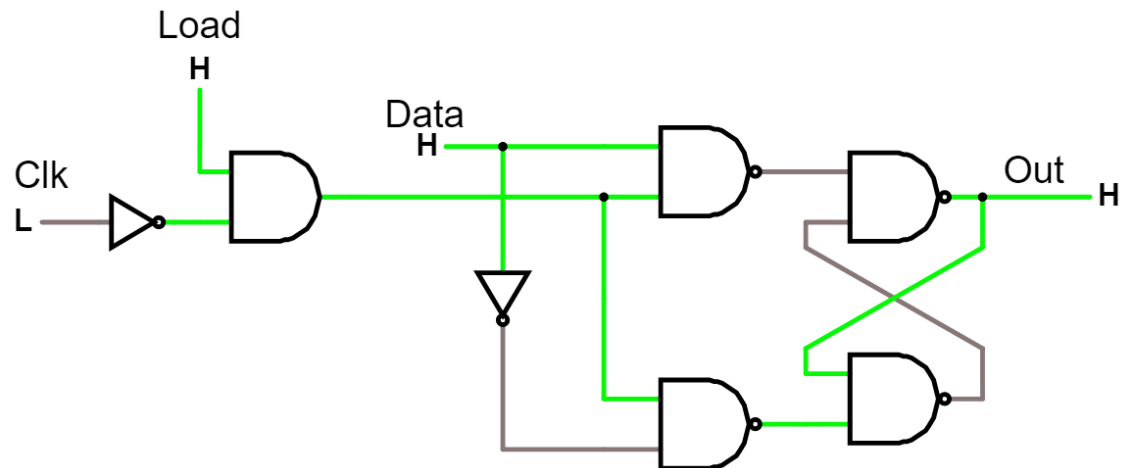
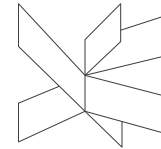


Figure 3: 1-bit register. [Simulation](#)

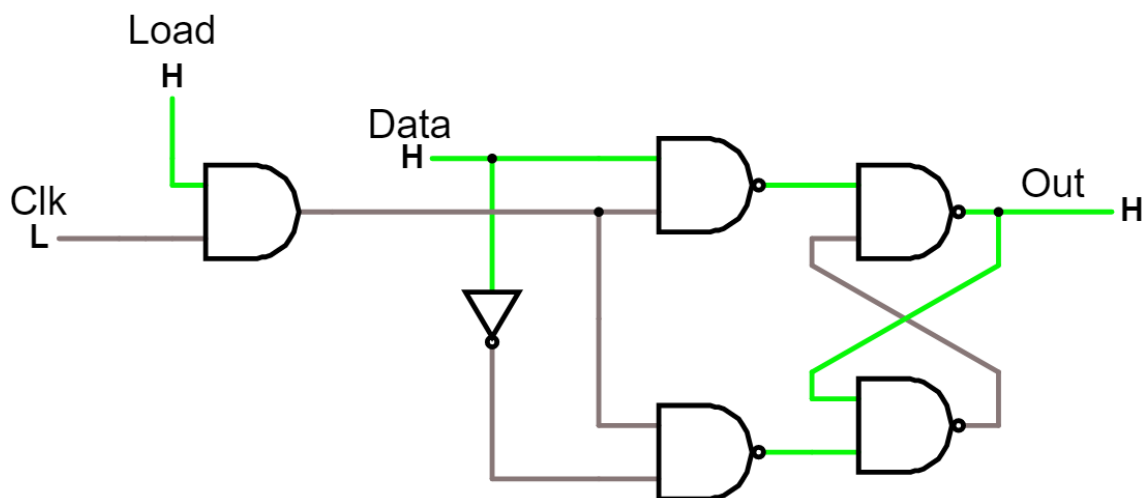
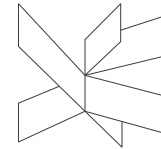


Figure 4: 1-bit register. [Simulation](#)

Solution

Trigger	
High level	Figure 4
Low level	Figure 3
Rising edge	Figure 1
Falling edge	Figure 2



2 Latches

2.1 How are the latch on Figure 9 triggered?

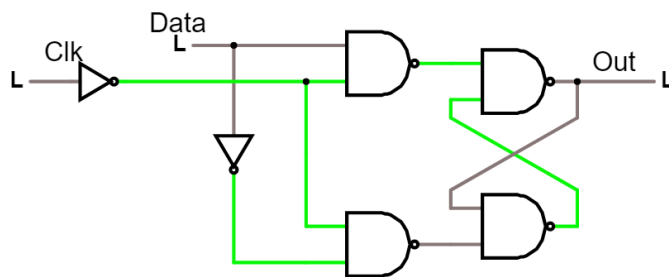


Figure 5 [Simulation](#)

Solution

Low level triggered

2.1.1 Draw 'Out' on Figure 6

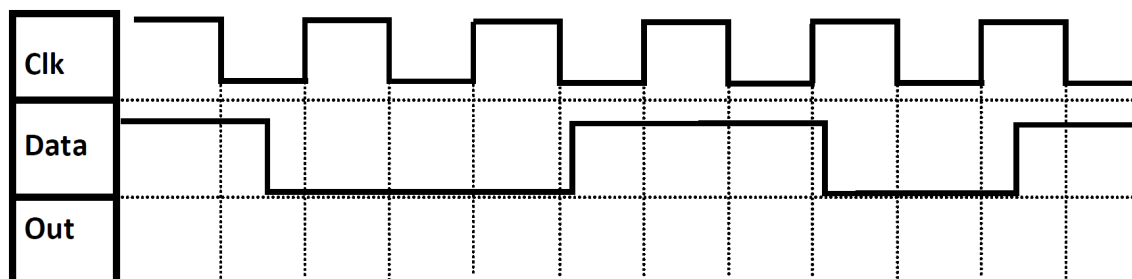
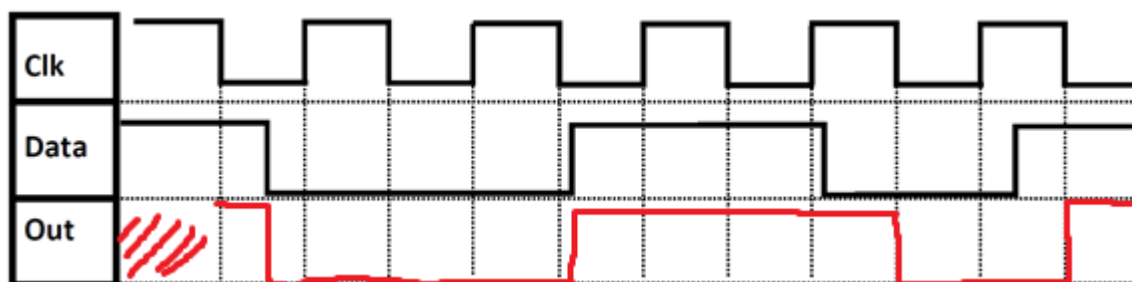
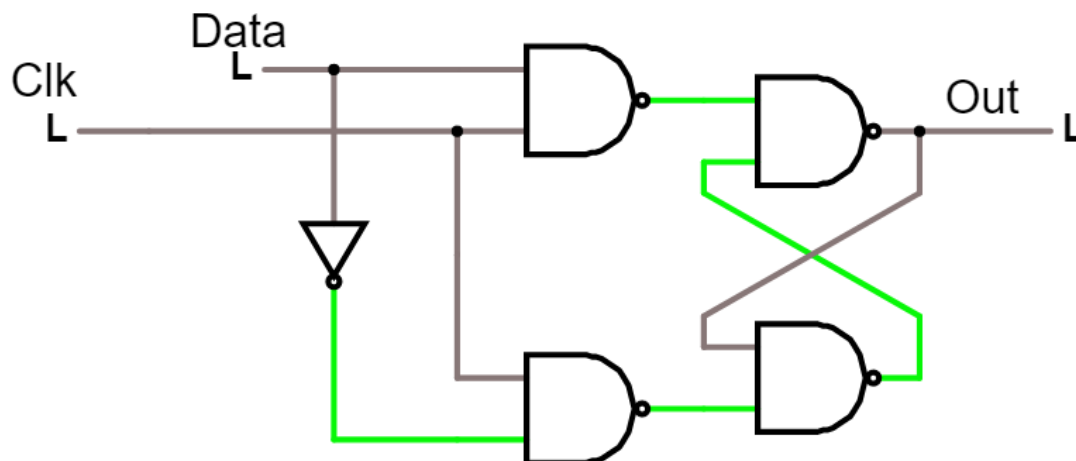


Figure 6

Solution

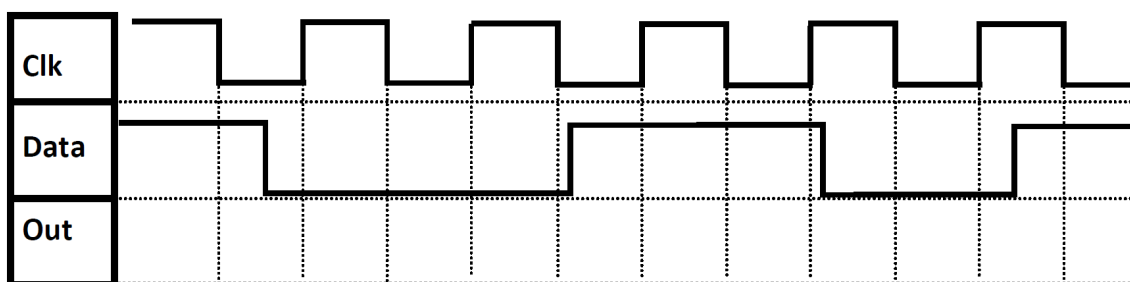




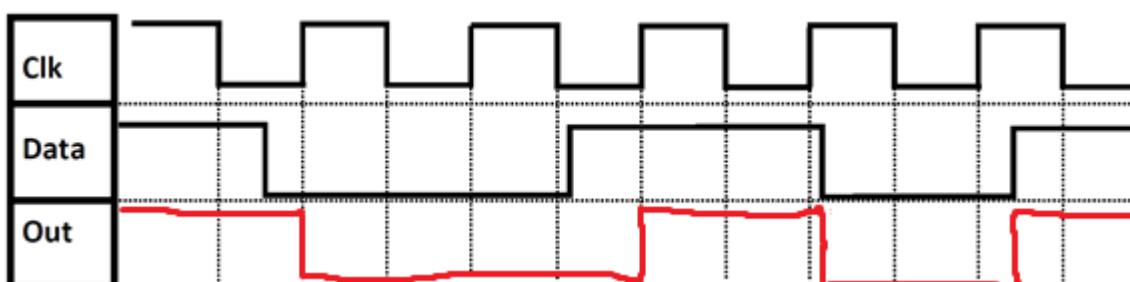
Solution

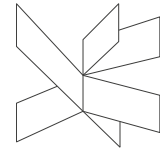
High level triggered

2.2.1 Draw 'Out' on Figure 8



Solution





2.3 How are the latch on Figure 9 triggered?

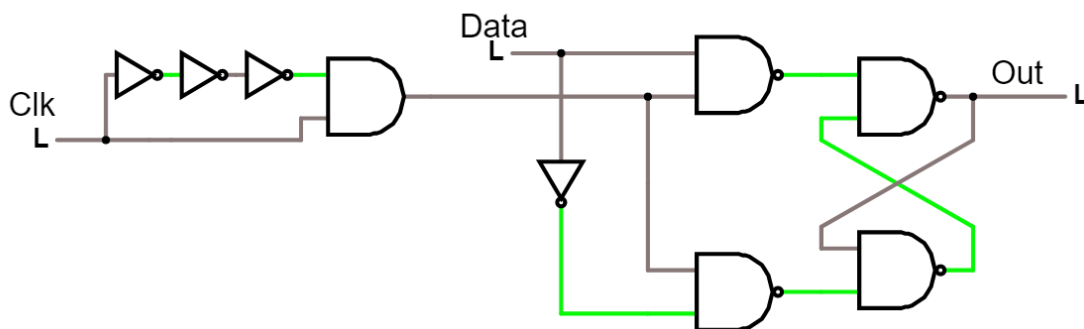


Figure 9: [Simulation](#)

Solution

Rising Edge

2.3.1 Draw 'Out' on Figure 10,

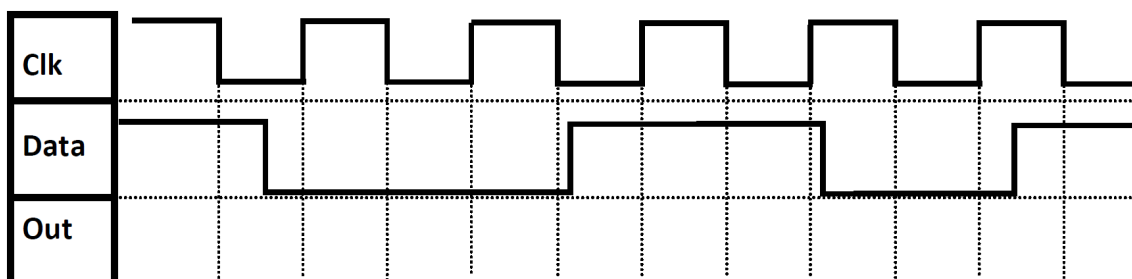
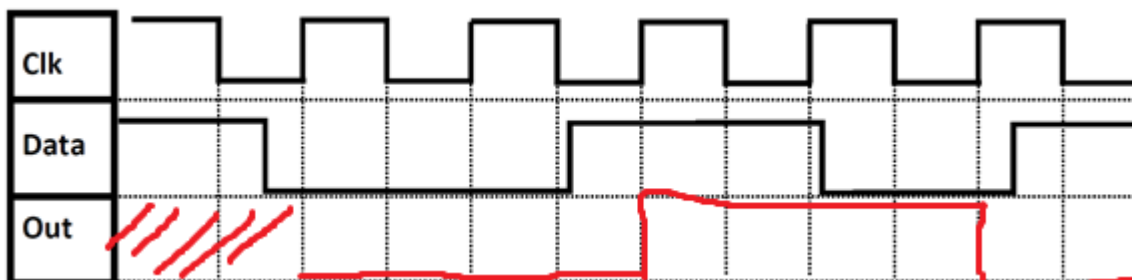
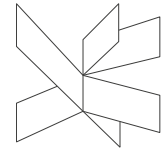


Figure 10

Solution





2.4 How are the latch on Figure 11 triggered?

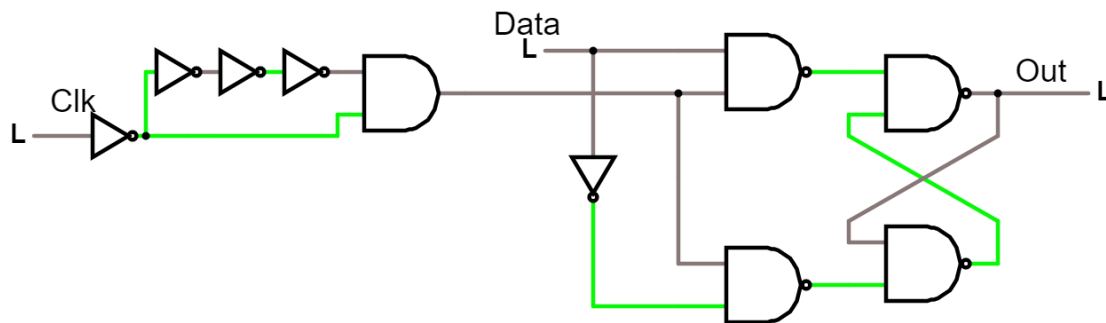


Figure 11: [Simulation](#)

Solution

Falling Edge

2.4.1 Draw 'Out' on Figure 12.

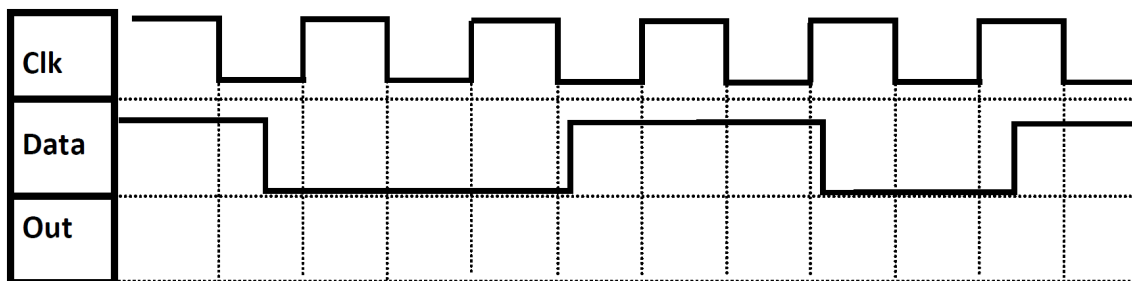
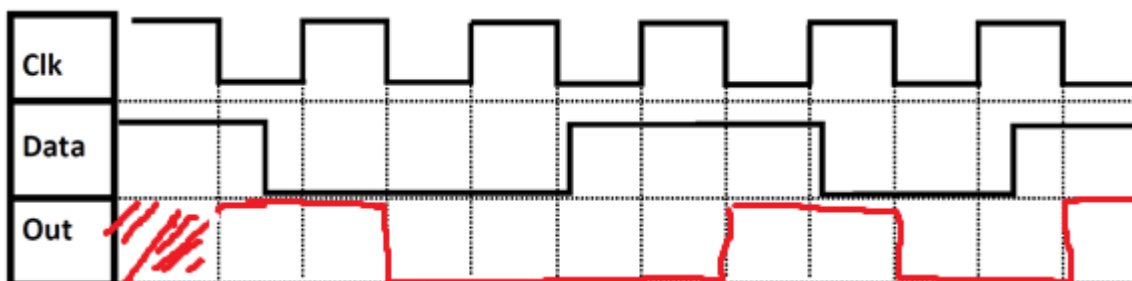
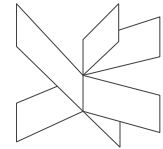


Figure 12

Solution





3 1-bit register

3.1 1-bit register High level triggered

A 1-bit register which is High-level triggered can be seen on Figure 13

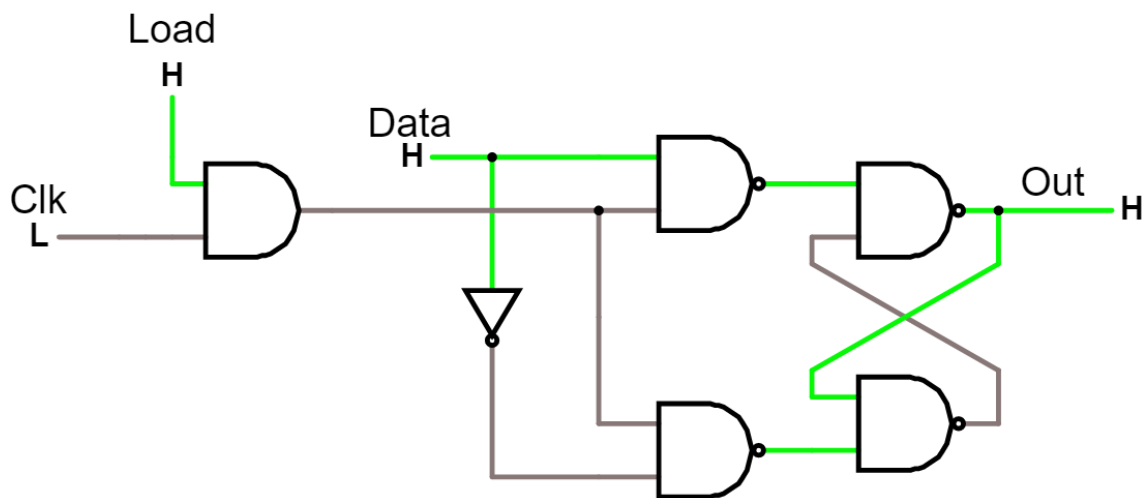


Figure 13: 1-bit register. [Simulation](#)

TASK: Draw 'Out' on Figure 14

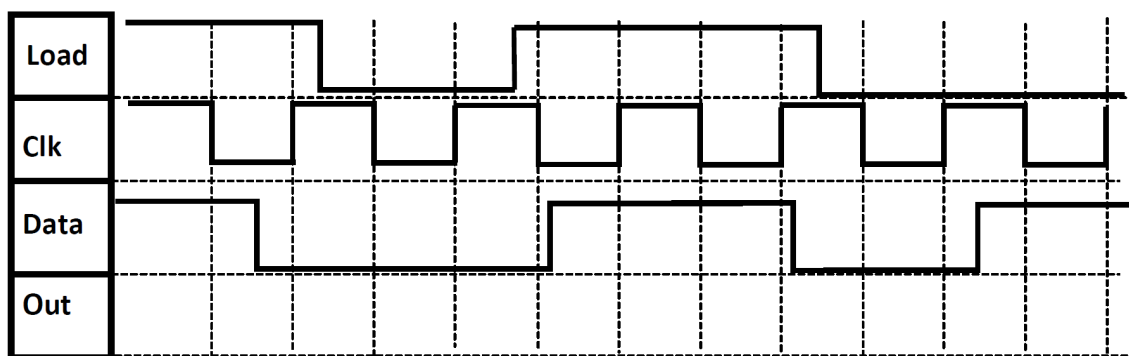
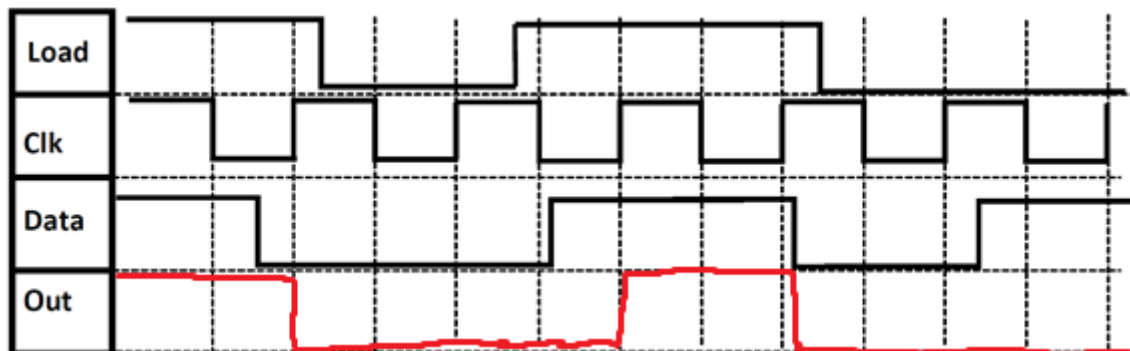
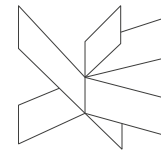


Figure 14

SOLUTION



3.2 1-bit register Low level triggered

A 1-bit register which is low-level triggered can be seen on Figure 15

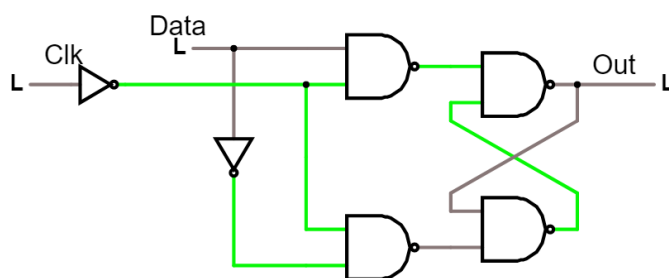


Figure 15 [Simulation](#)

TASK: Draw 'Out' on Figure 16

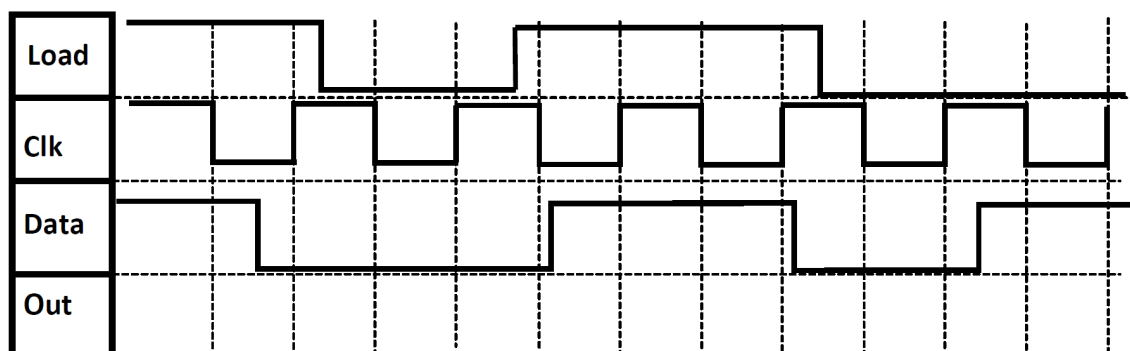
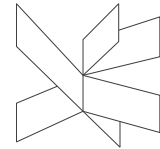


Figure 16



SOLUTION



3.3 1-bit register rising edge triggered

A 1-bit register which is rising edge triggered can be seen on Figure 17

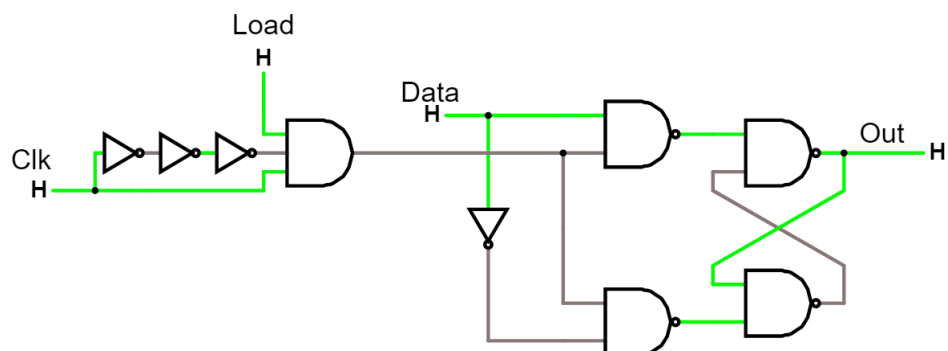
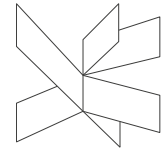


Figure 17: [Simulation](#)



Load										
Clk										
Data										
Out										

Figure 18

Signal	1	2	3	4	5	6	7	8	9	10
Load	1	1	0	0	1	1	1	0	0	0
Clk	0	1	0	1	0	1	0	1	0	1
Data	1	0	1	1	0	1	0	1	0	1
Out	1	1	0	0	1	1	1	1	0	0

A 1-bit register which is falling edge triggered can be seen on Figure 19.

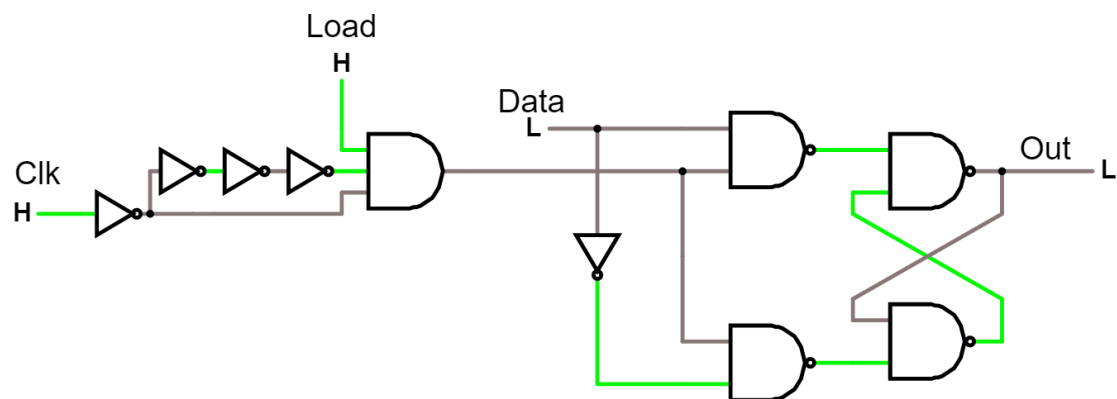
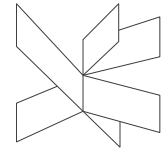


Figure 19: 1-bit register. [Simulation](#)



TASK: Draw 'Out' on Figure 20

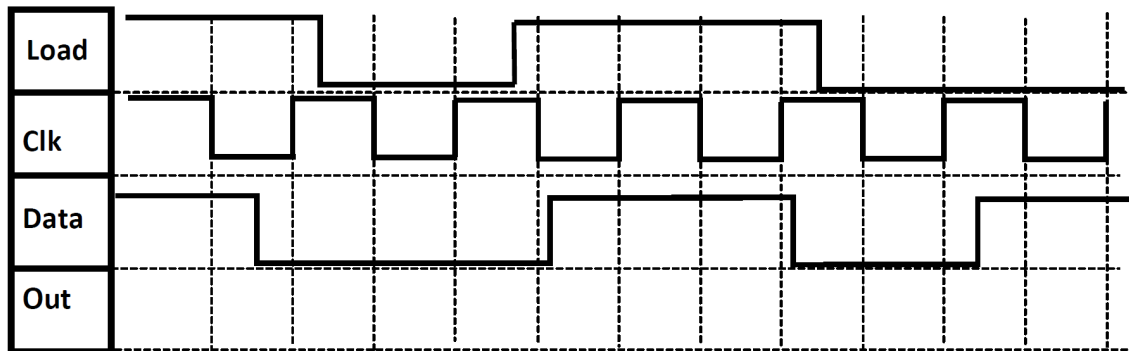


Figure 20

SOLUTION

