Introduction to Embedded System Design using Zynq

Zynq
Vivado 2015.2 Version

Outline

- The Zynq Architecture
- Embedded System Development with Vivado

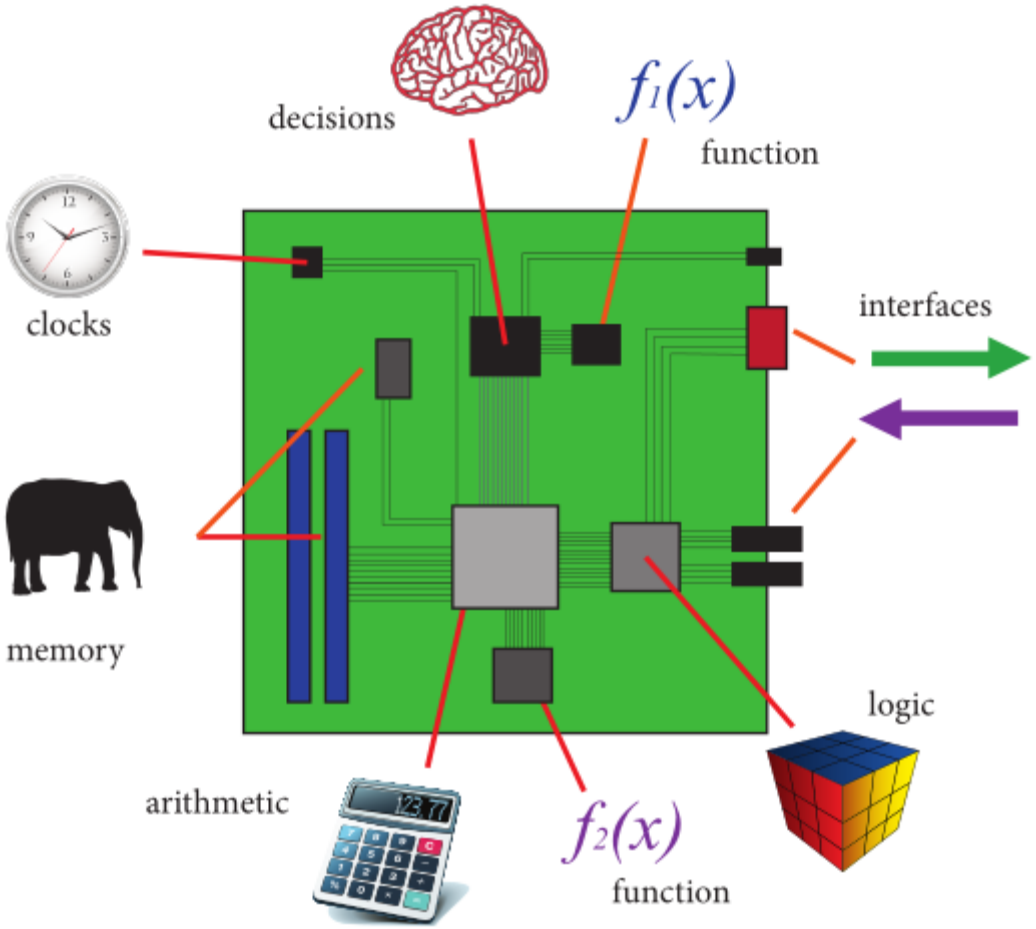
Introducing Zynq

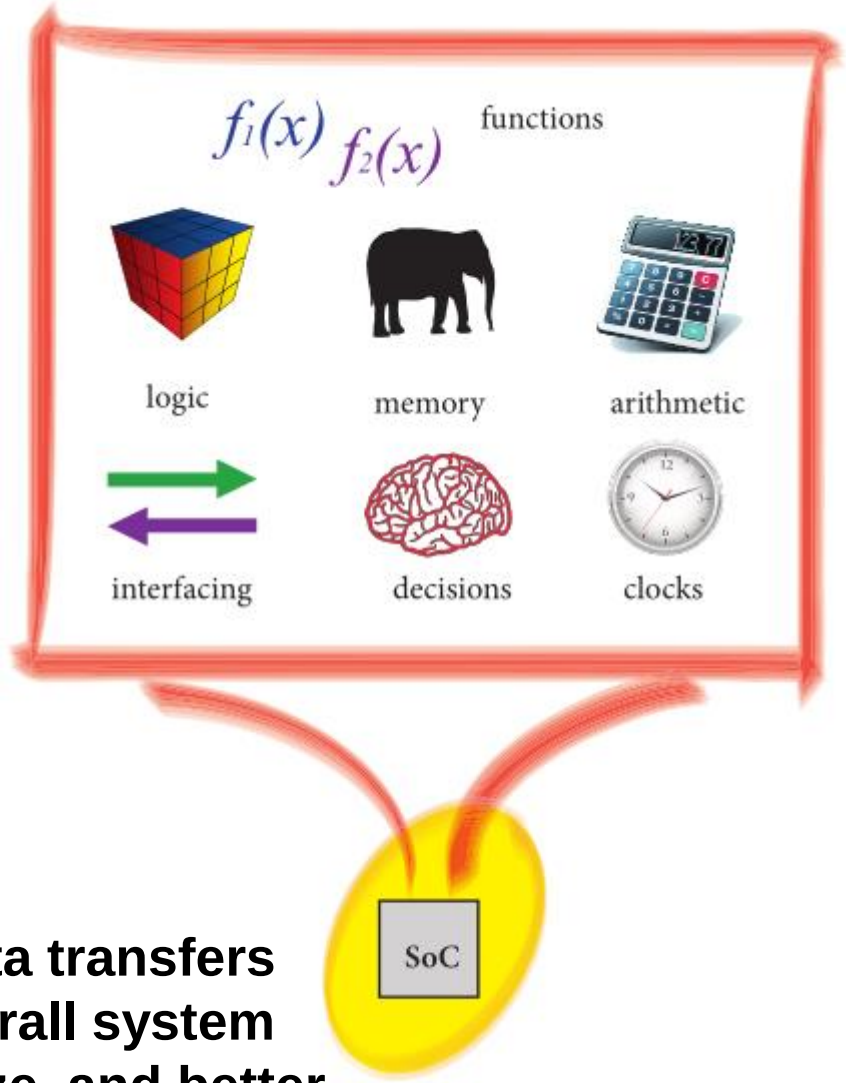
- Xilinx's new generation of All-Programmable System-on-Chip (SoC)
- a (processing) element that can be applied to anything.
- Zynq devices are intended to be flexible and form a compelling platform for a wide variety of applications, just as the metal zinc can be mixed with various other metals to form alloys with differing desirable properties.

Definition of Zynq

- It combines a dual-core ARM Cortex-A9 processor with traditional FPGA.
- The ARM Cortex-A9 is an application grade processor, capable of running full operating systems such as Linux.
- The programmable logic is based on Xilinx 7-series FPGA architecture, which is completed by industry standard AXI interfaces, which provide high bandwidth, low latency connections between the two parts of the device.
- The processor and logic can each be used for what they do best, without the overhead of interfacing between two physically separate devices.
- Benefits arising from simplifying the system to a single chip include reductions in physical size and overall cost.

Comparison of System-on-a-Board and System-on-Chip





SoC is lower cost, enables faster and more secure data transfers between the various system elements, has higher overall system speed, lower power consumption, smaller physical size, and better reliability.

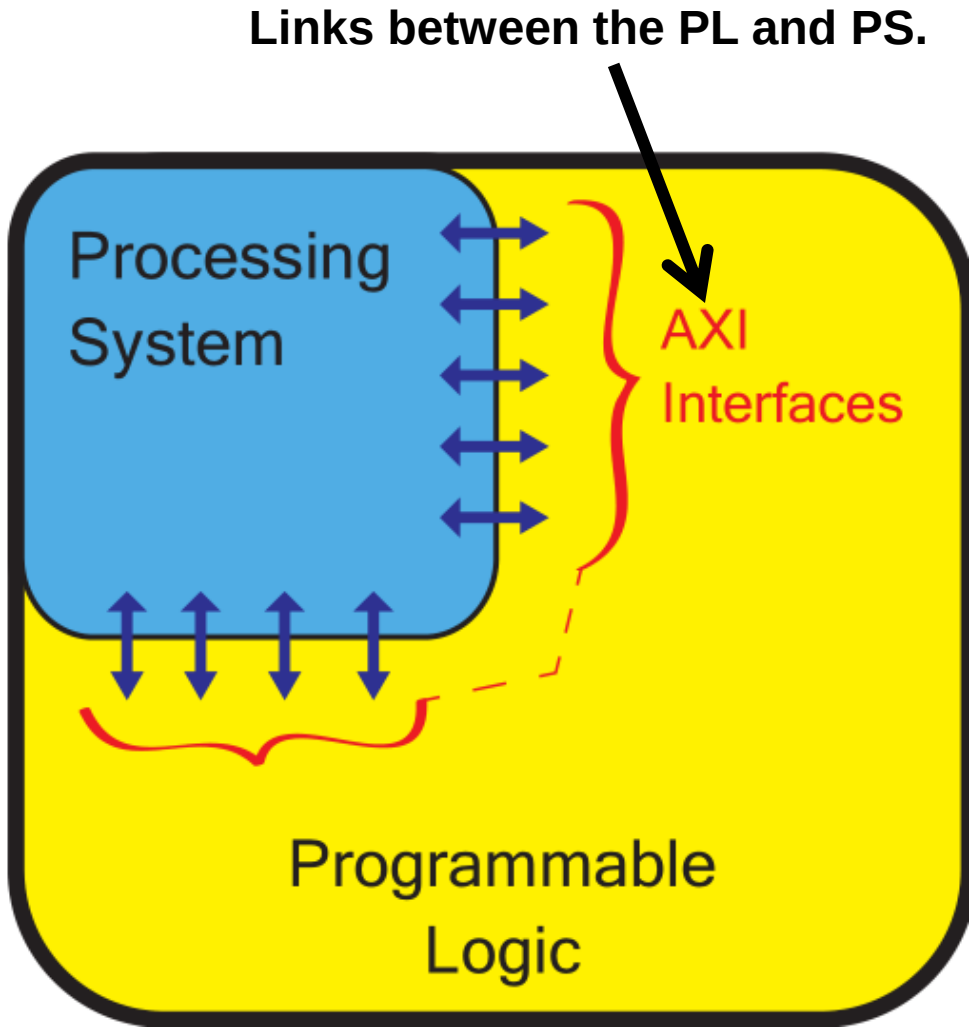
A simplified model of the Zynq architecture – an 'All-Programmable SoC' (APSoC)

Comprises two main parts:

- **A Processing System (PS) formed around a dual-core ARM Cortex-A9 processor, and**
- **Programmable Logic (PL), which is equivalent to that of an FPGA.**

The overall functionality can be appropriately partitioned between hardware and software:

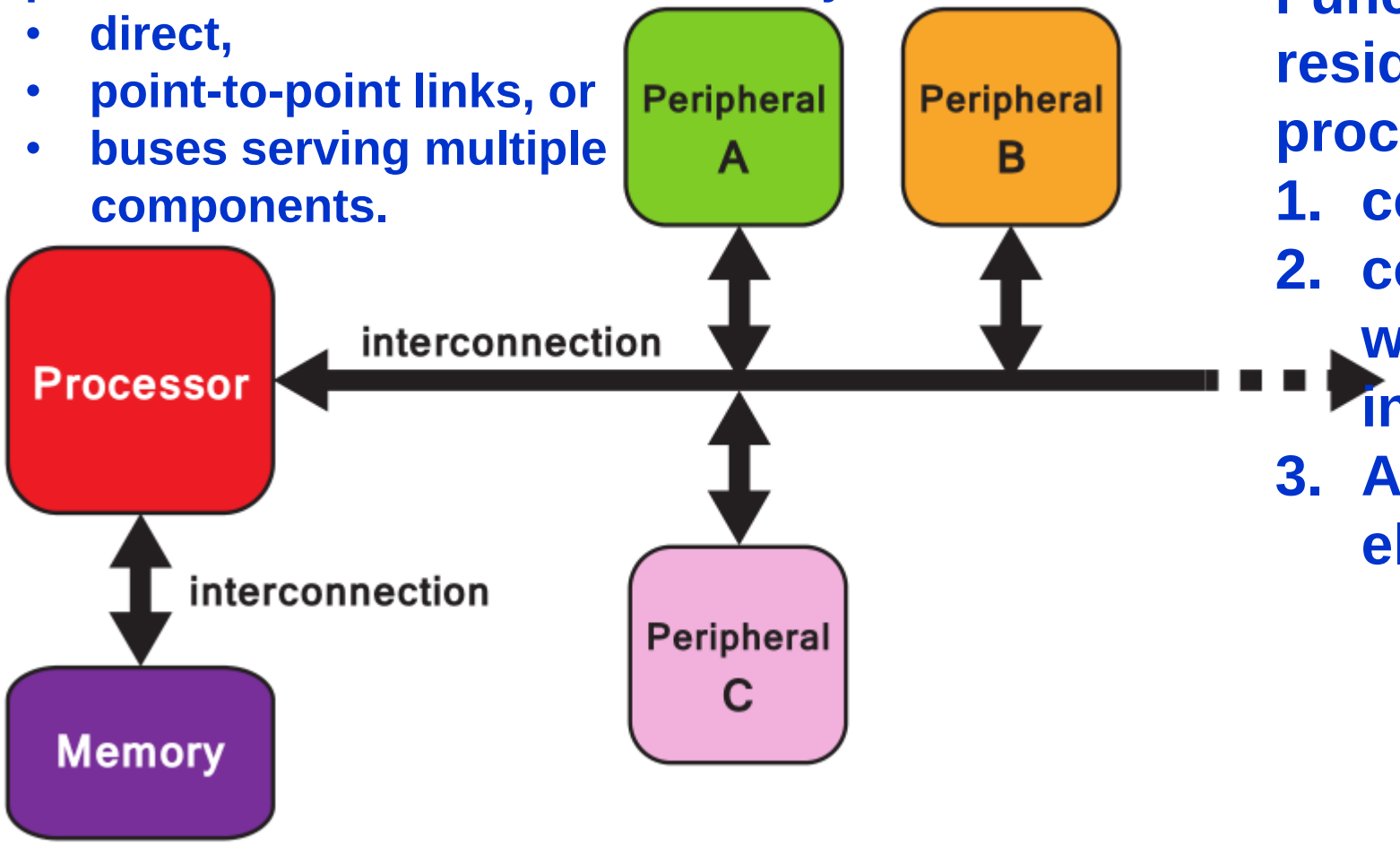
- **PL: implementing high-speed logic, arithmetic and data flow subsystems,**
- **PS: supports software routines and/or operating systems**



The hardware system architecture of an embedded SoC (simplified)

Communication between system elements takes place via interconnections in the style of

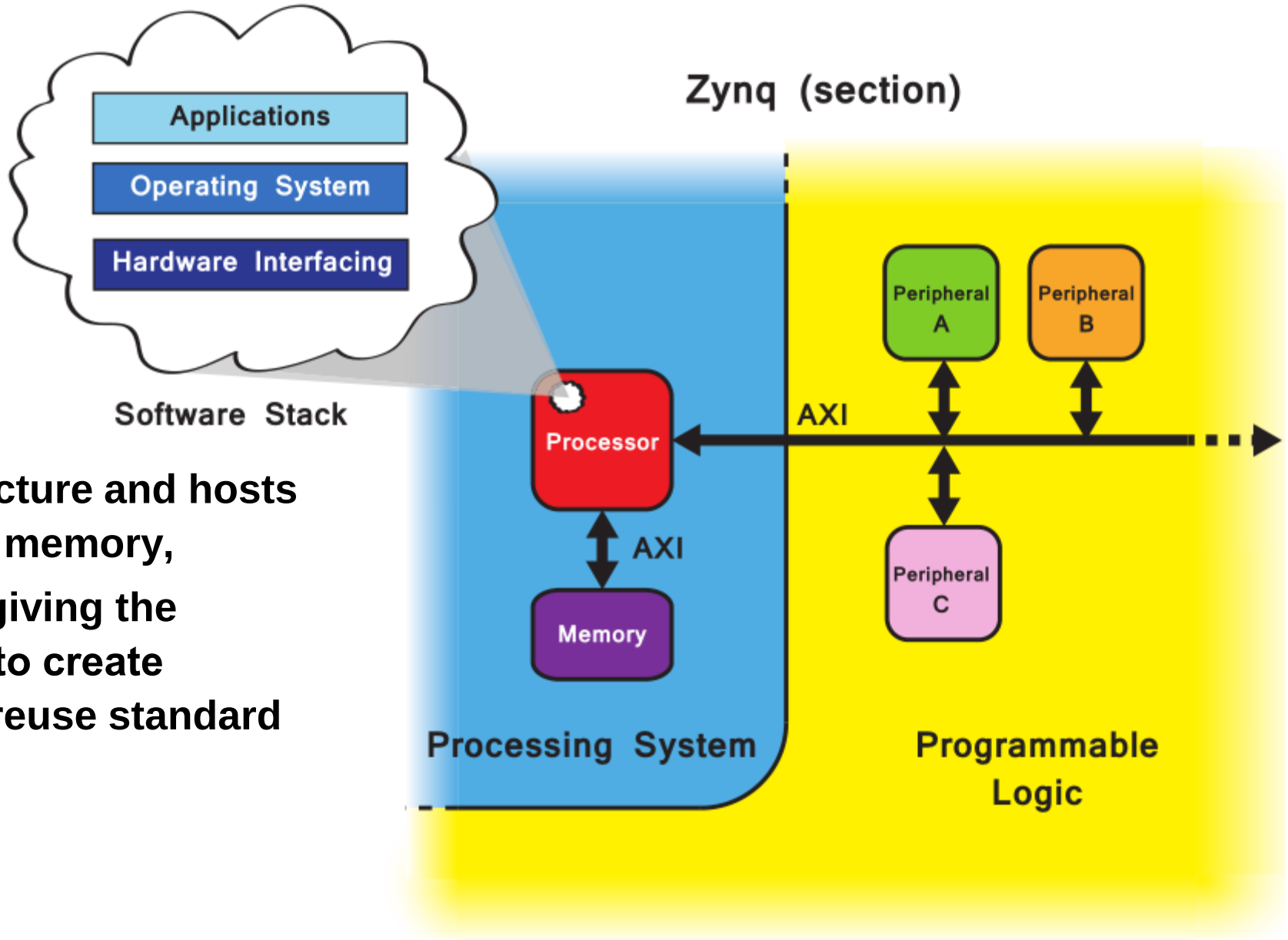
- **direct,**
- **point-to-point links, or**
- **buses serving multiple components.**



Peripherals:
Functional components residing away from the processor

1. **coprocessors**
2. **cores for interacting with external interfaces,**
3. **Additional memory elements.**

Relationship of the software system & hardware system in Zynq architecture

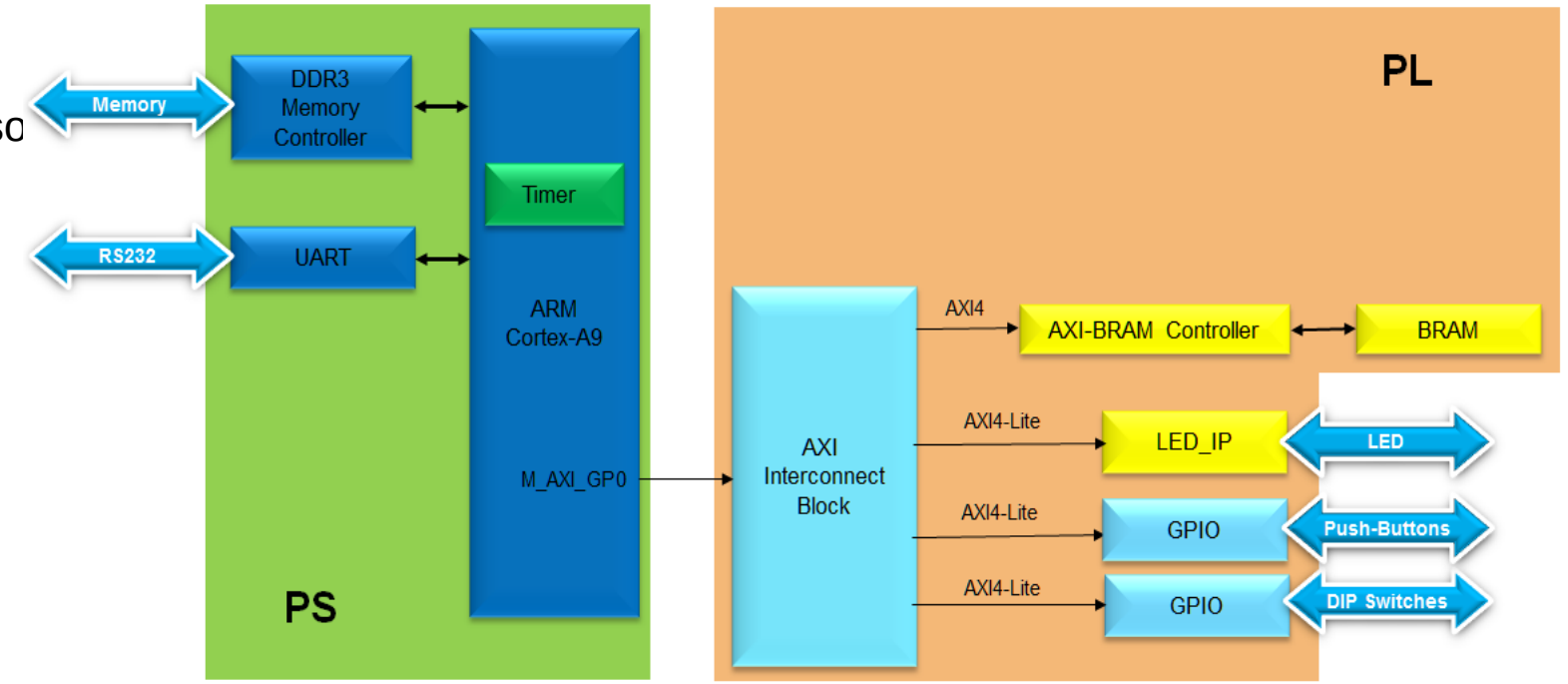


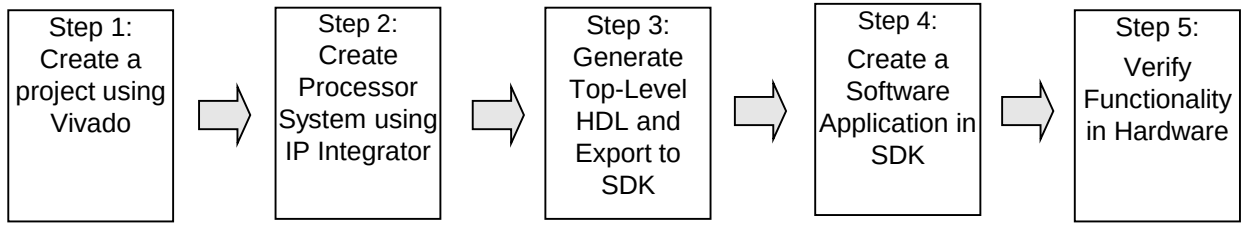
- The PS has a fixed architecture and hosts the processor and system memory,
- PL is completely flexible, giving the designer a ‘blank canvas’ to create custom peripherals, or to reuse standard ones.

Embedded Design Architecture in Zynq

Embedded design with Zynq is based on:

- Processor and peripherals
  - Dual ARM® Cortex™ -A9 processo Zynq-7000 AP SoC
  - AXI interconnect
  - AXI component peripherals
  - Reset, clocking, debug ports
- Software platform for processing system
  - Bare Metal Applications or OS's (e.g. Linux, FreeRTOS)
  - C language support
  - Processor services
  - C drivers for hardware
- User application
  - Interrupt service routines (optional)



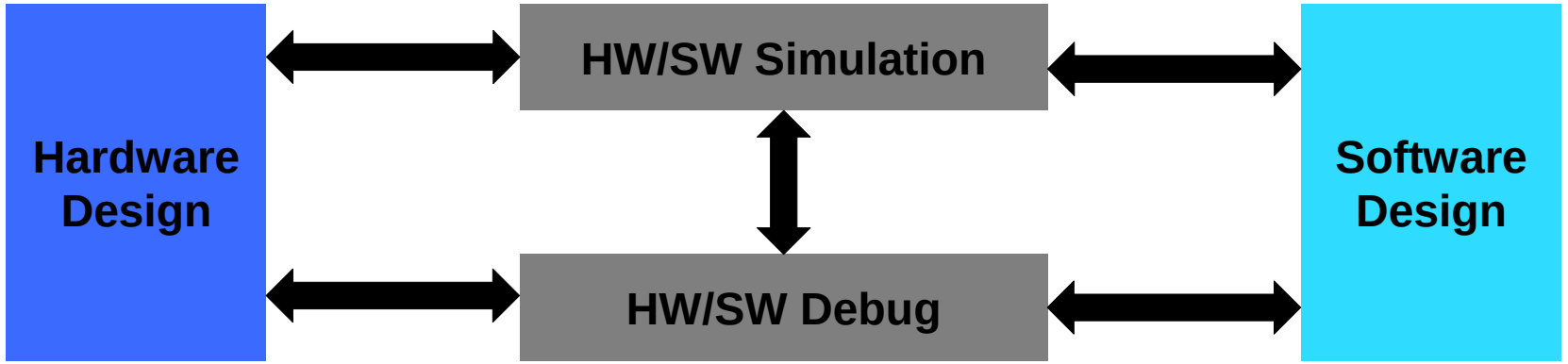


Vivado

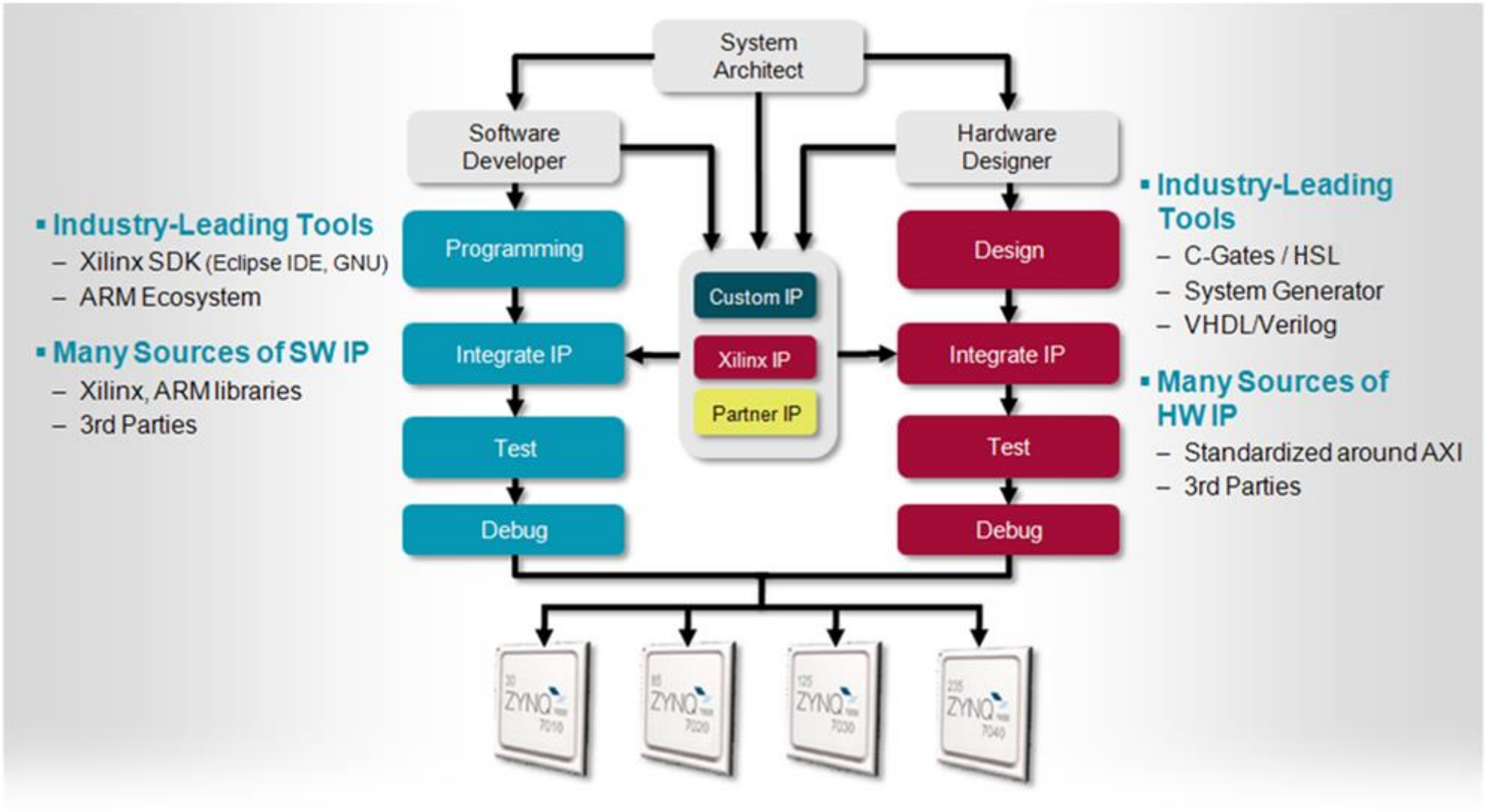
- **What are Vivado, IP Integrator and SDK?**
  - Vivado is the tool suite for Xilinx FPGA design and includes capability for embedded system design
    - IP Integrator, is part of Vivado and allows system level design of the hardware part of an Embedded system
      - Integrated into Vivado
    - Vivado includes all the tools, IP, and documentation that are required for designing systems with the Zynq-7000 AP SoC hard core and/or Xilinx MicroBlaze soft core processor
    - Vivado + IPI replaces ISE/EDK
  - SDK is an Eclipse-based software design environment
    - Enables the integration of hardware and software components
    - Links from Vivado
- **Vivado is the overall project manager and is used for developing non-embedded hardware and instantiating embedded systems**
  - Vivado/IP Integrator flow is recommended for developing Zynq embedded systems

Vivado Components

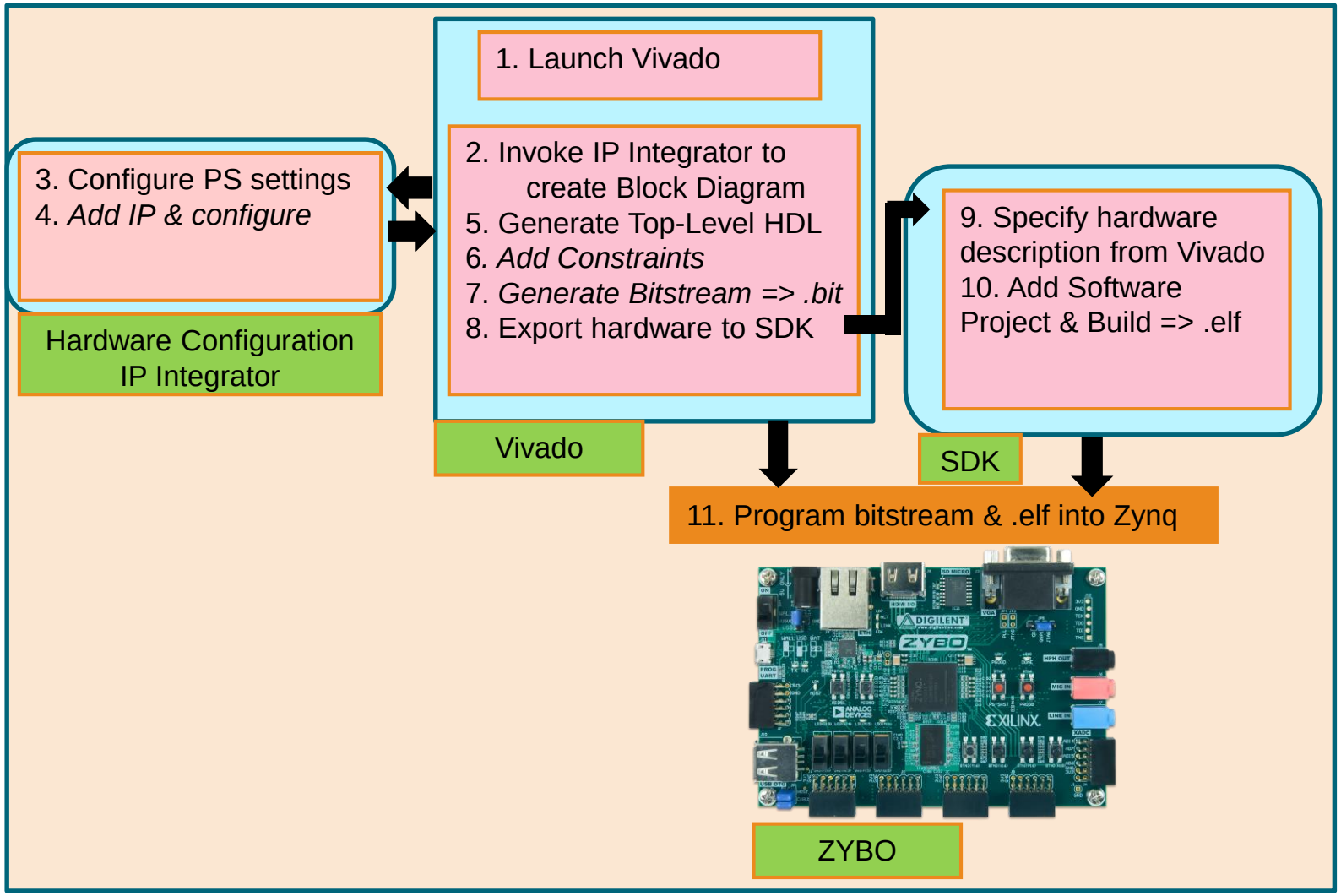
- **Vivado/IP Integrator**
  - Design environment for configuration of PS, and hardware design for PL
  - Hardware Platform (xml)
  - Platform, software, and peripheral simulation
  - Vivado logic analyzer integration
- **Software Development Kit (SDK)**
  - Project workspace
  - Hardware platform definition
  - Board Support Package (BSP)
  - Software application
  - Software debugging



Embedded System Design Flow for Zynq-7000 AP SoC

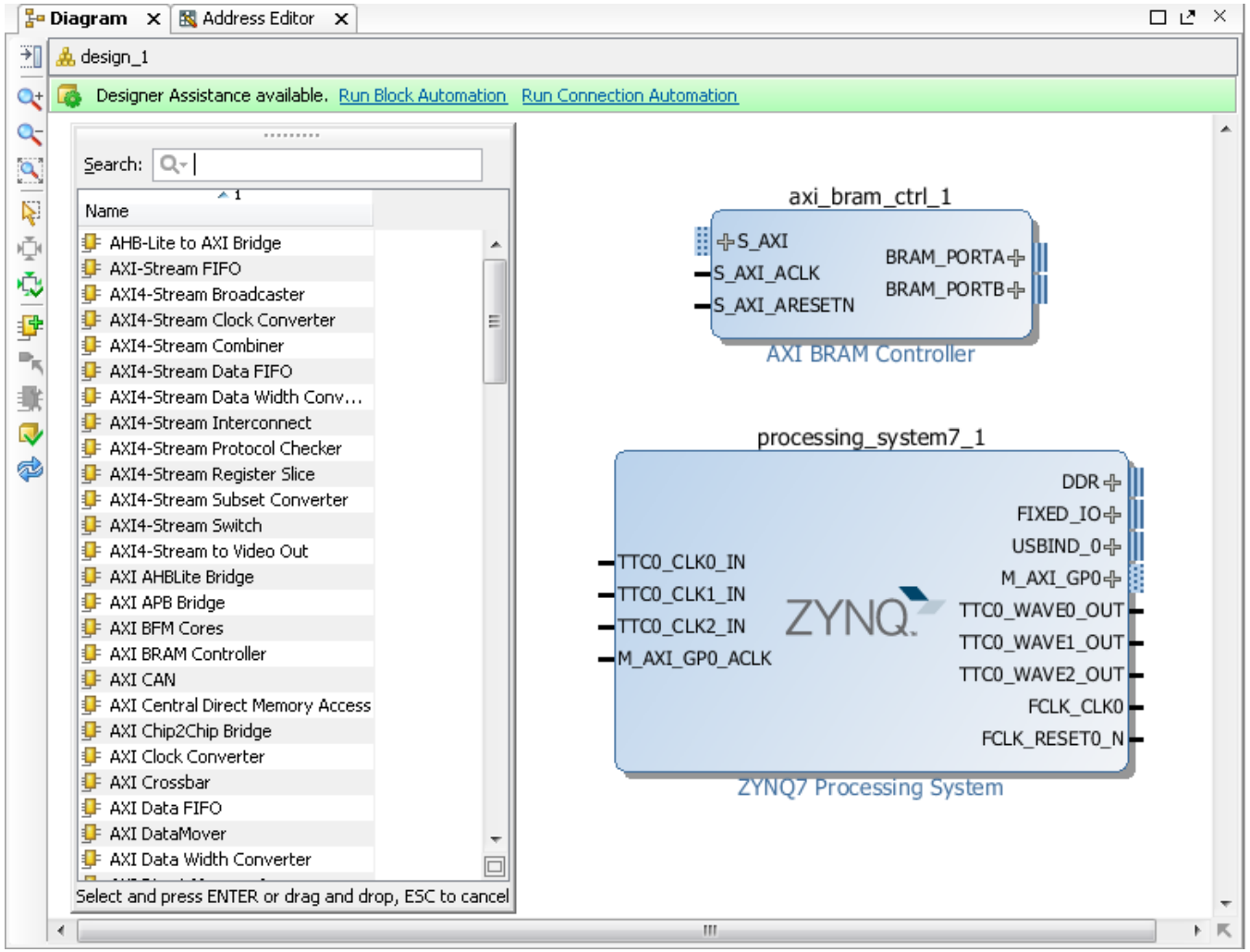


Embedded System Design using Vivado



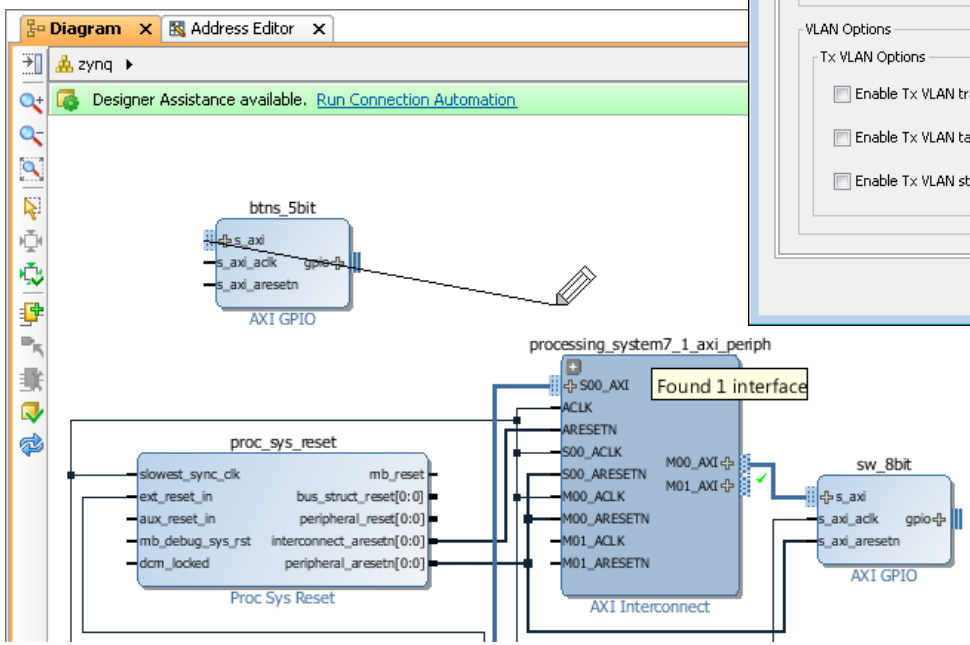
Integrator Block Diagram

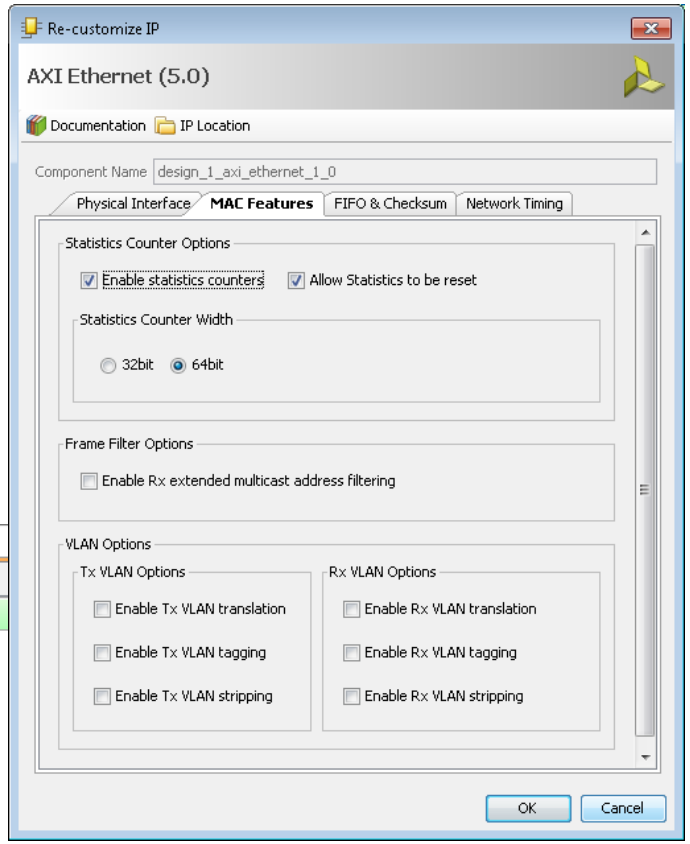
- **IP Integrator Block Diagram opens a blank canvas**
- **IP can be added from the IP catalog**
- **Drag and drop interface**
- **Intelligent Design environment**
  - Design Assistance
  - Connection automation
  - Highlights valid connections
  - Group, create hierarchal blocks
- **Can create and import custom IP using IP Packager**



Configuring Hardware in IP Integrator

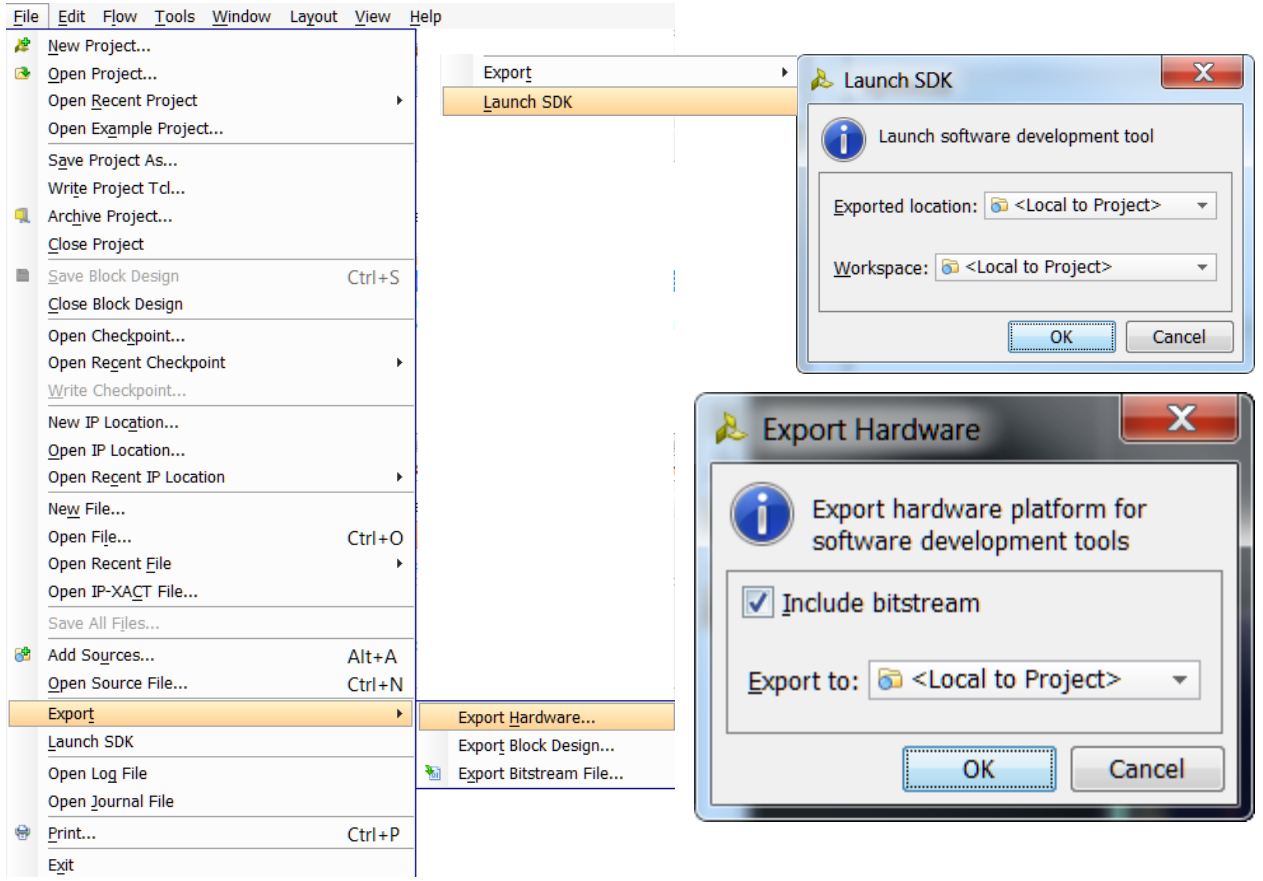
- **Double click blocks to access configuration options**
- **Drag pointer to make connections**
  - Highlights valid connections
- **Connection Automation**
  - Automatically connect recognised interfaces
- **Automatically Redraw system**





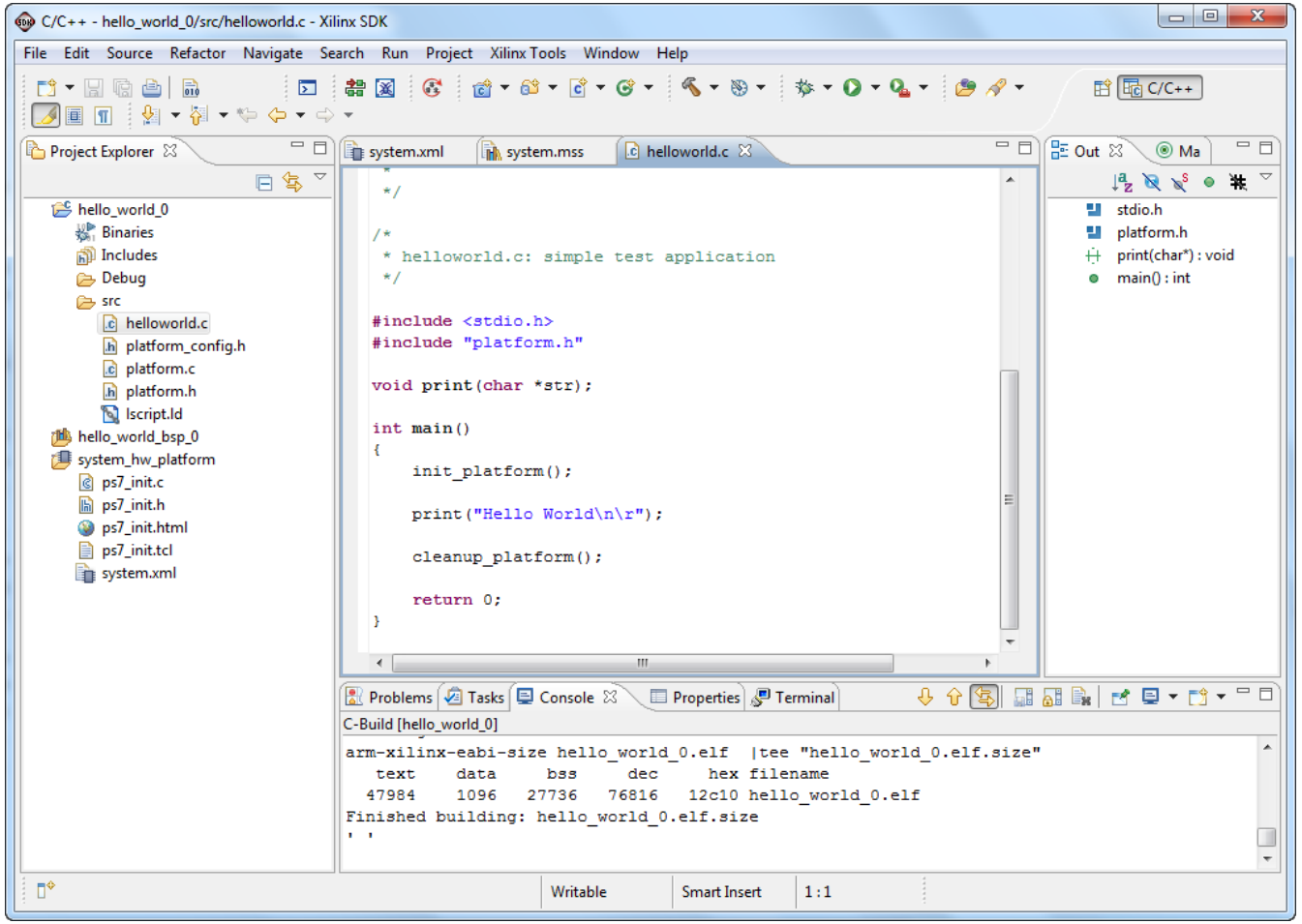
Exporting to SDK

- **Export hardware first**
  - The Hardware Description File (hdf) format file containing all the relevant information will be created and placed under the *.sdk directory
  - Include bitstream if generated
- **Launch SDK**
  - Software development is performed with the Xilinx Software Development Kit tool (SDK)
- **The SDK tool will then associate user software projects to hardware**



Software Development Flow

- **Create hardware platform project**
  - Automatically performed when SDK tool is launched from Vivado project
- **Create BSP**
  - System software, board support package
- **Create software application**
- **Create linker script**
- **Build project**
  - compile, assemble, link output file *<app_project>.elf*



References

- **Zynq ebook Chapter 1.**