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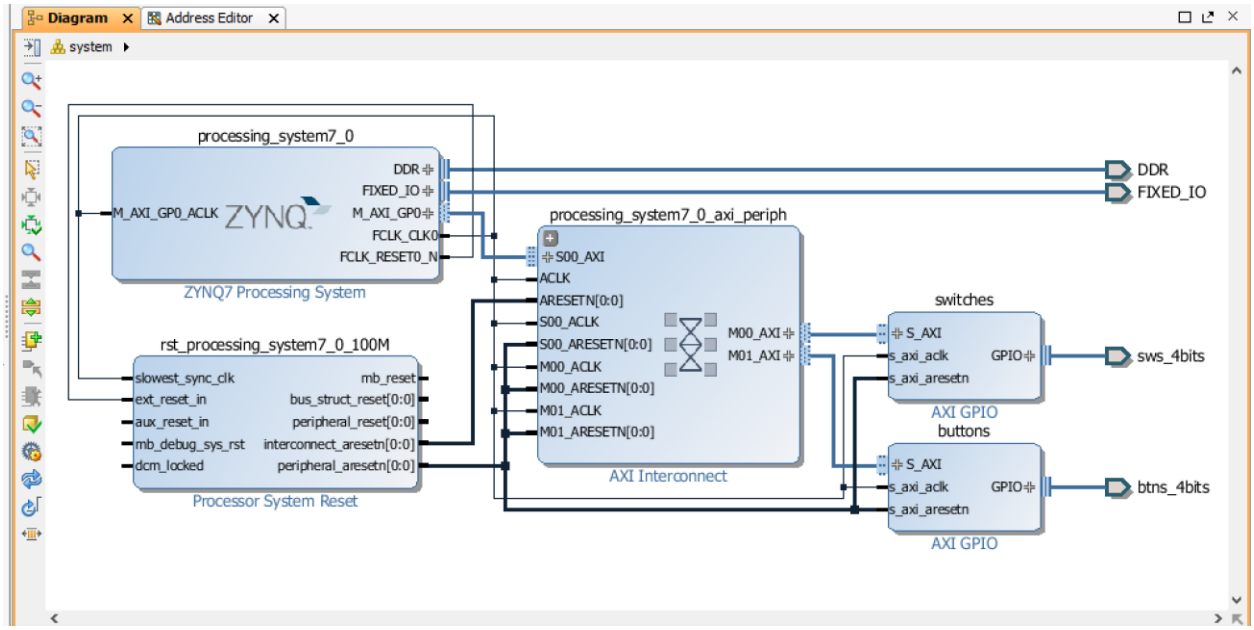
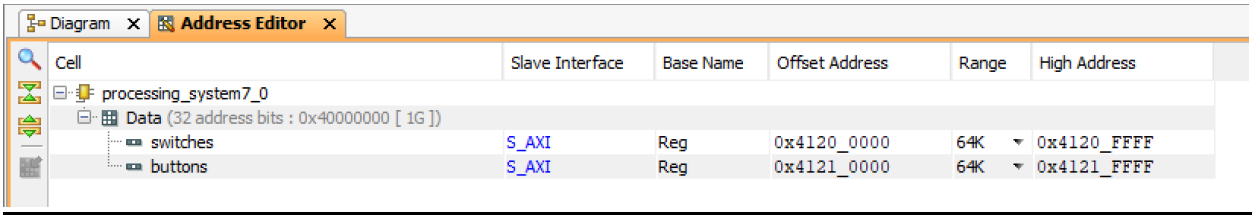
CECS 461

Lab 2

Block Design



Peripheral Memory Map



Cell	Slave Interface	Base Name	Offset Address	Range	High Address
processing_system7_0					
Data (32 address bits : 0x40000000 [1G])					
switches	S_AXI	Reg	0x4120_0000	64K	0x4120_FFFF
buttons	S_AXI	Reg	0x4121_0000	64K	0x4121_FFFF

System.mss File

```
 PARAMETER HW_INSTANCE = ps7_ram_1
 END

 BEGIN DRIVER
  PARAMETER DRIVER_NAME = generic
  PARAMETER DRIVER_VER = 2.0
  PARAMETER HW_INSTANCE = ps7_scuc_0
 END

BEGIN DRIVER
 PARAMETER DRIVER_NAME = scugic
 PARAMETER DRIVER_VER = 3.0
 PARAMETER HW_INSTANCE = ps7_scugic_0
END

BEGIN DRIVER
 PARAMETER DRIVER_NAME = scutimer
 PARAMETER DRIVER_VER = 2.1
 PARAMETER HW_INSTANCE = ps7_scutimer_0
END

BEGIN DRIVER
 PARAMETER DRIVER_NAME = scuwdt
 PARAMETER DRIVER_VER = 2.1
 PARAMETER HW_INSTANCE = ps7_scuwdt_0
END

BEGIN DRIVER
 PARAMETER DRIVER_NAME = generic
 PARAMETER DRIVER_VER = 2.0
 PARAMETER HW_INSTANCE = ps7_slcr_0
END

BEGIN DRIVER
 PARAMETER DRIVER_NAME = uartps
 PARAMETER DRIVER_VER = 3.0
 PARAMETER HW_INSTANCE = ps7_uart_1
END

BEGIN DRIVER
 PARAMETER DRIVER_NAME = xadcps
 PARAMETER DRIVER_VER = 2.2
 PARAMETER HW_INSTANCE = ps7_xadc_0
END

BEGIN DRIVER
 PARAMETER DRIVER_NAME = gpio
 PARAMETER DRIVER_VER = 4.0
 PARAMETER HW_INSTANCE = switches
END
```

1) **List all major operations in Step 2 & 3 in Lab 2 manual**
    - Enable AXI_M_GP0 interface, FCLK_RESET0_N, , and FCLK_CLK0 ports, Add two instances of a GPIO Peripheral from the IP catalog to the processor system.
    - The push button and dip switch instances will be connected to corresponding pins on the board. This can be done manually or using Designer Assistance. Normally, one would consult the board's user manual to find this information.

2) **At which step the Vivado tool generates xparameter.h? Does Lab 1 and Lab 2 have the same xparameter.h? If different, Please describe the major difference. If the same, explain why.**

    In step 5-1-9, is when the library generator will run in the background and will create the xparameter.h. In lab 1 we did not have xparameter.h

3) **What is the difference between Lab 1 and Lab 2 when we export hardware platform from Vivado IP integrator to SDK?**

    When we export the hardware platform, we had to include the bitsteam.

4) **Describe the difference between Lab 1 and Lab 2 for running the application program.**

    The difference is in Lab 2 we must program the FPGA and then run the Programming System. In Lab 1 we only run the Programming System.